NTEGRATED CIRCUITS

Multimedia ICs

1997

Data Handbook IC22

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Short-form specification	The data in this specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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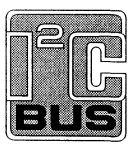

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

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DACs

TYPE NUMBER	RESOLUTION (BITS)	CONVERSION RATE MAX. (Msps)	DNL RAMP INPUT AT MAX. SPEED (LSB)	SFDR[1]	DISSIPATION (mW)	SUPPLY VOLTAGE AND I/O	PACKAGE	FEATURES/ REMARKS
8-bit								
TDA8702	8	30	±0.5	–52 (4.43)	250	5 V; TTL	DIP16, SO16L	–
TDA8712	8	50	±0.5	–52 (4.43)	250	5 V; TTL	DIP16, SO16L	–
TDF8712	8	50	±0.5	–52 (4.43)	250	5 V; TTL	DIP16, SO16L	–40 to +85 °C
TDA8771	3 × 8	35	±0.5	–50 (4.43)	200	5 V; TTL	QFP44	3 V output; 1 kΩ load
TDA8772/A	3 × 8	85	±0.5	–50 (4.43)	405	5 V; TTL	QFP44	1 V output; 75 Ω load
10-bit								
TDA8775	3 × 10	50	±0.5	–55 (4.43)	395	5 V; TTL	LQFP48	0.7 V output; 37.5 Ω or 150 Ω load
TDA8776	10	500	±0.2	–68 (10)	925	–5.2 V; ECL	PLCC28	internal reference; 50 Ω output load
TDA8776A	10	1000	±0.2	–60 (50)	925	–5.2 V; ECL	PLCC28	internal reference; 50 Ω output load

Notes

1. SFDR measured at maximum speed; value in brackets is output rate in MHz.

AUDIO POWER AMPLIFIERS

PART	POWER	GAIN (dB)	THD (%)	FEATURES	PACKAGE	V_s (V)
TDA1308; TDA1308T	2 × 60 mW headphone amplifier	–	–	short-circuit	SOT97–1; SOT96–1	3 to 7
TDA1517 TDA1517P	2 × 6 W	20	0.1	mute; short-circuit; standby	SOT110-1 HDIP18	8.5 to 18
TDA1519	2 × 6 W	40	0.1	mute; short-circuit; standby	SOT110-1;	8.5 to 18
TDA2615	2 × 6 W hi-fi	30	0.15	mute; short-circuit	SOT110-1	±7.5 to ±21 or 15 to 42
TDA2616; TDA2616Q	2 × 12 W hi-fi	30	0.15	mute; short-circuit	SOT131-2; SOT157-2	±7.5 to ±21 or 15 to 42
TDA7053A	2 × 1 W	40	0.3	volume control; mute; short-circuit	SOT38-1; SOT162-1	4.5 to 18
TDA7057AQ	2 × 5 W	40	0.3	volume control; mute; short-circuit	SOT141-6	4.5 to 18
TDA8542	2 × 1 W	30	0.15	standby; mute	SOT38-1; SOT162-1	2.2 to 18
TDA8559; TDA8559T	2 × 35 mW or 1 × 140 mW headphone amplifier	–	–	mute; standby	–	1.9 to 30

AUDIO STEREO DECODERS

TYPE	FEATURES	VARIOUS	PACKAGE
TDA9850	BTSC stereo decoder	dBX noise reduction	SDIP32/SO32
TDA9852	BTSC stereo decoder + volume control	dBX noise reduction	SDIP42
TDA9855	BTSC stereo decoder + audio processing	dBX noise reduction	SDIP52/PLCC68
TEA5582	BTSC stereo decoder (low cost)	except dBX noise reduction	DIP20

PHILIPS MONITOR ICs

FUNCTION	TYPE	DESCRIPTION	REMARKS	PACKAGE	STATUS
H + V deflection controller	TDA4850	advanced concept for VGA/XGA monitors	up to 40 kHz; DC-controllable/DC-coupled	DIP20	mass production
	TDA4851	advanced concept for VGA/multifrequency monitors	low jitter DC-controllable/DC-coupled up to 100 kHz	DIP20	mass production
	TDA4852	advanced concept for multifrequency monitors/no VGA on chip	low jitter DC-controllable/DC-coupled up to 100 kHz	DIP20	mass production
	TDA4855	autosync deflection controller	extensive geometry control; F/V converter; flexible switched B +supply function block; dynamic focus; X-ray protection; up to 100 kHz DC-controllable	SDIP32	mass production
	TDA4858	economy autosync deflection controller	TDA4855 without: VGA dynamic focus smoothed top of EW parabola	SDIP32	mass production
Vertical booster	TDA4860	half bridge	<15" monitor; I_{max} = 2.0 A	SIL9MP	mass production
	TDA4861	half bridge	>17" monitor; I_{max} = 2.8 A	SIL9P	mass production
	TDA4866	full bridge	<15" monitor; I_{max} = 2.0 A	SIL9P	mass production
	TDA8351	full bridge	>17" monitor; I_{max} = 3.0 A	SIL9P	mass production
Video amplification	TDA4881	3-channel preamplifier fully DC controllable	70 MHz min./3 dB; 2-gain controls; grey scale tracking	DIP20	mass production
	TDA4882	3-channel preamplifier for OSD/85 MHz fully DC controllable	better HF-stability; less overshoot; easy application; good tracking of contrast/brightness; grey scale tracking; 2-gain controls	DIP20	mass production
	TDA4884	3-gain control version of TDA4882 for ACCU colour/85 MHz	incorporates same improvements as TDA4882 except: no grey scale tracking brightness via grid 1	DIP20	mass production
	TDA4885	3-channel preamplifier with I^2C-bus control	150 MHz pixel rate; grey scale tracking; gain modulation for brightness uniformity; OSD mixer; universal output stage	SDIP32	mass production

SELECTION TABLE FOR TELETEXT AND CLOSED CAPTION

TYPE	NO. OF PAGES	ACQUISITION CHANNELS	LANGUAGE/REGION	OTHER FEATURES(1)	PACKAGE
SAA5246A	8 external	4	All WST	PC Text software compatible. External 8K8 SRAM for page storage	QFP64 or DIP48
SAA5249	500 external	1	By region	PC Text software compatible single chip teletext decoder containing data slicer, acquisition display driver	QFP64 or DIP48
SAA5252	Display Line 21 Closed Captioning data. Allows full page text mode	1	FCC compliant	Stand-alone or I^2C-bus controlled line 21 closed captioning decoder with on-chip display RAM and OSD facility	SO24 or DIP24
SAA5254	1	1	By region	PC Text software compatible single chip decoder supporting Fastext/FLOF, 1.1K × 8 on-chip RAM	QFP64 or DIP40
SAA5281	8 internal	4	All WST	PC Text software compatible, 8K × 8 on-chip RAM. Fastext/FLOF and TOP	QFP64 or SDIP52
SAA5296	10 internal	10	All WST	Embedded 80C51 microcontroller, 32K internal ROM tuner control functions and 32 characters OSD	QFP80 or SDIP52
PC Text(1)	–	–	–	Intelligent page acquisition and caching gives quick response to users. Level 1.5 teletext. Window class can be used as main window or as a control. Works with Windows 3.1, Windows 3.11 and Windows 95	–

Note

1. PC Text is a new software product which has been developed for multimedia applications. The software, which is available under licence, consists of a number of Windows Dynamic Link Libraries (DLLs) providing functions and a window class to facilitate rapid development of teletext applications on PCs.

A HIGH-SPEED CONVERTER FOR EVERY APPLICATION

ADCs and front-ends

TYPE NUMBER	RESOLUTION (BITS)	CONVERSION RATE MAX. (Msps)	DNL RAMP INPUT AT MAX. SPEED (LSB)	ENOB[1]	DISSIPATION (mW)	SUPPLY VOLTAGE AND I/O	PACKAGE	FEATURES/ REMARKS
6-bit								
TDA8705	2 × 6	40	±0.25	5.8 (10)	250	5 V; TTL	SO28	internal reference
TDA8705A	2 × 6	80	±0.25	5.8 (20)	250	5 V; TTL	SO28	internal reference
TDA8706	6	20	±0.5	5.7 (4.43)	300	5 V; TTL	DIP20, SO20	analog YUV, MUX
TDA8706A	6	40	±0.2	5.8 (4.43)	36	2.7 to 5.5 V; TTL	SSOP24	analog RGB, MUX; –40 to +85 °C
TDA8707	3 × 6	35	±0.35	5.3 (4.43)	335	5 V; TTL	QFP44	RGB inputs; –40 to +85 °C
8-bit								
TDA8703	8	40	±0.5	7.1 (4.43)	290	5 V; TTL	DIP24, SO24	see TDA8790 (new device)
TDA8708A	8	32	±0.5	6.7 (4.43)	365	5 V; TTL	DIP28, SO28	CVBS and Y inputs; AGC and clamp
TDA8709A	8	32	±0.5	6.7 (4.43)	380	5 V; TTL	DIP28, SO28	U, V, C, RGB inputs; gain control and clamp inputs
TDA8714	8	75	±0.2	7.7 (4.43) 7.2 (10)	340	5 V; TTL	SO24, SSOP24	40, 60 and 75 Msps versions
TDA8716	8	120	±0.25	7.5 (10)	780	–5.2 V; ECL	DIP24, SO32	–
TDA8718	8	600	±0.3	6.5 (100)	990	–5.2 V; ECL	PLCC28	–
TDA8752[2]	3 × 8	80	±0.5	7.0 (4.43)	1000	5 V; TTL	QFP100	100 MHz gain amp; PLL; clamp; I²C-bus
TDA8753A	3 × 8	20	±0.5	7.2 (4.43)	500	5 V; TTL	SDIP42	clamp; YUV: 4 : 1 : 1
TDA8755	3 × 8	20	±0.3	7.1 (4.43)	550	5 V; TTL	SO32	clamp; YUV: 4 : 1 : 1
TDA8758	2 × 8	32	±0.4	7.1 (4.43)	530	5 V; TTL	LQFP48	Y/C interface
TDA8785	8 (+8-bit DAC)	30	±0.4	7.0 (4.43)	600	5 V; TTL	QFP44	100 MHz gain amp; fast offset amp.

TYPE NUMBER	RESOLUTION (BITS)	CONVERSION RATE MAX. (Msps)	DNL RAMP INPUT AT MAX. SPEED (LSB)	ENOB[1]	DISSIPATION (mW)	SUPPLY VOLTAGE AND I/O	PACKAGE	FEATURES/ REMARKS
TDA8790	8	40	±0.25	7.3 (4.43)	30	2.7 to 5.5 V; CMOS	SSOP20	4 mW standby
TDA8792	8	25	±0.3	7.3 (4.43) 7.0 (10)	53	3.3 V; TTL	SSOP24	30 MHz input bandwidth
TDF8704	8	50	±0.2	7.4 (4.43)	380	5 V; TTL	SO24	–40 to +85 °C; for automotive
9-bit								
TDA8761A	9	40	±0.3	8.2 (10)	185	5 V/3 V; TTL	SSOP28	256 QAM
10-bit								
TDA8760	10	40	±0.6	8.2 (10)	850	5 V; TTL	PLCC44	220 MHz input at –3 dB
TDA8762A	10	80	±0.3	9.3 (4.43)	380	5 V; TTL	SSOP28	60 and 80 Msps versions
TDA8763	10	50	±0.5	9.2 (4.43)	240	5 V/3 V; TTL	SSOP28	internal ref.; 30, 40 and 50 Msps versions
TDA8763A	10	50	±0.5	9.2 (4.43)	195	5 V/3 V; TTL	SSOP28	30, 40 and 50 Msps versions
TDA8766	10	20	±0.25	9.3 (10)	53	2.7 to 5.25 V; CMOS	LQFP32	5 × 5 × 1.4 mm package
TDA8779[2]	2 × 10 (+2 × 10 DAC)	20	±0.5	9.2 (5.0)	520	5 V/3 V; TTL	QFP44	quadrature transceiver for telecom
TDA8786	10 (+CDS + AGC); note 3	18	±0.5	9.0 (4.43)	400	5 V/3 V; TTL	LQFP48	control DAC with 3-wire interface
12-bit								
TDA8767	12	30	±0.75	–	335	5 V/3 V; TTL	QFP44	differential or single input

Notes

1. Effective Number Of Bits (ENOB) measured at maximum speed; value in brackets is the input rate in MHz.
2. In development; production 1Q 97.
3. Correlated Double Sampling (CDS).

DIGITAL VIDEO DECODERS

Device	Colour standards	Input formats	ADC	Clock generator	Output formats	Output pixels	Special features	Package
SAA7110(A)	NTSC PAL SECAM	up to 6 × CVBS or 3 × Y/C	internal (anti-alias filters)	internal	16-bit YUV 4 : 2 : 2 12-bit YUV 4 : 1 : 1	square 8-bit	BCS control, picture inversion, real time control	PLCC68
SAA7111	NTSC PAL	up to 4 × CVBS or 2 × Y/C	internal (anti-alias filters)	internal	16-bit YUV 4 : 2 : 2 12-bit YUV 4 : 1 : 1 8-bit CCIR 656 16-bit RGB	CCIR 8-bit	BCS control, line 21 text slicer, boundary scan test	PLCC68 QFP64
SAA7111A	NTSC PAL SECAM	up to 4 × CVBS or 2 × Y/C	internal (anti-alias filters)	internal	16-bit YUV 4 : 2 : 2 12-bit YUV 4 : 1 : 1 8-bit CCIR 656 24-bit & 16-bit RGB	CCIR 8-bit	BCS control, VBI bypass, boundary scan test	PLCC68 QFP64 LQFP64
SAA7112	NTSC PAL SECAM	up to 6 × CVBS or 3 × Y/C 16-bit YUV 8-bit CCIR 656	internal (anti-alias filters)	internal	16-bit YUV 4 : 2 : 2 12-bit YUV 4 : 1 : 1 8-bit YUV 4 : 1 : 0 8-bit CCIR 656	CCIR 8-bit	high performance scaler, universal VBI data slicer, expansion & image port, scan rate conversion	LQFP100
SAA7151B	NTSC PAL SECAM	up to 2 × CVBS or 4 × Y/C	external (TDA8758)	external (SAA7157)	16-bit YUV 4 : 2 : 2 12-bit YUV 4 : 1 : 1	CCIR 8-bit	SCART interface, optional external comb filter	PLCC68
SAA7191B	NTSC PAL SECAM	up to 2 × CVBS or 1 × Y/C	external (TDA8758)	external (SAA7197)	16-bit YUV 4 : 2 : 2 12-bit YUV 4 : 1 : 1	square 8-bit		PLCC68
SAA7196	NTSC PAL SECAM	up to 2 × CVBS or 1 × Y/C 16-bit YUV	external (TDA8758)	internal	16-bit YUV 4 : 2 : 2 24-bit RGB 15-bit RGB 8-bit monochrome	square 8-bit	scaler, expansion port, BCS control	LQFP120

DIGITAL VIDEO ENCODERS

Device	Colour standards	Input formats	Input pixels	Macro-vision	Closed caption teletext	DACs	Output formats	Control	Special features	Package
SAA7124	NTSC PAL	8-bit CCIR 656	CCIR 8-bit	rev. 6	yes yes	4 10-bit 2× ovs.	CVBS, Y/C RGB YUV	fast I²C-bus, advanced remote genlock	2 CVBS + 1 Y/C output signals simultaneously	PLCC84 QFP80 LQFP64
SAA7125	NTSC PAL	8-bit CCIR 656	CCIR 8-bit	no	yes yes	4 10-bit 2× ovs.	CVBS, Y/C RGB YUV	fast I²C-bus, advanced remote genlock	2 CVBS + 1 Y/C output signals simultaneously	PLCC84 QFP80 LQFP64
SAA7182	NTSC PAL SECAM	8-bit CCIR 656 16-bit YUV 4 : 2 : 2	CCIR 8-bit	no	yes yes	6 10-bit 2× ovs.	CVBS, Y/C RGB	fast I²C-bus, advanced remote genlock	colour matrix	PLCC84
SAA7182A	NTSC PAL SECAM	8-bit CCIR 656 16-bit YUV 4 : 2 : 2	CCIR 8-bit	no	yes yes	6 10-bit 2× ovs.	CVBS, Y/C RGB YUV	fast I²C-bus, advanced remote genlock	analog RGB MUX, 16 : 9 signalling, 5 V/3.3 V core	PLCC84 QFP80
SAA7183	NTSC PAL SECAM	8-bit CCIR 656 16-bit YUV 4 : 2 : 2	CCIR 8-bit	rev. 6	yes yes	6 10-bit 2× ovs.	CVBS, Y/C RGB	fast I²C-bus, advanced remote genlock	colour matrix	PLCC84
SAA7183A	NTSC PAL SECAM	8-bit CCIR 656 16-bit YUV 4 : 2 : 2	CCIR 8-bit	rev. 6	yes yes	6 10-bit 2× ovs.	CVBS, Y/C RGB YUV	fast I²C-bus, advanced remote genlock	analog RGB MUX, 16 : 9 signalling, 5 V/3.3 V core	PLCC84 QFP80
SAA7184	NTSC PAL	8-bit CCIR 656 16-bit YUV 4 : 2 : 2	CCIR 8-bit	rev. 6	yes no	3 10-bit 2× ovs.	CVBS, Y/C	I²C or MPU-bus, remote genlock	cross colour reduction	PLCC68
SAA7185(B)	NTSC PAL	8-bit CCIR 656 16-bit YUV 4 : 2 : 2	CCIR 8-bit	no	yes no	3 10-bit 2× ovs.	CVBS, Y/C	I²C or MPU-bus, remote genlock	cross colour reduction	PLCC68
SAA7187	NTSC PAL	8-bit CCIR 656 16-bit YUV 4 : 2 : 2 24-bit YUV 4 : 4 : 4	square 8-bit	no	yes no	3 10-bit 2× ovs.	CVBS, Y/C	I²C or MPU-bus, remote genlock	cross colour reduction	PLCC68
SAA7199B	NTSC PAL	16-bit YUV 4 : 2 : 2 24-bit YUV 4 : 4 : 4 24-bit RGB	CCIR & square 8-bit	no	no no	3 9-bit 1× ovs.	CVBS, Y/C	I²C or MPU-bus, on-chip genlock	LUT 3 × 256 × 8-bit, still video capturing	PLCC84

Internet World Wide Web Home Page

WHAT IS IT?

Welcome to our place in cyberspace.

The Multimedia Group now has its own home page within Philips Semiconductors. Explore our Web pages and take a look at our product offering of advance High-performance Digital Video and Audio Processing Applications and Products.

In addition we offer you the latest information on Products, News, Support, Employment and Offices.

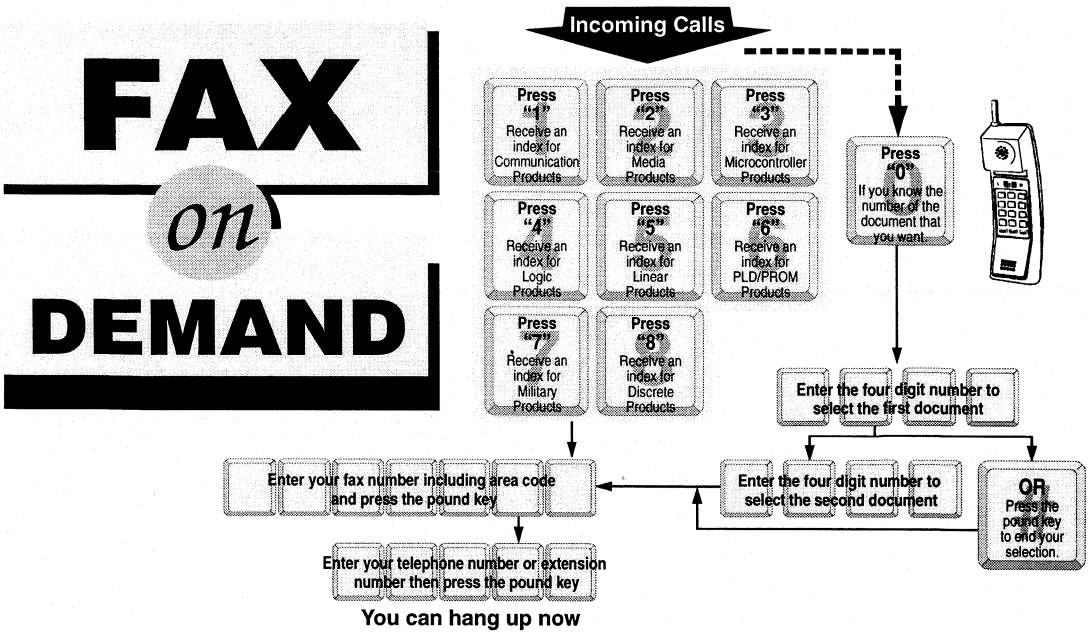
HOW TO REACH US

For access to the Philips Semiconductors Home Page go to the World Wide Web location:

http://www.semiconductors.philips.com/

You can find us in the Product category of Multimedia Products.

FAX-on-DEMAND System



What is it?

The FAX-on-DEMAND system is a computer facsimile system that allows customers to receive selected documents by fax automatically.

How does it work?

To order a document, you simply enter the document number. This number can be obtained by asking for an index of available documents to be faxed to you the first time you call the system.

Our system has a selection of the latest product data sheets from Philips with varying page counts. As you know, it takes approximately one minute to FAX one page. This isn't bad if the number of pages is less than 10. But if the document is 37 pages long, be ready for a long transmission!

Philips Semiconductors also maintains product information on the World-Wide Web. Our home page can be located at:
http://www.semiconductors.philips.com

Who do I contact if I have a question about FAX-on-DEMAND?

Contact your local Philips sales office.

FAX-on-DEMAND phone numbers:

England (United Kingdom, Ireland)	44-181-730-5020
France	33-1-40-99-60-60
Germany (Austria, Switzerland)	49-40-23536-357
Italy	39-167-295502
North America	1-800-282-2000

Locations soon to be in operation:

Hong Kong
Japan
The Netherlands

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MEDIA COMPONENTS PRODUCTS
PREFIXES PC, SA, TD, TE, TS, UA, UM

Example: TD A XXXX P N

Device Family
- PCx = CMOS Circuit
- SAx = Digital Circuit
- TDx = Linear Circuit
- TEx = Linear Circuit
- TSx = Analog Circuit
- UAx = Digital Circuit
- UMx = Digital Circuit

Package Code:
- A = Plastic Leaded Chip Carrier (PLCC)
- B = Quad Flat Pack (QFP)
- N = Plastic Dual In-Line
- D = Plastic SO
- F = Ceramic Dual In-Line
- U = Plastic Single In-Line

Package Code on Part:
- GP = Quad Flat Pack (QFP)
- P = Plastic Dual In-Line
- T = Plastic SO
- D = Ceramic Dual In-Line
- WP = Plastic Leaded Chip Carrier (PLCC)

Device Number

Operating Temperatures:
- A = Temperature range not specified (see data sheet)
- B = 0 to +70°C
- C = –55°C to +125°C
- D = –25°C to +70°C
- E = –25°C to +85°C
- F = –40°C to +85°C

TOTAL QUALITY MANAGEMENT

Philips Semiconductors is a Quality Company, renowned for the high quality of our products and service. We keep alive this tradition by constantly aiming towards one ultimate standard, that of zero defects. This aim is guided by our Total Quality Management (TQM) system, the basis of which is described in the following paragraphs.

Quality assurance

Based on ISO 9000 standards, customer standards such as Ford TQE and IBM MDQ. Our factories are certified to ISO 9000 by external inspectorates.

Partnerships with customers

PPM co-operations, design-in agreements, ship-to-stock, just-in-time and self-qualification programmes, and application support.

Partnerships with suppliers

Ship-to-stock, statistical process control and ISO 9000 audits.

Quality improvement programme

Continuous process and system improvement, design improvement, complete use of statistical process control, realization of our final objective of zero defects, and logistics improvement by ship-to-stock and just-in-time agreements.

ADVANCED QUALITY PLANNING

During the design and development of new products and processes, quality is built-in by advanced quality planning. Through failure-mode-and-effect analysis the critical parameters are detected and measures taken to ensure good performance on these parameters. The capability of process steps is also planned in this phase.

PRODUCT CONFORMANCE

The assurance of product conformance is an integral part of our quality assurance (QA) practice. This is achieved by:

- Incoming material management through partnerships with suppliers.
- In-line quality assurance to monitor process reproducibility during manufacture and initiate any necessary corrective action. Critical process steps are 100% under statistical process control.
- Acceptance tests on finished products to verify conformance with the device specification. The test results are used for quality feedback and corrective actions. The inspection and test requirements are detailed in the general quality specifications.
- Periodic inspections to monitor and measure the conformance of products.

PRODUCT RELIABILITY

With the increasing complexity of Original Equipment Manufacturer (OEM) equipment, components reliability must be extremely high. Our research laboratories and development departments study the failure mechanisms of semiconductors. Their studies result in design rules and process optimization for the highest built-in product reliability. Highly accelerated tests are applied to the product reliability evaluation. Rejects from reliability tests and from customer complaints are submitted to failure analysis, to result in corrective action.

CUSTOMER RESPONSES

Our quality improvement depends on joint action with our customer. We need our customer's inputs and we invite constructive comments on all aspects of our performance. Please contact our local sales representative.

RECOGNITION

The high quality of our products and services is demonstrated by many Quality Awards granted by major customers and international organizations.

BASIC TYPE NUMBER

This type designation code applies to semiconductor monolithic, semiconductor multi-chip, thin film, thick film and hybrid integrated circuits. The basic type number comprises three letters followed by a serial number.

First and second letters

DIGITAL FAMILY CIRCUITS

The first two letters identify the family.(1)

SOLITARY CIRCUITS

The first letter divides solitary circuits into:

S Solitary digital circuits

T Analog circuits

U Mixed analog/digital circuits.

The second letter is a serial letter without any further significance except 'H' which stands for hybrid circuits.(2)

MICROPROCESSORS

The first two letters identify microprocessors and related circuits:

MA Microcomputer or central processing unit

MB Slice processor (functional slice of microprocessor)

MD Related memories

ME Other related circuits such as interfaces, clocks, peripheral controllers, etc.

CHARGE-TRANSFER DEVICES AND SWITCHED CAPACITORS

The first two letters identify:

NH Hybrid circuits

NL Logic circuits

NM Memories

NS Analog signal processing using switched capacitors

NT Analog signal processing using charge-transfer devices

NX Imaging devices

NY Other related circuits.

(1) A logic family is an assembly of digital circuits designed to be interconnected and defined by its base electrical characteristics, such as supply voltage, power consumption, propagation delay, noise immunity.

(2) The first letter 'S' should be used for all solitary memories, to which, in the event of hybrids, the second letter 'H' should be added, for example, SH for bubble memories.

Third letter

The third letter indicates the operating ambient temperature range:

A temperature range not specified below

B 0 to +70 °C

C −55 to +125 °C

D −25 to +70 °C

E −25 to +85 °C

F −40 to +85 °C

G −55 to +85 °C.

If a device has another temperature range, the letter 'A' or a letter indicating a narrower temperature may be used, for example, the range of 0 to +75 °C can be indicated by 'A' or 'B'. Should two devices with the same basic type number both have temperature ranges other than those specified, one would use the letter 'A' and the other the letter 'X'.

SERIAL NUMBER

This may be a four-digit number assigned by Pro Electron, or the serial number (which may be a combination of figures and letters) of an existing company type designation of the manufacturer.

VERSION LETTER

A single version letter may be added to the basic type number. This indicates a minor variant of the basic type or the package. The version letter has no fixed meaning except for 'Z' which means customized wiring. The following letters are recommended for package variants:

C Cylindrical

D Ceramic dual in-line (CERDIL, CERDIP)

F Flat pack (two leads)

G Flat pack (four leads)

H Quad flat pack (QFP)

L Chip on tape (foil)

P Plastic dual in-line (DIL)

Q Quad in-line (QUIL)

T Mini pack (SOL, SO, VSO)

U Uncased chip.

TWO-LETTER SUFFIX

A two-letter suffix may be used instead of a single package version letter to give more information. To avoid confusion with serial numbers that end with a letter, a hyphen should precede the suffix.

First letter (general shape)

C Cylindrical
D Dual in-line (DIL)
E Power DIL (with external heatsink)
F Flat pack (leads on two sides)
G Flat pack (leads on four sides)
H Quad flat pack (QFP)
K Diamond (TO-3 family)
M Multiple in-line (except dual, triple and quad)
Q Quad in-line (QUIL)
R Power QUIL (with external heatsink)
S Single in-line (SIL)
T Triple in-line
W Leaded chip carrier (LCC)
X Leadless chip carrier (LLCC)
Y Pin grid array (PGA).

Second letter (material)

C Metal-ceramic
G Glass-ceramic
M Metal
P Plastic.

EXAMPLES

PCF1105WP: digital IC; PC family; operating temperature range −40 to +85 °C; serial number 1105; plastic leaded chip carrier.

GMB74LS00A-DC: digital IC; GM family; operating temperature range 0 to +70 °C; company number 74LS00A; ceramic DIL package.

TDA1000P: analog IC; operating temperature range non-standard; serial number 1000; plastic DIL package.

SAC2000: solitary digital circuit; operating temperature range −55 to +125 °C; serial number 2000.

RATING SYSTEMS

The rating systems described are those recommended by the IEC in its publication number 134.

Definitions of terms used

ELECTRONIC DEVICE

An electronic tube or valve, transistor or other semiconductor device. This definition excludes inductors, capacitors, resistors and similar components.

CHARACTERISTIC

A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

BOGEY ELECTRONIC DEVICE

An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics that are directly related to the application.

RATING

A value that establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms. Limiting conditions may be either maxima or minima.

RATING SYSTEM

The set of principles upon which ratings are established and which determine their interpretation. The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

Absolute maximum rating system

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type, as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout the life of the device, no absolute maximum value for the intended service is exceeded with any device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

Design maximum rating system

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design to that, initially and throughout the life of the device, no design maximum value for the intended service is exceeded with a bogey electronic device, under the worst probable conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

Design centre rating system

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

ELECTROSTATIC CHARGES

Electrostatic charges can exist in many things; for example, man-made-fibre clothing, moving machinery, objects with air blowing across them, plastic storage bins, sheets of paper stored in plastic envelopes, paper from electrostatic copying machines, and people. The charges are caused by friction between two surfaces, at least one of which is non-conductive. The magnitude and polarity of the charges depend on the different affinities for electrons of the two materials rubbing together, the friction force and the humidity of the surrounding air.

Electrostatic discharge is the transfer of an electrostatic charge between bodies at different potentials and occurs with direct contact or when induced by an electrostatic field. All of our MOS devices are internally protected against electrostatic discharge but they **can** be damaged if the following precautions are not taken.

WORK STATION

Figure 1 shows a working area suitable for safely handling electrostatic sensitive devices. It has a work bench, the surface of which is conductive or covered by an antistatic sheet. Typical resistivity for the bench surface is between 1 and 500 kΩ per cm^2. The floor should also be covered with antistatic material. The following precautions should be observed:

- Persons at a work bench should be earthed via a wrist strap and a resistor.
- All mains-powered electrical equipment should be connected via an earth leakage switch.
- Equipment cases should be earthed.
- Relative humidity should be maintained between 50 and 65%.
- An ionizer should be used to neutralize objects with immobile static charges.

RECEIPT AND STORAGE

MOS devices are packed for dispatch in antistatic/conductive containers, usually boxes, tubes or blister tape. The fact that the contents are sensitive to electrostatic discharge is shown by warning labels on both primary and secondary packing.

The devices should be kept in their original packing whilst in storage. If a bulk container is partially unpacked, the unpacking should be performed at a protected work station. Any MOS devices that are stored temporarily should be packed in conductive or antistatic packing or carriers.

ASSEMBLY

MOS devices must be removed from their protective packing with earthed component pincers or short-circuit clips. Short-circuit clips must remain in place during mounting, soldering and cleansing/drying processes. Do not remove more devices from the storage packing than are needed at any one time. Production/assembly documents should state that the product contains electrostatic sensitive devices and that special precautions need to be taken.

During assembly, ensure that the MOS devices are the last of the components to be mounted and that this is done at a protected work station.

All tools used during assembly, including soldering tools and solder baths, must be earthed. All hand tools should be of conductive or antistatic material and, where possible, should not be insulated.

Measuring and testing of completed circuit boards must be done at a protected work station. Place the soldered side of the circuit board on conductive or antistatic foam and remove the short-circuit clips. Remove the circuit board from the foam, holding the board only at the edges. Make sure the circuit board does not touch the conductive surface of the work bench. After testing, replace the circuit board on the conductive foam to await packing.

Assembled circuit boards containing MOS devices should be handled in the same way as unmounted MOS devices. They should also carry warning labels and be packed in conductive or antistatic packing.

Digital multimedia technology transforming the PC into TV, radio, and VCR

The PC invaded the office and replaced the typewriter, phone, FAX, adding machine, financial ledgers, Rolodex, appointment book, and more.

Now the Multimedia PC is invading the home replacing the TV, radio, VCR, phone, newspaper, games, books, picture album, and more.

Philips supplies the PC Multimedia components, turning PCs into consumer products by supplying the following components in high volume:

- Computer monitors and monitor ICs
- CD-ROM, recordable CD drives, mechanisms and ICs
- Cameras and camera ICs
- TV, cable TV, digital cable and satellite receiver tuners
- Digital cable and satellite receiver ICs
- FM radio tuners
- Video processing ICs
- 2D and 3D graphic and video accelerators
- MPEG audio & video decoders
- Close caption, Teletext and Intercast ICs
- Audio processing ICs

Philips supplies the components required in video conferencing, editing, TV in the computer, radio in the computer, and VCR in the computer.

TV Audio and Video Signal

The Composite Video signal received from a TV antenna, cable TV set-top converter, video tape recorder (VCR) or video camera contains a black and white image, the color image information, timing required to start the display of a horizontal line or a whole new frame on the TV display. The signal contains the stereo sound of the program, Close Caption text to be displayed on the bottom of the TV screen for people with poor hearing. Teletext (or Intercast) with business and other information is also sent with the TV signal.

Locking to the TV signal and extracting the video, audio and data is difficult, as the signal can be corrupted by the source (for example, tape stretch and motor wobble in the VCR), or by the attenuation, noise and ghosting in the transmission channel.

Philips' 50 years of experience in the consumer TV and broadcast studio led to the development of the rugged Line Locked Clock system which locks to noisy and non-standard TV signals reliably, without jitter, tearing or loss of color.

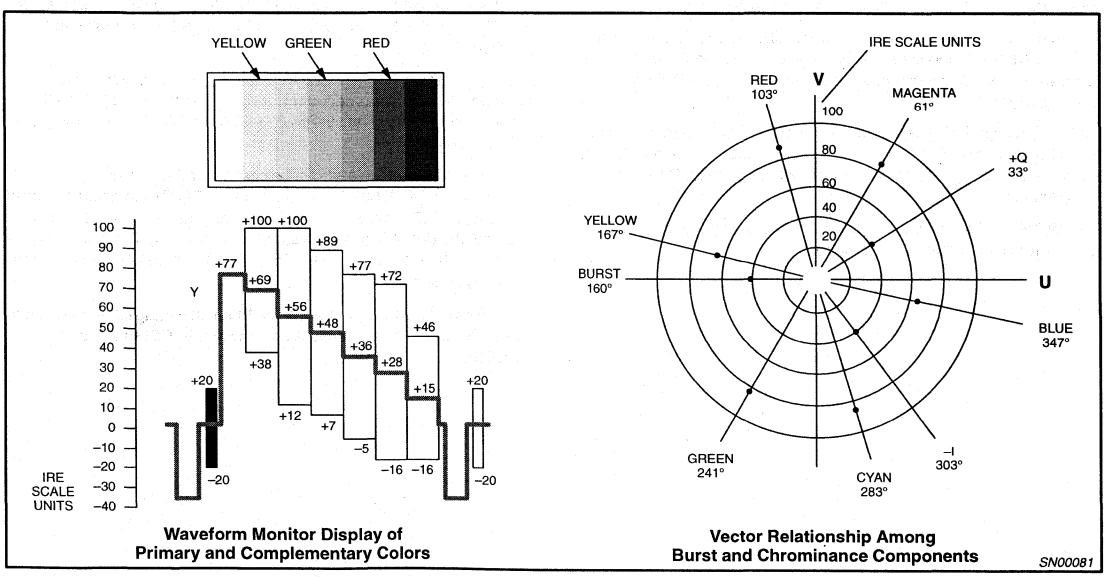

Figure 1. The composite video signal contains timing, black & white and color information.

Digital multimedia technology transforming the PC into TV, radio, and VCR

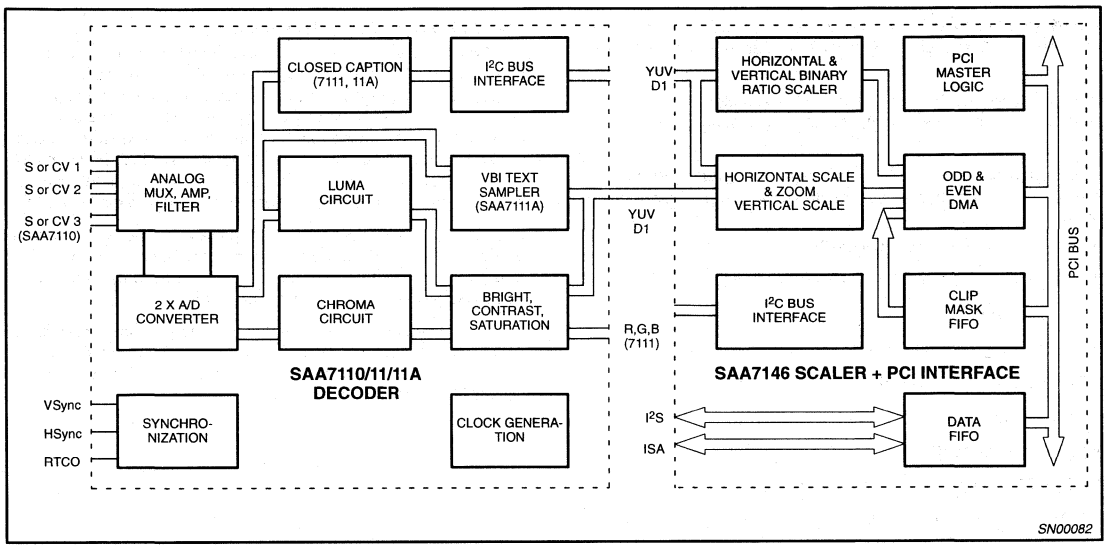

Figure 2. The SAA7110, SAA7111, and SAA7111A accept analog composite or S Video signal and decode it into digital YUV or RGB signal.

Video Signal Decoding to S Video and Composite Video

The analog video signal needs to be digitized and decoded in order for the computer to store, process and display the video images.

A composite video signal is digitized and filtered into its black and white (luminance) and color (chrominance) components. In this form, with separated luminance and chrominance, it is called S Video signal.

An S video signal with separated chrominance and luminance signal is digitized by two A/D converters. The chrominance signal is further separated via a digital quadrature demodulator into its U and V color components.

The digital YUV signal can be processed as is or transcoded via a digital matrix into a digital RGB signal.

Video Signal CCIR 601 and Square Pixel Sampling and Computer Graphics Display Standard

Computer monitors display "square pixels" with 640 horizontal pixels and 480 vertical pixels. As the aspect ratio of the display screen is 4×3, the 640×480 pixels are equally spaced horizontally and vertically.

To sample the NTSC signal 640 times during the active video portion, the A/D in the decoder needs to sample at a 12.27MHz "square pixel" rate. The Philips SAA7110 and SAA7196 are square pixel decoders.

Video communication and compression standards employ the international CCIR 601 NTSC, PAL, and SECAM digitizing standard specifying 720 samples during the active portion of the video signal. Hence, the decoder needs to sample the signal at a "CCIR 601" sample rate of 13.5 MHz. The Philips SAA7111 and SAA7111A are CCIR 601 decoders.

The SAA7146 shown above scales the digital image and sends it to the PCI bus. It will be discussed below in the "PCI Interface ICs" section.

Digital multimedia technology transforming the PC into TV, radio, and VCR

PC Buses and Video Capture Architecture

Audio and video capture with its real time and high data rate (beyond 20 MBytes/second) requires availability of enough bus bandwidth at the right time. It is the nature of live multimedia data streams that the flow of video and audio data cannot be stopped. Data that is not captured is lost, and multimedia playback that has gaps and interruptions is quite disturbing. Scheduling and bandwidth allocation in a predictable manner on the video bus is a major issue.

In most consumer applications the audio has the highest priority, as any gap in the data produces unacceptable "clicks". The video data is secondary in importance as previous images can be repeated with little noticeable effect if a frame or a portion of it is lost.

Two architectures exist to play live video signal in a PC. The Shared Frame Buffer architecture allows playing live video and graphics on the computer monitor. The PCI architecture, with its typical bandwidth of 100 MByte/Second, allows live video playback **and capture** in the PC.

Shared Frame Buffer Architecture

If the VGA Graphic controller in the graphic card has a digital "video" port, a low cost video/graphics system (as shown in Figure 3) can be built.

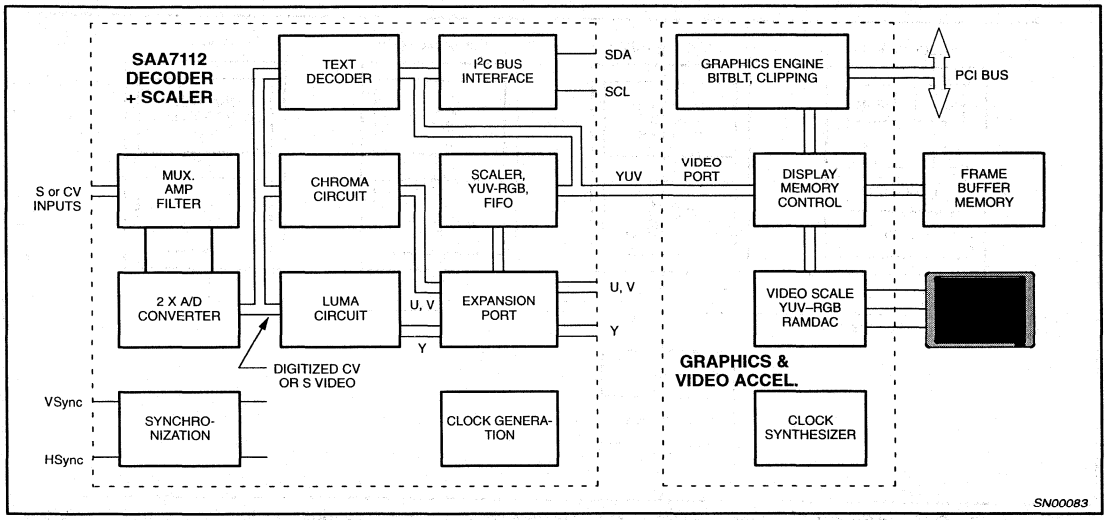

Figure 3. The live video image is written into the graphics Frame Buffer memory via the Video Port of the graphics controller.

Digital multimedia technology transforming the PC into TV, radio, and VCR

PCI (Peripheral Component Interface) Architecture

The PCI architecture frees the CPU to run its operating system on its local bus while most video traffic is conducted on the peripheral PCI bus.

The arbiter on the PCI bus manages and distinguishes the real-time importance of each master requesting the bus, increasing the robustness of the PCI bus and its capability to recover from an error.

The PCI architecture, with its typical bandwidth of 100 MBytes/Second, is the only architecture allowing Ive video playback **and capture** in the PC. The architecture is a "shared memory' structure where the live images are decoded and scaled by the video capture engine and sent to the desired memory location in the computer. Note that the Philips video capture and scaling ICs treat the Odd and Even fields of the interlaced video image independently.

Thus, in a video conference application, the Odd field of the image from the local camera (the 'vanity' image) is sent directly to the frame Buffer RAM of the graphic controller to be displayed on the computer monitor. The Even field is scaled down and sent to the video conference compression engine.

In a video editing application, the Odd field of the image from the VCR is sent directly to the frame Buffer RAM of the graphic controller to monitor the incoming images. The Even field is scaled down and sent to the Hard Disk for storage and further editing.

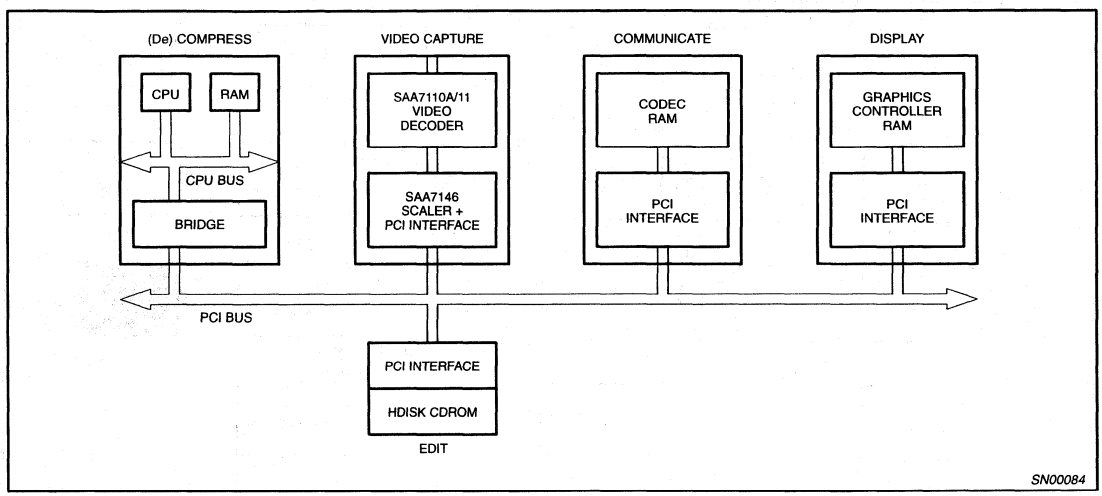

Figure 4. The Odd and Even fields of the interlaced video image are scaled and sent to various destinations in the PC for Video Conferencing, Editing, Publishing and Playback applications.

Digital multimedia technology transforming the PC into TV, radio, and VCR

PCI Interface ICs and Video Conference Applications

The SAA7146 is a four way bridge to the PCI bus. The SAA7146 scales digital video images and sends them into and out of the PCI bus. The SAA7146 also sends and receives digital stereo sound (in I^2S format). The DEBI port of the SAA7146 allows interfacing with ISA devices like MPEG decoders. The I^2C port can read Close Captioning data from the SAA7111 video decoder or from the SAA5252 Closed Captioning decoder.

In the Video Conference system (Figure 5), the SAA7146 receives the digital YUV images from the Video Decoder. The SAA7146 scales and bursts the image to the PCI bus of the computer for local display on the monitor, for compression and transmission over the phone, ISDN line or LAN.

The images received are decompressed by the computer, scaled or zoomed by the SAA7146 and encoded by the Video Encoder into composite and S Video signal for TV display or VCR recording. Similarly, the SAA7146 sends and receives the digital sound in the I^2S format.

The TM-1 IC shown below (Figure 6), further relieves the computer from the compression/decompression and communication tasks.

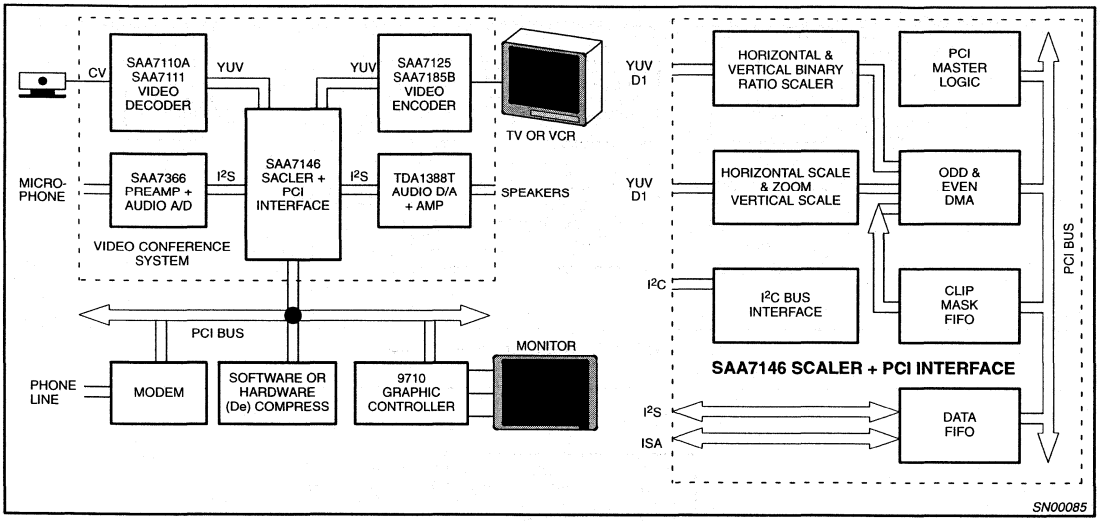

Figure 5. Video Conference System (SAA7146 based)

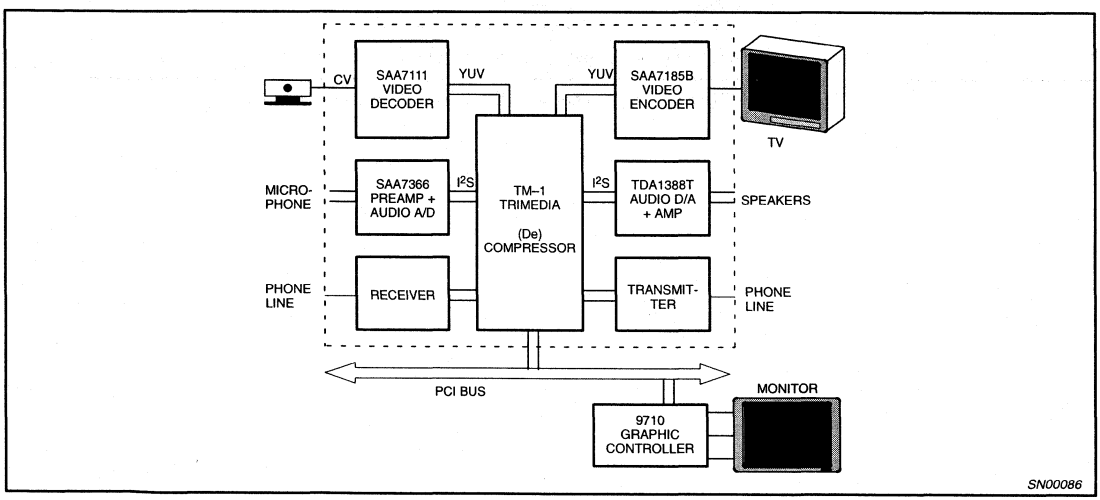

Figure 6. The TM-1 handles video I/O, audio I/O, communication I/O and (de)compression.

Digital multimedia technology transforming the PC into TV, radio, and VCR

TV in the Computer

The following component-set supplied by Philips will turn a PCI-based computer into a TV and allow video capture for editing, desktop publishing or video conferencing.

Philips FI1236 TV Tuners accept the NTSC TV signal from a Cable TV or TV antenna. The tuner selects one channel in the 50–850 MHz band.

The composite video signal is sent to an SAA7111 video decoder to generate digital YUV images and extract the Closed Caption text for the hearing impaired from the TV signal. The SAA7146 scales the YUV image and transmits it and the Closed Caption information to the PCI bus.

Composite audio signal from the TV tuner is decoded into stereo sound by the TDA9850 Stereo Decoder. The tone is controlled by the TEA6300 and sent to the speakers via the TDA1517 Stereo Power Amplifier.

The tuners available are shown in Figure 8, and are all pin compatible.

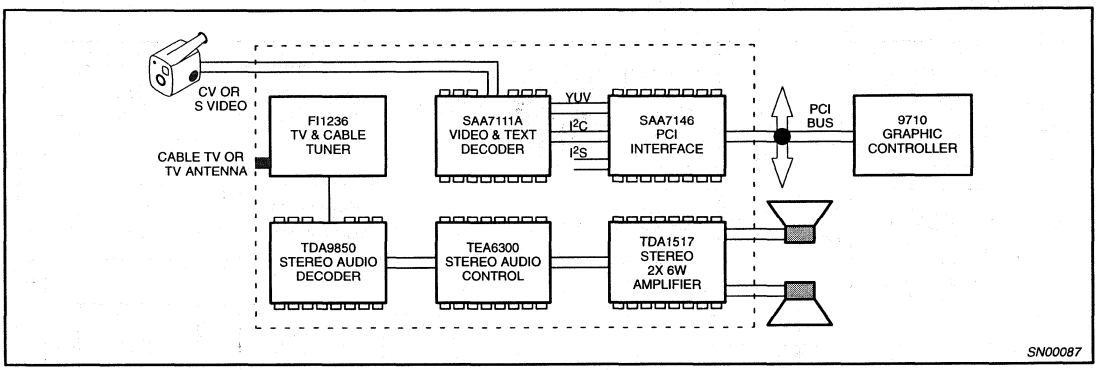

Figure 7. This chipset will turn your PC into a TV.

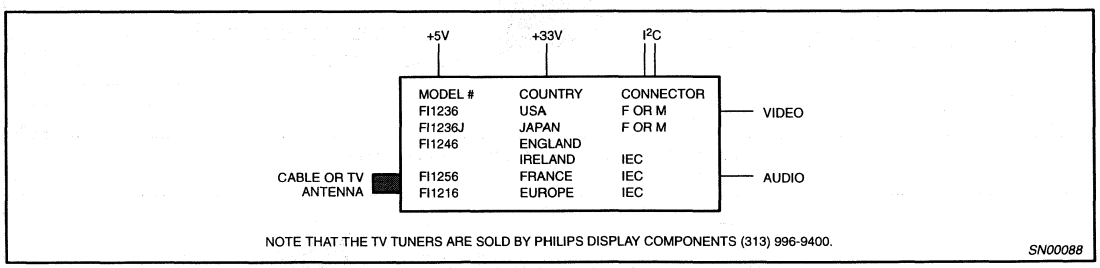

Figure 8. The TV/cable tuner connects to the TV antenna or cable TV outlet.

Digital multimedia technology transforming the PC into TV, radio, and VCR

Stereo Decoders

The MTS (Multichannel Sound Modulation) stereo sound from the tuner contains the Left + Right sound in the 50–15,000 Hz band. A Pilot Tone is transmitted at 15,734 Hz and the Left – Right signal is modulated on a 31,468 Hz carrier.

The Second Audio Program (SAP) allows the TV viewer to listen to the TV program in two languages. The SAP sound is modulated on a 78,670 Hz carrier.

The Stereo Decoder locks its PLL to the Pilot Tone and extracts the Left, Right, and SAP sound signals (Figure 9).

The TEA6300 Sound Control and the Stereo Power Amplifiers are shown in Figure 10 to exemplify a much larger product family described in the data book.

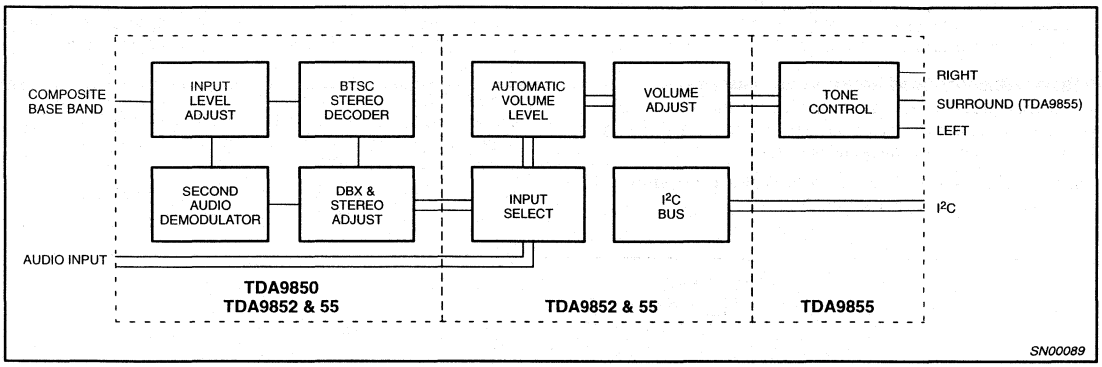

Figure 9. The stereo decoder extracts the stereo sound and second language.

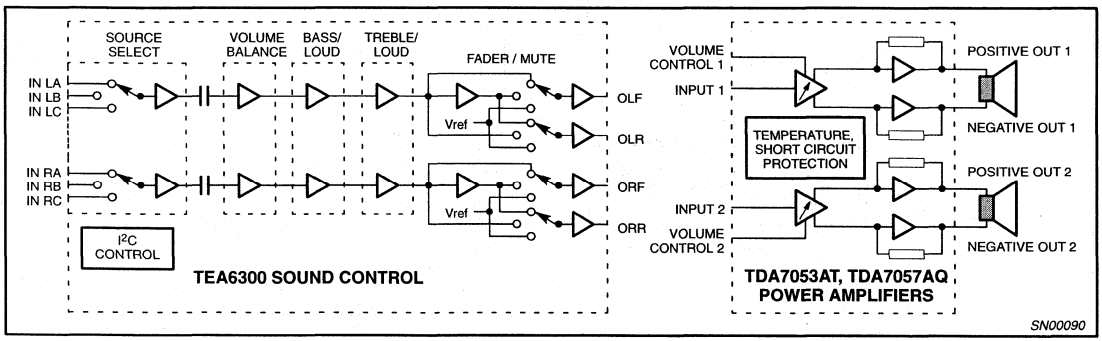

Figure 10. Samples of sound control and power amplifiers are shown here.

Digital multimedia technology transforming the PC into TV, radio, and VCR

Video Scalers

Scaling the video image is required for several reasons:

- The video image in the Windows environment on the computer monitor can be dragged and scaled to any size by the viewer.
- The image needs to be scaled to reduce the bandwidth when sending the data to the hard disk.
- The size and format of the image need to be changed to match the requirements of compression and graphic controller ICs.

The Philips SAA7112, SAA7140A, SAA7140B, SAA7146, SAA7186, and SAA7196 scalers use adjacent pixels and lines to interpolate and smooth the lines and images generated as the image is scaled.

Closed Caption and Teletext Decoders

TV program providers transmit images, sound and text. The text contains Closed Captioning for the hearing impaired and Teletext (or Intercast) containing business and other data.

The text is sent as digital data during the vertical blanking interval (when no active video is transmitted).

For data and text extraction, the ICs need to receive the analog composite video signal. Locate the horizontal line where the digital data is embedded. Recover the clock and extract the data sent. Error correction and detection takes place and the text data is assembled and stored. The PC is interrupted when a line or page of data is available.

'VCR' in the Computer

Video CDs contain 74 minutes of MPEG 1 compressed audio and video.

The compressed video is read from the CD ROM and sent via the SAA7146 'ISA' port to the SAA7131 MPEG 1 audio and video decoder.

The SAA7131 decompresses the signal into digital YUV video and digital I^2S audio. The SAA7146 becomes PCI bus master, and bursts the digital video image and digital audio sound to any desired memory location in the PC.

The decompressed images from the SAA7131 can also be sent to a TV via the SAA7185B NTSC and PAL Encoder.

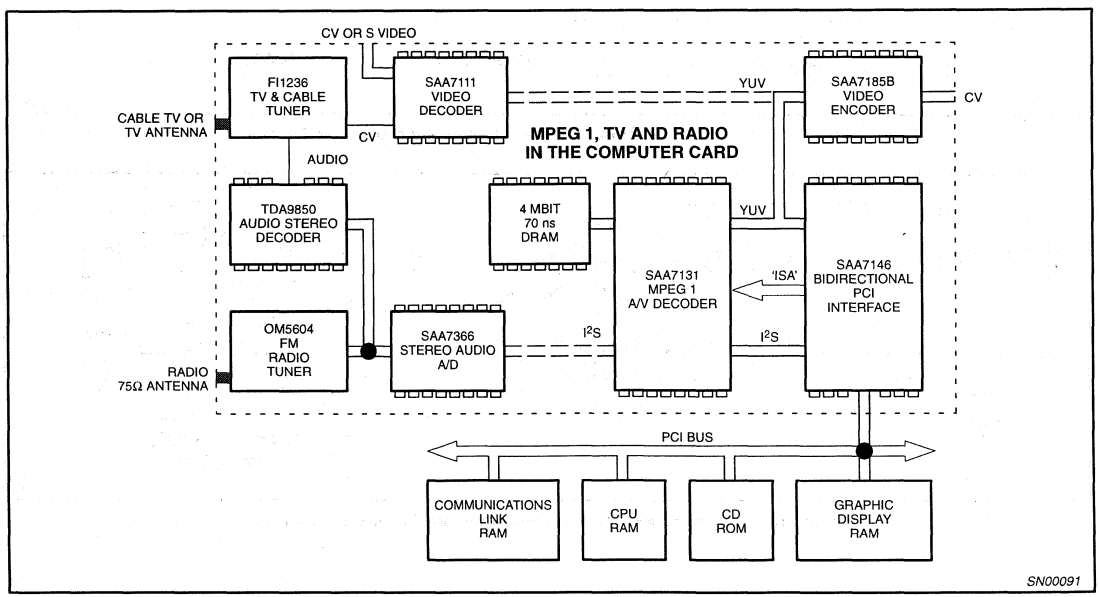

Figure 11. TV, Radio and MPEG (VCR) playback in the PC are accomplished by this chipset.

Digital multimedia technology transforming the PC into TV, radio, and VCR

MPEG 1 Audio and Video Decoder

The SAA7131 MPEG 1 Audio and Video Decoder performs system-level parsing, extracting the compressed video stream and the compressed audio stream and storing them in the external 2 MBit DRAM FIFO.

The video and audio decompression engines in the SAA7131 decode the compressed streams in the FIFO and assemble the decompressed frames and sound in the FIFO.

The video images are played out of the SAA7131 as YUV or RGB data in 352 × 288 (SIF format), 320 × 240 (CIF format), or 640 × 480 resolutions.

Radio in the Computer

The OM5604 FM Radio Tuner receives the FM signal from a TV or 75Ω antenna. The OM5604 tuner selects one channel in the 87.5–108 MHz band and produces stereo signal output. The stereo radio sound is digitized by the SAA7366 and sent to the PCI bus.

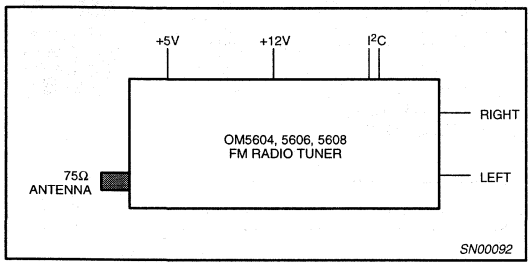

Figure 12. The FM radio tuners are factory tuned.

Video Encoding

The digital RGB or YUV video or graphic image needs to be encoded to analog composite or S video signal in order for the computer to display the images on consumer TVs, projection TVs, or store the images on a VCR.

In the Video Encoder the digital YUV 4:2:2 signal is interpolated to 4:4:4 signal. The U and V components are combined via a quadrature modulator into color (chrominance) components. The Y black & white (luminance) components are delayed.

The Y (luminance) and C (chrominance) are sent to 10-bit D/A converters to convert them to analog S video signals.

Adding the Y and C signals together creates the composite video signal.

Philips encoders like the SAA7124/5 (shown in Figure 13) allow the encoding of digital YUV, Closed Caption, Teletext, and Overlay information into NTSC, PAL, and SECAM composite and S video signals.

The Philips decoders and encoders can be Genlocked via the RTC (Real Time Control) I/Os.

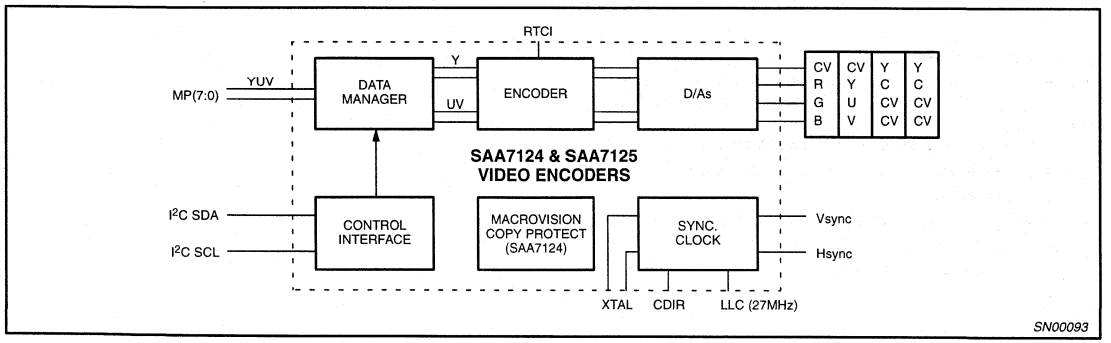

Figure 13. The Video Encoder converts digital images and text into analog composite and S Video signals.

Digital multimedia technology transforming the PC into TV, radio, and VCR

2D Graphics Accelerators

The SAA9710 is a single-chip PCI graphic and video accelerator with internal clock synthesizers and RAMDAC. The SAA9710 accepts graphic images from the host via the PCI bus. The graphic image is painted in the Frame Buffer memory and displayed on the computer monitor. The video images can also be written via the PCI bus into the shared (graphics and video) Frame Buffer and displayed on the computer monitor.

The SAA9710 can scale, zoom and clip the video image and a YUV image can be color space converted to the RGB image required by the RAMDAC. Video images can also be overlayed over the graphic images via the VAFCI port of the SAA9710.

The 90C24 graphic accelerator is an AT and VL bus single-chip graphic accelerator with internal clock synthesizers and RAMDAC. It contains the flat panel control and power management required in portable and LCD display applications.

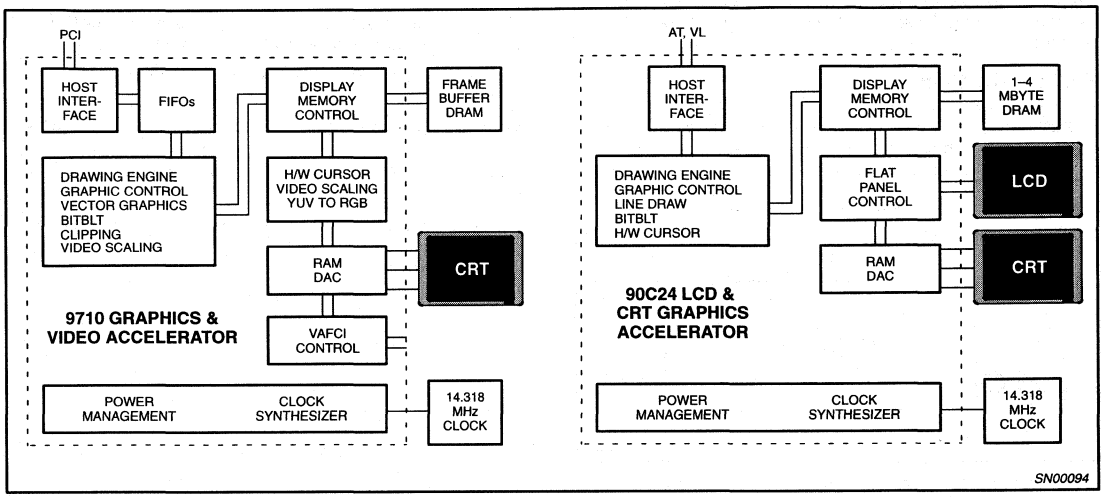

Figure 14. the 9710 and 90C24 are 2D graphic accelerators for desktop and portable applications.

3D Graphics Coprocessor

The SAA7101 is a PCI based 3D graphic coprocessor converting existing 2D graphic controllers into 3D graphic controllers. The SAA7101 performs:

- Flat and Gouraud shading of trapezoids, triangles, lines.
- Texture mapping and modulation for triangles and lines.
- Texture filtering
- Antialiasing via super sampling and accumulation buffer.
- Supports stencial buffer
- 3D Z buffer and texel buffer in DRAM.

See Figure 15.

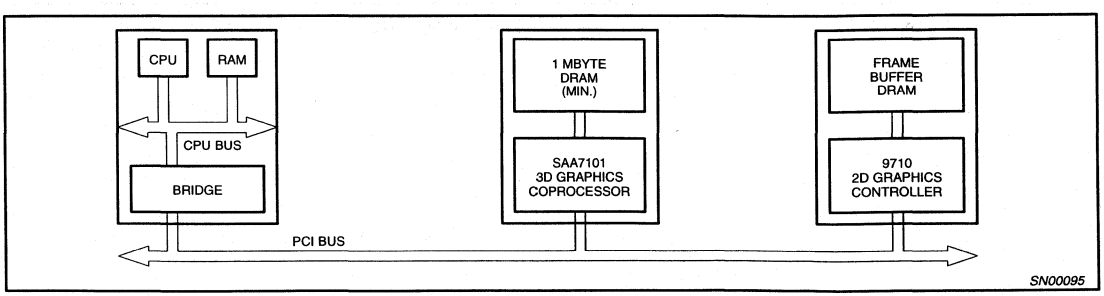

Figure 15. The SAA7101 turns the 9710 2D accelerator into a 3D accelerator.

Digital multimedia technology transforming the PC into TV, radio, and VCR

Digital Satellite and Cable TV Receivers

The following chipset (Figure 16) is available from Philips to design digital Cable and Satellite modems and receivers.

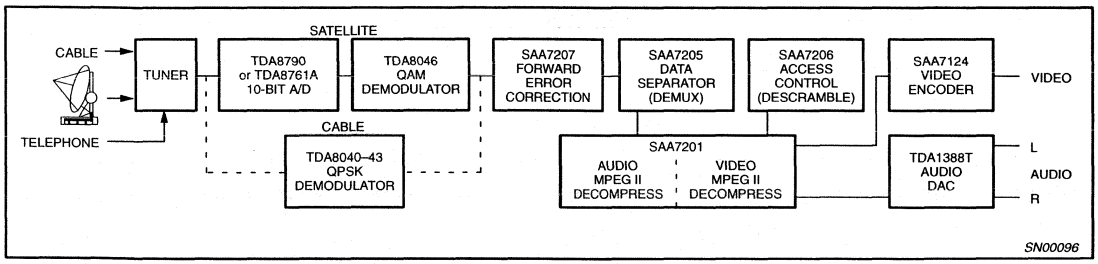

Figure 16. DVB and DAVIC compliant digital cable and satellite receivers can be built with this chipset.

Line-locked digital colour decoding

Ton NILLESEN *

On présente dans cet article une méthode de décodage numérique des signaux vidéo couleur basée sur des fréquences d'échantillonnage verrouillées sur la ligne. La fréquence d'échantillonnage est synthétisée à partir de la fréquence d'un cristal. On génère une fréquence stable de sous-porteuse en utilisant la fréquence variable d'échantillonnage par contrôle direct à partir du synthétiseur.

A digital colour decoding principle involving line-locked sample frequencies is presented. The sampling frequency is synthesized from a crystal frequency. A stable subcarrier frequency is generated from the variable sampling frequency by forward control from the synthesizer.

* CAB-Elcoma, N.V. Philips, Eindhoven (The Netherlands).

To digitally decode PAL or NTSC composite video signals in a TV receiver, it is advantageous for the sampling rate to be related to the colour subcarrier frequency because this simplifies the demodulator and the chroma filters. However after colour decoding, the component video signals for luminance and colour difference are available and the colour subcarrier is then no longer relevant. Line-locked sampling is then a better choice.
In fact, for video processing and conversion to other scanning frequencies, line-locked sampling is a natural choice because it results in orthogonal sampling, which simplifies video signal processing with line and field memories [1].

WHY LINE LOCKED ?

Standard conversion to other scanning frequencies might be used for instance for reduction of large area flicker by means of field rate conversion to higher frequencies. Another type of conversion is compression of the signals for features such as picture in picture and multi picture-in-picture, whereas expansion of the signals is required for picture enlargement or C-MAC decoding, etc..

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ACTA ELECTRONICA. **27**, 1-2, 1985, 101-107.

Some other examples of signal processing using line or field memories are :

- cross colour and cross luminance reduction with line-, field- or frame-combfilters,
- noise reduction by an integrating temporal filter,
- resolution enhancement by a peaking spatial filter.

Furthermore, a line-locked sample frequency is a must for matrix displays such as LCDs, the index tube and dot matrix printers and it is also a necessity for display of good quality characters.
And last but not least, the circuitry for processing line-locked component video signals is substantially independent of transmission standards.

APPLICATION OF SAMPLE RATE CONVERTER

If a subcarrier-locked colour decoder is used, line-locked samples can be obtained by sample rate conversion. An obvious approach for a Sample Rate Converter (SRC) is via digital-to-analog (DA) and analog-to-digital (AD) conversion. The subcarrier-locked samples are then converted to analog signals and re-sampled with the line-locked sample frequency (fig. 1a). Although this is a straigtforward method, using well-known techniques, it is not attractive because it is expensive. It requires ADCs and DACs, three of each for the three component signals, including the reconstruction filters, and a second clock generator. Furthermore, the additional conversion step degrades signal quality. A second approach is a SRC in the digital domain, the line-locked samples being calculated from surrounding subcarrier-locked samples by means of interpolating algorithms (fig. 1b). Both approaches require two clock generators coupled to the video signal, one burst-locked and the second line-locked.

However, it is not necessary to have the line-locked clock available with equidistant clock transitions. Transfer and processing of the samples with amplitude information belonging to line-locked sampling positions can be done with a gated version of the original clock (fig. 1c). The gated clock should then have a constant number of clock transitions per line period. However a reverse sample rate conversion is then required before DA-conversion. This second SRC is eliminated if the line-locked clock is physically available. DA-conversion is then done with the line-locked clock. However the most complex part of the sample rate conversion is the interpolating algorithm required [2].

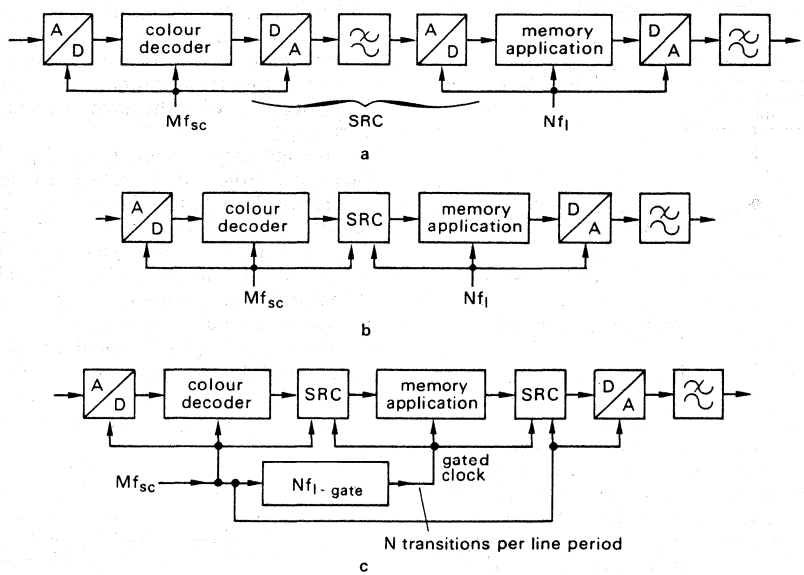

Fig. 1. Application of sample rate converters : a. anolog sample rate converter, b. digital sample rate converter and two clocks coupled to video signal, c. two digital sample rate converters and single clock.

INTERPOLATION OF SAMPLES

In principle, interpolation is done by low-pass filtering. The low-pass filter should reject the sidebands of the original subcarrier-locked samples, including at harmonics of the sampling frequency, but should pass the baseband spectrum containing the desired signal with a flat frequency- and linear phase-characteristic. Linear interpolation is certainly not sufficient, neither in the passband nor in the stopband, to preserve good signal quality. Each new sample should therefore be calculated from several surrounding original samples with proper weighting factors. The weighting factors should be of sufficient number and sufficient accuracy to generate new samples with a timing accuracy of about 0.2 ns, if the resulting signal should have a bandwidth of 5 MHz and 8-bit quantization (fig. 2).

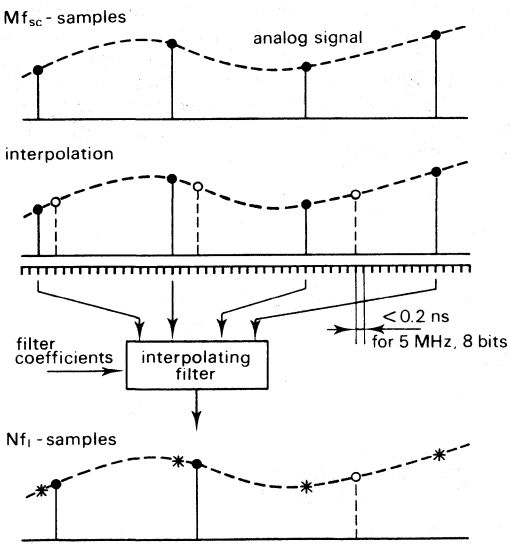

Fig. 2. Principle of sample rate conversion.

For compatibility with non-standard video signals with variable line frequencies, the conversion rate cannot be expressed as a simple ratio of small prime integers but is irrational and time-varying. As a consequence the interpolating filters will be complex with a large set of filter coefficients. A digital SRC will therefore require a relatively large chip area. These are the reasons for considering line-locked colour decoding which produces line-locked samples of the luminance and the colour difference signals directly.

COLOUR DECODING PRINCIPLE

The NTSC and PAL colour systems use suppressed-carrier amplitude modulation with quadrature subcarriers (fig. 3). The chroma signal can be demodulated by multiplying it by the correctly-phased subcarrier sine and cosine waves. This gives the colour difference signals plus some high frequency components,

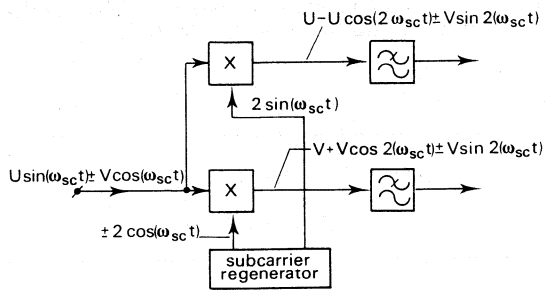

Fig. 3. Colour decoding principle for PAL system.

the latter being removed by filtering. For digital signals, the chroma signal has to be multiplied by the sampled subcarrier waves. If the sample rate is four times the subcarrier frequency, with the correct phase, the multiplications simplify to multiplication by 1, 0, −1 and 0 of successive samples. With line-locked or other sample frequencies asynchronous with the subcarrier, real four-quadrant multipliers are required for demodulation with the asynchronously-sampled subcarrier [3].

In the subcarrier regenerator (fig. 4) the subcarrier phase is coupled to the received colourbust. In order to reduce the effects of noise, the phase information extracted from several bursts is averaged by means of a narrow filter which in general is implemented as a phase locked loop (PLL). In analog circuits, the phase detector normally consists of a multiplier and the loop filter in a second order loop delivers an output signal which is partly proportional to the phase detector output signal and partly an integrated version of that signal. So digitally these blocks can be realised with adders, multipliers and an integrator.

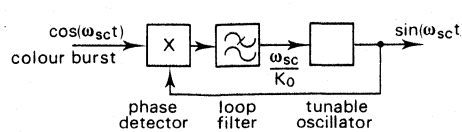

Fig. 4. Schematic diagram of the analog subcarrier regenerator.

The tunable oscillator is normally a voltage controlled oscillator with an oscillator control sensitivity of K_0 ($rd \cdot s^{-1} \cdot V^{-1}$). So for an output frequency of ω_{sc}, the subcarrier frequency, the loop filter has to deliver a control voltage of ω_{sc}/K_0. For sinewave oscillators the instantaneous output is sin ($\omega_{sc}t$). As a consequence, the oscillator transfers the input signal ω_{sc}/K_0 to the output signal sin ($\omega_{sc}t$) which, apart from the sine function and the constant K_0, is an integrating action. The sine function prevents saturation of the output by the ever increasing value of the instantaneous phase. With the sine function the output phase follows the instantaneous phase modulo 2 π radians.

THE DISCRETE TIME OSCILLATOR (DTO)

The integrating and modulo function of the oscillator can be realised digitally with an accumulator consisting of an adder and D-flip-flops (fig. 5a). The multibit output of the adder is applied to its input via D-flip-flops which are clocked with the clock frequency f_{cl}. At the second input of the adder, a constant multibit value p is applied. So at each clock period the previous content of the accumulator is incremented by p until overflow occurs at the value q. The next value will then be the previous value plus p modulo q. So the output resembles a time discrete quantised sawtooth signal whose period is set by p. Obviously the ratio between p and q equals the ratio between the clock period and the period of the output signal f_0. So the control value p should be $f_0/f_{cl} \cdot q$. If the overflow value is defined as being 1, then the input value simplifies to $p = f_0/f_{cl}$ (fig. 5b).

That brings us to our definition of a discrete time oscillator (DTO) also known as ratio counter or rate multiplier or accumulator or numerically controlled oscillator. The input value should equal the ratio between the desired output frequency and the clock frequency. Its modulo 1 output indicates from zero to one the instantaneous phase within a single preriod (fig. 6).

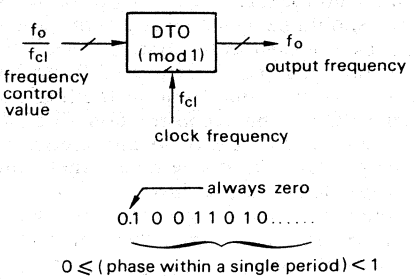

Fig. 6. The discrete time oscillator.

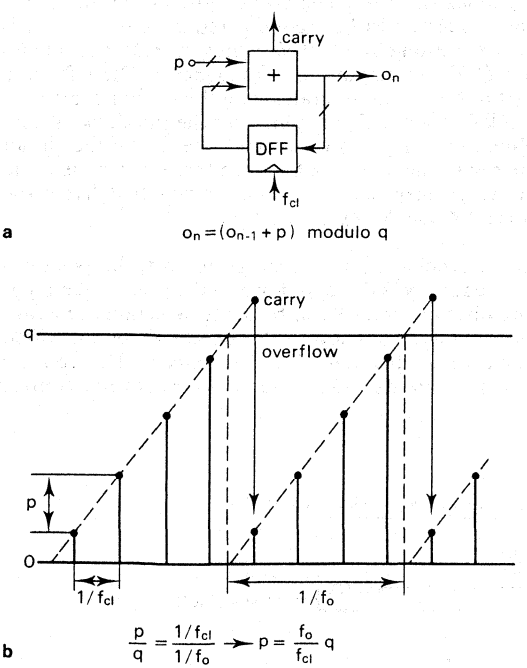

Fig. 5. Principle of the discrete time oscillator.

Note that the ratio f_0/f_{cl} at the input is dimensionless, indicating the phase increment per clock period, whereas the output of the DTO is the instantaneous phase modulo 1, which in principle is varying. Both signals can, in binary notation, be approximated to the required accuracy. However if the clock frequency is not constant whereas a constant subcarrier frequency should be generated, then the frequency control value should be corrected accordingly to the desired accuracy. As a consequence, the line-locked clock should be known with sufficient accurary and has therefore to be generated with a crystal frequency as reference.

Nf_l GENERATOR

It is a logical step to generate the line-locked sample frequency from a crystal frequency by means of a DTO. The DTO is clocked with the crystal frequency f_c and the desired output frequency is Nf_l, so the loop

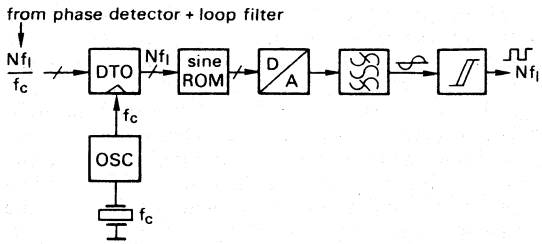

Fig. 7. Generation of line-locked sampling frequency ($N f_i$) with crystal accuracy.

filter in the horizontal phase locked loop should deliver the numerical value $N f_i/f_c$ (fig. 7).
The DTO delivers then a quantised sawtooth signal with frequency $N f_i$ but in the discrete time domain sampled with the crystal clock f_c. However the sample frequency should be available as a continuous signal so that it can be used as the system clock. Therefore the DTO output signal is converted from digital to analog after a conversion from sawtooth to sinewave via a sine-ROM. The reconstruction filter delivers then an analog sinewave with no undesired harmonics or mixing products. That sinewave is then converted to the proper logical signal levels.
If this sample frequency generator is used in the horizontal phase locked loop, then the relationship between instantaneous sampling frequency and the crystal controlled reference frequency is known. As a consequence, the generated frequency control value $N f_i/f_c$ from the horizontal phase locked loop can be used to correct the DTO in the subcarrier loop for variations in $N f_i$.

FORWARD CONTROL (DIVIDER)

Figure 8 shows the subcarrier phase locked loop with the burst phase detector, the loop filter, the DTO and the sine plus cosine ROM which delivers the demodulating sine and cosine waves. Between the loop filter and the DTO the correction is done for the varying clock frequency.

Since the subcarrier DTO operates with the line-locked clock, a value $f_{sc}/N f_i$ should be applied to its input as frequency control value. This value is obtained via an arithmetical divider (A/B) which divides the intermediate control value at the output of the subcarrier loop filter by $N f_i/f_c$ from the horizontal PLL. The intermediate control value should therefore be f_{sc}/f_c, the ratio between the subcarrier frequency and the crystal frequency. Apart from long-term variations, this ratio remains constant regardless of the clock frequency. Consequently, the subcarrier loop filter can be designed for narrow noise bandwidth, optimised for subcarrier regeneration. The inaccuracy of the forward control due to the limited wordlength of the signals is handled by the loop as internally-generated noise and can be chosen at a sufficiently low level.

LINE-LOCKED COLOUR DECODER

A complete block diagram of a line-locked colour decoder is presented in figure 9. For simplicity, several functions such as automatic colour control, colour killer, compensating delays etc. have been omitted in the block diagram. The signal-flow in the horizontal and subcarrier PLLs are indicated in heavy lines as is the correction circuit (A/B) which corrects the subcarrier DTO for varying line frequencies. The left-hand part of the circuit operates with the crystal controlled clock frequency f_c and generates the line-locked sampling frequency $N f_i$ with which the rest of the circuit operates. The coupling between these two parts is via the resynchronisation register R which delivers the control value $N f_i/f_c$ to the DTO.

In the synchronisation processing part, the $N f_i$ sample frequency is divided down to the line frequency f_i. The division ratio N can be made selectable to adapt the sample frequency to the bandwith of the video signal or to different line frequencies. The counter drives a state decoder which delivers several control

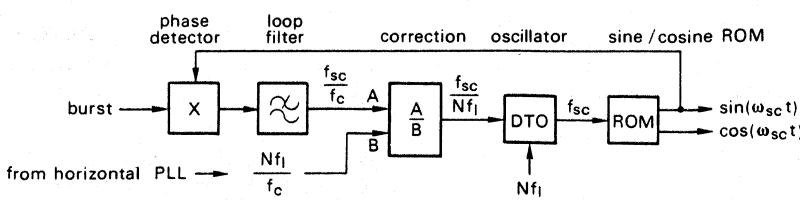

Fig. 8. Forward control of subcarrier DTO operating with line-locked clock.

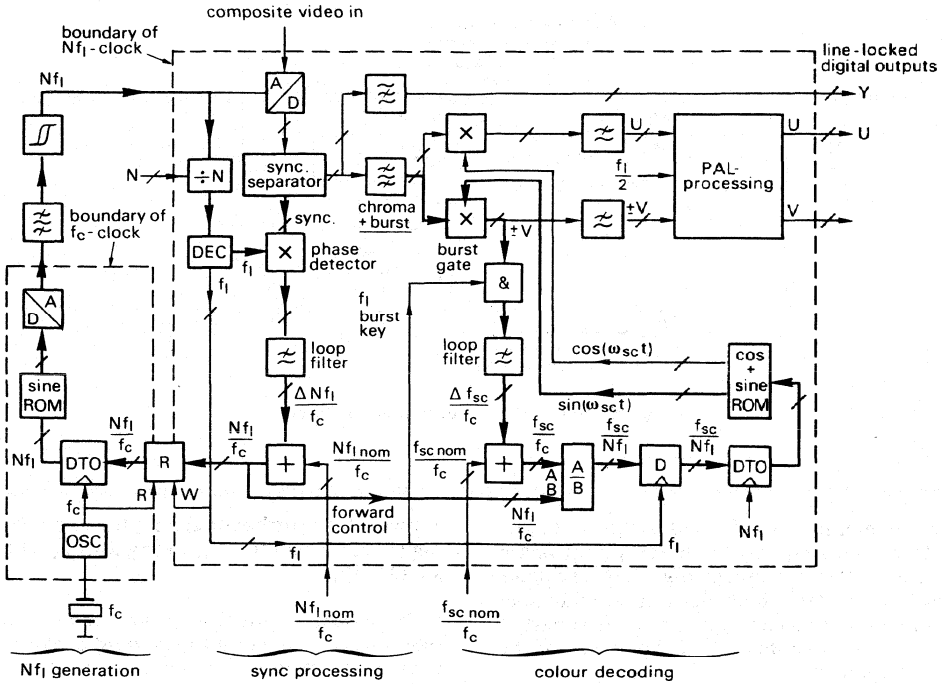

Fig. 9. Simplified block diagram of line-locked digital colour decoder.

signals at line frequency. One of these line frequency signals is applied to the horizontal phase detector where its phase is compared with the phase of the separated synchronisation signal. The result is applied to the loop filter and then added to the nominal input value ($Nf_{l\,nom}/f_c$) for the DTO. As a consequence the loop filter has only to deliver the error on the nominal value and the nominal value can be made selectable to accomodate different line frequencies or different numbers of samples per line.
The frequency control value has only to be updated once per line period. However updating the sample frequency also requires a new correction of the subcarrier DTO input value. For that reason the control values to both DTOs are effectuated on command of a line frequency signal f_l when both control values have been calculated. In fact the subcarrier DTO is updated somewhat later than the Nf_l-DTO to compensate for the delay of the video signals from ADC to demodulator. The synchronisation signal f_l acts as write clock for the resynchronisation buffer R. The new data is then clocked with f_c and applied to the input of the Nf_l-DTO. In the subcarrier DTO the new value becomes availables as soon as the D-flip-flops in front of the subcarrier DTO are clocked with a line frequency signal.

In the subcarrier loop the demodulated burst signal is used as actual phase information for subcarrier regeneration. For PAL the average V-phase of the burst is zero if the subcarrier phase is correct. So the V-demodulator together with the burstgate, consisting of a multiple input AND-gate, forms the phase detector. After passage through the loop filter, the result is added to the nominal frequency control value ($f_{sc\,nom}/f_c$) and divided by Nf_l/f_c. After the division, which takes several clock cycles, the result is applied to the DTO via the D-flip-flops.

To prevent side-locking, the loop filter output $\Delta f_{sc}/f_c$ should be limited so that the regenerated subcarrier remains close enough to the nominal value. The nominal value can be altered to accommodate the subcarrier frequency in different standards. This gives this system a clear advantage over conventional decoders. Although only a single crystal frequency f_c is present, any subcarrier can be regenerated with the proper accuracy only by changing the nominal frequency control value $f_{sc\,nom}/f_c$.

Let us consider now the analog part of the clock generation circuitry. The reconstruction filter and wave shaper for the Nf_l clock frequency can be implemented with an analog PLL. The advantages of this are :

- the filter curve tracks the input frequency so that the bandwidth can be smaller than with a fixed filter : this allows fewer bits to be used in the DA-converter ;
- several line-locked frequencies can be generated if the PLL is provided with dividers ;
- the entire circuit can be integrated.

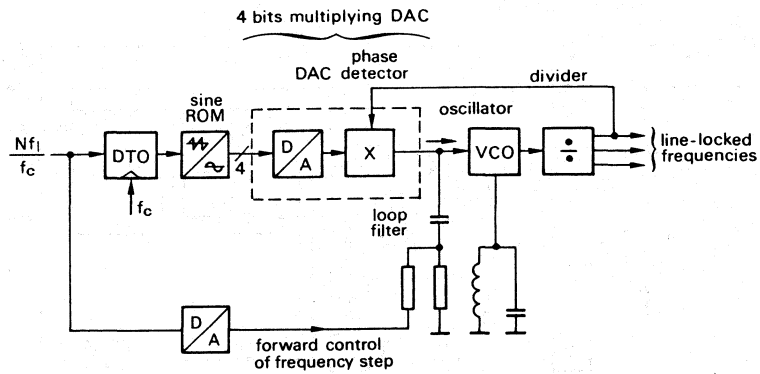

Fig. 10. Analog PLL as reconstruction filter.

Such an implementation is indicated in figure 10. The analog PLL is indicated with a charge pump phase detector, a loop filter, a voltage controlled oscillator (VCO) and the divider which delivers several line-locked frequencies. As a consequence the first part of the circuit can also operate on a subharmonic of the actual sample frequency.
The phase detector is driven by the DA-converter so that these functions can be combined in form of a multiplying DAC. Good results have been obtained with a 4 bit DAC so that this function can be very small in chip area. The required accuracy of the DAC of course is dependent on the quality of the reconstruction filter. A smaller filter bandwidth requires fewer bits for the DAC. However a narrow noise bandwidth of the PLL results in a slower response on frequency steps and consequently larger phase errors. That response can be improved by forward control of the oscillator to the required frequency. That information is available at the input of the Nf_1-DTO and could be used via DA-conversion for pre-correction of the VCO-frequency.

The factor N, which determines the sample frequency, can have any appropriate value. An attractive choice *is* $N=858$ for 60 Hz TV systems and $N=864$ for 50 Hz systems. The sampling frequency will then be 13.5 MHz which is in accordance with the CCIR recommendation for digital processing in studio equipment. The number of active samples per line period is then 720 for all TV standards.

CONCLUSION

In this presentation, the principle and the main advantages of line-locked colour decoding have been shown :

- owing to the orthogonal samples, line-locked decoding is optimized for the growing use of picture processing [4, 5] ;

- the system in principle is sample-rate-invariant so that it has excellent multi-standard capabilities and it enables the choice of a common clock for all standards ;

- for applications somewhat further in the future, it is quite important that the principle is directly applicable with matrix displays.

This article is written as a lecture (for ICCE 85 in Chicago).

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2 RAMSTAD (T.A.). — **Digital methods for conversion between arbitrary sampling frequencies.** IEEE Trans. Acoust., Speech Signal Process. **ASSP-32,** (1984), 577-591.

3 CLARKE (C.P.K.). — **Digital PAL decoding using line-locked sampling.** 8th Int. Broadcasting Convention Proc., IEE pub. nº **191,** (1980).

4 **Memory based features.** Philips publication 9398 401 30011, (1985).

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Digital interfaces for component video signals AN ETV/IR89126

Author: A. H. Nillesen

Several coding parameters have to be specified for interconnecting the digital component video signals YD, UD and VD between several devices. For the digital studio environment the CCIR has made two recommendations on these parameters.

CCIR Recommendation 601 describes an extensive family of clock frequencies and the signal amplitudes, timing codes and auxiliary data for digital video component signals common to the 525- and 625-line TV standards. CCIR Recommendation 656 describes the means of interconnecting digital television equipment complying with the 4:2:2 encoding parameters as defined in Recommendation 601.

In the early eighties the basic sampling clock of digital circuits for TV receivers has been chosen, by Philips, Siemens and others, in accordance with the digital component studio standard CCIR Rec. 601, due to obvious benefits of having that parameter in common with the broadcasting side (e.g. MAC-decoding and descrambling). However with respect to signal amplitudes and multiplexing format a different choice was made. Possible benefits from the recommendations on these parameters were not seen, or considered as imaginary, whereas the drawbacks were considered as serious. This paper addresses the signal amplitudes and the multiplexing format which have been chosen for digital YUV interfaces in the TV receiver, including the extensions and revisions from later dates.

1. THE CONVERSION FACTOR

To express the amplitudes of the digital component signals, the conversion factor CF is defined as being the ratio between the digital and the normalized representation of the signal. Normalization is done to Red=Green=Blue=1 at peak white and the digital signals are represented on a scale of 256 (8 bits).

$$CF = \text{Conversion} - \text{Factor} = \frac{\text{digital signal amplitude on 8 bits scale}}{\text{normalised signal amplitude } (R_{max} = G_{max} = B_{max} = 1)}$$

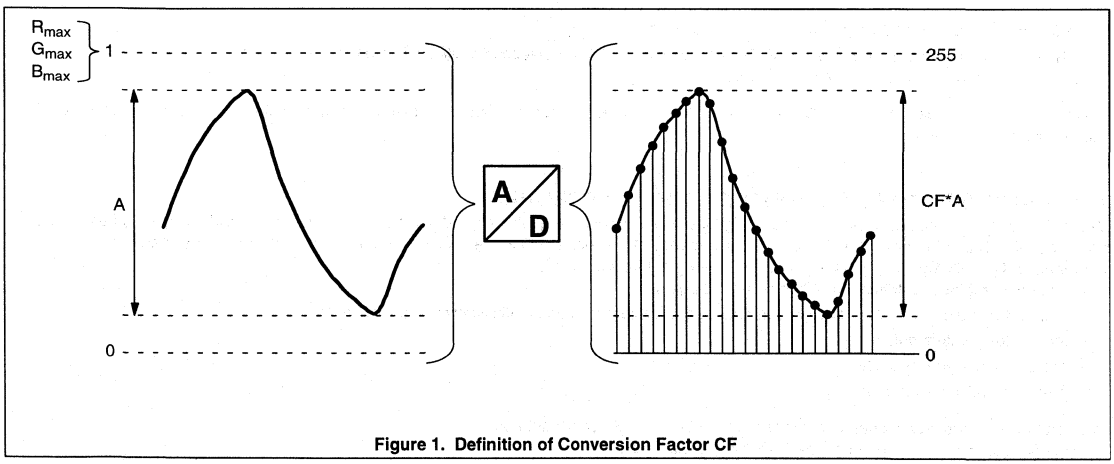


Figure 1. Definition of Conversion Factor CF

2. MAXIMUM AMPLITUDE OF NORMALIZED SIGNALS

With normalized signals the colour separation signals red, green and blue are unity at peak white: $R_{max}=G_{max}=B_{max}=1$.

The colour equations for broadcast signals are based on the NTSC primaries as specified in CCIR Report 624-2. The resulting equation for the luminance signal is:

$$Y=0.299*R+0.587*G+0.114*B \qquad (2.1)$$

which gives: $Y_{p-p}=1$

$|B-Y|$ is maximum for R,G,B=0.0,1 (=blue)
or R,G,B=1,1,0 (=yellow=white minus blue)
which gives: $(B-Y)_{p-p}=2*(1-0.114)=1.772$

$|R-Y|$ is maximum for R,G,B=1,0,0 (=red)
or R,G,B=0,1,1 (=cyan=white minus red)
which gives: $(R-Y)_{p-p}=2*(1-0.299)=1.402$

maximum amplitudes of normalized signals
$Y_{p-p}=1$, $(B-Y)_{p-p}=1.772$, $(R-Y)_{p-p}=1.402$ (2.2)

3. MAIN CODING PARAMETERS OF CCIR REC. 601/656

The digital component signals according to CCIR Rec. 601 have been chosen such that, coded in straight binary

- digital levels 0 and 255 are reserved for synchronization data.
- the luminance signal is to occupy only 220 quantisation levels, to provide working margins, and that black is at level 16.
- the colour difference signals are to occupy 225 quantisation levels and that the zero level is to be level 128 in order to cope with the bipolar nature of the colour difference signals.

The conversion factors follow from these limits on the digital signal range and the maximum peak-to-peak value of the normalized signals:

$signa_{lp-p}$*CF =digital-limit

luminance: Yp-p*CFy=219, which gives CFy=219

colour difference: (B-Y)p-p*CFu=224, CFu=126
(R-Y)p-p*CFv=224, CFv=160

The resulting digital component signals CY, CU, CV are: [1)]

CCIR digital YUV:

$$CY = 219 * Y + 16 \quad (3.1)$$
$$CU = 126 * (B-Y) + 128 \quad (3.2)$$
$$CV = 160 * (R-Y) + 128 \quad (3.3)$$

} binary coded

- the data words 0 and 255 are reserved for data identification
- the video data words are conveyed (CCIR Rec. 656) as a 27Mwords/second multiplex in the following order:
  CU,CY,CV,CY,CU,CY,CV, etc.

in which the word sequence CU,CY,CV, refers to cosited luminance and colour-difference samples and the following word, CY, corresponds to the next luminance sample.

4. PARAMETERS TO BE CONSIDERED FOR TV RECEIVERS

Without doubt the characteristics of analog or digital video component signals at broadcasting side and receiving end are quite different due to the large differences in environment and cost/performance. As a consequence the coding characteristics of digital interface signals are influenced differently by several parameters. Regarding signal amplitudes:

- maximum digital resolution should be balanced against:
- margin for static and dynamic amplitude changes, i.e. tolerances and multiplicative noise (echo, tilt).
- margin for additive noise.
- margin for filter overshoots
- probable limit on saturation

Also on the ratio between signal amplitudes some criteria should be considered:

- simple gain correction to normalized signals e.g. matrixing.
- simple correction between digital decoder and interface.

The list can be extended with requirements from EMC, limitations or advantages of certain IC technologies, application specific requirements etc. Although no choice is best in all cases, consensus is required on the major coding characteristics, due to obvious benefits of standardization. The agreement on this subject between system engineers from the Consumer-Electronics and the Components divisions of Philips (and others) will be explained in the following chapters.

5. MAIN CODING PARAMETERS FOR DIGITAL TV

The component video signals for digital TV are specified as:

digital TV signals:

$$YD = 192 * Y + 16 \quad (5.1)$$
$$UD = 3/4 * 192 * (B-Y) \quad (5.2)$$
$$VD = 192 * (R-Y) \quad (5.3)$$

} straight binary / two's-complement

- multiplex formats are specified for sampling ratios of 4:1:1 and 4:2:2

1) CCIR recommendations use different nomenclature: Y, C_B, C_R.

The colour difference signals are coded in two's complement in order to fit directly to digital arithmetic functions. The difference with the offset binary coding of the CCIR signals (3.1-3.3) is an inversion of the MSB. Concerning the specified conversion factors it will be shown that several criteria on the coding parameters are fulfilled simultaneously:

- digital resolution is practically optimum for 75% colour difference amplitudes.
- signal amplitudes fit conveniently to D2MAC decoders, taking into account 30% headroom for noise.
- UD/VD ratio fits conveniently to the required gain matching ratio for PAL/NTSC colour difference signals.
- amplitude margin is in accordance with the amplitude tolerance of analog decoded signals.
- matrixing to colour selection signals is simple

6. PEAK AMPLITUDE RATIOS

The amplitude ratios should be chosen such that

- the maximum amplitudes are more or less equal in order to maximize digital resolution
- simple gain ratios are required for matrixing
- required correction of the decoded signals is simple

in which 'simple' means that the required gain can be realized with very few additions.

6.1. Probable Maximum Saturation

Due to the gamma of the picture tube the displayed saturation will be higher than the electrical saturation except at 100%. Saturation is less than 100% if the displayed colour has a certain white content, which means that none of the the RGB signals then becomes zero but have a minimum non-zero value. That minimum value becomes relatively smaller if it is displayed via the gamma of the picture tube.

The electrical saturation can be expressed as $\frac{E_{max} - E_{min}}{E_{max}} = 1 - \frac{E_{min}}{E_{max}}$

from which follows: $\text{displayed saturation} = 1 - \left[\frac{E_{min}}{E_{max}}\right]^{gamma}$

in which Emin is the minimum value of the RGB signals in coloured areas
Emax is the maximum value of the RGB signals in coloured areas
gamma is the gamma of the drive-to-output display characteristic.

As a consequence a minor reduction of the maximum displayed saturation will result in a significant reduction of the maximum amplitude of the colour difference signals, e.g. only 5% reduction of the maximum displayed saturation at maximum intensity results from 30% reduction of the electrical saturation at gamma=2.4.

Therefore it is important to take into account that it is most unlikely that natural scenes contain fully saturated colours at maximum intensity. PAL and NTSC have been specified such that at maximum saturation the modulated subcarrier would never swing 'blacker-than-black' by more than 33%. As a consequence the composite signal reaches 100% amplitude at 1/1.33=75% amplitude of saturated colours (yellow and cyan in 100.0.75.0 EBU colour bars). On the same ground also D2MAC colour difference signals are specified for only 77% maximum electrical amplitude. Furthermore the most common luminance step colour bar signals used as test signal result in colour difference signals at 75% of their theoretical maximum amplitude [1].

For these reasons it is supposed that the colour difference signals will most probably not exceed 75% of their theoretical maximum value, which corresponds to 96% maximum displayed saturation at a practical value of gamma=2.4. [2)]

6.2. Ratio of Conversion Factors

For equal amplitudes of the digital signals the ratio of the conversion factors should be inversely proportional to the analog amplitudes. As a consequence the ratio of the conversion factors for equal peak amplitudes at 75% maximum electrical saturation is given by

$$CF_y : CF_u : CF_v = \frac{1}{Y_{p-p}} : \frac{1}{0.75 * (B - Y)_{p-p}} : \frac{1}{0.75 * (R - Y)_{p-p}}$$

Substitution of (2.2) gives CF_y:CF_u:CF_v=1.0.75:0.95 which, after rounding to simple integers, results in:

$$\boxed{CF_y : CF_u : CF_v = 4:3:4} \qquad (6.2)$$

2) It should be noted that the gamma of TV cathode ray tubes is about 2.4 whereas the 'transmitted' gamma is nominally 2.8 which results in an overall gamma of 1.2.

With these simple factors, which will lead to simple (digital) matrixing for R and B, the probable maximum amplitudes of the digital signals are practically equal which gives optimum digital resolution.

6.3. U/V Gain Matching for PAL and NTSC

In NTSC and PAL the colour difference signals U=(B-Y)' and V=(R-Y)' used to modulate the subcarrier are reduced in amplitude with respect to the normalized signals:

$U=0.493*(B-Y)$ (6.3)

$V=0.877*(R-Y)$ [3] (6.4)

As a consequence gain correction is required to obtain normalized signal amplitudes from the demodulated U and V signals. The required gain matching ratio, derived from (6.3) and (6.4), equals 0.493/0.877=9/16. Therefore the ratio CF_u/CF_v=3/4 fits very conveniently to the required gain matching ratio for U/V from decoded PAL or NTSC signals. If the decoded V signal is first reduced with 3/4 (one adder) then the remaining 'error' is 3/4, being the desired CF_u/CF_v. The final correction of 3/4, which will result in equal conversion factors, should then be applied just before or just after DA-conversion to obtain analog colour difference signals with normalized amplitudes, which is common practice for TV receivers.

7. DIGITAL SIGNAL AMPLITUDES

The worst case margins required for noise and amplitude tolerances are quite large. Linear or statistical addition of these margins would lead to insufficient digital resolution at quantisation in 8 bits. As an example, statistical addition of

- 30% headroom for noise (subchapter 7.1)
- 18% tolerance on transmitted burst-to-chrominance ratio [2]
- 2dB gain tolerance of analog decoders (subchapter 7.2)

would require a total range for the colour difference signals of more than two times the nominal value. Therefore the conversion factors have been chosen such

- that there is sufficient margin in amplitude to handle the tolerance of analog decoders

and

- that the margin is according to the 'headroom' for additive noise as proposed by the EBU for D2MAC signals.

If, for certain applications, the margin is considered as insufficient then a kind of gain control should be applied. Gain control on the CVBS signal in front of the digital decoder is already common practice (TDA8708). However automatic gain correction of component signals, i.e. signals originating from external RGB (SCART) or analog decoders, is far more complicated. Detection and control of the amplitudes should then be done on the three component signals simultaneously.

7.1. noise

The criterion for noise handling capability in this context is the probability that signal quality is degraded by noise clipping due to signal quantisation. A probability of one sample per line (about 10^{-3}) seems a reasonable measure for good noise behavior. Assuming that the noise has a Gaussian distribution (white noise), the peak value to be taken into account is then approximately three times the rms value, six times for the peak-to-peak value.

Signal-to-noise-ratios below 0dB are normal operating conditions in the design of TV circuits. E.g. for burst processing it is common practice to design the subcarrier regenerator for stable output (less than 5 degree rms phase noise) at S/N=-10dB ($CVBS_{p-p}/Noise_{rms}$) [3]. In that case the required margin for noise amplitude would be approximately twenty times larger then the CVBS signal amplitude.

Although it is unlikely that such a margin is present in the analog prestages at nominal CVBS amplitude, it is obvious that a compromise is necessary between quantisation noise and the margin for external noise. Therefore the worst probable case of S/N for D2MAC reception is used as a guideline [4].

In the D2MAC system the carrier is frequency-modulated by the baseband signal [5]. In FM systems there is a rather sharp threshold between carrier-to-noise ratios for 'good' and 'bad' S/N of the demodulated signal. Therefore the assumption is made that the worst probable S/N for D2MAC reception occurs at a carrier-to-noise ratio of 11dB, just above the threshold. That results in an unweighted noise level of about -26dB (=0.05) [4,6] for the demodulated signal (depending on the filter response of the prestages). That means that 6*0.05=30% headroom has to be taken into account for additive noise.

7.2. MAC Decoder

MAC decoding in principle is time-demultiplexing. Therefore the MAC decoder is transparent (no internal gain) with respect to digital amplitudes. If the MAC (mid-range) clamping level is referred to as zero and if the peak-to-peak range is unity, then the MAC signals according to the D2-MAC specification [5] are transmitted as:

$Ym=Y-0.5,\ Um=0.733*(B-Y)$ and $Vm=0.927*(R-Y)$ [4] (7.1)

3) In NTSC the vectors I and Q are also derived from (B-Y)' and (R-Y)'.

It is supposed that regarding DC level:
- the digitized grey clamping level equals 128 (analog 'zero' becomes digital 128)

and regarding AC input:
- the ratio between the nominal digital peak-to-peak amplitude and the maximum range (256) of the ADC equals MR (Modulation Range).

then the corresponding digital component signals will be (See Fig. 2):

```
MY=128+MR*256*(Y-0.5)                    (7.2)
MU=128+MR*256*0.733*(B-Y)                (7.3)
MV=128+MR*256*0.927*(R-Y)                (7.4)
```

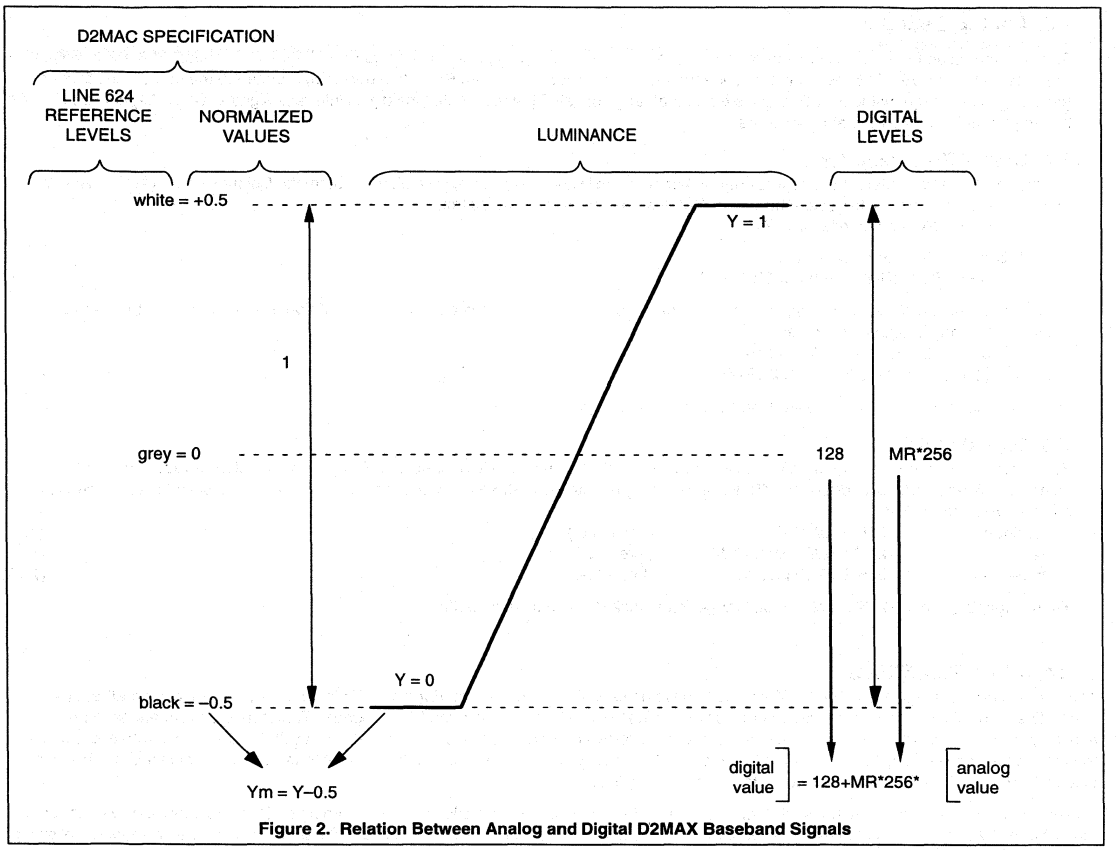


Figure 2. Relation Between Analog and Digital D2MAX Baseband Signals

4) The colour difference signals in the D2MAC multiplex are scaled to unity amplitude at 77% of their maximum value. As a consequence the scale factors for B-Y and R-Y are 1/(0.77*1.772)=0.733 and 1/(0.77*1.402)=0.927 respectively.

With 30% headroom for additive noise (MR=0.77) the decoded signals (7.2)-(7.4) and the resulting conversion factors become:

MY=197*Y+29 CF_y=197 (7.5)
MU=144*(B-Y)+128 CF_u=3/4*192 (7.6)
MV=183*(R-Y)+128 CF_v=183=192/1.05 (7.7)

Consequences for interfacing:
- luminance black level should be corrected to 16 (one adder).
- error on CFy results in an acceptable saturation error
- V-signal has to be corrected with 192/183w17/16*63/64 (two adders)
- no correction is needed for the U-signal

7.3. Analog Decoder

An accepted value for the specified tolerance on the output signals of analog colour decoders (e.g.TDA4555) is +/-2dB (0.8-1.25). With a fixed digital black level of 16 the available range for luminance is 255-16+1=240. Reduction with 2dB, rounded to the nearest multiple of 4 (resulting in an integer value for CFu), gives a nominal range of 192. That means that the digital interface signals (CF_y=192) can also handle the amplitude tolerance of analog decoders.

7.4. Digital PAL Decoder

In PAL and NTSC decoders the amplitude of the demodulated U and V signals is, via action of Automatic Colour Control (ACC), directly related to the amplitude of the colour burst. For PAL the relation can be derived from

BP=peak burst amplitude=3/7

Substitution in in (6.3) and (6.4) gives

U=1.15*BP*(B-Y) and V=2.05*BP*(R-Y) (7.8)

If the burst peak amplitude in the digital PAL decoder is kept at BP=125 and the amplitude of the V signal is reduced with 3/4 then the resulting UD and VD signals become:

UD=1.15*125*(B-Y)=3/4*192*(B-Y) (7.9)
VD=3/4*2.05*125*(R-Y)=192*(R-Y) (7.10)

which is in accordance with the desired interface signals (5.1)-(5.3).

7.5. Digital Matrixing

For certain applications, e.g. gamma correction for LCD, it might be required to operate on colour separation signals rather than colour difference signals. With six adders the YD, UD and VD signals can be matrixed to digital luminance, red and blue signals normalized to a conversion factor of 216.

luminance:	216*Y=9/8*YD	(one adder)	(7.11)
red:	216*R=9/8*YD+3/2*UD	(three adders)	(7.12)
blue:	216*B=9/8*(YD+VD)	(two adders)	(7.13)

These signals cover 90% (216) of the total range from black (16) to maximum (255).

8. DATA MULTIPLEXING

The video interface signal according to CCIR Rec.656 is based on 4:2:2 sample ratio. For digital TV the 4:1:1 sample ratio is an attractive alternative, in particular for memory based processing of video originating from decoded CVBS signals. Therefore data formats have been specified for 4:1:1 and 4:2:2 The luminance and colour difference signals are conveyed as separate data with identical clock rate according to the luminance sample rate, 13.5MHz or 27MHz in case of frequency doubling. Luminance data is transferred on eight data lines, whereas the colour difference signals are multiplexed on four or eight data lines.

The 4:2:2 multiplex format is chosen such that it can simply be made from the multiplexed data according to CCIR Rec.656. In the 4:1:1 format the UD and VD signals are multiplexed on separate data lines. The multiplex formats of the colour difference samples are given in the following tables together with the cosited luminance sample.

'4:2:2' format

dataline	samplebits	
Y7 Y6 ... Y0	T7 Y6 ... Y0	next Y
C7 C6 ... C0	U7 U6 ... U0	V7 V6 ... V0
time-slot	0	1

'4:1:1' format

dataline	samplebits			
Y7 76 ... Y0	Y7 Y6 ... Y0	next Y-samples		
C7 C6 C5 C4	U7 U6 V7 V6	U5 U4 V5 V4	U3 U2 V3 V2	U1 U0 V1 V0
time-slot	0	1	2	3

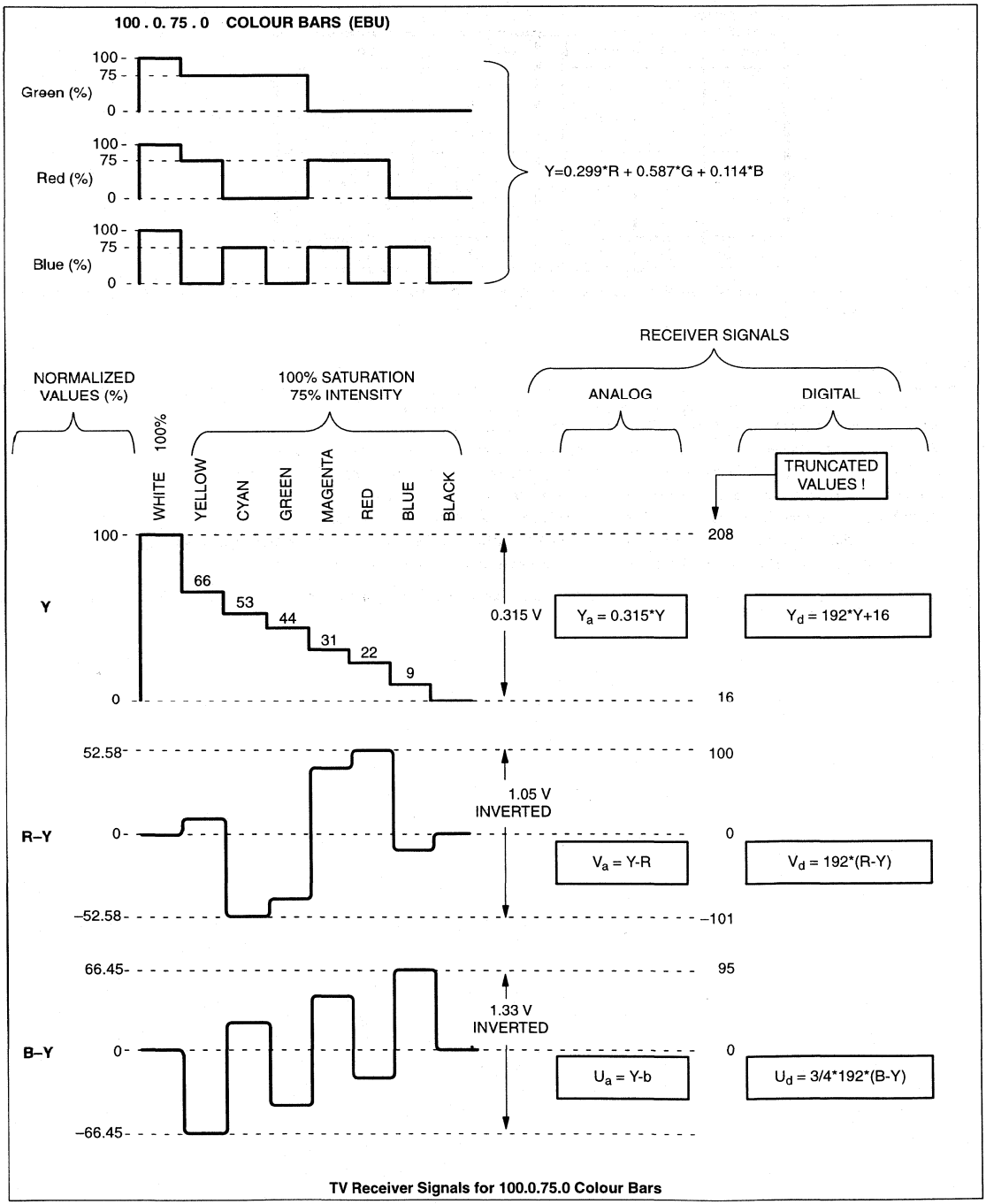
The start of the multiplex frame is identified by the positive going edge of a control signal (BLN or HREF or MUX, depending on the integrated circuit used as source).

9. CONCLUSION

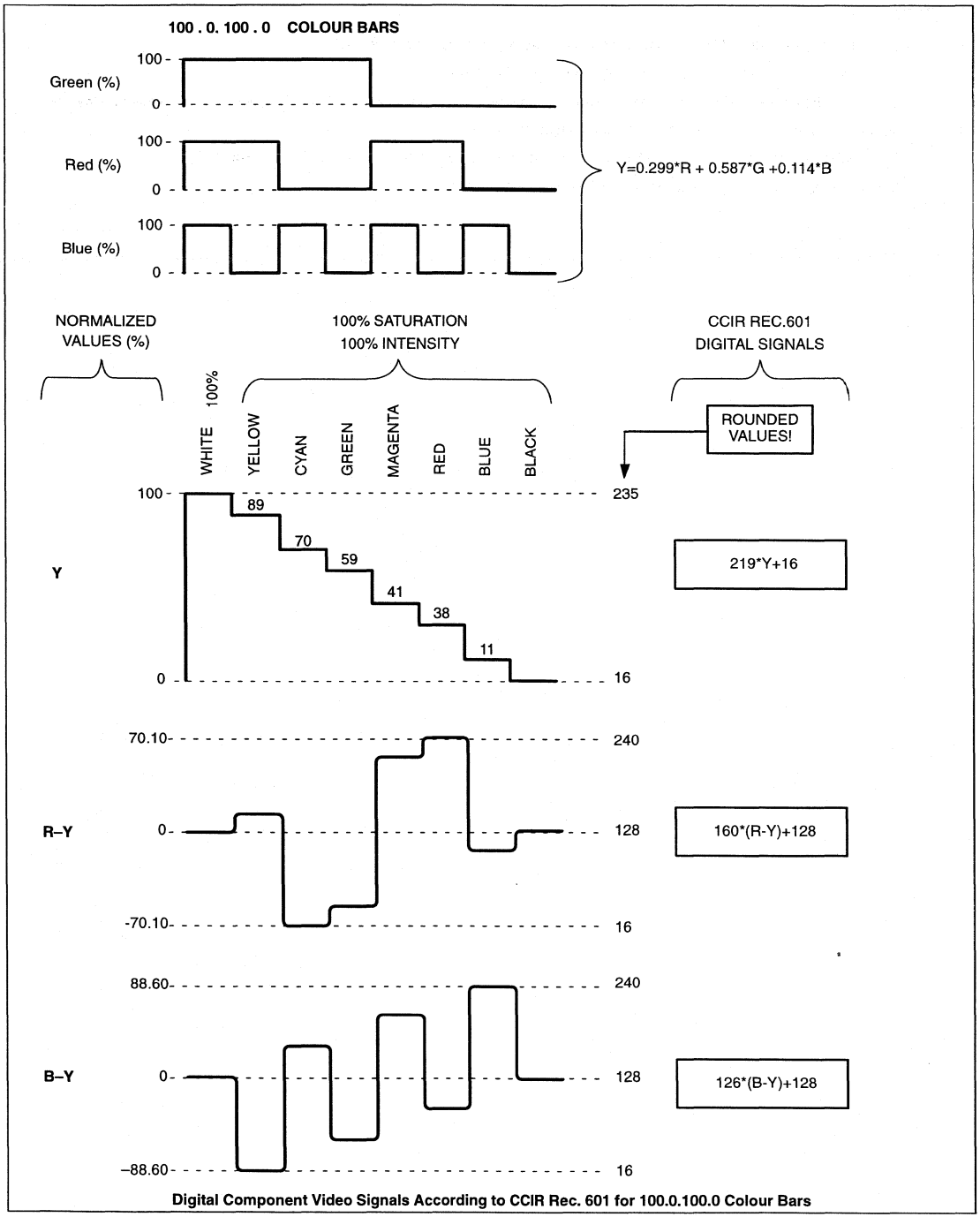
Signal amplitudes and multiplexing formats for digital component video signals as used for interconnecting TV receiver functions are based on receiver specific requirements. Concerning amplitudes the following criteria are fulfilled:

- digital resolution is practically optimum for 75% colour difference amplitudes.
- signal amplitudes fit conveniently to D2MAC decoders, taking into account 30% headroom for noise.
- UD/VD ratio fits conveniently to the required gain matching ratio for PAL/NTSC colour difference signals.
- amplitude margin is in accordance with the amplitude tolerance of analog decoded signals.
- matrixing to colour selection signals is simple Data multiplexing parameters are specified for:
- 4:2:2 as well as 4:1:1 sample frequency ratio to cope with different bandwidths, in particular for memory applications
- clock frequency equal to luminance sample frequency for application with or without frequency doubling

The following figures give the characteristic amplitudes of the digital component video signals according to the specifications for application in TV receivers and according to CCIR Rec.601.



TV Receiver Signals for 100.0.75.0 Colour Bars



Digital Component Video Signals According to CCIR Rec. 601 for 100.0.100.0 Colour Bars

REFERENCES

[1] CCIR Recommendation 471-1; "Nomenclature and description of colour bar signals"

[2] IBA Technical Review, part 2 Technical Reference Book, July 1974

[3] Donald Richman; Proc. IRE, vol. 43, 1954; "Colour-carrier reference phase synchronization accuracy in NTSC colour television"

[4] Appendix to part 2 of [5]; "Guidelines for system implementation"

[5] EBU Technical centre; Tech.3258-E; October 1986; "Specification of the systems of the MAC/packet family"

[6] Arno Neelen, Philips Components division, PCALE; private communication.

CCIR REC.601.4 Encoding parameters of digital televison for studios

SECTION 11B: DIGITAL TELEVISION

RECOMMENDATION ITU-R BT.601-4

ENCODING PARAMETERS OF DIGITAL TELEVISION FOR STUDIOS

(Questions ITU-R 25/11, ITU-R 60/11 and ITU-R 61/11)

(1982-1986-1990-1992-1994)

The ITU Radiocommunication Assembly,

considering

a) that there are clear advantages for television broadcasters and programme producers in digital studio standards which have the greatest number of significant parameter values common to 525-line and 625-line systems;

b) that a worldwide compatible digital approach will permit the development of equipment with many common features, permit operating economies and facilitate the international exchange of programmes;

c) that an extensible family of compatible digital coding standards is desirable. Members of such a family could correspond to different quality levels, facilitate additional processing required by present production techniques, and cater for future needs;

d) that a system based on the coding of components is able to meet some, and perhaps all, of these desirable objectives;

e) that the co-siting of samples representing luminance and colour-difference signals (or, if used, the red, green and blue signals) facilitates the processing of digital component signals, required by present production techniques,

recommends

that the following be used as a basis for digital coding standards for television studios in countries using the 525-line system as well as in those using the 625-line system:

1. Component coding

The digital coding should be based on the use of one luminance and two colour-difference signals (or, if used, the red, green and blue signals).

The spectral characteristics of the signals must be controlled to avoid aliasing whilst preserving the pass-band response. When using one luminance and two colour-difference signals as defined in Table 1 suitable filters are defined in Figs. 4 and 5. When using E'_R, E'_G, E'_B signals or luminance and colour-difference signals as defined in Table 2 a suitable filter characteristic is shown in Fig. 4.

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2. Extensible family of compatible digital coding standards

The digital coding should allow the establishment and evolution of an extensible family of compatible digital coding standards. It should be possible to interface simply between any two members of the family.

The member of the family to be used for the standard digital interface between main digital studio equipment, and for international programme exchange (i.e. for the interface with video recording equipment and for the interface with the transmission system) should be that defined in § 4.

In a higher member of the family the sampling frequencies of the luminance and colour-difference signals (or, if used, the red, green and blue signals) are related by the ratio 4:4:4. The specifications for the 4:4:4 member are defined in § 5.

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TABLE 1

4:2:2 member of the family

Parameters	525-line, 60 field/s systems	625-line, 50 field/s systems
1. Coded signals: Y, C_R, C_B	These signals are obtained from gamma pre-corrected signals, namely: E'_Y, $E'_R - E'_Y$, $E'_B - E'_Y$ (Annex 1, § 2 refers)	
2. Number of samples per total line: – luminance signal (Y) – each colour-difference signal (C_R, C_B)	858 429	864 432
3. Sampling structure	Orthogonal, line, field and frame repetitive. C_R and C_B samples co-sited with odd (1st, 3rd, 5th, etc.) Y samples in each line	
4. Sampling frequency: – luminance signal – each colour-difference signal	13.5 MHz 6.75 MHz The tolerance for the sampling frequencies should coincide with the tolerance for the line frequency of the relevant colour television standard	
5. Form of coding	Uniformly quantized PCM, 8 (optionally 10) bits per sample, for the luminance signal and each colour-difference signal	
6. Number of samples per digital active line: – luminance signal – each colour-difference signal	720 360	
7. Analogue-to-digital horizontal timing relationship: – from end of digital active line to O_H	16 luminance clock periods	12 luminance clock periods
8. Correspondence between video signal levels and quantization levels: – scale – luminance signal – each colour-difference signal	(See § 3.4) (Values are decimal) 0 to 255 220 quantization levels with the black level corresponding to level 16 and the peak white level corresponding to level 235. The signal level may occasionally excurse beyond level 235 225 quantization levels in the centre part of the quantization scale with zero signal corresponding to level 128	
9. Code-word usage	Code words corresponding to quantization levels 0 and 255 are used exclusively for synchronization. Levels 1 to 254 are available for video	

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3. Specifications applicable to any member of the family

3.1 Sampling structures should be spatially static. This is the case, for example, for the orthogonal sampling structure specified in § 4 for the 4:2:2 member of the family and in § 5 for the 4:4:4 member.

3.2 If the samples represent luminance and two simultaneous colour-difference signals, each pair of colour-difference samples should be spatially co-sited. If samples representing red, green and blue signals are used they should be co-sited.

TABLE 2

4:4:4 member of the family

Parameters	525-line, 60 field/s systems	625-line, 50 field/s systems
1. Coded signals: Y, C_R, C_B or R, G, B	These signals are obtained from gamma pre-corrected signals, namely: $E'_Y, E'_R - E'_Y, E'_B - E'_Y$ or E'_R, E'_G, E'_B	
2. Number of samples per total line for each signal	858	864
3. Sampling structure	Orthogonal, line, field and frame repetitive. The three sampling structures to be coincident and coincident also with the luminance sampling structure of the 4:2:2 member	
4. Sampling frequency for each signal	13.5 MHz	
5. Form of coding	Uniformly quantized PCM, 8 (optionally 10) bits per sample	
6. Duration of the digital active line expressed in number of samples	720	
7. Correspondence between video signal levels and the 8 most significant bits (MSB) of the quantization level for each sample:	(See § 3.4) (Values are decimal)	
– scale	0 to 255	
– R, G, B or luminance signal[1]	220 quantization levels with the black level corresponding to level 16 and the peak white level corresponding to level 235. The signal level may occasionally excurse beyond level 235	
– each colour-difference signal[1]	225 quantization levels in the centre part of the quantization scale with zero signal corresponding to level 128	

(1) If used.

3.3 The digital standard adopted for each member of the family should permit worldwide acceptance and application in operation; one condition to achieve this goal is that, for each member of the family, the number of samples per line specified for 525-line and 625-line systems shall be compatible (preferably the same number of samples per line).

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3.4 In applications of these specifications, the contents of digital words are expressed in both decimal and hexadecimal forms, denoted by the suffixes "d" and "h" respectively.

To avoid confusion between 8-bit and 10-bit representations, the eight most-significant bits are considered to be an integer part while the two additional bits, if present, are considered to be fractional parts.

For example, the bit pattern 10010001 would be expressed as 145_d or 91_h, whereas the pattern 1001000101 would be expressed as 145.25_d or 91.4_h.

Where no fractional part is shown, it should be assumed to have the binary value 00.

4. Encoding parameter values for the 4:2:2 member of the family

The specification (Table 1) applies to the 4:2:2 member of the family, to be used for the standard digital interface between main digital studio equipment and for international programme exchange.

5. Encoding parameter values for the 4:4:4 member of the family

The following specification given in Table 2 applies to the 4:4:4 member of the family suitable for television source equipment and high-quality video signal processing applications.

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ANNEX 1

Definition of signals used in the digital coding standards

1. Relationship of digital active line to analogue sync reference

The relationship between 720 digital active line luminance samples and the analogue synchronizing references for 625-line and 525-line systems is shown in Fig. 1. A luminance sample is co-sited with the analogue line reference point O_H.

The identification numbers of the samples that make up the digital line, the digital line blanking and the digital active line are shown in Fig. 2. The respective numbers of colour-difference samples can be obtained by dividing the number of luminance samples by two. The (12, 132) and (16, 122) were chosen symmetrically to dispose the digital active line about the permitted variations. They do not form part of the digital line specification and relate only to the analogue interface.

The numbers of the digital lines that make up the digital fields and the digital field blanking intervals are shown in Fig. 3.

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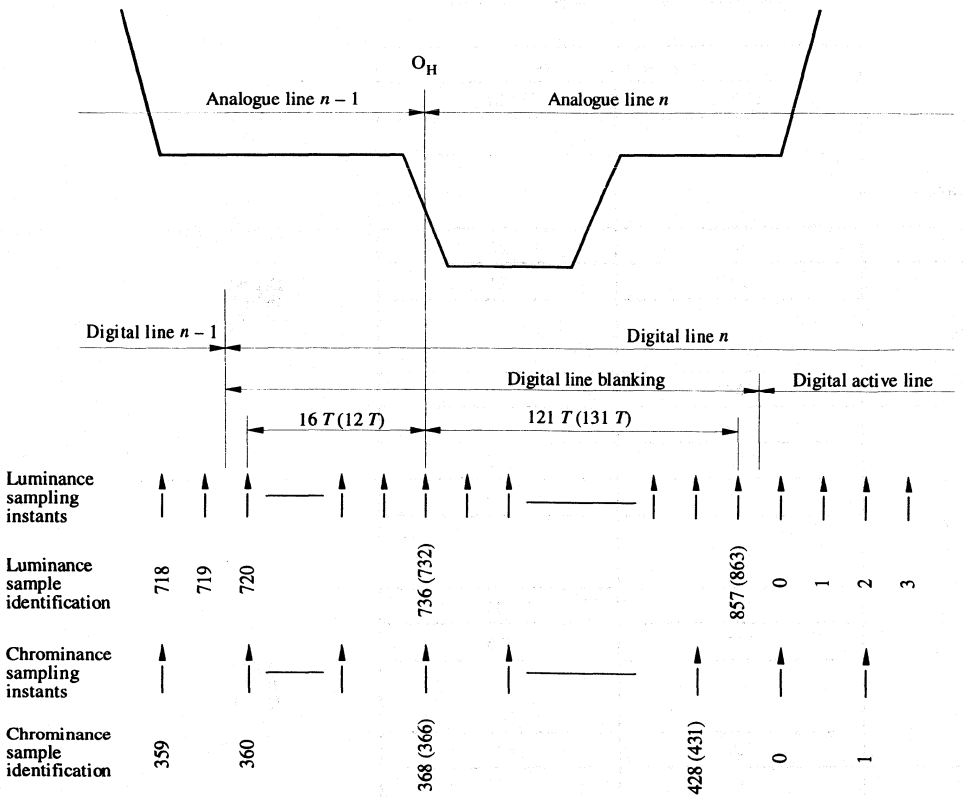
FIGURE 1

Relationship between video samples and the analogue line synchronization

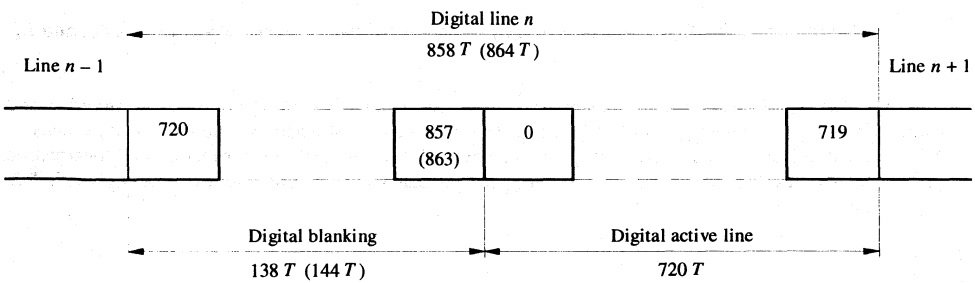


Note 1 – Sample identification numbers in parentheses are for 625-line systems where these differ from those of 525-line systems. T represents the luminance sampling period.

D01

FIGURE 2

Definitions of the digital line samples



Note 1 – Sample identification numbers and sample periods in parentheses are for 625-line systems where these differ from those of 525-line systems.

D02

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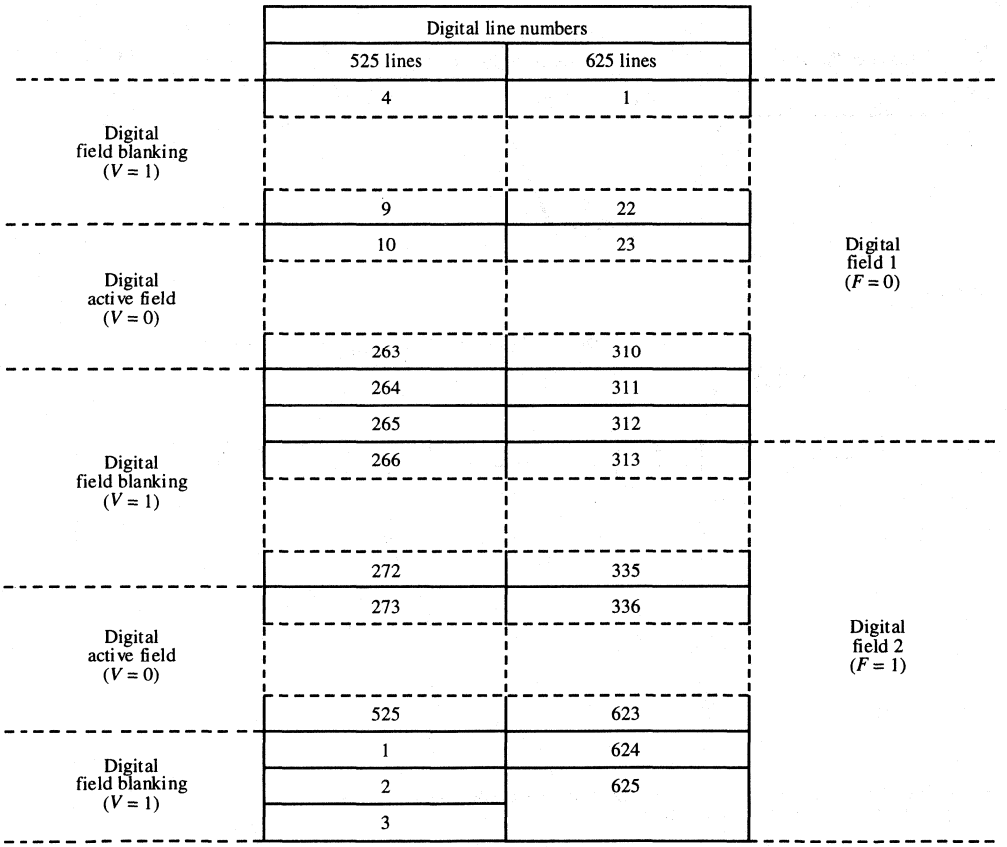
FIGURE 3

Line numbers in the digital picture (frame)



Note 1 – Digital line numbers correspond to the associated analogue line numbers defined in Recommendation ITU-R BT.470.

D03

2. Definition of the digital signals Y, C_R, C_B, from the primary (analogue) signals E'_R, E'_G and E'_B

This section describes, with a view to defining the signals Y, C_R, C_B, the rules for construction of these signals from the primary analogue signals E'_R, E'_G and E'_B. The signals are constructed by following the three stages described in § 2.1, 2.2 and 2.3 below. The method is given as an example, and in practice other methods of construction from these primary signals or other analogue or digital signals may produce identical results. An example is given in § 2.4.

CCIR REC.601.4 Encoding parameters of digital televison for studios

2.1 *Construction of luminance (E'_Y) and colour-difference ($E'_R - E'_Y$) and ($E'_B - E'_Y$) signals*

The construction of luminance and colour-difference signals is as follows:

$$E'_Y = 0.299\,E'_R + 0.587\,E'_G + 0.114\,E'_B$$

whence:

$$\begin{aligned}(E'_R - E'_Y) &= E'_R - 0.299\,E'_R - 0.587\,E'_G - 0.114\,E'_B \\ &= 0.701\,E'_R - 0.587\,E'_G - 0.114\,E'_B\end{aligned}$$

and:

$$\begin{aligned}(E'_B - E'_Y) &= E'_B - 0.299\,E'_R - 0.587\,E'_G - 0.114\,E'_B \\ &= -0.299\,E'_R - 0.587\,E'_G + 0.886\,E'_B\end{aligned}$$

Taking the signal values as normalized to unity (e.g. 1.0 V maximum levels), the values obtained for white, black and the saturated primary and complementary colours are as follows:

TABLE 3

Normalized signal values

Condition	E'_R	E'_G	E'_B	E'_Y	$E'_R - E'_Y$	$E'_B - E'_Y$
White	1.0	1.0	1.0	1.0	0	0
Black	0	0	0	0	0	0
Red	1.0	0	0	0.299	0.701	–0.299
Green	0	1.0	0	0.587	–0.587	–0.587
Blue	0	0	1.0	0.114	–0.114	0.886
Yellow	1.0	1.0	0	0.886	0.114	–0.886
Cyan	0	1.0	1.0	0.701	–0.701	0.299
Magenta	1.0	0	1.0	0.413	0.587	0.587

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2.2 *Construction of re-normalized colour-difference signals (E'_{C_R} and E'_{C_B})*

Whilst the values for E'_Y have a range of 1.0 to 0, those for $(E'_R - E'_Y)$ have a range of +0.701 to −0.701 and for $(E'_B - E'_Y)$ a range of +0.886 to −0.886. To restore the signal excursion of the colour-difference signals to unity (i.e. +0.5 to −0.5), coefficients can be calculated as follows:

$$K_R = \frac{0.5}{0.701} = 0.713; \qquad K_B = \frac{0.5}{0.886} = 0.564$$

Then:

$$E'_{C_R} = 0.713\,(E'_R - E'_Y) = 0.500\,E'_R - 0.419\,E'_G - 0.081\,E'_B$$

and:

$$E'_{C_B} = 0.564\,(E'_B - E'_Y) = -0.169\,E'_R - 0.331\,E'_G + 0.500\,E'_B$$

where E'_{C_R} and E'_{C_B} are the re-normalized red and blue colour-difference signals respectively (see Notes 1 and 2).

Note 1 – The symbols E'_{C_R} and E'_{C_B} will be used only to designate re-normalized colour-difference signals, i.e. having the same nominal peak-to-peak amplitude as the luminance signal E'_Y thus selected as the reference amplitude.

Note 2 – In the circumstances when the component signals are not normalized to a range of 1 to 0, for example, when converting from analogue component signals with unequal luminance and colour-difference amplitudes, an additional gain factor will be necessary and the gain factors K_R, K_B should be modified accordingly.

2.3 *Quantization*

In the case of a uniformly-quantized 8-bit binary encoding, 2^8, i.e. 256, equally spaced quantization levels are specified, so that the range of the binary numbers available is from 0000 0000 to 1111 1111 (00 to FF in hexadecimal notation), the equivalent decimal numbers being 0 to 255, inclusive.

In the case of the 4:2:2 system described in this Recommendation, levels 0 and 255 are reserved for synchronization data, while levels 1 to 254 are available for video.

Given that the luminance signal is to occupy only 220 levels, to provide working margins, and that black is to be at level 16, the decimal value of the luminance signal, $\overline{Y}$, prior to quantization, is:

$$\overline{Y} = 219\,(E'_Y) + 16$$

and the corresponding level number after quantization is the nearest integer value.

Similarly, given that the colour-difference signals are to occupy 225 levels and that the zero level is to be level 128, the decimal values of the colour-difference signals, $\overline{C}_R$ and $\overline{C}_B$, prior to quantization are:

$$\overline{C}_R = 224\,[0.713\,(E'_R - E'_Y)] + 128$$

and:

$$\overline{C}_B = 224\,[0.564\,(E'_B - E'_Y)] + 128$$

which simplify to the following:

$$\overline{C}_R = 160\,(E'_R - E'_Y) + 128$$

and:

$$\overline{C}_B = 126\,(E'_B - E'_Y) + 128$$

and the corresponding level number, after quantization, is the nearest integer value.

The digital equivalents are termed Y, C_R and C_B.

2.4 *Construction of Y, C_R, C_B via quantization of E'_R, E'_G, E'_B*

In the case where the components are derived directly from the gamma pre-corrected component signals E'_R, E'_G, E'_B, or directly generated in digital form, then the quantization and encoding shall be equivalent to:

$$E'_{R_D}\ (\text{in digital form}) = \text{int}\,(219\,E'_R) + 16$$

$$E'_{G_D}\ (\text{in digital form}) = \text{int}\,(219\,E'_G) + 16$$

$$E'_{B_D}\ (\text{in digital form}) = \text{int}\,(219\,E'_B) + 16$$

Then:

$$Y = \frac{77}{256} E'_{R_D} + \frac{150}{256} E'_{G_D} + \frac{29}{256} E'_{B_D}$$

$$C_R = \frac{131}{256} E'_{R_D} - \frac{110}{256} E'_{G_D} - \frac{21}{256} E'_{B_D} + 128$$

$$C_B = -\frac{44}{256} E'_{R_D} - \frac{87}{256} E'_{G_D} + \frac{131}{256} E'_{B_D} + 128$$

taking the nearest integer coefficients, base 256. To obtain the 4:2:2 components Y, C_R, C_B, low-pass filtering and sub-sampling must be performed on the 4:4:4 C_R, C_B signals described above. Note should be taken that slight differences could exist between C_R, C_B components derived in this way and those derived by analogue filtering prior to sampling.

2.5 Limiting of Y, C_R, C_B signals

Digital coding in the form of Y, C_R, C_B signals can represent a substantially greater gamut of signal values than can be supported by the corresponding ranges of R, G, B signals. Because of this it is possible, as a result of electronic picture generation or signal processing, to produce Y, C_R, C_B signals which, although valid individually, would result in out-of-range values when converted to R, G, B. It is both more convenient and more effective to prevent this by applying limiting to the Y, C_R, C_B signals than to wait until the signals are in R, G, B form. Also, limiting can be applied in a way that maintains the luminance and hue values, minimizing the subjective impairment by sacrificing only saturation.

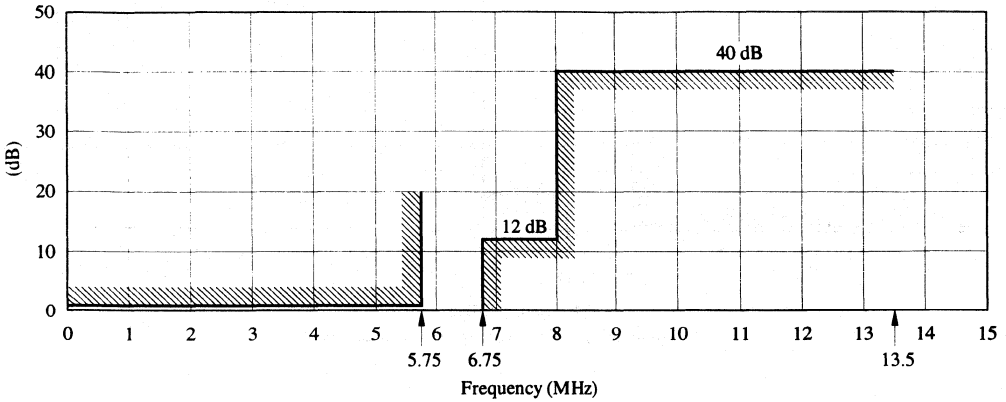
CCIR REC.601.4 Encoding parameters of digital televison for studios

ANNEX 2

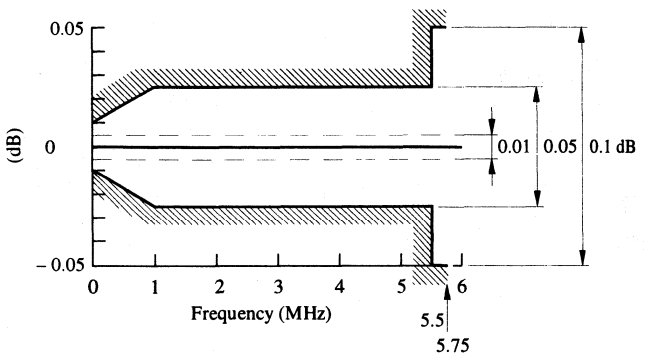
Filtering characteristics

FIGURE 4

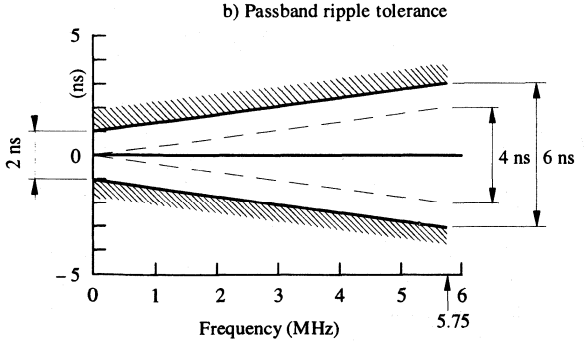
Specification for a luminance or *RGB* signal filter used when sampling at 13.5 MHz



a) Template for insertion loss/frequency characteristic



b) Passband ripple tolerance



c) Passband group-delay tolerance

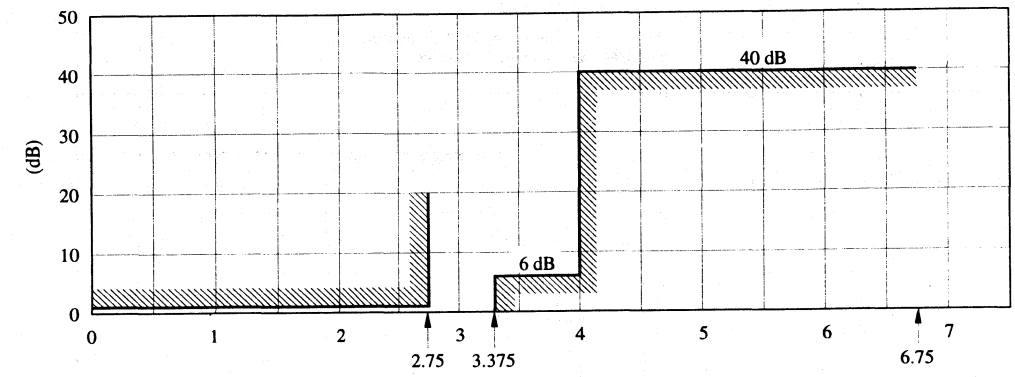
Note 1 – The lowest indicated values in b) and c) are for 1 kHz (instead of 0 MHz).

D04

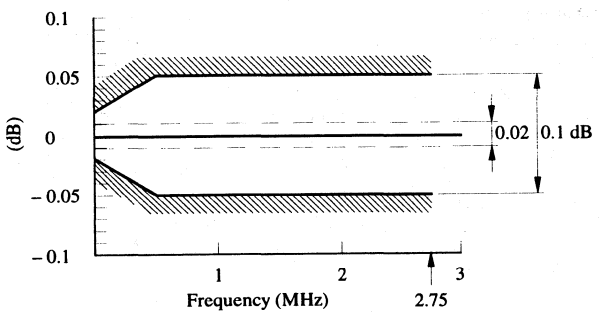
CCIR REC.601.4 Encoding parameters of digital televison for studios

FIGURE 5

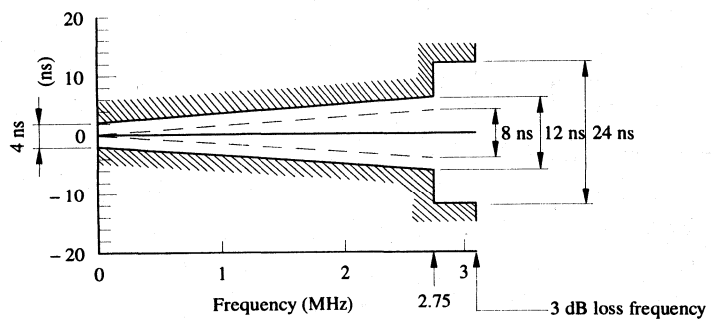
Specification for a colour-difference signal filter used when sampling at 6.75 MHz



a) Template for insertion loss/frequency characteristic



b) Passband ripple tolerance



c) Passband group-delay tolerance

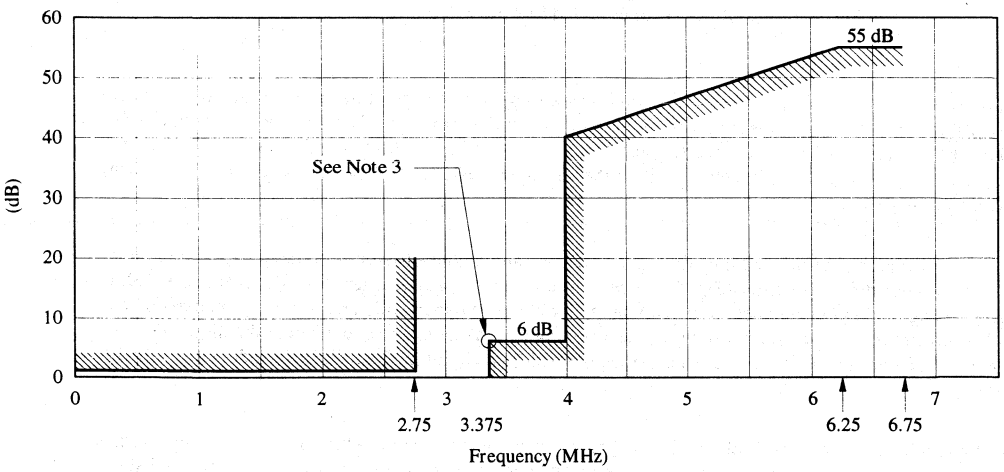
Note 1 – The lowest indicated values in b) and c) are for 1 kHz (instead of 0 MHz).

D05

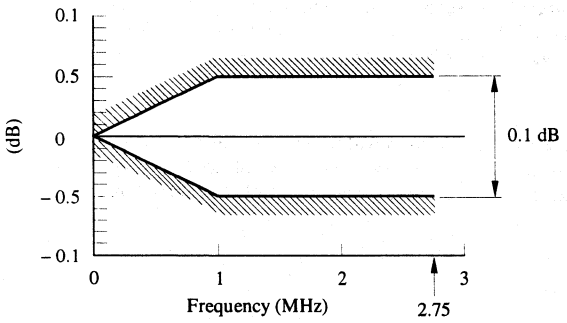
CCIR REC.601.4 Encoding parameters of digital televison for studios

FIGURE 6

Specification for a digital filter for sampling-rate conversion from 4:4:4 to 4:2:2 colour-difference signals



a) Template for insertion loss/frequency characteristic



b) Passband ripple tolerance

Notes to Figs. 4, 5 and 6:

Note 1 – Ripple and group delay are specified relative to their values at 1 kHz. The fill lines are practical limits and the dashed lines give suggested limits for the theoretical design.

Note 2 – In the digital filter, the practical and design limits are the same. The delay distortion is zero, by design.

Note 3 – In the digital filter (Fig. 6), the amplitude/frequency characteristic (on linear scales) should be skew-symmetrical about the half-amplitude point, which is indicated on the figure.

Note 4 – In the proposals for the filters used in the encoding and decoding processes, it has been assumed that, in the post-filters which follow digital-to-analogue conversion, correction for the (sin *x*/*x*) characteristic of the sample-and-hold circuits is provided.

D06

CCIR REC.601.4 Encoding parameters of digital televison for studios

ANNEX 3

Some guidance on the practical implementation of the filters recommended in Annex 2

In the proposals for the filters used in the encoding and decoding processes, it has been assumed that, in the post-filters which follow digital-to-analogue conversion, correction for the (sin x/x) characteristic is provided. The passband tolerances of the filter plus (sin x/x) corrector plus the theoretical (sin x/x) characteristic should be the same as given for the filters alone. This is most easily achieved if, in the design process, the filter, (sin x/x) corrector and delay equalizer are treated as a single unit.

The total delays due to filtering and encoding the luminance and colour-difference components should be the same. The delay in the colour-difference filter (Fig. 5) is double that of the luminance filter (Fig. 4). As it is difficult to equalize these delays using analogue delay networks without exceeding the passband tolerances, it is recommended that the bulk of the delay differences (in integral multiples of the sampling period) should be equalized in the digital domain. In correcting for any remainder, it should be noted that the sample-and-hold circuit in the decoder introduces a flat delay of one half a sampling period.

The passband tolerances for amplitude ripple and group delay are recognized to be very tight. Present studies indicate that it is necessary so that a significant number of coding and decoding operations in cascade may be carried out without sacrifice of the potentially high quality of the 4:2:2 coding standard. Due to limitations in the performance of currently available measuring equipment, manufacturers may have difficulty in economically verifying compliance with the tolerances of individual filters on a production basis. Nevertheless, it is possible to design filters so that the specified characteristics are met in practice, and manufacturers are required to make every effort in the production environment to align each filter to meet the given templates.

The specifications given in Annex 2 were devised to preserve as far as possible the spectral content of the Y, C_R, C_B signals throughout the component signal chain. It is recognized, however, that the colour-difference spectral characteristic must be shaped by a slow roll-off filter inserted at picture monitors, or at the end of the component signal chain.

SECTION 11A: CHARACTERISTICS OF SYSTEMS FOR MONOCHROME AND COLOUR TELEVISION

REPORT 624-4

CHARACTERISTICS OF TELEVISION SYSTEMS

(Question 1/11)

(1974-1978-1982-1986-1990)

The following Tables, given for information purposes, contain details of a number of different television systems in use at the time of the XVIIth Plenary Assembly of the CCIR, Düsseldorf, 1990.

A list of countries and geographical areas, and the television systems used, are given in Annex I.

Specifications of the SECAM IV colour television system, which is still under consideration, are given in Annex II.

Information on the results of the comparative laboratory tests carried out on the various colour television systems in the period 1963-1966 by broadcasting authorities, administrations and industrial organizations, together with the main parameters of systems may be found in Reports 406 and 407, XIIth Plenary Assembly, New Delhi, 1970.

All television systems listed in this Report employ an aspect ratio of the picture display (width/height) of 4/3, a scanning sequence from left to right and from top to bottom and an interlace ratio of 2/1, resulting in a picture (frame) frequency of half the field frequency. All systems are capable of operating independently of the power supply frequency.

TABLE I – *Basic characteristics of video and synchronizing signals*

Item	Caracteristics		System								
			M	N [1]	B, G	H	I	D, K	K1	L	Rec. 472 [2]
1	Number of lines per picture (frame)		525	625	625	625	625	625	625	625	625
2	Field frequency, nominal value (fields/second) [3]		60 (59.94)	50	50	50	50	50	50	50	50
3	Line frequency f_H and tolerance when operated non-synchronously (Hz) [3] [4]		15 750 (15 734.264 ± 0.0003%)	15 625 ± 0.15% (± 0.00014%)	15 625 [5] ± 0.02% (± 0.0001%)	15 625 ± 0.02% (± 0.0001%)	15 625 ± 0.00002% [6]	15 625 [5] ± 0.02% (± 0.0001%)	15 625 ± 0.02% (± 0.0001%)	15 625 ± 0.02% (± 0.0001%)	15 625 ± 0.02% (± 0.0001%)
3 *(a)*	Maximum variation rate of line frequency valid for monochrome transmission (%/s) [7] [8]		0.15		0.05	0.05	0.05	0.05	0.05	0.05	
4 [10]	Nominal and peak levels of the composite video signal (see Fig. 1) (%)	blanking level (reference level)	0	0	0	0	0	0	0	0	
		peak-white-level	100	100	100	100	100	100	100	100	
		synchronizing level	−40	−40 (−43)	−43	−43	−43	−43	−43	−43	
		difference between black and blanking level	7.5 ± 2.5 [9]	7.5 ± 2.5 (0)	0	0	0	0-7	0 (colour) 0-7 (mono.)	0 (colour) 0-7 (mono.)	$0\ ^{+5}_{-0}$
		peak level including chrominance signal	120		133 [11]		133	115 [12]	115 [12]	124 [12]	

TABLE I *(continued)*

Item	Caracteristics	System								
		M	N ([1])	B, G	H	I	D, K	K1	L	Rec. 472 ([2])
5	Assumed gamma of display device for which pre-correction of monochrome signal is made	2.2	2.2 (2.8)	2.8 ([13])						([14])
6	Nominal video bandwidth (MHz)	4.2	4.2	5	5	5.5	6	6	6	5.0 or 5.5 or 6.0
7	Line synchronization	see Table I-1								
8	Field synchronization	see Table I-2								

([1]) The values in brackets apply to the combination N/PAL used in Argentina.

([2]) Figures are given for comparison.

([3]) Figures in brackets are valid for colour transmission.

([4]) In order to take full advantage of precision offset when the interfering carrier falls in the sideband of the upper video range (greater than 2 MHz) of the wanted signal a line-frequency stability of at least 2×10^{-7} is necessary.

([5]) The exact value of the tolerance for line frequency when the reference of synchronism is being changed requires further study.

([6]) When the reference of synchronism is being changed, this may be relaxed to 15 625 ± 0.02%.

([7]) These values are not valid when the reference of synchronism is being changed.

([8]) Further study is required to define maximum variation rate of line frequency valid for colour transmission. In the UK and Japan this is 0.1 Hz/s /CCIR, 1982-86b; CCIR, 1986-90/.

([9]) In Japan values $0\ ^{+10}_{-0}$ are used.

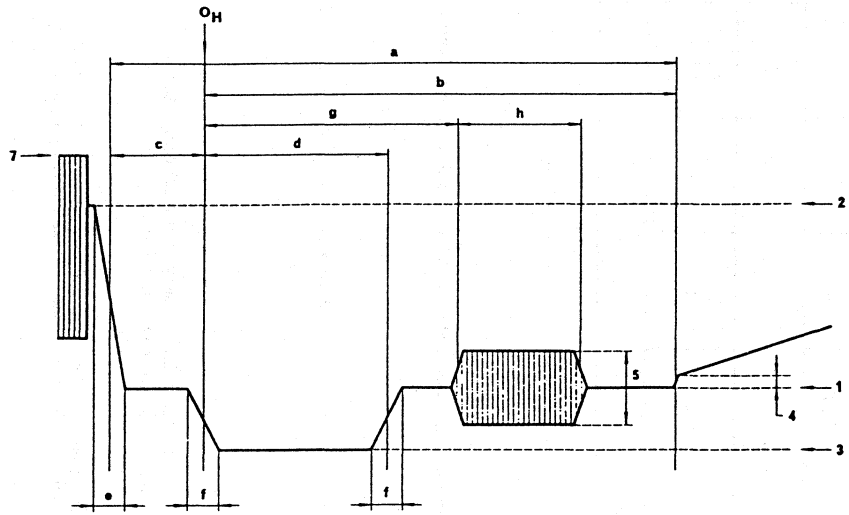
([10]) It is also customary to define certain signal levels in 625-line systems, as follows:
Synchronizing level = 0
Blanking level = 30
Peak white-level = 100
For this scale, the peak level including chrominance signal for system D, K/SECAM equals 110.7. (See [CCIR, 1982-86a].) According to common studio operating practices, peak white-level = 100 corresponds to 1.0 V measured across a matched 75 ohms termination.

([11]) Value applies to PAL signals.

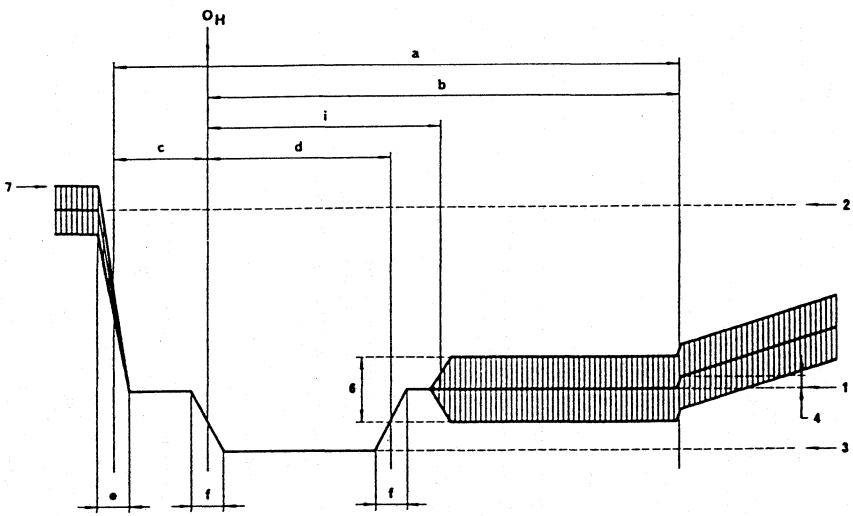
([12]) Values apply to SECAM signals. For programme exchange the value is 115.

([13]) Assumed value for overall gamma approximately 1.2. The gamma of the picture tube is defined as the slope of the curve giving the logarithm of the luminance reproduced as a function of the logarithm of the video signal voltage when the brightness control of the receiver is set so as to make this curve as straight as possible in a luminance range corresponding to a contrast of at least 1/40.

([14]) In Recommendation 472, a gamma value for the picture signal is given as approximately 0.4.



(a) NTSC and PAL systems



(b) SECAM system

FIGURE 1 – *Levels in the composite signal and details of line-synchronizing signals*

1 blanking level
2 peak white-level
3 synchronizing level
4 difference between black and blanking levels
5 peak-to-peak value of burst
6 peak-to-peak value of colour sub-carrier
7 peak level including chrominance signal

TABLE I-1 – *Details of line synchronizing signals (see Fig. 1)*
Durations (measured between half-amplitude points on the appropriate edges) for various systems

Symbol	Characteristics	M (1)	N (2)	B, G, H, I, D, K, K1, L (see also Rec. 472)
H	Nominal line period (μs)	63.492 (63.5555)	64	64 (3)
a	Line-blanking interval (μs)	10.2 to 11.4 (8) (10.9 ± 0.2)	10.24 to 11.52 (12 ± 0.3)	12 ± 0.3 (4)
b	Interval between time datum (O_H) and back edge of line-blanking pulse (μs)	8.9 to 10.3 (9.2 to 10.3)	8.96 to 10.24 (10.5)	10.5 (5)
c	Front porch (μs)	1.27 to 2.54 (1.27 to 2.22)	1.28 to 2.56 (1.5 ± 0.3)	1.5 ± 0.3 (4) (6)
d	Synchronizing pulse (μs)	4.19 to 5.71 (8) (4.7 ± 0.1)	4.22 to 5.76 (4.7 ± 0.2)	4.7 ± 0.2
e	Build-up time (10 to 90%) of the edges of the line-blanking pulse (μs)	≤ 0.64 (≤ 0.48)	≤ 0.64 (0.3 ± 0.1)	0.3 ± 0.1
f	Build-up time (10 to 90%) of the edges of the line-synchronizing pulses (μs)	≤ 0.25	≤ 0.25 (0.2 ± 0.1)	0.2 ± 0.1 (7)

(1) Values in brackets apply to M/NTSC.

(2) The values in brackets apply to the combination N/PAL used in Argentina.

(3) In France, and the countries of the OIRT, the tolerance for the instantaneous line period value is ± 0.032 μs.

(4) In 625-line countries using Teletext System B as specified in the Annex to Recommendation 653 to reduce the possibilities of data loss, the following values are preferred [CCIR, 1982-86c and d]:

a) line blanking interval: $12^{+0.0}_{-0.3}$ μs

c) front porch: $1.5^{+0.3}_{-0.0}$ μs

(5) Average calculated value, for information. For system I the value is 10.4 [CCIR, 1982-86b].

(6) For system I, the values are 1.65 ± 0.1.

(7) For system I, the values are 0.25 ± 0.05.

(8) In Japan, the values in brackets apply to studio facilities.

FIGURE 2 – *Details of field-synchronizing waveforms*

FIGURES 2-1 – *Diagrams applicable to all systems except M*

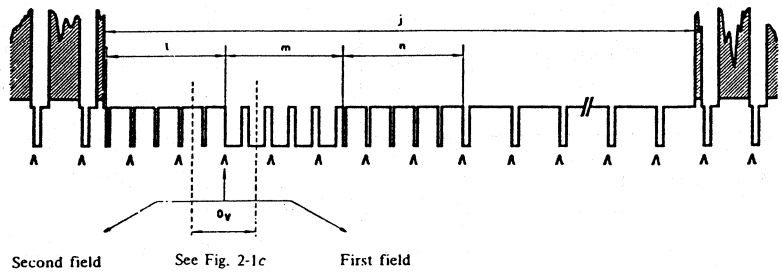


FIGURE 2-1*a* – *Signal at beginning of each first field*

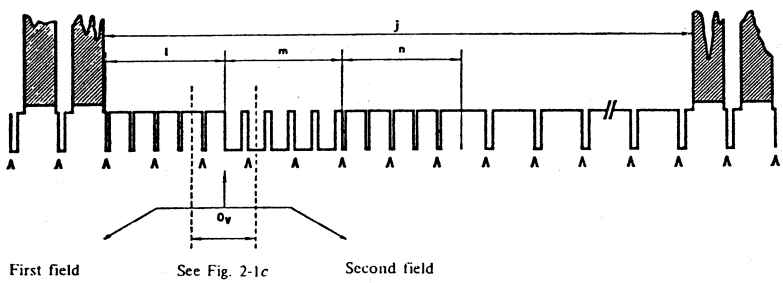
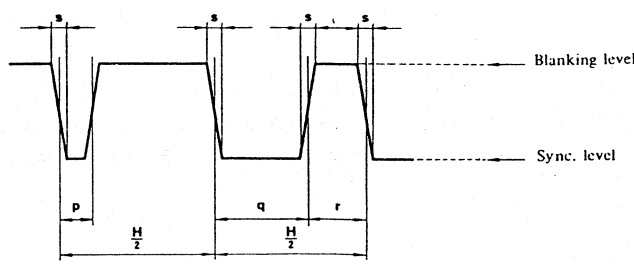


FIGURE 2-1*b* – *Signal at beginning of each second field*

Note 1. – ΛΛΛ indicates an unbroken sequence of edges of line-synchronizing pulses throughout the field-blanking period.

Note 2. – At the beginning of each first field, the edge of the field-synchronizing pulse, O_V, coincides with the edge of a line-synchronizing pulse if *l* is an *odd* number of half-line periods as shown.

Note 3. – At the beginning of each second field, the edge of the field-synchronizing pulse, O_V, falls midway between the edges of two line-synchronizing pulses if *l* is an *odd* number of half-line periods as shown.



(The durations are measured between the half-amplitude points on the appropriate edges)

FIGURE 2-1*c* – *Details of equalizing and synchronizing pulses*

FIGURE 2 – *Details of field-synchronizing waveforms*

FIGURES 2-2 – *Diagrams applicable to system M*

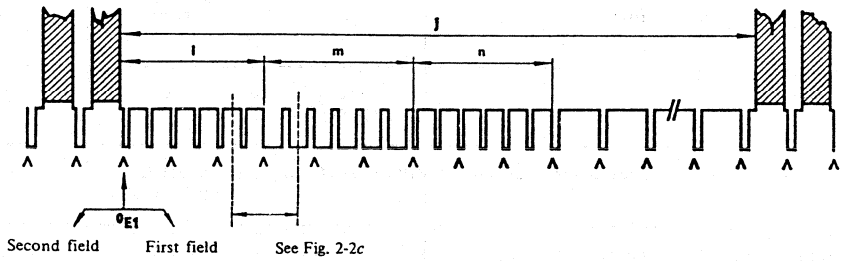


FIGURE 2-2*a* – *Signal at beginning of each first field*

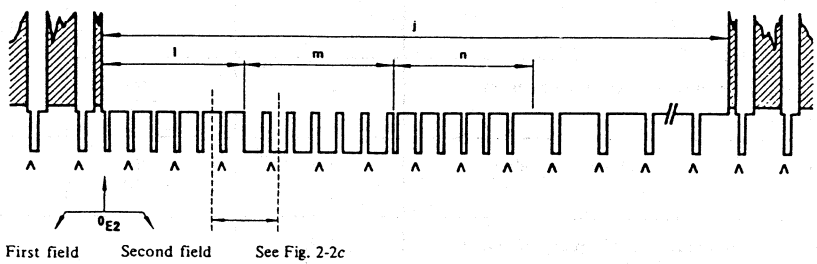


FIGURE 2-2*b* – *Signal at beginning of each second field*

Note 1. – Λ indicates an unbroken sequence of edges of line-synchronizing pulses throughout the field-blanking period.

Note 2. – Field-one line numbers start with the first equalizing pulse in Field 1, designated O_{E1} in Fig. 2-2*a*.

Note 3. – Field-two line numbers start with the second equalizing pulse in Field 2, one-half-line period after O_{E2} in Fig. 2-3*b*.

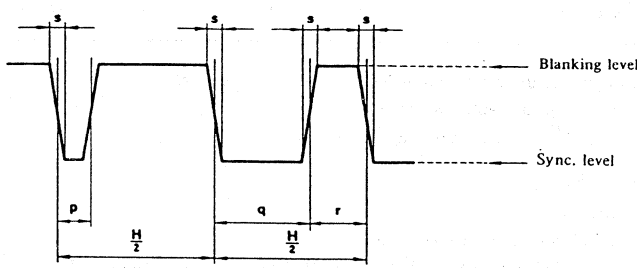


FIGURE 2-2*c* – *Details of equalizing and synchronizing pulses*

TABLE I-2 – *Details of field synchronizing signals (see Fig. 2)*

Duration (measured between half-amplitude points on the appropriate edges) for various systems

Symbol	Characteristics	M	N (1)	B, G, H, I, D, K, K1, L (see also Rec. 472)
v	Field period (ms)	16.667 (2) (16.6833)	20	20
j	Field-blanking interval (for *H* and *a*, see Table I-1)	(19 to 21) *H* + *a* (3)	(19 to 25) *H* + *a* (25 *H* + *a*)	25 *H* + *a*
j' (4)	Build-up time (10 to 90%) of the edges of field-blanking pulses (μs)	⩽ 6.35	⩽ 6.35 (0.3 ± 0.1)	0.3 ± 0.1
k (4)	Interval between front edge of field-blanking interval and front edge of first equalizing pulse (μs)	(1.5 ± 0.1)		3 ± 2 (5) (systems B/SECAM, G/SECAM, D, K, K1 and L only; no ref. in Rec. 472)
l	Duration of first sequence of equalizing pulses	3 *H*	3 *H* (2.5 *H*)	2.5 *H*
m	Duration of sequence of synchronizing pulses	3 *H*	3 *H* (2.5 *H*)	2.5 *H*
n	Duration of second sequence of equalizing pulses	3 *H*	3 *H* (2.5 *H*)	2.5 *H*
p	Duration of equalizing pulse (μs)	(2.3 ± 0.1) (6)	2.30 to 2.56 (2.35 ± 0.1)	2.35 ± 0.1
q	Duration of field-synchronizing pulse (μs)	27.1 (nominal value)	26.52 to 28.16 (27.3)	27.3 (7) (nominal value)
r	Interval between field-synchronizing pulse (μs)	(4.7 ± 0.1)	3.84 to 5.63 (4.7 ± 0.2)	4.7 ± 0.2 (8)
s	Build-up time (10 to 90%) of synchronizing and equalizing pulses (μs)	⩽ 0.25	⩽ 0.25 (0.2 ± 0.1)	0.2 ± 0.1 (9)

(1) The values in brackets apply to the combination N/PAL used in Argentina.

(2) The value in brackets applies to the M/NTSC system.

(3) The value $0.07\ v\ {}^{+\ 0.012\ v}_{-\ 0}$ is used in Japan

where v is the field period.

(4) Not indicated in the diagram.

(5) This value is to be specified more precisely at a later date.

(6) The following specification is also applied in Japan: an equalizing pulse has 0.45 to 0.5 times the area of a line-synchronizing pulse.

(7) For system I: 27.3 ± 0.1.

(8) For system I: 4.7 ± 0.1.

(9) For system I: 0.25 ± 0.05.

TABLE II – *Characteristics of video signal for colour television*

Item	Characteristics	Colour television system					
		M/NTSC	M/PAL	B, D, G, H, N/PAL	I/PAL	B, D, G, H, K, K1, L/SECAM	N/PAL (1)
2.1	Assumed chromaticity coordinates (CIE, 1931) for primary colours of receiver		x y Red 0.67 0.33 Green 0.21 0.71 Blue 0.14 0.08		x y Red 0.64 0.33 Green 0.29 0.60 Blue 0.15 0.06 (2)		
2.2	Chromaticity coordinates for equal primary signals $E'_R = E'_G = E'_B$	Illuminant C $x = 0.310$ $y = 0.316$ (3)		Illuminant D_{65} $x = 0.313$ $y = 0.329$ (2)			
2.3	Assumed gamma value of the receiver for which the primary signals are pre-corrected (4)	2.2	2.8				
2.4	Luminance signal	$E'_Y = 0.299\ E'_R + 0.587\ E'_G + 0.114\ E'_B$ (5) E'_R, E'_G and E'_B are gamma – pre-corrected primary signals (6)					
2.5	Chrominance signals (Colour difference)	$E'_I = -0.27(E'_B - E'_Y) + 0.74(E'_R - E'_Y)$ $E'_Q = 0.41(E'_B - E'_Y) + 0.48(E'_R - E'_Y)$	$E'_U = 0.493(E'_B - E'_Y)$ $E'_V = 0.877(E'_R - E'_Y)$			$D'_R = -1.902(E'_R - E'_Y)$ $D'_B = 1.505(E'_B - E'_Y)$	
2.6	Attenuation of colour difference signals	dB MHz E'_I < 3 at 1.3, ≥ 20 at 3.6 E'_Q < 2 at 0.4, < 6 at 0.5, ≥ 6 at 0.6	dB MHz E'_U < 2 at 1.3 E'_V > 20 at 3.6	dB MHz E'_U < 3 at 1.3 E'_V > 20 at 4		dB MHz D'_R ≤ 3 at 1.3 D'_B ≥ 30 at 3.5 Low frequency pre-correction not taken into account (7)	dB MHz E'_U < 3 at 1.3 E'_V > 20 at 3.6

See notes at the end of Table II.

TABLE II *(continued)*

Item	Characteristics	Colour television system					
		M/NTSC	M/PAL	B, D, G, H, N/PAL	I/PAL	B, D, G, H, K, K1, L/SECAM	N/PAL (1)
2.7	Low frequency pre-correction of colour difference signals					For sinusoidal signals: $D'_R{}^* = A_{BF}(f)D'_R$ $D'_B{}^* = A_{BF}(f)D'_B$ $A_{BF}(f) = \frac{1+j(f/f_1)}{1+j(f/3f_1)}$ f = signal frequency (kHz) f_1 = 85 kHz (See Fig. 6 for the amplitude response) (8)	
2.8	Time-coincidence error between luminance and chrominance signals (μs)	<0.05 Excluding pre-correction for receiver response					
2.9	Equation of composite colour signal	$E_M = E'_Y + + E'_Q \sin(2nf_{sc}' + 33°) + + E'_I \cos(2nf_{sc}' + 33°)$ where: E'_Y, see item 2.4 E'_Q and E'_I, see item 2.5 f_{sc}, see item 2.11 (See also Fig. 4*a*)	$E_M = E'_Y + E'_U \sin 2nf_{sc}' \pm E'_V \cos 2nf_{sc}'$ where: E'_Y, see item 2.4 E'_U and E'_V, see item 2.5 f_{sc}, see item 2.11 The sign of the E'_Y component is the same as that of the sub-carrier burst (changing for each line) (see item 2.16 and Fig. 4*b*)			$E_M = E'_Y + G \cos 2\pi (f_{OR}' + \Delta f_{OR} \int_0^t D'_R{}^* \, dt)$ or $E_M = E'_Y + G \cos 2\pi (f_{OB}' + \Delta f_{OB} \int_0^t D'_B{}^* \, dt)$ alternately from line to line where: E'_Y, see item 2.4 f_{OR} and f_{OB}, see item 2.11 Δf_{OR} and Δf_{OB}, see item 2.12 $D'_R{}^*$ and $D'_B{}^*$, see item 2.7 G, see item 2.13	
2.10	Type of chrominance sub-carrier modulation	Suppressed-carrier amplitude-modulation of two sub-carriers in quadrature				Frequency modulation	

See notes at the end of Table II.

TABLE II *(continued)*

Item	Characteristics	Colour television system							
		M/NTSC	M/PAL	B, D, G, H, N/PAL	I/PAL	B, D, G, H, K, K1, L/SECAM			N/PAL (1)
2.11	Chrominance sub-carrier frequency *(a)* nominal value and tolerance (Hz)	3 579 545 ± 10	3 575 611.49 ± 10	4 433 618.75 ± 5	4 433 618.75 ± 1 (9) (10)	f_{OR} = 4 406 250 ± 2000 f_{OB} = 4 250 000 ± 2000 (11)			3 582 056.25 ± 5
	(b) relationship between chrominance sub-carrier frequency f_{sc} and line frequency f_H	$f_{sc} = \frac{455}{2} f_H$	$f_{sc} = \frac{909}{4} f_H$	$f_{sc} = \left(\frac{1135}{4} + \frac{1}{625}\right) f_H$		Unmodulated sub-carrier at beginning of line 282 f_H for f_{OR} 272 f_H for f_{OB} (12)			$f_{sc} = \left(\frac{917}{4} + \frac{1}{625}\right) f_H$
2.12	Bandwidth of chrominance sidebands (quadrature modulation of sub-carrier) (kHz) or Frequency deviation of chrominance sub-carrier (frequency modulation of sub-carrier) (kHz)	$f_{sc} \begin{matrix} +620 \\ -1300 \end{matrix}$	$f_{sc} \begin{matrix} +600 \\ -1300 \end{matrix}$	$f_{sc} \begin{matrix} +570 \\ -1300 \end{matrix}$ (13)	$f_{sc} \begin{matrix} +1066 \\ -1300 \end{matrix}$		Nominal deviation $D'^* = 1$ (14)	Maximum deviation	$f_{sc} \begin{matrix} +620 \\ -1300 \end{matrix}$
						Δf_{OR} (15)	280 ± 9 (± 14)	+350 ± 18 (± 35) −506 ± 25 (± 50)	
						Δf_{OB} (15)	230 ± 7 (± 11.5)	+506 ± 25 (± 50) −350 ± 18 (± 35)	

See notes at the end of Table II.

TABLE II *(continued)*

Item	Characteristics	Colour television system					
		M/NTSC	M/PAL	B, D, G, H, N/PAL	I/PAL	B, D, G, H, K, K1, L/SECAM	N/PAL (1)
2.13	Amplitude of chrominance sub-carrier	$G = \sqrt{E'^2_I + E'^2_Q}$	$G = \sqrt{E'^2_U + E'^2_V}$ (16) (17)		(16)	$G = M_0 \frac{1 + j\,16F}{1 + j\,1.26F}$ where the peak-to-peak amplitude, $2M_0$ is 23 ± 2.5 % of the luminance amplitude (between blanking level and peak-white) and $F = \frac{f}{f_0} - \frac{f_0}{f}$ where f_0 = 4286 kHz and f is the instantaneous sub-carrier frequency. The deviation of frequency, f_0, from its nominal value due to misalignment of the circuits concerned should not exceed ± 20 kHz. (See Fig. 7 for the amplitude response)	
2.14	Synchronization of chrominance sub-carrier	Sub-carrier burst on blanking back porch	Sub-carrier burst on blanking back porch				
	(g) Start of sub-carrier burst (see Fig. 1*a*) (µs)	4.71 to 5.71 (5.3 nominal) at least 0.38 µs after the trailing edge of line synchronization signal	5.8 ± 0.1 after epoch O_{II}	5.6 ± 0.1 after epoch O_{II} (18)			
	(h) Duration of sub-carrier burst (see Fig. 1*a*) (µs)	2.23 to 3.11 (9 ± 1 cycles)	2.52 ± 0.28 (9 ± 1 cycles)	2.25 ± 0.23 (10 ± 1 cycles)			2.51 ± 0.28 (9 ± 1 cycles)

See notes at the end of Table II.

TABLE II *(continued)*

<table>
<tr><th rowspan="2">Item</th><th rowspan="2">Characteristics</th><th colspan="6">Colour television system</th></tr>
<tr><th>M/NTSC</th><th>M/PAL</th><th>B, D, G, H, N/PAL</th><th>I/PAL</th><th>B, D, G, H, K, K1, L/SECAM</th><th>N/PAL (1)</th></tr>
<tr><td>2.15</td><td>Peak-to-peak value of chrominance sub-carrier burst
(see Fig. 1a) (19)</td><td>4/10 of difference between blanking level and peak white-level ± 10%</td><td colspan="3">3/7 of difference between blanking level and peak white-level ± 10%
For systems D and I the tolerance is ± 3%
(16) (17) (16)</td><td></td><td></td></tr>
<tr><td>2.16</td><td>Phase of chrominance sub-carrier burst
(see Fig. 1a)</td><td>180° relative to ($E'_B - E'_Y$) axis
(see Fig. 4a)
In the NTSC sequence of four colour fields, field 1 is identified in accordance with Note (20)
(see also Fig. 5c)</td><td colspan="3">135° relative to E'_U axis with the following sign (see Fig. 4b)
<table><tr><td rowspan="3">Line</td><td colspan="8">Field Number (21)</td></tr><tr><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td><td>7</td><td>8</td></tr><tr><td colspan="8">Burst blanking sequence (see Figs. 5a and 5b)</td></tr><tr><td></td><td>I</td><td>II</td><td>III</td><td>IV</td><td>I</td><td>II</td><td>III</td><td>IV</td></tr><tr><td>even</td><td>−</td><td>−</td><td>+</td><td>+</td><td>−</td><td>−</td><td>+</td><td>+</td></tr><tr><td>odd</td><td>+</td><td>+</td><td>−</td><td>−</td><td>+</td><td>+</td><td>−</td><td>−</td></tr></table></td><td></td><td></td></tr>
<tr><td>2.17</td><td>Blanking of chrominance sub-carrier</td><td>Following each equalizing pulse and also during the broad synchronizing pulses in the field-blanking interval</td><td>11 lines of field-blanking interval:
260 to 270
522 to 7
259 to 269
223 to 8
(See Fig. 5b)</td><td colspan="2">9 lines of the field-blanking interval:
lines 311 to 319 inclusive
623 to 6 inclusive
310 to 318 inclusive
622 to 5 inclusive
(See Fig. 5a)</td><td>(a) from leading edge of line-blanking signal up to $i = 5.6 \pm 0.2$ (μs) after epoch O_H, i.e. during $c + i$ (see Fig. 1b) (22)
(b) During field-blanking interval, excluding frame identification signals, or, in countries where this is possible, during the whole of the field-blanking interval (see item 2.18)</td><td></td></tr>
</table>

See notes at the end of Table II.

TABLE II *(continued)*

Item	Characteristics	Colour television system					
		M/NTSC	M/PAL	B, D, G, H, N/PAL	I/PAL	B, D, G, H, K, K1, L/SECAM	N/PAL (1)
2.18	Synchronization of chrominance sub-carrier switching during line blanking	See item 2.16. For signals used in programme integration, the tolerance on the coincidence between the reference sub-carrier and the horizontal synchronizing pulses in nominally 0 ± 40° of the reference sub-carrier	By E'_V chrominance component of sub-carrier burst (See item 2.16)			In the SECAM system, one of two colour synchronization methods can be chosen: - line identification: by chrominance sub-carrier reference signals on the line-blanking back porch ([23]) - by identification signals occupying 9 lines of field-blanking period: *(a)* line 7 to 15 in 1st and 3rd field *(b)* line 320 to 328 in 2nd and 4th field (See Fig. 9) ([24]) *Shape of video signals corresponding to identification signals:* For lines D'_R – Trapezoid with linear variation from beginning of line on 15 ±5 µs from 0 up to level +1.25 and then constant at the level +1.25 ± 0.06 (±0.13) (See Fig. 8)	

See notes at the end of Table II.

TABLE II *(continued)*

Item	Characteristics	Colour television system					
		M/NTSC	M/PAL	B, D, G, H, N/PAL	I/PAL	B, D, G, H, K, K1, L/SECAM	N/PAL (1)
						For lines D'_B – Trapezoid with linear variation from the beginning of the line on 18 ± 6 µs (20 ± 10 µs) from 0 down to level −1.52 and then constant at the level −1.52 ± 0.07 (± 0.15) (see Fig. 8) (15) *Peak-to-peak amplitude of identification signals:* For lines D'_B: 500 ± 50 mV For lines D'_R: 540^{+40}_{-50} mV if amplitude of luminance signal (between blanking level and peak white) equals 700 mV *Maximum deviation during transmission of identification signals (kHz):* For lines D'_R: +350 ± 18 (± 35) For lines D'_B: −350 ± 18 (± 35) (15)	

See notes next page.

(1) These values apply to the combination N/PAL used in Argentina. Only those values are given in this column which are different from the values given in the column B, G, H, N/PAL.

(2) For SECAM systems and for existing sets, it is provisionally allowed to use the following chromaticity coordinates for the primary colours and white:

	x	y	
Red	0.67	0.33	
Green	0.21	0.71	
Blue	0.14	0.08	
White	0.310	0.316	(C-white)

(3) In Japan, the chromaticity of studio monitors is adjusted to a D-white at 9300 K.

(4) The primary signals are pre-corrected so that the optimum quality is obtained with a display having the indicated value of gamma.

(5) In certain countries using the SECAM systems and in Japan it is also permitted to obtain the luminance signal as a direct output from an independent photo-electric analyser instead of from the primary signals.

(6) For the SECAM system, it is allowable to apply a correction to reduce interference distortions between the luminance and chrominance signals by an attenuation of the luminance signal components as a function of the amplitude of the luminance components in the chrominance band.

(7) This value will be defined more precisely later.

(8) The maximum deviations from the nominal shape of the curve (see Fig. 6) should not exceed ± 0.5 dB in the frequency range from 0.1 to 0.5 MHz and ± 1.0 dB in the frequency range from 0.5 to 1.3 MHz.

(9) When the signal originates from a portable or overseas source the tolerance on the frequency may be relaxed to ± 5 Hz. Maximum rate of variation of f_{SC}: 0.1 Hz/s.

(10) This tolerance may not be maintained during such operational procedures as "genlock".

(11) A reduction of the tolerance is desirable.

(12) The initial phase of the sub-carrier undergoes in each line a variation defined by the following rule:

From frame to frame: by 0°: 180°: 0°: 180° and so on, and also from line to line in either one of the following two patterns:

0°: 0°: 180°: 0°: 0°: 180°: and so on,
or 0°: 0°: 0°: 180°: 180°: 180°: and so on.

(13) f_M ± 1300 kHz is adopted in the People's Republic of China.

(14) The unity value represents the amplitude of the luminance signal between the blanking level and the peak white-level.

(15) Provisionally, the tolerances may be extended up to the values given brackets.

(16) During transmission of a monochrome programme of significant duration, in order to ensure satisfactory operation of colour-killers in receivers, all signals having the same nominal frequency as the colour sub-carrier that appears in the line-blanking interval, should be attenuated by at least 35 dB below the peak-to-peak value of the burst given in item 2.15, column 3 of Table II, and shown as item 5 in Fig. 1.

(17) The value given in Note (16) is accepted on a tentative basis.

(18) Transmitter pre-correction for receiver group delay is not included.

(19) For the use of automatic gain control circuits, it is important that the burst amplitude should maintain the correct ratio with the chrominance signal amplitude.

(20) Field 1 of the sequence of four fields in the NTSC video signal is defined by a whole line between the first equalizing pulse and the preceding horizontal synchronizing pulse and a negative-going zero-crossing of the reference sub-carrier nominally at the 50% point of the first equalizing pulse. The zero-crossing of the reference sub-carrier shall be nominally coincident with the 50% point of the leading edges of all horizontal synchronizing pulses for programme integration at the studio.

(21) Field 1 of the sequence of eight colour fields is defined as that field, where the phase φ E'_U of the extrapolated E'_U component (see item 2.5 of Table II) of the video burst at the hall amplitude point of the leading edge of the line synchronizing pulse of line 1 is in the range $-90° \leqslant \varphi\ E'_U < 90°$.

(22) The value of the tolerance will be defined more precisely later.

(23) The line identification method is preferable, because it will enable agreements to be reached subsequently on the suppression of frame identification signals in international programme exchanges. In the absence of such agreements, signals meeting the SECAM standard are regarded as comprising such identification signals.

In France, a decree of 14 March 1978 specified that colour TV receivers placed on sale on or after 1 December 1979 must use the line identification method of decoding [CCIR, 1982-86c].

(24) The order in which the identification signals D_R* and D_B* appear on the four fields of a complete cycle given in Fig. 9 is in conformity with Recommendation 469.

TABLE III – *Characteristics of the radiated signals (monochrome and colour)*

Item	Characteristics		M	N [1]	B, G	H	I	D, K	K1	L
1	Frequency spacing (see Fig. 10)	Nominal radio-frequency channel bandwidth (MHz)	6	6	B: 7 G: 8	8	8	8	8	8
2		Sound carrier relative to vision carrier (MHz)	+4.5 [2]	+4.5	+5.5 ±0.001 [3], [4], [5], (24)	+5.5	+5.9996 ±0.0005 (25)	+6.5 ±0.001	+6.5	+6.5
3		Nearest edge of channel relative to vision carrier (MHz)	−1.25	−1.25	−1.25	−1.25	−1.25	−1.25	−1.25	−1.25
4		Nominal width of main sideband (MHz)	4.2	4.2	5	5	5.5	6	6	6
5		Nominal width of vestigial sideband (MHz)	0.75	0.75	0.75	1.25	1.25	0.75	1.25	1.25
6	Minimum attenuation of vestigial sideband (dB at MHz) [6]		20 (−1.25) 42 (−3.58)	20 (−1.25) 42 (−3.5)	20 (−1.25) 20 (−3.0) 30 (−4.43) [7]	20 (−1.75) 20 (−3.0)	20 (−3.0) 30 (−4.43)	20 (−1.25) 30 (−4.33 ±0.1) [8] [9]	20 (−2.7) 30 (−4.3) ref.: 0 (+0.8)	15 (−2.7) 30 (−4.3) ref.: 0 (+0.8)
7	Type and polarity of vision modulations		C3F neg.	C3F neg.	C3F neg.	C3F neg.	C3F neg.	C3F neg.	C3F neg.	C3F pos.
8	Levels in the radiated signal (% of peak carrier)	Synchronizing level	100	100	100	100	100	100	100	< 6
		Blanking level	72.5 to 77.5	72.5 to 77.5 (75 ± 2.5)	75 ± 2.5 [10]	72.5 to 77.5	76 ± 2	75 ± 2.5	75 ± 2.5	30 ± 2
		Difference between black level and blanking level	2.88 to 6.75 (26)	2.88 to 6.75	0 to 2 (nominal)	0 to 7	0 (nominal)	0 to 4.5 [11]	0 to 4.5	0 to 4.5
		Peak white-level	10 to 15	10 to 15 (10 to 12.5)	10 to 12.5 [10] [12]	10 to 12.5	20 ± 2	10 to 12.5 [13] [14]	10 to 12.5	100 (≈ 110) [15]

See notes at the end of Table III.

TABLE III *(continued)*

Item	Characteristics	M	N ([1])	B, G	H	I	D, K	K1	L
9	Type of sound modulation	F3E	F3E	F3E	F3E	F3E	F3E	F3E	A3E
10	Frequency deviation (kHz)	± 25	± 25	± 50	± 50	± 50	± 50	± 50	
11	Pre-emphasis for modulation (μs)	75	75	50	50	50	50	50	
12	Ratio of effective radiated powers of vision and (primary) sound (16)	10/1 to 5/1 ([17])	10/1 to 5/1	20/1 to 10/1 ([3]) ([18]) ([19])(24)	5/1 to 10/1	5/1 10/1 ([20])(25)	10/1 to 5/1 ([21])	10/1	10/1 10/1 to 40/1(27)
13	Pre-correction for receiver group-delay characteristics at medium video frequencies (ns) (see also Fig. 3)	0	(1 MHz 0 ± 100 1 MHz 0 ± 100 1 MHz 0 ± 60)	([22])			([23a])		
14	Pre-correction for receiver group-delay characteristics at colour sub-carrier frequency (ns) (see also Fig. 3)	−170 (nominal)	(+60 −170 −40)	−170 (nominal) ([22])			([23b])		

([1]) The values in brackets apply to the combination N/PAL used in Argentina.

([2]) In Japan, the values +4.5 ± 0.001 are used.

([3]) In the Federal Republic of Germany, Italy, the Netherlands and Switzerland a system of two sound carriers is used, the frequency of the second carrier being 242.1875 kHz above the frequency of the first sound carrier. The ratio between vision/sound e.r.p. for this second carrier is 100/1. For further information on this **system** see Report 795. For stereophonic sound transmissions a similar system is used in Australia with vision/sound power ratios being 20/1 and 100/1 for the first and second sound carriers respectively.

([4]) New Zealand uses a sound carrier displaced 5.4996 ±0.0005 MHz from the vision carrier.

([5]) The sound carrier for single carrier sound transmissions in Australia may be displaced 5.5 ± 0.005 MHz from the vision carrier.

([6]) In some cases, low-power transmitters are operated without vestigial-sideband filter.

([7]) For B/SECAM and G/SECAM: 30 dB at −4.33 MHz, within the limits of ± 0.1 MHz.

([8]) In some countries, members of the OIRT, additional specifications are in use:
(a) not less than 40 dB at −4.286 MHz ± 0.5 MHz,
(b) 0 dB from −0.75 MHz to +6.0 MHz,
(c) not less than 20 dB at ± 6.375 MHz and higher;
Reference: 0 dB at +1.5 MHz.

([9]) In the People's Republic of China, the attenuation value at the point (−4.33 ± 0.1) has not yet been determined.

(10) *Australia uses the nominal modulation levels specified for system I.*

(11) *In the People's Republic of China, the values 0 to 5 have been adopted.*

(12) Italy is considering the possibility of controlling the peak white-level after weighting the video frequency signal by a low-pass filter, so as to take account only of those spectrum components of the signal that are likely to produce inter-carrier noise in certain receivers when the nominal level is exceeded. Studies should be continued with a view to optimizing the response of the weighting filter to be used.

(13) The USSR has adopted the value 15 ± 2%.

(14) A new parameter "white level with sub-carrier" should be specified at a later date. For that parameter, the USSR has adopted the value of 7 ± 2%.

(15) The peak white-level refers to a transmission without colour sub-carrier. The figure in brackets corresponds to the peak value of the transmitted signal, taking into account the colour sub-carrier of the respective colour television system.

(16) The values to be considered are:

- the r.m.s. value of the carrier at the peak of the modulation envelope for the vision signal. For system L, only the luminance signal is to be considered. (See Note (15) above);
- the r.m.s. value of the unmodulated carrier for amplitude-modulated and frequency-modulated sound transmissions.

(17) In Japan, a ratio of 1/0.15 to 1/0.35 is used. In the United States, the sound carrier e.r.p. is not to exceed 22% of the peak authorized vision e.r.p.

(18) It may be that the Austrian Administration will continue to use a 5/1 power ratio in certain cases, when necessary.

(19) Recent studies in India [CCIR, 1982-86f] confirm the suitability of a 20/1 ratio of effective radiated powers of vision and sound. This ratio still enables the introduction of a second sound carrier.

(20) The ratio 10/1 is used in the Republic of South Africa and in the United Kingdom.

(21) In the People's Republic of China, the value 10/1 has been adopted.

(22) In the Federal Republic of Germany and the Netherlands the correction for receiver group-delay characteristics is made according to curve B in Fig. 3*a)*. Tolerances are shown in the table under Fig. 3*a)*. From [CCIR, 1966-69] it is learned that Spain uses curve A. The OIRT countries using the B/SECAM and G/SECAM systems use a nominal pre-correction of 90 ns at medium video frequencies. In Sweden, the pre-correction is 0 ± 40 ns up to 3.6 MHz. For 4.43 MHz, the correction is −170 ± 20 ns and for 5 MHz it is −350 ± 80 ns. In New Zealand the pre-correction increases linearly from 0 ± 20 ns at 0 MHz to 60 ± 50 ns at 2.25 MHz, follows curve A of Fig. 3a from 2.25 MHz to 4.43 MHz and then decreases linearly to −300 ± 75 ns at 5 MHz. In Australia, the nominal pre-correction follows curve A up to 2.5 MHz, then decreases to 0 ns at 3.5 MHz, −170 ns at 4.43 MHz and −280 ns at 5 MHz. Based on studies on receivers in India, the receiver group delay pre-equalization proposed to be adopted in India at 1 MHz, 2 MHz, 3 MHz, 4.43 MHz and 4.8 MHz are +125 ns, +150 ns, +142 ns, −75 ns and −200 ns respectively. In Denmark, the precorrection at 0, 0.25, 1.0, 2.0, 3.0, 3.8, 4.43 and 4.8 MHz are 0, +5, +53, +75, +75, 0, -170 and -400 ns.

(23a) Not yet determined. The Czechoslovak Socialist Republic proposes +90 ns (nominal value).

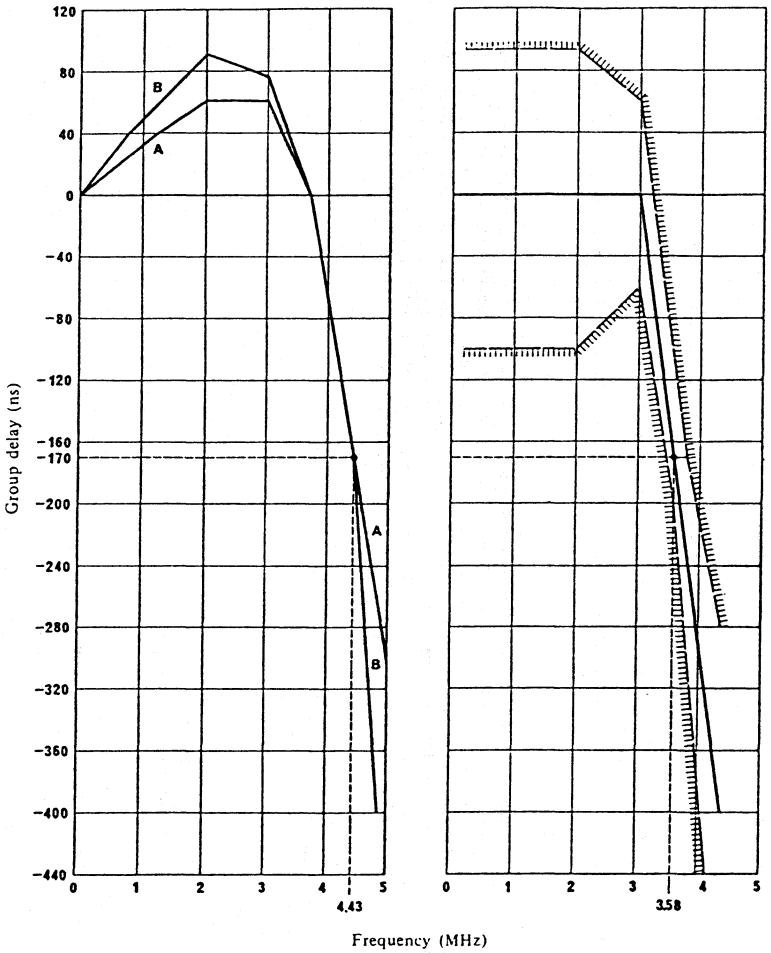
(23b) Not yet determined. The Czechoslovak Socialist Republic proposes +25 ns (nominal value).

(24) In Denmark, Finland, New Zealand, Sweden and Spain a system of two sound carriers is used. In Iceland and Norway the same system is being introduced. The second carrier is 5.85 MHz above the vision carrier and is DQPSK modulated with 728 kbit/s sound and data multiplex. The ratios between vision/sound power are 20/1 and 100/1 for the first and second carrier respectively. For further information, see Recommendation 707, Report 795 and Report 1214.

(25) In the United Kingdom, a system of two sound carriers is used. The second sound carrier is 6.552MHz above the vision carrierand is DQPSK modulated with a 728kbit/s sound and data multiplex able to carry two sound channels. The ratio between vision and sound e.r.p. for the second carrier is 100/1. Further information on this system is given in Report 795.

(26) In Japan, the values of 0 to 6.75 have been adopted.

(27) In France, experimental.



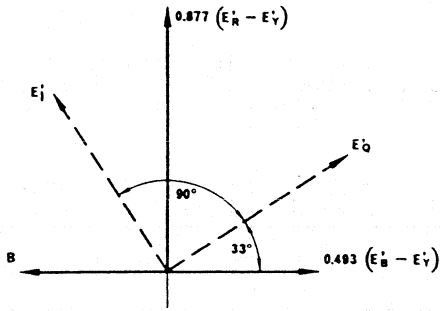
(a) B/PAL and G/PAL systems (See Table III ([22]))

(b) M/PAL and M/NTSC systems

FIGURE 3 *Curve of pre-correction for receiver group-delay characteristics*

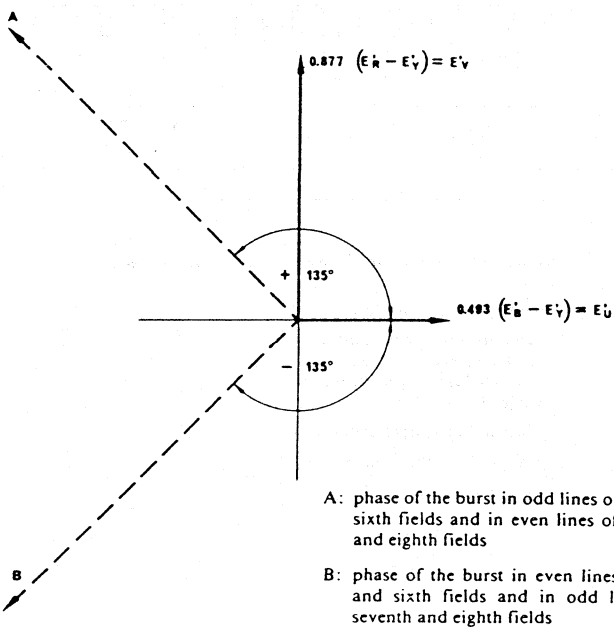
Nominal values and tolerances (ns)

Frequency (MHz)	Curve A	Curve B
0·25		+ 5 ± 0
1·00	+ 30 ± 50	+ 53 ± 40
2·00	+ 60 ± 50	+ 90 ± 40
3·00	+ 60 ± 50	+ 75 ± 40
3·75	0 ± 50	0 ± 40
4·43	−170 ± 35	−170 ± 40
4·80	−260 ± 75	−400 ± 90



B: phase of the burst

a) NTSC system



A: phase of the burst in odd lines of the first, second, fifth and sixth fields and in even lines of the third, fourth, seventh and eighth fields

B: phase of the burst in even lines of the first, second, fifth and sixth fields and in odd lines of the third, fourth, seventh and eighth fields

b) PAL system

FIGURE 4 – *Chrominance axes and phase of the burst*

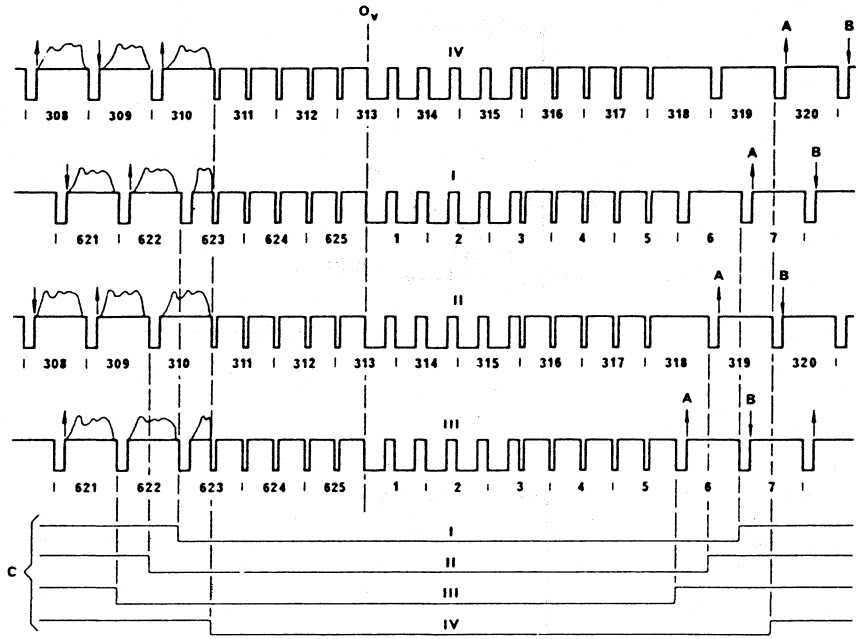


FIGURE 5a – *Burst-blanking sequence in the B, G, H and I/PAL systems*

O_V: field-synchronizing datum

I, II, III, IV: first and fifth, second and sixth, third and seventh, fourth and eighth fields (see item 2.16 of Table II)

A: phase of burst: nominal value + 135°

B: phase of burst: nominal value – 135°

C: burst-blanking intervals

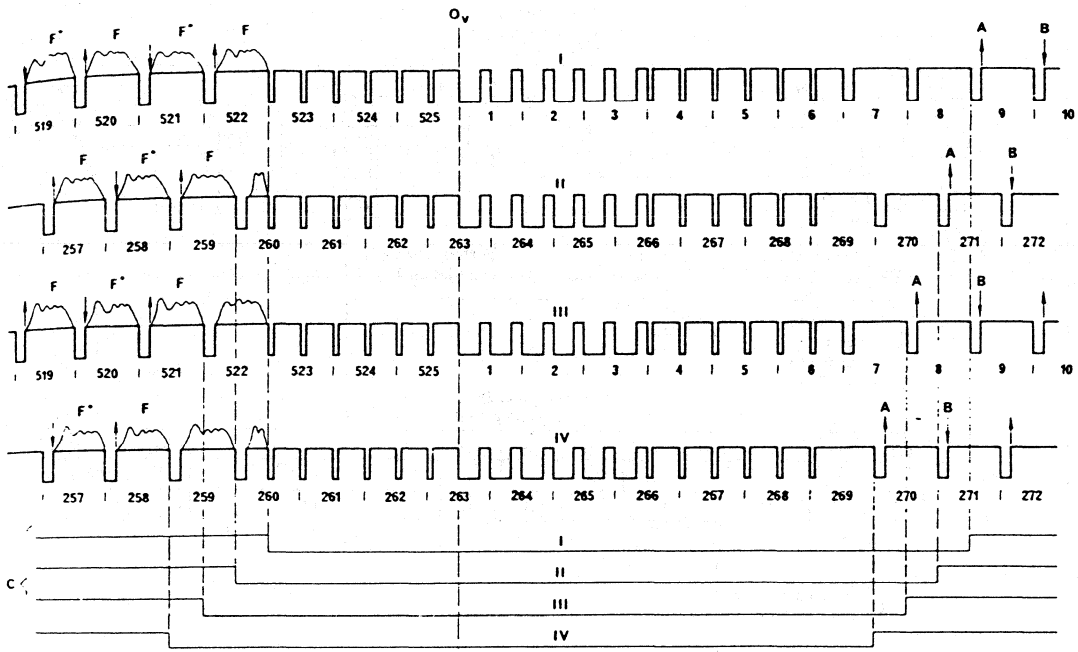


FIGURE 5b – *Burst-blanking sequence in M/PAL system*

O_V: field-synchronizing datum

I, II, III, IV: first and fifth, second and sixth, third and seventh, fourth and eighth fields (see item 2.16 of Table II)

A: phase of burst; nominal value + 135°

B: phase of burst; nominal value – 135°

C: burst-blanking intervals

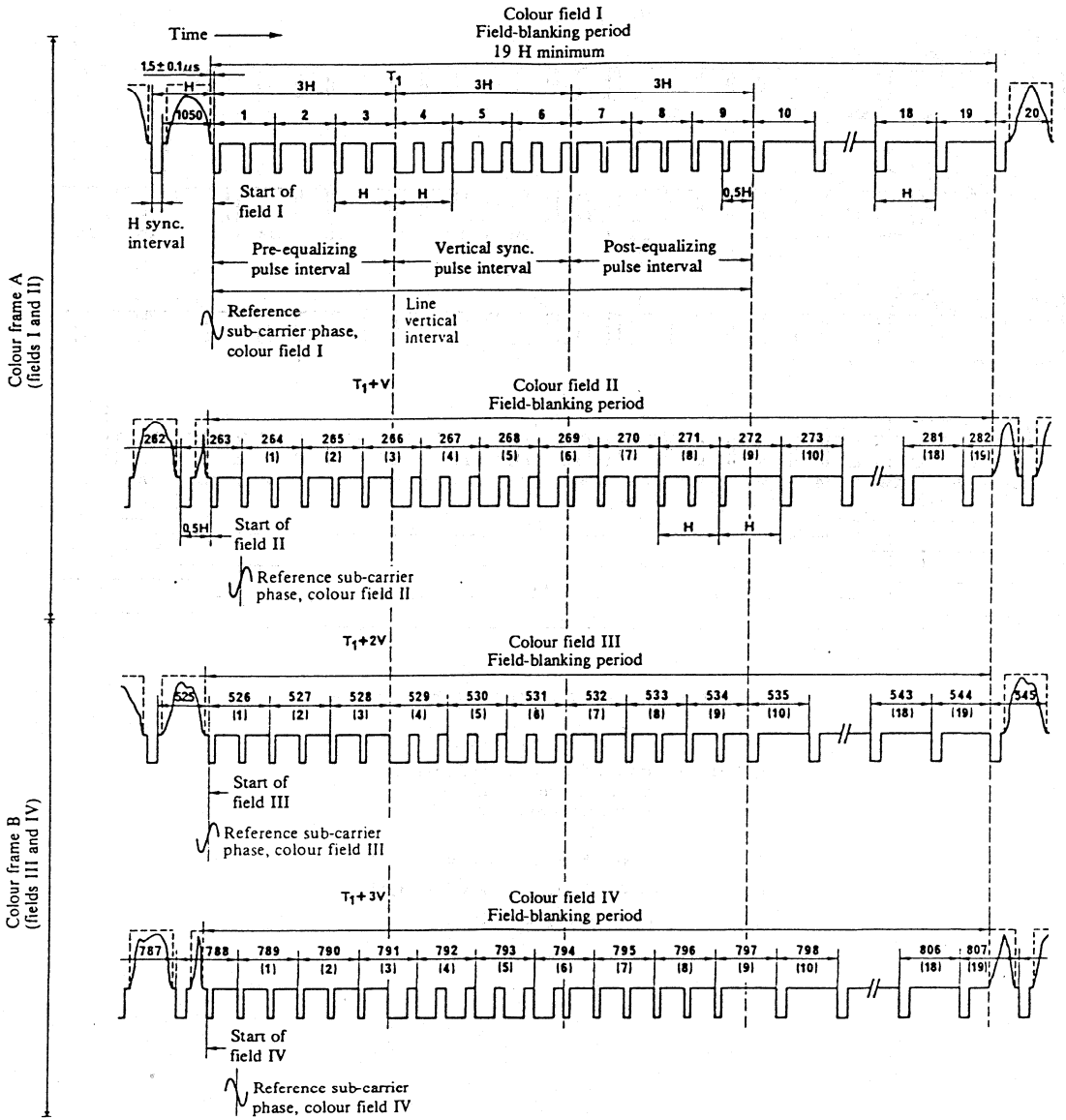


FIGURE 5c – *Burst-blanking sequence in M/NTSC System*

Note. – The numbering of specific lines is in accordance with new engineering practice. Line numbers in parentheses ( ) represent an alternative method of line numbering used in some systems in some countries.

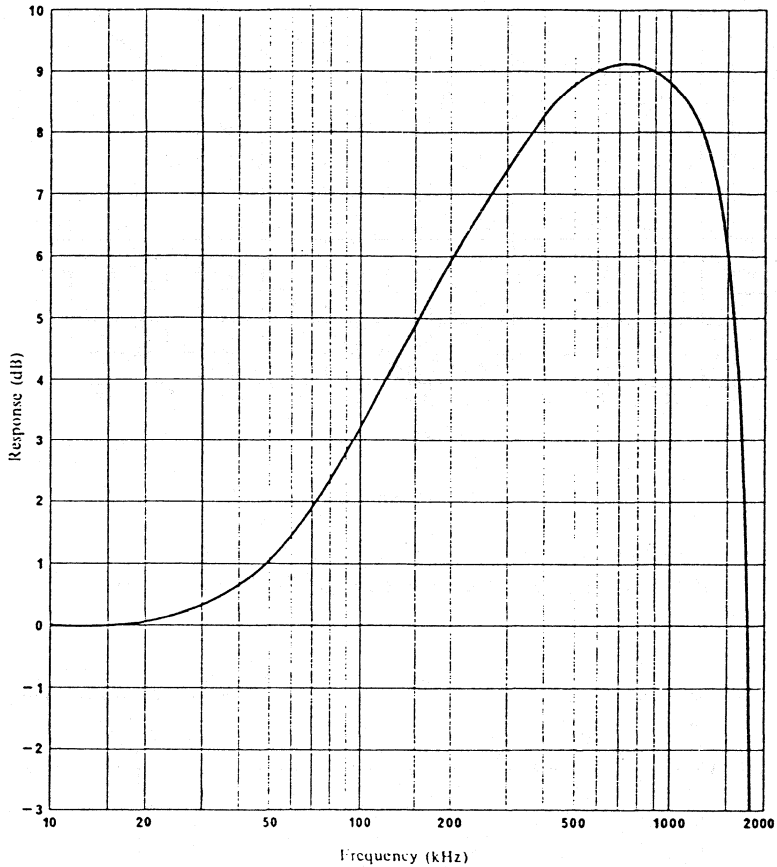


FIGURE 6 – *Nominal response of transfer function resulting from the video-frequency precorrection circuit $A_{BF}(f)$ and the low-pass filter (See Table II, item 2.7)*

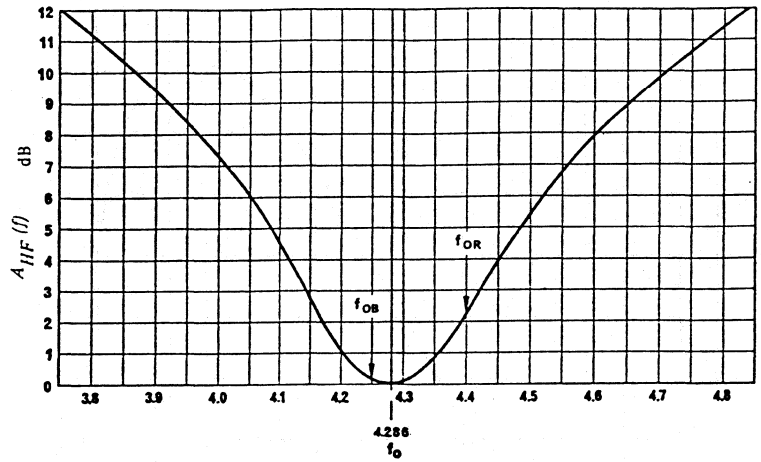


FIGURE 7 – *Attenuation curve of frequency correction $A_{HF}(f)$*

Deviations from the nominal curve outside point f_0 must not exceed ± 0.5 dB

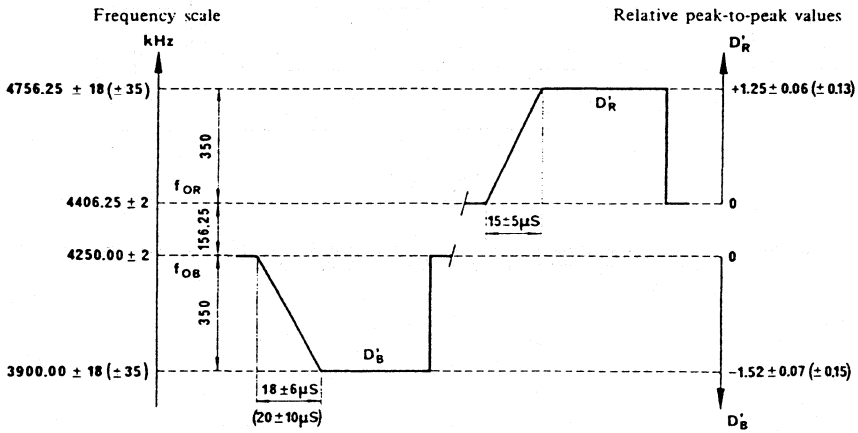


FIGURE 8 – *Shape of video signals corresponding to the chrominance synchronization signals*

The value 1 represents the amplitude of the luminance signal between the blanking level and the white level. Provisionally, the tolerances may be extended up to the values given in brackets.

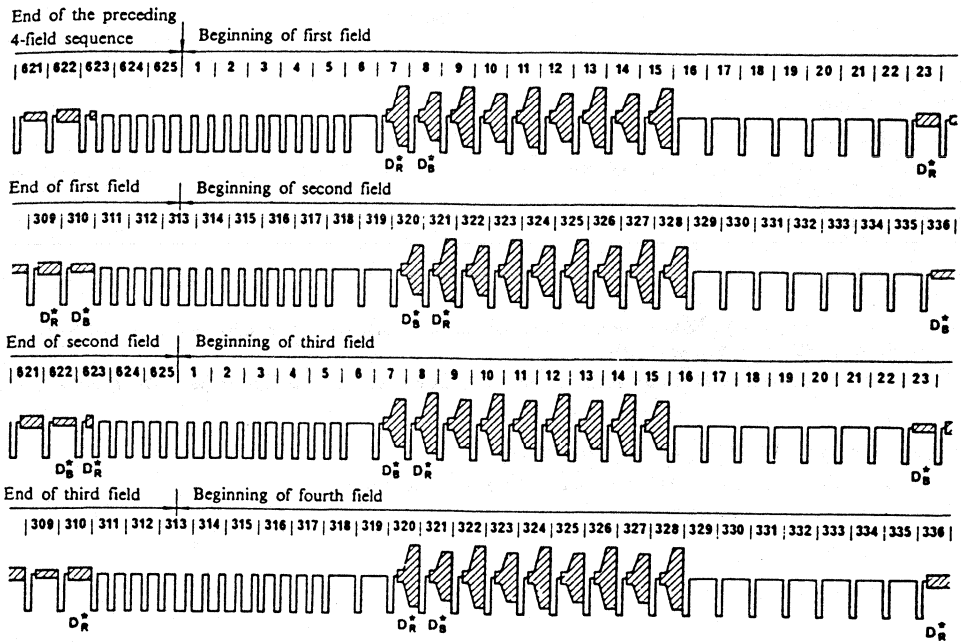


FIGURE 9 – *Sequence of D_R^* or D_B^* signal over four consecutive fields*

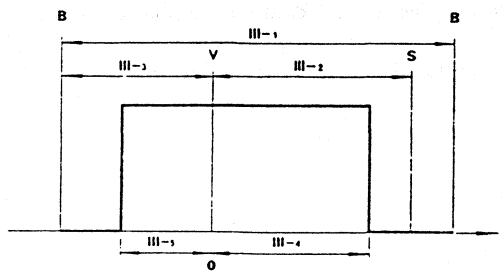


FIGURE 10 – *Significance of items 1 to 5 in Table III*

B : Channel limit
V : Vision carrier
S : Sound carrier

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[1966-69]: XI/170 (Spain).

[1978-82]: 11/251 (EBU).

[1982-86]: **a.** 11/286 (USSR); **b.** 11/273 (United Kingdom); **c.** 11/365 (Australia); **d.** 11/376 (Germany (Federal Republic of)); **e.** 11/297 (France); **f.** 11/397 (India).

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CCIR Documents

[1966-69]: XI/136 (United Kingdom); XI/194 (Netherlands).

[1970-74]: 11/1 (EBU); 11/63 (USA); 11/276 (Germany (Federal Republic of)).

[1974-78]: 11/54 (OIRT); 11/440 (OIRT).

ANNEX I

SYSTEMS USED IN VARIOUS COUNTRIES/GEOGRAPHICAL AREAS

Explanation of signs used in the table:

* : planned (whether the standard is indicated or not);

– : not yet planned, or no information received;

/ : the abbreviation following the stroke indicates the colour transmission system in use (NTSC, PAL or SECAM).

(Figures in brackets refer to the notes following the table.)

Country/Geographical area	System used in bands: I/III VHF broadcasting (Band 8)		IV/V UHF broadcasting (Band 9)	
Afganistan (Democratic Republic of)	D/SECAM		–	
Algeria (Algerian Democratic and Popular Republic)	B/PAL	(8)	G/PAL	(8)
Germany (Federal Republic of)	B/PAL	(12)	G/PAL	(12)
Angola (People's Republic of)	I/PAL	(8)	I/PAL*	(8)
Netherlands Antilles	M		–	
Saudi Arabia (Kingdom of)	B/SECAM, PAL	(8)	G/SECAM	(8)
Argentine Republic	N/PAL		N/PAL	
Australia	B/PAL	(11)	B/PAL	(11)
Austria	B/PAL		G/PAL	(1)
Bahrain (State of)	B/PAL		G/PAL	
Bangladesh (People's Republic of)	B/PAL		–	
Belgium	B/PAL		H/PAL	
Benin (People's Republic of)	K1/SECAM	(8)	K1/SECAM	(8)
Bermuda	M/NTSC		–	
Burma (Socialist Republic of the Union of)	M/NTSC		–	
Bolivia (Republic of)	M/NTSC		M/NTSC	
Botswana	I/PAL	(8)	I/PAL*	(8)
Brazil (Federative Republic of)	M/PAL		M/PAL	
Brunei Darussalam	B/PAL		–	
Bulgaria (People's Republic of)	D/SECAM		K/SECAM	
Burkina Faso	K1/SECAM	(8)	K1*/SECAM	(8)
Burundi (Republic of)	K1/SECAM*	(8)	K1/SECAM*	(8)
Cameroon (Republic of)	B/PAL		G*/PAL	
Canada	M/NTSC		M/NTSC	
Cape Verde (Republic of)	K1/SECAM*	(8)	K1/SECAM*	(8)
Central African Republic	K1/SECAM*	(8)	K1/SECAM*	(8)
Chile	M/NTSC		M/NTSC	
China (People's Republic of)	D/PAL		D/PAL	
Cyprus (Republic of)	B/SECAM		G/SECAM	
Colombia (Republic of)	M/NTSC		M*	
Comores (Islamic Federal Republic of)	K1/SECAM*	(8)	K1/SECAM*	(8)
Congo (People's Republic of the)	K1/SECAM*	(8)	K1/SECAM*	(8)
Korea (Republic of)	M/NTSC		M/NTSC	
Costa Rica	M/NTSC		M/NTSC	
Côte d'Ivoire (Republic of)	K1/SECAM	(8)	K1/SECAM*	(8)
Cuba	M/NTSC		M/NTSC	
Denmark (Including Greenland and Faeroe Islands)	B/PAL	(13)	G/PAL	(13)
Djibouti (Republic of)	B/SECAM	(8)	–	(8)
Egypt (Arab Republic of)	B/SECAM	(8)	G/SECAM	(8)
El Salvador (Republic of)	M/NTSC			
United Arab Emirates	B/PAL		G/PAL	
Spain	B/PAL	(13)	G/PAL	(13)
United States of America	M/NTSC		M/NTSC	
Ethiopia	B,G/PAL	(8)	G/PAL*	(8)
Finland	B/PAL	(13)	G/PAL	(13)
France	L/SECAM	(7)(14)	L/SECAM	(7)(14)
Gabonese Republic	K1/SECAM	(8)	K1/SECAM*	(8)
Gambia (Republic of the)	I/PAL	(8)	I/PAL*	(8)
Ghana	B/PAL	(8)	B/PAL*	(8)
Gibraltar	B/PAL		G/PAL	
Greece	B/SECAM		G/SECAM	
Guinea (Republic of)	K1/SECAM, PAL*	(8)	K1/PAL*	(8)
Guinea-Bissau (Republic of)	I/PAL*	(8)	I/PAL*	(8)
Equatorial Guinea (Republic of)	B/PAL	(8)	G/PAL*	(8)
Hong Kong	–		I/PAL	
Hungarian People's Republic	D/SECAM		K/SECAM	
India (Republic of)	B/PAL		–	
Indonesia (Republic of)	B/PAL		–	
Iran (Islamic Republic of)	B/SECAM		G/SECAM	
Iraq (Republic of)	B,G/SECAM	(8)	G/SECAM*	(8)
Ireland	I/PAL	(3)	I/PAL	(3)
Iceland	B/PAL	(13)	G*	(13)
Israel (State of)	B/PAL		G/PAL	(5)
Italy	B/PAL	(12)	G/PAL	(12)
Jamaica	N		–	
Japan	M/NTSC		M/NTSC	
Jordan (Hashemite Kingdom of)	B		G*	

Country/Geographical area	System used in bands: I/III VHF broadcasting (Band 8)		System used in bands: IV/V UHF broadcasting (Band 9)	
Kenya (Republic of)	B/PAL	(8)	B,G/PAL*	(8)
Kuwait (State of)	B/PAL	(8)	G/PAL*	(8)
Lesotho (Kingdom of)	I*/PAL	(8)	I*/PAL	(8)
Liberia (Republic of)	B/PAL	(8)	G/PAL*	(8)
Libya (Socialist People's Libyan Arab Jamahiriya)	B,G/PAL	(8)	B,G/PAL*	(8)
Luxembourg	B/PAL		G/PAL, L/SECAM	
Madagascar (Democratic Republic of)	K1/SECAM	(8)	K/SECAM*	(8)
Malaysia	B/PAL		G/PAL	
Malawi	I/PAL	(8)	I/PAL*	(8)
Maldives	B/PAL		–	
Mali (Republic of)	B/SECAM	(8)	G/SECAM*	(8)
Malta (Republic of)	B/PAL		–	
Morocco (Kingdom of)	B,G/SECAM	(8)	G/SECAM	(8)
Mauritius	B,G/SECAM	(8)	B,G/SECAM*	(8)
Mauritania (Islamic Republic of)	B/SECAM	(8)	B/SECAM*	(8)
Mexico	M/NTSC		M/NTSC	
Monaco	L/SECAM		G/PAL, G/SECAM	
Mongolian People's Republic	D/SECAM		-	
Montserrat	M/NTSC		–	
Mozambique (People's Republic of)	G/PAL*	(8)	G/PAL	(8)
Namibia	I/PAL	(8)	I/PAL	(8)
Niger (Republic of the)	K1/SECAM	(8)	K1/SECAM	(8)
Nigeria (Federal Republic of)	B/PAL	(8)	I/PAL*	(8)
Norway	B/PAL	(13)	G/PAL	(13)
New Zealand	B/PAL	(13)(10)	G/PAL	(13)(10)
Oman (Sultanate of)	B/PAL		G/PAL	
Uganda (Republic of)	B/PAL	(8)	-	(8)
Pakistan (Islamic Republic of)	B/PAL		G/PAL	
Panama (Republic of)	M/NTSC		M*/NTSC	
Papua New Guinea	B/PAL		G/PAL	
Netherlands (Kingdom of the)	B/PAL	(12)	G/PAL	(12)
Peru	M/NTSC		M/NTSC	
Poland (People's Republic of)	D/SECAM		K/SECAM	
Portugal	B/PAL		G/PAL	
Qatar (State of)	B/PAL		G/PAL	
Syrian Arab Republic	B/PAL		G/PAL	
German Democratic Republic	B/SECAM		G/SECAM	
Democratic People's Republic of Korea	D/PAL		K/PAL	
Roumania (Socialist Republic of)	D/PAL		K/PAL	
United Kingdom of Great Britain and Northern Ireland	–	(4)	I/PAL	(13)
Rwanda (Republic of)	K1/SECAM*	(8)	K1/SECAM*	(8)
St. Christopher and Nevis	M/NTSC		–	
Sao Tome and Principe (Dem. Rep. of)	B/PAL	(8)	-	(8)
Senegal (Republic of the)	K1/SECAM	(8)	K1/SECAM*	(8)
Seychelles	B/PAL	(8)	-	(8)
Sierra Leone	B/PAL	(8)	G/PAL*	(8)
Singapore (Republic of)	B/PAL		G*/PAL	(9)
Somali Democratic Republic	B/PAL	(8)	G/PAL*	(8)
Sudan (Republic of the)	B/PAL	(8)	G/PAL*	(8)
Sri Lanka (Democratic Socialist Republic of)	B		–	
South Africa (Republic of)	I/PAL		I/PAL	
Sweden	B/PAL	(13)	G/PAL	(13)
Switzerland (Confederation of)	B/PAL		G/PAL	(6)
Surinam (Republic of)	M/NTSC		–	
Tanzania (United Republic of)	I/PAL	(8)	I/PAL	(8)
Chad (Republic of the)	K1/SECAM*	(8)	K1/SECAM*	(8)
Czechoslovak Socialist Republic	D/SECAM		K/SECAM	
Thailand	B/PAL		G/PAL*	
Togolese Republic	K1/SECAM	(8)	K1/SECAM*	(8)
Tunisia	B/SECAM, PAL	(2)	G/SECAM, PAL	(2)
Turkey	B/PAL		G/PAL	
Union of Soviet Socialist Republics	D/SECAM		K/SECAM	
Uruguay (Oriental Republic of)	N/PAL		–	
Venezuela (Republic of)	M		–	
British Virgin Islands	M/NTSC		–	
Viet Nam (Socialist Republic of)	D/SECAM		K/SECAM	
Yemen Arab Republic	B/PAL	(8)	G/PAL*	(8)
Yemen (People's Democratic Rep. of)	B/PAL	(8)	-	(8)
Yugoslavia (Socialist Federal Republic of)	B/PAL		G/PAL	
Zaire (Republic of)	K1/SECAM	(8)	K1/SECAM*	(8)
Zambia (Republic of)	G/PAL*	(8)	G/PAL*	(8)
Zimbabwe (Republic of)	G/PAL*	(8)	G/PAL*	(8)

Note 1. – Austria reserves the right to the possible use of additional frequency-modulated sound carriers, in the band between 5.75 and 6.75 MHz, in relation to the picture carrier.

Note 2. – In Tunisia SECAM is used for broadcasting the national programmes; PAL is used for rebroadcasting other programmes.

Note 3. – System I will be used at all stations though with a vision to sound ratio of up to 10/1. In addition Ireland reserves the right to the possible use of an additional sound carrier in the band between 5.5 MHz and 6.75 MHz in relation to the vision carrier.

Note 4. – The United Kingdom has ceased to use Bands I and III for television broadcasting.

Note 5. – No final decision has been taken about the width of the residual sideband, but for planning purposes this country is willing to accept the assumption of a residual sideband 1.25 MHz wide.

Note 6. – The Swiss Administration is planning to use additional frequency-modulated sound carriers, in the frequency interval between the spacings of 5.5 and 6.5 MHz in relation to the picture carrier, at levels lower than or equal to the normal level of the sound carrier, for additional sound-tracks or for sound broadcasting.

Note 7. – In the French Overseas departments and territories, the system K1 is used instead of L/SECAM which is used in the metropolitan area.

Note 8. - This information has been taken from the preliminary requirements file as submitted by the administrations concerned to the ITU in preparation of the African Television Planning Conference AFBC(2). In a number of cases transmitters using different systems as those indicated in the requirements file may continue to operate for a transitional period.

Note 9. – Singapore reserves the right to use additional frequency-modulation sound channels in the band between 5.5 and 6.5 MHz in relation to the picture carrier, for additional sound channels for sound broadcasting.

Note 10. – In New Zealand ——————————————————————————————— the modulation levels are identical to those of System I.

Note 11. – Australia uses nominal modulation levels as specified for System I. For stereophonic sound transmission, an additional f.m. carrier is used similar to the system used in the Federal Republic of Germany .

Note 12. - The Federal Republic of Germany, Italy and the Netherlands use an additional f.m. carrier for stereophonic or two-channel sound transmission.

Note 13. - Denmark, Spain, Finland, Iceland, Norway, New Zealand, United Kingdom and Sweden have approved the use of an additional digital carrier for stereophonic or multichannel sound transmission.

Note 14. - In France, the use of an additional digital carrier for stereophonic or multichannel sound transmission is being investigated.

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[1986-90] : 11/41 (United Kingdom); 11/44 (Sweden); 11/64 (Japan); 11/79 (France); 11/80 (France); 11/142 (Netherlands).

ANNEX II

CHIEF TECHNICAL CHARACTERISTICS OF THE SECAM IV COLOUR TELEVISION SYSTEM

1. Signals transmitted

SECAM IV is compatible with standard black-and-white 625-line television systems, except system N. The luminance signal is obtained from gamma-corrected primary signals E'_R, E'_G, E'_B, and corresponds to the equation:

$$E'_Y = 0.30\ E'_R + 0.59\ E'_G + 0.11\ E'_B$$

The colour information is transmitted by two colour-difference signals:

$$D'_R = \frac{1}{1.14}\ (E'_R - E'_Y)$$

$$D'_B = \frac{1}{2.03}\ (E'_B - E'_Y)$$

Before modulation, the frequency band of the colour-difference signals occupies more than 1.5 MHz.

2. Transmission procedure

The colour-difference signals are transmitted by modulation of a sub-carrier. They are differentiated from one line to the next as follows:

Signal transmitted during one of the lines

$$E_{S1} = \left\{\sqrt{D'^2_B + D'^2_R} + E_p\right\}\cos\ [\omega_0 t + \varphi\ (t)]$$

Signal transmitted during the following line

$$E_{S2} = \left\{\sqrt{D'^2_R + D'^2_B} + E_p\right\}\cos\ (\omega_0 t + \varphi_0)$$

where:

E_p is a d.c. voltage equal to 10% of the maximum signal,

$$\varphi(t) = \text{arc tan}\ (D'_B / D'_R)$$

3. Frequency of the colour sub-carrier

The frequency of the colour sub-carrier is equal to: $f_0 = 4.43361875$ MHz. It is related to the line sweep frequency, $f_H = 15\,625$ Hz, by the following equation:

$$f_0 = (284 - 1/4)\ f_H + 25\ \text{Hz}.$$

4. Colour synchronization signal

The receiver switch is synchronized by synchronization signals transmitted with the composite video signal. They represent six wave trains of the colour sub-carrier, each train lasting about 40 µs. They are transmitted during the field returns in the 6th-11th lines of the first field and in the 319th-324th lines of the second field. During the even lines, the sub-carrier phase in the train is $\varphi = 90°$, and during all the odd lines $\varphi = 180°$. The amplitude of each wave train is equal to 30% of the composite signal E'_Y measured between the white and black levels.

5. **Reception procedure**

The colour-difference signals D'_R and D'_B are obtained by multiplication of the transmitted signals $E_{(2n+1)}$ and E_{2n}, each signal being delayed in turn by the duration of one line. The level of the signal E_{2n} must be 10 to 20 times higher than that of the signal $E_{(2n+1)}$.

To obtain the correct polarity for the signals E'_{B-Y} and E'_{R-Y} at each line, a switch working to the line periodicity is used.

REPORT 1077-1

ENHANCED 4:3 ASPECT RATIO TELEVISION SYSTEMS

(Question 42/11)

(1986-1990)

1. **Introduction**

Since the development of electronic television, the art has experienced a continuous evolutionary development which has produced a stream of improvements in the quality of pictures displayed to the viewer. A quantum step in quality occurred with the introduction of colour. New digital technology now offers storage, filtering and processing capabilities that will permit separate scanning standards for the picture source, emission and in the display, thereby providing increased quality through conventional television systems. New distribution media having wider bandwidth, such as broadcasting satellites, will permit new services with increased definition and wider aspect ratios.

2. **Definition of terms**

The term *enhanced television* designates a number of different improvements applicable to 525/60 and 625/50 television systems, providing an aspect ratio of 4 : 3 or wider, either with unchanged or with new emission standards.

The term enhanced television is used here to include all television systems (from source to display) not covered by Report 624 (Conventional television systems) and Report 801 (High definition television). It is noted that the signal format may change at different parts of the signal chain.

Enhanced television systems may be classified according to the following parameters:

Aspect ratio - either normal aspect ratio (4:3) or wider aspect ratio (for example, 16:9). Enhancements not involving a wider aspect ratio are described in this report. Wider aspect ratio systems are described in Report 1220.

Signal format - either composite (based on NTSC, PAL or SECAM) or component (for example, MAC systems).

It should be noted that there exists no clear definition of some of the terms widely used in the description of enhanced television systems. For example:

Compatibility: Various degrees of compatibility are possible. These range from full compatibility with existing systems, through systems that share the same scanning formats, to systems that have no direct compatibility with existing systems. The compatibility can also apply only to parts of the systems, for example, receiver compatibility.

CCIR 656-2 Recommendations of the CCIR, 1994

RECOMMENDATION ITU-R BT.656-2

INTERFACES FOR DIGITAL COMPONENT VIDEO SIGNALS IN 525-LINE AND 625-LINE TELEVISION SYSTEMS OPERATING AT THE 4:2:2 LEVEL OF RECOMMENDATION ITU-R BT.601

(Question ITU-R 65/11)

(1986-1992-1994)

The ITU Radiocommunication Assembly,

considering

a) that there are clear advantages for television broadcasting organizations and programme producers in digital studio standards which have the greatest number of significant parameter values common to 525-line and 625-line systems;

b) that a worldwide compatible digital approach will permit the development of equipment with many common features, permit operating economies and facilitate the international exchange of programmes;

c) that to implement the above objectives, agreement has been reached on the fundamental encoding parameters of digital television for studios in the form of Recommendation ITU-R BT.601;

d) that the practical implementation of Recommendation ITU-R BT.601 requires definition of details of interfaces and the data streams traversing them;

e) that such interfaces should have a maximum of commonality between 525-line and 625-line versions;

f) that in the practical implementation of Recommendation ITU-R BT.601 it is desirable that interfaces be defined in both serial and parallel forms;

g) that digital television signals produced by these interfaces may be a potential source of interference to other services, and due notice must be taken of No. 964 of the Radio Regulations (RR),

recommends

that where interfaces are required for component-coded digital video signals in television studios, the interfaces and the data streams that will traverse them should be in accordance with the following description, defining both bit-parallel and bit-serial implementations.

1. Introduction

This Recommendation describes the means of interconnecting digital television equipment operating on the 525-line or 625-line standards and complying with the 4:2:2 encoding parameters as defined in Recommendation ITU-R BT.601.

Part 1 describes the signal format common to both interfaces.

Part 2 describes the particular characteristics of the bit-parallel interface.

Part 3 describes the particular characteristics of the bit-serial interface.

Supplementary information is to be found in Annex 1.

CCIR 656-2 Recommendations of the CCIR, 1994

PART 1

Common signal format of the interfaces

1. General description of the interfaces

The interfaces provide a unidirectional interconnection between a single source and a single destination.

A signal format common to both parallel and serial interfaces is described in § 2.

The data signals are in the form of binary information coded in 8-bit or, optionally, 10-bit words* . These signals are:

- video signals,
- timing reference signals,
- ancillary signals.

2. Video data

2.1 Coding characteristics

The video data is in compliance with Recommendation ITU-R BT.601, and with the field-blanking definition shown in Table 1.

2.2 Video data format

The data words in which the eight most significant bits are all set to 1 or are all set to 0 are reserved for data identification purposes and consequently only 254 of the possible 256 8-bit words (or 1 016 of the possible 1 024 10-bit words) may be used to express a signal value.

The video data words are conveyed as a 27 Mword/s multiplex in the following order:

$$C_B, Y, C_R, Y, C_B, Y, C_R, \text{ etc.}$$

where the word sequence C_B, Y, C_R, refers to co-sited luminance and colour-difference samples and the following word, Y, corresponds to the next luminance sample.

2.3 Interface signal structure

Figure 1 shows the ways in which the video sample data is incorporated in the interface data stream. Sample identification in Fig. 1 is in accordance with the identification in Recommendation ITU-R BT.601.

2.4 Video timing reference codes (SAV, EAV)

There are two timing reference signals, one at the beginning of each video data block (start of active video, SAV) and one at the end of each video data block (end of active video, EAV) as shown in Fig. 1.

---

* Within this Recommendation, the contents of digital words are expressed in both decimal and hexadecimal form. To avoid confusion between 8-bit and 10-bit representations, the eight most significant bits are considered to be an integer part while the two additional bits, if present, are considered to be fractional parts.

For example, the bit pattern 10010001 would be expressed as 145_d or 91_h, whereas the pattern 1001000101 is expressed as 145.25_d or 91.4_h.

Where no fractional part is shown, it should be assumed to have the binary value 00.

Eight-bit words occupy the left most significant bits of a 10-bit word, i.e. bit 9 to bit 2, where bit 9 is the most significant bit.

TABLE 1

Field interval definitions

		625	525
V-digital field blanking			
Field 1	Start (V = 1)	Line 624	Line 1
	Finish (V = 0)	Line 23	Line 10
Field 2	Start (V = 1)	Line 311	Line 264
	Finish (V = 0)	Line 336	Line 273
F-digital field identification			
Field 1	F = 0	Line 1	Line 4
Field 2	F = 1	Line 313	Line 266

Note 1 – Signals F and V change state synchronously with the end of active video timing reference code at the beginning of the digital line.

Note 2 – Definition of line numbers is to be found in Recommendation ITU-R BT.470. Note that digital line number changes state prior to O_H as described in Recommendation ITU-R BT.601.

Each timing reference signal consists of a four word sequence in the following format: FF 00 00 XY. (Values are expressed in hexadecimal notation. FF 00 values are reserved for use in timing reference signals.) The first three words are a fixed preamble. The fourth word contains information defining field 2 identification, the state of field blanking, and the state of line blanking. The assignment of bits within the timing reference signal is shown in Table 2.

Bits P_0, P_1, P_2, P_3, have states dependent on the states of the bits F, V and H as shown in Table 3. At the receiver this arrangement permits one-bit errors to be corrected and two-bit errors to be detected.

2.5 *Ancillary data*

Provision is made for ancillary data to be inserted synchronously into the multiplex during the blanking intervals at a rate of 27 Mword/s.

Ancillary data signals may be conveyed in 10-bit form during the line-blanking period only, and in 8-bit form only during the active line periods of lines in the field blanking. (It should be noted that digital video tape recorders operating in accordance with Recommendation ITU-R BT.657 do not record data in the line-blanking period, nor during some lines in the field-blanking period.)

The reserved data values $00.x_h$ and $FF.x_h$ (see § 2.2) are reserved for identification purposes and must not appear in the ancillary data.

TABLE 2

Video timing reference codes

Data bit number	First word (FF)	Second word (00)	Third word (00)	Fourth word (XY)
9 (MSB)	1	0	0	1
8	1	0	0	F
7	1	0	0	V
6	1	0	0	H
5	1	0	0	P_3
4	1	0	0	P_2
3	1	0	0	P_1
2	1	0	0	P_0
1 (Note 2)	1	0	0	0
0	1	0	0	0

Note 1 – The values shown are those recommended for 10-bit interfaces.

Note 2 – For compatibility with existing 8-bit interfaces, the values of bits D_1 and D_0 are not defined.

F = 0 during field 1
1 during field 2

V = 0 elsewhere
1 during field blanking

H = 0 in SAV
1 in EAV

P_0, P_1, P_2, P_3: protection bits (see Table 3)

MSB: most significant bit

Table 1 defines the state of the V and F bits.

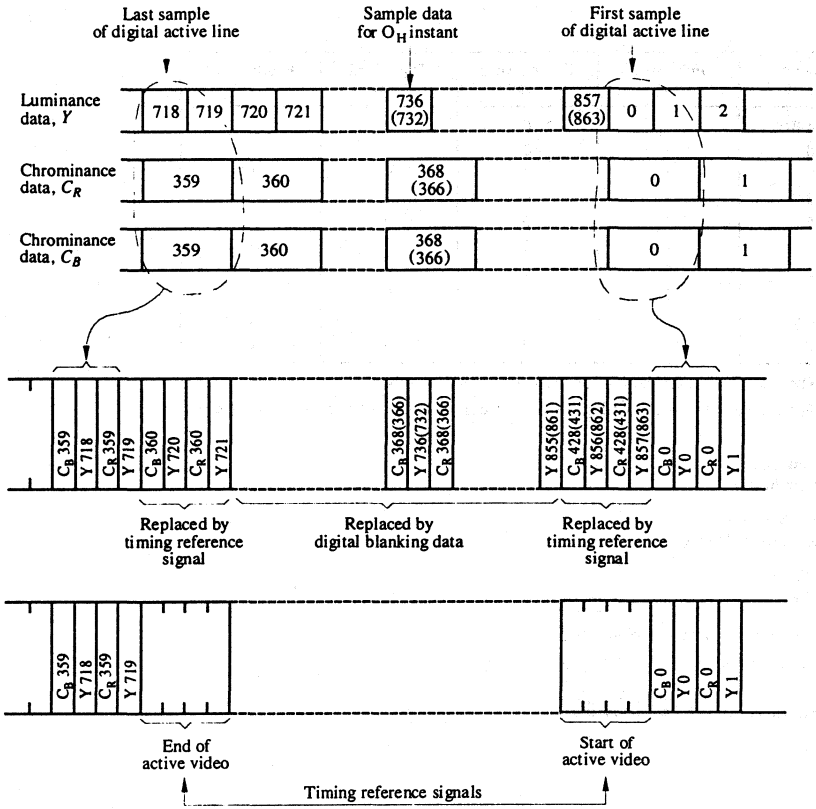
TABLE 3

Protection bits

F	V	H	P_3	P_2	P_1	P_0
0	0	0	0	0	0	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	0
1	0	0	0	1	1	1
1	0	1	1	0	1	0
1	1	0	1	1	0	0
1	1	1	0	0	0	1

FIGURE 1

Composition of interface data stream



Note 1 – Sample identification numbers in parentheses are for 625-line systems where these differ from those for 525-line systems. (See also Recommendation ITU-R BT.803.)

D01

All ancillary data signals carried during the active portions of lines in the field-blanking period must be preceded by the preamble:

00.x FF.x FF.x

Unless it is the intended function of a particular item of equipment, the ancillary signals must not be modified by that equipment.

2.6 Data words during blanking

The data words occurring during digital blanking intervals that are not used for the timing reference code or for ancillary data are filled with the sequence 80.0_h, 10.0_h, 80.0_h, 10.0_h etc. corresponding to the blanking level of the C_B, Y, C_R, Y signals respectively, appropriately placed in the multiplexed data.

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PART 2

Bit-parallel interface

1. General description of the interface

The bits of the digital code words that describe the video signal are transmitted in parallel by means of eight (optionally, ten) conductor pairs, where each carries a multiplexed stream of bits (of the same significance) of each of the component signals, C_B, Y, C_R, Y. The eight pairs also carry ancillary data that is time-multiplexed into the data stream during video blanking intervals. An additional pair provides a synchronous clock at 27 MHz.

The signals on the interface are transmitted using balanced conductor pairs. Cable lengths of up to 50 m (≈ 160 feet) without equalization and up to 200 m (≈ 650 feet) with appropriate equalization may be employed.

The interconnection employs a twenty-five pin D-subminiature connector equipped with a locking mechanism (see § 5).

For convenience, the bits of the data word are assigned the names DATA 0 to DATA 9. The entire word is designated as DATA (0-9). DATA 9 is the most significant bit. Eight-bit data words occupy DATA (2-9).

Video data is transmitted in NRZ form in real time (unbuffered) in blocks, each comprising one active television line.

2. Data signal format

The interface carries data in the form of eight (optionally, ten) parallel data bits and a separate synchronous clock. Data is coded in NRZ form. The recommended data format is described in Part 1.

3. Clock signal

3.1 General

The clock signal is a 27 MHz square wave where the 0-1 transition represents the data transfer time. This signal has the following characteristics:

Width: 18.5 ± 3 ns

Jitter: Less than 3 ns from the average period over one field.

Note 1 – This jitter specification, while appropriate for an effective parallel interface, is not suitable for clocking digital-to-analogue conversion or parallel-to-serial conversion.

3.2 Clock-to-data timing relationship

The positive transition of the clock signal shall occur midway between data transitions as shown in Fig. 2.

4. Electrical characteristics of the interface

4.1 General

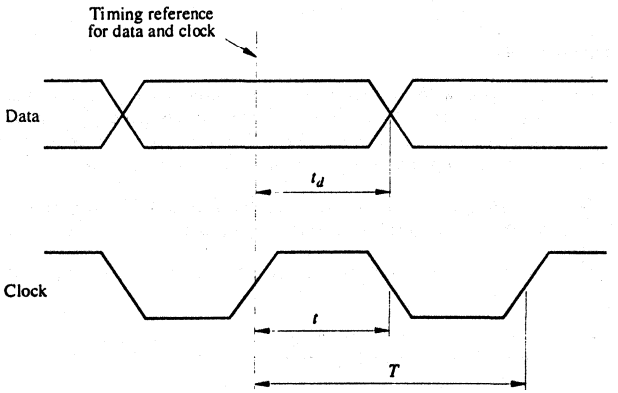
Each line driver (source) has a balanced output and the corresponding line receiver (destination) a balanced input (see Fig. 3).

Although the use of ECL technology is not specified, the line driver and receiver must be ECL-compatible, i.e. they must permit the use of ECL for either drivers or receivers.

All digital signal time intervals are measured between the half-amplitude points.

FIGURE 2

Clock-to-data timing (at source)



Clock period (625): $T = \frac{1}{1\,728 f_H} = 37$ ns

Clock period (525): $T = \frac{1}{1\,716 f_H} = 37$ ns

Clock pulse width: $t = 18.5 \pm 3$ ns

Data timing – sending end: $t_d = 18.5 \pm 3$ ns

f_H: line frequency

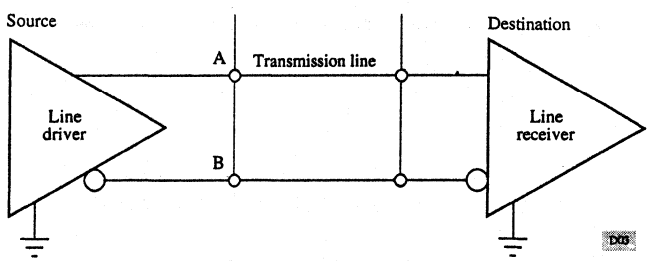
D02

4.2 Logic convention

The A terminal of the line driver is positive with respect to the B terminal for a binary 1 and negative for a binary 0 (see Fig. 3).

FIGURE 3

Line driver and line receiver interconnection



4.3 ***Line driver characteristics (source)***

4.3.1 *Output impedance*: 110 Ω maximum.

4.3.2 *Common mode voltage*: – 1.29 V ± 15% (both terminals relative to ground).

4.3.3 *Signal amplitude*: 0.8 to 2.0 V peak-to-peak, measured across a 110 Ω resistive load.

4.3.4 *Rise and fall times*: less than 5 ns, measured between the 20% and 80% amplitude points, with a 110 Ω resistive load. The difference between rise and fall times must not exceed 2 ns.

4.4 ***Line receiver characteristics (destination)***

4.4.1 *Input impedance*: 110 Ω ± 10 Ω.

4.4.2 *Maximum input signal*: 2.0 V peak-to-peak.

4.4.3 *Minimum input signal*: 185 mV peak-to-peak.

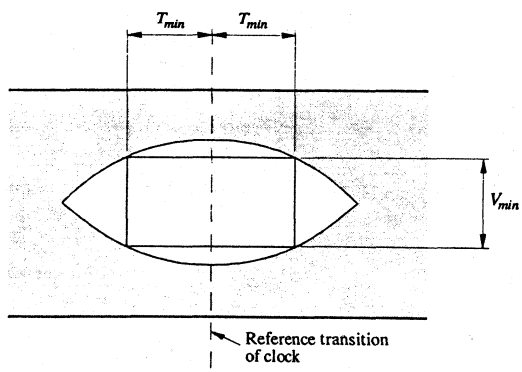
However, the line receiver must sense correctly the binary data when a random data signal produces the conditions represented by the eye diagram in Fig. 4 at the data detection point.

4.4.4 *Maximum common mode signal*: ±0.5 V, comprising interference in the range 0 to 15 kHz (both terminals to ground).

4.4.5 *Differential delay*: Data must be correctly sensed when the clock-to-data differential delay is in the range between ±11 ns (see Fig. 4).

FIGURE 4

Idealized eye diagram corresponding to the minimum input signal level



T_{min} = 11 ns
V_{min} = 100 mV

Note 1 – The width of the window in the eye diagram, within which data must be correctly detected comprises ± 3 ns clock jitter, ± 3 ns data timing (see § 3.2), ± 5 ns available for differences in delay between pairs of the cable. (See also Recommendation ITU-R BT.803.)

D04

5. Mechanical details of the connector

The interface uses the 25 contact type D subminiature connector specified in ISO Doc. 2110-1980, with the contact assignment shown in Table 4.

TABLE 4

Contact assignments

Contact	Signal line
1	Clock
2	System ground A
3	Data 9 (MSB)
4	Data 8
5	Data 7
6	Data 6
7	Data 5
8	Data 4
9	Data 3
10	Data 2
11	Data 1
12	Data 0
13	Cable shield
14	Clock return
15	System ground B
16	Data 9 return
17	Data 8 return
18	Data 7 return
19	Data 6 return
20	Data 5 return
21	Data 4 return
22	Data 3 return
23	Data 2 return
24	Data 1 return
25	Data 0 return

Note 1 – The cable shield (contact 13) is for the purpose of controlling electromagnetic radiation from the cable. It is recommended that contact 13 should provide high-frequency continuity to the chassis ground at both ends and, in addition, provide DC continuity to the chassis ground at the sending end. (See also Recommendation ITU-R BT.803.)

Connectors are locked together by two UNC 4-40 screws on the cable connectors, which go in female screw locks mounted on the equipment connector. Cable connectors employ pin contacts and equipment connectors employ socket contacts. Shielding of the interconnecting cable and its connectors must be employed (see Note 1).

Note 1 – It should be noted that the ninth and eighteenth harmonics of the 13.5 MHz sampling frequency (nominal value) specified in Recommendation ITU-R BT.601 fall at the 121.5 and 243 MHz aeronautical emergency channels. Appropriate precautions must therefore be taken in the design and operation of interfaces to ensure that no interference is caused at these frequencies. Emission levels for related equipment are given in CISPR Recommendation: "Information technology equipment – limits of interference and measuring methods", Doc. CISPR/B (Central Office) 16. Nevertheless, RR No. 964 prohibits any harmful interference on the emergency frequencies. (See also Recommendation ITU-R BT.803.)

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PART 3

Bit-serial interface

1. General description of the interface

The multiplexed data stream of 10-bit words (as described in Part 1) is transmitted over a single channel in bit-serial form. Prior to transmission, additional coding takes place to provide spectral shaping, word synchronization and to facilitate clock recovery*.

2. Coding

The uncoded serial bit-stream is scrambled using the generator polynomial $G1(x) \cdot G2(x)$, where:

$G1(x) = x^9 + x^4 + 1$ to produce a scrambled NRZ signal, and

$G2(x) = x + 1$ to produce a polarity-free NRZI sequence.

3. Order of transmission

The least significant bit of each 10-bit word shall be transmitted first.

4. Logic convention

The signal is transmitted in NRZI form, for which the bit polarity is irrelevant.

5. Transmission medium

The bit-serial data stream can be conveyed using either a coaxial cable (see § 6) or fibre-optic bearer (see § 7).

6. Characteristics of the electrical interface

6.1 Line driver characteristics (source)

6.1.1 Output impedance

The line driver has an unbalanced output with a source impedance of 75 Ω and a return loss of at least 15 dB over a frequency range of 5-270 MHz.

6.1.2 Signal amplitude

The peak-to-peak signal amplitude lies between 800 mV ± 10% measured across a 75 Ω resistive load directly connected to the output terminals without any transmission line.

6.1.3 d.c. offset

The d.c. offset with reference to the mid-amplitude point of the signal lies between +0.5 and −0.5 V.

6.1.4 Rise and fall times

The rise and fall times, determined between the 20% and 80% amplitude points and measured across a 75 Ω resistive load connected directly to the output terminals, shall lie between 0.75 and 1.50 ns and shall not differ by more than 0.50 ns.

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* Previous versions of this Recommendation have described a serial interface based on an 8B9B word-mapping technique. Due to implementation difficulties this technique is no longer recommended.

In addition to the 10-bit interface based on scrambling described in this revision of the Recommendation, there exists an 11-bit word format (10B1C) in which the eleventh bit is the complement of the least significant bit (LSB) of the scrambled data word.

*6.1.5 Jitter**

The timing of the rising edges of the data signal shall be between ± 10% of the clock period, as determined over a period of one line.

6.2 Line receiver characteristics (destination)

6.2.1 Terminating impedance

The cable is terminated by 75 Ω with a return loss of at least 15 dB over a frequency range of 5-270 MHz.

*6.2.2 Receiver sensitivity**

The line receiver must sense correctly random binary data when either connected to a line driver operating at the extreme voltage limits permitted by § 6.1.2 or when connected via a cable having a loss of 40 dB at 270 MHz and a loss characteristic of $1/\sqrt{f}$.

*6.2.3 Interference rejection**

When connected directly to a line driver operating at the lower limit specified in § 6.1.2, the line receiver must sense correctly the binary data in the presence of a superimposed interfering signal at the following levels:

d.c.	±2.5 V
Below 1 kHz:	2.5 V peak-to-peak
1 kHz to 5 MHz:	100 mV peak-to-peak
Above 5 MHz:	40 mV peak-to-peak

6.3 Cables and connectors

6.3.1 Cable

It is recommended that the cable chosen should meet any relevant national standards on electromagnetic radiation.

Note 1 – It should be noted that the ninth and eighteenth harmonics of the 13.5 MHz sampling frequency (nominal value) specified in Recommendation ITU-R BT.601 fall at the 121.5 and 243 MHz aeronautical emergency channels. Appropriate precautions must therefore be taken in the design and operation of interfaces to ensure that no interference is caused at these frequencies. Emission levels for related equipment are given in CISPR Recommendation: "Information technology equipment – limits of interference and measuring methods" (Doc. CISPR/B (Central Office) 16). Nevertheless, RR No. 964 prohibits any harmful interference on the emergency frequencies. (See also Recommendation ITU-R BT.803.)

6.3.2 Characteristic impedance

The cable used shall have a nominal characteristic impedance of 75 Ω.

6.3.3 Connector characteristics

The connector shall have mechanical characteristics conforming to the standard BNC type (IEC Publication 169-8), and its electrical characteristics should permit it to be used at frequencies up to 850 MHz in 75 Ω circuits.

* Parameters defined in § 6.1.5, 6.2.2 and 6.2.3 are target values and may be refined in the future with regard to practical implementations of the system.

7. Characteristics of the optical interface

To be defined (see Annex 1).

ANNEX 1

Notes concerning interfaces for digital video signals in 525-line and 625-line television systems

1. Introduction

This Annex includes supplementary information on subjects not yet fully specified, and indicates studies in which further work is required.

2. Definitions

Interface is a concept involving the specification of the interconnection between two items of equipment or systems. The specification includes the type, quantity and function of the interconnection circuits and the type and form of the signals to be interchanged by these circuits.

A parallel interface is an interface in which the bits of a data word are sent simultaneously via separate channels.

A serial interface is an interface in which the bits of a data word, and successive data words, are sent consecutively via a single channel.

3. Ancillary data signals

3.1 Introduction

The specification for ancillary data signals in § 2.5 of Part 1 of the present Recommendation covers only the parameters essential for the proper operation of the interface, i.e. preamble and location suitable for ancillary data signals. This section deals with additional format specifications that will be necessary for practical operation, together with a review of some projected applications.

3.2 Ancillary data signals format specifications

Mechanisms are being studied for both 8-bit and 10-bit ancillary data signals. They include procedures to spread long messages of linked sub-messages, and error detection and protection processes.

3.2.1 8-bit ancillary data signals

Studies held within the EBU have resulted in the reservation of lines 20 and 333 (625-line television systems) for equipment and self-checking purposes, and in the specification of the insertion mechanism as follows:

All ancillary data signals carried during the active portions of lines in the field-blanking period must be preceded by the preamble:

00.x FF.x FF.x

When ZZ has the value 15_h ((8,4) Hamming-coded form of D9-D6 set to 0000), this indicates that there are no further ancillary data signals on that line. Any value of ZZ other than 15_h must be interpreted as indicating the presence of an ancillary signal immediately following the preamble.

The insertion of an ancillary data signal must result in the change of ZZ from 15_h and must be accompanied by the insertion, immediately after the inserted data, of the preamble 00.x FF.x FF.x 15.x to indicate that the remainder of the line is available for the insertion of further ancillary signals.

Further consideration is being given to a five-word header to follow the preamble:

Data type:	TT_1	TT_2	TT_3	3 words (4 bits Hamming (8,4) coded)
Data length:	LL_1	LL_2		2 words (4 bits Hamming (8,4) coded)

Except for the preamble, all data are protected by a (8,4) Hamming code.

3.2.2 10-bit ancillary data signals

Consideration is being given (on the basis of studies conducted by the SMPTE) to a three-word header to follow the preamble:

Data identification (ID):	DID	1 word (8 bits + even and odd parity bits)
Data block number:	DBN	1 word (8 bits + even and odd parity bits)
Data count:	DC	1 word (8 bits + even and odd parity bits)

A checksum word is added at the end of the message.

3.3 Survey of applications based on ancillary data signals

3.3.1 Time code

Studies are in progress within the SMPTE to specify a time code carried by a signal called digital vertical interval time code (DVITC), that makes use of all the luminance data of one active line. The values chosen for these luminance data are specified in order that the D/A luminance waveform of the line fits in with the analogue waveform of a vertical interval time code signal.

3.3.2 Digital audio

Work is in progress within the SMPTE in order to specify the transport of up to 16 channels of 20-bit digital audio AES/EBU on a scrambled serial digital video interface at 270 Mbit/s. This transport mechanism is based on the use of 10-bit ancillary data signals. Work is in progress in order to support the optional additional four bits of the AES/EBU multiplex.

3.3.3 Monitoring and diagnostics

Studies are being conducted by the SMPTE in order to monitor the good operation of 10-bit digital video interfaces by generating error detection check-words and status flags, and by checking the validity of the check-words after transmission. The insertion of check-words and status flags is based on the draft format of 10-bit ancillary data signals.

3.3.4 Other applications

Other applications are being considered, including 4:3-16:9 aspect ratio signalling information, teletext, programme production and technical operation.

In addition, there exists detailed specifications covering panning information data in MAC/packet and HD-MAC/packet systems, and the digital assistance (DA) data in HD-MAC/packet systems.

4. Parallel interfaces

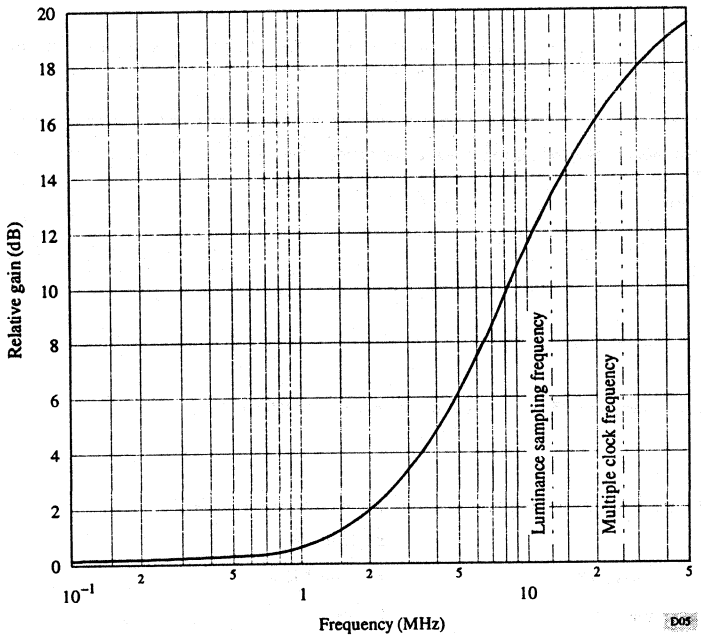
Appropriate coding of the clock signal, such as the use of an alternating parity (AP) coding, has been shown to extend the interconnection distance by reducing the effects of cable attenuation.

To permit correct operation with longer interconnection links, the line receiver may incorporate equalization.

When equalization is used, it may conform to the nominal characteristic of Fig. 5. This characteristic permits operation with a range of cable lengths down to zero. The line receiver must satisfy the maximum input signal condition of § 4.4 of Part 2 of this Recommendation.

FIGURE 5

Line receiver equalization characteristic for small signals



5. Serial interfaces

The transmission of signals can be achieved in both electrical form, using coaxial cable, and in optical form using an optical fibre. Coaxial cables would probably be preferred for connections of medium length, while preference would go to optical fibres for very long connection lengths.

It is possible to implement a system for detection of the occurrence of errors at the receiving end of the connection and thus automatically monitoring its performance.

In a fully integrated digital installation or system it may be useful for all interconnections to be transparent to any appropriate digital stream, irrespective of the message content. Thus, although the interface will be used to transmit a video signal, it should be "transparent" to the message content, i.e. it should not base its operation on the known structure of the message itself.

6. Optical interfaces

The need for specifications for optical interfaces has been recognized, and several approaches are currently under study. These include multi-mode fibre systems, monomode carrying a single signal or time division multiplexed signals (TDM), and also wavelength division multiplexes (WDM). The following is a tentative specification for a single-signal monomode system. The intended application range is from 0 km to approximately 2 km.

6.1 Source characteristics

6.1.1 Output wavelength

1 300 nm nominal

Maximum spectral line width 150 nm between half-power points.

6.1.2 Output power

The maximum and minimum output power values are still under study. It appears that a maximum output power value of approximately –8 dBm could be appropriate for the considered application range.

6.1.3 Logic convention

Maximum power output corresponds to the signalling of a logical 1.

6.1.4 Rise and fall times

To be decided.

6.1.5 Jitter

To be decided.

6.1.6 Isolation

Transmitter must withstand 10% of its output power returned by reflection.

6.2 Optical fibre link

FIBRE (compatible with optical fibre specified in ITU-T Recommendation G.652)

Fibre type	–	single mode
Dimensions: mode field dia.	–	9-10 μm ± 10%
cladding	–	125 μm
Operating window	–	around 1 300 nm
Mode field concentricity	–	< 3 μm
Cladding noncircularity	–	< 2%
Cut-off wavelength	–	1 100-1 280 nm
Attenuation at 1 300 nm	–	< 1 dB/km
Maximum dispersion (1 270-1 340 nm)	–	6 ps/nm · km
CONNECTOR		
Type	–	SC type as being standardized by the IEC. Other types are also under consideration.

6.3 Destination characteristics

The appropriate link bit-error ratio is still under study. It should be noted, however, that the error ratio required for the audio and other ancillary data signals might be more critical than the error ratio acceptable for the video signal.

6.3.1 Sensitivity

The bit-error ratio shall be specified in the form 10^{-xx} at less than –YY dBm and the relationship between BER and input power level shall be in line with theoretical values in the case of Gaussian noise.

6.3.2 Maximum input power

The maximum input power rating should be equal to the maximum value defined in § 6.1.2 above.

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7. Interference with other services

Processing and transmission of digital data, such as digital video signals at high data rates produces a wide spectrum of energy that has the potential to cause cross-talk or interference. In particular, attention is drawn in the present Recommendation to the fact that the ninth and eighteenth harmonics of the 13.5 MHz sampling frequency (nominal value) specified in Recommendation ITU-R BT.601 fall at the 121.5 and 243 MHz aeronautical emergency channels. Appropriate precautions must therefore be taken in the design and operation of interfaces to ensure that no interference is caused at these frequencies. Permitted maximum levels of radiated signals from digital data processing equipment are the subject of various national and international standards, and it should be noted that emission levels for such related equipment are given in CISPR Recommendation: "Information technology equipment – Limits of interference and measuring methods", Doc. CISPR/B (Central Office) 16.

In the case of the bit-parallel interface, work carried out by the Canadian Broadcasting Corporation (CBC) indicates that, with a correct shielding of the cables, no interference problem with other services is to be expected. Radiation levels should comply with the limits given in Table 5. These limits are equivalent to those of the FCC in the United States of America.

TABLE 5

Limits of spurious emissions (CSA Class A)

Frequency (MHz)	Maximum field strength at 30 m (dB(μV/m))
30-88	30
88-216	50
216-1 000	70

Transmission by optical fibres eliminates radiation generated by the cable and also prevents conducted common-mode radiation, but the performance of coaxial cable can also be made near-perfect. It is believed that the major portion of any radiation would be from the processing logic and high-power drivers common to both methods. Due to the wideband, random nature of the digital signal, little is gained by frequency optimization.

8. Conclusion

Further studies are required:

- to establish the types of ancillary signals to be carried, including their characterization and location in the data stream, and to propose international standards as necessary;
- on the practical methods required to ensure acceptably low levels of radiated interference from the digital signals;
- on optical interfaces for bit-serial signals.

Color space, digital coding, and sampling schemes for video signals

There are various ways to represent video information. This note describes some aspects of different color spaces, conversion between them, and normalized digital coding.

RGB at video camera output

The principal signal components of color camera or scanners, or other imaging pickup devices are Red, Green and Blue, RGB. These are also the principal components for video signal reproduction (i.e. picture display) at the monitor, as the CRT phosphors are comprised of these colors. But there is a non-linear relation between the camera signal pickup function (light input) and the CRT signal display function (light output). The transfer function is approximately exponential, and commonly referred to as "gamma" curve. Gamma is mainly a light reproduction function of the CRT.

$$R_{display} = R_{camera}^{\gamma}$$
$$G_{display} = G_{camera}^{\gamma}$$
$$B_{display} = B_{camera}^{\gamma}$$

During the development of the video transmission standards it was decided to compensate for this gamma-curve at the source side (camera, studio), and not to burden the television receiver with this effort and cost. The NTSC standard defines a gamma of 2.2, the PAL and SECAM standards defines a gamma of 2.8. Normally this gamma-correction is performed directly in the camera.

$$R_{transmit} = R_{pickup}^{1/\gamma}$$
$$G_{transmit} = G_{pickup}^{1/\gamma}$$
$$B_{transmit} = B_{pickup}^{1/\gamma}$$

The gamma-pre-corrected RGB signals at the camera output are stretched in the darker range and compressed in the lighter signal range. This has, as a side effect, a positive effect on noise influence on the transmission channel. The human eye is more sensitive to noise in dark areas, where the gamma behavior of the CRT reduces visibility.

Computer graphics generation is defined normally in "linear" RGB color space. The computer monitor of today has often a smaller gamma factor than used by the television standard definition, but there is no standard value. Sometimes it is compensated in the monitor itself, or by means of the look-up tables of the graphics RAMDAC, or not at all. The human eye is not very sensitive against gamma mismatch.

If video (camera) RGB gets merged with computer RGB, it is preferably be done in the same RGB space, including the assumed gamma. The anti-gamma compensation, as implemented in the Philips scaling ICs , compensates for a gamma-pre-correction of 1.4 only. The remaining gamma factor is assumed to be still performed by the computer monitor. A greater value of gamma-correction-compensation would lose more digital codes in the available 8-bit number range, and produce larger quantization steps in bright areas, which is not acceptable.

RGB can assume only positive values, and generate a cube like color space. The RGB components are commonly normalized to unity (e.g. 1 Volt peak-peak as analog signal). If any of the components is 0, it means there is no color of this component, if it is 1, there is full (100%) saturation of this color. All components equal zero represents the color 'black', all components equal 1 represents bright 'white'. The RGB cube is an additive color space.

Matrix to YUV (YCbCr)

In order to allow a compatible migration from black&white television to color television the YUV color space was utilized. Y stands for the luminance (lightness) information, and is compatible to black&white (and gray) signal. U and V are the so-called color difference signals B-Y an R-Y, and carry the additional color information (additive color space). The YUV representation of video information is also oriented on the human perception of visual information, whereby RGB representation is more based on the technical reproduction of color information. The human eye senses luminance and color with different receptors. There are less color receptors, and they have significant less spatial resolution. The YUV color space representation can take advantage of that fact, by spending less bandwidth for color difference information than for luminance information (see sampling schemes, later in this note).

Luminance Y can be positive only, the color difference signals U and V can be positive or negative. Commonly YUV is also normalized to unity (peak-to-peak = 1). The following matrix equation transforms gamma-pre-corrected and normalized RGB into normalized YUV (see also CCIR recommendation 601).

$$Y = 0.299 * R + 0.587 * G + 0.114 * B$$
$$U = C_b = (B - Y) = -0.169 * R - 0.331 * G + 0.500 * B$$
$$V = C_r = (R - Y) = 0.500 * R - 0.419 * G - 0.081 * B$$

(**NOTE:** For analog signal processing often un-normalized signals are used, which results in different number in the matrix equations, but does not change the cross relationship between RGB and YUV.)

Color space, digital coding, and sampling schemes for video signals

U and V form a square color plane. But for colors of natural pictures and due to some restrictions in the video standards NTSC and PAL, this square color plane is reduced to a color circle plane. The vectors of natural colors don't point into the extreme corners of the square UV plane. The size of that circle is further restricted, if luminance values are close to minimum or maximum. There can't be any color in black or white e.g.. (Artificial YUV signals, e.g., test signals can use those extreme combinations). The YUV color space is best represented by a round column, with the dimension of luminance Y as axle in its center, and this round YUV color space column is shaped to a point at the bottom and at the top.

CCIR rec. 601 describes also how to represent these YUV signals by digital codes. It is recommended not to use the entire available number range for nominal signal values, but leaving some margin, room for digital signal processing, e.g. for over and under shoots. In an 8 bit system, luminance Y black is coded with 16 decimal (= 10 hexadecimal), 100% white is coded with 235 decimal (= EB hexadecimal). The color difference signals Cb and Cr are coded in offset binary, which 'offsets' the 'no color' point into the middle of the number range to code 128 (80 hex). 100% color saturation uses the codes from 16 (10 hex) to 240 (F0 hex). 75% color saturation uses only codes from 44 (2C hex) to 212 (D4 hex) (see also data sheet SAA7151B, Fig.13, for example).

The codes 00 hex and FF hex should not be used for video signal coding. These two codes are reserved for synchronization purposes (see CCIR rec 656).

(Note regarding nomenclature: The terms "YUV" and "YCbCr" are referring to the same color space and cross relationship to RGB. The expressions "B-Y" and "R-Y" are normally used for non-normalized color difference signals. It is not part of any standard specification, but some literature is using the term "YUV" to indicate analog signal representation, and the term "YCbCr" for its digital representation. Most data sheets and documents in this book are using both terms interchangeable for digital signal representation of normalized signals.)

The CCIR recommendation 601 (re-printed elsewhere in this book) gives an example of a digital RGB to YUV conversion. It is assuming digital sampled RGB, defined in codes like luminance signal Y, i.e., between 16 for black and 235 for full saturation. The given equation assumes a matrix realization by means of 8x8bit multipliers, which is only approximating the correct relationship. This equation system should not be used as reference to construct the inverse matrix from YUV to RGB. Today's technology allows matrix implementation by means of look-up tables, avoiding the limiting multiplier resolution and truncation problem.

The accurate digital RGB to digital YCrCb conversion is described by the following matrix:

$$\begin{bmatrix} Y \\ Cr \\ Cb \end{bmatrix} = \begin{bmatrix} 0.299 & 0.587 & 0.114 \\ \left(\frac{0.701}{(2*0.701)} * \frac{224}{219}\right) & \left(-\frac{0.587}{(2*0.701)} * \frac{224}{219}\right) & \left(\frac{0.114}{(2*0.701)} * \frac{224}{219}\right) \\ \left(-\frac{0.299}{(2*0.886)} * \frac{224}{219}\right) & \left(-\frac{0.587}{(2*0.886)} * \frac{224}{219}\right) & \left(\frac{0.886}{(2*0.886)} * \frac{224}{219}\right) \end{bmatrix} * \begin{bmatrix} R \\ G \\ B \end{bmatrix}$$

The digital RGB ranges from 16 to 235, i.e. over 219 possible values. The digital CrCb goes from 16 to 240, uses 224 possible values. This causes a re-normalization factors.

The inverse matrix from digital YCrCb to digital RGB (16 to 235) calculates to :

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} 1 & 1.371 & 0 \\ 1 & -0.698 & -0.336 \\ 1 & 0 & 1.732 \end{bmatrix} * \begin{bmatrix} Y \\ Cr \\ Cb \end{bmatrix}$$

Color space, digital coding, and sampling schemes for video signals

YIQ, and other YUV related color spaces

YIQ color space is similar to YUV color space except that it has the I and Q color axes rotated 33 degrees with the respect to the U and V axes of the YUV definition.. "I" means "in phase", and "Q" means "quadrature phase". This color space was adopted by early NTSC systems to take full advantage of the human eye color response with respect to color bandwidth capability.

```
I = V * cos(33°) - U * sin(33°)
Q = V * sin(33°) + U * cos(33°)
```

The Philips digital decoder have fully adjustable "hue" control. The demodulation angle can be programmed to any value, and can achieve an I-Q demodulation, i.e., generating I and Q outputs instead of U and V.

Some other color space approaches (like HSI, or HSV, or HSL etc.) describe the UV plane in polar coordinates by means of a vector, its length(S = saturation) and its angle(H = hue). The luminance (Intensity, Value, Lightness) corresponds to the Y of YUV space. This color space representations are related to the quadrature encoding of U and V onto a color subcarrier, in the transmission standards NTSC and PAL.

CMYK for color printer

CMYK color space is a subtractive color space used for color printing. CMYK stands for Cyan, Magenta, Yellow and Black. It describes, which color component is removed from white, to generate a certain wanted/printed color. In theory, only the CMY portion is required, however, in actual printing ink applications, black ink is added to enhance the contrast ratio and purity of the black portion of the image. K is defined as min(CMY), that is, K is equal the lowest value of C, M, or Y.

The relation of CMY to RGB is given vectorally as :

$$\begin{bmatrix} C \\ M \\ Y \end{bmatrix} = \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} - \begin{bmatrix} R \\ G \\ B \end{bmatrix}$$

4:4:4 sampling (RGB, YCbCr)

Figure 1 illustrates the sampling positions for 4:4:4 sampling, which is mainly used for RGB, but can also be used for YUV or YCbCr. At each pixel a sample is taken for R, G, and B, or Y, U, and V etc.

All three components have the same spatial resolution (bandwidth). If 8 bits per component is used, a 24 bit system is required.

4:2:2 YCbCr sampling

Figure 2 represents a more effective sampling format, in which Y samples are measured at each pixel position, and Cb and Cr samples only at every second pixel position. By that the color information has horizontally a resolution, that is half of that of luminance. The human eye does not perceive chrominance with the same clarity as luminance,. therefore this type of data reduction causes very little visual loss of content. The 4:2:2 sampling scheme reduces the data bandwidth need by a third.

Cb and CR samples are co-sited with every second Y samples, but starting with the first Y sample of each line. If 8 bits per component is used, a 16 bit system is required.

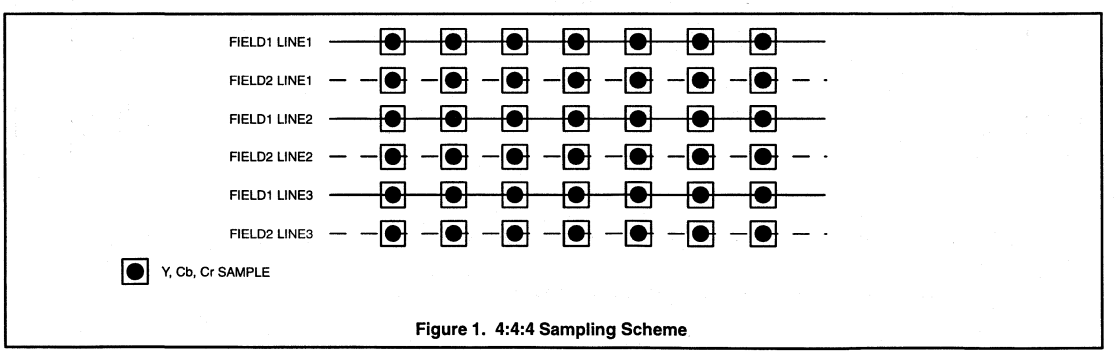


Figure 1. 4:4:4 Sampling Scheme

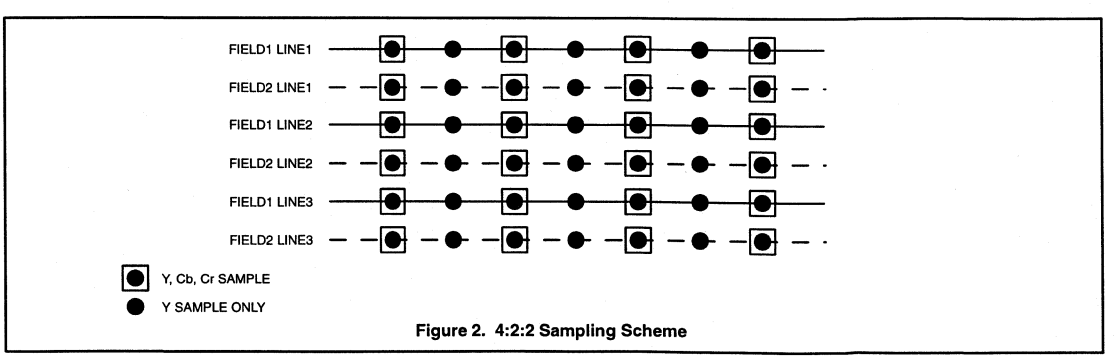


Figure 2. 4:2:2 Sampling Scheme

Color space, digital coding, and sampling schemes for video signals

4:1:1 YCbCr (orthogonal) sampling

Figure 3 is an example of 4:1:1 sampling, often used in consumer type video products. The achievable color bandwidth in this case is only one third that of luminance. But in broadcasted video (NTSC, PAL, or SECAM), or in tape-recorded video, there is normally not more chroma bandwidth supported/available.

The CbCr samples are taken co-sited with every fourth luminance pixel, but starting with the first luminance sample of each line. An 8 bit per component system is capable of fitting into a 12 bit wide frame buffer. 7 bit per component and 6 bit per component systems are also used in combination with 4:1:1 sampling, which reduces the needed frame buffer capacity even more (e.g., for PIP function on television sets).

4:2:0 YCbCr (spatial) sampling

This sampling scheme is used generally for MPEG and H-261 compression standards, and is also called "coded picture sampling". Figure 4 shows the two dimensional 2:1 sub-sampling of color pixels relative to luminance pixels. The CbCr samples are not co-sited with a luminance sample, but representing the color information for a quartet of four Y pixels, ordered in a square. The CbCr values are normally derived (calculated) from a 4:4:4 or 4:2:2 sampling scheme by both horizontal and vertical filtering and interpolation. Usually the CbCr values are transported only every second scan line with pairs of Y samples, the other line carries only Y samples (4:2:0). The overall data bandwidth of 4:2:0 sampling is identical to 4:1:1 sampling.

In the example in Figure 4 a non-interlaced video source is represented, as those compression standards know only 'pictures' and use whole frames, or just one field.

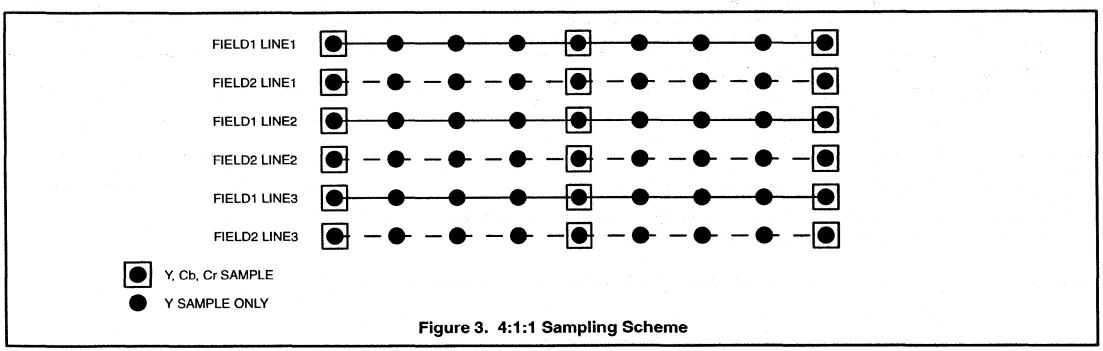


Figure 3. 4:1:1 Sampling Scheme

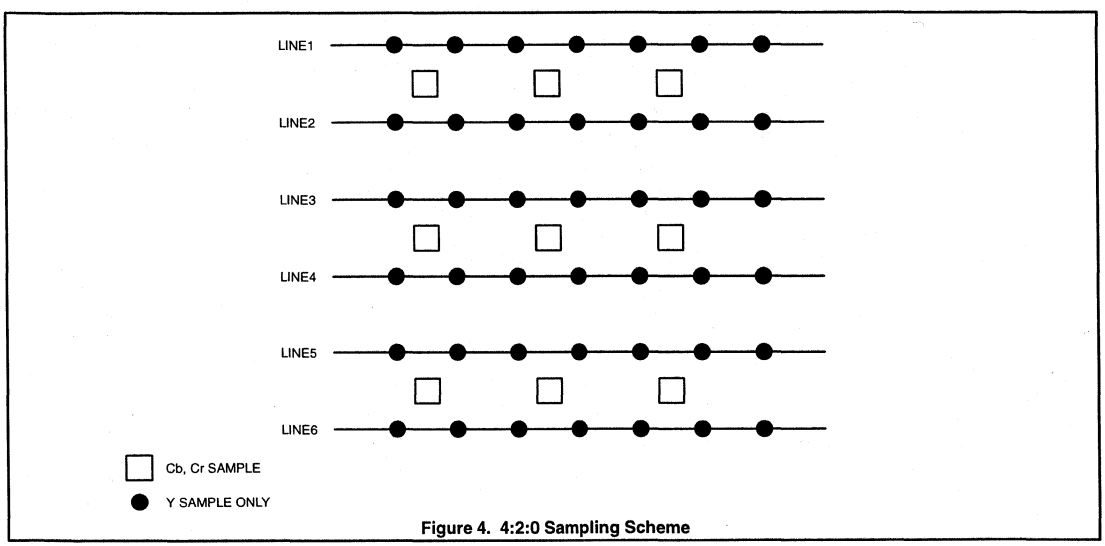


Figure 4. 4:2:0 Sampling Scheme

Video signal bandwidth/resolution

BANDWIDTHS OF VARIOUS VIDEO SIGNALS

FORMAT	FORMAT RESOLUTION		BANDWIDTH	BANDWIDTH
	TOTAL RESOLUTION	ACTIVE RESOLUTION	MBytes/sec (burst)[1]	MBytes/sec (continuous)[2]
CCIR 601 (30 Frames per Second, 4:3 Aspect Ratio)				
QCIF	214 × 131	176 × 120	1.68	1.27
CIF	429 × 262	352 × 240	6.74	5.07
Full resolution	858 × 525	720 × 485	27.0	20.95
CCIR 601 (25 Frames per Second, 4:3 Aspect Ratio)				
QCIF	216 × 156	176 × 144	1.69	1.27
CIF	432 × 312	352 × 288	6.74	5.07
Full resolution	864 × 625	720 × 576	27.0	20.74
Square Pixel (30 Frames per Second, 1:1 Aspect Ratio)				
QCIF	195 × 131	160 × 120	1.53	1.15
CIF	390 × 262	320 × 240	6.13	4.61
Full resolution	780 × 525	640 × 480	24.55	18.43
Square Pixel (25 Frames per Second, 1:1 Aspect Ratio)				
QCIF	236 × 156	192 × 144	1.84	1.38
CIF	472 × 312	384 × 288	7.36	5.53
Full resolution	944 × 625	768 × 576	29.5	22.12

NOTE:
1. Burst bandwidth assumes that the transfer of video occurs only during the active period.
2. Continuous bandwidth assumes entire frame time is used to transfer active video.

Data rates given here are for 16-bit 4:2:2 YC_RC_B video; if 24-bit RGB is used, the rates are 150% higher.

What is Teletext?

Author: Marc Schneider

WHAT IS TELETEXT?

Teletext is a system that was developed in the late '70s to deliver public information to television viewers in the comfort of their home. Since it's creation, Teletext has undergone several enhancements to improve it's flexibility, and yet maintain a low overall cost to the customer. In the 80's, new extensions were added to Teletext handle independent data services, and the format continues to expand to this day.

Multimedia computing is now discovering the benefits of having Teletext reception as another value added feature. With the ever increasing quest for more information on the desktop,applications can range from stock trading, electronic news, E–Mail, downloadable software,education, and customer service just to name a few.

Even though Teletext format has been enhanced quite a lot since it's original inception, the basic functionality is still very much the same. Here are a few examples of this:

Basic Teletext system overview

- Teletext is a format to transmit data within a video signal
- Can be multiplexed with the video, or not
- Data rate is a few MBit/s
- Accepted global standard (WST)
- Secure delivery data channel
- Data error checking
- Low cost
- Uni-directional
- Page format: 24 rows × 40 columns

HOW IS IT ENCODED IN A VIDEO SIGNAL?

There are two common methods for encoding the Teletext data into a video stream. The most common is to use the Vertical Blanking Interval or VBI. This is a generally unused space located between the vertical sync pulse and the actual active video picture. Because of the limited number of available lines in the VBI, the actual amount of data that can be transmitted is limited to about 17.76Kbits/sec times the number of transmitted lines. So, if we were to transmit 3 lines of Teletext data per field, that would work out to:

One horizontal line (525) of data = 37 Bytes or = 296 bits per line/field

296	
× 60	(fields per second)
17,760	bits/sec per line data rate
× 3	lines/sec
53,280	bits/sec

So, a three line/field transmission has an effective data rate close to ISDN rates!

If, however, the broadcaster has a dedicated channel (cable, MDS, satellite, video LAN,etc.), it is then possible to put Teletext data on *every* line. In this case, the data through–output would increase to almost half of Ethernet rates!

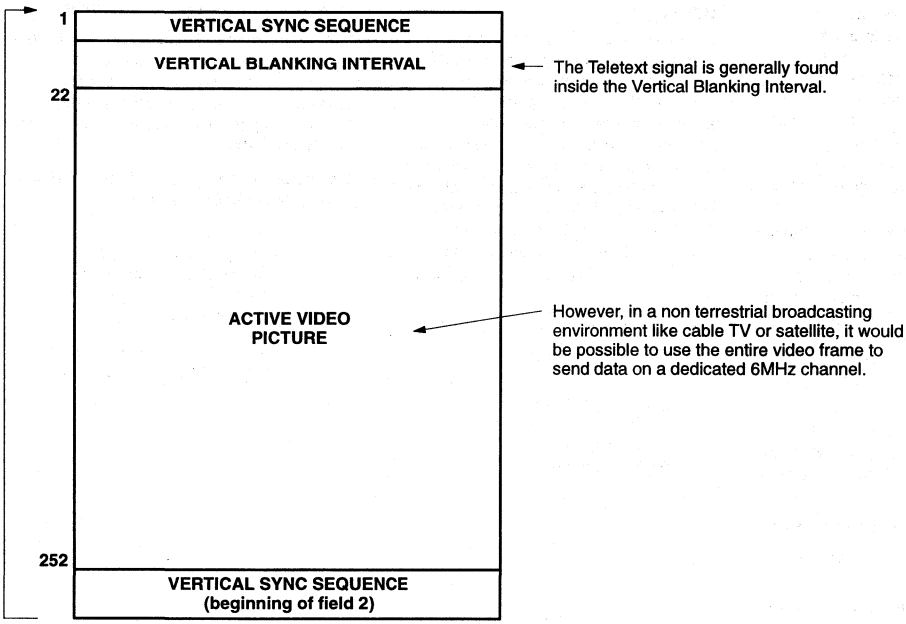
One horizontal line (525) of data = 37 Bytes or = 296 bits per line/field

296	
× 60	(fields per second)
17,760	bits/sec per line data rate
× 251	(usable lines/field)
4,457,760	bits/sec data rate

Now the data rate has been increased to over 4.5Mbits/sec, half Ethernet speed!

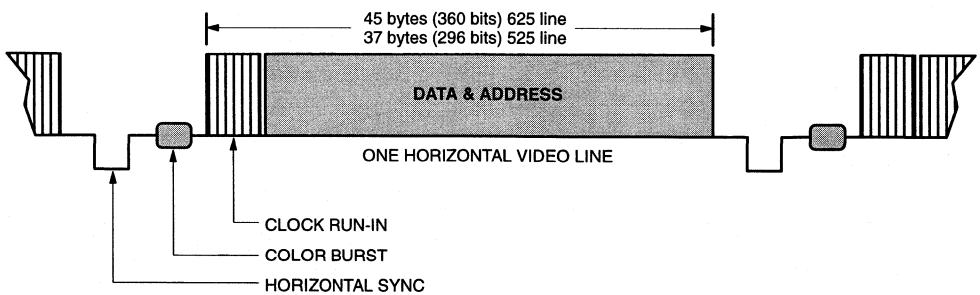
What is Teletext?

WHERE CAN TELETEXT DATA RESIDE IN A VIDEO SIGNAL?



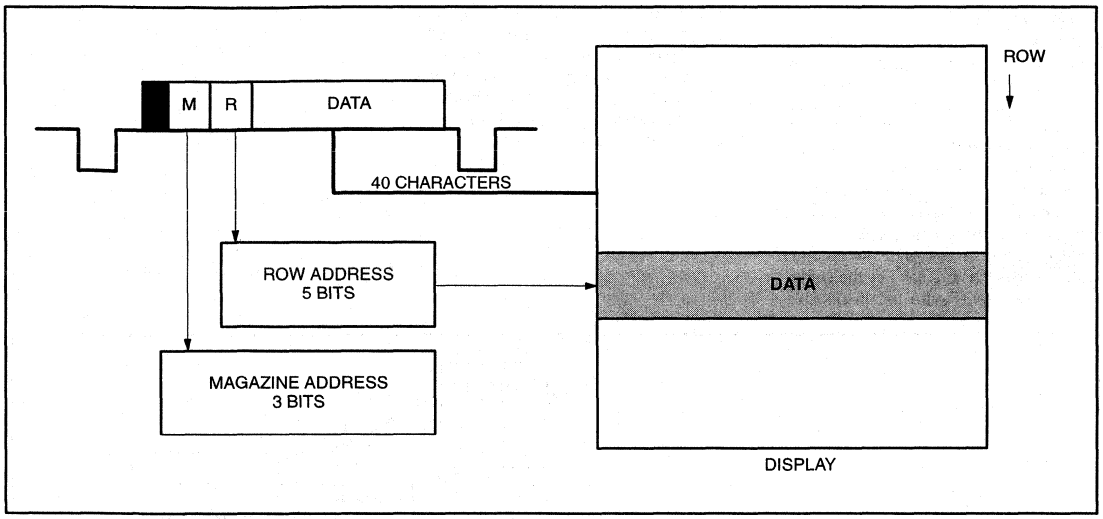
WHAT DOES THE DATA LOOK LIKE?

Each Video line use to convey the Teletext data is called a Teletext Data Line.

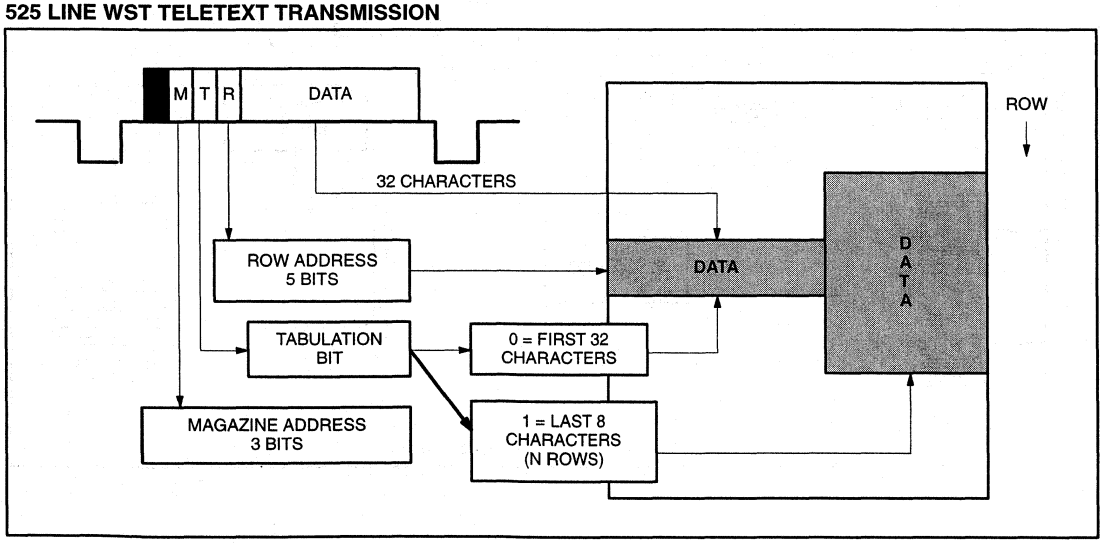


What is Teletext?

625 LINE WST TELETEXT TRANSMISSION



525 LINE WST TELETEXT TRANSMISSION



What is Teletext?

HOW IS IT BROADCAST TO CUSTOMERS?

The most common way for Teletext to reach a large customer base is to send it using normal over-the-air broadcast television transmissions. Although this is the common approach, it is not the only method. Cable companies can distribute the data on a dedicated channel or add it to the VBI of an existing channel. Multi–point Distribution System operators (MMDS or wireless cable) can provide Teletext data via direct microwave transmissions to the customer. Satellite broadcasters can use the same approach as well. Figure 1 is an example.

And signal distribution isn't required to general off-air distribution. Teletext can also be used over a video local area network (VLAN) for supporting anything from printing devices, data servers, and even individual workstations. A simple way to provide secure data delivery in a growing multi-media environment and at a low cost.

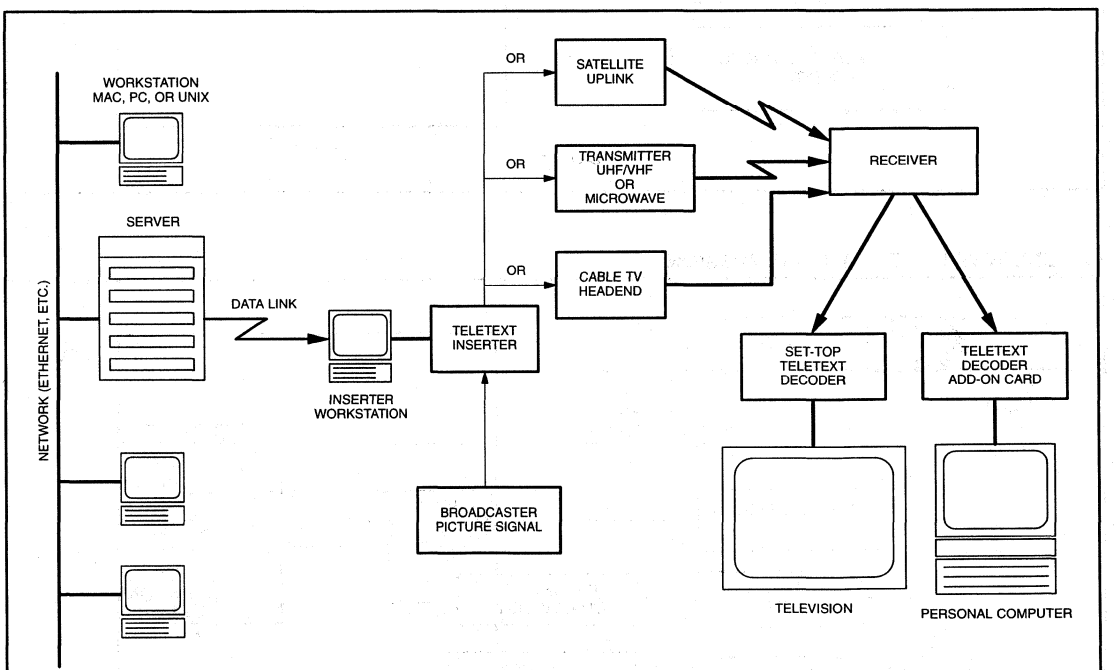


Figure 1. A Broadcast transmission example

What is Teletext?

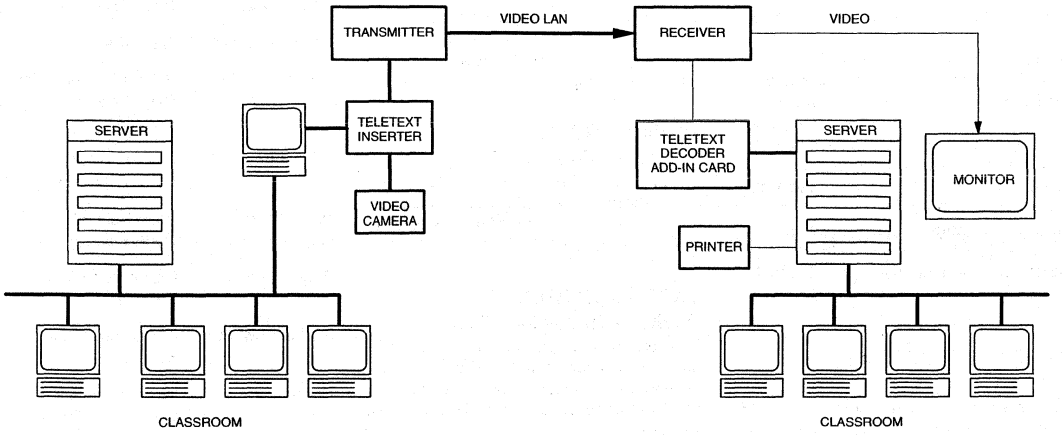


Figure 2. An example of remote corporate training

In Figure 2, an instructor at a corporate headquarters could be teaching a class locally while also delivering the same information to students at multiple remote sites. In addition to the normal video and audio transmissions, the instructor could send data specifically to individual students at the remote site (or sites) on demand over the same video link. Teletext offers a new way to add addition information to video training without affecting the current video distribution network.

What is Teletext?

WHAT ABOUT ERROR CORRECTION?

The WST standard provides for two basic layers of error correction for page format Teletext, Hamming code is used for addressing, and parity for character data. The Hamming correction can catch both single and double bit errors, while the parity checking can resolve single bit errors. For Packet 31 transmissions, there is the addition of a 16 bit CRC check added to the end of the data packet, although this is optional. Both page format Teletext and Packet 31 could be encoded with 8 bit data allowing any third party protection format to be used.

WHAT ARE TELETEXT PACKETS?

Packets are the actual data information with an assigned address. There are three basic types of packet in the WST standard, page headers, normal rows, and extension packets. Each has a specific assigned purpose and bit format:

PAGE HEADERS – Packet Address 0

This packet contains page number and control information, plus 32 display characters including 'TIME'. It appears at the top of the display.

NORMAL ROWS – Packet Address 1 – 23

These contain 32 bytes (40 bytes 625 line) of data defining a row of 32 (40) characters on the display. The address defines the vertical position of the row.

EXTENSION PACKETS – Packet Address 24 – 31

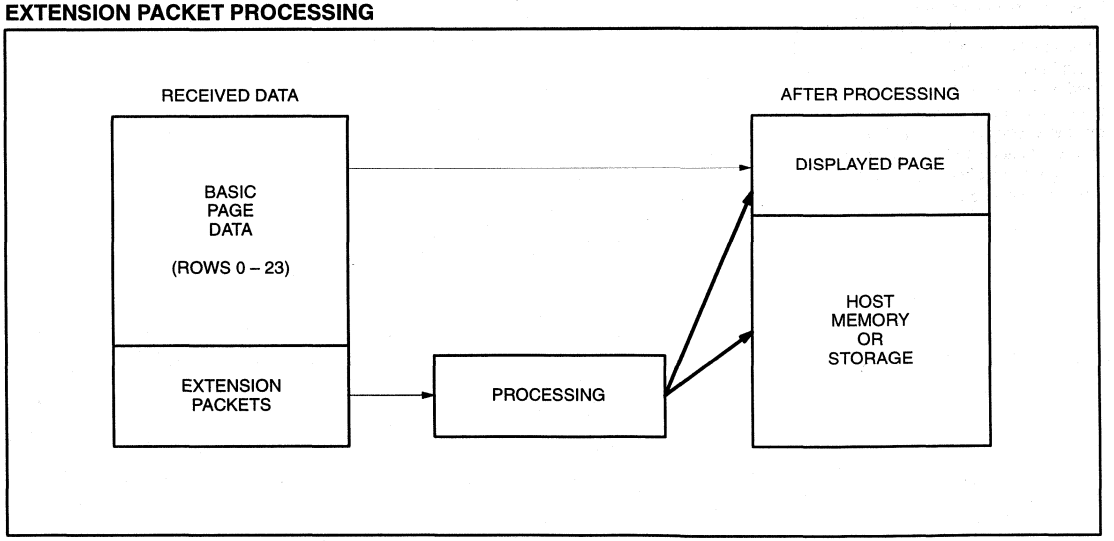
Typically each has its own special function and is not directly displayed. They are used to enhance the performance of the more advanced decoders or to provide special data services.

There are a total of eight extension packet functions pre-defined under the WST standard. They are:

Packet Number	Function
Packet (row) 24	Page Extension
Packet (row) 25	Telesoftware
Packet (row) 26	Schedule Information & Page Related Redefinition
Packet (row) 27	Linked Pages (FLOF/FASTEXT)
Packet (row) 28	Page Related Redefinition
Packet (row) 29	Magazine Related Redefinition
Packet (row) 30	Broadcaster Data Services
Packet (row) 31	Independent Data Services (Multi–media)

With these extensions, Teletext can support a wide variety of functional services from programming a VCR to acquiring the latest software for a home or business computer.

EXTENSION PACKET PROCESSING



What is Teletext?

HOW DOES A DECODER FUNCTION?

There are two basic architectures to a WST decoder. The first is for standalone applications, as in a television set or a set–top decoder (Figure 3). These units are self contained and usually offer limited capabilities for extension packet handling. Generally the decoder is made up of a video input processor (VIP), the Teletext processor, some form of page memory storage for received data, a character generator to drive a CRT, and a character language font ROM for displaying the text in the native language the receiver is being used. These processors offer a simple serial interface for communicating with the televisions microcontroller. Although the actual data usually can be removed via this interface, it is generally not recommend for performance reasons.

The second method for receiving Teletext data is to use a acquisition only decoder. This type of decoder relies on a host microprocessor to determine what happens to the received data once is has been acquired and error checked. At this point, the processor must handle all of the storage and display functions remaining to present the data to the user. This is the preferred method used for teletext interacting with a personal computer. Because the host computer already has memory, disk, networking, and advanced display functions, there is no need to have these function duplicated in the Teletext receiver. (See Figure 4.)

Typically a decoder used in this method supports all of the packets described under the WST standard. The text processor is a minimal Teletext decoder only handling the error correction and acquisition functions. It is therefore quite flexible in supporting multiple packet format reception.

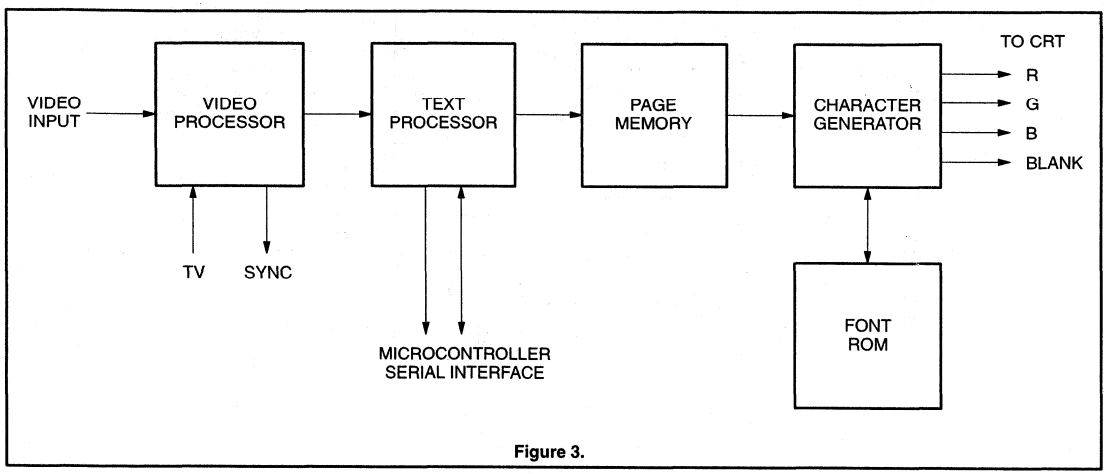


Figure 3.

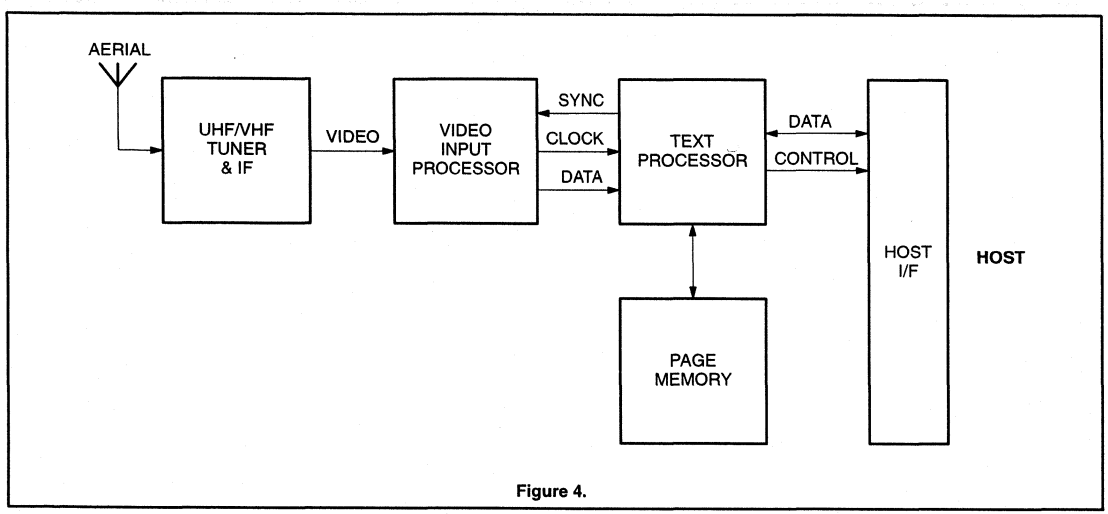


Figure 4.

What is Teletext?

WHAT ARE SOME RECOMMENDED CONFIGURATIONS?

For basic level 1 Teletext reception in the 525 line television system, the standard configuration is comprised of the SAA5191 data slicer, SAA9042 WST Teletext decoder, a DRAM for local storage, and either a microcontroller as the control host or and I2C UART to interface to an external host (i.e., a microcomputer). This solution will not decode Packet 31 transmissions but will decode all other extension packets.

Figure 5 demonstrates a standalone decoder with the acquisition and display sections of the SAA9042 timed from the incoming video signal. Although this will work quite well for set–top or computer add–in card applications, it should be noted that in the absence of any incoming composite sync signal, or if the signal is very noisy, the field sync integrator in the acquisition section will not be able to detect the start of the field. Consequently the display section will not receive a reliable vertical trigger, and thus a stable text display cannot be guaranteed under all signal conditions.

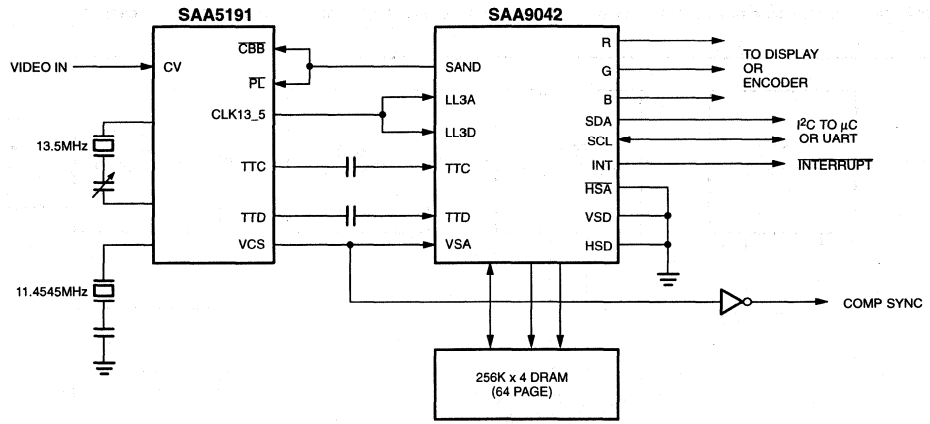


Figure 5. Standalone Example (Direct Sync Mode Shown)

What is Teletext?

For acquisition only and Datacast reception (packet 31), the SAA5250 CMOS Interface for Data Acquisition and Control, or CIDAC, is a WST decoder designed for direct interfacing to a microprocessor host. Unlike the SAA9042, CIDAC only has one acquisition channel and support for only a 2K×8 static RAM for local buffering. But because CIDAC was intended to interface to a microprocessor, the need for most of the larger local storage and multiple acquisition channels are unnecessary in this application since the microcomputer host has superior storage and data transfer capabilities already.

In the circuit shown in Figure 6, the SAA5231 is used purely as a data slicer since the CIDAC doesn't require a dot clock for display the VCO section of the SAA5231 is left unused. Because the CIDAC was design as a multi-Teletext format decoder, the chip was designed primarily for full field data reception. For VBI applications, it is suggested to add a simple circuit between the SAA5231 and the CIDAC that creates a VBI 'window'.

The purpose of the VBI window generator is simple. To aid the CIDAC in the reduction of invalid data being processed, and to provide the host microprocessor with a data valid interrupt so the microprocessor will not be required to poll the CIDAC on a regular basis to determine if new data has arrived.

The TDA4820T is a adaptive sync separator which provides the PLD with vertical and composite sync. With these signals at hand, the PLD simply counts the number of horizontal lines after the vertical sync period until the desired active video line for the window to open is found. Upon finding this, the PLD then allows the data from the SAA5231 to be passed onto the CIDAC, but not before it is gated with the composite blanking signal first. This has the result of passing only valid data for a select number of horizontal lines and pre-filtering out any sync or color burst information which could be confused as valid data.

The other function the PLD generates is a simple interrupt pulse for the microprocessor. This pulse can be generated before, during, or after the window closes. The choice is up to the PLD's designer and is important for the microprocessors best performance. In addition, it is recommended that the PLD designer add a hardware select line from the PLD to the microprocessor to allow it to select full field or VBI reception for flexibility.

In conclusion, the WST Teletext format allows a system designer great flexibility while providing a low cost means to deliver secure data over a wide area network. Philips Semiconductors has been providing complete Teletext solutions since the formats early beginning and as a customer you can look forward to continued innovative and cost effective solutions from Philips Semiconductors, World wide supplier of Teletext components.

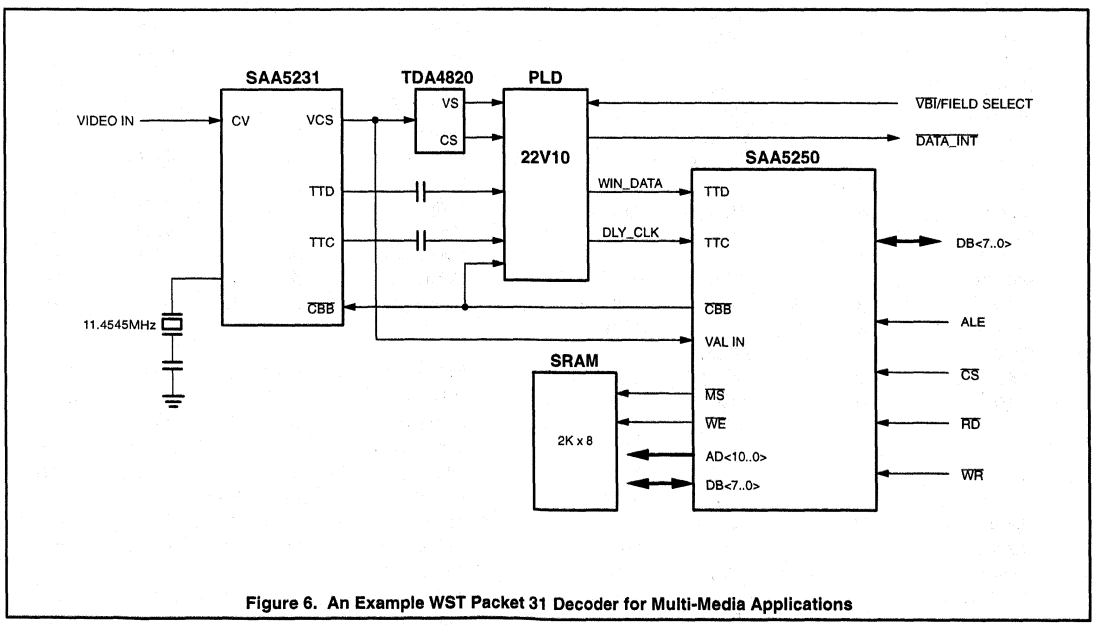


Figure 6. An Example WST Packet 31 Decoder for Multi-Media Applications

International TV systems and standards

Country/Area	VHF	UHF	System colour	channel
A				
Afganistan	B	G	PAL	CCIR
Albania	B	G	PAL	IT*
Algeria	B	(G)	PAL	CCIR
Angola	I		PAL	ANGOLA
Antigua	M		NTSC	US
Argentina	N		PAL	US
Australia	B	B	PAL	AUSTRALIA
Austria	B	G	PAL	CCIR
Azores Is.	B		PAL	CCIR, US
B				
Bahamas	M		NTSC	US*
Bahrain	B		PAL	CCIR
Bangladesh	B		PAL	CCIR
Barbados	N		NTSC	US
Belgium	B	N	PAL	CCIR
Benin	KI		SECAM	F.O.T.*
Bermuda	M		NTSC	US
Bolivia	M, N		PAL	US
Botswana	I		PAL	UK
Brazil	M	M	PAL	US
Brunei	B		PAL	CCIR
Bulgaria	D	K	SECAM	OIRT
Burkina Faso	K1		SECAM	OIRT
Burundi	K1		SECAM	?
C				
Cambodia	M		NTSC	US
Cameroon (United Rep. of)	B		PAL	?
Canada	M	M	NTSC	US
Canary Is.	B	G	PAL	CCIR
Centr. Afr. Rep.	B			CCIR
Chad	D		SECAM	?
Chile	M		NTSC	US
China	D	D	PAL	CHINA
C.I.S.	D	K	SECAM/ PAL	OIRT
Colombia	M		NTSC	US*
Congo	D		SECAM	F.O.T*
Costa Rica	M		NTSC	US
Cuba	M		NTSC	US*
Cyprus	B, B	H, G	PAL	CCIR
CzechRepublic	D	K	SECAM/ PAL	OIRT
D				
Denmark	B	G	PAL	CCIR
Diego Garcia	M		NTSC	US
Djibouti	K1		SECAM	F.O.T
Dominica (Common wealth of)	M		NTSC	?
Dominican Rep.	M	M	NTSC	US

Country/Area	VHF	UHF	System colour	channel
E				
Ecuador	M		NTSC	US*
Egypt	B		PAL	CCIR
El Salvador	M		NTSC	US*
Equatorial Guinea	B		?	CCIR
Ethopia	B		PAL	CCIR
F				
Finland	B	G	PAL	CCIR
France	E	L	SECAM	FRENCH
G				
Gabon	K1		SECAM	F.O.T
Galapagos Is.	M		NTSC	US
Gambia	(K1)			(F.O.T)
Germany	B	G	PAL	CCIR
Ghana	B		PAL	CCIR
Gibraltar	B		PAL	CCIR
Greece	B	H	SECAM	CCIR
Greenland	B		PAL	US
Guadeloupe	K1		SECAM	F.O.T
Guam	M		NTSC	US
Guatemala	M		NTSC	US
Guiana (French)	K1		SECAM	F.O.T
Guinea	K1		PAL	?
Guyana	K1		SECAM	F.O.T
H				
Haiti	M		NTSC	US*
Hawaii	M		NTSC	US
Honduras	M		NTSC	US
Hong Kong	A	I	PAL	UK
Hungary	D	K	SECAM/ PAL	OIRT
I				
Iceland	B	G	PAL	CCIR
India	B		PAL	CCIR
Indonesia	B	G	PAL	IN
Iran (Islamic Rep. of)	B		SECAM	CCIR
Iraq	B		SECAM	CCIR
Ireland	A,I	A, I	PAL	IR
Italy	B	G	PAL	IT
Ivory Coast	K1		SECAM	IC
J				
Jamaica	M		NTSC	US
Japan	M	M	NTSC	JAPAN
Johnstone Is. (American)	M		NTSC	US
Jordan	B		PAL	CCIR
K				
Kenya	B		PAL	CCIR
Korea (Dem. People's Rep.)	D		PAL	OIRT
Korea (Rep. of)	M	M	NTSC	US
Kuwait	B		PAL	CCIR

International TV systems and standards

Country/Area	VHF	UHF	System colour	channel
L				
Laos	M		PAL	
Lebanon	B		SECAM	CCIR
Lesotho	I		PAL	?
Liberia	B		PAL	CCIR
Libya	B		SECAM	CCIR
Luxembourg	G	L, C	SECAM/ PAL	CCIR*
M				
Macao	I		PAL	?
Madagascar	K1		SECAM	F.O.T.
Madeira Is.	B		PAL	CCIR
Malaysia	B		PAL	CCIR
Maldives	B		PAL	CCIR*
Mali	K1		SECAM	?
Malta	B	H	PAL	CCIR
Martinique	K1		SECAM	F.O.T.
Maruitania	B		SECAM	?
Maruitius	B		SECAM	CCIR
Mexico	M	M	NTSC	US
Micronesia	M		NTSC	US
Midway Is. (American)	M		NTSC	US
Monaco	E	L, G	SECAM/ PAL	CCIR
Mongolia	D		SECAM	OIRT
Morocco	B		SECAM	MO
Mozambique	B		PAL	?
Myarma	M		NTSC	US*
N				
Nambia	I		PAL	?
Nepal			PAL	
Netherlands	B	G	PAL	CCIR
Neth. Antilles	B	G	PAL	US
New Caledonia	K1		SECAM	F.O.T.
New Zealand	B		PAL	NZ
Nicaragua	M		NTSC	US
Niger	K1		SECAM	F.O.T.*
Nigeria	B	G	SECAM	CCIR*
Norfolk Is.	B		PAL	?
Norway	B	G	PAL	CCIR
O				
Oman	B	G	PAL	CCIR
P				
Pakistan	B		PAL	CCIR
Panama	M		NTSC	US
Papua New Ginea	B	G	PAL	?
Paraguay	N		PAL	US*
Peru	M		NTSC	US
Philippines	M	M	NTSC	US
Poland	D	K	SECAM/ PAL	OIRT
Polynesia	K1		SECAM	F.O.T.
Portugal	B	G	PAL	CCIR*
Puerto Rico	M	M	NTSC	US

CountryArea	VHF	UHF	System colour	channel
Q				
Qatar	B	G	PAL	CCIR
R				
Reunion	K1		SECAM	F.O.T.
Romania	D	K	PAL	OIRT
S				
St. Kitts & Nevis	M		NTSC	US
Saint Lucia	M		NTSC	US*
St Pierre et Miquelon	K1		SECAM	F.O.T.
St. Vincent	M		NTSC	?
Samoa (American)	M		NTSC	US
Samoa (Western)	(M)		(NTSC)	(US)
San Marino	B	G	PAL	IT
Saudi Arabia	B	G	SECAM	CCIR
Senegal	K1		SECAM	F.O.T.
Seychelles	B		PAL	?
Sierra Leone	B		PAL	CCIR
Singapore	B		PAL	CCIR
Slovak Republic	D	K	SECAM/ PAL	OIRT
Somalia	B		PAL	?
South Africa	I	I	PAL	SA
Spain	B	G	PAL	CCIR
Sri Lanka	B		PAL	CCIR
Sudan	B		PAL	CCIR
Surinam	M		NTSC	US
Swaziland	G		PAL	CCIR
Sweden	B	G	PAL	CCIR
Switzerland	B	G	PAL	CCIR
Syrian Arab Rep.	B		SECAM	CCIR
T				
Tahiti	K1		SECAM	F.O.T.
Taiwan	M		NTSC	TAIWAN
Tanzania	B	I	PAL	CCIR
Thailand	B		PAL	CCIR
Togo Rep.	K1		SECAM	F.O.T.*
Trinidad & Tobago	M	M	NTSC	US
Tunisia	B		SECAM	CCIR
Turkey	B	G	PAL	CCIR
Turks & Caicos Is.	M		NTSC	US
U				
Uganda	B		PAL	CCIR
United Arab Emirates	B	G	PAL	CCIR
United Kingdom	A	I	PAL	UK
United States of America	M	M	NTSC	US
Uruguay	N		PAL	US

International TV systems and standards

Country	VHF	UHF	System colour	channel
V				
Vatican City State			NTSC	US
Venezuela	M		SECAM/ NTSC	
Vietnam	D, M		NTSC	US
Virguin Is. (American)	M		NTSC	US
Virguin Is. (British)	M			
Y				
Yemen	B	H	PAL	CCIR
Yugoslavia	B		PAL	CCIR
Z				
Zaire	K		SECAM	F.O.T.
Zambia	B		PAL	CCIR
Zimbabwe	B		PAL	CCIR

Notes:
Abbreviations used in the Channel section are shown i the following table:

F.O.T.	French Overseas Territories
IC	Ivory Coast
IR	Ireland
IT	Italy
OIRT	Organisation International de Radiodiffusion et Television
MO	Morocco
NZ	New Zealand
SA	South Africa
UK	United Kingdom
*	Indefinite.
( )	No broadcase originating in this country; but one can listen to a broadcast from the neighboring country.
?	Details not available.
blank	No broadcast station.

International TV systems and standards

BASIC CHARACTERISTICS OF VIDEO AND SYNCHRONIZING SIGNALS

Characteristics	CCIR system designation										
	A	M	N	C	B,G	H	I	D,K	K1	L	E
Number of lines per frame	405	525	625	625	625	625	625	625	625	625	819
Number of fields per second	50	60 (59.94)	50	50	50	50	50	50	50	50	50
Line frequency f_H, Hz, and tolerances	10,125	15,750 15,734 (±0.0003%)	15,625 ±0.15%	15,625 ±0.02%	15,625 ±0.02% (±0.0001%)	15,625 ±0.02% (±0.0001%)	15,625 (±0.0001%)	15,625 ±0.02% (±0.0001%)	15,625 ±0.02% (±0.0001%)	15,625 ±0.02% (±0.0001%)	20,475
Interlace ratio	2/1	2/1	2/1	2/1	2/1	2/1	2/1	2/1	2/1	2/1	2/1
Aspect ratio	4/3	4/3	4/3	4/3	4/3	4/3	4/3	4/3	4/3	4/3	4/3
Blanking level, IRE units	0	0	0	0	0	0	0	0	0	0	0
Peak-white level	100	100	100	100	100	100	100	100	100	100	100
Sync-pulse level	–43	–40	–40	–43	–43	–43	–43	–43	–43	–43	–43
Picture-black level to blanking level (setup)	0	7.5 ±2.5	7.5 ±2.5	0	0	0	0	0–7	0 color 0–7 mono	0 color 0–7 mono	0–5
Nominal video bandwidth, MHz	3	4.2	4.2	5	5	5	5.5	6	6	6	10
Assumed display gamma	2.8	2.2	2.2	2.8	2.8	2.8	2.8	2.8	2.8	2.8	2.8

Notes: (1) Systems A, C, and E are not recommended by CCIR for adoption by countries setting up a new television service. (2) Values of horizontal line rate tolerances in parentheses are for color television. (3) In the systems using an assumed display gamma of 2.8, an overall system of gamma of 1.2 is assumed. All other systems assumed an overall transfer function of unity.

CCIR COLOR SYSTEMS CHARACTERISTICS (II)

Item	M/NTSC	M/PAL	B,G,H,PAL	I/PAL	B,D,G,H,K,K1,L/SECAM
Subcarrier frequency, MHz	3.579545 ± 10	3.575611.49 ± 10	4.433618.75 ± 5	4.433618.75 ± 1	f_{OR} = 4.406250 ± 2000 f_{OB} = 4.250000 ± 2000
f_{SC} multiple of f_H	$f_{SC} = \frac{455}{2} f_H$	$f_{SC} = \frac{909}{4} f_H$	$f_{SC} = \frac{1135}{4} + \frac{1}{25} f_H$		f_{OR} = 282 f_H f_{OB} = 272 f_H

TV sound transmission standards

TV SOUND TRANSMISSION STANDARDS

	M, N	M	M	M	B, G, H	B, G, H	I	D, K, K'	D	L	L
Intercarrier 1 (MHz)	4.5	4.5	4.5	4.5	5.5	5.5	6.0	6.5	6.5	direct AM dem. at 1st IF	direct AM dem. at 1st IF
Intercarrier 2 (MHz)	–	–	–	4.72	5.74	5.85	6.552	–	* 6.74	–	5.85
Vision modulation	negative	negative	negative	negative	negative	negative	negative	negative	negative	positive	positive
Sound modulation IC1 IC2	FM	FM	FM	FM FM	FM FM	FM digital	FM digital	FM	FM FM	AM	AM digital
Audio coding AF1	M	M MPX (FM/AM) SAP	M MPX (FM/AM)	M L + R A	M (L + R)/2 A	M1	M1	M	M (L + R)/2 A	M	M1
Audio coding AF2	–	–	–	M L – R B	M R B	L, R A, B (NICAM)	L, R A, B (NICAM)	–	M R B	–	L, R A, B (NICAM)
Country of stereo sound transmission		USA Brazil Canada Mexico Taiwan Argentina	Japan	Rep of Korea	Germany Australia Netherlands Italy Austria Switzerland Malaysia Israel Saudi Arabia	Scandinavia Belgium Spain New Zealand Singapore	UK Hong Kong		Peoples Rep. of China * 6.25 in Czech., Poland, Slovakia	France	France

OM-1 DOS API version 1.10

INTRODUCTION

The purpose of the OM-1 consortium is to promote the use of MPEG in the consumer market. One way to accomplish this is by specifying a common Applications Programming Interface (API). This API is used by various applications to control an communicate, in a uniform manner, with different vendors' MPEG hardware.

This document describes the OM-1 API which may be used to interface an MPEG decoder/display board to interactive applications such as games running under MS-DOS™. Applications which are geared towards linear playback should use the Windows API.

This API may be freely used by anyone to develop MPEG related products and is provided without licensing fees or royalties of any kind. It represents the effort of interested manufacturers, software developers, and content developers to meet the need for a widely available and public MPEG API. It is based on proposals and comments presented to the committee. Interested companies are invited to join this committee to participate in future enhancements of the API as well as future OM-1 projects.

The specification presented here is provided without warranty or guarantee of usability or merchandisability. Use of this specification does not imply licensing of intellectual property associated to ISO 1172 (MPEG-1) or any derivation of that standard.

OVERVIEW OF FEATURES

This document describes an MPEG API for DOS. It is intended to provide the basic capabilities to play back MPEG streams on a wide variety of hardware.

The API addresses the needs of both simple and sophisticated applications. It includes file handling functions, so that an application can play an MPEG stream simply by opening a file. It may also be used to implement more complex systems where:

- multiple streams are pieced together according to an event and played in real time. An example might be a game where the hero is running down a corridor, and when he gets to the end of the corridor a selection is made in real time to go left or right. The appropriate MPEG stream is played in response to the selection. The overall effect is such that the video appears to be continuous. This capability is supported by the ability to play back from buffers and the ability to set signals within the stream.
- private data from the MPEG stream is passed back to the application. An example might be close-captioning text which should accompany the audio and video. By using private data, the application developer can present the close-captioning in loose synchronization with the MPEG audio and video.

There are also facilities for reading the capabilities of the hardware, for setting the audio and video parameters of the display, and for setting callback functions that can be associated wither with a particular stream or with the driver in general.

Accessing and downloading OM-1 DOS API version 1.10

To access/download via the Internet:

```
Type: ftp.creaf.com              ;connects to Creative labs ftp site
Logon as anonymous
Password: your e-mail address
Type: cd pub/om1                 ;change to relevant directory
Type: image                      ;change transfer type to binary
Type: get file_name              ;file called om1_110.doc or om1_110.zip
Type: bye                        ;log off the ftp site
```

You now have the file on your machine.

Video CD specification

The Video CD specification (called *The White Book*) may be obtained by contacting:

Mr. B. Gall
FAX: +31 40 27 32113

The I²C-bus and how to use it

(including specifications)

1.0 THE I²C-BUS BENEFITS DESIGNERS AND MANUFACTURERS

In consumer electronics, telecommunications and industrial electronics, there are often many similarities between seemingly unrelated designs. For example, nearly every system includes:

- Some intelligent control, usually a single-chip microcontroller
- General-purpose circuits like LCD drivers, remote I/O ports, RAM, EEPROM, or data converters
- Application-oriented circuits such as digital tuning and signal processing circuits for radio and video systems, or DTMF generators for telephones with tone dialling.

To exploit these similarities to the benefit of both systems designers and equipment manufacturers, as well as to maximize hardware efficiency and circuit simplicity, Philips developed a simple bidirectional 2-wire bus for efficient inter-IC control. This bus is called the Inter IC or I²C-bus. At present, Philips' IC range includes more than 150 CMOS and bipolar I²C-bus compatible types for performing functions in all three of the previously mentioned categories. All I²C-bus compatible devices incorporate an on-chip interface which allows them to communicate directly with each other via the I²C-bus. This design concept solves the many interfacing problems encountered when designing digital control circuits.

Here are some of the features of the I²C-bus:

- Only two bus lines are required; a serial data line (SDA) and a serial clock line (SCL)
- Each device connected to the bus is software addressable by a unique address and simple master/ slave relationships exist at all times; masters can operate as master-transmitters or as master-receivers
- It's a true multi-master bus including collision detection and arbitration to prevent data corruption if two or more masters simultaneously initiate data transfer
- Serial, 8-bit oriented, bidirectional data transfers can be made at up to 100 kbit/s in the standard mode or up to 400 kbit/s in the fast mode
- On-chip filtering rejects spikes on the bus data line to preserve data integrity
- The number of ICs that can be connected to the same bus is limited only by a maximum bus capacitance of 400 pF.

Figure 1 shows two examples of I²C-bus applications.

1.1 Designer benefits

I²C-bus compatible ICs allow a system design to rapidly progress directly from a functional block diagram to a prototype. Moreover, since they 'clip' directly onto the I²C-bus without any additional external interfacing, they allow a prototype system to be modified or upgraded simply by 'clipping' or 'unclipping' ICs to or from the bus.

Here are some of the features of I²C-bus compatible ICs which are particularly attractive to designers:

- Functional blocks on the block diagram correspond with the actual ICs; designs proceed rapidly from block diagram to final schematic
- No need to design bus interfaces because the I²C-bus interface is already integrated on-chip
- Integrated addressing and data-transfer protocol allow systems to be completely software-defined
- The same IC types can often be used in many different applications
- Design-time reduces as designers quickly become familiar with the frequently used functional blocks represented by I²C-bus compatible ICs
- ICs can be added to or removed from a system without affecting any other circuits on the bus
- Fault diagnosis and debugging are simple; malfunctions can be immediately traced
- Software development time can be reduced by assembling a library of reusable software modules.

In addition to these advantages,the CMOS ICs in the I²C-bus compatible range offer designers special features which are particularly attractive for portable equipment and battery-backed systems.

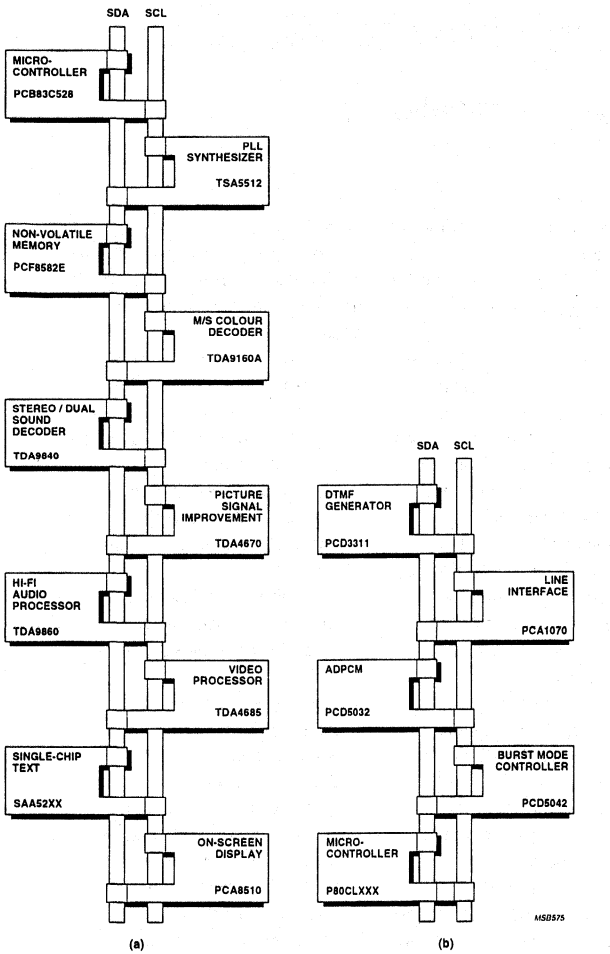


Fig.1 Two examples of I²C-bus applications (a) a high performance highly-integrated TV set (b) DECT cordless phone base-station

They all have:

- Extremely low current consumption
- High noise immunity
- Wide supply voltage range
- Wide operating temperature range.

1.2 Manufacturer benefits

I²C-bus compatible ICs don't only assist designers, they also give a wide range of benefits to equipment manufacturers because:

- The simple 2-wire serial I²C-bus minimizes interconnections so ICs have fewer pins and there are not so many PCB tracks; result - smaller and less expensive PCBs
- The completely integrated I²C-bus protocol eliminates the need for address decoders and other 'glue logic'
- The multi-master capability of the I²C-bus allows rapid testing and alignment of end-user equipment via external connections to an assembly-line computer
- The availability of I²C-bus compatible ICs in SO (small outline), VSO (very small outline) as well as DIL packages reduces space requirements even more.

These are just some of the benefits. In addition, I²C-bus compatible ICs increase system design flexibility by allowing simple construction of equipment variants and easy upgrading to keep designs up-to-date. In this way, an entire family of equipment can be developed around a basic model. Upgrades for new equipment, or enhanced-feature models (i.e. extended memory, remote control, etc.) can then be produced simply by clipping the appropriate ICs onto the bus. If a larger ROM is needed, it's simply a matter of selecting a micro-controller with a larger ROM from our comprehensive range. As new ICs supersede older ones, it's easy to add new features to equipment or to increase its performance by simply unclipping the outdated IC from the bus and clipping on its successor.

1.3 The ACCESS.bus

Another attractive feature of the I²C-bus for designers and manufacturers is that its simple 2-wire nature and capability of software addressing make it an ideal platform for the ACCESS.bus (Fig.2). This is a lower-cost alternative for an RS-232C interface for connecting peripherals to a host computer via a simple 4-pin connector (see Section 19).

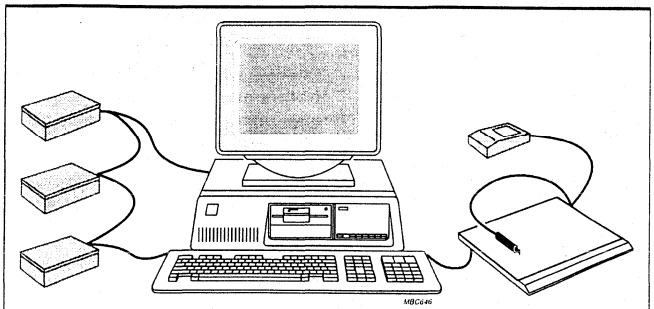


Fig.2 The ACCESS.bus – a low-cost alternative to an RS-232C interface

2.0 INTRODUCTION TO THE I²C-BUS SPECIFICATION

For 8-bit digital control applications, such as those requiring microcontrollers, certain design criteria can be established:

- A complete system usually consists of at least one microcontroller and other peripheral devices such as memories and I/O expanders
- The cost of connecting the various devices within the system must be minimized
- A system that performs a control function doesn't require high-speed data transfer
- Overall efficiency depends on the devices chosen and the nature of the interconnecting bus structure.

In order to produce a system to satisfy these criteria, a serial bus structure is needed. Although serial buses don't have the throughput capability of parallel buses, they do require less wiring and fewer IC connecting pins. However, a bus is not merely an interconnecting wire, it embodies all the formats and procedures for communication within the system.

Devices communicating with each other on a serial bus must have some form of protocol which avoids all possibilities of confusion, data loss and blockage of information. Fast devices must be able to communicate with slow devices. The system must not be dependent on the devices connected to it, otherwise modifications or improvements would be impossible. A procedure has also to be devised to decide which device will be in control of the bus and when. And, if different devices with different clock speeds are connected to the bus, the bus clock source must be defined. All these criteria are involved in the specification of the I²C-bus.

3.0 THE I²C-BUS CONCEPT

The I²C-bus supports any IC fabrication process (NMOS, CMOS, bipolar). Two wires, serial data (SDA) and serial clock (SCL), carry information between the devices connected to the bus. Each device is recognised by a unique address - whether it's a microcontroller, LCD driver, memory or keyboard interface - and can operate as either a transmitter or receiver, depending on the function of the device. Obviously an LCD driver is only a receiver, whereas a memory can both receive and transmit data. In addition to transmitters and receivers, devices can also be considered as masters or slaves when performing data transfers (see Table 1). A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

The I²C-bus is a multi-master bus. This means that more than one device capable of controlling the bus can be connected to it. As masters are usually micro-controllers, let's consider the case of a data transfer between two microcontrollers connected to the I²C-bus (Fig.3). This highlights the master-slave and receiver-transmitter relationships to be found on the I²C-bus. It should be noted that these relationships are not permanent, but only depend

Table 1 Definition of I²C-bus terminology

Term	Description
Transmitter	The device which sends the data to the bus
Receiver	The device which receives the data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by a master
Multi-master	More than one master can attempt to control the bus at the same time without corrupting the message
Arbitration	Procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
Synchronization	Procedure to synchronize the clock signals of two or more devices

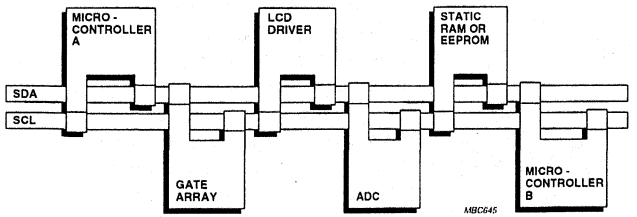


Fig.3 Example of an I²C-bus configuration using two microcontrollers

on the direction of data transfer at that time. The transfer of data would proceed as follows:

1) Suppose microcontroller A wants to send information to microcontroller B:

- microcontroller A (master), addresses microcontroller B (slave)
- microcontroller A (master-transmitter), sends data to microcontroller B (slave-receiver)
- microcontroller A terminates the transfer.

2) If microcontroller A wants to receive information from microcontroller B:

- microcontroller A (master) addresses microcontroller B (slave)
- microcontroller A (master-receiver) receives data from microcontroller B (slave-transmitter)
- microcontroller A terminates the transfer.

Even in this case, the master (microcontroller A) generates the timing and terminates the transfer.

The possibility of connecting more than one microcontroller to the I²C-bus means that more than one master could try to initiate a data transfer at the same time. To avoid the chaos that might ensue from such an event - an arbitration procedure has been developed. This procedure relies on the wired-AND connection of all I²C interfaces to the I²C-bus.

If two or more masters try to put information onto the bus, the first to produce a 'one' when the other produces a 'zero' will lose the arbitration. The clock signals during arbitration are a synchronized combination of the clocks generated by the masters using the wired-AND connection to the SCL line (for more detailed information concerning arbitration see Section 7.0).

Generation of clock signals on the I²C-bus is always the responsibility of master devices; each master generates its own clock signals when transferring data on the bus. Bus clock signals from a master can only be altered when they are stretched by a slow-slave device holding-down the clock line, or by another master when arbitration occurs.

4.0 GENERAL CHARACTERISTICS

Both SDA and SCL are bidirectional lines, connected to a positive supply voltage via a pull-up resistor (see Fig.4). When the bus is free, both lines are HIGH. The output stages of devices connected to the bus must have an open-drain or open-collector in order to perform the wired-AND function. Data on the I²C-bus can be transferred at a rate up to 100 kbit/s in the standard-mode, or up to 400 kbit/s in the fast-mode. The number of interfaces connected to the bus is solely dependent on the bus capacitance limit of 400 pF.

5.0 BIT TRANSFER

Due to the variety of different technology devices (CMOS, NMOS, bipolar) which can be connected to the I²C-bus, the levels of the logical '0' (LOW) and '1' (HIGH) are not fixed and depend on the associated level of V_{DD} (see Section 15.0 for Electrical Specifications). One

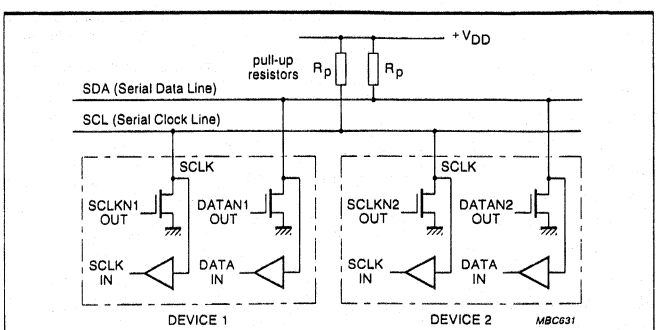


Fig.4 Connection of I²C-bus devices to the I²C-bus

clock pulse is generated for each data bit transferred.

5.1 Data validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW (see Fig.5).

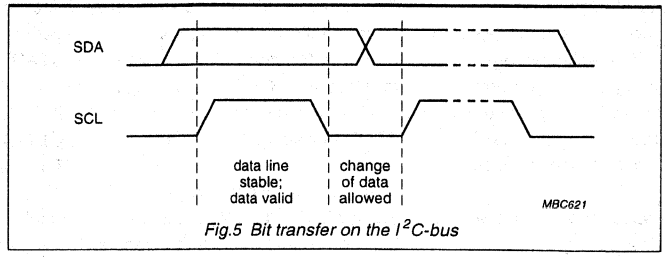


Fig.5 Bit transfer on the I²C-bus

5.2 START and STOP conditions

Within the procedure of the I²C-bus, unique situations arise which are defined as START and STOP conditions (see Fig.6).

A HIGH to LOW transition on the SDA line while SCL is HIGH is one such unique case. This situation indicates a START condition.

A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition. This bus free situation is specified in Section 15.0.

Detection of START and STOP conditions by devices connected to the bus is easy if they incorporate the necessary interfacing hardware. However, microcontrollers with no such interface have to sample the SDA line at least twice per clock period in order to sense the transition.

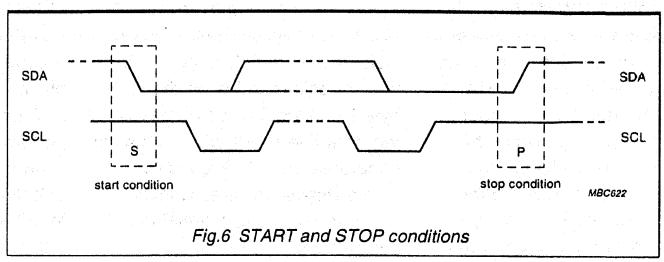


Fig.6 START and STOP conditions

6.0 TRANSFERRING DATA

6.1 Byte format

Every byte put on the SDA line must be 8-bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first (Fig.7). If a receiver can't receive another complete byte of data until it has performed some other function, for example servicing an internal interrupt, it can hold the clock line SCL LOW to force the transmitter into a wait state. Data transfer then continues when the receiver is ready for another byte of data and releases clock line SCL.

In some cases, it's permitted to use a different format from the I²C-bus format (for CBUS compatible devices for example). A message which starts with such an address can be terminated by generation of a STOP condition, even during the transmission of a byte. In this case, no acknowledge is generated (see Section 9.1.3).

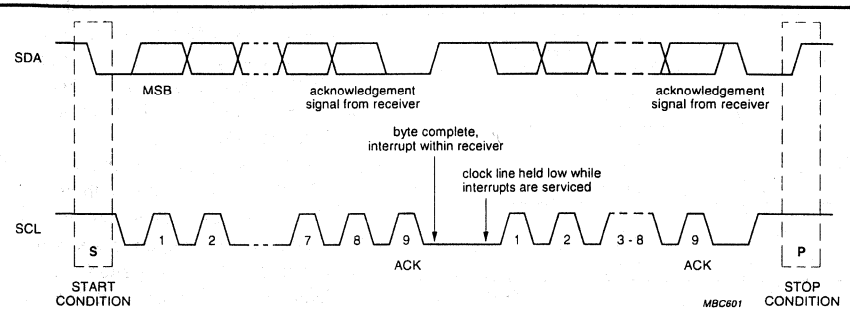


Fig.7 Data transfer on the I²C-bus

6.2 Acknowledge

Data transfer with acknowledge is obligatory. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse.

The receiver must pull down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse (Fig.8). Of course, set-up and hold times (specified in Section 15) must also be taken into account.

Usually, a receiver which has been addressed is obliged to generate an acknowledge after each byte has been received, except when the message starts with a CBUS address (see Section 9.1.3).

When a slave-receiver doesn't acknowledge the slave address (for example, it's unable to receive because it's performing some real-time function), the data line must be left HIGH by the slave. The master can then generate a STOP condition to abort the transfer.

If a slave-receiver does acknowledge the slave address but, some time later in the transfer cannot receive any more data bytes, the master must again abort the transfer. This is indicated by the slave generating the not acknowledge on the first byte to follow. The slave leaves the data line HIGH and the master generates the STOP condition.

If a master-receiver is involved in a transfer, it must signal the end of data to the slave-transmitter by not generating an acknowledge on the last byte that was clocked out of the slave. The slave-transmitter must release the data line to allow the master to generate a STOP or repeated START condition.

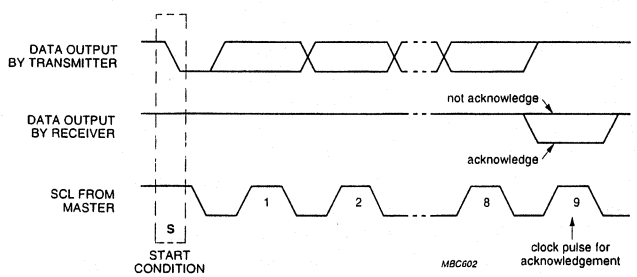


Fig.8 Acknowledge on the I²C-bus

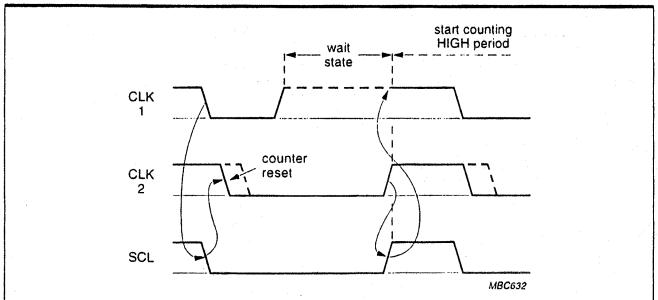


Fig.9 Clock synchronization during the arbitration procedure

7.0 ARBITRATION AND CLOCK GENERATION

7.1 Synchronization

All masters generate their own clock on the SCL line to transfer messages on the I²C-bus. Data is only valid during the HIGH period of the clock. A defined clock is therefore needed for the bit-by-bit arbitration procedure to take place.

Clock synchronization is performed using the wired-AND connection of I²C interfaces to the SCL line. This means that a HIGH to LOW transition on the SCL line will cause the devices concerned to start counting off their LOW period and, once a device clock has gone LOW, it will hold the SCL line in that state until the clock HIGH state is reached (Fig.9). However, the LOW to HIGH transition of this clock may not change the state of the SCL line if another clock is still within its LOW period. The SCL line will therefore be held LOW by the device with the longest LOW period. Devices with shorter LOW periods enter a HIGH wait-state during this time.

When all devices concerned have counted off their LOW period, the clock line will be released and go HIGH. There will then be no difference between the device clocks and the state of the SCL line, and all the devices will start counting their HIGH periods. The first device to complete its HIGH period will again pull the SCL line LOW.

In this way, a synchronized SCL clock is generated with its LOW period determined by the device with the longest clock LOW period, and its HIGH period determined by the one with the shortest clock HIGH period.

7.2 Arbitration

A master may start a transfer only if the bus is free. Two or more masters may generate a START condition within the minimum hold time ($t_{HD;STA}$) of the START condition which results in a defined START condition to the bus.

Arbitration takes place on the SDA line, while the SCL line is at the HIGH level, in such a way that the master which transmits a HIGH level, while another master is transmitting a LOW level will switch off its DATA output stage because the level on the bus doesn't correspond to its own level.

Arbitration can continue for many bits. Its first stage is comparison of the address bits (addressing information is in Sections 9.0 and 13.0). If the masters are each trying to address the same device, arbitration continues with comparison of the data. Because address and data information on the I²C-bus is used for arbitration, no information is lost during this process.

A master which loses the arbitration can generate clock pulses until the end of the byte in which it loses the arbitration.

If a master also incorporates a slave function and it loses arbitration during the addressing stage, it's possible that the winning master is trying to address it. The losing master must therefore switch over immediately to its slave-receiver mode.

Figure 10 shows the arbitration procedure for two masters. Of course, more may be involved (depending on how many masters are connected to the bus). The moment there is a difference between the internal data level of the master generating DATA 1 and the actual level on the SDA line, its data output is switched off, which means that a HIGH output level is then connected to the bus. This will not affect the data transfer initiated by the winning master.

Since control of the I²C-bus is decided solely on the address and data sent by competing masters, there is no central master, nor any order of priority on the bus.

Special attention must be paid if, during a serial transfer, the arbitration procedure is still in progress at the moment when a repeated START condition or a STOP condition is transmitted to the I²C-bus. If it's possible for such a situation to occur, the masters involved must send this repeated START condition or STOP condition at the same position in the format frame. In other words, arbitration isn't allowed between:

- A repeated START condition and a data bit
- A STOP condition and a data bit
- A repeated START condition and a STOP condition.

7.3 Use of the clock synchronizing mechanism as a handshake

In addition to being used during the arbitration procedure, the clock synchronization mechanism can be used to enable receivers to cope with fast data transfers, on either a byte level or a bit level.

On the byte level, a device may be able to receive bytes of data at a fast rate, but needs more time to store a received byte or prepare another byte to be transmitted. Slaves can then hold the SCL line LOW after reception and acknowledgement of a byte to force the master into a wait state until the slave is ready for the next byte transfer in a type of handshake procedure.

On the bit level, a device such as a microcontroller without, or with only a limited hardware I²C interface on-chip can slow down the bus clock by extending each clock LOW period. The speed of any master is thereby adapted to the internal operating rate of this device.

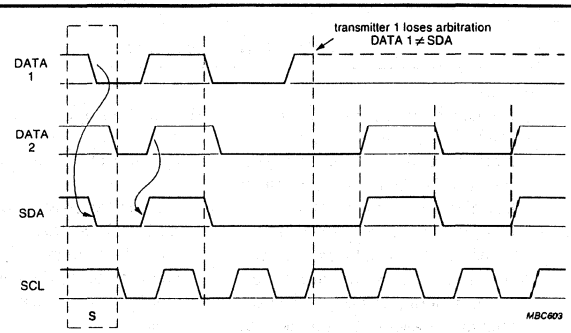


Fig.10 Arbitration procedure of two masters

8.0 FORMATS WITH 7-BIT ADDRESSES

Data transfers follow the format shown in Fig.11. After the START condition (S), a slave address is sent. This address is 7 bits long followed by an eighth bit which is a data direction bit (R/$\overline{W}$) - a 'zero' indicates a transmission (WRITE), a 'one' indicates a request for data (READ). A data transfer is always terminated by a STOP condition (P) generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated START condition (Sr) and address another slave without first generating a STOP condition. Various combinations of read/write formats are then possible within such a transfer.

Possible data transfer formats are:

- **Master-transmitter transmits to slave-receiver. The transfer direction is not changed (Fig.12)**
- **Master reads slave immediately after first byte (Fig.13).** At the moment of the first acknowledge, the master-transmitter becomes a master-receiver and the slave-receiver becomes a slave-transmitter. This acknowledge is still generated by the slave. The STOP condition is generated by the master
- **Combined format (Fig.14).** During a change of direction within a transfer, the START condition and the slave address are both repeated, but with the R/$\overline{W}$ bit reversed. If a master receiver sends a repeated START condition, it has previously sent a not acknowledge ($\overline{A}$).

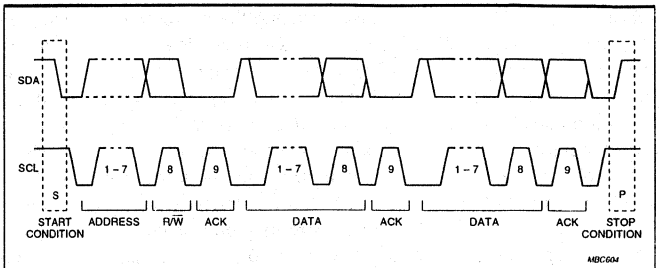


Fig.11 A complete data transfer

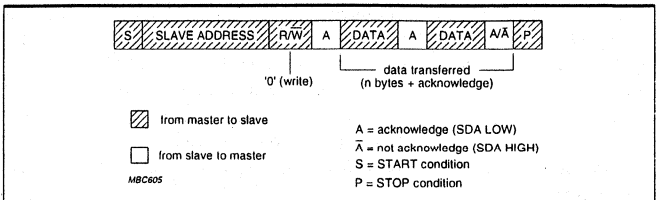


Fig.12 A master-transmitter addresses a slave receiver with a 7-bit address. The transfer direction is not changed

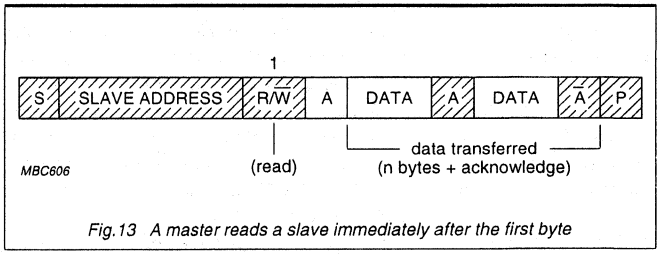


Fig.13 A master reads a slave immediately after the first byte

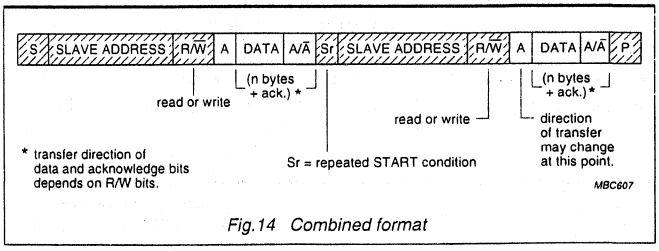


Fig.14 Combined format

NOTES:

1) Combined formats can be used, for example, to control a serial memory. During the first data byte, the internal memory location has to be written. After the START condition and slave address is repeated, data can be transferred.
2) All decisions on auto-increment or decrement of previously accessed memory locations etc. are taken by the designer of the device.
3) Each byte is followed by an acknowledgement bit as indicated by the A or $\overline{A}$ blocks in the sequence.
4) I²C-bus compatible devices must reset their bus logic on receipt of a START or repeated START condition such that they all anticipate the sending of a slave address.

9.0 7-BIT ADDRESSING (see Section 13 for 10-bit addressing)

The addressing procedure for the I²C-bus is such that the first byte after the START condition usually determines which slave will be selected by the master. The exception is the 'general call' address which can address all devices. When this address is used, all devices should, in theory, respond with an acknowledge. However, devices can be made to ignore this address. The second byte of the general call address then defines the action to be taken. This procedure is explained in more detail in Section 9.1.1.

9.1 Definition of bits in the first byte

The first seven bits of the first byte make up the slave address (Fig.15). The eighth bit is the LSB (least significant bit). It determines the direction of the message. A 'zero' in the least significant position of the first byte means that the master will write information to a selected slave. A 'one' in this position means that the master will read information from the slave.

When an address is sent, each device in a system compares the first seven bits after the START condition with its address. If they match, the device considers itself addressed by the master as a slave-receiver or slave-transmitter, depending on the R/$\overline{W}$ bit.

A slave address can be made-up of a fixed and a programmable part. Since it's likely that there will be several identical devices in a system, the programmable part of the slave address enables the maximum possible number of such devices to be connected to the I²C-bus. The number of programmable address bits of a device depends on the number of pins available. For example, if a device has 4 fixed and 3 programmable address bits, a total of 8 identical devices can be connected to the same bus.

The I²C-bus committee coordinates allocation of I²C addresses. Further information can be obtained from the Philips representatives listed on the back cover. Two groups of eight addresses (0000XXX and 1111XXX) are reserved for the purposes shown in Table 2. The bit combination 11110XX of the slave address is reserved for 10-bit addressing (see Section 13).

Table 2 Definition of bits in the first byte

Slave address	R/$\overline{W}$ bit	Description
0000 000	0	General call address
0000 000	1	START byte
0000 001	X	CBUS address
0000 010	X	Address reserved for different bus format
0000 011	X	Reserved for future purposes
0000 1XX	X	
1111 1XX	X	
1111 0XX	X	10-bit slave addressing

NOTES:

1) No device is allowed to acknowledge at the reception of the START byte.
2) The CBUS address has been reserved to enable the inter-mixing of CBUS compatible and I²C-bus compatible devices in the same system. I²C-bus compatible devices are not allowed to respond on reception of this address.
3) The address reserved for a different bus format is included to enable I²C and other protocols to be mixed. Only I²C-bus compatible devices that can work with such formats and protocols are allowed to respond to this address.

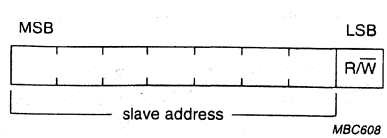


Fig.15 The first byte after the START procedure

9.1.1 General call address

The general call address is for addressing every device connected to the I²C-bus. However, if a device doesn't need any of the data supplied within the general call structure, it can ignore this address by not issuing an acknowledgement. If a device does require data from a general call address, it will acknowledge this address and behave as a slave- receiver. The second and following bytes will be acknowledged by every slave-receiver capable of handling this data. A slave which cannot process one of these bytes must ignore it by not acknowledging. The meaning of the general call address is always specified in the second byte (Fig.16).

There are two cases to consider:

- When the least significant bit B is a 'zero'
- When the least significant bit B is a 'one'.

When bit B is a 'zero'; the second byte has the following definition:

- 00000110 (H'06'). Reset and write programmable part of slave address by hardware. On receiving this 2-byte sequence, all devices designed to respond to the general call address will reset and take in the programmable part of their address. Precautions have to be taken to ensure that a device is not pulling down the SDA or SCL line after applying the supply voltage, since these low levels would block the bus
- 00000100 (H'04'). Write programmable part of slave address by hardware. All devices which define the programmable part of their address by hardware (and which respond to the general call address) will latch this programmable part at the reception of this two byte sequence. The device will not reset.
- 00000000 (H'00'). This code is not allowed to be used as the second byte.

Sequences of programming procedure are published in the appropriate device data sheets.

The remaining codes have not been fixed and devices must ignore them.

When bit B is a 'one'; the 2-byte sequence is a 'hardware general call'. This means that the sequence is transmitted by a hardware master device, such as a keyboard scanner, which cannot be programmed to transmit a desired slave address. Since a hardware master doesn't know in advance to which device the message has to be transferred, it can only generate this hardware general call and its own address - identifying itself to the system (Fig.17).

The seven bits remaining in the second byte contain the address of the hardware master. This address is recognised by an intelligent device (e.g. a microcontroller) connected to the bus which will then direct the information from the hardware master. If the hardware master can also act as a slave, the slave address is identical to the master address.

In some systems, an alternative could be that the hardware master transmitter is set in the slave-

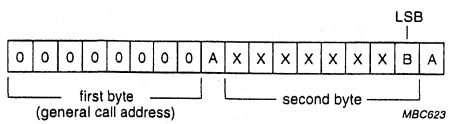


Fig.16 General call address format

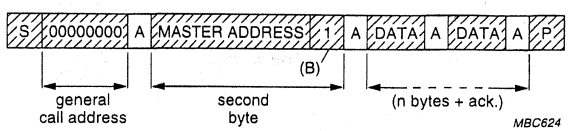


Fig.17 Data transfer from a hardware master-transmitter

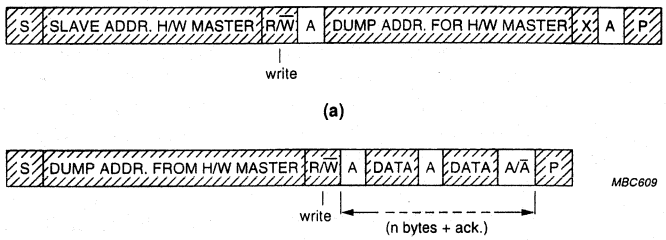


Fig.18 Data transfer by a hardware-transmitter capable of dumping data directly to slave devices (a) Configuring master sends dump address to hardware master (b) Hardware master dumps data to selected slave

receiver mode after the system reset. In this way, a system configuring master can tell the hardware master-transmitter (which is now in slave-receiver mode) to which address data must be sent (Fig.18). After this programming procedure, the hardware master remains in the master-transmitter mode.

9.1.2 START byte

Microcontrollers can be connected to the I²C-bus in two ways. A microcontroller with an on-chip hardware I²C-bus interface can be programmed to be only interrupted by requests from the bus. When the device doesn't have such an interface, it must constantly monitor the bus via software. Obviously, the more times the microcontroller monitors, or polls the bus, the less time it can spend carrying out its intended function. There is therefore a speed difference between fast hardware devices and a relatively slow microcontroller which relies on software polling.

In this case, data transfer can be preceded by a start procedure which is much longer than normal (Fig.19). The start procedure consists of:

- A START condition (S)
- A START byte (00000001)
- An acknowledge clock pulse (ACK)
- A repeated START condition (Sr).

After the START condition S has been transmitted by a master which requires bus access, the START byte (00000001) is transmitted. Another microcontroller can therefore sample the SDA line at a low sampling rate until one of the seven zeros in the START byte is detected. After detection of this LOW level on the SDA line, the microcontroller can switch to a higher sampling rate to find the repeated START condition Sr which is then used for synchronization.

A hardware receiver will reset on receipt of the repeated START condition Sr and will therefore ignore the START byte.

An acknowledge-related clock pulse is generated after the START byte. This is present only to conform with the byte handling format used on the bus. No device is allowed to acknowledge the START byte.

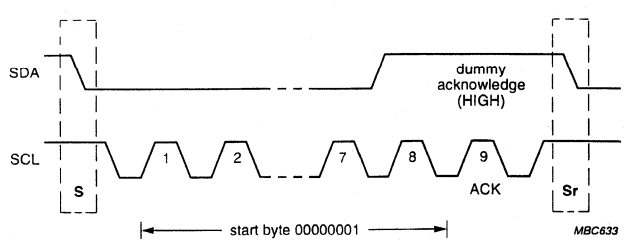


Fig.19 START byte procedure

9.1.3 CBUS compatibility

CBUS receivers can be connected to the I²C-bus. However, a third bus line called DLEN must then be connected and the acknowledge bit omitted. Normally, I²C transmissions are sequences of 8-bit bytes; CBUS compatible devices have different formats.

In a mixed bus structure, I²C-bus devices must not respond to the CBUS message. For this reason, a special CBUS address (0000001X) to which no I²C-bus compatible device will respond, has been reserved. After transmission of the CBUS address, the DLEN line can be made active and a CBUS-format transmission (Fig.20) sent. After the STOP condition, all devices are again ready to accept data.

Master-transmitters can send CBUS formats after sending the CBUS address. The transmission is ended by a STOP condition, recognised by all devices.

NOTE: If the CBUS configuration is known, and expansion with CBUS compatible devices isn't foreseen, the designer is allowed to adapt the hold time to the specific requirements of the device(s) used.

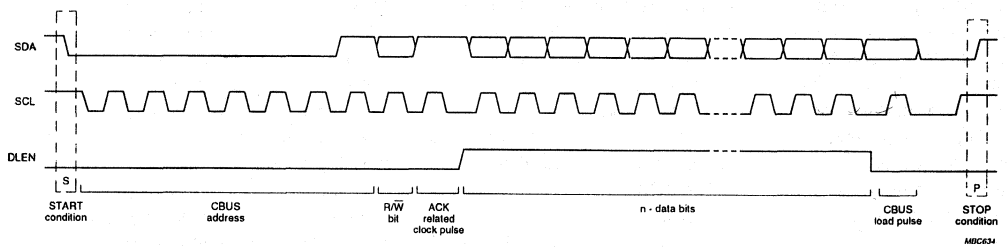


Fig.20 Data format of transmissions with CBUS transmitter/receiver

10.0 ELECTRICAL CHARACTERISTICS FOR I²C-BUS DEVICES

The electrical specifications for the I/Os of I²C-bus devices and the characteristics of the bus lines connected to them are given in Tables 3 and 4 in Section 15.

I²C-bus devices with fixed input levels of 1.5 V and 3 V can each have their own appropriate supply voltage. Pull-up resistors must be connected to a 5 V ± 10% supply (Fig.21). I²C-bus devices with input levels related to V_{DD} must have one common supply line to which the pull-up resistor is also connected (Fig.22).

When devices with fixed input levels are mixed with devices with input levels related to V_{DD}, the latter devices must be connected to one common supply line of 5 V ± 10% and must have pull-up resistors connected to their SDA and SCL pins as shown in Fig.23.

Input levels are defined in such a way that:

- The noise margin on the LOW level is 0.1 V_{DD}
- The noise margin on the HIGH level is 0.2 V_{DD}
- As shown in Fig.24, series resistors (R_S) of e.g. 300 Ω can be used for protection against high-voltage spikes on the SDA and SCL lines (due to flash-over of a TV picture tube, for example).

10.1 Maximum and minimum values of resistors R_p and R_s

For standard-mode I²C-bus devices, the values of resistors R_p and R_s in Fig.24 depend on the following parameters:

- Supply voltage
- Bus capacitance
- Number of connected devices (input current + leakage current).

The supply voltage limits the minimum value of resistor R_p due

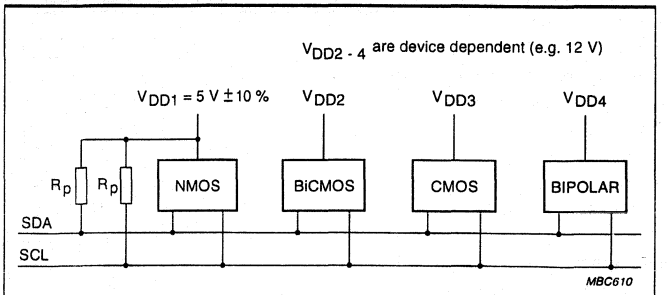


Fig.21 Fixed input level devices connected to the I²C-bus

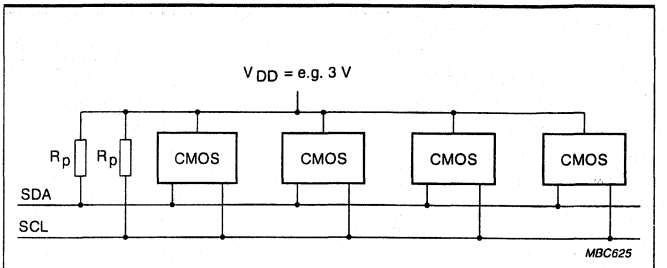


Fig.22 Devices with wide supply voltage range connected to the I²C-bus

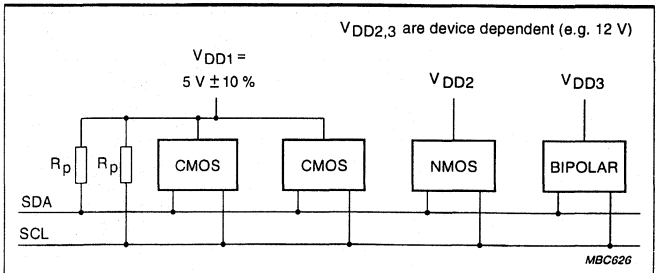


Fig.23 Devices with input levels related to V_{DD} (supply V_{DD1}) mixed with fixed input level devices (supply $V_{DD2,3}$) on the I²C-bus

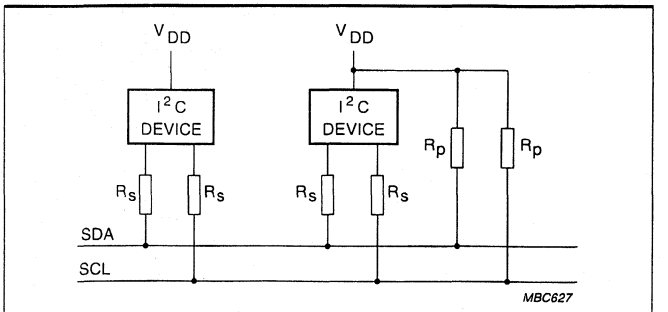


Fig.24 Series resistors (R_s) for protection against high-voltage spikes

to the specified minimum sink current of 3 mA at V_{OLmax} = 0.4 V for the output stages. V_{DD} as a function of $R_{p\ min}$ is shown in Fig.25. The desired noise margin of $0.1V_{DD}$ for the LOW level, limits the maximum value of R_s. $R_{s\ max}$ as a function of R_p is shown in Fig.26.

The bus capacitance is the total capacitance of wire, connections and pins. This capacitance limits the maximum value of R_p due to the specified rise time. Fig.27 shows $R_{p\ max}$ as a function of bus capacitance.

The maximum HIGH level input current of each input/output connection has a specified maximum value of 10 μA. Due to the desired noise margin of $0.2V_{DD}$ for the HIGH level, this input current limits the maximum value of R_p. This limit depends on V_{DD}. The total HIGH level input current is shown as a function of $R_{p\ max}$ in Fig.28.

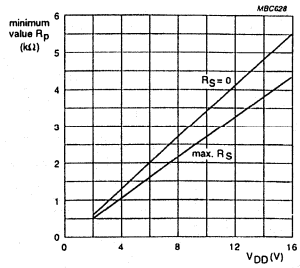


Fig.25 Minimum value of R_p as a function of supply voltage with the value of R_s as a parameter

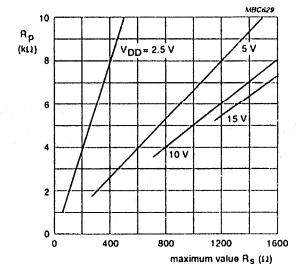


Fig.26 Maximum value of R_s as a function of the value of R_p with supply voltage as a parameter

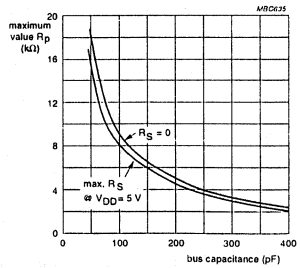


Fig.27 Maximum value of R_p as a function of bus capacitance for a standard-mode I²C-bus

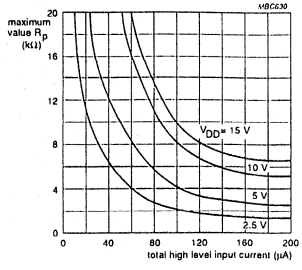


Fig.28 Total HIGH level input current as a function of the maximum value of R_p with supply voltage as a parameter

11.0 EXTENSIONS TO THE I²C-BUS SPECIFICATION

The I²C-bus with a data transfer rate of up to 100 kbit/s and 7-bit addressing has now been in existence for more than ten years with an unchanged specification. The concept is accepted world-wide as a de facto standard and hundreds of different types of I²C-bus compatible ICs are available from Philips and other suppliers. The I²C-bus specification is now extended with the following two features:

- A **fast-mode** which allows a fourfold increase of the bit rate to 0 to 400 kbit/s
- **10-bit addressing** which allows the use of up to 1024 additional addresses.

There are two reasons for these extensions to the I²C-bus specification:

- New applications will need to transfer a larger amount of serial data and will therefore demand a higher bit rate than 100 kbit/s. Improved IC manufacturing technology now allows a fourfold speed increase without increasing the manufacturing cost of the interface circuitry
- Most of the 112 addresses available with the 7-bit addressing scheme have been issued more than once. To prevent problems with the allocation of slave addresses for new devices, it is desirable to have more address combinations. About a tenfold increase of the number of available addresses is obtained with the new 10-bit addressing.

All new devices with an I²C-bus interface are provided with the fast-mode. Preferably, they should be able to receive and/or transmit at 400 kbit/s. The minimum requirement is that they can synchronize with a 400 kbit/s transfer; they can then prolong the LOW period of the SCL signal to slow down the transfer. Fast-mode devices must be downward-compatible which means that they must still be able to communicate with 0 to 100 kbit/s devices in a 0 to 100 kbit/s I²C-bus system.

Obviously, devices with a 0 to 100 kbit/s I²C-bus interface cannot be incorporated in a fast-mode I²C-bus system because, since they cannot follow the higher transfer rate, unpredictable states of these devices would occur.

Slave devices with a fast-mode I²C-bus interface can have a 7-bit or a 10-bit slave address. However, a 7-bit address is preferred because it is the cheapest solution in hardware and it results in the shortest message length. Devices with 7-bit and 10-bit addresses can be mixed in the same I²C-bus system regardless of whether it is a 0 to 100 kbit/s standard-mode system or a 0 to 400 kbit/s fast-mode system. Both existing and future masters can generate either 7-bit or 10-bit addresses.

12.0 FAST-MODE

In the fast-mode of the I²C-bus, the protocol, format, logic levels and maximum capacitive load for the SDA and SCL lines quoted in the previous I²C-bus specification are unchanged. Changes to the previous I²C-bus specification are:

- The maximum bit rate is increased to 400 kbit/s
- Timing of the serial data (SDA) and serial clock (SCL) signals has been adapted. There is no need for compatibility with other bus systems such as CBUS because they cannot operate at the increased bit rate
- The inputs of fast-mode devices must incorporate spike suppression and a Schmitt trigger at the SDA and SCL inputs
- The output buffers of fast-mode devices must incorporate slope control of the falling edges of the SDA and SCL signals
- If the power supply to a fast-mode device is switched off, the SDA and SCL I/O pins must be floating so that they don't obstruct the bus lines
- The external pull-up devices connected to the bus lines must be adapted to accommodate the shorter maximum permissible rise time for the fast-mode I²C-bus. For bus loads up to 200 pF, the pull-up device for each bus line can be a resistor; for bus loads between 200 pF and 400 pF, the pull-up device can be a current source (3 mA max.) or a switched resistor circuit as shown in Fig.37.

13.0 10-BIT ADDRESSING

The 10-bit addressing does not change the format in the I²C-bus specification. Using 10 bits for addressing exploits the reserved combination 1111XXX for the first seven bits of the first byte following a START (S) or repeated START (Sr) condition as explained in Section 9.1. The 10-bit addressing does not affect the existing 7-bit addressing. Devices with 7-bit and 10-bit addresses can be connected to the same I²C-bus, and both 7-bit and 10-bit addressing can be used in a standard-mode system (up to 100 kbit/s) or a fast-mode system (up to 400 kbit/s).

Although there are eight possible combinations of the reserved address bits 1111XXX, only the four combinations 11110XX are used for 10-bit addressing. The remaining four combinations 11111XX are reserved for future I²C-bus enhancements.

13.1 Definition of bits in the first two bytes

The 10-bit slave address is formed from the first two bytes following a START condition (S) or a repeated START condition (Sr).

The first seven bits of the first byte are the combination 11110XX of which the last two bits (XX) are the two most-significant bits (MSBs) of the 10-bit address; the eighth bit of the first byte is the R/$\overline{W}$ bit that determines the direction of the message. A 'zero' in the least significant position of the first byte means that the master will write information to a selected slave. A 'one' in this position means that the master will read information from the slave.

If the R/$\overline{W}$ bit is 'zero', then the second byte contains the remaining 8 bits (XXXXXXXX) of the 10-bit address. If the R/$\overline{W}$ bit is 'one', then the next byte contains data transmitted from a slave to a master.

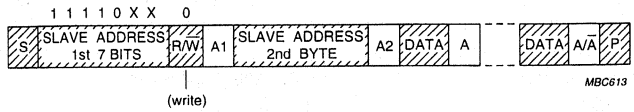


Fig.29 A master-transmitter addresses a slave-receiver with a 10-bit address

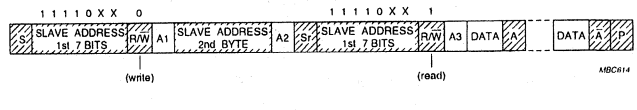


Fig.30 A master-receiver addresses a slave-transmitter with a 10-bit address

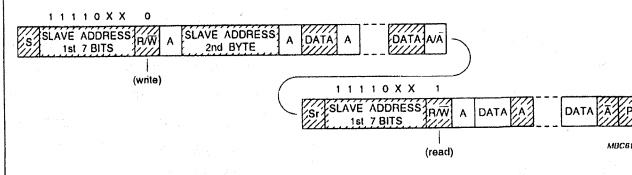


Fig.31 Combined format. A master addresses a slave with a 10-bit address, then transmits data to this slave and reads data from this slave

13.2 Formats with 10-bit addresses

Various combinations of read/write formats are possible within a transfer that includes 10-bit addressing. Possible data transfer formats are:

- **Master-transmitter transmits to slave-receiver with a 10-bit slave address. The transfer direction is not changed (Fig.29).** When a 10-bit address follows a START condition, each slave compares the first seven bits of the first byte of the slave address (11110XX) with its own address and tests if the eighth bit (R/$\overline{W}$ direction bit) is 0. It is possible that more than one device will find a match and generate an acknowledge (A1). All slaves that found a match will compare the eight bits of the second byte of the slave address (XXXXXXXX) with their own addresses, but only one slave will find a match and generate an acknowledge (A2). The matching slave will remain addressed by the master until it receives a STOP condition (P) or a repeated START condition (Sr) followed by a different slave address
- **Master-receiver reads slave-transmitter with a 10-bit slave address. The transfer direction is changed after the second R/$\overline{W}$ bit (Fig.30).** Up to and including acknowledge bit A2, the procedure is the same as that described for a master-transmitter addressing a

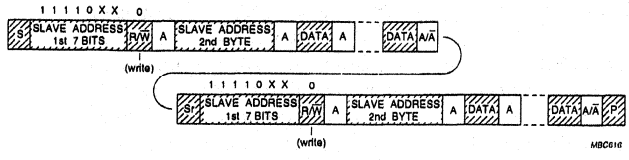


Fig.32 Combined format. A master transmits data to two slaves, both with 10-bit addresses

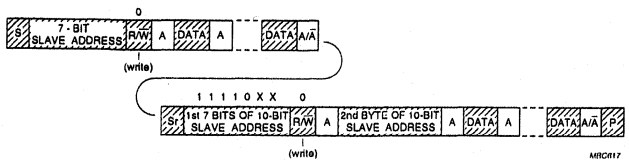


Fig.33 Combined format. A master transmits data to two slaves, one with a 7-bit address, and one with a 10-bit address

slave-receiver. After the repeated START condition (Sr), a matching slave remembers that it was addressed before. This slave then checks if the first seven bits of the first byte of the slave address following Sr are the same as they were after the START condition (S), and tests if the eighth (R/$\overline{W}$) bit is 1. If there is a match, the slave considers that it has been addressed as a transmitter and generates acknowledge A3.

The slave-transmitter remains addressed until it receives a STOP condition (P) or until it receives another repeated START condition (Sr) followed by a different slave address. After a repeated START condition (Sr), all the other slave devices will also compare the first seven bits of the first byte of the slave address (11110XX) with their own addresses and test the eighth (R/$\overline{W}$) bit. However, none of them will be addressed because R/$\overline{W}$ = 1 (for 10-bit devices), or the 11110XX slave address (for 7-bit devices) does not match)

- **Combined format. A master transmits data to a slave and then reads data from the same slave (Fig.31).** The same master occupies the bus all the time. The transfer direction is changed after the second R/$\overline{W}$ bit
- **Combined format. A master transmits data to one slave and then transmits data to another slave (Fig.32).** The same master occupies the bus all the time
- **Combined format. 10-bit and 7-bit addressing combined in one serial transfer (Fig.33).** After each START condition (S), or each repeated START condition (Sr), a 10-bit or 7-bit slave address can be transmitted. Figure 33 shows how a master-transmits data to a slave with a 7-bit address and then transmits data to a second slave with a 10-bit address. The same master occupies the bus all the time.

NOTES:

1) Combined formats can be used, for example, to control a serial memory. During the first data byte, the internal memory location has to be written. After the START condition and slave address is repeated, data can be transferred.
2) All decisions on auto-increment or decrement of previously accessed memory locations etc. are taken by the designer of the device.
3) Each byte is followed by an acknowledgement bit as indicated by the A or $\overline{A}$ blocks in the sequence.
4) I²C-bus compatible devices must reset their bus logic on receipt of a START or repeated START condition such that they all anticipate the sending of a slave address.

14.0 GENERAL CALL ADDRESS AND START BYTE

The 10-bit addressing procedure for the I²C-bus is such that the first two bytes after the START condition (S) usually determine which slave will be selected by the master. The exception is the 'general call' address 00000000 (H'00'). Slave devices with 10-bit addressing will react to a 'general call' in the same way as slave devices with 7-bit addressing (see Section 9.1.1).

Hardware masters can transmit their 10-bit address after a 'general call'. In this case, the 'general call' address byte is followed by two successive bytes containing the 10-bit address of the master-transmitter. The format is as shown in Fig.17 where the first DATA byte contains the eight least-significant bits of the master address.

The START byte 00000001 (H'01') can precede the 10-bit addressing in the same way as for 7-bit addressing (see Section 9.1.2).

15.0 ELECTRICAL SPECIFICATIONS AND TIMING FOR I/O STAGES AND BUS LINES

The I/O levels, I/O current, spike suppression, output slope control and pin capacitance for I²C-bus devices are given in Table 3. The I²C-bus timing is given in Table 4. Figure 34 shows the timing definitions for the I²C-bus.

The noise margin for HIGH and LOW levels on the bus lines for fast-mode devices are the same as those specified in Section 10.0 for standard-mode I²C-bus devices.

The minimum HIGH and LOW periods of the SCL clock specified in Table 4 determine the maximum bit transfer rates of 100 kbit/s for standard-mode devices and 400 kbit/s for fast mode devices. Standard-mode and fast-mode I²C-bus devices must be able to follow transfers at their own maximum bit rates, either by being able to transmit or receive at that speed or by applying the clock synchronization procedure described in Section 7 which will force the master into a wait state and stretch the LOW period of the SCL signal. Of course, in the latter case the bit transfer rate is reduced.

Table 3 Characteristics of the SDA and SCL I/O stages for I²C-bus devices

Parameter	Symbol	standard-mode devices		fast-mode devices		Unit
		Min.	Max.	Min.	Max.	
LOW level input voltage: fixed input levels V_{DD}-related input levels	V_{IL}	 −0.5 −0.5	 1.5 $0.3V_{DD}$	 −0.5 −0.5	 1.5 $0.3V_{DD}$	V
HIGH level input voltage: fixed input levels V_{DD}-related input levels	V_{IH}	 3.0 $0.7V_{DD}$	 *1) *1)	 3.0 $0.7V_{DD}$	 *1) *1)	V
Hysteresis of Schmitt trigger inputs: fixed input levels V_{DD}-related input levels	V_{hys}	 n/a n/a	 n/a n/a	 0.2 $0.05V_{DD}$	 - -	V
Pulse width of spikes which must be suppressed by the input filter	t_{SP}	n/a	n/a	0	50	ns
LOW level output voltage (open drain or open collector): at 3 mA sink current at 6 mA sink current	 V_{OL1} V_{OL2}	 0 n/a	 0.4 n/a	 0 0	 0.4 0.6	V
Output fall time from V_{IHmin} to V_{ILmax} with a bus capacitance from 10 pF to 400 pF: with up to 3 mA sink current at V_{OL1} with up to 6 mA sink current at V_{OL2}	t_{of}	 - n/a	 250[3] n/a	 $20 + 0.1C_b$[2] $20 + 0.1C_b$[2]	 250 250[3]	ns
Input current each I/O pin with an input voltage between 0.4 V and $0.9V_{DDmax}$	I_i	−10	10	−10[4]	10[4]	µA
Capacitance for each I/O pin	C_i	-	10	-	10	pF

n/a = not applicable

1) maximum $V_{IH} = V_{DDmax} + 0.5$ V

2) C_b = capacitance of one bus line in pF.

3) The maximum t_f for the SDA and SCL bus lines quoted in Table 4 (300 ns) is longer than the specified maximum t_{of} for the output stages (250 ns). This allows series protection resistors (R_s)to be connected between the SDA/SCL pins and the SDA/SCL bus lines as shown in Fig.37 without exceeding the maximum specified t_f.

4) I/O pins of fast-mode devices must not obstruct the SDA and SCL lines if V_{DD} is switched off.

Table 4 Characteristics of the SDA and SCL bus lines for I²C-bus devices

Parameter	Symbol	Standard-mode I²C-bus		Fast-mode I²C-bus		Unit
		Min.	Max.	Min.	Max.	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Bus free time between a STOP and START condition	t_{BUF}	4.7	-	1.3	-	µs
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	4.0	-	0.6	-	µs
LOW period of the SCL clock	t_{LOW}	4.7	-	1.3	-	µs
HIGH period of the SCL clock	t_{HIGH}	4.0	-	0.6	-	µs
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	-	0.6	-	µs
Data hold time: for CBUS compatible masters (see NOTE, Section 9.1.3) for I²C-bus devices	$t_{HD;DAT}$	 5.0 0[1]	 - -	 - 0[1]	 - 0.9[2]	 µs µs
Data set-up time	$t_{SU;DAT}$	250	-	100[3]	-	ns
Rise time of both SDA and SCL signals	t_r	-	1000	20 + 0.1C_b[4]	300	ns
Fall time of both SDA and SCL signals	t_f	-	300	20 + 0.1C_b[4]	300	ns
Set-up time for STOP condition	$t_{SU;STO}$	4.0	-	0.6	-	µs
Capacitive load for each bus line	C_b	-	400	-	400	pF

All values referred to V_{IHmin} and V_{ILmax} levels (see Table 3).

1) A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.

2) The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

3) A fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r\,max} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the standard-mode I²C-bus specification) before the SCL line is released.

4) C_b = total capacitance of one bus line in pF.

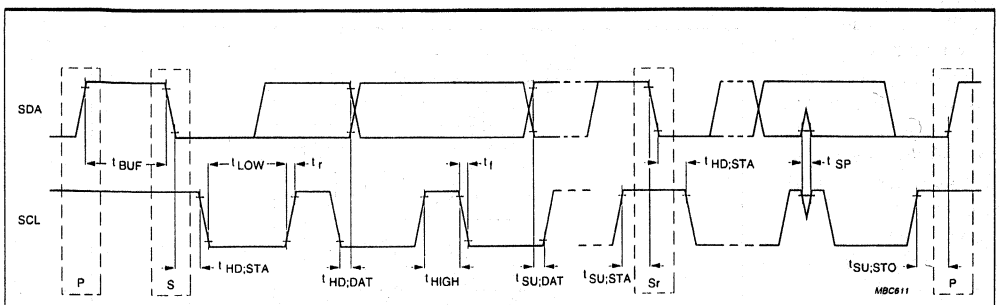


Fig.34 Definition of timing on the I²C-bus

16.0 APPLICATION INFORMATION

16.1 Slope-controlled output stages of fast-mode I²C-bus devices

The electrical specifications for the I/Os of I²C-bus devices and the characteristics of the bus lines connected to them are given in Tables 3 and 4 in Section 15.

Figures 35 and 36 show examples of output stages with slope control in CMOS and bipolar technology. The slope of the falling edge is defined by a Miller capacitor (C1) and a resistor (R1). The typical values for C1 and R1 are indicated on the diagrams. The wide tolerance for output fall time t_{of} given in Table 3 means that the design is not critical. The fall time is only slightly influenced by the external bus load (C_b) and external pull-up resistor (R_p). However, the rise time (t_r) specified in Table 4 is mainly determined by the bus load capacitance and the value of the pull-up resistor.

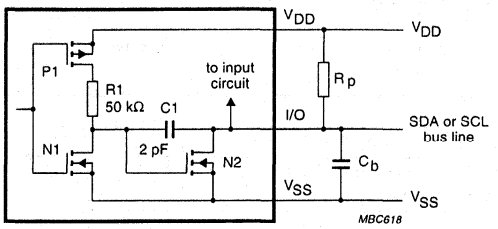


Fig.35 Slope-controlled output stage in CMOS technology

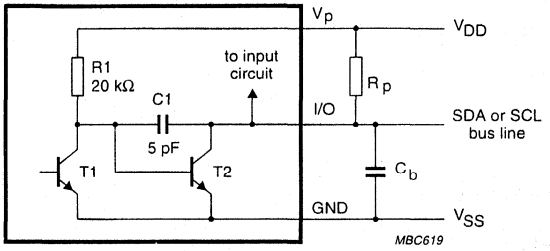


Fig.36 Slope-controlled output stage in bipolar technology

16.2 Switched pull-up circuit for fast-mode I²C-bus devices

The supply voltage (V_{DD}) and the maximum output LOW level determine the minimum value of pull-up resistor R_p (see Section 10.1). For example, with a supply voltage of V_{DD} = 5 V ± 10% and V_{OLmax} = 0.4 V at 3 mA, $R_{p\,min}$ = (5.5 − 0.4)/0.003 = 1.7 kΩ. As shown in Fig.38, this value of R_p limits the maximum bus capacitance to about 200 pF to meet the maximum t_r requirement of 300 ns. If the bus has a higher capacitance than this, a switched pull-up circuit as shown in Fig.37 can be used.

The switched pull-up circuit in Fig.37 is for a supply voltage of V_{DD} = 5 V ± 10 % and a maximum capacitive load of 400 pF. Since it is controlled by the bus levels, it needs no

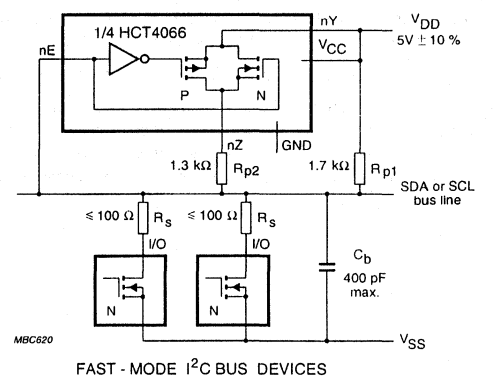


Fig.37 Switched pull-up circuit

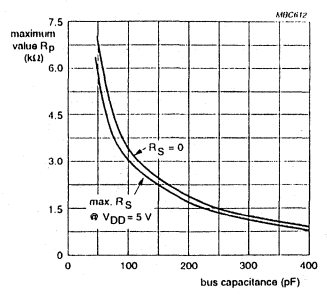


Fig.38 Maximum value of R_p as a function of bus capacitance for meeting the $t_{r\,max}$ requirement for a fast-mode I²C-bus

additional switching control signals. During the rising/falling edges, the bilateral switch in the HCT4066 switches pull-up resistor R_{p2} on/off at bus levels between 0.8 V and 2.0 V. Combined resistors R_{p1} and R_{p2} can pull-up the bus line within the maximum specified rise time (t_r) of 300 ns. The maximum sink current for the driving I²C-bus device will not exceed 6 mA at V_{OL2} = 0.6 V, or 3 mA at V_{OL1} = 0.4 V.

Series resistors R_s are optional. They protect the I/O stages of the I²C-bus devices from high-voltage spikes on the bus lines, and minimize crosstalk and undershoot of the bus line signals. The maximum value of R_s is determined by the maximum permitted voltage drop across this resistor when the bus line is switched to the LOW level in order to switch off R_{p2}.

16.3 Wiring pattern of the bus lines

In general, the wiring must be so chosen that crosstalk and interference to/from the bus lines is minimized. The bus lines are most susceptible to crosstalk and interference at the HIGH level because of the relatively high impedance of the pull-up devices.

If the length of the bus lines on a PCB or ribbon cable exceeds 10 cm and includes the V_{DD} and V_{SS} lines, the wiring pattern must be:

SDA _____
V_{DD} _____
V_{SS} _____
SCL _____

If only the V_{SS} line is included, the wiring pattern must be:

SDA _____
V_{SS} _____
SCL _____

These wiring patterns also result in identical capacitive loads for the SDA and SCL lines. The V_{SS} and V_{DD} lines can be omitted if a PCB with a V_{SS} and/or V_{DD} layer is used.

If the bus lines are twisted-pairs, each bus line must be twisted with a V_{SS} return. Alternatively, the SCL line can be twisted with a V_{SS} return, and the SDA line twisted with a V_{DD} return. In the latter case, capacitors must be used to decouple the V_{DD} line to the V_{SS} line at both ends of the twisted pairs.

If the bus lines are shielded (shield connected to V_{SS}), interference will be minimized. However, the shielded cable must have low capacitive coupling between the SDA and SCL lines to minimize crosstalk.

16.4 Maximum and minimum values of resistors R_p and R_s for fast-mode I²C-bus devices

The maximum and minimum values for resistors R_p and R_s connected to a fast-mode I²C-bus can be determined from Fig.25, 26 and 28 in Section 10.1. Because a fast-mode I²C-bus has faster rise times (t_r) the maximum value of R_p as a function of bus capacitance is less than that shown in Fig.27 The replacement graph for Fig.27 showing the maximum value of R_p as a function of bus capacitance (C_b) for a fast mode I²C-bus is given in Fig.38.

17.0 DEVELOPMENT TOOLS

17.1 Development tools for 8048 and 8051-based systems

Product	Description
OM1016	I²C-bus demonstration board with microcontroller, LCD, LED, Par. I/O, SRAM, EEPROM, Clock, DTMF generator, AD/DA conversion, infrared link.
OM1018	manual for OM1016
OM1020	LCD and driver demonstration board
OM4151	I²C-bus evaluation board (similar to OM1016 above but without infrared link).
OM5027	I²C-bus evaluation board for low-voltage, low-power ICs & software

17.2 Development tools for 68000-based systems

Product	Description
OM4160	Microcore-1 demonstration/evaluation board: SCC68070, 128K EPROM, 512K DRAM, I²C, RS-232C, VSC SCC66470, resident monitor
OM4160/3	Microcore-3 demonstration/evaluation board: 128K EPROM, 64K SRAM, I²C, RS-232C, 40 I/O (inc. 8051-compatible bus), resident monitor
OM4160/3QFP	Microcore-3 demonstration/evaluation board for 9XC101 (QFP80 package)

17.3 Development tools for all systems

Product	Description
OM1022	I²C-bus analyzer. Hardware and software (runs on IBM or compatible PC) to experiment with and analyze the behaviour of the I²C-bus (includes documentation)

18.0 SUPPORT LITERATURE

Data handbooks	Ordering code
Semiconductors for radio and audio systems IC01a 1995 IC01b 1995	 9398 652 61011 9398 652 62011
Semiconductors for television and video systems IC02a 1995 IC02b 1995 IC02c 1995	 9398 652 63011 9398 652 64011 9398 652 65011
Semiconductors for telecom systems IC03 1995	 9398 652 66011
Display drivers and microcontroller peripherals IC12	 planned
8048-based 8-bit microcontrollers IC14 1994	 9398 652 40011
RF/wireless communications IC17 1994	 9398 652 60011 98-2000-290-05 (USA)
Semiconductors for in-car electronics and general industrial electronics IC18	 planned
80C51-based 8-bit microcontrollers IC20 1994	 9398 652 70011 98-8080-390-03 (USA)
68000-based 16-bit microcontrollers IC21	 planned
ICs for multimedia systems IC22 1995	 planned
Desktop video data handbook	9398 652 84011
Brochures/leaflets/lab. reports	
I²C-bus compatible ICs and support overview	9398 706 38011
I²C-bus control programs for consumer applications	9398 380 30011
Microcontrollers, microprocessors and support overview	9398 706 37011
Application notes for 80C51-based 8-bit microcontrollers	9398 652 57011
OM5027 I²C-bus evaluation board for low-voltage, low-power ICs & software	9398 706 98011
P90CL301 I²C driver routines	AN94078
User manual of Microsoft Pascal I²C-bus driver (MICDRV4.OBJ)	ETV/IR8833
User's guide to I²C-bus control programs	ETV8835

19.0 APPLICATION OF THE I²C-BUS IN THE ACCESS.bus SYSTEM

The ACCESS.bus (bus for connecting ACCESSory devices to a host system) is an I²C-bus based open-standard serial interconnect system jointly developed and defined by Philips and Digital Equipment Corporation. It is a lower-cost alternative to an RS-232C interface for connecting up to 14 inputs/outputs from peripheral equipment to a desk-top computer or workstation over a distance of up to eight metres. The peripheral equipment can be relatively low speed items such as keyboards, hand-held image scanners, cursor positioners, bar-code readers, digitizing tablets, card readers or modems.

All that's required to implement an ACCESS.bus is an 8051-family microcontroller with an I²C-bus interface, and a 4-wire cable carrying a serial data (SDA) line, a serial clock (SCL) line, a ground wire and a 12 V supply line (500 mA max.) for powering the peripherals.

Important features of the ACCESS.bus are that the bit rate is only about 20% less than the maximum bit rate of the I²C-bus, and the peripherals don't need separate device drivers. Also, the protocol allows the peripherals to be changed by 'hot-plugging' without re-booting.

As shown in Fig.39, the ACCESS.bus protocol comprises three levels: the I²C-bus protocol, the base protocol, and the application protocol.

The base protocol is common to all ACCESS.bus devices and defines the format of the ACCESS.bus message. Unlike the I²C-bus protocol, it restricts masters to sending and slaves to receiving data. One item of appended information is a checksum for reliability control. The base protocol also specifies seven types of control and status messages which are used in the system configuration which assigns unique addresses to the peripherals without the need for setting jumpers or switches on the devices.

The application protocol defines the message semantics that are specific to the three categories of peripheral device (keyboards, cursor locators, and text devices which generate character streams e.g. card readers) which are at present envisaged.

Philips offers computer peripheral equipment manufacturers technical support, a wide range of I²C-bus devices and development kits for the ACCESS.bus. Hardware, software and marketing support is also offered by DEC.

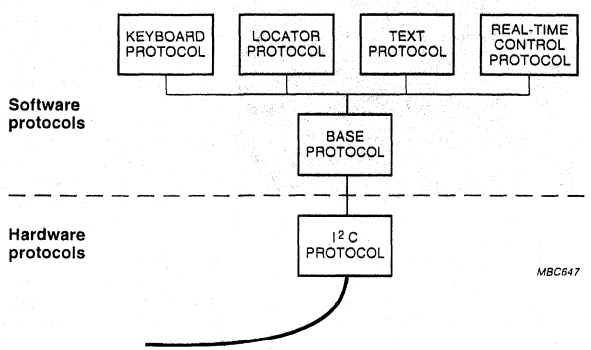


Fig.39 ACCESS.bus protocol hierarchy

EMBEDDED SYSTEMS

Programming the I²C Interface

When intelligent devices need to communicate

Mitchell Kahn

The Inter-Integrated Circuit Bus ("I²C Bus" for short) is a two-wire, synchronous, serial interface designed primarily for communication between intelligent IC devices. The I²C bus offers several advantages over "traditional" serial interfaces such as Microwire and RS-232. Among the advanced features of I²C are multimaster operation, automatic baud-rate adjustment, and "plug-and-play" network extensions.

Mention the I²C bus to a group of American engineers and you'll likely get hit with an abundance of blank stares. I say American engineers because until recently the I²C bus was primarily a European phenomenon. Within the last year, however, interest in I²C in the United States has risen dramatically. Embedded systems designers are realizing the cost, space, and power savings afforded by robust serial interchip protocols.

The idea of serial interconnect between integrated circuits is not new. Many semiconductor vendors offer devices designed to "talk" via serial links with other processors. Current examples include Microwire (National Semiconductor), SPI (Motorola), and most recently Echelon's Neuron chips. In all cases, the goal is the same: to reduce the wiring and pincount necessary for a parallel data bus. It simply does not make economic sense to route a full-speed parallel bus to a slow peripheral.

Unfortunately for most serial-bus-capable devices, the choice of a bus protocol will dictate the CPU architecture. For example, only two CPU architectures implement an on-chip I²C port. If your choice of architecture precludes use of these architectures, then your only option is to implement the protocol in software.

The software implementation of the I²C protocol discussed in this article came about as a result of an implicit challenge during a staff meeting. One of our managers proposed that we hire a consultant to write a software I²C driver for the Intel 80C186EB embedded processor. Being somewhat new to the group, I took exception (although not verbally!) to his suggestion. A weekend of intense hacking later, I presented the first prototype of the driver. My reward? I got to write a generic version of the driver for general distribution.

Design Trade-offs

Three distinct tasks are involved in implementing the I²C protocol: watching the bus, waiting for a specific amount of time, and driving the bus. This became apparent when I flowcharted 1 byte of a typical bus transaction; see Figure 1. The time delays associated with creating the bus waveforms would normally have been relegated to the 80C186EB's on-chip timers. I could not, however, assume that the end users of my code would be able to spare a timer for the software I²C port. I had to forego the elegance (and to some extent accuracy) of the on-chip timers for the sledgehammer approach of software timing loops. Luckily, the I²C protocol is extremely forgiving with regard to timing accuracy. The decision to use assembly instead of a high-level language stemmed directly from the need to control program-execution time. I had neither the time nor the inclination to hand-tune high-level code.

Having made the decision to use assembly language, I faced my next problem: Could I make the code portable? Intel offers a plethora of CPU and embedded-controller architectures. Would it be possible to make the code somewhat portable between disparate assembly languages? I found my answer in the use of macros.

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All the basic building blocks of the I²C protocol (watching, waiting, and doing) can be compartmentalized into distinct macros. The algorithms that make up the I²C driver are written with these macros as the framework. You don't need to understand the intricacies of the I²C protocol to port these routines—you just need to know how to make your CPU watch, wait, and do.

For example, a 4.7_uS delay is a common event during a transfer. The macro *%Wait_4_7_uS* implements just such a delay by using the 8086 LOOP instruction with a couple of NOPs for tuning; see Example 1(a). Total execution time is readily calculated from instruction timing tables. The same macro is ported to the i960 architecture in Example 1(b). Although I am a neophyte when it comes to i960 programming, I had no problems porting the core macros.

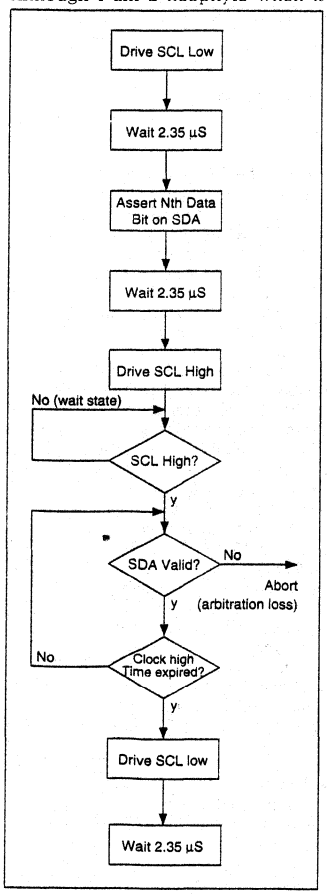


Figure 1: *Flowchart of process for transmission of a single bit.*

Hardware Dependencies

A few words about the target hardware are in order before I discuss the code. Any implementation of the I²C protocol requires two open-drain (or open-collector), bidirectional port pins for the Serial Clock (SCL) and Senal Data (SDA) lines. The code in this article was designed for the 80C186EB embedded processor, which has two open-drain ports on-chip. The two pins, P2.6 (SCL) and P2.7 (SDA), are part of a larger 8-bit port. Processors without open-drain I/O ports can easily implement I²C with the addition of an external open-collector latch.

Two special-function registers, P2PIN and P2LTCH, are used to read and write the state of the port pins. The 80C186EB allows the special-function registers to be located anywhere in either memory or I/O space. For this implementation, I chose to leave the registers in I/O space, even though this limited my choice of instructions. The 80186 architecture does not provide for read-modify-write instructions in I/O space (an AND to I/O, for example); it can only load and store (IN and OUT). So why did I limit myself? Again, I had to assume the lowest common denominator for our customers when designing my code.

Building the Framework

Early on in development, I decided to partition my code macros according to physical processes involved in the I²C protocol. Code not directly involved in mimicking the actions of a hardware I²C port was not written as macros. For example, the code necessary to access the stack frame is not written as a macro, whereas the code needed to toggle the clock line is. This was done to isolate architecture-dependent code sequences from the more generic I²C functions. Macros were also not used for "gray areas" such as the shifting of serial data, which is both architecture dependent and physical in nature. The I²C functions that passed the litmus test fell into the three aforementioned categories of watching, waiting, and doing.

The "waiting" macros provide a fixed-minimum time delay. They are implemented using a simple LOOP $ delay. The LOOP instruction decrements the CX register, then branches to the target (in this case itself) if the result is non-zero. The delay is (n-1)*15+5 clocks, where n is the starting value in the CX register. All the delays were calculated assuming a 16-MHz clock rate (62.5 nanoseconds per clock). The code still works at lower CPU speeds because the I²C protocol only specifies minimum timings. In fact, the delay macros are only "accurate enough," providing timings as close as I could get to the specified minimum without undue tuning.

The "watching" macros are "spin-on-bit" polling loops. These pieces of code wait for a transition on the appropriate I²C line to occur before allowing execution to continue. There are two polling macros for each of the two I²C signal lines; one for high-to-low transitions and one for low-to-high transitions. The

(a)

```
%*DEFINE(Wait_4_7_uS)(
        mov     cx, 5           ; 4 clocks
        loop    $               ; 4*15+5 = 65 clocks
        nop                     ; 3 clocks
        nop                     ; 3 clocks
                                ; total = 75 clocks
                                ; 75 * 62.5ns = 4.69uS (close enough)

        )
```

(b)

```
define(Wait_4_7_uS,'

        lda     0x17, r4        # instruction may be issued in parallel
                                # so assume no clocks.
0b:     cmpdeco 0, r4           # compare and decrement counter in r4
        bne.t   0b              # if !=0 branch back (predict taken
                                # branch)
                                #
                                # The cmpdeco and bne.t together take 3
                                # clocks in parallel minimum.
                                #
                                # 0x17 (25 decimal) * 3 = 75 clocks
                                # at 16MHz this is 4.69uS
')
```

Example 1: *(a) 80C186 implementation of 4.7_uS wait macro; (b) 80960CA implementation of 4.7_uS wait macro.*

polling of the SCL line that gives rise to an important feature of I²C: automatic, bit-by-bit baud-rate adjustment. Any device on the I²C bus may hold the clock line low in order to stall the bus for more time (a serial wait state). The other devices on the bus are then forced to poll the SCL line until the slow device releases control of the clock.

The *%Get_SDA_Bit* macro also falls under the category of "watching." Its function is simply to return the state of the SDA line without waiting for a transition. *%Get_SDA_Bit* is used primarily to pull the serial data off the bus when the clock is valid.

The "doing" macros control the state of the clock and data lines. As with the polling macros, there are four types—one for each transition of the SCL or SDA lines. The "doing" macros are named to reflect the physical operations they perform. For example, *%Drive_SCL_Low* always drives the SCL line to a low state. *%Release_SCL_High*, on the other hand, relinquishes control of the SCL line, which may then be pulled high or driven low by another device on the bus. A read-modify-write operation is used for the bit manipulation so that the other 6 bits of Port 2 are not affected by the I²C operations.

Getting on the Bus

Three procedures were created using the macro framework. I'll describe only the master transmit (Listing One, page 106) and master receive functions (Listing Two, page 108), as they represent the needs of most I²C users. The slave procedure is long and intricate and will not be described here.

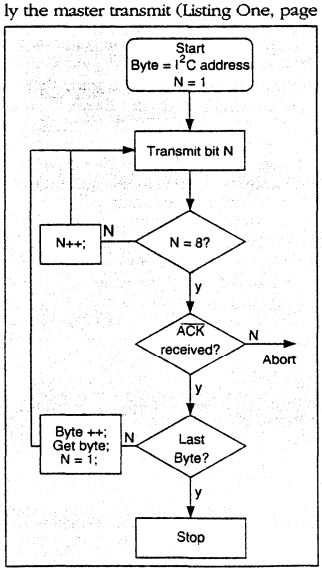


Figure 2: *Flowchart for I²C transmit procedure.*

An I²C master transmission proceeds as follows:

1. The master polls the bus to see if it is in use.
2. The master generates a start condition on the bus.
3. The master broadcasts the slave address and expects an acknowledge (ACK) from the addressed slave.
4. The master transmits 0 or more bytes of data, expecting an ACK following each byte.
5. The master generates a stop condition and releases the bus.

The stack frame for the master transmit procedure, I2CXA.A86, includes a far pointer to the message for transmission, the byte count for the message, and the slave address. Far pointers and far procedure calls are used in all the procedures. No attempt was made to conform to a specific high-level language calling convention, although such a conversion would be trivial. The procedures save only the state of the modified segment registers.

The master transmit procedure performs error checking on the passed parameters before attempting to send the message. The maximum message length is set at 64 Kbytes by the segmentation of the 80186 memory space. This restriction could be removed by including code to handle segment boundaries. The transmit procedure also checks the direction bit in the slave address to ensure that a reception was not erroneously indicated. Errors are reported back to the calling procedure through the AX register. (The exact code is in Listing One.)

The first step in sending a message is getting on the I²C bus. The macro *%Check_For_Bus_Free* simply polls the bus to determine if any transactions are in progress. If so, the transmit procedure aborts with the appropriate error code. If the bus is free, a start condition is generated. The start condition is defined as a high-to-low transition of SDA with SCL high followed by a 4.7_uS pause. These waveforms are easily generated with the *%Drive_SDA_Low* and *%Wait_4_7_uS* macros.

All communication on the I²C bus between the stop and start conditions, including addressing and data, takes place as an 8-bit data value followed by an acknowledge bit. This lead to the natural nested loop structure for the body of the procedure; see Figure 2.

The inner loop is responsible for transmitting the 8 bits of each data byte. Each transmitted bit generates the appropriate data (SDA) and clock (SCL) waveforms while checking for both serial wait states and potential bus collisions. A bus collision occurs when two masters attempt to gain control of the bus simultaneously. The I²C protocol handles collisions with the simple rule: "He who transmits the first 0 on the SDA line wins the bus." To ensure that we (the master transmit procedure) own the bus, the SDA line is checked whenever transmitting a 1. If a 0 is present, then a collision has occurred (because another master is pulling the line low), and the transfer must be aborted.

Three distinct tasks are involved in implementing the I²C protocol: watching the bus, waiting for a specific amount of time, and driving the bus

Control is turned over to the outer loop after the 8 bits of data (or address) have been transmitted. The outer loop immediately checks for an acknowledge from the addressed slave. The transfer is aborted if an acknowledge is not received. At the end of the ACK bit the message length counter is decremented. Control is returned to the inner loop if more data remains, otherwise a stop condition is generated and the master transmit procedure terminates.

Registers are used for intermediate result storage throughout the body of the procedure. For example, the AH register is used to hold the current value (either address or data) being shifted onto the SDA line. This eliminates the need for local data storage within the procedure.

On the Receiving End

The steps involved in an I²C master receive transaction are almost identical to those in transmission:

1. The master polls the bus to see if it is in use.
2. The master generates a start condi-

tion on the bus.
3. The master broadcasts the slave address and expects an ACK from the addressed slave.
4. The master receives 0 or more bytes of data and sends an ACK to the slave after each byte. The master signals the last byte by not sending an ACK.
5. The master generates a stop condition and releases the bus.

A far pointer to the receive buffer is passed on the stack to the master receive procedure. The remainder of the parameters—slave address and message count—are identical between the two procedures. The received message length is fixed at 64 Kbytes, again because of segmentation. The error-checking, bus-availability sensing, and start-condition generation sections of the receive procedure are lifted verbatim from the transmit code.

The structure of the receive procedure differs slightly once the start condition has been generated; see Figure 3. The slave address is transmitted using one iteration of the transmit procedure's outer loop. Control is passed to the receive loop once the slave acknowledges its address.

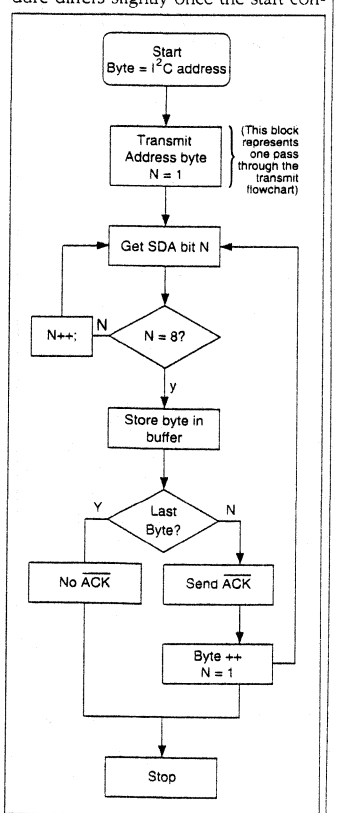


Figure 3: *Flowchart for I2C receive procedure.*

The receive loop structure is patterned after that of the transmit procedure. The inner loop controls the clocking of the SCL line and the shifting of the serial data off the SDA line into the CPU. Eight iterations of the inner loop are performed to receive each byte. The outer loop stores the received byte in the buffer, decrements the byte count, then sends an ACK to the slave. The last data byte is signalled by not sending an ACK.

Using the Procedures

Listing Three (page 110) shows a short program that uses both the master transmit and master receive procedures. The call to procedure I2C_XMIT displays the word "bUS-" on a four-character, seven-segment display controlled by the SAA1064 I²C compatible display driver. The time of day is read from the PCF8583 real-time clock by the call to procedure I2C_RECV.

Please note that interrupts must be disabled during the execution of both procedures. An interruption at an inopportune time (when the master is not in control of the clock) could cause the bus to hang. If you need to service interrupts periodically, then enable them only when the clock is driven low.

These procedures have been tested on a wide array of I²C devices ranging from serial EEPROMs to voice synthesizers. No compatibility problems have been seen to date.

Enhancing the Code

I've kicked around many ideas for enhancing the I²C procedures. You could, for example, replace the timing loops with timed interrupts. That way, the CPU could perform useful work during the pauses. Along the same lines, the pauses could be scheduled using a real-time kernel, again improving CPU throughput. Finally, you could add a high-level language calling structure.

The use of timed interrupts adds an order of magnitude to the complexity of the code, but would be worth it for high-performance, real-time systems.

Conclusion

I²C is not the only game in town when in comes to serial protocols. Hopefully, some of the techniques presented here will carry over into the development of other "simulated" serial protocols, such as those targeted at the home-automation market. Who knows, maybe someday a snippet of my code may find its way into a truly intelligent dishwasher. I'll be waiting....

References

I²C Bus Specification, Philips Corporation (undated).

DDJ

All the basic building blocks of the I²C protocol (watching, waiting, and doing) can be compartmentalized into distinct macros

I²S bus specification

1.0 INTRODUCTION

Many digital audio systems are being introduced into the consumer audio market, including compact disc, digital audio tape, digital sound processors, and digital TV-sound. The digital audio signals in these systems are being processed by a number of (V)LSI ICs, such as:

- A/D and D/A converters;
- digital signal processors;
- error correction for compact disc and digital recording;
- digital filters;
- digital input/output interfaces.

Standardized communication structures are vital for both the equipment and the IC manufacturer, because they increase system flexibility. To this end, we have developed the inter-IC sound (I²S) bus – a serial link especially for digital audio.

2.0 BASIC SERIAL BUS REQUIREMENTS

The bus has only to handle audio data, while the other signals, such as sub-coding and control, are transferred separately. To minimize the number of pins required and to keep wiring simple, a 3-line serial bus is used consisting of a line for two time-multiplexed data channels, a word select line and a clock line.

Since the transmitter and receiver have the same clock signal for data transmission, the transmitter as the master, has to generate the bit clock, word-select signal and data. In complex systems however, there may be several transmitters and receivers, which makes it difficult to define the master. In such systems, there is usually a system master controlling digital audio data-flow between the various ICs. Transmitters then, have to generate data under the control of an external clock, and so act as a slave. Figure 1 illustrates some simple system configurations and the basic interface timing. Note that the system master can be combined with a transmitter or receiver, and it may be enabled or disabled under software control or by pin programming.

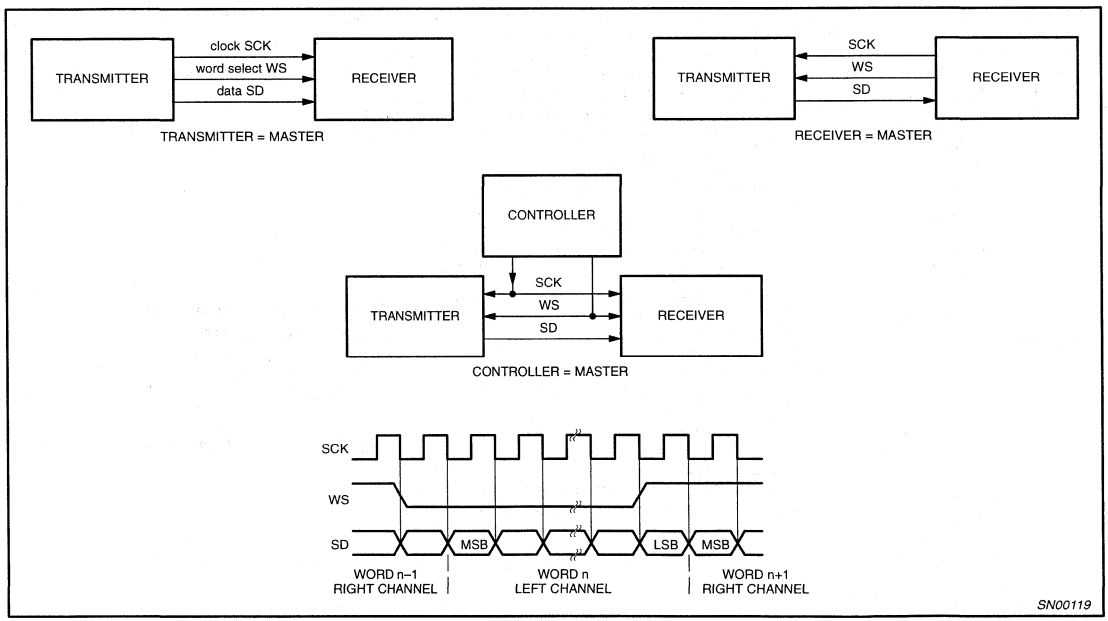


Figure 1. Simple System Configurations and Basic Interface Timing

3.0 THE I²S BUS

As shown in Figure 1, the bus has three lines:

- continuous serial clock (SCK);
- word select (WS);
- serial data (SD);

and the device generating SCK and WS is the master.

3.1 Serial Data

Serial data is transmitted in two's complement with the MSB first. The MSB is transmitted first because the transmitter and receiver may have different word lengths. It isn't necessary for the transmitter to know how many bits the receiver can handle, nor does the receiver need to know how many bits are being transmitted.

When the system word length is greater than the transmitter word length, the word is truncated (least significant data bits are set to '0') for data transmission. If the receiver is sent more bits than its word length, the bits after the LSB are ignored. On the other hand, if the receiver is sent fewer bits than its word length, the missing bits are set to zero internally. And so, the MSB has a fixed position, whereas the position of the LSB depends on the word length. The transmitter always sends the MSB of the next word one clock period after the WS changes.

Serial data sent by the transmitter may be synchronized with either the trailing (HIGH-to-LOW) or the leading (LOW-to-HIGH) edge of the clock signal. However, the serial data must be latched into the receiver on the leading edge of the serial clock signal, and so there are some restrictions when transmitting data that is synchronized with the leading edge (see Figure 2 and Table 1).

3.2 Word Select

The word select line indicates the channel being transmitted:

- WS = 0; channel 1 (left);
- WS = 1; channel 2 (right).

WS may change either on a trailing or leading edge of the serial clock, but it doesn't need to be symmetrical. In the slave, this signal is latched on the leading edge of the clock signal. The WS line changes one clock period before the MSB is transmitted. This allows the slave transmitter to derive synchronous timing of the serial data that will be set up for transmission. Furthermore, it enables the receiver to store the previous word and clear the input for the next word (see Figure 1).

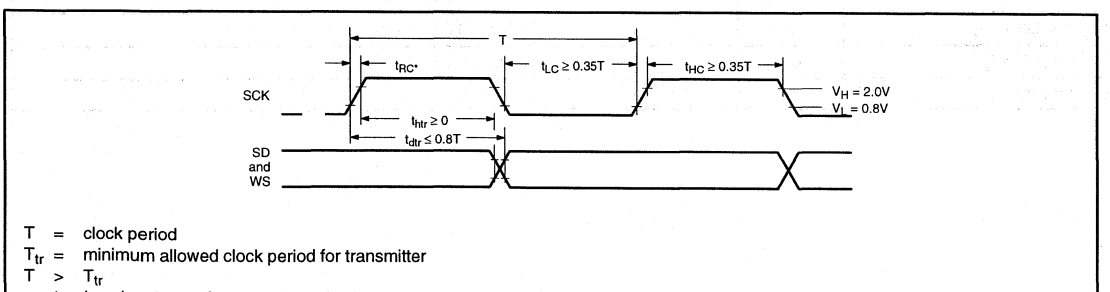
4.0 TIMING

In the I²S format, any device can act as the system master by providing the necessary clock signals. A slave will usually derive its internal clock signal from an external clock input. This means, taking into account the propagation delays between master clock and the data and/or word-select signals, that the total delay is simply the sum of:

- the delay between the external (master) clock and the slave's internal clock; and
- the delay between the internal clock and the data and/or word-select signals.

For data and word-select inputs, the external to internal clock delay is of no consequence because it only lengthens the effective set-up time (see Figure 2). The major part of the time margin is to accommodate the difference between the propagation delay of the transmitter, and the time required to set up the receiver.

All timing requirements are specified relative to the clock period or to the minimum allowed clock period of a device. This means that higher data rates can be used in the future.



T = clock period
T_{tr} = minimum allowed clock period for transmitter
T > T_{tr}
* t_{RC} is only relevant for transmitters in slave mode.

SN00120

Figure 2. Timing for I²S Transmitter

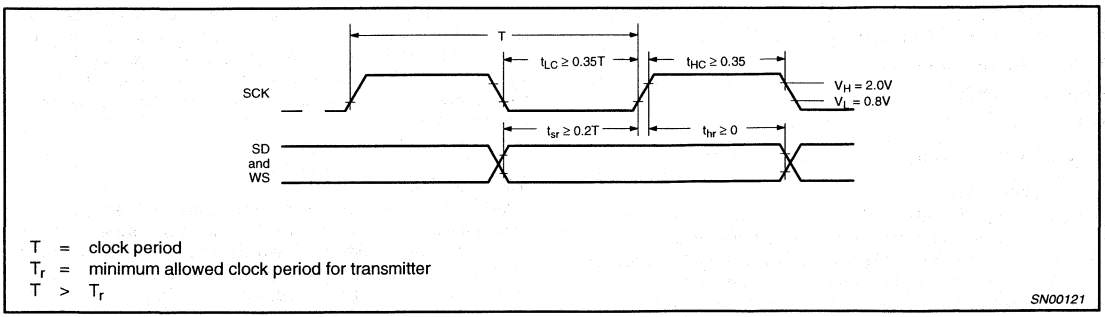


Figure 3. Timing for I²S Receiver

Note that the times given in both Figures 2 and 3 are defined by the transmitter speed. The specification of the receiver has to be able to match the performance of the transmitter

Example: Master transmitter with data rate of 2.5MHz (±10%) (all values in ns)

	MIN	TYP	MAX	CONDITION
clock period T	360	400	440	$T_{tr} = 360$
clock HIGH t_{HC}	160			min > 0.35T = 140 (at typical data rate)
clock LOW t_{LC}	160			min > 0.35T = 140 (at typical data rate)
delay t_{dtr}			300	max < 0.80T = 320 (at typical data rate)
hold time t_{htr}	100			min > 0
clock rise-time t_{RC}			60	max > $0.15T_{tr}$ = 54 (only relevant in slave mode)

Example: Slave receiver with data rate of 2.5MHz (±10%) (all values in ns)

	MIN	TYP	MAX	CONDITION
clock period T	360	400	440	$T_{tr} = 360$
clock HIGH t_{HC}	110			min < 0.35T = 126
clock LOW t_{LC}	110			min < 0.35T = 126
set-up time t_{sr}	60			min < 0.20T = 72
hold time t_{htr}	0			min < 0

Table 1. Timing for I²S transmitters and receivers

	TRANSMITTER				RECEIVER				
	LOWER LIMIT		UPPER LIMIT		LOWER LIMIT		UPPER LIMIT		
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	NOTES
Clock period T	T_{tr}				T_r				1
MASTER MODE:									
clock generated by transmitter or receiver:									
HIGH t_{HC}	$0.35T_{tr}$				$0.35T_{tr}$				2a
LOW t_{LC}	$0.35T_{tr}$				$0.35T_{tr}$				2a
SLAVE MODE:									
clock accepted by transmitter or receiver:									
HIGH t_{HC}		$0.35T_{tr}$				$0.35T_r$			2b
LOW t_{LC}		$0.35T_{tr}$				$0.35T_r$			2b
rise-time t_{RC}			$0.15T_{tr}$						3
TRANSMITTER:									
delay t_{dtr}				0.8T					4
hold time t_{htr}	0								3
RECEIVER:									
set-up time t_{sr}						$0.2T_r$			5
hold time t_{hr}						0			5

All timing values are specified with respect to high and low threshold levels.

NOTES:

1. The system clock period T must be greater than T_{tr} and T_r because both the transmitter and receiver have to be able to handle the data transfer rate.
2a. At all data rates in the master mode, the transmitter or receiver generates a clock signal with a fixed mark/space ratio. For this reason t_{HC} and t_{LC} are specified with respect to T.
2b. In the slave mode, the transmitter and receiver need a clock signal with minimum HIGH and LOW periods so that they can detect the signal. So long as the minimum periods are greater than $0.35T_r$, any clock that meets the requirements can be used (see Figure 3).
3. Because the delay (t_{dtr}) and the maximum transmitter speed (defined by T_{tr}) are related, a fast transmitter driven by a slow clock edge can result in t_{dtr} not exceeding t_{RC} which means t_{htr} becomes zero or negative. Therefore, the transmitter has to guarantee that t_{htr} is greater than or equal to zero, so long as the clock rise-time t_{RC} is not more than t_{RCmax}, where t_{RCmax} is not less than $0.15T_{tr}$.
4. To allow data to be clocked out on a falling edge, the delay is specified with respect to the rising edge of the clock signal and T, always giving the receiver sufficient set-up time.
5. The data set-up and hold time must not be less than the specified receiver set-up and hold time.

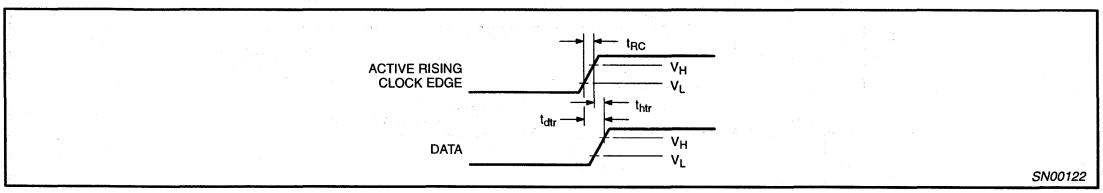


Figure 4. Clock rise-time definition with respect to the voltage levels

5.0 VOLTAGE LEVEL SPECIFICATION

5.1 Output Levels

V_L < 0.4V
V_H > 2.4V both levels able to drive one standard TTL input (I_{IL} = –1.6mA and
I_{IH} = 0.04mA).

5.2 Input Levels

V_{IL} = 0.8V
V_{IH} = 2.0V

Note: At present, TTL is considered a standard for logic levels. As other IC (LSI) technologies become popular, other levels will also be supported.

6.0 POSSIBLE HARDWARE CONFIGURATIONS

6.1 Transmitter (see Figure 5)

At each WS-level change, a pulse WSP is derived for synchronously parallel-loading the shift register. The output of one of the data latches is then enabled depending on the WS signal. Since the serial data input is zero, all the bits after the LSB will also be zero.

6.2 Receiver (see Figure 6)

Following the first WS-level change, WSP will reset the counter on the falling edge of SCK. After decoding the counter value in a "1 out of n" decoder, the MSB latch (B1) is enabled (EN1 = 1), and the first serial data bit (the MSB) is latched into B1 on the rising edge of SCK. As the counter increases by one every clock pulse, subsequent data bits are latched into B2 to Bn.

On the next WS-level change, the contents of the n latches are written in parallel, depending on WSD, into either the left or the right data-word latch. After this, latches B2 to Bn are cleared and the counter reset. If there are more than n serial data bits to be latched, the counter is inhibited after Bn (the receiver's LSB) is filled and subsequent bits are ignored.

Note: The counter and decoder can be replaced by an n-bit shift-register (see Figure 7) in which a single '1' is loaded into the MSB position when WSP occurs. On every subsequent clock pulse, this '1' shifts one place, enabling the N latches. This configuration may prove useful if the layout has to be taken into account.

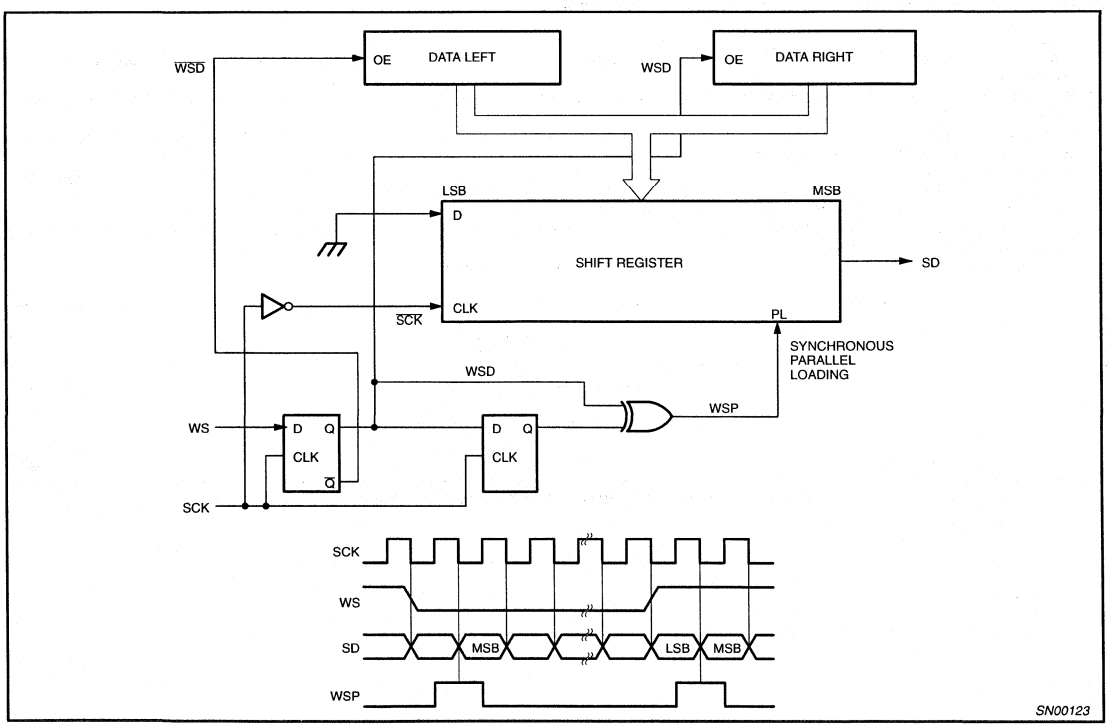


Figure 5. Possible transmitter configuration

I²S bus specification

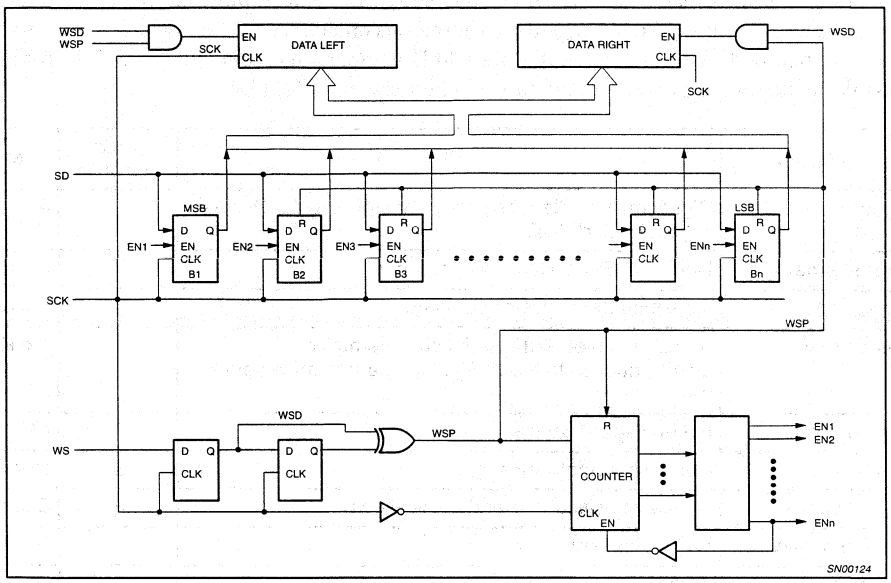


Figure 6. Possible receiver configuration. The latches and the counter use synchronous set, reset and enable inputs, where set overrules the reset input, and reset overrules the enable input.

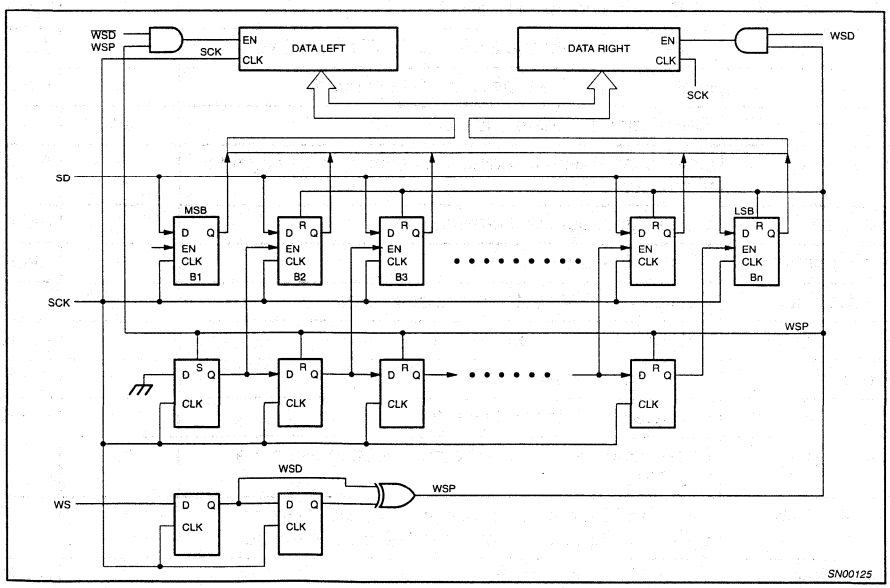


Figure 7. Possible receiver configuration, using an n-bit shift-register to enable control of data input register.

This table identifies material Aki Kaniel and George Ellis are submitting for inclusion in IC22. Unfortunately, we have had no response to numerous emails regarding cut-off date — so make sure these are included. Also, be aware that Ronald Bruegmann has sent files on 6/7/96 for review and possible inclusion; approved documents will be forwarded 6/11/96.

filename	title	page count	sponsor
digital media	Digital multimedia technology transforming the PC into TV, radio, and VCR	11	Aki Kaniel
USB standard	Universal Serial Bus (USB) standard	7	Aki Kaniel
TV sound	TV sound transmission standards	1	Aki Kaniel
bus on diet	A bus on a diet — the serial bus alternative an introduction to the P1394 high performance serial bus	13	Aki Kaniel
I2S bus spec	I^2S bus specification	7	Aki Kaniel
comb filter	Comb filter application	3	George Ellis
crystal specs	Crystal specifications and applications	2	George Ellis
video glossary	Video glossary	3	George Ellis
audio glossary	Audio glossary	2	George Ellis
i2c addresses	I^2C bus addresses	1	George Ellis
DPC71 eval brd	DPC71 Evaluation board	23	George Ellis
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i2cbus spec	The I^2C-bus and how to use it (including specifications)	24	Aki Kaniel
DIFCVS	AN ETV/IR89126 Digital interfaces for component video signals	10	Aki Kaniel

A bus on a diet — the serial bus alternative an introduction to the P1394 high performance serial bus

Author: Michael Johas Teener, Plumbing Architect; Apple Computer, Inc.

Version 1.6 — This paper is largely based on one of the same title presented to CompCon '92 in February 1992. Reprinted with permission.

ABSTRACT

This paper briefly discusses the justifications for the use a serial bus in computer systems. It then describes a leading proposal for such an interconnect: the proposed IEEE P1394 High Performance Serial Bus.

NOTE: A previous version of this paper was presented at IEEE CompCon '92, in February 1992. This version has been updated with the latest changes to the P1394 specification.

1.0 INTRODUCTION: WHY SERIAL?

Traditionally, computer systems are tied together with parallel backplane busses. Although this has served well in the past, designers are looking at narrower alternatives for three primary reasons:

1. **Physical constraints.** Systems are getting smaller and the space available is decreasing faster than connector technology can cope.
2. **Cost.** Semiconductor technology is still on a fairly fast evolutionary path, while connector and inter-connect technology is relatively mature. For a fixed level of performance, the cost of an interconnect drops much faster if its implementation is semiconductor intensive (narrow) instead of connector intensive (wide).
3. **Reliability.** The primary point of failure in an interconnect is usually its physical connection. The fewer the signals, the simpler (and more reliable) its connector.

1.1 Memory or Channel

There are two primary ways to view an interconnect: as some kind of extended memory space or as a more abstract channel interface. In a memory space interconnect, all resources are viewed as memory or registers that are accessed by "read", "write" and other processor-to-memory transactions. In channel interfaces, the transactions are at a higher level; typically some kind of command such as "read logical block" or "print page."

This paper confines itself to the memory model interconnects, so channel interfaces such as FibreChannel are not discussed.

1.2 Some Serial Bus Alternatives

There are a variety of serial designs that may serve as examples of serial busses. Three of these are listed below:

1. **IEEE 1596 SCI.** The Scalable Coherent Interface has three physical layers, and two of the three are 1250 Mbaud serial designs: one using coax and one using optical fiber. SCI is a pure 64-bit address memory-model interconnect that follows the IEEE 1212 Command and Status Register (CSR) Architecture. It has a sophisticated and powerful cache coherence mechanism that supports large multiprocessor systems with up to 65k nodes. This comes at the cost of significant complexity, but all that complexity is hidden in the implementation of the interface: something that scales well with developing semiconductor technology. Right now, this is the ultimate in serial bus performance.
2. **Apple Desktop Bus(ADB).** This is a proprietary minimalist serial interface that provides a simple read-write protocol to up to 16 devices, each with only eight eight-bit registers. Its data rate of 90 kbits/sec is very low, really only adequate for a CPU to communicate with keyboards, pointing devices or other desktop devices. ADB is extremely simple to implement, requiring less than 1000 gates.
3. **IEEE P1394 High Performance Serial Bus.** The P1394 serial bus lies somewhere between the previous examples. Like SCI, it follows the IEEE 1212 architecture and has a 64-bit address space. It does not, however, support cache coherency and its latency and transfer rate are not adequate for use in tightly-coupled multiprocessing. On the other hand, as a low-cost interconnect for loosely-coupled systems it may find considerable use.

Since the P1394 serial bus lies in the fuzzy middle ground between an ultimate serial bus like SCI and the very modest ADB, it makes a good candidate for further examination.

2.0 THE P1394 HIGH PERFORMANCE SERIAL BUS[1]

The P1394 specification describes a high speed serial bus designed for low cost yet providing the data transfer speed and low latency needed for a peripheral bus or as a backup to a traditional parallel backplane bus. The highlights of the Serial Bus[2] include:

1. Consistent with the IEEE 1212 Control and Status Register Architecture Specification.
2. Bus transactions that include both block and single quadlet reads and writes, as well as an "isochronous" mode which provides a low-overhead guaranteed bandwidth service.
3. Automatic assignment of node addresses - no need for address switches.
4. Both fair and priority bus access mechanisms that guarantee all nodes at least partial access, regardless of priority.
5. A Physical Medium Dependent layer supporting both cable media and backplane busses.
6. Variable speed data transmission of 24.576 Mbit/sec for TTL backplanes, 49.152 Mbit/sec for BTL and ECL backplanes, and 98.304, 196.608 and 393.216 Mbit/sec for the cable medium.
7. The cable medium allows up to 16 physical connections (cable hops) between any two devices. Each hop can be up to 4.5 meters long, giving a total cable distance of 72 meters . Bus management recognizes smaller configurations to optimize performance.

1. NOTE: much of this description of the P1394 Serial Bus is extracted from draft 60 of the proposed specification.
2. In the rest of this paper, the P1394 High Performance Serial Bus will be referred to simply as the Serial Bus.

2.1 Topology

The physical topology of the Serial Bus is divided into two parts as shown in Figure 1. The first part is called the "backplane environment" which is specific to the particular host parallel backplane. The other part is called the "cable environment" and is completely specified in the P1394 document. Nodes on a single bus may reside in different backplane environments, or directly in the cable environment. There is no requirement that the Serial Bus have any particular set of environments. All nodes may reside strictly in a single back-plane, or they all may be directly attached to the cable, or any combination of backplanes or cable.

2.1.1 Cable Environment

The physical topology for the cable environment is a non-cyclic network with limited branches and extent. The medium consists of 2 shielded twisted pairs for signals and one pair for power and ground which connect together ports on a node. Each port consists of terminators, transceivers and simple logic. The cable and ports act as bus repeaters between the nodes to simulate a single logical bus.

Since each node must continuously repeat bus signals, the separate power and ground wires within the cable enable the physical layer of each node to remain operational even if node local power is off. The pair can even power an entire node if its requirements are modest. The Serial Bus cable provides 8 to 40 VDC at up to 1.5 A. The actual current available is system-dependent.

2.1.2 Backplane Environment

The Serial Bus can be extended within each physical device as a two-signal electrical bus. This can provide a simple and direct way for internal processing resources to communicate with appropriate peripherals.

The backplane interface to the Serial Bus will make use of the pins reserved for a Serial Bus by the various ANSI/IEEE bus standards. Drivers and receivers for these signals follow the conventions established by the appropriate parallel bus standard: e.g., Futurebus using BTL and Fastbus and SCI using ECL.

2.2 Node and Board Architectures

The Serial Bus architecture is defined in terms of entities called nodes. A node is an addressable entity, which can be independently reset and identified. More than one node may be co-located on a single physical module, and more than one functional unit may be co-located on a single node.

2.3 Addressing

The Serial Bus follows the IEEE 1212 standard for 64-bit fixed addressing, where the upper 16 bits of each address is the node_id. This allows a system of up to 64k nodes. The Serial Bus divides the node_ID into two smaller fields: the higher order 10 bits specify a bus_ID and lower order 6 bits specify a physical_ID. Each of the fields reserves the value of all "1"s for special purposes, so this addressing scheme provides for 1023 busses each with 63 nodes to be accessible in a simple manner. This standardization is continued within the node, with 2 48 bytes (256 terabytes) divided between CSRs (command and status registers - core IEEE 1212 resources, registers specific to the Serial Bus, a ROM ID area, and node-specific resources) and general memory space.

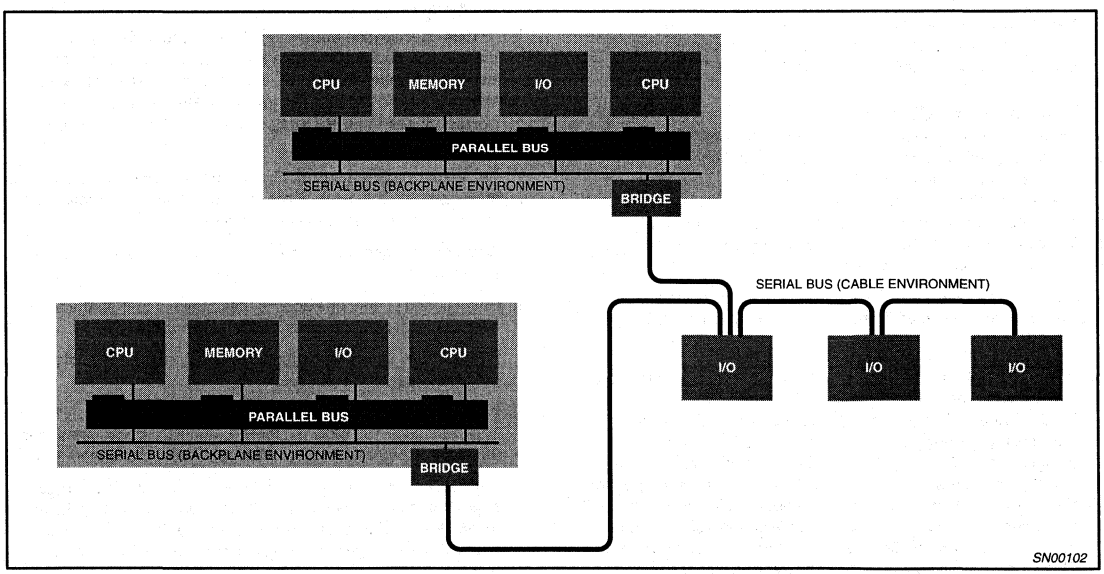

Figure 1. Serial Bus Physical Topology

2.4 Protocol Architecture

The serial bus protocols are described as a set of three stacked layers as shown in Figure 2:

1. **The Transaction Layer** defines a complete request-response protocol to perform the bus transactions required to support the IEEE 1212 architecture (the operations of read, write, and lock). Note that the Transaction Layer does not add any services for isochronous data, although it does provide a path for isochronous management data to get to the Serial Bus Management via reads from and writes to the isochronous control CSRs.
2. **The Link Layer** provides an acknowledged datagram[3] service to the Transaction Layer. It provides addressing, data checking, and data framing. One Link Layer transfer is called a "subaction". The Link Layer also provides an isochronous data transfer service directly to the application.
3. **The Physical Layer** translates the logical symbols used by the Link Layer into electrical signals on the different Serial Bus media. It also guarantees that only one node at a time is sending data. The Physical Layer also defines the mechanical interfaces for the Serial Bus. There is a different Physical Layer for each environment: cable and backplane.

The fourth entity in the Serial Bus protocol is Serial Bus Management which provides the basic control functions and standard CSRs needed by nodes on the bus.

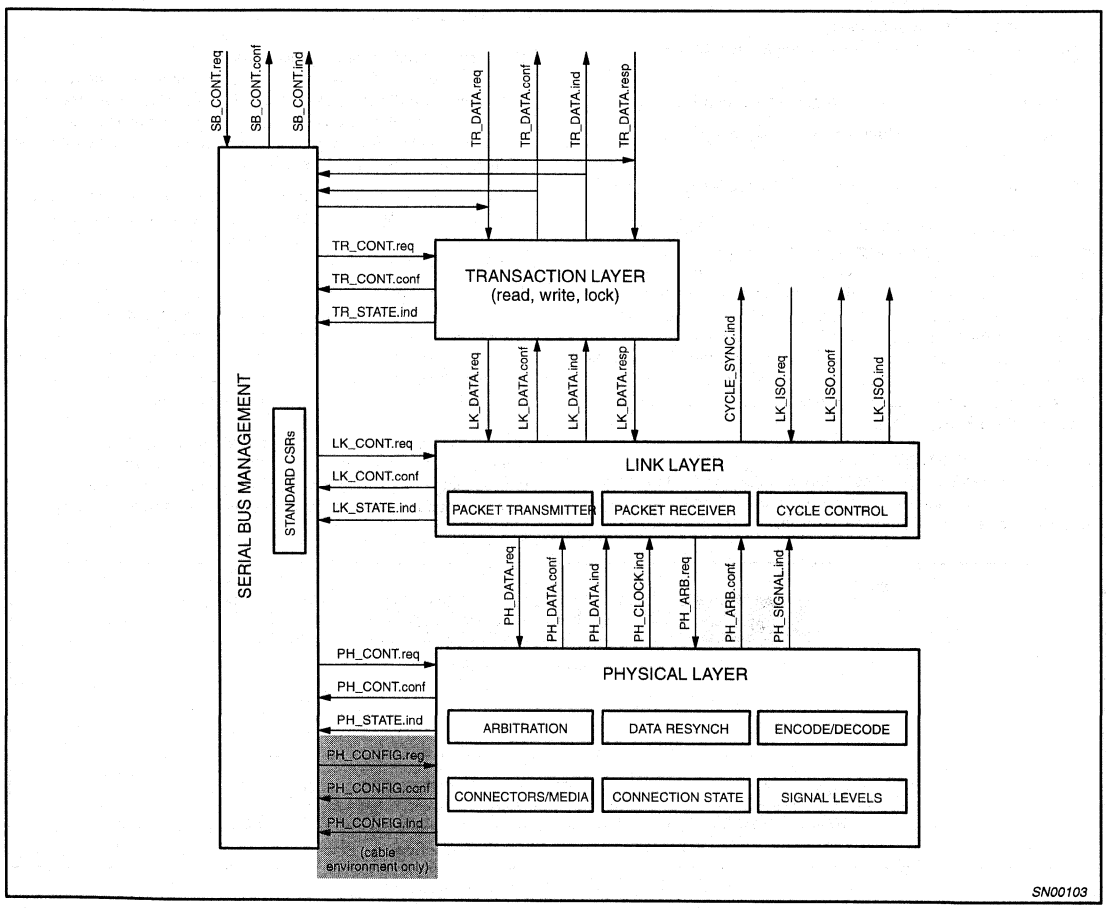

Figure 2. Serial Bus Protocol Stack

3. One-way data transfer with confirmation of reception.

3.0 TRANSACTION LAYER

Data is transferred between nodes (a requester and one or more responders) on the serial bus by three different types of transactions, where each transaction consists of one or two subactions: a request and possibly a response. The three transactions are:

1. Read — data is transferred from a responder back to a requester.
2. Write — data is transferred from a requester to one or more responders.
3. Lock — data is transferred from a requester to a responder, operated on by the responder, and then transferred back to the requestor.

Transactions consist of four actions:

1. Request — the action taken by a requestor to start the transaction.
2. Indication — the reception of a request by a responder.
3. Response — the action taken by the responder to finish the transaction.
4. Confirmation — the reception of the response by the requestor.

The Serial Bus architecture limits the maximum number of data bytes in a transaction to the largest power-of-two such that the whole Link Layer subaction takes less than 62 µsec (this is half the isochronous cycle time, and restricting asynchronous subaction to this value helps minimize buffer requirements). This means that packets are limited to 512 bytes at the cable base rate of 98.304 Mbit/sec. Implementations, however, can impose further restrictions. The only required transactions are quadlet write/read on quadlet aligned addresses (these are the transactions necessary to access the standard CSR resources).

3.1 Lock Subcommands

Since the Serial Bus supports split transactions, it cannot be easily locked while transaction sequences implement indivisible test-and-set operations. Therefore, special lock transactions are defined which communicate the intent from the requester to the responder, thus allowing the indivisible updates to be performed at the responder.

4.0 LINK LAYER

The Link Layer provides a half-duplex data packet delivery service. The process of delivering a single packet is called a "subaction", and there are two types used in the Serial Bus Link Layer:

1. Asynchronous Subaction — a variable amount of data and several bytes of Transaction Layer information are transferred to an explicit address and an acknowledge is returned. N is
2. Isochronous Subaction or "Channel" — a variable amount of data is transferred on regular intervals with simplified addressing and no acknowledge.

The subaction has three possible parts:

1. Arbitration Sequence — a node that wishes to become a source requests the Physical Layer to gain control of the bus. This may be immediate if the node already controls the bus (as it would be if the subaction is the transaction response corresponding to the immediately preceding acknowledge).
2. Packet Transmission —the source node sends a speed code, format and transaction codes, addresses of the source and destination nodes, and data. Isochronous packets include a short channel identifier rather than source or destination addresses.
3. Acknowledgment — a uniquely addressed destination returns a code indicating the action taken by the packet receiver. If the acknowledgment is "pending", then the transmission packet of the corresponding response may be concatenated to the end of the acknowledge code. Isochronous packets and asynchronous broadcast packets do not have acknowledgments.

All asynchronous subactions are normally separated by periods of idle bus called "subaction gaps," but if a responding transaction layer is fast enough, then the request subaction and corresponding response subaction may be concatenated as shown in Figure 3.

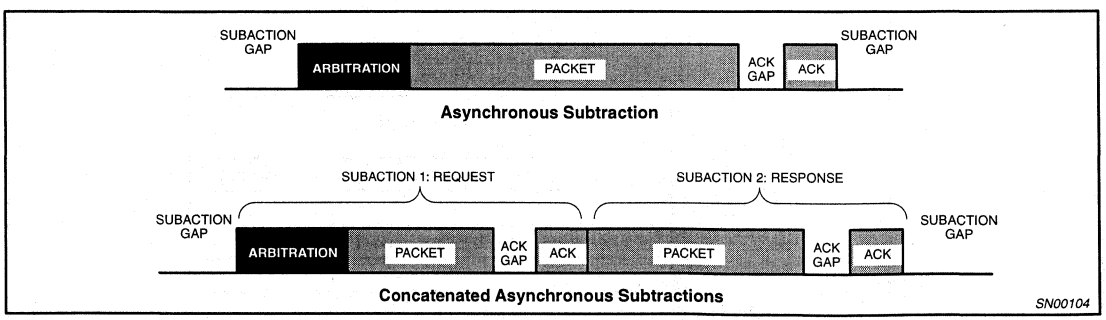

Figure 3. Example Asynchronous Subactions

The link layer operations also have the request, indication, response, and confirmation actions:

1. Request — the action taken by a link requestor to transmit a packet to a link responder.
2. Indication — the reception of a packet by a link responder.
3. Response — the transmission of an acknowledgement & optional packet by a link responder.
4. Confirmation — the reception of the acknowledgement & optional packet by the link requester.

The Transaction Layer and Link Layer interact in a way that optimizes the use of the bus. In particular, write transactions can be implemented in two different ways: unified or split. If the transaction and link layers of a responding node are fast enough, the entire transaction can be implemented with a single Link Layer subaction: the transmission of a packet and the corresponding acknowledgement.

Where the response takes longer to generate, then a split transaction is required with separate Link Layer subactions for the request and the response. Note that other Link Layer subactions occur on the bus between the request and response subactions of a single transaction.[4]

When the Transaction Layer is busy and cannot accept a packet, the Link Layer sends a "busy" acknowledge back to the requesting node (this indicates that the destination Transaction Layer will not be returning a response). As an option, the Link Layer at the requesting node can retry the packet for a limited period. If bus retry traffic is high, then slower-acting nodes may be starved. To prevent this from happening there is a two-phase busy/retry protocol which allows all retries to be processed in a timely fashion.

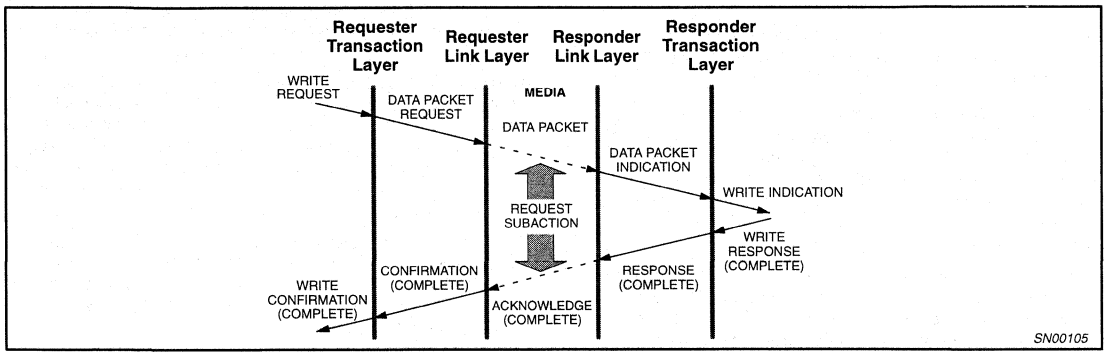

Figure 4. Unified Transaction

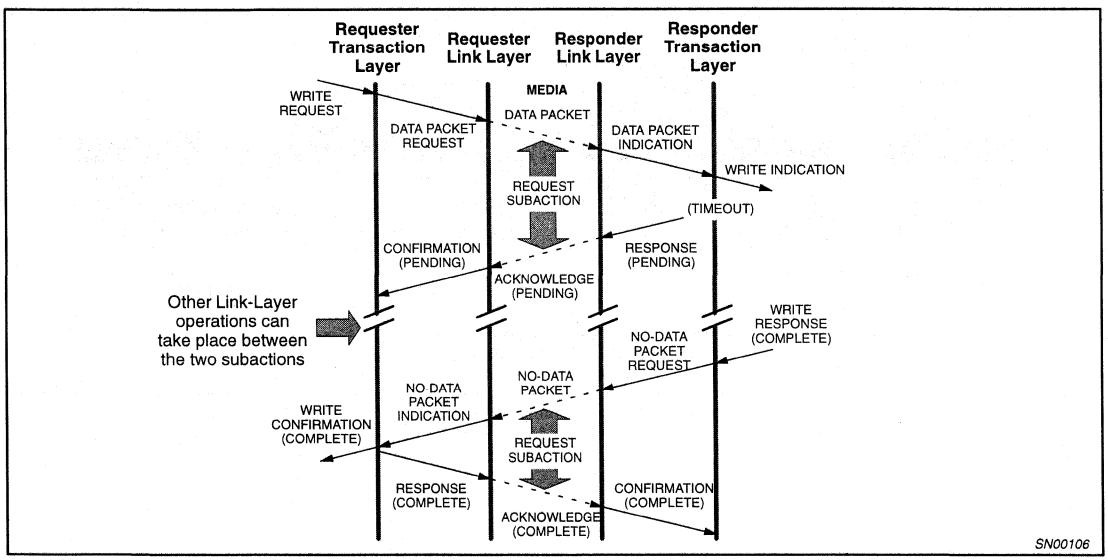

Figure 5. Split Transaction Example

4. Split transactions are required for reads and locks since they return data to the requestor.

4.1 Arbitration

To enhance the usefulness of Serial Bus, each node on the bus can use one of three different access methods. These access protocols are:

1. **Fair Arbitration.** Fair arbitration is used by nodes which can equally share the bus bandwidth. This is the default method.
2. **Urgent Arbitration.** Urgent arbitration can be used by nodes which desire a majority of the bus band-width or have severe latency requirements. For example, a high-bandwidth real-time data collection node may use priority arbitration when critical data buffers are more than half full. This method is only available in the backplane environment.
3. **Isochronous Access.** Data that is regularly generated and consumed, such as digital sound, can be transferred using an isochronous access method that guarantees bandwidth on the bus with very low overhead.

The first two arbitration methods use the request-response arbitration service provided by the Physical Layer while isochronous access requires a higher level protocol.

4.2 Isochronous Access

The normal bus request used by asynchronous subactions is quite adequate for nodes that do not require a guaranteed amount of bandwidth or a relatively precise timing reference (for example, digital audio or video equipment or many types of instrumentation). The data transferred by such equipment are more conveniently handled using an isochronous access method.

These isochronous services can be provided without upsetting the basic access protocol by establishing the convention that the highest priority access is reserved for a "cycle" master that is responsible for maintaining a common clock source. The cycle master will try to transmit a special timing request called a "cycle start" at very specific intervals set by a "cycle synch" source (nominally 8 KHz ± 100 ppm, or 125 µsec ± 12.5 nsec). If another transfer is still taking place when the cycle synch occurs, then the cycle-start will be delayed resulting in significant jitter in the start time of the transfer. Since this jitter is frequently unacceptable as a timing reference, the amount of time that the cycle start request was delayed is encoded within the request.

Nodes sending isochronous data respond to cycle start requests by immediately arbitrating for the bus without waiting for a subaction gap and sending an isochronous packet as soon as arbitration succeeds. This leads to a smaller minimum gap between isochronous packets than is needed for asynchronous arbitration to start. (The timing for gaps between isochronous packets is the same as for asynchronous acknowledges.)

Only when all the nodes sending isochronous data have won arbitration and finished sending their data will the bus stay idle long enough for a subaction gap to appear. It is the subaction gap which will allow normal asynchronous arbitration to resume. Figure 6 illustrates the basic isochronous access system.

The isochronous packets are labeled with 8-bit "channel" numbers which have been previously chosen using a simple distributed resource allocation algorithm using the compare-and-swap lock transaction. Since nodes sending isochronous packets still arbitrate for the bus and the natural priority of a node is not related to channel number, the order of packet transmission is also not related with channel number.

When a node has been assigned a channel, it can send a variable amount of data up to a maximum specified by the channel manager. The distributed resource allocation algorithm guarantees that the time consumed by all nodes sending isochronous data not exceed the 125 µsec in a cycle.

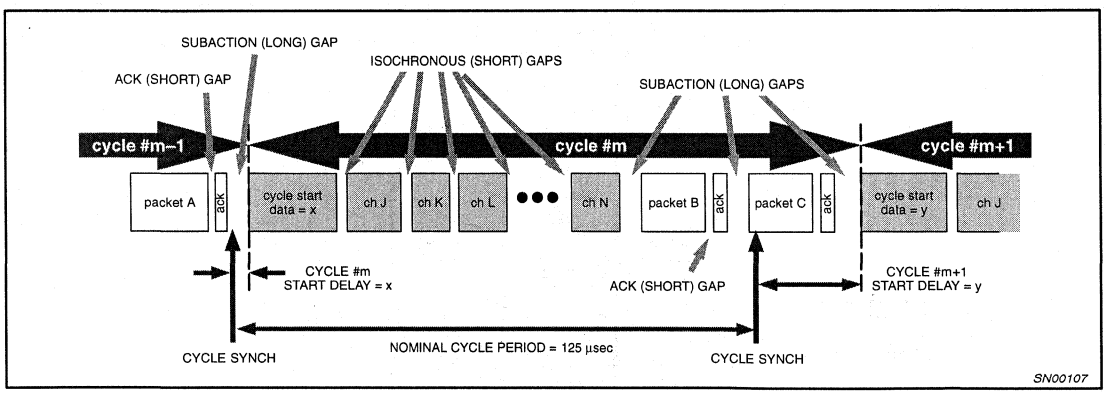

Figure 6. Isochronous Cycle Structure

5.0 PHYSICAL LAYER

The Physical Layer has three primary functions: data transmission and reception, arbitration, and the actual electrical and mechanical interface. The cable and backplane environments each have a separate physical layer but share two fundamental concepts: "data-strobe" encoding for packet data, and a simple method for ensuring fair access to the bus.

5.1 Packet Data Transmission and Reception

During packet transmission, there is only a single node transmitting on the bus, so the entire media can operate in a half duplex mode using two signals: Sbus_Data and Sbus_Strb. NRZ data is transmitted on Sbus_Data and is accompanied by the Sbus_Strb signal which changes state whenever two consecutive NRZ data bits are the same, ensuring that a transition occurs on either Sbus_Data or Sbus_Strb for each data bit. A clock which transitions each bit period can be derived from the exclusive-or of Sbus_Data with Sbus_Strb as shown in Figure 7.

5.2 Fair Arbitration

The normal cable and backplane arbitration methods guarantee that only one node will be transmitting at the end of the arbitration period. As described above, these methods only provide a strict priority access; the node with the highest natural priority (highest arbitration number on a backplane, closest to the root on a cable) will always win. The normal asynchronous access method for the Serial Bus adds a simple scheme that splits the access opportunities evenly among competing nodes.

The fairness protocol is based on the concept of a fairness interval. A fairness interval consists of one or more periods of bus activity separated by short idle periods called subaction gaps and is followed by a longer idle period known as an arb reset gap. At the end of each subaction gap, bus arbitration is used to determine the next bus owner. This concept is shown in Figure 8.

The implementation of the fair arbitration protocol is defined in terms of these fairness intervals, as is discussed in the following clauses.

When using fair arbitration, an active node becomes a bus owner exactly once in each fairness interval. The arb_enable signal is set to one by an arb_reset_gap and is cleared when the node becomes a bus owner. This disables further arbitration requests for the remainder of the fairness interval. A fairness interval ends when arbitration by the final fair node is successful; this generates a arb_reset_gap since all nodes now have their arb_enable signals reset and cannot drive the bus. The arb_reset_gap re-enables arbitration on all cards and starts the next fairness interval. This process is illustrated in Figure 9.

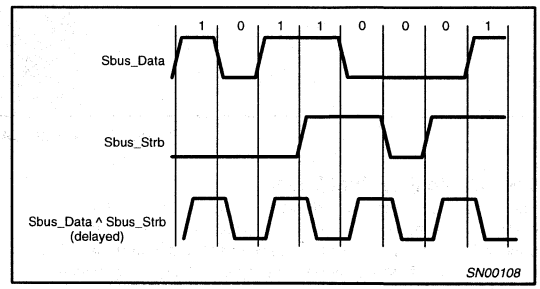

Figure 7. Data-strobe Encoding

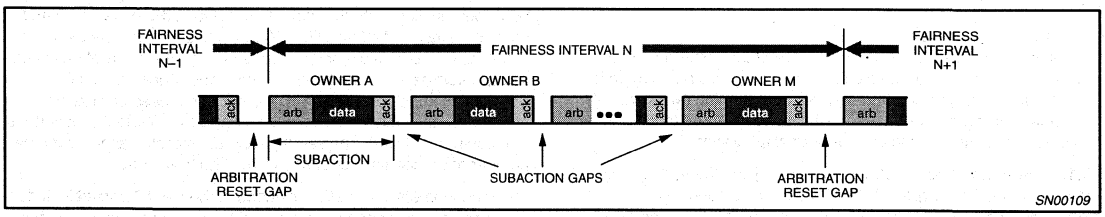

Figure 8. Fairness Interval

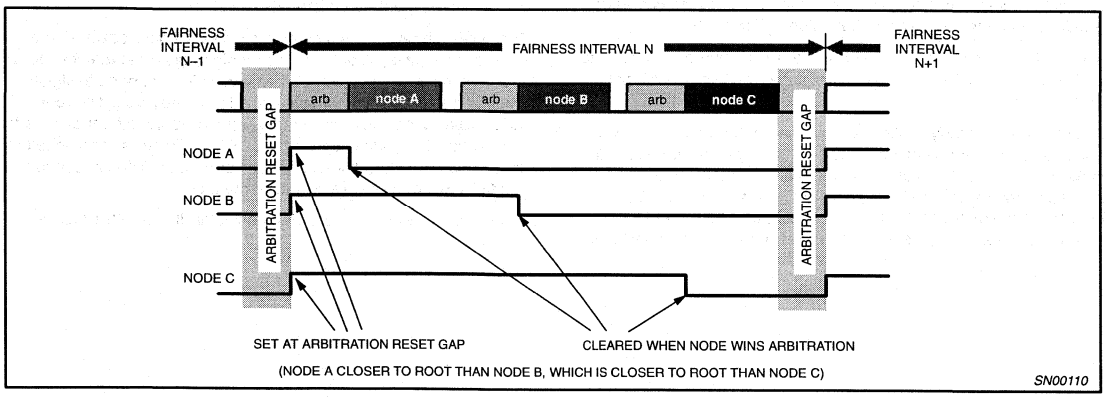

Figure 9. Fair Arbitration

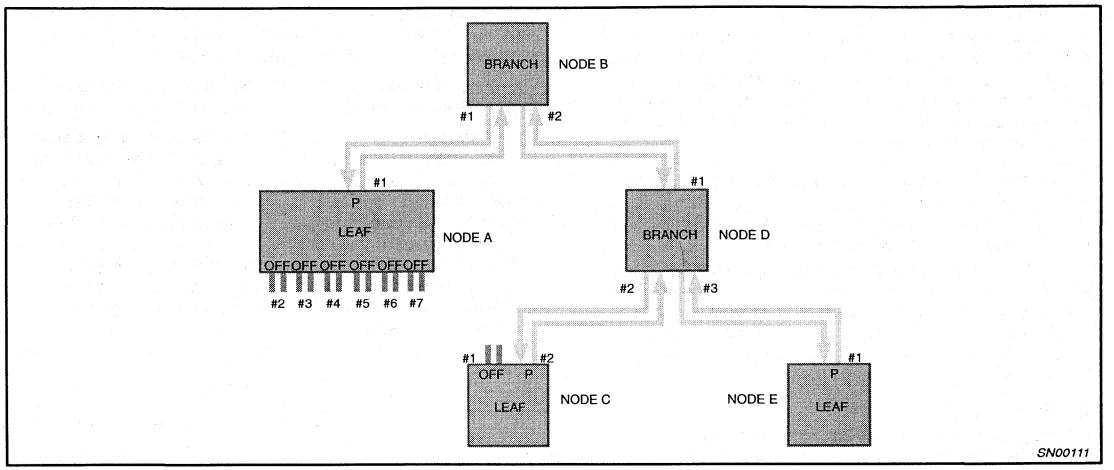

Figure 10. Example State After Bus Initialization

5.3 Cable Physical Layer

The cable environment is a network of nodes connected by point-to-point links called physical connections. The physical connection consists of a port on each of the nodes and the cable between them. A node can have multiple ports, which allows a branching multihop interconnect as shown in Figure 1. The primary restriction is that nodes must be connected together as an acyclic graph (no loops).

5.3.1 Cable Arbitration

The cable access method takes advantage of the point-to-point (non-bussed) nature of the cable environment by having each node handshake with its immediate neighbors to determine ownership of the media. There are four phases to this scheme, three to initialize the cable configuration, and one for normal arbitration.

5.3.1.1 Bus initialize — Whenever a node joins the bus, a signal forces all nodes into a special state that clears all topology information and starts the next phase. After bus initialize, the only information known to a node is whether it is a branch (more than one directly connected neighbor), a leaf (only a single neighbor) or isolated (unconnected). This is illustrated in Figure 10.

Note that each port of the node is individually numbered. There is no particular order to the numbering, it is just a way to give each port a unique label.

5.3.1.2 Tree identify — After a bus initialize, the tree ID process translates the general network topology into a tree, where one node is designated a root and all of the physical connections have a direction associated with them pointing towards the root node. The direction is set by labeling each connected port as a "parent" (connected to a node closer to the root) or "child" port (connected to a node further from the root). Any unconnected ports are labeled "off" and do not participate in further arbitration processes. Any loop in the topology is detected by a timeout in the tree-ID process.

5.3.1.3 Self identify— The next step is to give each node an opportunity to select a unique physical_ID and identify itself to any management entity attached to the bus.

Sending the self-ID information is done by transmitting one to four very short packets onto the cable that includes the physical ID and some management information. The physical ID is simply the count of the number of times a node passes through the state of receiving self-ID information before having its own opportunity to do so, i.e., the first node sending self-ID packet(s) chooses zero as its physical ID, the second chooses one, and so on. Note that a node is not required to decode the self-ID packet, it merely has to count the number of self identify sequences since the bus reset.

The management information included in the self-ID packet includes codes for the power needed to turn on the attached Link Layer, the state of the various ports (unconnected, connected to child, connected to parent), and data rate limitations.

The self-ID process uses a deterministic selection process where the root node passes control of the media to the node attached to its lowest numbered connected port and waits for that node to signal that it and all of its children have identified themselves. The root then passes control to its next highest port and waits for that node to finish. When the nodes attached to all the root's ports are finished, the root itself sends self identification information. The child nodes use the same process in a recursive manner.

Figure 11 illustrates the state of the bus after the self-ID process is complete.

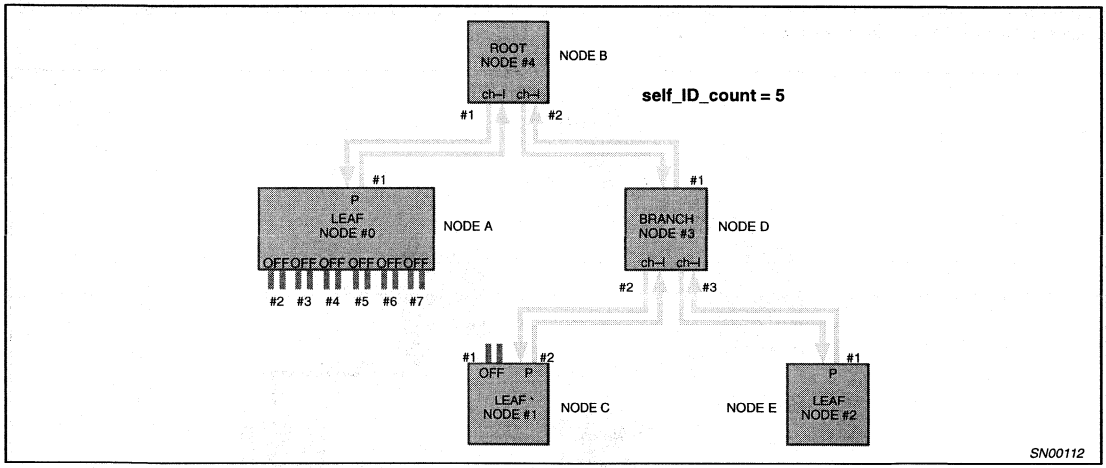

Figure 11. StateAfter Self-identify

5.3.1.4 Normal arbitration— Once the self identify process is complete, nodes can use the normal arbitration method to send packets. This process is illustrated by the example shown in Figure 12.

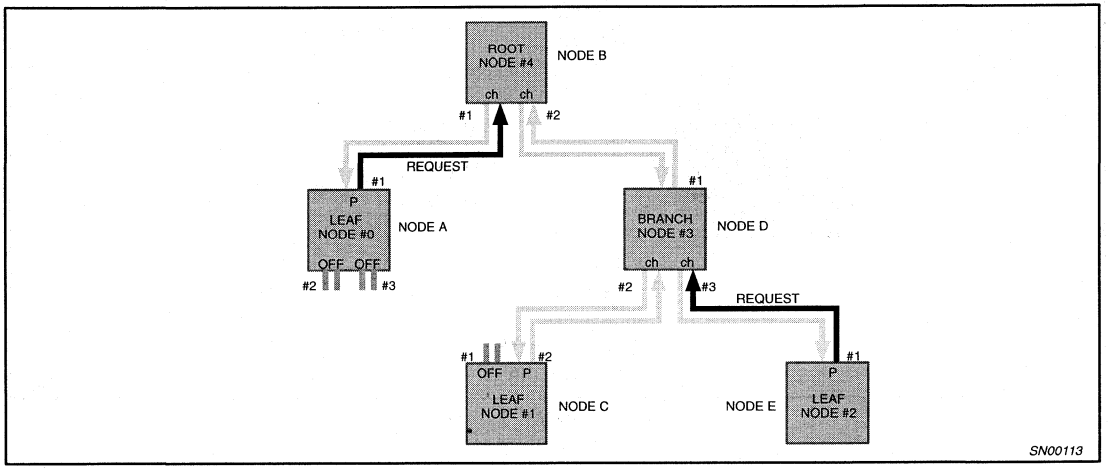

Figure 12. Arbitration Request

1. Node A and node E begin arbitrating at the same time by sending a request to their parents.

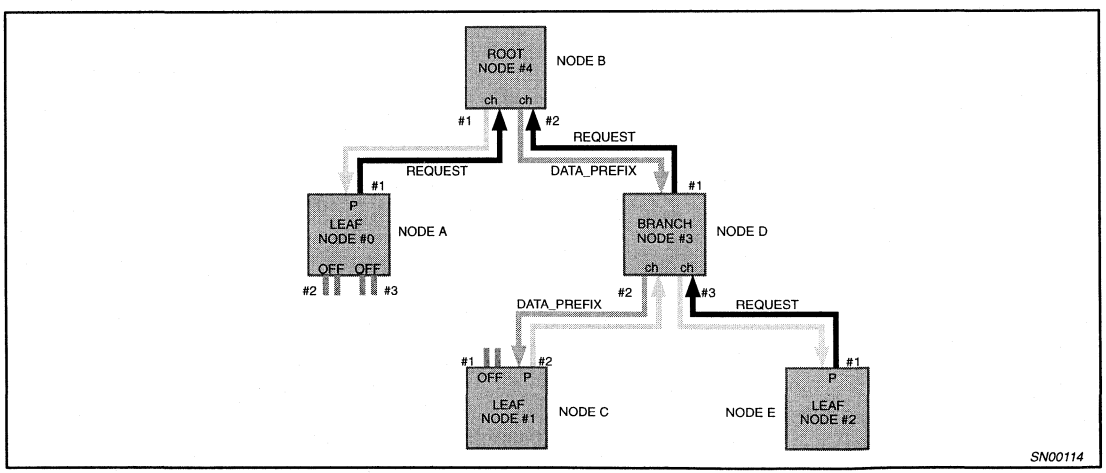

Figure 13. Arbitration Request (continued)

2. The parent of node E (node D) forwards the request to its parent (node B) and denies access to its other children (node C) by sending a data_prefix, while simultaneously the parent of node A (node B) denies access to its other children (node D). Since node B is root, it doesn't have to forward the request any further.

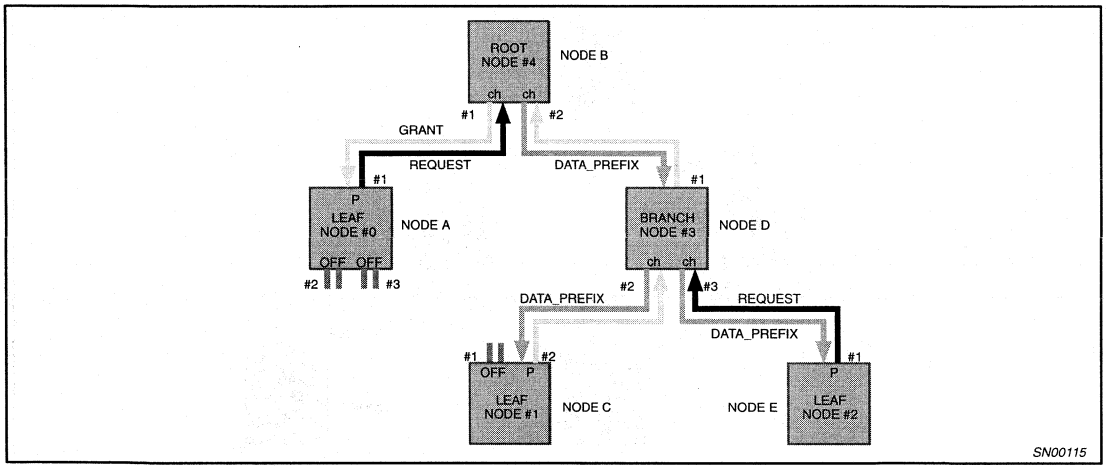

Figure 14. Arbitration Grant

3. Instead the root grants access to the first request (node A), while the other parent (node D) acknowledges the deny by withdrawing its request and passing on the deny.

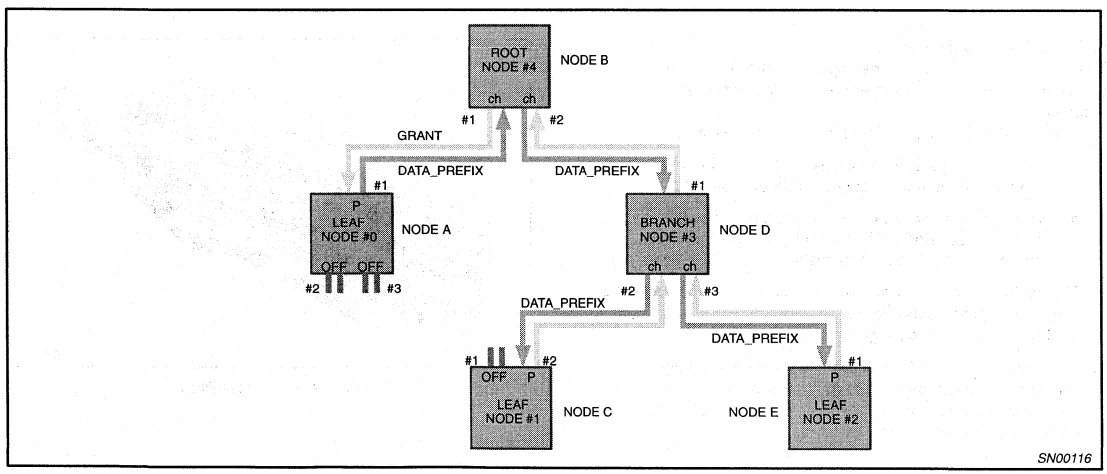

Figure 15. Data Prefix

4. This causes node E to withdraw its request. Simultaneously, node A receives the grant and, since it was the original requesting node[5], sends a data_prefix signal to warn all nodes that data is about to be sent.

5. If node A had children, they would have received a data_prefix when A started arbitration. If, however, one of node A's children had requested the bus first, node A would have done an internal deny and passed on the request to the root, and later on the grant when it received it.

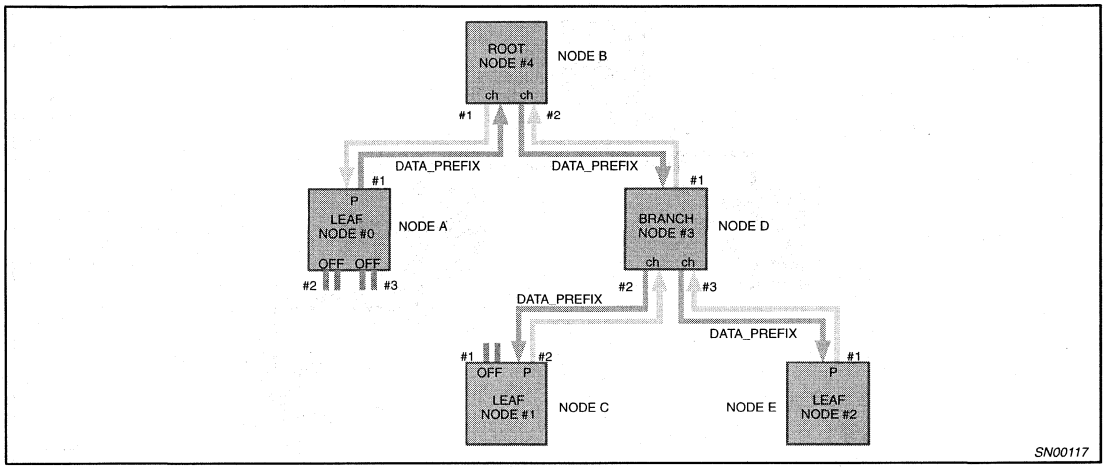

Figure 16. Start of Data Transmission

5. The parent of node A (the root in this case) sees the data prefix and withdraws the grant. At this point, the physical connections between all the nodes are now in the same state and pointed away from the node that won the arbitration. This allows the unused second signal to be turned around and used as a strobe to time the transmission of data.

5.3.2 Cable Media Interface

The cable media interface is the implementation of a physical connection. There are three major parts of the cable media interface:

1. The electrical interface to the cable, which consists of:
   a. Two low voltage, low current bidirectional differential signals to carry clocked packet data or arbitration signals.
   b. Power pair that provides the current needed by the physical layer to repeat signals. Nodes can either source or sink current, and there can be multiple power sources on a bus.
2. The cable connectors, which are small and rugged and provide 6 electrical contacts plus a shield as shown in Figure 17. The hole for the socket must be roughly 6 mm by 11 mm.
3. The cable media itself, which has two well shielded signal pairs with relatively high-impedance (meaning that little power is needed to drive an adequate signal), and one relatively low impedance pair for power.

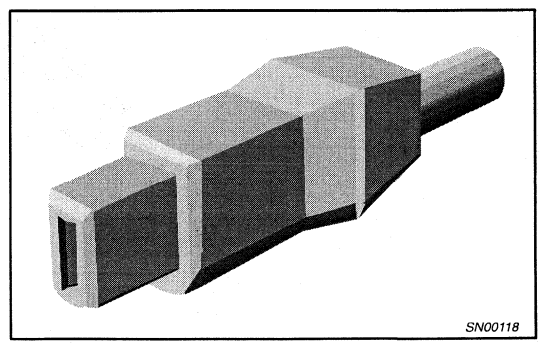

Figure 17. Cable Plug

5.4 Backplane Physical Layer and Arbitration

The backplane environment is a multidrop, very tightly controlled transmission line. There are two signals: Sbus_Data and Sbus_Strb which are shared among all nodes on a broadcast bus.

The backplane environment does not have the initialization requirements of the cable environment since the topology is fixed as a broadcast bus (no repeaters) and physical addresses may be set by the host backplane using its built-in slot identifier mechanism. If the backplane does not provide such a slot identifier mechanism, then the serial bus shall support some method for determining a unique arbitration number (i.e., hardwiring the address).

The backplane access method is bit-wise arbitration on a dominant-mode media. It depends on two assumptions: (1) if any node asserts the bus, then all nodes perceive the bus as asserted after a certain length of time ("wired-or" and "open-collector" are other names for this); and (2) each node has a guaranteed unique arbitration number. The procedure followed by competing nodes is:

```
START
wait for SBUS_DATA and SBUS_STRB to remain unasserted for a fixed period (a gap);
assert SBUS_STRB;
for each bit in the arbitration sequence {
   if the arbitration bit is a one {
      assert SBUS_DATA;
      wait eight base rate bit times (an arbitration symbol period); }
   else {
      release SBUS_DATA;
      wait five base rate bit times (the sample time) and sample SBUS_DATA;
      if SBUS_DATA is asserted {
         lost arbitration,
         wait three base rate bit times (the hold time);
         release SBUS_STRB and go back to START }
   }
won arbitration, release SBUS_DATA and continue to assert SBUS_STRB;
begin packet transmission
```

ACKNOWLEDGEMENTS

The P1394 working group has been blessed with unusually good working relationships. The author is particularly grateful to David James and David Gustavson for sticking with the development since its beginnings. Mr. James and Dan O'Connor have been the primary contributors to the link and transaction protocols. The physical layer is largely the work of Roger Van Brunt with the able assistance of Florin Oprescu. The cable environment PMD development has been led by Andy Carter.

REFERENCES

[1] *High Performance Serial Bus,* IEEE P1394 Draft 6.5, December 1993.

[2] *Scalable Coherent Interface,* IEEE Std. 1596, IEEE Standards Press, 1991

(All P1394 standards drafts are available from the IEEE Computer Society at 201-371-0101 or via anonymous FTP from "ftp.apple.com.")

Universal Serial Bus (USB) standard

UNIVERSAL SERIAL BUS (USB) STANDARD

The Universal Serial Bus is a fast, bi-directional, isochronous, low cost, dynamically attachable serial interface. The USB bus was proposed by COMPAQ, DEC, IBM, Intel, Microsoft and Northern Telecom as a peripheral interconnect bus, minimizing the number of PC connectors, reducing the PC and peripheral's costs and easing the additions of peripherals to a PC.

This document contains excerpts from the USB specifications. Complete and updated USB Specifications can be downloaded from the internet USB Home Page — http://www.teleport.com/~usb/

The motivation for the Universal Serial Bus comes from these interrelated considerations:

- **Connection of the PC to the telephone**
  The Universal Serial Bus provides an ubiquitous link that can be used across a wide range of PC to telephone interconnects.
- **Ease of use**
  The USB supports transfer rates up to 12 Mbs for the real-time data of voice, audio, and compressed video.

  The USB offers protocol flexibility for mixed-mode isochronous data transfers and asynchronous messaging. The USB simplifies I/O interfaces by allowing plug and play of keyboard, mouse, joystick. Self identifying of peripherals and automatic mapping of function to driver.
- **Port expansion**
  The USB supports up to 127 physical devices and allows the proliferation of peripherals such as telephone/fax/modem adapters, answering machines, scanners, PDA's, keyboards, mice, etc.
- **Robustness**
  Signal integrity is enhanced by using differential drivers, receivers and shielding. CRC protection over control and data fields. Error handling/fault recovery mechanism built into protocol. Self-recovery in protocol, using time-outs for lost or broken packets. Support for identification of faulty devices.

The range of data traffic workloads that can be serviced over a Universal Serial Bus is shown below. As can be seen, a 12 Mbs bus comprehends the mid-speed and low-speed data ranges.

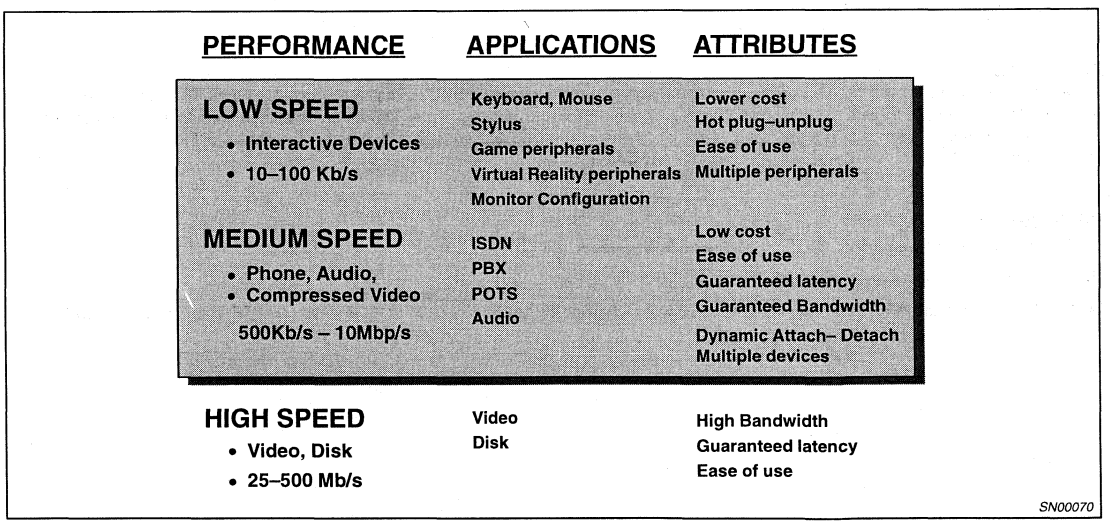

Figure 1. The USB can be used in low- and medium-speed applications.

Universal Serial Bus (USB) standard

Bus Topology Overview

The USB is a cable bus that supports data exchange between a host computer and a wide range of simultaneously accessible peripherals. The attached peripherals share USB bandwidth through a host scheduled token based protocol. The bus allows peripherals to be attached, configured, used, and detached while the host and other peripherals are in operation. This is referred to as dynamic (or hot) attachment and removal.

The Universal Serial Bus connects USB devices with the USB host. The USB physical interconnect is a tiered star topology. A hub is at the center of each star. Each wire segment is a point-to-point connection between the host and a hub or function, or a hub connected to another hub or function.

There is only one **host** in any USB system. The USB interface to the host computer system is referred to as the host controller. The host controller may be implemented in a combination of hardware, firmware, or software. A root hub is integrated within the host system to provide one or more attachment points.

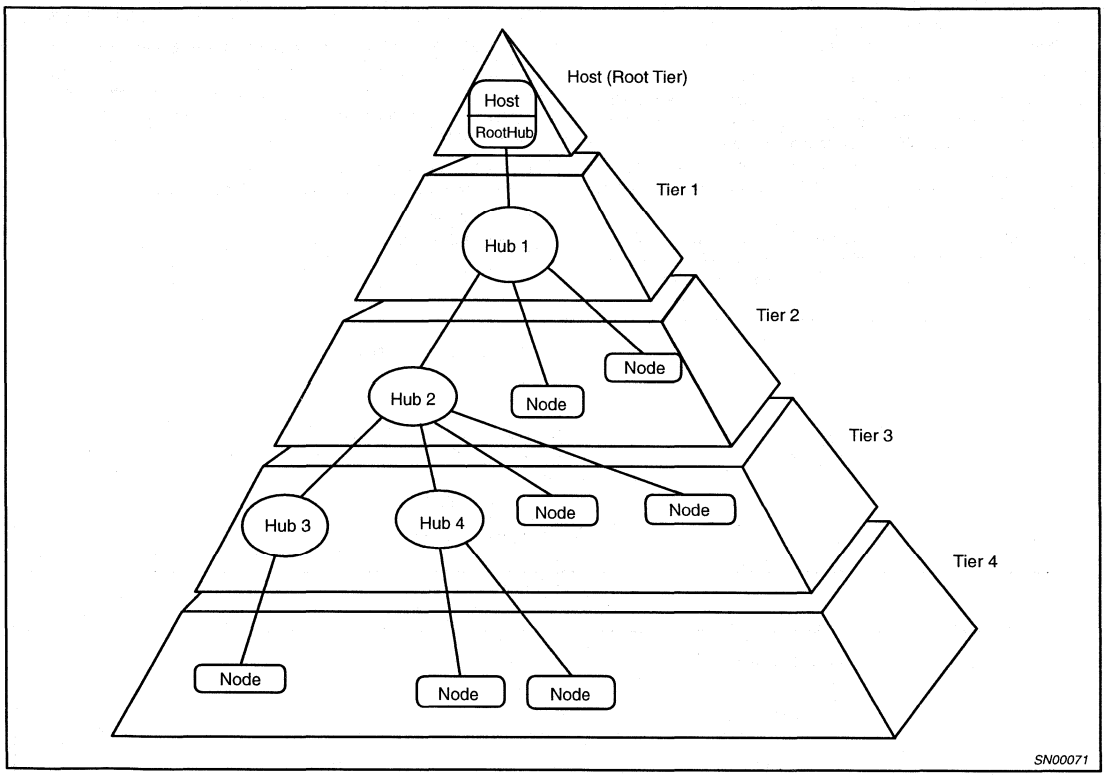

Figure 2. Bus Topology

Universal Serial Bus (USB) standard

USB Hubs and Functions Device Descriptions

Two major divisions of device classes exist: hubs and functions. Only hubs have the ability to provide additional USB attachment points. Functions provide additional capabilities to the host.

Hubs are a key element in the plug-and-play architecture of USB. Figure 3 shows a typical hub. Hubs serve to simplify USB connectivity from the user's perspective and provide robustness at low cost and complexity.

Hubs are wiring concentrators and enable the multiple attachment characteristics of USB. Attachment points are referred to as ports. Each hub converts a single attachment point into multiple attachment points. The architecture supports concatenation of multiple hubs.

The upstream port of a hub connects the hub towards the host. Each of the other downstream ports of a hub allows connection to another hub or function. Hubs can detect attach and detach at each downstream port and enable the distribution of power to downstream devices. Each downstream port can be individually enabled and configured as either full or low speed. The hub isolates low speed ports from full speed signaling.

A hub consists of two portions: the Hub Controller and the Hub Repeater. The repeater is a protocol controlled switch between the upstream port and downstream ports. It also has hardware support for reset and suspend/resume signaling. The controller provides the interface registers to allow communication to/from the host. Hub specific status and control commands permit the host to configure a hub and to monitor and control its ports.

Functions

A function is a USB device that is able to transmit or receive data or control information over the bus. A function is typically implemented as a separate peripheral device with a cable that plugs into a port on a hub. However, a physical package may implement multiple functions and an embedded hub with a single USB cable. This is known as a compound device. A compound device appears to the host as a hub with one or more permanently attached USB devices.

Each function contains configuration information that describes its capabilities and resource requirements. Before a function can be used, it must be configured by the host. This configuration includes allocating USB bandwidth and selecting function specific configuration options.

Examples of functions are:

- Locator device such as a mouse, tablet, or light pen.
- Input device such as a keyboard.
- Output device such as a printer.
- Telephony adapter such as ISDN.

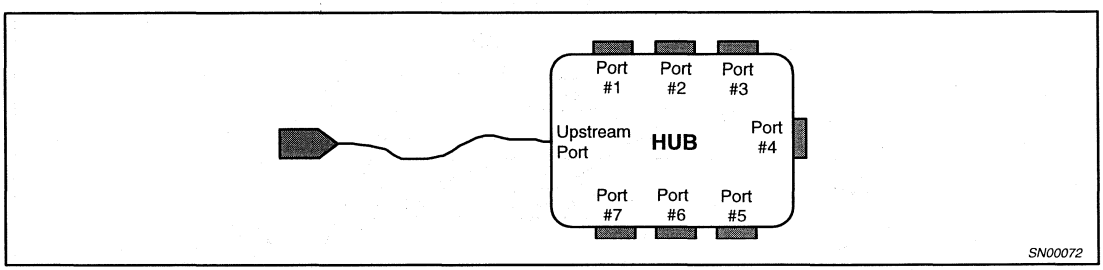

Figure 3. A Typical Hub

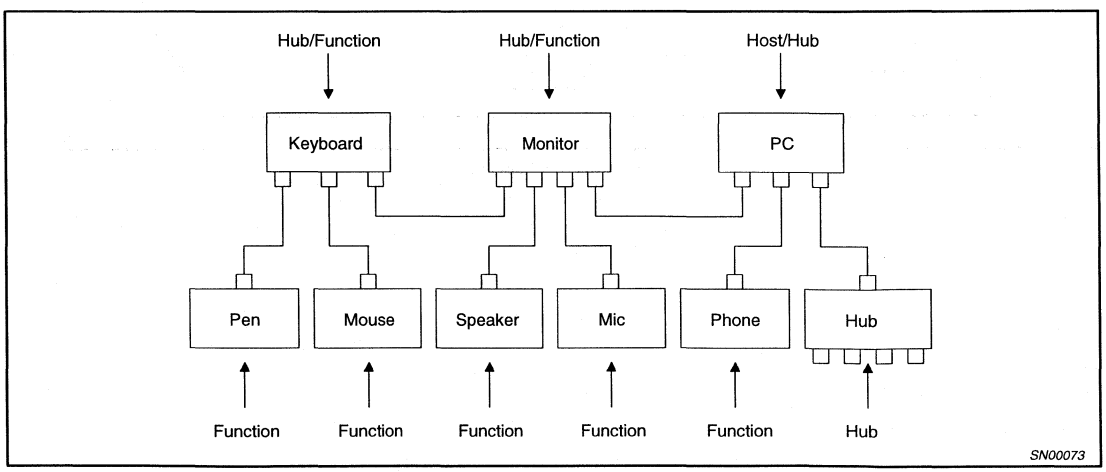

Figure 4. Hubs in a Desktop Computer Environment

USB Host: Hardware and Software

The USB Host interacts with USB devices through the host controller. The host is responsible for the following:

- Detecting the attachment and removal of USB devices
- Managing control flow between the host and USB devices
- Managing data flow between the host and USB devices
- Collecting status and activity statistics
- Providing a limited amount of power to attached USB devices

USB system software on the host manages interactions between USB devices and host-based device software. There are five areas of interactions between USB system software and device software, they are:

- Device enumeration and configuration
- Isochronous data transfers
- Asynchronous data transfers
- Power management
- Device and bus management information

Whenever possible, USB software uses existing host system interfaces to manage the above interactions. For example, if a host system uses Advanced Power Management (APM) for power management, USB system software connects to the APM message broadcast facility to intercept suspend and resume notifications.

Bus Protocol

All bus transactions involve the transmission of up to three packets. Each transaction begins when the host controller, on a scheduled basis, sends a USB packet describing the type and direction of transaction, the USB device address, and endpoint number. This packet is referred to as the Token Packet. The USB device that is addressed selects itself by decoding the appropriate address fields. In a given transaction, data is transferred either from the host to a device or from a device to the host. The direction of data transfer is specified in the token packet. The source of the transaction then sends a Data Packet or indicates it has no data to transfer. The destination in general responds with a Handshake Packet indicating whether the transfer was successful.

The USB data transfer model between a source or destination on the host and an endpoint on a device is referred to as a pipe. There are two types of pipes: stream and message. Stream data has no USB defined structure while message data does. Additionally, pipes have associations of data bandwidth, transfer service type, and endpoint characteristics like directionality and buffer sizes. Pipes come into existence when a USB device is configured. One message pipe, Control Pipe 0, always exists once a device is powered in order to provide access to the device's configuration, status, and control information.

The transaction schedule allows flow control for some stream mode pipes. At the hardware level, this prevents buffers from underrun or overrun situations by using a NACK handshake to throttle the data rate. The token for a NACK'ed transaction is reissued when bus time is available. The flow control mechanism permits the construction of flexible schedules that accommodate concurrent servicing of a heterogeneous mix of stream mode pipes. Thus, multiple stream mode pipes can be serviced at different intervals and with packets of different sizes.

ELECTRICAL SPECIFICATIONS

USB transfers signal and power over a four wire cable, shown in below. The signaling occurs over two wires and point-to-point segments. The signals on each segment are differentially driven into a cable of 90Ω intrinsic impedance. The differential receiver features input sensitivity of at least 200 mV and sufficient common mode rejection.

There are two modes of signaling. The USB full speed signaling bit rate is 12 Mbs. A limited capability low speed signaling mode is also defined at 1.5 Mbs. The low speed method relies on less EMI protection. Both modes can be simultaneously supported in the same USB system by mode switching between transfers in a device transparent manner. The low speed mode is defined to support a limited number of low bandwidth devices such as mice, since more general use would degrade the bus utilization.

The clock is transmitted encoded along with the differential data. The clock encoding scheme is NRZI with bit stuffing to ensure adequate transitions. A SYNC field precedes each packet to allow the receiver(s) to synchronize their bit recovery clocks.

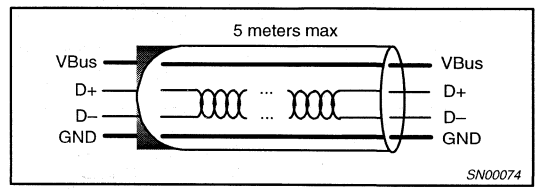

Figure 5. USB Cable

The cable also carries VBus and GND wires on each segment to deliver power to devices. VBus is nominally +5 V at the source. USB allows cable segments of variable lengths up to several meters by choosing the appropriate conductor gauge to match the specified IR drop and other attributes such as device power budget and cable flexibility. In order to provide guaranteed input voltage levels and proper termination impedance, biased terminations are used at each end of the cable. The terminations also permit the detection of attach and detach at each port and differentiate between full speed and low speed devices.

USB Driver Characteristics

The USB uses a differential output driver to drive the USB data signal onto the USB cable. The static output swing of the driver in its low state must be below the V_{OL} of 0.3 V with a 1.5 kΩ load to 3.6 V and in its high state must be above the V_{OH} of 2.8 V with a 15 kΩ load to ground. The output swings between the differential high and low state must be well balanced to minimize signal skew. Slew rate control on the driver is required to minimize the radiated noise and cross talk. The driver's outputs must support three-state operation to achieve bi-directional half duplex operation. High impedance is also required to isolate the port from downstream devices that are being hot inserted or which are connected but powered down. The driver must tolerate a voltage on the signal pins of -0.5 V to 3.8 V with respect to local ground reference without damage. It must tolerate this voltage for 10.0 µs while the driver is active and driving, and tolerate the condition indefinitely when the driver is in its high impedance state.

Universal Serial Bus (USB) standard

Full Speed (12 Mbs) Driver Characteristics

A full speed USB connection is made through a shielded, twisted pair cable with a characteristic impedance (Z_0) of 90Ω ±15% and a maximum length of 5 meters. The impedance of each of the drivers must be between 29Ω and 44Ω. The data line rise and fall times must be between 4 ns and 20 ns, smoothly rising or falling (monotonic), and be well matched to minimize RFI emissions and signal skew.

For a CMOS implementation, the driver impedance will typically be realized by a CMOS driver with an impedance significantly less than this resistance with a discrete series resistor making up the balance. Figure 6 shows an example of how a full speed driver might be done using two identical CMOS buffers which have an output impedance between 3Ω and 15Ω and two series resistors of 27Ω. Figure 7 shows the full speed driver signal waveforms.

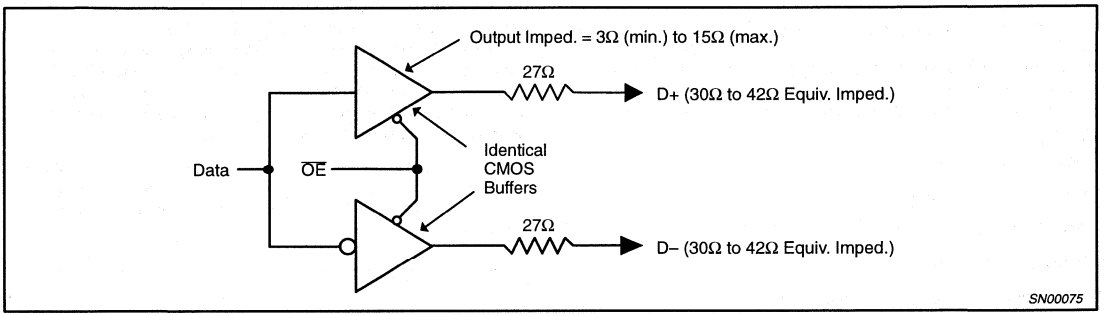

Figure 6. Example Full Speed CMOS Driver Circuit

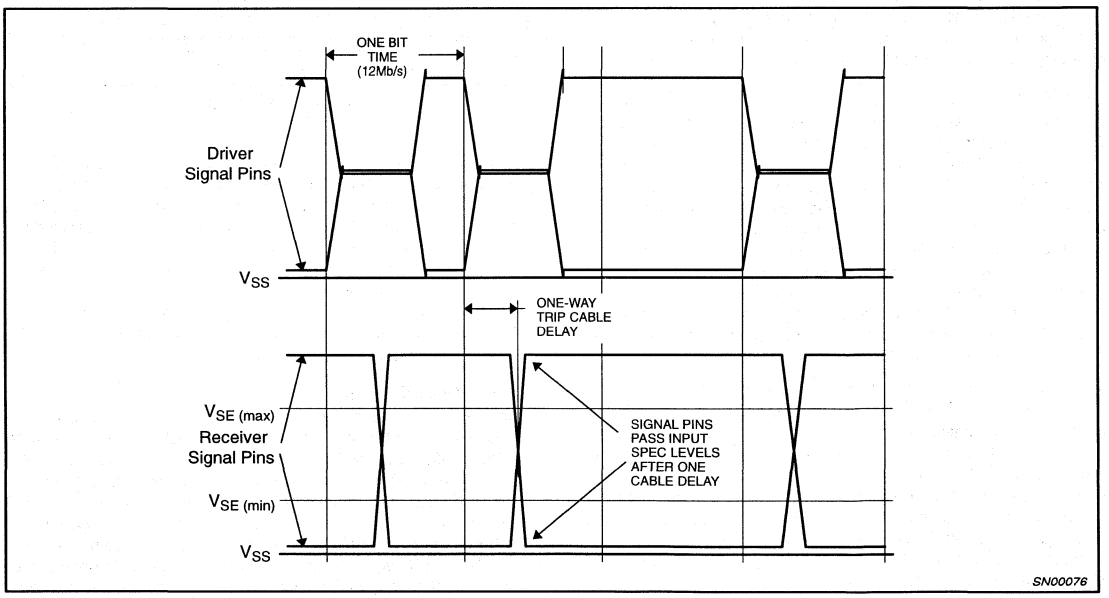

Figure 7. Full Speed Driver Signal Waveforms

Low Speed (1.5 Mbs) Driver Characteristics

A low speed USB connection is made through an unshielded, untwisted wire cable a maximum of 3 meters in length. The rise and fall time of the signals on this cable must be greater than 75 ns to keep RFI emissions under FCC class B limits, and less than 300 ns to limit timing delays and signaling skews and distortions. The driver must reach the specified static signal levels with smooth rise and fall times, and minimal reflections and ringing when driving the cable (see Figure 8). This cable and driver are used only on network segments between low speed devices and the ports to which they are connected.

Driver Usage

Full speed buffers are used on the upstream ports (towards the host) of all hubs and full speed functions. All devices with hubs must be full speed devices. A full speed driver will be used to send data at both and low speed data rates. However, the signaling always uses full speed signaling conventions and edge rates. Running at low speed data rates does not change the driver's characteristics.

Low speed buffers are used on the upstream ports of low speed functions. The downstream ports of all hubs (including the host) are required to be capable of both driver characteristics, such that any type of device can be plugged in to these ports . Low speed drivers only send at the low speed data rate using low speed signaling conventions and edge rates.

Receiver Characteristics

A differential input receiver must be used to accept the USB data signal. The receiver must feature an input sensitivity of at least 200 mV when both differential data inputs are in the range of at least 0.8 V to 2.5 V with respect to its local ground reference. This is called the common mode input voltage range. Proper data reception is also required when the differential data lines are outside the common mode range, as shown in Figure 9. The receiver must tolerate static input voltages between –0.5 V to 3.8 V with respect to its local ground reference without damage. In addition to the differential receiver, there must be a single-ended receiver for each of the two data lines. The receivers must have a switching threshold between 0.8 V and 2.0 V (TTL inputs). It is recommended that the single-ended receiver have some hysteresis to reduce its sensitivity to noise.

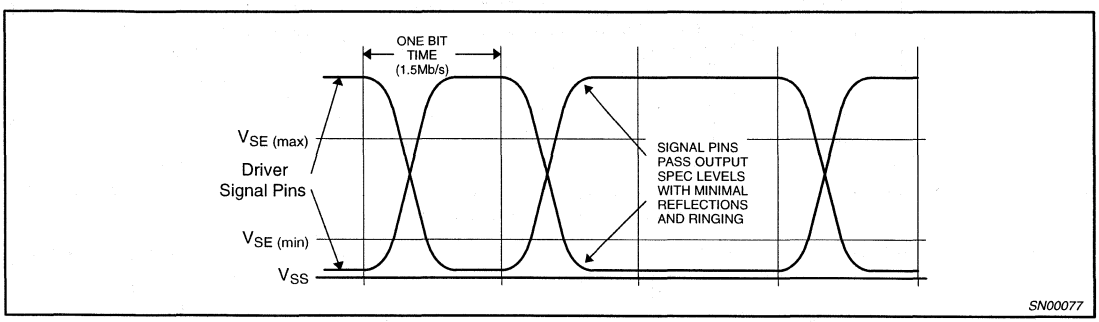

Figure 8. Low Speed Driver Signal Waveforms

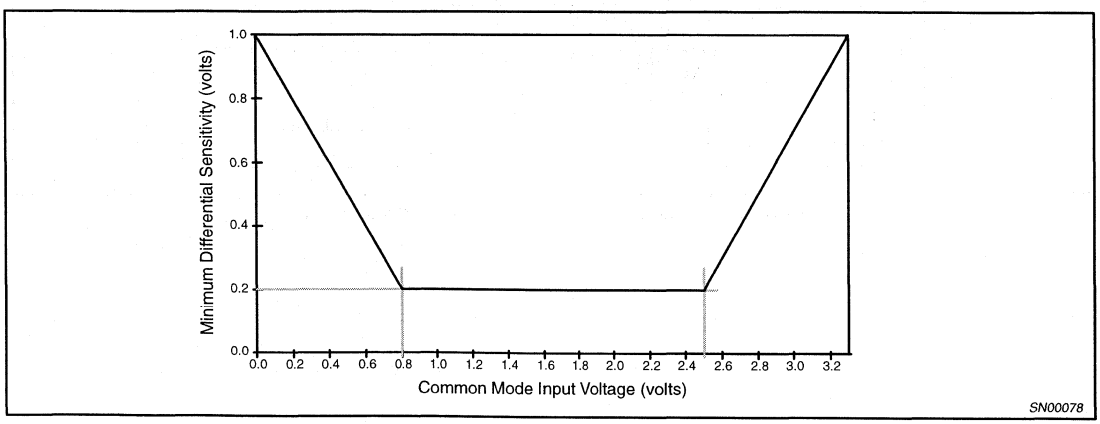

Figure 9. Differential Input Sensitivity Over Entire Common Mode Range

Universal Serial Bus (USB) standard

Signal Termination

The USB is terminated at the hub and function ends. Full speed and low speed devices are differentiated by the position of the pull-up resistor on the downstream end of the cable. Full speed devices are terminated as shown in Figure 10 with the pull-up on the D+ line. Low speed devices are terminated as shown in Figure 11 with the pull-up on the D– line.

The pull-up terminator is a 1.5 kΩ ±5% resistor tied to a voltage source between 3.0 V and 3.6 V referenced to the local ground. The pulldown terminators are resistors of 15 kΩ ±5% connected to their local ground.

Power Distribution and Management

Each USB segment provides a limited amount of power over the cable. The host supplies power for use by USB devices that are directly connected. In addition, any USB device may have its own power supply. USB devices that rely totally on power from the cable are called bus-powered devices. In contrast, those that have an alternate source of power are called self-powered devices. A hub also supplies power for its connected USB devices. The architecture permits bus-powered hubs within certain constraints of topology. Self-powered devices must implement prescribed power decoupling safety mechanisms.

A USB host has a power management system which is independent of the USB. USB system software interacts with the host's power management system to handle system power events such as SUSPEND or RESUME. Additionally, USB devices can carry USB-defined power management information which allow them to be power managed by system software or generic device drivers.

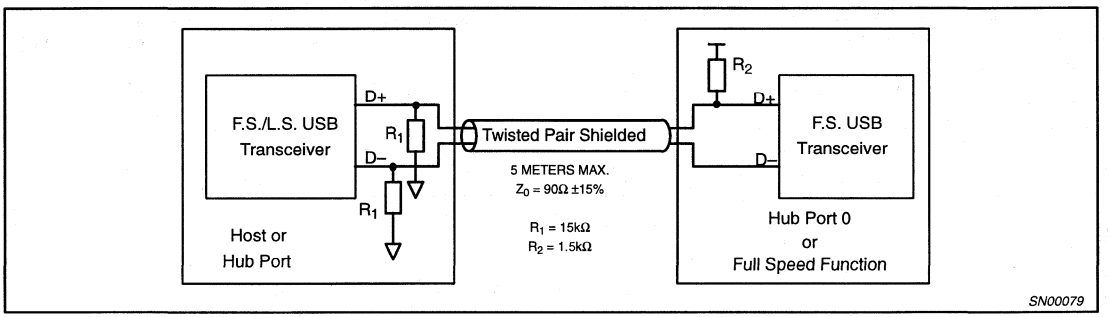

Figure 10. Full Speed Device Cable and Resistor Connections

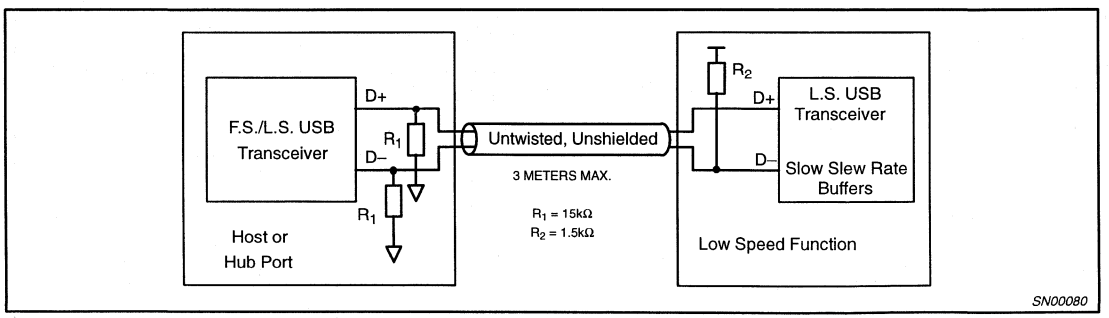

Figure 11. Low Speed Device Cable and Resistor Connections

Contact addresses

Requests for various standards specifications can be directed to the following:

CCIR

The International Radio Consultative Committee
International Telecommunications Union
Place Des Nations
CH-1211 Geneva
20 Switzerland

Telephone: (011) 4122 730 5800

CCITT

The International Telephone and Telegraph Consultative Committee
International Telecommunications Union
Place Des Nations
CH-1211 Geneva
20 Switzerland

Telephone: (011) 4122 730 5851

EBU

European Broadcasting Union
The Technical Center of the EBU
Ancienne Route 17A
P.O. Box 67
CH-1218 Grand-Saconnex (Geneva) 20
Switzerland

Telephone: (041) 22 7172705

EIA

Electronic Industries Association
2500 Wilson Blvd.
Arlington, VA 22201

Telephone:
Headquarters: (703) 907 7500
Standards: (800) 854 7179

IEEE

Institute of Electrical and Electronics Engineers

Headquarters:
345 East 47th Street
New York, NY 10017

Telephone: (212) 705 7900

Standards Office:
IEEE Service Center
P.O. Box 1331
Piscataway, NJ 00855

Telephone: (908) 981 0060

SMPTE

Society of Motion Picture and Television Engineers
595 W. Hartsdale Avenue
White Plains, NY 10607

Telephone: (914) 761 1100

Video glossary

DEFINITION OF TERMS

AC-COUPLED – A means by which the constant, or DC component, of a signal is removed, usually by passing the signal through a capacitor.

AM – Amplitude Modulation (AM) is a modulation process by which the amplitude of the carrier signal is scaled in proportion to the modulation signal (which is the signal which carries the content). AM modulation is used for the video portion of the transmitted TV signal for both NTSC and PAL standards.

Anti-Top Flutter Pulse – Disables the phase detector during equalization and framing times.

APL – Average Picture Level. The mean or average signal level during the active video period. It is expressed as a percentage of the difference between blanking and peak white (O and 100 IRE).

AV – Audio Video

Back Porch – That section of the video waveform between the end of horizontal sync and the beginning of active video. The color burst signal is inserted during this period.

Bandwidth – The frequency range over which an input signal of uniform amplitude will be passed with uniform output (within a specified limit).

Baseband Video – Same as Composite Video (CVS or CVBS)

Black Burst – Black Burst (Color Black) is a composite video signal containing sync information, color reference (burst) and setup information (in the case of NTSC). Black Burst is often used as the studio reference to facilitate synchronization of all the devices in the system.

Black Level – The signal level which represents black picture intensity. For NTSC, this level is 7.5 IRE (also called Setup) and for PAL this level is 0 IRE.

Black Level Noise – Very similar to a white spot noise spike except it is in the opposite or black level direction.

Blanking Level – The video level immediately preceding or following horizontal sync exclusive of the active video region. The video level for blanking is defined as 0 IRE. In the case of PAL, blanking level and black level are the same.

Breezeway – That portion of the Back Porch between the end of horizontal sync and the beginning of the color burst.

CIF – Picture format used in Video Conferencing. CIF has 352 H × 288 V luminance pixels, and 176 H × 144 V chrominance pixels. QCIF is a similar picture format with one-quarter the size of CIF.

Color Difference Signals – The chrominance information of a video signal, expressed as the combination of two orthogonal axis signals, B-Y (also called U or Cb) and R-Y (also called V or Cr). These signals contain no luminance (Y) information.

Composite Video – Composite video (CVS/CVBS) signal carries video picture information for color, brightness and synchronizing signals for both horizontal and vertical scans. Sometimes referred to as "Baseband Video".

CTV – Color Television

CVBS or CVS – Same as composite video.

Data Slicing – The process of extracting digital data from an incoming, non-TTL signal.

DC Coupled – An electrical connection passing both the DC component as well as the AC component of a signal.

DC Restoration – The process of setting the DC level of a video signal to a defined level. DC restoration is generally applied during the back porch region of the video signal by means of a clamp pulse applied to the restoration circuit at that point of the signal.

DCT – Discrete Cosine Transform is used to transform a time-domain or space-domain signal to a pseudo-frequency domain signal. This is a lossless, linear, invertible transformation used in video compression algorithms.

Demodulation – The process by which the original signal content is recovered from the modulated carrier. In color television, demodulation may additionally refer to the recovery of the color difference signals from the modulated chroma subcarrier.

Equalization Pulses – The pulses existing before and after the vertical pulse during the vertical interval. These are half horizontal in length and are inserted to effect the half-line offset in vertical sync required for interlace.

Field – For interlaced video the total picture is divided into two fields, one even and one odd each containing one half of the total vertical information. Each field takes one sixtieth of a second (one fiftieth for PAL) to complete. Two fields make a complete frame of video.

FM – Frequency modulation is the method by which the modulation signal which contains the information is used to vary the frequency of the carrier. For NTSC and PAL video, FM modulation is used to transmit the sound portion of the program.

Frame – One frame (two fields) of video contains the full vertical interlaced information content of the picture. For NTSC this consists of 525 lines and for PAL a frame is consisted of 625 lines.

Front Porch – The section of the video signal that lies between the end of active video and the beginning or leading edge of horizontal sync.

Full Field Teletext – In this mode, Teletext information is transmitted over, virtually, all available TV lines.

Gamma – Cathode ray tubes (CRTs) do not have a linear relationship between brightness and the input voltage applied. To compensate for this non-linearity, a pre distortion or gamma correction is applied, generally at the camera source. A value of gamma equal to 2.2 is typical, but can vary for different CRT phosphors.

Genlock – Two composite video signals can by phase locked to each other by synchronizing both the composite sync and color burst of the two signals. This process is called genlock.

Ghost Rows – These are the rows that are specified by the "row address field" of the "page header" but do not get displayed. These are rows 24 to 31. Sometimes referred to as "Extension Packets", these rows carry miscellaneous control information. (Page extension for Telesoftware, linked pages, higher display level, etc.)

GOB – Group of Blocks. A picture is divided into groups of blocks, which are further divided into Macroblocks that are, in turn, divided into blocks. A block is the basic unit of compression in Videoconferencing.

Harmonic Distortion – A distortion added to a signal which consists of multiples or harmonics of that signal which were not present in the original. System non-linearity can contribute to this distortion.

Video glossary

Huffman Coding/Entropy Coding – A lossless compression scheme that is based on probabilities of occurrence of symbols at the source. Compression is achieved by assigning shorter-length codes to higher probability symbols.

Horizontal Blanking – The sum of the front porch, horizontal sync and back porch periods, i.e. the entire period from the end of active video to the beginning of active video on a line.

Horizontal Sync – A negative active pulse of 287mv amplitude (300mv for PAL) inserted in the composite video signal. This pulse is extracted by the monitor (or receiving system) and used to horizontally synchronize or define the left hand side of the image.

Hue – Tint or color such as red, pink, yellow, etc.

Hum – An undesirable superimposition of 60Hz (50Hz in Europe) power energy into the signal content.

H.261 – Video compression standard; serves the need for videoconferencing over ISDN (International Services Data Network).

H.263 – Video compression standard; serves the need for videoconferencing over POTS (Plain Old Telephone System).

Intercarrier Sound – The means by which sound is separated from the modulated television signal by the use of a sound carrier to beat against the video carrier. This produces a 4.5MHz signal which contains the audio portion of the television signal.

Interlace – A method to give a higher apparent number of lines on the television CRT screen. One television frame is written on the CRT with television lines of the "even field" placed in between those of the "odd field".

IQ Signals – Similar to the color difference signals (R-Y), (B-Y) but using different vector axis for encoding or decoding. Used by some USA TV and IC manufacturers for color decoding.

IRE – 1/140 of a volt which is the peak to peak amplitude of a video signal from the bottom of sync to the top of peak white. Sync and burst amplitude is defined as 40 IRE units, while active video is 100 IRE Max. The unit was originally defined by the Institute of Radio Engineers, hence the name.

JPEG – Joint Pictures Expert Group
A compression/decompression standard used for static images, which, depending if quantizing methods are applied, may or may not produce loss of information. A combination of DCT (discrete cosine transforms), quantization, zig-zag scanning and huffman coding techniques are used in the compression/decompression process.

Linear Distortion – Distortions which are independent of amplitude.

Luminance – The brightness or black and white content of a picture. No hue or saturation components exist. Luminance is also referred to by the letter Y and is defined as a sum of scaled red, green and blue primaries by the formula:
Y=.30R+.59G+.11 B.

Modulation – The process whereby a signal containing information is used to vary some characteristic of a carrier. In the case of AM the carrier amplitude is varied, in the case of FM the carrier frequency is varied and in the case of chroma modulation, the phase of the carrier (called subcarrier in this case) is modulated.

Motion Estimation – A process used in Video Compression to estimate the motion of objects between two successive encoded frames.

MPEG – Motion Pictures Expert Group
A compression/decompression standard used for moving image sequences. The same techniques are used as were for JPEG, quantizing is always used, therefore the technique is always lossy. Both forward and backward prediction frames (P and B frames) are generated and referenced to an index fram (I frame).

MPEG 1 – Serves the need for storage, retrieval and decoding of compressed digital video. Provides VCR Quality video at a bit-rate of about 1.5 Mbits/sec over read channels of very low error-rate.

MPEG 2 – Provides broadcast quality video at a max bit-rate of about 15 Mbits/sec. Serves the need for video-on-demand broadcasting, editing, recording and playback of digital video.

NABTS – North American Broadcasting Teletext *Specifications. **Note that this is** not a standard.*

This document specifies both the acquisition protocol and the display format. The display format is NAPLPS.

NAPLPS – North American Presentation Level Protocol Syntax. Again, this is not a display standard. It applies to both Teletext and Videotex services.

Non-Linear Distortion – These are distortions which are amplitude dependent. Differential gain and phase measurements are used to measure these distortions.

NTSC – National Television Standards Committee (USA).

Page Header – This is equivalent to Row 0. Carry Control information about this page.

PAL – Phase Alternate Line. A television standard used in Europe and other countries which alternates the relationship of the color axes on a line by line basis so that color modulation errors can be canceled out.

Peak White – Maximum amplitude signal corresponding to the maximum brightness of the video screen.

Peritel – An audio/video connector standard for European TV receivers. Serves the same purpose as AV connector on some of the newer American TV sets.

Quadrature AM – Refers to the process by which two different modulation signals each modulate carriers of the same frequency but which are 90 degrees out of phase. The summed signals can be added together for transmission and can be recovered at the receiver end if they are demodulated 90 degrees apart. This is the process used to modulate chrominance information onto the color subcarrier of a video signal.

Quadrature Distortion – Distortion which results if the sidebands of a vestigial sideband transmission are uneven or asymmetrical. If synchronous decoding is used instead of envelope detection, this distortion can be minimized.

RF Video – System used on standard Television transmissions via an antenna or cable system. Baseband video is amplitude modulated on an RF carrier.

RGB – Three separate signals of Red, Green and Blue used to produce a color image.

Run-length Coding – In a list of numbers, Run-length coding replaces consecutive zeros with a Run-length. Each non-zero number then, is represented by a pair of numbers, a Run-length and a level. The Run-length refers to the number of zeros preceding the non-zero number. Run-length coding is applied to DCT coefficients after they have been zig-zag scanned, prior to entropy coding.

R-Y, G-Y, B-Y – Red, Green or Blue signals without the luminance (-Y).

Video glossary

Sandcastle Pulse – Multilevel pulse generated by the horizontal processor and the vertical deflection circuit. This pulse contains gating pulse and blanking signal information for use by the color decoder and the video control circuits.

Saturation – A characteristic describing color amplitude or intensity. A color of a given hue may consist of low or high saturation value which relates to the vividness of the color.

SECAM – Sequential Color and Memory system. TV color system used primarily in France and the USSR.

Setup – A video level which, for NTSC, defines black level and which is 7.5 IRE above blanking. Pal does not have setup.

SIF – Picture format used in Video Conferencing. SIF has 352 H × 240 V luminance pixels, and 176 H × 120 V chrominance pixels. QSIF is a similar picture format with one-quarter the size of SIF.

SRM – Service Reference Model of NAPLPS. It is a skeleton NAPLPS, specifying a low level type display in order to allow for easy implementation (256h × 200v pixels).

Subcarrier – The carrier used to convey chroma information within the composite video signal. The R-Y and B-Y color difference signals are modulated onto the subcarrier by a process of quadrature AM modulation. The frequency of the subcarrier signal is related to the odd half-line multiples of the horizontal frequency in such a manner as to allow the chrominance frequency spectrum to co-exist or interleave within the luminance spectrum.

Synchronous Detection – A process by which demodulation is performed by multiplying the signal by another signal generated by a oscillator which is locked to the original carrier. This is the method preferred over envelope detection.

Teletext – One way broadcast of digital information.

Termination – Unless proper source and termination impedance's are presented to a transmission line, such as a co-ax cable, undesirable reflections and ringing can occur. Video transmission cable typically has a characteristic impedance of 75 ohms and should be terminated by same.

Unmodulated – Refers to the pure carrier frequency with no AM, FM, or Phase modulation imposed upon it. Also referred to as CW or continuous wave.

Vectorscope – An oscilloscope specifically designed to demodulate and display chroma as an x-y display of the decoded color with respect to the R-Y and B-Y (or I and Q) axis. Hue is displayed as the angle around the display, and saturation as the amount of displacement from the center.

Vertical Blanking Interval (VBI) – The time it takes the beam to fly back to the top of the screen in order to retrace the opposite field (odd or even). VBI is in the order of 20 TV (25 for PAL) lines. Teletext information is transmitted over 4 of these lines (lines 14-17).

Videotex – A two-way interactive system through which the user can communicate to a large, organized and secure, database through a telephone line using the TV as the display medium.

Waveform Monitor – An oscilloscope designed to measure the specific timings of a video signal.

World System Teletext (WST) – World System Teletext is based on the British teletext standard in which a one-to-one correspondence exists between transmitted characters,page memory, word addresses and the display screen character locations. Over 98% of the world's teletext decoders are WST compatible.

Y Signal – Luminance. Determines the brightness of each spot (pixel) on CRT screen either color or B/W systems, but not the color.

Zig-Zag Scanning – A process of converting a two-dimensional DCT coefficient block into a one-dimensional block that results in better energy-packing. Zig-zag scanning is used prior to run-length coding and entropy encoding.

Audio glossary

DEFINITION OF TERMS

AC-coupled – A means by which the constant, or DC (direct current) component of a signal is removed, usually by passing the signal through a capacitor.

ADC – Analog to Digital Converter. Device to translate analog voltages into an equivalent numerical representation.

AES/EBU – **A**udio **E**ngineering **S**ociety / **E**uropean **B**roadcasting **U**nion . Has become synonym for the professional digital audio data format used in broadcasting or recording environments. The signals are transmitted on one (unbalanced) or two wires (balanced) vs. ground. This is the professional version of the *IEC958* digital format with enhanced functionality.

Aliasing – Undesired (but hardly avoidable) artifacts that are created in the process of converting signals from the analog into the digital domain. They are caused by analog signal elements that are folded into the audible band during conversion (as described in the *Nyquist criteria*) .

Anti-Aliasing Filter – Building block in a digital audio system used to remove *Aliasing* artifacts.

BCC – A combination of Philips *Bitstream* and *Continuous Calibration* techniques (used in newer generation devices).

BCK – *Bitclock.*

Bitclock – One of the signals in the *I²S* or *LSB-justified* digital audio format. There has to be at least one bitclock per significant bit. To accommodate for different systems the data can be "padded" by an arbitrary number of additional bitclocks.

Bitstream – Conversion technique where a digital signal is represented by means of a stream of bits at a very high frequency (1-Bit conversion).

CC – Continuous Calibration.

CC-DAC – Analog to Digital Converter using the *Continuous Calibration.*

Channel Separation – Means by which the amount of *Crosstalk* between the left and the right audio channel is described.

Continuous Calibration – Technique used in newer Digital to Analog Converters (DACs) where the internal current sources that are used in the conversion process are continuously recalibrated to ensure very high accuracy output signals.

Crosstalk – Undesired amount of signal from one channel found in the other. Usually found as the Channel Separation value.

DAC – Analog to Digital Converter. Device to translate the digital (numerical) representation of a signal into an equivalent analog voltage.

Data – The signal line in a digital audio data bus like I²S that actually carries the data for the left or right channel. Every bit coincides with exactly one *Bitclock* while the *Word Select* signal indicates which channel the data is currently representing.

Digital Filter – Building block in a digital audio device that manipulates the digital data in some way. In the most general sense a Digital Filter can be used to perform any possible task. Popular examples for digital filter functions are volume control , tone control, de-emphasis, etc.

Dynamic Range – Means by which the difference between the largest possible signal and the smallest possible representable digital signal is measured. The maximum possible dynamic range of a digital system can be found to be 6dB*N, where N is the number of significant bits (i.e., 96 dB for a 16 bit system, 108 dB for 18 bits, etc.).

Full Scale Input Voltage – Analog Voltage that causes an *ADC* to output the maximum (full scale) digital value.

Full Scale Output Voltage – Analog Voltage that results when a *DAC* outputs the maximum digital value (full scale).

Fs – Sampling Frequency.

Fsys – *System Frequency / System Clock.*

I²C-Bus – **I**nter-**I**ntegrated-**C**ircuit-Bus. Bus system, invented by Philips and widely used in the industry, mainly as a medium to transmit control information between different ICs (Inter IC, e.g., to send data from a microcontroller to a sound controller chip). The format transports data on a 3 signal bus (*WS – Word Select, BCK - Bitclock* and *DATA*).

I²S-Bus – **I**nter **I**ntegrated-circuit **S**ound-Bus. Serial Digital Audio Format, introduced by Philips and widely used in the industry, where the most significant bit is transmitted **one** *Bitclock* **after** the *Word Select* signal changed status. The relevant bits (usually 16, 18 or 20 bit, but any number is possible) can be followed by any number of "idle" *Bitclocks* until the *Bitclock* changes status again. This format is supported by most of Philips Semiconductors Digital Audio Devices.

IEC958 – One wire (plus ground) serial Digital Audio Format. Can be found these days e.g. on medium to high quality CD-players as the digital output signal. Also referred to as *S/PDIF.*

LSB – The Least Significant Bit in digital data.

LSB-justified – Serial Digital Audio Format where the least significant bit is always transmitted **last** before the *Word Select* signal changes status. The relevant bits (usually 16, 18 or 20 bit) can follow any number of "idle" *Bitclocks.* Supported by most of Philips Semiconductors Digital Audio Devices.

Master Mode – The device generates its own *System Clock* that might be used to control other devices in the system.

MSB – The **M**ost **S**ignificant **Bi**t in digital data.

MSB-justified – Digital Audio Format where the most significant bit is always transmitted **first** after the *Word Select* signal changed status. The relevant bits (any number is possible) can be followed by any number of "idle" *Bitclocks* until the Word Select changes status again. Most popular example is *I²S.*

Noise Shaper – Building block (usually as part of a Digital Filter) in higher class devices to shift noise from the "in-band" range (i.e., within the audible frequencies) to the "out-of-band" range where it can be easily removed using inexpensive first order analog filters Post Filtering.

Nyquist criteria – Physical law, named after its finder Nyquist, that states that the digital representation of an analog signal will never contain any frequencies that are higher than half of the sampling frequency. Frequencies above the so-called Nyquist frequency will be folded back into the audible range and cause usually undesired artifacts (*Aliasing*).

Oversampling – Method to sample a signal at a higher frequency (usually a multiple of the desired sampling frequency *Fs.*

Audio glossary

Post Filtering – Analog Filter circuitry to remove "out-of-band" frequency left-overs at the output of a *DAC*. Depending on the quality of the digital filtering inside the digital device the analog post filtering can be as easy as a single pole RC filter or as complicated as a 3rd or even 4th order Opamp based filter network.

Resolution – Benchmark number related to the *Dynamic Range*. A device can be characterized either using the Resolution (usually in bits) or the dynamic range (usually given in dB).

Sampling Frequency – Number of times per second that an analog signal is probed and translated into a digital value (sampled). The value is given in Hz. Most common sampling frequencies for audio systems are 32 kHz, 44.1 kHz (CD standard) and 48 kHz (professional systems).

"S"-Format – Sony Digital Audio Format. Same as *LSB-justified* format.

Signal to Noise – Means by which a devices noise behavior is rated. The absolute output noise voltage is put into relation to a sinewave of known amplitude at the output (e.g., 0 dB or *Full Scale Output Voltage*).

Slave Mode – The device receives a *System Clock* from another device in the system so that its timing is externally controlled.

S/N – *Signal to Noise*.

S/PDIF – Sony/Philips Digital Interface Format.

SYSCLK – *System Clock*.

System Clock – Signal needed in almost all digital systems to operate ADCs, DACs or other Digital Audio devices. The signal is generally used for clocking internal circuitry and in most cases a multiple of the *Bitclock* signal.

System Frequency – *System Clock*.

THD – **T**otal **H**armonic **D**istortion. Means by which a device's signal processing linearity is rated. It assumes the input of a perfect sinewave and takes in account the sum of all harmonics generated through nonlinearity in the signal processing chain and put them in relation to the amplitude of the original sinewave. Compare to *(THD+N)/S*.

(THD+N)/S – **T**otal **H**armonic **D**istortion plus **N**oise To **S**ignal Ratio. Means by which a device's signal processing linearity and noise behavior is rated. It assumes the input of a perfect sinewave and takes in account the sum of all harmonics generated through nonlinearity in the signal processing chain as well as all the additional noise introduced and puts it in relation to the amplitude of the original sinewave. Compare to *THD*.

Up-Sampling Filter – Building block *(Digital Filter)* in a digital audio system used to sample an already sampled signal at a higher frequency. This moves undesired artifacts to higher frequencies where they can easily be removed using inexpensive filters.

WS – Word Select signal. This signal indicates if *Data* and *Bitclock* are currently valid for representation of the left or right channel (used e.g., in the I^2S or LSB-justified formats). The frequency of this signal is equal to the *Sampling Frequency*.

APPLICATION INFORMATION

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Crystal specifications and applications

Philips video decoders and encoders require crystals that meet specific parameters. Specifying the frequency alone will not guarantee proper operation.

Operational failures that could be a related to crystal dysfunction are:
1. Inability to achieve line lock (horizontal lock).
2. Inability to achieve chroma lock.
3. Slow lock acquisition.

The oscillators of the Philips decoders and encoders were originally designed for third overtone crystals which are applied using the example in Figure 1A. There are two load capacitors to match the C_{load} parameter of the crystal and a LC trap to prevent the crystal from operating in the fundamental mode. The drawback of these crystals is that it is difficult to obtain devices in low profile or surface mount because the third overtone AT cut precludes the smaller packages.

Tests were performed to determine if fundamental mode crystals would perform well without excessive loading of the oscillator. The C_{load} parameter of fundamental crystals was 18pF instead of the 8pF for the third overtone, therefore increased load capacitance was required. The LC trap is not required, see Figure 1B.

When specifying these fundamental crystals, it is important that the resonance resistance be kept low (80 ohms or less) to allow the oscillator to start.

The THIRD OVERTONE specifications are:

Nominal Frequency:	26.800000MHz (square pixel decoders) 24.576000MHz (CCIR decoders) 27.000000MHz (CCIR encoders) 24.545445MHz (square pixel encoders–NTSC) 29.500000MHz (square pixel encoders–Pal)
Load capacitance C_{load}:	8pF
Adjustment tolerance:	±40ppm
Resonance resistance:	50Ω (square pixel) 60Ω (CCIR)
Drive level dependency:	80Ω
Motional capacitance C_1:	1.1fF (square pixel) 1.0fF (CCIR)
Parallel capacitance C_0:	3.5pF (square pixel) 3.3pF (CCIR)
Temperature range:	0 to 70° Celsius
Frequency stability:	±20ppm

The FUNDAMENTAL mode specifications are:

Nominal Frequency:	26.800000MHz (square pixel decoders) 24.576000MHz (CCIR decoders) 27.000000MHz (CCIR encoders)
Load capacitance C_{load}:	18pF (standard)
Adjustment tolerance:	±30ppm (B option)
Resonance resistance:	80Ω
Drive level:	2mWatts max.
Motional capacitance C_1:	4fF to 35fF
Parallel capacitance C_0:	7pF
Temperature range:	0 to 70° Celsius
Frequency stability:	±50ppm (B option)

The Philips part numbers for these crystals are:
9922 520 30004 for 26.800000MHz These are third overtone crystals
9922 520 30009 for 24.576000MHz
These are available from the Philips Components Passive Group, phone: (803) 772–2500

Crystal specifications and applications

Crystals are also available from MMD–Mills Marketing and Distribution:

MMC–001–24.576 000MHz	These are third overtone
MMC–002–24.545445 MHz	
MMC–003–26.800000 MHz	
MMC–004–27.000000 MHz	
MMC–005–29.500000 MHz	

MMD also carries fundamental mode crystals:

B20BA1–24.576MHz	These are low–profile through–hole
B20BA1–26.800MHz	
B20BA1–27.000MHz	
D20BA1–24.576MHz	These are low–profile surface mount
D20BA1–26.800MHz	
D20BA1–27.000MHz	

MMD can be reached at (714) 444–1402, Fax:(714) 444–1149. The contacts are Rodney Mills and Matt LaVine.

Crystals are also available from Ecliptek. Their part numbers are:

ECX–2194–26.800MHz	These are third overtone
ECX–2097–24.576MHz	

Ecliptek can be reached at (714) 433–1200 ext. 250, the contact is Mark Stoner.

There is a procedure that may be used to determine if a crystal is properly loaded and running at the correct frequency:

For the decoders :

1. Program the decoder for normal operation (no video input is needed).
2. Set the horizontal phase lock loop bit, HPLL to a logical 1 (normal operation has this bit set to 0). This puts the decoder in a free–running mode, in the center of the lock range.
3. Measure the frequency of the LLC clock output pin, not the crystal itself, this frequency should be:

   27.000000 MHz for CCIR decoders set for either NTSC or Pal (or Secam)
   24.545445 Mhz for square pixel decoders set for NTSC
   or
   29.500000 MHz for square pixel decoders set for Pal or Secam

For the encoders:

1. Set the CDIR pin to a logical 0. This sets the LLC pin as an output. Program the encoder to the MASTER sync mode. Measure the frequencies as you would for the corresponding decoders above.
2. Conversely, if you do not have an accurate frequency counter but do have an accurate source of video (or H/Comp. sync) you can use this signal as a reference. Connect one probe of a dual–trace scope to your reference (this could also be demodulated broadcast video from a tuner, a very accurate source) and connect the other probe to any output of the decoder or encoder that contains horizontal information. For the decoders this could be either the HREF or HS output, for the encoders this could be RCV2 (set as an output) or RCM2 or look at the composite or luminance outputs.
3. Compare the rate at which one trace takes to drift one horizontal interval with respect to the other. A 1 second interval corresponds to a 60ppm difference, a 4 second interval corresponds to a 15ppm accuracy. Anything less than 2 seconds should be considered out of spec.

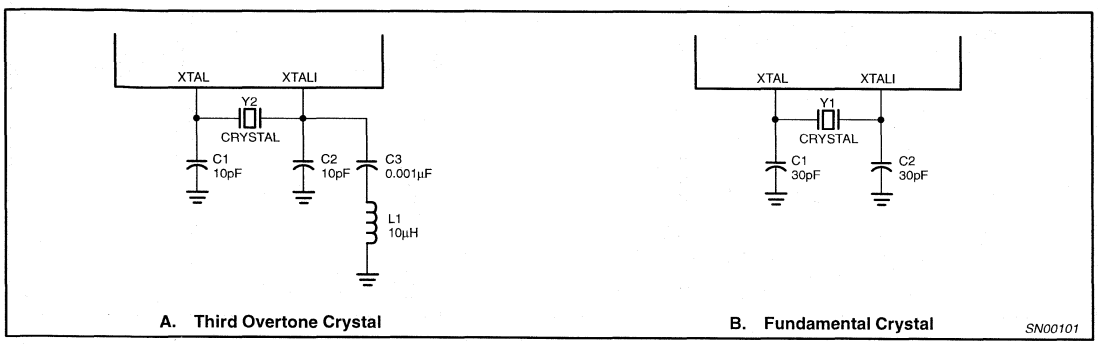

Figure 1. Crystal Application Example

Evaluation board DPC71

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Note: The "E" Revision of the DPC71 evaluation board no longer supports the SAA7151B and SAA7191B decoders and the associated peripheral ICs (A/D converters and clock IC). Instead, additional support has been added for the SAA7111A (3.3vt decoder), for two optional analog comb filters and support for the SAA7124/7125 encoder. Provision has been made to accommodate all three package types of the SAA7111.

1. OVERVIEW

The DPC71 evaluation board has been developed to aid customers in the assessment of Philips digital video decoders and encoders.

The following devices are supported by this board:

- SAA7110 single chip square pixel video decoder
- SAA7111/SAA7111A single chip CCIR video decoder
- SAA7124 CCIR video encoder w/ RGB and Component Out
- SAA7125 CCIR video encoder w/ RGB and Component Out and Macrovision ver.6
- SAA7188A CCIR video encoder w/ Macrovision ver.3
- SAA7184 CCIR video encoder w/ Macrovision ver.6
- SAA7187 Square pixel video encoder
- SAA7185B CCIR video encoder w/o Macrovision
- SAA7183 CCIR video encoder (NTSC, Pal and Secam) with Macrovision ver.6
- SAA7182 CCIR video encoder (NTSC, Pal and Secam) without Macrovision

In addition the S87C054/55 microcontroller is used for on–screen display and device programming. Other ancillary support devices are used for interface purposes.

An I^2C interface is provided for programming in addition to that of the microcontroller. On board voltage regulation is available for bench operation or the board can also be configured to run within an IBM compatible PC.

2. BOARD LAYOUT

The DPC71 board input section is at the right of the board. This section consists of an optional analog comb filter section that can be populated with either a CFM300 comb filter module or a SAA4961 CCD comb filter IC. Further information about comb filters is given in the comb filter application note elsewhere in this handbook. U1 can be populated with either a SAA7110 or SAA7111/SAA7111A single chip decoder. The use of the SAA7111A requires that voltage regulatorVR2 be changed to a 3.3vt. device and that the I2C and input circuits of the SAA7111A be modified (see sheet 3 of the schematics).

Two RCA jacks (J11 and J12) are provided for composite video input and one DIN connector (J13) is available for S–Video input. The Composite 2 input is connected to both the decoder and comb filter sections and JP27 allows for selction of S–video type signals from either the comb filter output or directly from the S–video connector (see sheet 3 of schematics).

The interface section of the board is comprised of JP2, JP3 and P1,the D1 (CCIR656) interface. The left hand side of JP2 is comprised of signals from the decoder section, data, clocks and sync lines. The right hand side comprises the corresponding inputs to the encoder (output) section. These lines are arranged such that shunting adjacent pairs does the following (refer to Figure 1):

1. Connects the Y data from the decoder to the VP port of the SAA7185 (the VP2 port of the SAA7187).
2. Connects the UV data from the decoder to the DP port of the SAA7185 (the VP3 port of the SAA7187).
3. Connects the clock, sync and RTC lines from the decoder to the appropriate inputs of the encoder.

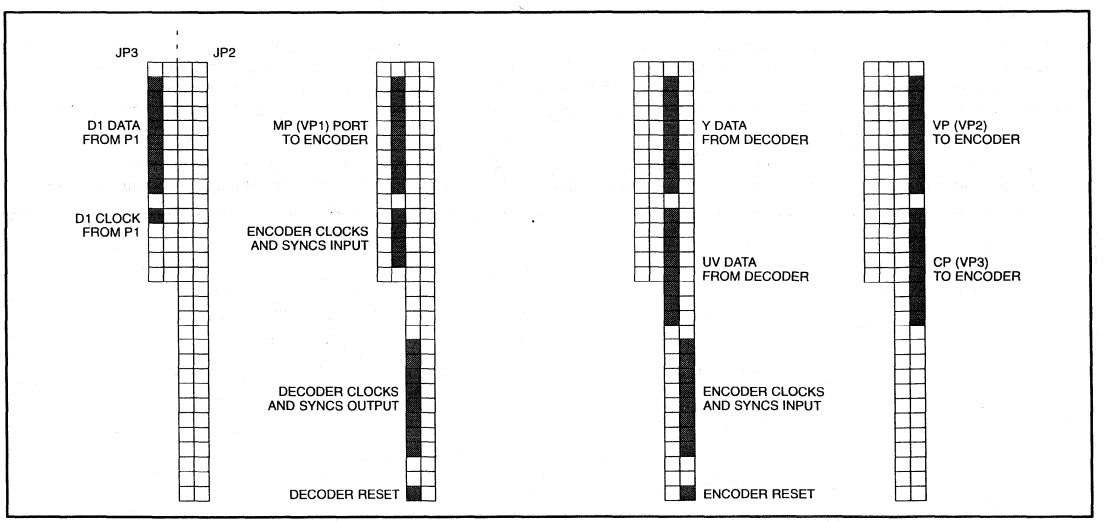


Figure 1.

JP3 is oriented next to JP2 in such a way that if shunts are inserted between the right hand side of JP3 and the left hand side of JP2, the Y data from the decoder section is applied to the MP port of the SAA7185/82/24 (VP1 port of the 7187). If the shunts are installed between the right and left hand side of JP3, the data from the D1 interface is applied to the MP port of the SAA7185/82/24 (the 7187 cannot be driven with a D1 data source).

JP2 and JP3 can also be used to interface digital video to and from other external devices.

Provision has also been made to interface the output stage to sources of CCIR656 (D1) video. A DB25 connector, meeting the D1 pinning spec. allows for input of the ECL based digital video. Three ECL to TTL translators (U9, 10, and 11) convert the input to TTL levels. The TTL YUV data is then made available at the left hand side of JP3. The data–embedded sync markers (EOV and SOV) are decoded with a Pal22V10 device (U12) and made available on the encoder sync input lines. These sync signals may be tri–stated to avoid conflict if a decoder (or other sync source) is being used.

The encoder section at the left of the board comprises the output section. The SAA7188A, SAA7184 and SAA7185 CCIR encoders and the SAA7187 square–pixel encoder can be evaluated at position U8, the SAA7124/5 and SAA7182/3 can be evaluated at position U13. The one pin difference of the SAA7187 is accounted for with JP11.

Digital video is input from JP2 and JP3 and composite video is output at J14 and S–video at J15. If a SAA7124/5 or SAA7182/3 is used, RGB (or CbYCr in the case of the SAA7124/5) and composite sync is available at P2. A simple reconstruction filter is used to remove residual clock energy from the outputs.

Programming support is provided by U6, a S87C054 microcontroller which also provides on–screen display via the OSD inputs of the encoder. Four push–buttons (S1–S4) allow for feature selection via a menu hierarchy. Additional programming can be done via the I^2C bus connector JP1. U7, a PCF8598 EEPROM is provided to store custom configurations.

U14, a LM319 comparator and Q1 comprise a circuit that removes and buffers composite sync from the composite video output of the encoder for use with the RGB outputs.

JP6, JP7, and JP8 configure the board for PC ISA bus power or for power from an external power supply. In the case of the PC based power option, V_{CC}_ENC and V_{CC}_DEC is regulated down from the +12 volt supply and V_{ee} is regulated from the –12 volt supply of the PC. In the case of an external power supply both V_{CC}_ENC and V_{CC}_DEC are regulated from +9 volts and the V_{ee} from –9 volt supplies. The +9 volt supply connects to J26, the –9 volt supply to J28 and ground to J27.

The jumpers and headers have the following functions:

- JP1 is the I^2C input
- JP2 and JP3 are the digital output of the decoder section and the digital inputs to the encoder as described previously
- JP4 selects the slave address for U1, low selects $9C_{hex}$, high selects $9E_{hex}$ (48_{hex} and $4A_{hex}$, respectively for the 7111)
- JP6, JP7, and JP8 allow for PC or external power selection.
- JP9 selects the slave address for the encoder, U8 (low selects 88_{hex}, high selects $8C_{hex}$)
- JP10 allows for VCLK selection for U6, pins 1 and 2 select 13.5MHz and pins 2 and 3 select 6.75MHz
- JP11 redefines the supply at pin 42 of U8, pins 1 and 2 connect pin 42 to the V_{cc} line for the SAA7187 and connecting pins 2 and 3 define pin 42 as ground (for the SAA7188A and the SAA7185). THIS IS VERY IMPORTANT.
- JP12 allow the selection of either vertical sync or field ID for input to the RCV1 pin of U8
- JP13 enables the sync outputs of the D1 decoder (U12). This should be disabled if sync is being derived from the decoder section.
- JP19 allow the selection of either vertical sync or field ID for input to the RCV1 pin of U13
- JP21 selects the slave address for the encoder, U13 (low selects 88_{hex}, high selects $8C_{hex}$)
- JP22 allows the polarity of the composite sync at P2 to be reversed.
- JP23–JP26 connect the analog and digital ground planes together.
- JP27 selects decoder Y/C in from either the comb filter or the S–Video connector.
- JP28 is the interface connector for teletext.
- JP29 is the output selector block that configures the SAA7124/5 and SAA7182/3 output pin assignments.

There are five push button switches, S1 through S4 select program features via the microcontroller (U6) control over the I^2C bus. Details are given later in the software specification. S6 is the reset (active HIGH) for the microcontroller. S5 was deleted from the previous board version.

Several ground pins are provided for scope probing as are pertinent test pins.

- J16 and J17 are test pins for the HCL and HSY outputs of U1 (SAA7110 only).
- J18 and J19 are test pins for the I^2C bus
- JP20 is the horzontal lock status of U1
- JP21 is the vertical blanking pulse from U1.

3. CONFIGURATION MODES

There are several configurations possible with the DPC71 evaluation board:

1. CCIR656 (D1) digital video is input to connector P1, the translated TTL digital video data is input to the MP port of U8 or U13 via JP3. The encoded HREF and FieldID are decoded by U12 and also coupled at JP3. (The clocks previously derived from the decoder and present at JP2 must be disconnected to avoid conflict. In the case of Examples 2, 3 and 4, the output of U12 is tri–stated by opening JP13). U8 (orU13) is run in slave mode, however the RCT input is not required.
2. Square pixel rate video decoding is provided by installing a SAA7110 at U1 (a 26.800MHz crystal is used at Y1) and SAA7187 at U8, the luminance data is derived from JP3 shunted to JP2 so that the data is input to the VP1 port of the SAA7187. The UV data is derived as before from JP2 and input to the VP3 port of the encoder. No crystal is needed for U8 in this mode. The encoder is run in the RTC slave mode.
3. CCIR601 video is input to the SAA7111 (U1), which requires a 24.576MHz crystal at Y1. U1 in turn drives the SAA7185 or other CCIR encoders in the same manner as in example (2) in the RTC slave mode.
4. The encoder U8 or U13 is run in a stand–alone mode. No external input is required if the internal color bar option is selected. External data may be input if it is locked to the LLC, H sync and V sync that is sourced by the encoder. A crystal is needed at Y4, for the CCIR encoders, a 27.000MHz crystal is used for all standards. For the SAA7187, a 24.5454MHz crystal is used for NTSC and for Pal a 29.500MHz crystal is used at Y4. When run in stand–alone (or master mode as it is also called) the sense of the input pin CDIR is set LOW by the microcontroller (U6).

Note: The D1 interface is not applicable in the square pixel format.

Also note that the digital outputs from the decoders may be tapped off at JP2 and sent to other off–board devices to be processed and may then be returned to be encoded. One example is connection to a MPEG compression/decompression system, another is a video–on–demand server.

4. REGISTER SETTINGS

Table 1. SAA7151 Register Settings

PCALC Lab 4/5/95

These register settings give examples of SAA7151 programming for the DPC71 evaluation board.
Register settings for NTSC, Pal and Secam standards are shown.

REGISTER	VALUE	FUNCTION
0	66	Increment delay
1	36	Begin HSY
2	0B	End HSY
3	EC	Begin HCL
4	D0	End HCL
5	XX	Horizontal sync out position–application specific
6 (Pal values in parentheses)		Luminance control
	10 (04)	CVBS, no aperture correction
	98 (88)	S–Video, no aperture correction
	15 (05)	CVBS, aperture correction, factor .25
	9D (8D)	S–Video, aperture correction, factor .25
	16 (06)	CVBS, aperture correction, factor .5
	9E (8E)	S–Video, aperture correction, factor .5
	17 (07)	CVBS, aperture correction, factor 1
	9F (8F)	S–Video, aperture correction, factor 1
7	00	Hue control, 360 deg. range, 256 steps
8	BF	Control no. 1–Video standard (NTSC–M), QUAM color–killer set to –30dB
	1F	Pal–BG, QUAM color–killer set to –30dB
	5F	Secam
9	3F	Control no. 2–AGC filter set to medium, Secam color–killer set to –30dB
A	7F	Pal sensitivity switch set to medium
B	7F	Secam sensitivity switch set to medium
C		Control no.3–Input select (also chrominance gain set by loop)
	28	CVBS input 1
	68	CVBS input 2
	48	S–Video (note– reg. 06 must have MSB set HIGH also)
D	4D	Control no. 4
E	30	Control no. 5
F	58	Control no. 6–VTR mode, manual field selection (controlled by reg. 08)
10	60	Control no. 7–manual standard selection (controlled by reg. 08), Y delay set to 0, Y delay has 16 steps of 37ns from 0 to 296ns (step 0 to 7) and from –296 to –37ns (step –8 to–1)
11	18	Chroma gain, 8 bit of control from 0 to 255
12	C0	Control no. 8–YUV bus active, vertical noise reduction normal

Table 2. SAA7188A, 7184 and 7185(B) Register Settings

PCALC Lab 5/21/96

These register settings assume that the encoder is being operated as follows:

Slave mode:LLC, RCV1 and RCV2 (and RTC in case of decoder input) are INPUT .
RCV1 is reset with Field ID (low for field 1, high for field 2).
RCV2 is reset with HREF (Horz. blanking–Low during blanking period).
NTSC–M:American standard (7.5IRE setup)–Pal B,G values in parentheses.
OSD:Set to reproduce 100/75 percent full field color bars.
Input Format:8 Bit 4:2:2 CbYCr CCIR656 from TSG422 (D1) test generator.
A video decoder can also be used as an digital input (16–bit mode).
Data is input to MP data port (VP in the case that a decoder is used).

REGISTER	VALUE	FUNCTION
00–39	00	
3A	1F	Input Port Control (selects 8–bit input mode)–e.g. D1 input
	0F	Selects 16–bit input mode–e.g. decoder input
	DF	Selects internal color bars
3B–41	00	
42	6B	OSD Y0
43	00	OSD U0 WHITE (100%)
44	00	OSD V0
45	22	OSD Y1
46	AC	OSD U1 YELLOW (75%)
47	0E	OSD V1
48	03	OSD Y2
49	1D	OSD U2 CYAN (75%)
4A	AC	OSD V0
4B	F0	OSD Y3
4C	C8	OSD U3 GREEN (75%)
4D	B9	OSD V3
4E	D4	OSD Y4
4F	38	OSD U4 MAGENTA (75%)
50	47	OSD V4
51	C1	OSD Y5
52	E3	OSD U5 RED (75%)
53	54	OSD V5
54	A3	OSD Y6
55	54	OSD U6 BLUE (75%)
56	F2	OSD V6
57	90	OSD Y7
58	00	OSD U7 BLACK
59	00	OSD V7
5A	XX	Chroma Phase (setting determined by application)
5B	79 (82)	Gain–U axis
5C	AD (B6)	Gain–V axis
5D	3C (2D)	Black Level
5E	3A (3F)	Blanking Level
5F	3A (3F)	Blanking Level during vertical (7184 and7185B only)
60	XX	Cross–Color Reduction (user choice)
61	15 (06)	Standard Control
	1D (0E)	Enables RTC function when a decoder is used as input

REGISTER	VALUE	FUNCTION
62	69 (4E)	Burst Amplitude for SAA7188A and 7185 (non B)
	E9 (CE)	for SAA7184/85B, selects improved RTC from SAA7111(A)
63	1F (CB)	Subcarrier (4 LSB's)
64	7C (8A)	Subcarrier
65	F0 (09)	Subcarrier
66	21 (2A)	Subcarrier (4 MSB's)
67	XX	Closed Caption–Odd Field–First Byte
68	XX	Closed Caption–Odd Field–Second Byte
69	XX	Closed Caption–Even Field–First Byte
6A	XX	Closed Caption–Even Field–Second Byte
6B	11 (15)	MP Port Select–Closed Caption Line Select
	91 (96)	Selects VP port as input (for 16 bit mode from video decoder)
6C	6D	RCV Port Control (Slave mode selected)
6D	07	RCM–CC Mode
6E	9D (AB)	H–Trigger (LSB's)–setting determined by app.
	9E (AC)	When used with video decoder in 16–bit mode–SEE NOTE 1.
6F	66	H–Trigger (MSB's)–setting determined by app.
70	C0 (80)	Subcarrier Reset–V–Trigger (4 field reset of SC)–used in D1 mode
	0E (0C)	When used in RTC mode with decoder–SEE NOTE 2.
71	XX	Begin MP Request–setting determined by app.
72	XX	End MP Request–setting determined by app.
73	XX	MP Request (MSB's)
74–76	00	NULL
77	XX	Begin RCV2 Out (defined only in Master mode)
78	XX	End RCV2 Out (defined only in Master Mode)
79	XX	RCV2 Out (MSB's)
7A	0C (70)	Field Length
7B	12 (17)	First Active Line
	(16)	First Active Line in the case of D1 Pal
7C	03 (35)	Last Active Line
7D	22	Field Control (MSB's)

NOTES:

1. For 8–bit from a D1 (CCIR656) or other 8–bit multiplexed (C_b,YC_r,Y,etc.) source:
   Register 6E–6F, H trigger (LSB's):
   Upper limit is $6B3_{hex}$ for NTSC, $6BF_{hex}$ for Pal
   Lower limit is 01_{hex}
   Typical value is 9D
   The initial origin of the H trigger is set by the input to RCV2 which in the case of D1 signals is the EOV (end of video) or SOV (start of video) pulse decoded from the video data stream, depending if RCV2 is triggered on the rising or falling edge–set in register 6C.
   For 16–bit input from a decoder (or other 16–bit source):
   Register 6E–6F:
   Upper limit is $6B3_{hex}$ for NTSC, $6BF_{hex}$ for Pal
   Lower limit is 01_{hex}
   Typical value is 9E
   This is affected by the timing of the RCV2 reset signal, which in the case that a SAA7111 is used, the HREF output of the decoder resets the H trigger (in this example the falling edge is used, however the sense of the trigger edge is programmable with reg. 6C).
2. For the RTC slave mode of the SAA7188A (7184 or 7185) register 70 is set to $0E_{hex}$ (NTSC) or to $0C_{hex}$ (Pal) to defeat the subcarrier reset. Setting register 70 to $C0_{hex}$ causes the encoder to reset the subcarrier every four fields, which is normal for NTSC, Setting register 70 to 80_{hex} resets the encoder every eight fields which is correct for Pal.

Table 3. SAA7110 Register Settings

PCALC Lab 5/23/96

These register settings give examples of SAA7110 programming for the DPC71 evaluation board. CVBS input 1 uses mode 1, CVBS input 2 uses mode 3 and the S–Video input uses mode "9" (this mode inputs chroma to pin 17 (AI31) and luma to pin 21 (AI21). This mode is not shown in the source managment section of the data sheet but is a viable configuration of the IC and allows for complete pin compatibility with the SAA7111). Register settings for NTSC, Pal and Secam standards are shown. Values in parenthesis are 50 Hz (Pal and Secam) level settings.

REGISTER	VALUE	FUNCTION
00	4C	Increment delay
01	3F	Begin HSY (50Hz)
02	0D	End HSY (50Hz)
03	EF	Begin HCL (50Hz)
04	BD	End HCL (50Hz)
05	XX	Horz. sync out position (50Hz)–application specific
06		Luminance control
	00	CVBS, no aperture correction
	80	S–Video, no aperture correction
	05	CVBS, aperture correction, factor .25 (coring, 1 bit)
	85	S–Video, aperture correction, factor .25 (coring, 1 bit)
	0A	CVBS, aperture correction, factor .5 (coring, 2 bit2)
	8A	S–Video, aperture correction, factor .5 (coring, 2 bits)
	0F	CVBS, aperture correction, factor 1 (coring, 3 bits)
	8F	S–Video, aperture correction, factor 1 (coring,3 bits)
07	01	Hue control, 360 deg. range, 256 steps
08	F8	Color killer (QUAM)
09	F8	Color killer (Secam)
0A	60	Pal sensitivity switch
0B	60	Secam sensitivity switch
0C	00	AGC loop constant, color killer ON (MSB)
	80	Color forced on (no color killer)
0D	86	Standard control, non Secam, status byte 1 selected
	87	Secam selected (selected in conjunction with reg. 0F)
0E	18	I/O, clock control and gen. purpose switch
0F		Control 1
	30	50Hz standard selected (Pal or Secam, depending on LSB of reg. 0D)
	70	60Hz standard selected (NTSC) The 3 LSB's control Y delay compensation (0 equals no compensation, range is –4 to 3 steps of pixel rate period)
10	00	Control 2
11	59	Chroma gain (Pal CCIR level)
	2C	Chroma gain (NTSC CCIR level)
12	40 (3E)	Saturation control, range 0 to 7F, 0 equals color off
13	50 (4F)	Contrast control, range 0 to 7f, 0 equals luminance off
14	42	Begin HSY (60Hz)
15	1A	End HSY (60Hz)
16	FC	Begin HCL (60Hz)
17	D3	End HCL (60Hz)
18	XX	Horz. sync out position (60Hz)–application specific

REGISTER	VALUE	FUNCTION
19	91 (9B)	Brightness, range 0 to FF, 256 steps
1A–1F	00	Reserved–fill with 0's
20		Analog Control no. 1
	D8	CVBS input 1 See note 1
	B8	CVBS input 2
	9B	S–Video
21		Analog Control no. 2
	16	CVBS input 1
	05	CVBS input 2
	12	S–Video
22		Mix control no. 1
	40	CVBS input 1
	91	CVBS input 2
	41	S–Video
23	4C	Clamp level control 21
24	80	Clamp level control 22
25	40	Clamp level control 31
26	80	Clamp level control 32
27	41	Gain control no. 1
28	FE	White peak control
29	01	Sync bottom control
2A	C5	Gain control no. 2
2B	0F	Gain control no. 3
2C		Mix control no. 2
	03	CVBS1 or CVBS2 selected–see note 1
	83	S–Video selected
2D	01	Integration value gain
2E	XX	Vertical blanking pulse SET–application specific
2F	XX	Vertical blanking pulse RESET–application specific
30		ADC gain setting
	60	For CVBS2
	44	For CVBS1 and S–Video
31		Mix control no. 3
	45	5 MHz ADC filter, GPSW active, integration on line basis
	75	5 MHz ADC filter, GPSW active, integration on a field basis
	47	5 MHz ADC filter, vertical blanking pulse out active, integration on line basis
	77	5 MHz ADC filter, vertical blanking pulse out active, integration on a field basis
32	02	Integration value peak white
33	8C	Mix control no. 4–LLC/2 ADC clock rate selected
34	03	Gain up–date level

NOTES:

1. Registers 20, 21 and 22 work in conjunction with reg. 06, bit D7, BYPS, which is set LOW for composite input and HIGH for S–Video input,and with reg. 2C which is set to a value of 03_{hex} for CVBS inputs 1 and 2 and set to 83_{hex} for S–Video.

Table 4. SAA7187 Register Settings

PCALC Lab 2/22/95

These register settings assume that the SAA7187 is being operated as follows:
Slave mode:LLC, RCV1 and RCV2 and RTC from the decoder are INPUT.
RCV1 is reset with Field ID (low for field 1, high for field 2).
RCV2 is reset with HREF (Horz. blanking–Low during blanking period).
NTSC–M:American standard (7.5IRE setup)–Pal B,G values in parentheses.
OSD:Set to reproduce 100/75 percent full field color bars.
Input Format:16 Bit 4:2:2 CbYCr from an SAA7110 digital video decoder.
Y data is input to the VP1 port, UV data is input to the VP3 port.

REGISTER	VALUE	FUNCTION
00–39	00	
3A		Input Port Control
	0D	Selects 16–bit input mode
	0E	Selects 8–bit input mode
	8D	Selects internal color bars
3B–41	00	Null
42	6B	OSD Y0
43	00	OSD U0 WHITE (100%)
44	00	OSD V0
45	22	OSD Y1
46	AC	OSD U1 YELLOW (75%)
47	0E	OSD V1
48	03	OSD Y2
49	1D	OSD U2 CYAN (75%)
4A	AC	OSD V2
4B	F0	OSD Y3
4C	C8	OSD U3 GREEN (75%)
4D	B9	OSD V3
4E	D4	OSD Y4
4F	38	OSD U4 MAGENTA (75%)
50	47	OSD V4
51	C1	OSD Y5
52	E3	OSD U5 RED (75%)
53	54	OSD V5
54	A3	OSD Y6
55	54	OSD U6 BLUE (75%)
56	F2	OSD V6
57	90	OSD Y7
58	00	OSD U7 BLACK
59	00	OSD V7
5A	XX	Chroma Phase (setting determined by application)
5B	79 (80)	Gain–U axis
5C	AA (BF)	Gain–V axis
5D	3B (2D)	Black Level
5E	3A (3F)	Blanking Level
5F	00	NULL
60	XX	Cross–Color Reduction (user choice)

REGISTER	VALUE	FUNCTION
61		Standard Control
	1D (0E)	RTC is active
	15 (06)	RTC is inactive
62	EC (D2)	Burst Amplitude
63	55 (0C)	Subcarrier (4 LSB's)
64	55 (8C)	Subcarrier
65	55 (79)	Subcarrier
66	25 (26)	Subcarrier (4 MSB's)
67	XX	Closed Caption–Odd Field–First Byte
68	XX	Closed Caption–Odd Field–Second Byte
69	XX	Closed Caption–Even Field–First Byte
6A	XX	Closed Caption–Even Field–Second Byte
6B	11 (14)	Closed Caption Line Select
6C	69	RCV Port Control (Slave mode selected)
6D	03	RCM–CC Mode
6E	F4 (3B)	H–Trigger (LSB's)–setting determined by app.
6F	05 (07)	H–Trigger (MSB's)–setting determined by app.
70	CE (8C)	Subcarrier Reset–V–Trigger (4 field reset of SC for NTSC, 8 field reset for Pal)
	0E (0C)	No reset–used in RTC mode with decoder – See Note 2.
71	XX	Begin MP Request–setting determined by app.
72	XX	End MP Request–setting determined by app.
73	XX	MP Request (MSB's)
74–76	00	NULL
77	XX	Begin RCV2 Out (defined only in Master mode)
78	XX	End RCV2 Out (defined only in Master Mode)
79	XX	RCV2 Out (MSB's)
7A	0C (70)	Field Length
7B	12 (15)	First Active Line
7C	03 (35)	Last Active Line
7D	22	Field Control (MSB's)

NOTES:

1. Register 6E–6F, H trigger (LSB's):
   Upper limit is 617hex (60Hz), 75Fhex (50Hz)
   Lower limit is 01hex
   In steps of 4,....typical value is 5F4hex
   The initial origin of the H trigger is set by the input to RCV2.
   This is affected by the timing of the RCV2 reset signal, which in the case that a SAA7151B is used, the HREF output of the decoder resets the H trigger (in this example the falling edge is used, however the sense of the trigger edge is programmable with reg. 6C).
2. For the RTC slave mode of the SAA7187 register 70 is set to 0Ehex (NTSC) or 07hex (Pal) to defeat the subcarrier reset.
   Setting register 70 to CEhex causes the encoder to reset the subcarrier every four fields, which is normal for NTSC.
   Setting register 70 to 87hex resets the encoder every eight fields which is correct for Pal.
   The last 5 bits of the register are used to set the vertical trigger.

Table 5. SAA7111 Register Settings

PCALC 4/19/95

The following are suggested register settings for the SAA7111 CCIR single chip video decoder. Values are given for several versions of both the NTSC and Pal standards. Secam is not supported by the SAA7111. Slave address (write mode) is: 48_{hex} for IICSA=0, $4A_{hex}$ for IICSA=1.

REGISTER	VALUE	FUNCTION
00	XX	Chip version (read only)
01	00	Reserved for chip version
02	D8	CVBS1 composite video input } Analog control 1
	DB	CVBS2 composite video input
	DE	S–Video input
03	23	Analog Control 2
04	00	Static gain control, channel 1
05	00	Static gain control, channel 2
06	XX	Horizontal sync begin (depends on user application)
07	XX	Horizontal sync stop (depends on user application)
08		Field Control
	08	50Hz
	48	60Hz
	88	Automatic field rate selection
09		Luminance Control
	10	NTSC aperture–no peaking
	11	NTSC .25 peaking factor
	12	NTSC .5 peaking factor
	13	NTSC 1.0 peaking factor
	00	Pal aperture–no peaking
	01	Pal .25 peaking factor
	02	Pal .5 peaking factor
	03	Pal 1.0 peaking factor
	80	S–Video–no peaking
0A	80	Luminance Brightness (CCIR level)
0B	47	Luminance Contrast (CCIR level)
0C	40	Chrominance Saturation
0D	00	Chroma Hue
0E	01	Chroma Control, Pal BGHI or NTSC M (new RTC–7184,85B,82 or24)
	41	(old RTC–7199B, 7188A, 7185(non B)) **note:** For subcarrier DTO reset of new RTC, program reg. 0E to 81 after both decoder and encoder have be programmed.
0F	00	Reserved
10	48	16 bit YUV output, no Y delay compensation, HS fine adjustment equal to 0
11	0C	YUV and sync busses enabled, color killer ON
12	80	Field ID on pin 40, H lock on pin 39, no dither

Table 6. SAA7183(7182) Register Settings

PCALC Lab 4/19/95

Register settings are given below for both 8–bit and 16–bit input, slave mode with RTC in the case that a video decoder is the data and clock source and without RTC in the case that CCIR656 from a D1 generator is the source. Examples for NTSC, Pal and Secam are shown. Pal and Secam values are shown in parentheses if they are the same, otherwise, the Secam values are in square brackets. OSD registers are programmed to produce 100/75 percent color bars.

The slave address is 88_{hex} if IICSA=0, and $8C_{hex}$ if IICSA=1

REGISTER	VALUE	FUNCTION
00–39	00	NULL
3A		Input Port Control
	07	16 bit mode selected (8 bits Y on MP port, 8 bits UV on CP port)
	03	8 bit mode selected (CbYCr on MP port)
	8X	Internal color bars selected
3B–41	00	NULL
42	6B	OSD Y0
43	00	OSD U0 WHITE (100%)
44	00	OSD V0
45	22	OSD Y1
46	AC	OSD U1 YELLOW (75%)
47	0E	OSD V1
48	03	OSD Y2
49	1D	OSD U2 CYAN (75%)
4A	AC	OSD V2
4B	F0	OSD Y3
4C	C8	OSD U3 GREEN (75%)
4D	B9	OSD V3
4E	D4	OSD Y4
4F	38	OSD U4 MAGENTA (75%)
50	47	OSD V4
51	C1	OSD Y5
52	E3	OSD U5 RED (75%)
53	54	OSD V5
54	A3	OSD Y6
55	54	OSD U6 BLUE (75%)
56	F2	OSD V6
57	90	OSD Y7
58	00	OSD U7 BLACK
59	00	OSD V7
5A	XX	Chroma Phase (setting determined by application)
5B	79 (8D) [6A]	Gain–U axis
5C	AD (C9) [7F]	Gain–V axis
5D	3C (2D)	Black Level, U Gain MSB
5E	3A (3F) [BF]	Blanking Level–RTC detect for SAA7151B, V Gain MSB
	7A (7F) [FF]	Blanking Level–RTC detect for SAA7111
5F	3A (3F)	Vertical Blanking Level
60	00	NULL

REGISTER	VALUE	FUNCTION
61	15 (06) [0E]	DAC and Standard Control, All DACs are active
62	69 (4E)	Burst Amplitude, RTC not active
	E9 (CE)	Burst Amplitude, RTC active
63	1F (CB) [B2]	Subcarrier (4 LSB's)
64	7C (8A) [3B]	Subcarrier
65	F0 (09) [A3]	Subcarrier
66	21 (2A) [28]	Subcarrier (4 MSB's)
67	XX	Closed Caption–Odd Field–First Byte
68	XX	Closed Caption–Odd Field–Second Byte
69	XX	Closed Caption–Even Field–First Byte
6A	XX	Closed Caption–Even Field–Second Byte
6B	6D	RCV Port Control (Slave mode selected)
6C		H Trigger (8 LSBs)
	9A (AE)	D1 mode
	9B (AF)	Decoder mode
6D		H Trigger (3 MSBs), V Trigger (5 bits)
	C0	D1 mode
	D0	Decoder mode
6E		Multi–Control
	30 (20)	No RTC used
	00	If RTC is used
6F	D1 (D4)	Closed Caption/TTX Control
70	XX	RCV2 Out, Start (8 LSBs)–determined by application
71	XX	RCV2 Out, End (8 LSBs)–determined by application
72	XX	RCV2 Out, (3 MSBs of regs. 71 and 72)
73	XX	Start of TTXRQ (8LSBs)
74	XX	End of TTXRQ (8 LSBs)
75	XX	Start of TTXRQ (3 MSBs), End of TTXRQ (3 MSBs)
76	XX	First TTXRQ line in odd field (8 LSBs)
77	XX	Last TTXRQ line in odd field (8 LSBs)
78	XX	First TTXRQ line in even field (8 LSBs)
79	XX	Last TTXRQ line in odd field (8 LSBs)
7A	12 (15)	First Active Line (8 LSBs)
7B	03 (35)	Last Active Line (8 LSBs)
7C	4X	LAL and FAL (MSB), MSBs of registers 76–79

Table 7. SAA7124(7125) Register Settings

PCALC Lab 5/22/96

Register settings are given below for slave mode with RTC in the case that a video decoder is the data and clock source and without RTC in the case that CCIR656 from a D1 generator is the source. Examples for NTSC, Pal are shown. Pal is shown in parentheses

The slave address is 88_{hex} if IICSA=0, and $8C_{hex}$ if IICSA=1

REGISTER	VALUE	FUNCTION
00–39	00	NULL
3A		I/O Port Control
	0B	CVBS and Component Out
	03	CVBS and RGB Out
	4B	CVBS and S–Video Out
	8X	Internal color bars selected
3B–59	00	NULL–No OSD registers
5A	XX	Chroma Phase (setting determined by application)
5B	79 (8D)	Gain–U axis
5C	AD (C9)	Gain–V axis
5D	3C (2D)	Black Level, U Gain MSB
5E	3A (3F)	Blanking Level–RTC detect for SAA7151B, V Gain MSB
	7A (7F)	Blanking Level–RTC detect for SAA7111
5F	3A (3F)	Vertical Blanking Level
60	00	NULL
61	15 (06)	DAC and Standard Control, All DACs are active
62	69 (4E)	Burst Amplitude, RTC not active
	E9 (CE)	Burst Amplitude, RTC active
63	1F (CB)	Subcarrier (4 LSB's)
64	7C (8A)	Subcarrier
65	F0 (09)	Subcarrier
66	21 (2A)	Subcarrier (4 MSB's)
67	XX	Closed Caption–Odd Field–First Byte
68	XX	Closed Caption–Odd Field–Second Byte
69	XX	Closed Caption–Even Field–First Byte
6A	XX	Closed Caption–Even Field–Second Byte
6B	6D	RCV Port Control (Slave mode selected)
6C		H Trigger (8 LSBs)
	9A (AE)	D1 mode
	9B (AF)	Decoder mode
6D	CC	H Trigger (3 MSBs), V Trigger (5 bits)
6E		Multi–Control
	30 (20)	No RTC used
	00	If RTC is used
6F	D1 (D4)	Closed Caption/TTX Control
70	XX	RCV2 Out, Start (8 LSBs)–determined by application
71	XX	RCV2 Out, End (8 LSBs)–determined by application
72	XX	RCV2 Out, (3 MSBs of regs. 71 and 72)
73–79	00	NULL
7A	12 (15)	First Active Line (8 LSBs)
7B	03 (35)	Last Active Line (8 LSBs)
7C	4X	LAL and FAL (MSB), MSBs of registers 76–79

5. SOFTWARE

5.1. I²C-Controller Software

Shipped with the DPC71 Evaluation Board is:

A MS Windows based program named "DPC71.EXE" which allows control over the more commonly controlled parameters of the devices for the various configurations described in section 3. This is graphical user interface (GUI) based program that allows facile manipulation of the decoder and encoder functions. There is also a universal I2C transmitter option that allows for the modification of any register in either hex or binary. Text comments can also be added to the individual register settings to aid in documentation. Individually tailored register files can be saved under user defined names for recall later.

This software communicates to the board via the I²C parallel printer port adaptor.

5.2. The I²C Parallel Printer Port Adaptor

An adaptor card is supplied to interface the DPC71 with an IBM compatible computer via the parallel printer port and a four conductor cable–also supplied. Figure 2a. illustrates the adaptor board and Figure 2b. the detail of the cable interface to JP4.

There are three plugs on the port interface: JP3 is the European configuration, JP4 is the U.S. configuration (this is the plug used for the evaluation board), and JP5 which is a buffered version of JP4 which will drive long cable loads. Refer to Fig. 2b. when connecting the interface cable as there is no polarization key on the plug.

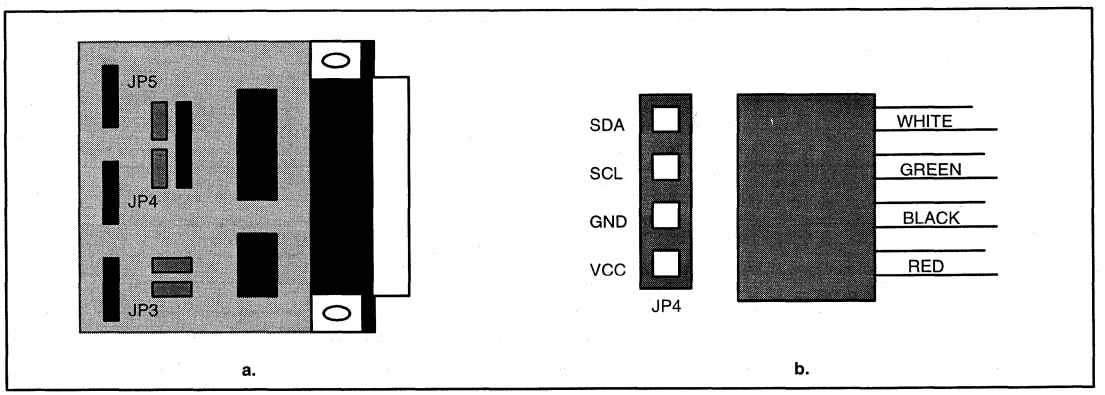


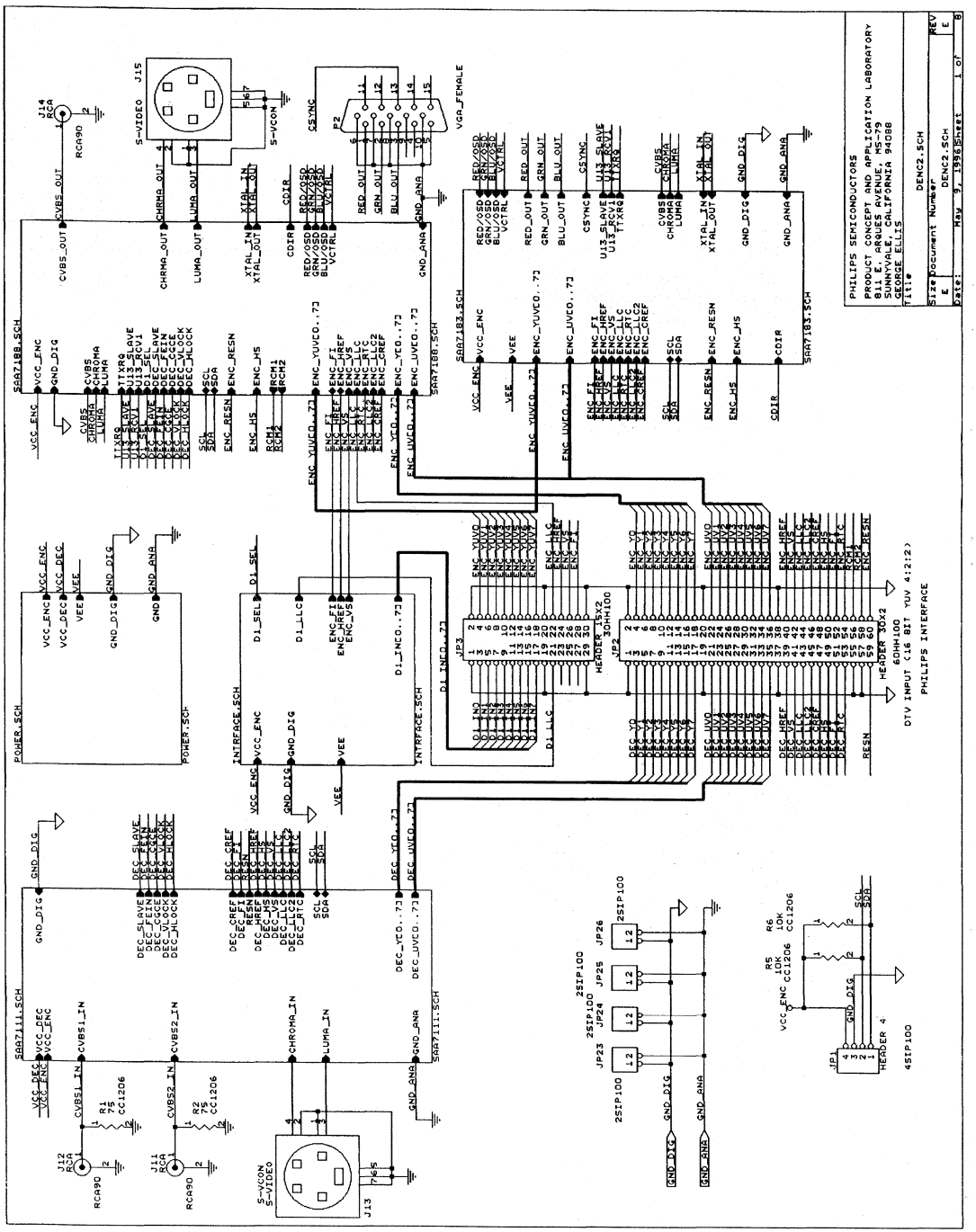
Figure 2.

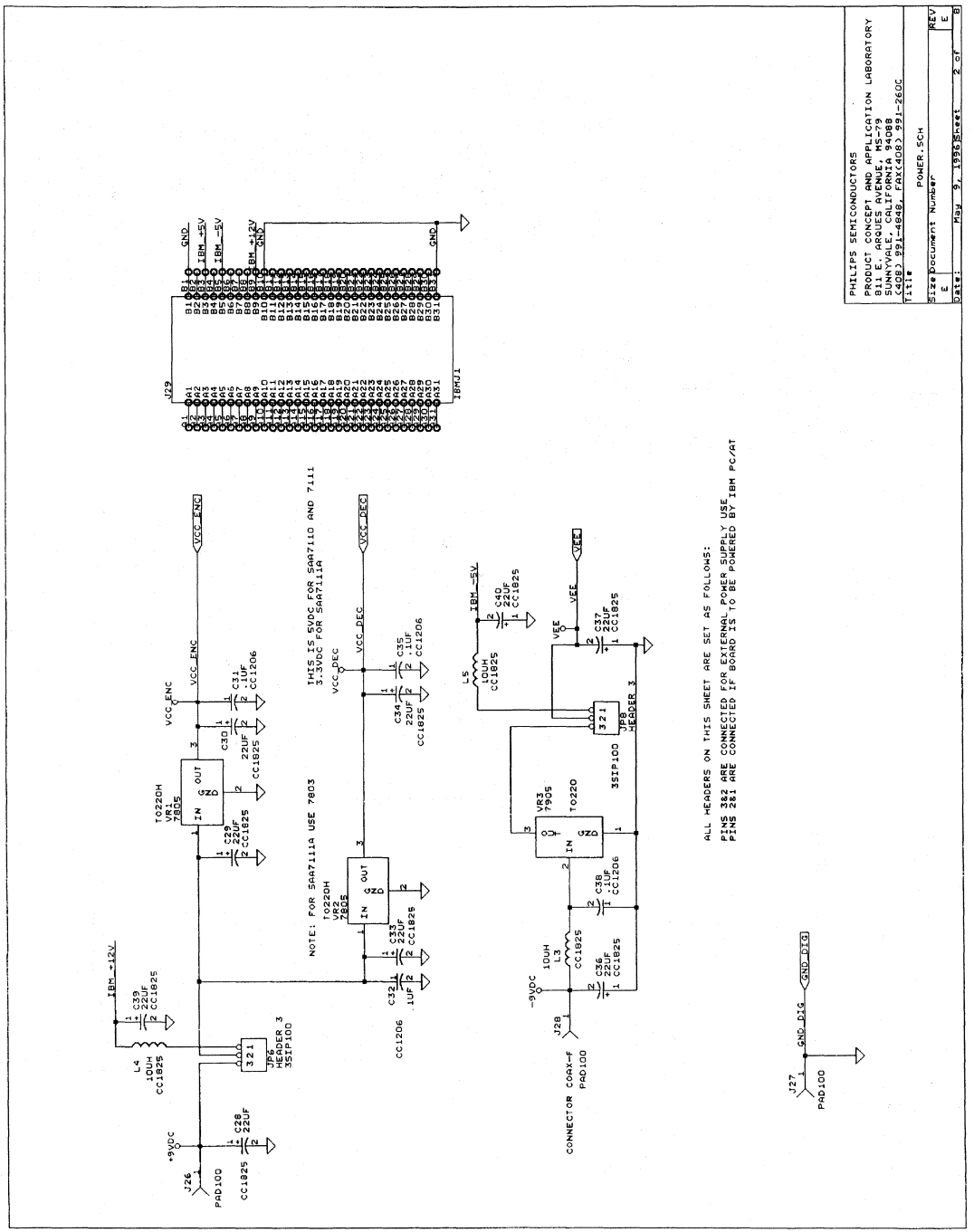
6. SCHEMATICS

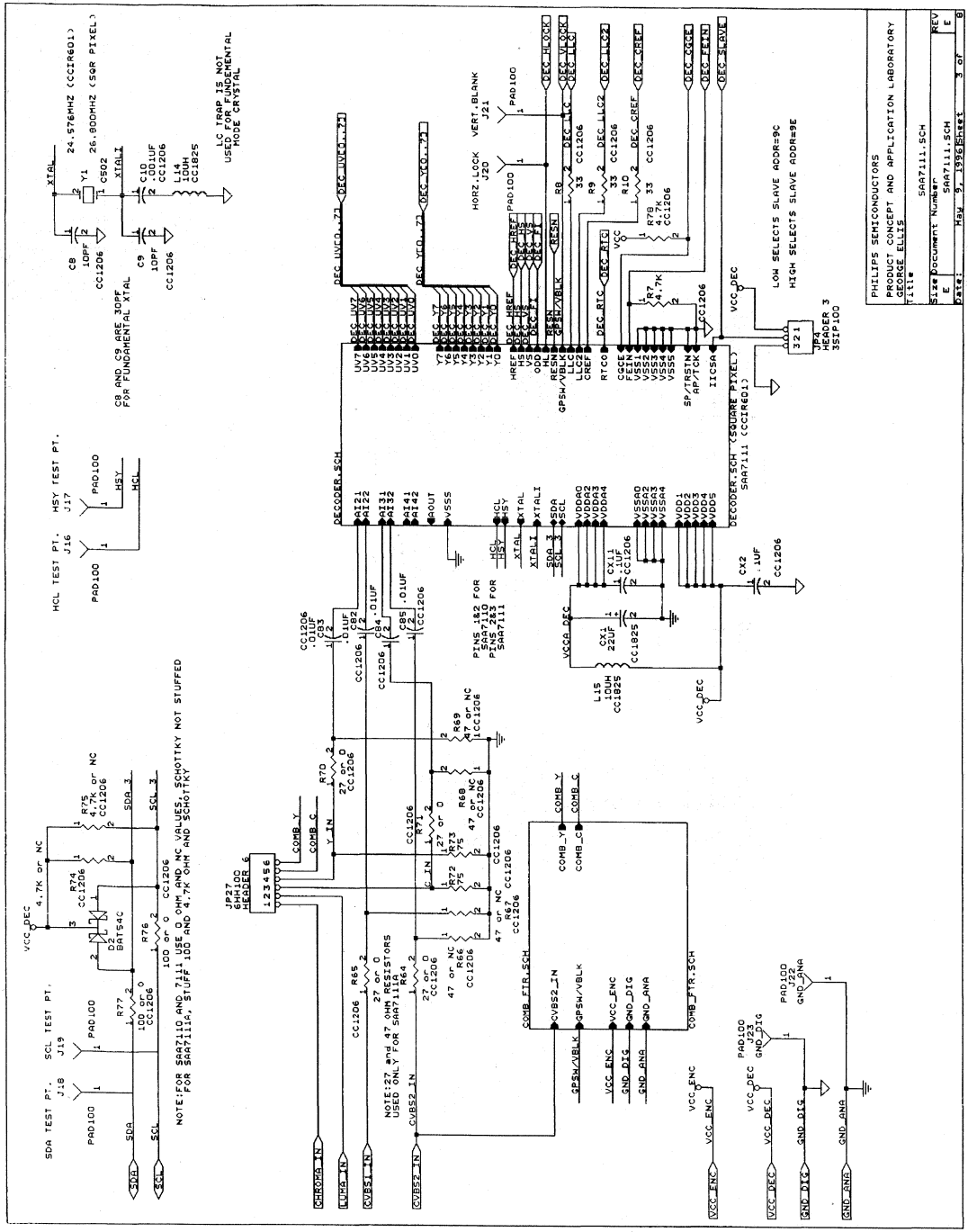
There are eight pages of schematics:

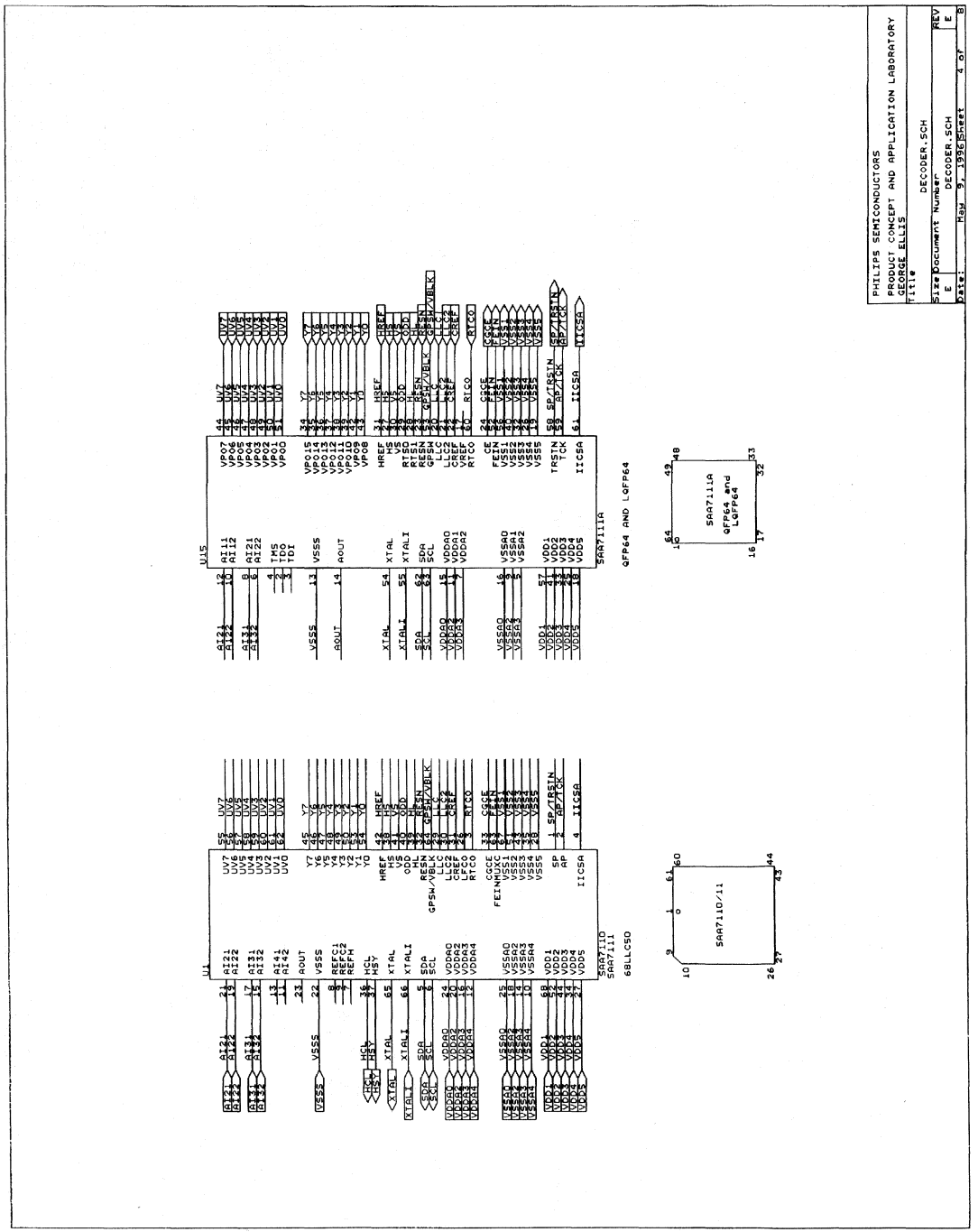
1. The root schematic–DENC2.SCH is used to access other schematis and outlines the block functions of the DPC71 evaluation board.
2. The power layout.
3. The circuit of the SAA7110 (or SAA7111) video decoder.
4. Decoder detail showing connections for alternative SAA7111 packages.
5. The D1 (CCIR656) input interface
6. The encoder, SAA7188A, SAA7184, SAA7185 or SAA7187 for video output, included is the S87C055 micro controller.
7. The SAA7182/3 (7124/5) video encoder and the composite sync generation circuit.
8. The comb filter block for the video decoder section.

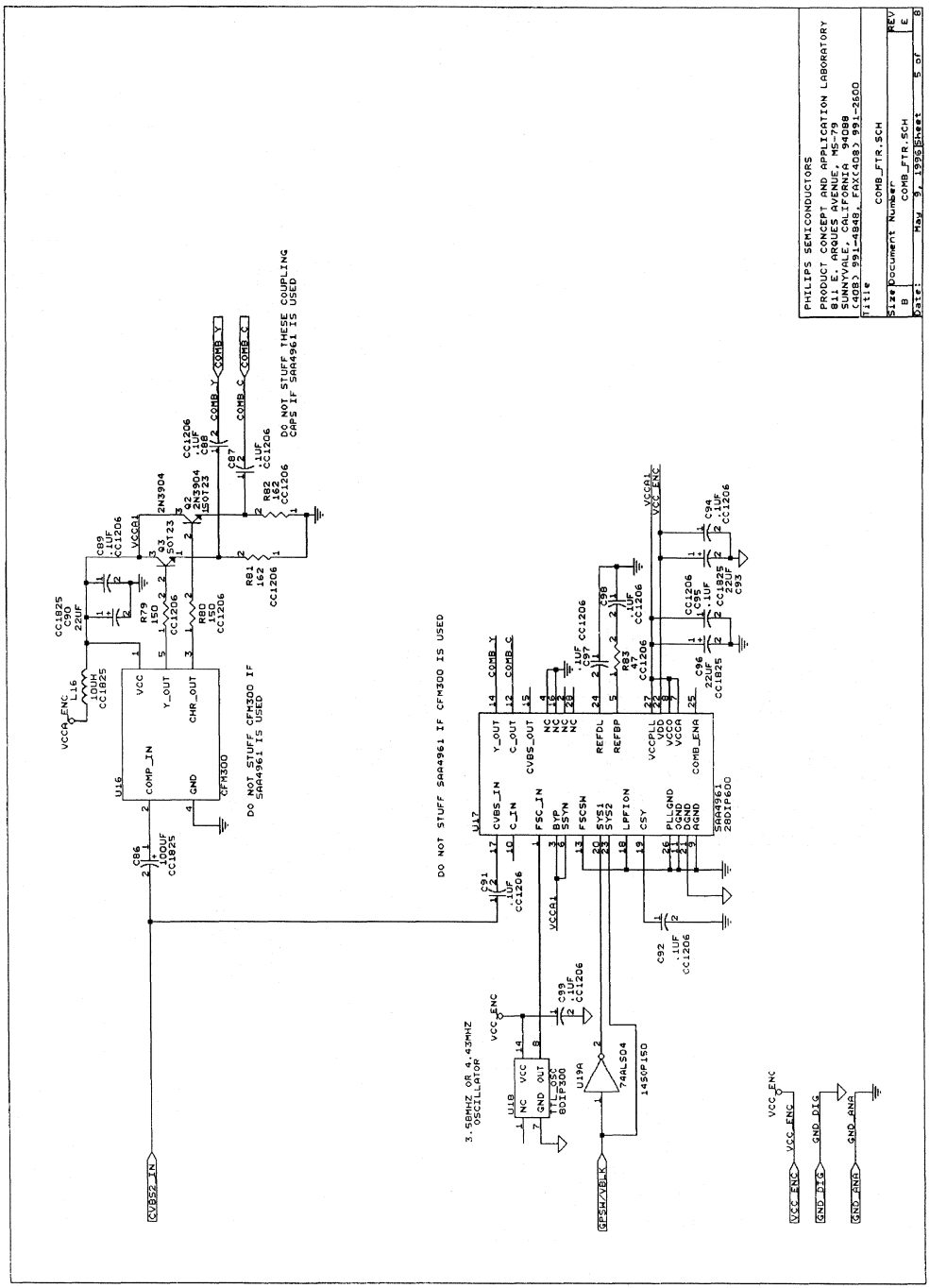
The schematics are done in ORCAD 386.

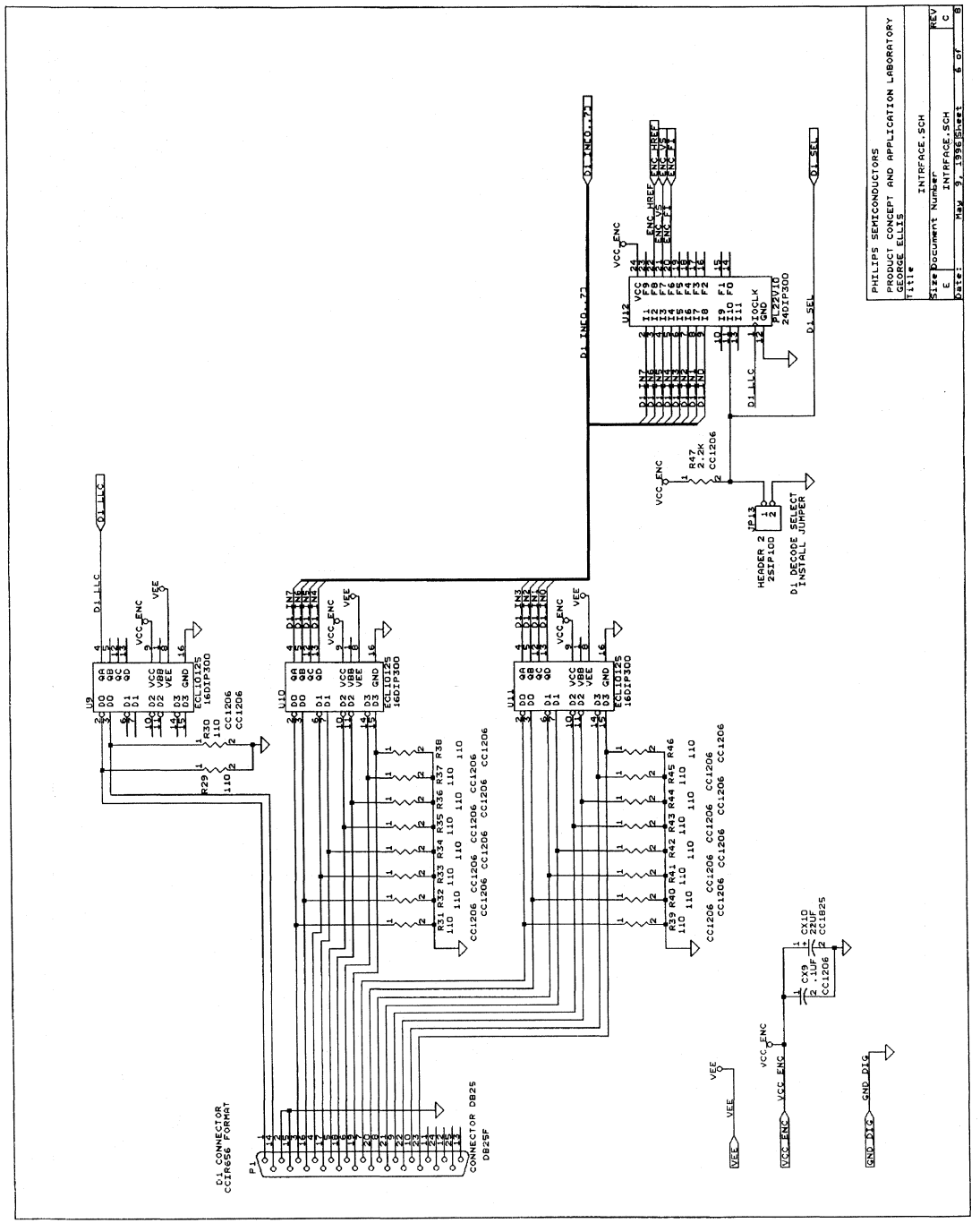

SAA7188.SCH
SAA7111.SCH
SAA7183.SCH
POWER.SCH
INTERFACE.SCH
S-VIDEO J15
S-VCON
VGA_FEMALE
CVBS_OUT
CHROMA_OUT
LUMA_OUT
XTAL_IN
XTAL_OUT
CSYNC
RED/OSD
GRN/OSD
BLU/OSD
VCTRL
RED_OUT
GRN_OUT
BLU_OUT
ENC_YUVCO..7
ENC_UVCO..7
ENC_YCO..7
ENC_RESN
ENC_HS
ENC_VS
SCL
SDA
DEC_YUVCO..7
DEC_VCO..7
DEC_UVCO..7
DEC_RESN
DEC_HREF
DEC_VS
DEC_LLC2
DEC_CREF
DEC_RTC
D1_SEL
D1_LLC
D1_INCO..7
VCC_ENC
VCC_DEC
VEE
GND_DIG
GND_ANA
PHILIPS SEMICONDUCTORS
PRODUCT CONCEPT AND APPLICATION LABORATORY
811 E. ARQUES AVENUE, MS-79
SUNNYVALE, CALIFORNIA 94088
TITLE DENC2.SCH
Size E Document Number DENC2.SCH REV E
Date: May 9, 1996 Sheet 1 of 8
DTV INPUT (16 BIT YUV 4:2:2)
PHILIPS INTERFACE
HEADER 15X2 30HM100
HEADER 30X2 60HM100
HEADER 4
4SIP100
2SIP100
CVBS1_IN
CVBS2_IN
CHROMA_IN
LUMA_IN
R1 75 CC1206
R2 75 CC1206
R5 10K CC1206
R6 10K CC1206
J11 RCA
J12 RCA
J13
J14 RCA
JP1
JP2
JP3
JP23
JP24
JP25
JP26


PHILIPS SEMICONDUCTORS
PRODUCT CONCEPT AND APPLICATION LABORATORY
811 E. ARQUES AVENUE, MS 27B
SUNNYVALE, CALIFORNIA 94088
(408) 991-4848, FAX(408) 991-2600
Title
POWER.SCH
Size Document Number REV
E E
Date: May 9, 1996 Sheet 2 of 2
ALL HEADERS ON THIS SHEET ARE SET AS FOLLOWS:
PINS 3&2 ARE CONNECTED FOR EXTERNAL POWER SUPPLY USE
PINS 2&1 ARE CONNECTED IF BOARD IS TO BE POWERED BY IBM PC/AT
THIS IS 5VDC FOR SAA7110 AND 7111
3.3VDC FOR SAA7111A
NOTE: FOR SAA7111A USE 7803
IBM_+12V
IBM_-5V
GND
VCC_ENC
VCC_DEC
VEE
-9VDC
+9VDC
GND_DIG
IBMJ1
J29
J26
J27
J28
L3
L4
L5
C28
C29
C30
C31
C32
C33
C34
C35
C36
C37
C38
C39
C40
JP6
JP8
HEADER 3
35IP100
PAD100
CONNECTOR COAX-F
TO220H
TO220
VR3
VR4
7805
7905
IN
OUT
GND


DECODER.SCH
DECODER.SCH (SQUARE PIXEL)
SAA7111 (CCIR601)
COMB_FIR.SCH
PHILIPS SEMICONDUCTORS
PRODUCT CONCEPT AND APPLICATION LABORATORY
GEORGE ELLIS
SAA7111.SCH
SAA7111.SCH
May 9, 1996
LOW SELECTS SLAVE ADDR=9C
HIGH SELECTS SLAVE ADDR=9E
NOTE:FOR SAA7110 AND 7111 USE 0 OHM AND NC VALUES, SCHOTTKY NOT STUFFED
FOR SAA7111A, STUFF 100 AND 4.7K OHM AND SCHOTTKY
C8 AND C9 ARE 30PF
FOR FUNDAMENTAL XTAL
LC TRAP IS NOT
USED FOR FUNDEMENTAL
MODE CRYSTAL
24.576MHZ (CCIR601)
26.900MHZ (SQR PIXEL)
HCL TEST PT. J16
HSY TEST PT. J17
SDA TEST PT. J18
SCL TEST PT. J19
HORZ_BLANK J21
VERT_BLANK J20
PINS 182 FOR SAA7110
PINS 283 FOR SAA7111
CHROMA_IN
LUMA_IN
CVBS1_IN
CVBS2_IN
VCC_DEC
VCC_ENC
GND_DIG
GND_ANA
HEADER 3
3SIP100


PHILIPS SEMICONDUCTORS
PRODUCT CONCEPT AND APPLICATION LABORATORY
CORSE ELLIS
Title
DECODER.SCH
Size Document Number REV
E DECODER.SCH E
Date: May 9, 1996 Sheet 4 of 8
U15
SAA7111A
QFP64 AND LQFP64
U1
SAA7110
SAA7111
68LLC5D
SAA7110/11
SAA7111A
QFP64 and LQFP64


PHILIPS SEMICONDUCTORS
PRODUCT CONCEPT AND APPLICATION LABORATORY
811 E. ARQUES AVENUE, MS-79
SUNNYVALE, CALIFORNIA 94088
(408) 991-4848, FAX(408) 991-2600
Title
COMB_FTR.SCH
Size Document Number REV
B COMB_FTR.SCH E
Date: May 9, 1996 Sheet 5 of 8
DO NOT STUFF SAA4961 IF CFM300 IS USED
DO NOT STUFF CFM300 IF SAA4961 IS USED
DO NOT STUFF THESE COUPLING CAPS IF SAA4961 IS USED
U16
CFM300
U17
SAA4961
28DIP600
U18
74ALS04
U19A
3.58MHZ OR 4.43MHZ OSCILLATOR
VCC_ENC
GND_DIG
GND_ANA
CVBS_IN
GPSW/VBLK
COMB_Y
COMB_C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PRODUCT CONCEPT AND APPLICATION LABORATORY
GEORGE ELLIS
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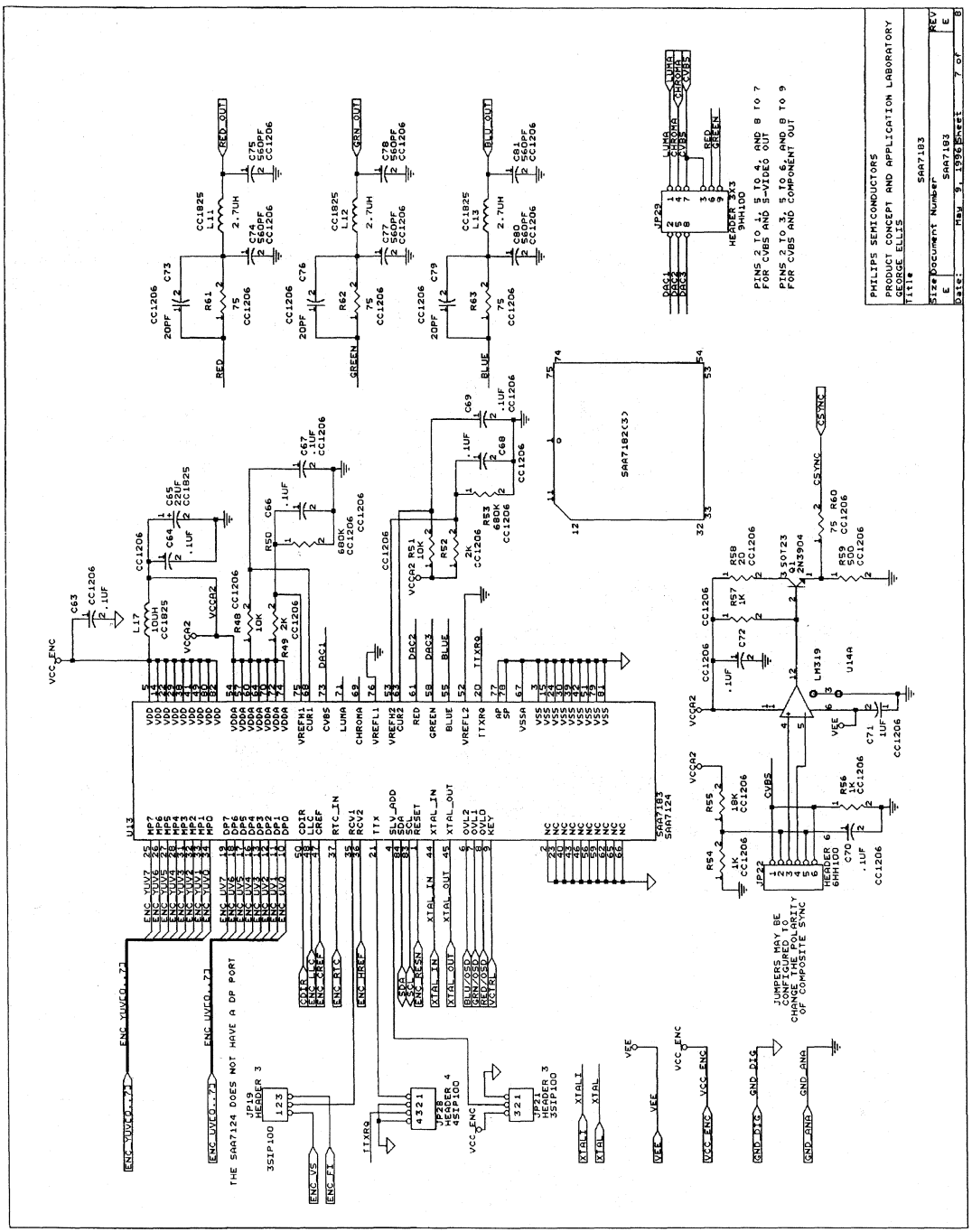
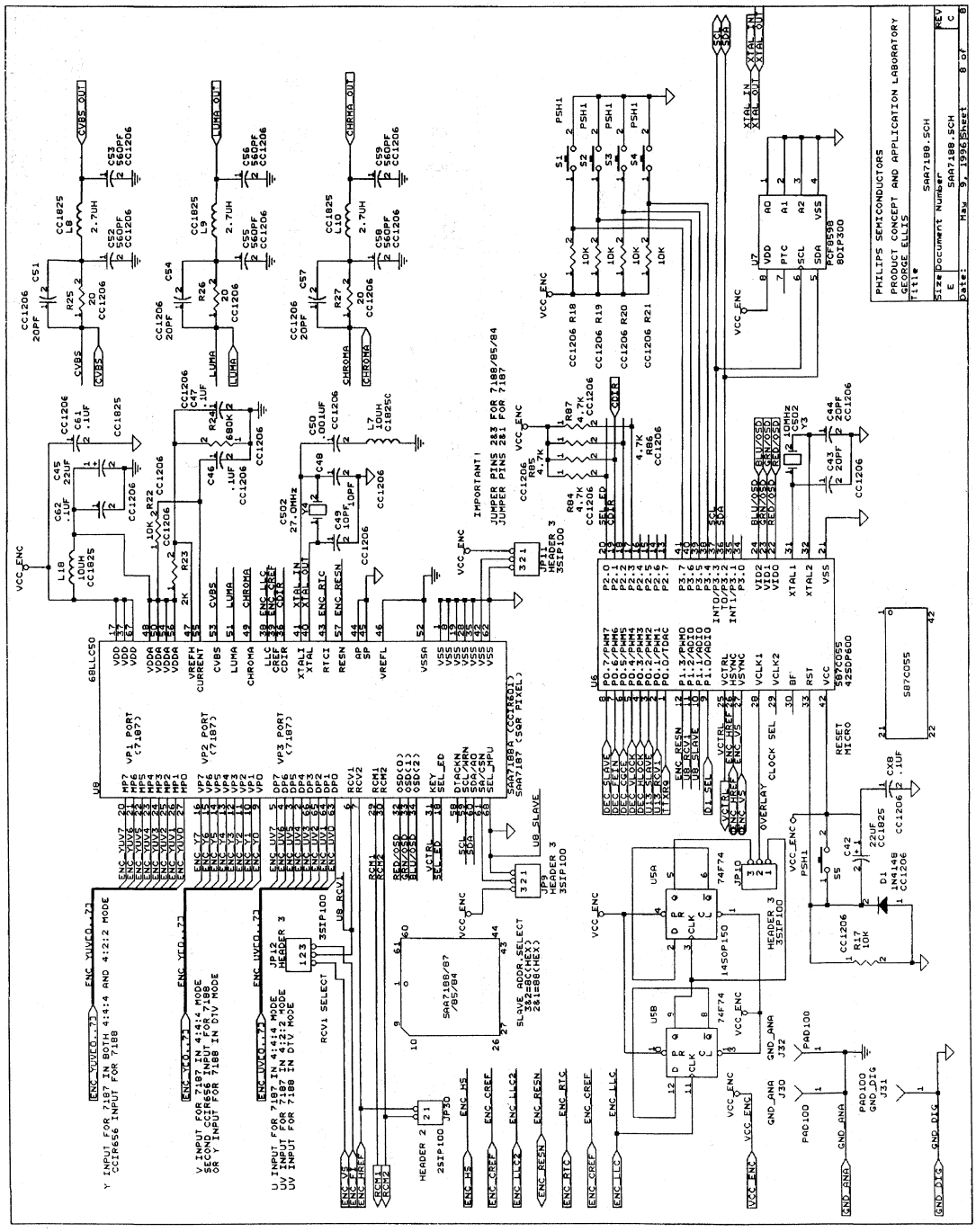
INTRFACE.SCH
Size: E
Document Number: INTRFACE.SCH
REV: C
Date: May 7, 1996 Sheet 6 of 8
D1 CONNECTOR
CCIR656 FORMAT
CONNECTOR DB25
DB25F
D1 DECODE SELECT
INSTALL JUMPER
HEADER 2
25IP100
PL22V10
24DIP300
ECL10125
16DIP300
CC1206
D1 LLC
D1 SEL
VCC_ENC
VEE
GND_DIG


PHILIPS SEMICONDUCTORS
PRODUCT CONCEPT AND APPLICATION LABORATORY
GEORGE ELLIS
SAA7183
SAA7183
May 9, 1996
7 of 8
SAA7182(3)
SAA7183
SAA7124
LM319
2N3904
THE SAA7124 DOES NOT HAVE A DP PORT
JUMPERS MAY BE CONFIGURED TO CHANGE THE POLARITY OF COMPOSITE SYNC
PINS 2 TO 4 AND 8 TO 7 FOR CVBS AND S-VIDEO OUT
PINS 5 TO 3 AND 6 TO 9 FOR CVBS AND COMPONENT OUT
HEADER 3X3
HEADER 6
HEADER 4
HEADER 3
RED_OUT
GRN_OUT
BLU_OUT
CSYNC
VCC_ENC
GND_DIG
GND_ANA
VEE
XTALI
XTALO



Clock and synchronization signals of SAA7187 and SAA7188 Application note for digital video encoder

Author: Leo Warmuth

1.0 INTRODUCTION

The devices of the SAA7187/88 family of video encoders can be used in a variety of applications differing regarding the signal flow of timing information. Video timing is defined by clock signals, synchronization signals and blanking signals. The video encoder ICs can generate these signals by itself (master mode), or can accept them as input (slave mode). The master/slave characteristic can be chosen independently for clock and sync-signals.

This application note describes the various clock and synchronization signals, their functions, and how to select and program them. The timing relation of some of these signals is programmable. An application example shows a possible configuration.

2.0 CLOCK LLC AND CREF SIGNAL

The SAA7187/88 has two clock signals: LLC and CREF, functionally compatible with other Philips digital video processing circuits. LLC on pin 38 is the Line-Locked-Clock in double pixel clock frequency. CREF on pin 39 is the clock qualifier signal, accompanying LLC, to indicate on which LLC edges the 16 bit wide YUV data stream transports valid data. CREF is continuously toggling in pixel rate frequency, but is not meant as pixel clock. The transitions of CREF have to maintain certain setup and hold times relative to clock LLC (see data sheet). The digital encoder ICs can generate and provide (drive) the clock signals by its own by means of the built-in crystal oscillator, or receive the clock signals from external. In remote genlock mode, LLC and CREF can be fed from one of the Philips digital decoder (DMSD), but must then be accompanied by RTC signal (real time control information).

2.1 Built-in clock signal generator

SAA7187/88 has built-in an optional crystal oscillator for LLC frequency. A crystal with double pixel clock frequency as base frequency, or as third harmonic frequency, with appropriate auxiliary circuitry, can be connected between the pins XTALi (input, pin 41) and XTALo (output, pin 40). The swing at the XTAL-pins is about 1Vpp, and is DC-compensated via an internal resistor between the two pins. Alternatively an external crystal oscillator could directly drive into XTALi.

An internal switch, hardware controlled by CDIR at pin 36, selects whether the IC provides or receives clock signals LLC and CREF (see Table 1). If CDIR is low, clock is taken from the internal crystal oscillator and the IC outputs LLC at pin 38 and CREF at pin 39. If CDIR is high, LLC pin and CREF pin are both switched to be input. The IC then requires a double pixel clock LLC from external circuitry at pin 38. Under certain conditions, CREF input at pin 39 has data-phase (timing) relevance, but it does not have directly clock and data qualifying function.

2.2 External Clock

In the "clock slave mode" case, i.e., if clock is provided from external into LLC pin 38, a CREF-like signal can optionally be applied to pin 39, but this is not required. If the IC sees a toggling signal, i.e., edges, at pin 39, CREF will contribute to re-synchronization of the internal horizontal counter (once per line) and – by that – defines the active data phases in the 16 bit wide YUV input data stream. If horizontal synchronization from external via RCV1 or RCV2 is selected, i.e., the encoder IC is in slave mode regarding horizontal timing, CREF defines together with the selected horizontal reference input signal, when the horizontal trigger counter has to start. From there the programming parameter HTRIG (11 bits in subaddress 6E and 6F) defines the start of the horizontal pixel counter, and the LSB of the parameter HTRIG determines one of the two possible phases of the internally effective CREF relative to the external provided CREF. The horizontal reference edge is defined regarding source and polarity by the various bits in subaddress 6Chec (see also later in this application note: re-trigger).

If no CREF is provided to the IC, a horizontal reference signal input is sampled direct with LLC resolution. The phase of the internal CREF, and expected valid data phases, are defined by the selected horizontal reference edge, and by the LSB of HTRIG. The horizontal reference edge is defined regarding source and polarity by the various bits in subaddress 6Chec (see also later in this application note: re-trigger).

Table 1. Selection of Clock Modes

CDIR	LLC	CREF	XTALo	XTALi	RTCI	RTCE
Pin 36	Pin 38	Pin 39	Pin 40	Pin 41	Pin 43	subaddress 61hex
low	output	output	local crystal		don't care	don't care
low	output	output	don't care	external oscillator	don't care	don't care
high	input	don't care but constant	don't care		don't care	0
high	input	input	don't care		don't care	0
high	input from DMSD/CGC	don't care but constant	don't care		RTCO from DMSD	1
high	input from DMSD/CGC	input from DMSD/CGC	don't care		RTCO from DMSD	1

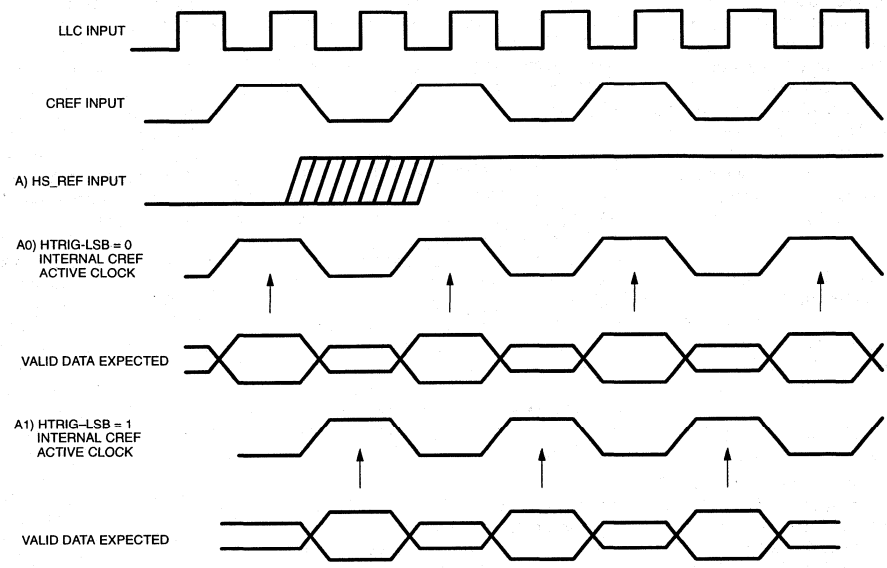


Figure 1. Timing of internal CREF and expected valid data input, if CREF and horizontal reference is provided from external into the encoder IC

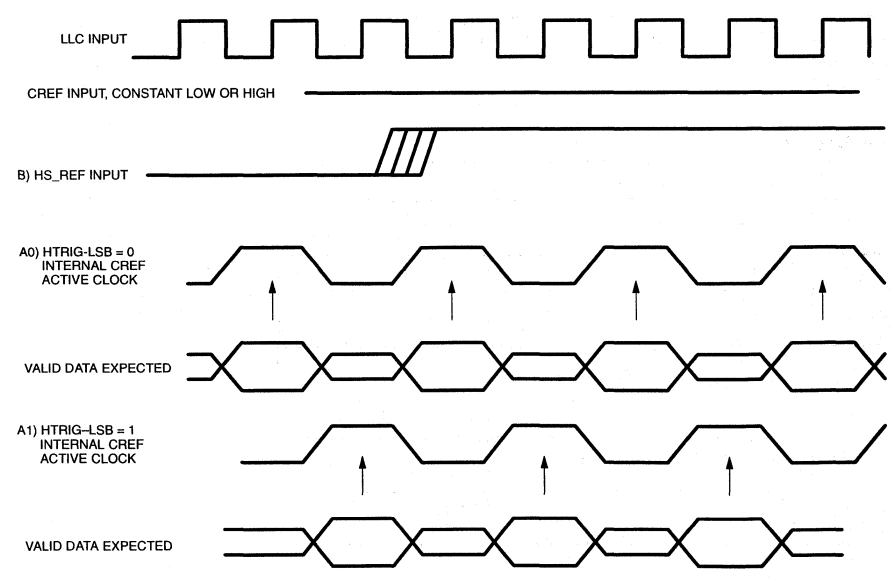


Figure 2. Timing of internal CREF based on horizontal reference signal input only

2.3 Clock accuracy

The digital encoder SAA7187 and SAA7188A synthesize all horizontal and vertical timing as well as the color subcarrier oscillation from the provided clock LLC, respectively crystal. If the clock frequency deviates from its nominal value, line and field frequency will change accordingly. Consumer type receiver equipment is rather tolerant regarding these raster frequencies, and can normally accept and follow several % deviations from the standard raster frequencies.

But the subcarrier frequency has much higher requirements regarding accuracy and stability to ensure proper color decoding. Broadcast quality class specification asks for less than 2ppm deviation of subcarrier frequency. Consumer type equipment may accept up to 50ppm static deviation, but dynamic deviation should be kept much smaller and very slow.

In case the crystal or the provided LLC at the digital encoder does not have the correct frequency, the synthesized color subcarrier frequency can still be adjusted to the required frequency value, by programming the 32 bit of "FSC" under subaddress 63hex to 66hex appropriate. Subcarrier phase reset PHRES in subaddress 70hex has then to be switched off, i.e., set to 00. In general, such an adjustment of "FSC" would produce a non-standard video output signal regarding subcarrier to line phase coupling, comparable to a regular VCR signal. The resulting video signal shows correct subcarrier frequency and (slightly) incorrect raster frequencies. It can be decoded and displayed correctly by any equipment that could handle VCR signals, e.g. by a consumer type television set.

2.4 Remote Genlock

In remote genlock mode the digital encoder runs with the line locked clock LLC, generated by a digital multi standard decoder (DMSD) respectively clock generator (CGC), like SAA7110, SAA7196, SAA7197 or SAA7157. In the decoding process the line locked clock LLC is derived from an analog video input signal as reference. If this input video signal is not stable or non standard, e.g., a camcorder play back signal, the DMSD will control LLC to stay line locked, which may result into a non-nominal clock frequency. The Philips digital decoder provides an RTC-signal (real time control information) to enable the digital encoder (DENC) to compensate such non-nominal clock, if decoder and encoder are running the same system, i.e., same sampling scheme (CCIR or SQP) and same video norm (field frequency, subcarrier frequency). Decoder LLC and RTCO output signal from DMSD must be connected to LLC and RTCI input signal of DENC. Horizontal and vertical sync signal of both systems can run with phase offset. The data path can have any processing delay, or may be not closed at all.

SAA7187 can be paired for remote genlock operation with the SAA7110, or SAA7191B plus SAA7197, or with SAA7196.

SAA7188A can be paired for remote genlock operation with SAA7151B plus SAA7157.

Clock and synchronization signals of SAA7187 and SAA7188 Application note for digital video encoder

3.0 RASTER CONTROL OUTPUT SIGNALS

The NTSC / PAL video encoder has an internal synchronization circuitry. For the purpose of this application note it is referred to as horizontal counter – counting in clocks along a horizontal line – and as vertical counter – counting in half lines through a video field. A third counter for color field sequence identification is implemented to support the interlace characteristic of the video signal as well as to distinguish the NTSC four color field sequence, and PAL eight color field sequence. The IC has four Raster Control pins (RCxx), which reflect the timing and status of the internal synchronization circuitry. Two of them carry vertical / field synchronization signals, and two carry horizontal / line synchronization information. One of each pair is output only, the other one can be defined as output or as input, to re-trigger the internal synchronization circuitry. (The nomenclature of these four pins is related to data flow in a particular application, but should not be understood as restriction.) All four signals are defined on one and the same internal synchronization circuitry.

3.1 Vertical – Field – Reference Output Signals

The digital encoder SAA7187 and SAA7188A have two pins to output field reference Raster Control signals. RCM1 on pin 29 has output only functionality, and a fixed (nominal) signal polarity. RCV1 on pin 6 has selectable signal polarity and can be used as output or as input to re-trigger internal timing (see later in this application note).

3.1.1 Field Reference Signal Types

For both field reference outputs, one signal out of a set of the following three signal types can be selected independently.

VS Vertical Sync signal is nominal active (nominal high) for 3 lines if 60Hz timing is selected, or for 2.5 lines if 50Hz timing is selected, i.e., during those half lines, in which the analog CVBS output contains the main vertical sync pulses..

FS Frame Sync signal is an odd_/even signal, that is active (nominal low) during every first i.e. odd field, and inactive (nominal high) during every second, i.e., even field in the 2:1 interlace scheme of two fields in one frame. The first field is that field, in which the first main vertical sync pulse (serration pulse) starts in coincidence with the begin of a line.

FSEQ The color Field SEQuence signal indicates the start of the color field sequence (see CCIR report 624, e.g.). FSEQ is active (nominal high) during the first field of the 4-(NTSC) or 8-(PAL) color field sequence for standard encoding. FSEQ is inactive (nominal low) through all the other fields.

The position of the output signals VS, FS and FSEQ as RCM1 at pin 29, as well as RCV1 at pin 6, has a fix timing relationship to the internal horizontal and vertical counters and is not directly effected by programming of HTRIG or VTRIG. The leading (nominal rising) edge of VS, and all edges of FS and FSEQ occur at nominal field start (according to CCIR nomenclature), and on half line boundaries. For standard interlaced mode and nominal field length, FS is low for 262.5 (312.5) lines and high for 262.5 (312.5) lines, for example. The leading (nominal falling) edge of FS or the leading (nominal rising) edge of FSEQ indicates the begin of a frame, the begin of a field, and also the begin of a line, and can be used to reset/trigger external vertical as well as horizontal synchronization counter.

If the encoder is forced into non-interlaced mode through external re-trigger, the FS function is meaningless. If non-standard encoding regarding subcarrier-to-line coupling is applied, selection of FSEQ function is meaningless.

Selecting any of these signal for output as RCM1 on pin 29 or as RCV1 on pin 6 has no direct effect on internal blanking or other processing in the encoder IC itself. RCM1 and RCV1 as output are just auxiliary timing signals for use by the application environment, to support the video signal source (e.g., MPEG decompression circuitry, or video memory controller, or graphics generator) to time its data stream output.

3.1.2 Pin 29 : RCM1

Pin 29 RCM1 has output only function and carries field synchronizing raster control information. Via two SRCM bits in subaddress 6Dhex one of three types of field sync signals can be selected.

Table 2. Selection of RCM1 signal function on Pin 29

F = relevant function, x = other function/signal definition, – = don't care

BITS UNDER SUBADDRESS 6Dh								BITS UNDER SUBADDRESS 61h								SHORT NAME	FUNCTION RESULTING SIGNAL
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0		
								–	x	x	x	x	x	x	F	FISE	select field frequency (V–pulse sequence) select number of clocks/line (selects FSEQ as 4 or 8 field sequence)
–	–	–	–	F	F	x	x									SRCM	select RCM1 signal function
				0	0										0	VS 50Hz	active **high** for **2.5** lines at begin of every field
				0	0										1	VS 60Hz	active **high** for **3** lines at begin of every field
				0	1										0	FS 50Hz	**low** in **first** (odd) field, **312.5** lines high in second (even) field, 312.5 lines
				0	1										1	FS 60Hz	**low** in **first** (odd) field, **262.5** lines high in second (even) field, 262.5 lines
				1	0										0	FSEQ 50Hz	**high** in the **first** field **of 8** field sequence
				1	0										1	FSEQ 60Hz	**high** in the **first** field **of 4** field sequence
				1	1										x	n.a.	reserved, do not use

3.1.3 Pin 6 as Output: RCV1

Pin 6 RCV1 can assume output as well as input function and carries field synchronizing raster control information. Via two SRCV1x bits, PRCV1 bit and ORCV1 bit in subaddress 6Chex one of three types of field sync signals can be determined for RCV1 output.

Table 3. Selection of RCV1 output signal function on pin 6

F = relevant function, x = other function/signal definition, – = don't care

BITS UNDER SUBADDRESS 6Ch								BITS UNDER SUBADDRESS 61h								SHORT NAME	FUNCTION RESULTING SIGNAL
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0		
								–	x	x	x	x	x	x	F	FISE	select field frequency (V-pulse sequence) select number of clocks/line (defines FSEQ as 4 or 8 field sequence)
x	x	x	x	F	x	x	x									PRCV1	Select RCV1 signal polarity
x	x	x	F	x	x	x	x									ORCV1	Input or Output of RCV1 signal
F	F	x	x	x	x	x	x									SRCV1	Select RCV1 signal function
x	x		0	x											–	input	RCV1 is input, see Table 6
0	0		1	0											0	VS 50Hz	Active **high** for **2.5** lines at begin of every field
0	0		1	1											0	VS 50Hz	Active **low** for **2.5** lines at begin of every field
0	0		1	0											1	VS 60Hz	Active **high** for **3** lines at begin of every field
0	0		1	1											1	VS 60Hz	Active **low** for **3** lines at begin of every field
0	1		1	0											0	FS 50Hz	**Low** in first (**odd**) field, **312.5** lines High in second (even) field, 312.5 lines
0	1		1	1											0	FS 50Hz	**High** in first (**odd**) field, **312.5** lines Low in second (even) field, 312.5 lines
0	1		1	0											1	FS 60Hz	**Low** in first (**odd**) field, **262.5** lines High in second (even) field, 262.5 lines
0	1		1	1											1	FS 60Hz	**High** in first (**odd**) field, **262.5** lines Low in second (even) field, 262.5 lines
1	0		1	0											0	FSEQ 50Hz	**High** in the **first** field of **8** field sequence
1	0		1	1											0	FSEQ 50Hz	**Low** in the **first** field of **8** field sequence
1	0		1	0											1	FSEQ 60Hz	**High** in the **first** field of **4** field sequence
1	0		1	1											1	FSEQ 60Hz	**Low** in the **first** field of **4** field sequence
1	1		–	–											x	n.a.	reserved, do not use

3.2 Horizontal – Line – Reference Output Signals

The digital encoder SAA7187 and SAA7188A have two pins to output line reference Raster Control signals. RCM2 on pin 30 has output only functionality, and a fixed (nominal) signal polarity. RCV2 on pin 7 has selectable signal polarity and can be used as output, or as trigger input to re–synchronize internal timing, or as 'blanking' input to gate input data stream (see later in this application note).

Both horizontal raster control output signals can be freely defined along the line, and are active (nominal high) between "begin" and "end" (see Table 4). Begin and end can be chosen independently for RCM2 and RCV2. Both pairs are relative to the same internal horizontal counter, and are defined in LLC clocks. The internal horizontal counter manifests its timing in the analog output, and can depend on re–trigger via RCV1 or RCV2 input signals and programming of HTRIG under subaddress 6Ehex and 6Fhex (see later in this application note).

RCM2 and RCV2 as output are auxiliary timing signals for use by the application environment, e.g., to help the data source (MPEG decompression circuitry, video memory controller or graphics overlay generator) to time its data stream, or disable it. The programming of RCM2 and RCV2 as output does not effect internal blanking, data enabling, or any timing or processing in the encoder IC itself.

3.2.1 Pin 30: RCM2

Pin 30 RCM2 has output only function. RCM2 is active high between 'Begin = BMRQ' and 'End = EMRQ' in every line, i.e., also during vertical blanking interval VBI. Programming of FAL and LAL has no effect on RCM2. If End is programmed before (i.e., with a lower number than) Begin, RCM2 may be seen/understood as an active low signal between End and Begin.

3.2.2 Pin 7 as Output : RCV2

Pin 7 RCV2 can assume output as well as input function (see Tables 3, 4, and 5).

Program bit ORCV2 = 1 defines pin 7 for RCV2 output signal. RCV2 output is active (nominal high) from programmed 'Begin = BRCV' to 'End = ERCV'. The polarity is defined by program bit PRCV2.

Program bit CBLF defines whether RCV2 output is active in every line (CBLF = 0), regardless of vertical position, or whether RCV2 output is only active during selected vertical active range (CBLF = 1). Vertical active range is defined between 'first active line' FAL and 'last active line' LAL under subaddress 7Bhex to 7Dhex. By that, RCV2 as output signal could be used as horizontal line timing reference signal ("HREF") or as composite blanking signal ("CBN"), to enable data output at the video signal source. But if pin 7 is programmed as RCV2 output signal, its signal and related programming has no effect for any timing, blanking, data enabling or processing in the encoder IC itself. FAL and LAL defines internal vertical blanking, independently of whether CBLF is selecting it for gating of RCV2 output or not.

Table 4. Definition of output timing of RCM2 (pin 30) and RCV2 (pin 7)

PROGRAM WORD	11 BIT ADDRESS IN HORIZONTAL DIRECTION LLC RESOLUTION	RCM2 PIN30 OUTPUT ONLY	RCV2 PIN7 ONLY IF OUTPUT
BRMQ	subaddress 71hex, 73hex	L-to-H transition, rising edge	
ERMQ	subaddress 72hex, 73hex	H-to-L transition, falling edge	
BRMQ	subaddress 77hex, 79hex		begin of 'active' phase
ERMQ	subaddress 78hex, 79hex		end of 'active' phase

Table 5. Selection of RCV2 output signal function on pin 7

F = relevant function, x = other function/signal definition, – = don't care

BITS IN SUBADDRESS 6Chex								SHORT NAME	FUNCTION DESCRIPTION
7	6	5	4	3	2	1	0		
x	x	x	x	x	x	x	F	PRCV2	Polarity of RCV2
x	x	x	x	x	x	F	x	ORCV2	I/O of RCV2
x	x	x	x	x	F	x	x	CBLF	RCV2 in VBI (see FAL and LAL)
					x	0	x	input	RVC2 is input, see Table 7
					0	1	0	"HREF"	RCV2 **output** is active **high** between BRCV till ERCV in every line of the entire field, i.e., **including** VBI
					0	1	1	"HREF_"	RCV2 **output** is active **low** between BRCV till ERCV in every line of the entire field, i.e., **including** VBI
					1	1	0	"CBN"	RCV2 **output** is active **high** between BRCV till ERCV in active lines only from FAL to LAL, i.e., **excluding** VBI
					1	1	1	"CB"	RCV2 **output** is active **low** between BRCV till ERCV in active lines only from FAL to LAL, i.e., **excluding** VBI

4.0 RASTER CONTROL INPUT SIGNALS, SYNC-SLAVE-MODE

The internal synchronization circuitry of the digital encoder SAA7187 and SAA7188A are always defined by FISE (number of clocks per line, subaddress 61hex), FLEN (number of lines per field, subaddress 7Ahex and 7Dhex), and PAL (defining color field sequence length, subaddress 61hex). In sync slave mode, those horizontal and vertical counters can be re-triggered by an external trigger event at pin 6 as RCV1 input and/or at pin 7 as RCV2 input. The rising or falling edge can be selected as timing reference (trigger event) to re-synchronize the internal synchronization circuitry, regarding horizontal or vertical counter, or odd-even flip-flop, or color field sequence counter. As long as no trigger event occurs the internal counters are free running in the defined loops. Any single occurance of the selected edge in RCV1 or RCV2 input will hard re-trigger — i.e., it is not a smoothed PLL procedure. Due to processing pipeline delay, the resulting re-synchronization does not take effect before the next following corresponding period. A programmable vertical and horizontal trigger offset can be applied via VTRIG and HTRIG.

RCV2 as input can also optionally be used as "composite blanking" signal to gate the input data stream, but only for data coming through V-port (and D-port).

VTRIG represents a negative delay between external trigger event and internal vertical counter start, i.e., start of main vertical sync (serration) pulses. The external re-synchronization event at RCV1 over–writes the vertical counter state with VTRIG value, which then synchronizes the next vertical period to the external trigger signal. VTRIG is defined with 5 bits under subaddress 70 hex. The programmed VTRIG number corresponds with the position of the external trigger event along the field, counted in half lines. Programming 00 will synchronize the internal vertical counter to generate vertical sync at the begin of that same half line, in which the external trigger event occurs. Programming of 1F hex results in vertical sync output 31 half lines ahead of the external trigger input, for example.

HTRIG represents a negative delay between external trigger event and internal horizontal counter start, i.e., leading edge of horizontal sync pulse. The external re-synchronization event at RCV1 or RCV2 over-writes the horizontal counter state with HTRIG value, which then synchronizes the next horizontal period to the external trigger signal. HTRIG is defined with 11 bits under subaddresses 6E hex and 6F hex in LLC clock resolution, and covers the whole line period. The programmed HTRIG number corresponds with its position (in LLC clocks) along the scan line.

4.1 Pin 6 as Input: RCV1

If pin 6 is selected as input, RCV1 signal could carry field synchronization information in a form like vertical sync VS, or frame sync FS, or field sequence identification FSEQ. The actual re-trigger function of RCV1 input is defined via the two SRCV1 bits, TRCV2 bit, ORCV1 bit and PRCV1 bit, all in subaddress 6Chex, and the PAL bit in subaddress 61hex. Table 6 describes signal meaning and effect of RCV1 as input at pin 6.

Table 6. Selection of RCV1 input signal function on pin 6

F = relevant function, x = other function/signal definition, – = don't care

BITS UNDER SUBADDRESS 6Ch								BITS UNDER SUBADDRESS 61h							SHORT NAME	RCV1 INPUT PIN 6	FUNCTION: Active edge results in retrigger of following counters:			
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0			HORIZONTAL	VERTICAL	ODD/EVEN	COLOR FIELD SEQ
0	0	0	0	0											x	VS	rising	horizontal	vertical	(n-interl.)	
0	0	0	0	1											x	VS	falling	horizontal	vertical	(n-interl.)	
0	0	1	0	0											x	VS	rising		vertical		
0	0	1	0	1											x	VS	falling		vertical		
0	1	0	0	0											x	FS	rising	horizontal	vertical	odd field	
0	1	0	0	1											x	FS	falling	horizontal	vertical	odd field	
0	1	1	0	0											x	FS	rising		vertical	odd field	
0	1	1	0	1											x	FS	falling		vertical	odd field	
1	0	0	0	0											0	FSEQ8	rising	horizontal	vertical	odd field	1st of 8 fields
1	0	0	0	1											0	FSEQ8	falling	horizontal	vertical	odd field	1st of 8 fields
1	0	1	0	0											0	FSEQ8	rising		vertical	odd field	1st of 8 fields
1	0	1	0	1											0	FSEQ8	falling		vertical	odd field	1st of 8 fields
1	0	0	0	0											1	FSEQ4	rising	horizontal	vertical	odd field	1st of 8 fields
1	0	0	0	1											1	FSEQ4	falling	horizontal	vertical	odd field	1st of 8 fields
1	0	1	0	0											1	FSEQ4	rising		vertical	odd field	1st of 8 fields
1	1	1	0	1											1	FSEQ4	falling		vertical	odd field	1st of 8 fields
1	1	x	x	x											x	n.a		reserved, do not use			
x	x	x	1	x											x	n.a.	output	RCV1 is output, see Table 3			
								–	x	x	x	x	x	x	F	FISE		Select field frequency (V-pulse sequence) select clocks per line defines FSEQ as 4 or 8 field sequence			
x	x	x	x	F	x	x	x									PRCV1		Select RCV1 signal porlarity			
x	x	x	F	x	x	x	x									ORCV1		Input or Output of RCV1 signal			
x	x	F	x	x	x	x	x									TRCV2		RCV1 or RCV2 for horizontal trigger			
F	F	x	x	x	x	x	x									SRCV1		Select RCV1 signal function			

4.2 Pin 7 as Input: RCV2

If pin 7 is selected as input, RCV2 signal can carry just line synchronization information like horizontal sync HS, or input data gating function like HREF or CBN. The horizontal re-trigger function and the data input gating function can be utilized seoarately, or they combined. The actual function of RCV2 input is defined via the CBLF bit, ORCV2 bit, PRCV2 bit and TRCV2 bit, all in subaddress 6Chex. Table 7 describes signal meaning and effect of RCV1 as input at pin 6.

Table 7. Selection of RCV2 input signal function on pin 7

("x" defines other functions/signals)

BITS IN SUBADDRESS 6Chex								SHORT NAME	RCV2 INPUT	FUNCTION DESCRIPTION
7	6	5	4	3	2	1	0		pin 7	
							F	PRCV2		Polarity of RCV2
						F		ORCV2		I/O of RCV2
					F			CBLF		RCV2 in VBI (see FAL and LAL)
		F						TRCV2		Select horizontal trigger from RCV1/2
		0			0	0	–		any input	but not used for re-trigger or gating
		0			1	0	0		input high	enable V-port data input for encoding
									input low	disable V-port data input for encoding
		0			1	0	1		input low	enable V-port data input for encoding
									input high	disable V-port data input for encoding
		1			0	0	0		rising edge	horizontal re-trigger, with HTRIG
		1			0	0	1		falling edge	horizontal re-trigger, with HTRIG
		1			1	0	0		rising edge	horizontal re-trigger, with HTRIG
									input high	disable V-port data input for encoding
									input low	enable V-port data input for encoding
		1			1	0	1		falling edge	horizontal re-trigger, with HTRIG
									input low	disable V-port data input for encoding
									input high	enable V-port data input for encoding
		x			x	1	x		output	RCV2 is output, see Table 5

5.0 SYNC TIMING DEPENDENCIES

The selected "active" edge of the external timing reference signal RCV1 or RCV2 loads the internal horizontal counter with the HTRIG value. At the end of the line the counter is automatically reset, and all timing signals are in phase with the requesting re-trigger. This horizontal counter also defines the begin and end points of the raster control output signals.

The effect of VTRIG for vertical synchronization timing is very similar.

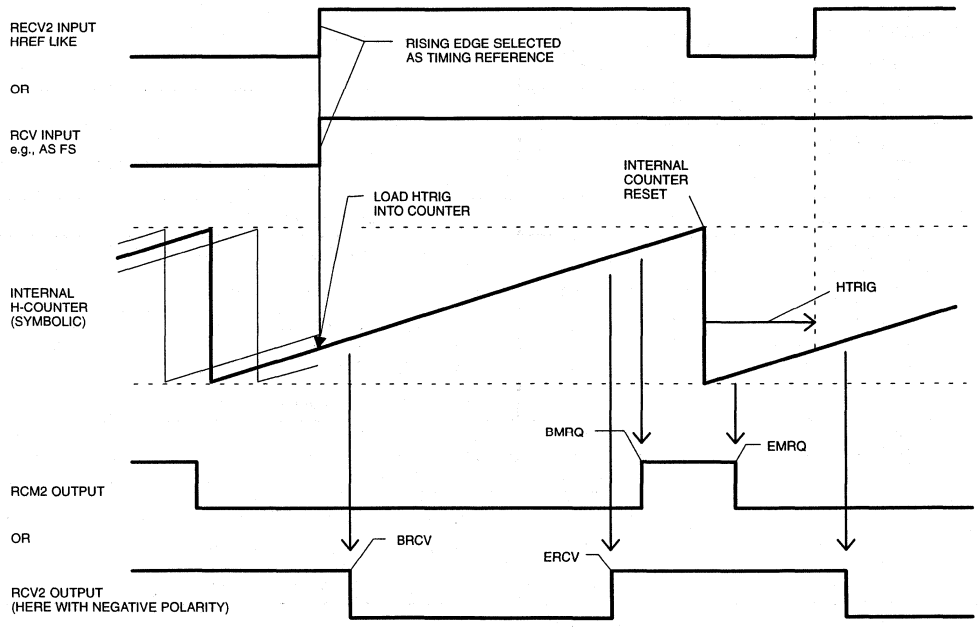


Figure 3. Horizontal ti ming for re-trigger and raster control output signal definition

Clock and synchronization signals of SAA7187 and SAA7188 Application note for digital video encoder

6.0 APPLICATION EXAMPLE

Figure 4 points out several of those features that can be realized in an application with SAA7188A (or SAA7187). Two or more digital video encoder devices can be locked to each other. All their analog video outputs are completely in phase: horizontally, vertically and also the subcarrier. One of the devices functions as timing master, the other ones work in sync slave mode. The master device provides on RCM1 the color field sequence indication signal FSEQ, which transports horizontal and vertical reference as well as subcarrier phase reference via the color field sequence indication. The RCV1 inputs of the other devices are set to FSEQ function and also used to trigger line timing. VTRIG and HTRIG are both set to zero.

RCM2 output of the master device can be freely defined in horizontal timing. By that it can be used as input data gating signal (HREF–gate) at the RCV2 inputs of the other encoder devices. This RCM2 output signal of the master device (or of each device) could also be fed back to its own RCV2 input for input data gating function.

RCM1 and RCM2 outputs of the slave devices can be used as trigger and timing signals for the digital video signal sources. RCM1 can be chosen as a vertical sync, or as an odd/even signal. RCM2 can be defined as an HS for trigger and counting purposes, or it can be used as a source gating signal. It can be placed 'early' to compensate for pipeline delay on the data delivery side, such as memory access, etc.

If the RCV2 pins of the slave (and/or the master) device are not used as gating input, they could be switched to output, and could be used as (early) enabling signal (CBN) at the signal source. In that case even VBI blanking is supported. (This option is not shown in Figure 4).

The digital encoder that works as timing master in the configuration of Figure 4 can be genlocked to an analog video reference signal via digital encoder circuitry. For this purpose, the SAA7188A can be combined with the SAA7151B, SAA7157 and TDA8708/09. The SAA7187 can be combined with the SAA7191B, SAA7197 and TDA8708/09 or with the SAA7110. The digital real-time decoder system locks itself to the analog reference video signal and generates line-locked clock, horizontal and vertical sync signals, and the real-time control signal RTC. If the encoder runs with the line-locked clock of the decoder, it is important to also have the RTC wire connected, in order to maintain the correct subcarrier frequency in the encoder, same as in the analog reference signal. To have the same clock at both the decoder and encoder side is very interesting in some applications; for example, as a frame buffer as it avoids the complications of an asynchronous two-clock system.

The SAA7151B or other decoder can provide a pair of vertical and horizontal syncs as VS and HS, or provide an odd/even signal FS ("ODD" on pin 39 of SAA7151B, for example) to synchronize the digital encoder to the reference video signal, and also into the correct interlace sequence. Proper programming of HTRIG and VTRIG can adjust pipeline processing delay in decoder and/or frame buffer circuitry. If FS from the decoder is used as RCV1 input for the first "master" encoder, it can also be utilized as a horizontal reference signal. Then RCV2 is free to be used as gating input, fed by the RCM2 output, or it can be switched to output a CBN-like signal to one of the video signal sources.

Figure 4 shows a rather complex system, but the various timing techniques, as discussed above, can be applied in simpler systems, too.

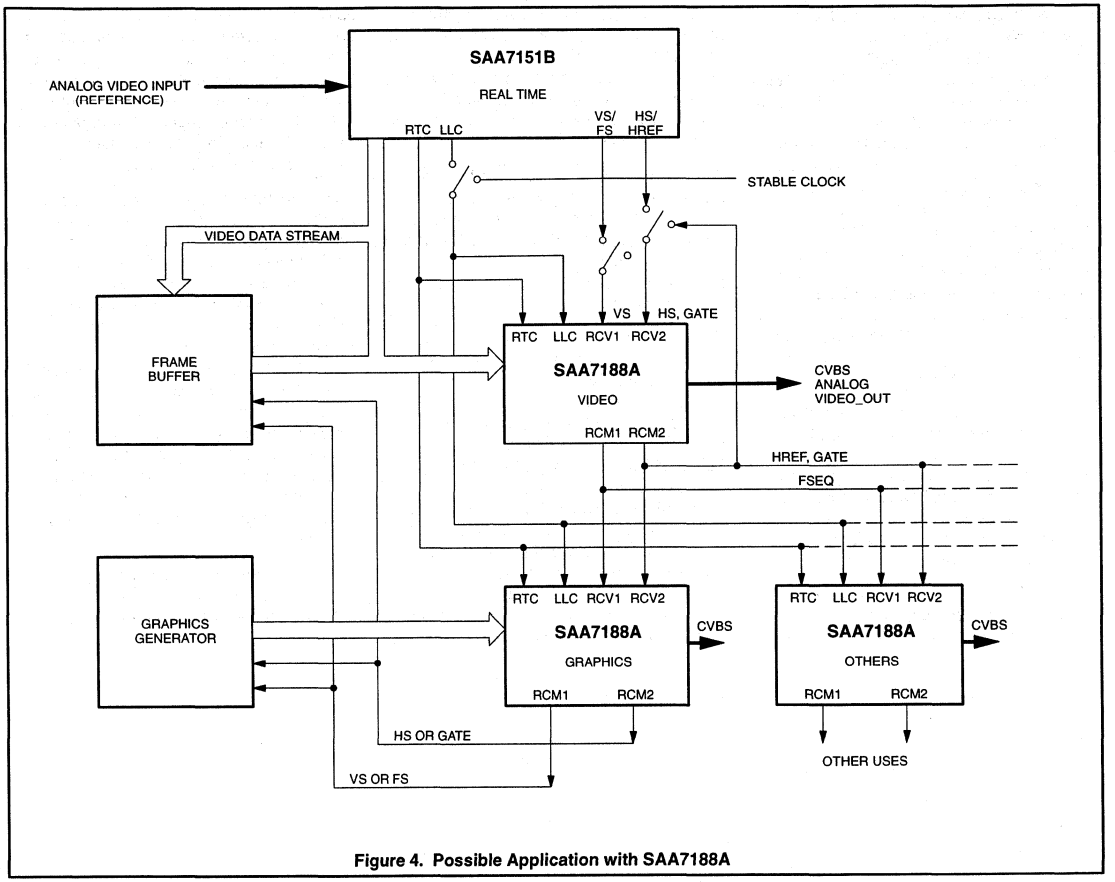


Figure 4. Possible Application with SAA7188A

7.0 APPENDIX: SOME PROGRAMMING TABLES

7.1 Synchronization Signals (6C, 6D, 70)

7.1.1 Subaddress 6C hex

Table 8. Program for RCV1 and RCV2 function at pin 6 and pin 7 in subaddress 6C-hex

BITS IN SUBADDRESS 6Chex								SHORT NAME	FUNCTION DESCRIPTION	DEFAULT AFTER RESET
7	6	5	4	3	2	1	0			
								PRCV2		
							0		RCV2 is active high, rising edge is timing reference	0
							1		RCV2 is active low, falling edge is timing reference	
								SRVC2	CBLF & ORCV2	
					0	0			RCV2 is input, has no input data gating function, but can be used for horizontal re-trigger, see TRCV2	00
					0	1			RCV2 is output, horizontal (timing) reference signal in all lines, begin and end freely programmable by BRCV and ERCV	
					1	0			RCV2 is input, and has input data gating function, can also be used for horizontal re-trigger, see TRCV2	
					1	1			RCV2 is output, can be used as external composite blanking signal, horizontal begin and end defined by BRCV and ERCV, vertial first active line defined by FAL, first inactive line defined by LAL (FAL – LAL, then all lines active).	
								PRCV1		
				0					RCV1 is active high, rising edge is timing reference	0
				1					RCV1 is active low, falling edge is timing reference	
								ORCV1		
			0						RCV1 is input	0
			1						RCV1 is input	
								TRCV2		
		0							Horizontal re-trigger by RCV1, RCV1 must be input	0
		1							Horizontal re-trigger by RCV2, RCV2 must be input	
								SRCV1		
0	0								VS (vertical sync), every field	00
0	1								FS (frame sync), odd_/even	
1	0								FSEQ color field sequence indication	
1	1								n.a.; don't use this combination	
0	0	0	0	0	0	0	0	00 hex	default after reset IC is prepared to accept an odd/_even signal at RCV1 (rising edge at begin of first field)	0000 0000

7.1.2 Subaddress 6D hex

Table 9. Program for RCM1 at pin 29 and "Line 21" encoding in subaddress 6D-hex

BITS IN SUBADDRESS 6Dhex								SHORT NAME	FUNCTION DESCRIPTION
7	6	5	4	3	2	1	0		
								CCEN	"Line 21" encoding, Closed Caption and Extented Data service
						0	0		no "line 21" encoding in either field
						0	1		"Line 21" encoding in first (odd) field only (extented data), data content as programmed in subaddress 69hex and 6Ahex
						1	0		"Line 21" encoding in second (even) field only (Closed Caption), data content as programmed in subaddress 67hex and 68hex
						1	1		"Line 21" encoding in both fields
								SRCM	select type of field reference output signal on pin 29 RCM1
				0	0				VS (vertical sync), active high during serration pulses (3 or 2.5 lines)
				0	1				FS (frame sync), active low during odd field, high during even field
				1	0				FSEQ color (field sequence indication signal), active high during first field of four fields, if FISE = 1 (60 Hz, 525 lines) first field of eight fields, if FISE = 0 (50 Hz, 625 lines)
				1	1				n.a.; do not use this combination
0	0	0	0						reserved

7.1.3 Subaddress 70 hex

Table 10. Program for VTRIG and VBI (vertical blanking interval) in subaddress 70-hex

BITS IN SUBADDRESS 70hex								SHORT NAME	FUNCTION DESCRIPTION
7	6	5	4	3	2	1	0		
								VTRIG	vertical trigger phase offset
			x	x	x	x	x		half line number, in which vertical/field trigger input occurs
								SBLBN	Vertical Blanking Interval (VBI)
		0							blanking is enforced in all lines outside FAL-to-LAL, (First Active Line to Last Active Line, see subaddress 7B, 7C, and 7D)
		1							blanking is only enforced only during equalization and serration (vertical sync) pulses, i.e., 9 (60Hz) or 7.5 (50Hz) lines, signal insertion a/o encoding also outside FAL-to-LAL, allowing data, time code or test signal insertion in regular VBI
								PHRES	color subcarrier reset mode, to support SC-H coupling
0	0								continuously running color subcarrier oscillation, e.g., for remote genlock RTC mode
0	1								color subcarrier phase reset every second line
1	0								color subcarrier phase reset every eighth field (PAL)
1	1								color subcarrier phase reset every fourth field (NTSC)

7.2 Video Standard Parameters (61, 70, 60)

7.2.1 Subaddress 60 hex

Table 11. Basic video standard parameters in subaddress 61-hex

BITS IN SUBADDRESS 61-hex								SHORT NAME	FUNCTION DESCRIPTION	DEFAULT AFTER RESET
7	6	5	4	3	2	1	0			
								FISE	field frequency mode select	
							0		50 Hz, 312.5 lines per field, 5 V-sync serration pulses etc, (start pre-equalization pulses 310 lines after field start) 864 (CCIR) pixels per line, i.e., 1778 LLC, 13.5 MHz 944 (SQP) pixels per line, i.e., 1888 LLC, 14.75 MHz FSEQ generates 4 field sequence	
							1		60 Hz, 262.5 lines per field, 6 V-sync serration pulses etc, (start pre-equalization pulses 259.5 lines after field start) 858 (CCIR) pixels per line, i.e., 1716 LLC, 13.5 MHz 780 (SQP) pixels per line, i.e., 1560 LLC, 12.27 MHz FSEQ generates 8 field sequence	1
								PAL	switch of subcarrier phase for V-component in alternative lines	
						0			no color subcarrier phase toggle switch, for NTSC encoding	0
						1			PAL-switch, i.e., subcarrier phase switch (±45° toggle) for V-color component in alternative lines, for PAL encoding	
								SCBW	chrominance bandwidth	
					0				extended chrominance bandwidth, e.g., option for S-video output	
					1				standard chrominance bandwidth	1
								RTCE	Real Time Control enable	
				0					no Real Time Control applied, standard subcarrier generation, relies on clock LLC stability	0
				1					Real Time Control of subcarrier frequency generation, RTC connection from appropriate Philips decoder needed	
								YGS	luminance gain select	
			0						luminance (black to white) is adjusted to 100 IRE	
			1						luminance (black to white) is adjusted to 92.5 IRE, giving room for 7.5 IRE setup, e.g., for NTSC	1
								INPI	PAL switch phase	
		0							nominal (standard) phase of PAL-switch	0
		1							opposite to standard, e.g., to adjust pipeline delay in RTC mode	
								DOWN	analog output (DACs)	
	0								DACs in normal operation, analog output of encoded video signal	0
	1								DACs are switched to lowest output voltage	
0									reserved	0
0	0	0	1	0	1	0	1	15 hex	default after reset	0001 0101

7.2.2 Subaddress 70 hex

Table 12. Program for subcarrier phase reset (SC-H) in subaddress 70-hex

BITS IN SUBADDRESS 70hex								SHORT NAME	FUNCTION DESCRIPTION
7	6	5	4	3	2	1	0		
								VTRIG	vertical trigger phase offset
			x	x	x	x	x		half line number, in which vertical/field trigger input occurs
								SBLBN	Vertical Blanking Interval (VBI)
		0							blanking is enforced in all lines outside FAL-to-LAL, (First Active Line to Last Active Line, see subaddress 7B, 7C, and 7D)
		1							blanking is only enforced only during equalization and serration (vertical sync) pulses, i.e., 9 (60Hz) or 7.5 (50Hz) lines, signal insertion a/o encoding also outside FAL-to-LAL, e.g., data, time code or test signal insertion in regular VBI
								PHRES	color subcarrier reset mode, to support SC-H coupling
0	0								continuously running color subcarrier oscillation, e.g., for remote genlock RTC mode
0	1								color subcarrier phase reset every second line
1	0								color subcarrier phase reset every eighth field (PAL)
1	1								color subcarrier phase reset every fourth field (NTSC)

7.2.3 Subaddress 60 hex

Table 13. Program for cross color reduction in analog CVBS-out under subaddress 60-hex

BITS IN SUBADDRESS 60hex								SHORT NAME	FUNCTION DESCRIPTION
7	6	5	4	3	2	1	0		
		0	0	0	0	0	0		reserved
								CCRS	Cross Color Reduction, reducing cross talk from luminance into chrominance as support for the testination receiver / decoder filter are active only from FAL-to-LAL, i.e., active video
0	0								standard CVBS, straight addition of luminance and chrominance signals
0	1								notch filter at 4.5 Mhz in luminance signal before adding chrominance, e.g., for PAL color subcarrier or NTSC sound carrier
1	0								notch filter at 3.3 Mhz in luminance signal before adding chrominance, wide and deep, e.g., for NTSC color subcarrier
1	1								notch filter at 3.3 Mhz in luminance signal before adding chrominance, more narrow than other one, e.g., for NTSC color subcarrier

7.3 Input Data Format and Signal Flow (3A, 6B)

7.3.1 Subaddress 3A hex, SAA7188A only

Table 14. Program for input data de-formating in subaddress 3A-hex

BITS IN SUBADDRESS 3A-hex								BIT NAME	FUNCTION DESCRIPTION	DEFAULT AFTER RESET
7	6	5	4	3	2	1	0			
								MUV2C	(M-port chroma two's complement)	
							0		Cb-Cr data at M-port is expected in two's complement	
							1		Cb-Cr data at M-port is expected in offset binary (acc. to CCIR 656)	1
								MY2C	(M-port luminance two's complement)	
						0			Y data at M-port is expected in two's complement around medium gray	
						1			Y data at M-port is expected in straight binary (acc. to CCIR 656)	1
								VUV2C	(V/D-port chroma two's complement)	
					0				Cb-Cr data at V/D-port is expected in two's complement (compare DTV-mode of SAA7151B)	0
					1				Cb-Cr data at V/D-port is expected in offset binary (CCIR-mode)	
								VY2C	(V-port luminance two's complement)	
				0					Y data at V-port is expected in two's complement around medium gray	0
				1					Y data at V-port is expected in straight binary (CCIR- and DTV-mode)	
								V656	data format at V-port and D-port	
			0						16 bit YUV interface formed by V-port = Y & D-port = UV	
			1						8-bit wide CCIR656 compatible data format at V-port	1
	0	0							reserved	00
								CBENB	internal color bar test signal switch	
0									normal encoding of input data	0
1									color bar test signal via encoding of LUT values	
0	0	0	1	0	0	1	1	13 hex	default after reset	0001 0011

7.3.2 Subaddress 6B hex, SAA7188A only

Table 15. Program for input data selection in subaddress 6B-hex

BITS IN SUBADDRESS 6B-hex								SEL_ED Pin 18	BIT NAME FUNCTION DESCRIPTION
7	6	5	4	3	2	1	0		
									MODIN defines data from which port gets encoded
0	0							–	data from M-port gets encoded
0	1							1	data from M-port gets encoded
0	1							0	data from V(/D)-port gets encoded
1	0							–	data from V(/D)-port gets encoded
1	1							1	data from V(/D)-port gets encoded
1	1							0	data from M-port gets encoded
		0	x	x	x	x	x		other function: line number for closed caption encoding

7.4 Input Data Formats (subaddress 3A), SAA7187 only

7.4.1 Subaddress 3A hex, SAA7187 only

Table 16. Program for input data de-formating in subaddress 3A-hex

BITS IN SUBADDRESS 3A-hex								BIT NAME	FUNCTION DESCRIPTION	DEFAULT AFTER RESET
7	6	5	4	3	2	1	0			
								FMT	Input Data Formats	
						0	0		YUV 4:4:4 on 24 pins, Y on VP1, V=Cr on VP2, U=Cb on VP3	00
						0	1		YUV 4:2:2 on 16 pins, Y on VP1, U=Cb and V=Cr multipexed on VP3	
						1	0		YUV 4:2:2 on 8 pins, on VP1, multipexed according to CCIR-656	
						1	1		reserved	
								VUVC	chroma two's complement	
					0				Cb-Cr input data is expected in two's complement	0
					1				Cb-Cr input data is expected in offset binary (CCIR-mode)	
								VY2C	luminance two's complement	
				0					Y data at V-port is expected in two's complement around medium gray	0
				1					Y data at V-port is expected in straight binary (CCIR- and DTV-mode)	
	0	0	0						reserved	000
								CBENB	internal color bar test signal switch	
0									normal encoding of input data	0
1									color bar test signal via encoding of LUT values	
0	0	0	0	0	0	0	0		00 hex default after reset	0000 0000

PHILIPS SEMICONDUCTORS ASSIGNED I²C-BUS ADDRESSES

Type number	Description	I²C slave address						
		A6	A5	A4	A3	A2	A1	A0
–	General call address	0	0	0	0	0	0	0
–	Reserved addresses	0	0	0	0	X	X	X
NE5751	Audio processor for RF communication	1	0	0	0	0	0	A
PCA1070	Programmable speech transmission IC	0	1	0	0	0	1	A
PCA8510	Stand-alone OSD circuit	1	0	1	1	1	0	1
PCA8516	Stand-alone OSD IC	1	0	1	1	1	0	1
PCA8581/C	128 × 8-bit EEPROM	1	0	1	0	A	A	A
PCB5020	Digital audio signal processor for car radio including ROM	0	0	1	1	0	A	A
PCB5021	Digital audio signal processor for car radio excluding ROM	0	0	1	1	0	A	A
PCD3311C	DTMF/modem/musical tone generator	0	1	0	0	1	0	A
PCD3312C	DTMF/modem/musical-tone generator	0	1	0	0	1	0	A
PCD4430	Programmable tone detector and DTMF generator	0	1	0	0	0	0	A
PCD4440	Analog voice scrambler/descrambler for mobile telephones	1	1	0	1	1	1	A
PCD5002	Pager decoder	0	1	0	0	1	1	1
PCF1810	8 × 8 cross-point matrix analog switch	0	0	1	1	1	A	A
PCF2116	LCD controller/driver	0	1	1	1	0	1	A
PCF8566	96-segment LCD driver 1:1 - 1:4 Mux rates	0	1	1	1	1	1	A
PCF8568	LCD row driver for dot matrix displays	0	1	1	1	1	0	A
PCF8569	LCD column driver for dot matrix displays	0	1	1	1	1	0	A
PCF8570/C	256 × 8-bit static RAM	1	0	1	0	A	A	A
PCF8573	Clock/calendar	1	1	0	1	0	A	A
PCF8574	8-bit remote I/O port (I²C-bus to parallel converter)	0	1	0	0	A	A	A
PCF8574A	8-bit remote I/O port (I²C-bus to parallel converter)	0	1	1	1	A	A	A
PCF8576	16-segment LCD driver 1:1 - 1:4 Mux rates	0	1	1	1	0	0	A
PCF8577A	32/64-segment LCD display driver	0	1	1	1	0	1	1
PCF8577C	32/64-segment LCD display driver	0	1	1	1	0	1	0
PCF8578	Row/column LCD dot matrix driver/display	0	1	1	1	1	0	A
PCF8579	Row/column LCD dot matrix driver/display	0	1	1	1	1	0	A
PCF8582/A	256 × 8-bit CMOS EEPROM	1	0	1	0	A	A	A
PCF8583	256 × 8-bit RAM/clock/calendar	1	0	1	0	0	0	A
PCF8591	4-channel, 8-bit Mux ADC and one DAC	1	0	0	1	A	A	A
PCF8593	Low-power clock calender	1	0	1	0	0	0	1

Type number	Description	I²C slave address						
		A6	A5	A4	A3	A2	A1	A0
PCX8594X-2	512 × 8-bit CMOS EEPROM	1	0	1	0	A	A	P
PCX8598X-2	1024 × 8-bit CMOS EEPROM	1	0	1	0	A	P	P
SAA1064	4-digit LED driver	0	1	1	1	0	A	A
SAA1136	PCM audio interface	0	0	1	1	1	0	0
SAA1137	PCM audio processor	0	1	0	0	0	0	A
SAA1300	Tuner switch circuit	0	1	0	0	0	A	A
SAA1770	D2MAC decoder for satellite and cable TV	0	0	1	1	1	1	A
SAA2502	MPEG audio source decoder	0	0	1	1	1	0	1
SAA2510	Video-CD MPEG-audio/video decoder	0	0	1	1	0	1	A
SAA4700	VPS dataline processor	0	0	1	0	0	0	A
SAA5240A	625-line teletext decoder; english/german/swedish	0	0	1	0	0	0	1
SAA5240B	625-line teletext decoder; french/italian/german	0	0	1	0	0	0	1
SAA5240P/D	625-line teletext decoder; spanish	0	0	1	0	0	0	1
SAA5240P/C	625-line teletext decoder; arabic	0	0	1	0	0	1	0
SAA5240P/F	625-line teletext decoder; hebrew	0	0	1	0	0	0	1
SAA5241A	625-line teletext decoder; english/german/swedish	0	0	1	0	0	0	1
SAA5241B	625-line teletext decoder; french/italian/german	0	0	1	0	0	0	1
SAA5243P/K	Computer controlled teletext circuit	0	0	1	0	0	0	1
SAA5243P/L	Computer controlled teletext circuit	0	0	1	0	0	0	1
SAA5243P/H	Computer controlled teletext circuit	0	0	1	0	0	0	1
SAA5243P/E	Computer controlled teletext circuit	0	0	1	0	0	0	1
SAA5244	Integrated VIP and teletext	0	0	1	0	0	0	1
SAA5245	525-line teletext decoder/controller	0	0	1	0	0	0	1
SAA5246	Integrated VIP and teletext	0	0	1	0	0	0	1
SAA5252	Line 21 decoder	0	0	1	0	1	0	0
SAA7110	Digital multistandard decoder	1	0	0	1	1	1	A
SAA7140	High performance video scaler	0	1	1	1	0	0	A
SAA7151B	8-bit digital multistandard TV decoder	1	0	0	0	1	A	1
SAA7152	Digital comb filter	1	0	1	1	0	0	1
SAA7165	Video enhancement D/A processor	1	0	1	1	1	1	1
SAA7186	Digital video scaler	1	0	1	1	1	A	0
SAA7191	Digital multistandard TV decoder	1	0	0	0	1	A	1
SAA7192A	Digital colour space-converter	1	1	1	0	0	0	A

Type number	Description	I²C slave address						
		A6	A5	A4	A3	A2	A1	A0
SAA7194	Digital video decoder/scaler	0	1	0	0	0	0	A
SAA7199B	Digital multistandard encoder	1	0	1	1	0	0	A
SAA7250	General purpose digital audio signal processor	0	0	1	1	0	0	A
SAA7370	CD-decoder plus digital servo processor	0	0	1	1	0	0	A
SAA9020	Field memory controller	0	0	1	0	1	A	A
SAA9041	Digital video text - backend	0	0	1	0	0	0	1
SAA9051	Digital multistandard colour TV decoder	1	0	0	0	1	A	1
SAA9053	Digital NTSC TV decoder	1	0	0	0	1	A	1
SAA9056	Digital SECAM colour decoder	1	0	0	0	1	A	1
SAA9060	Black and white PIP	1	0	0	0	1	1	0
SAA9065	Video enhancement and D/A processor	1	0	1	1	1	1	1
SAB3028	Remote control RC-5 transcoder	0	1	0	0	1	1	0
SAB3035	Digital tuning circuit for computer-controlled TV	1	1	0	0	0	A	A
SAB3036	Digital tuning circuit for computer-controlled TV	1	1	0	0	0	A	A
SAB3037	Digital tuning circuit for computer-controlled TV	1	1	0	0	0	A	A
SAB9070	PIP8 controller	0	0	1	0	0	1	0
SAF1134P	Dataline 16 decoder for VPS (gate array)	0	0	1	0	0	A	A
SAF1135P	Dataline 16 decoder for VPS (cell array)	0	0	1	0	0	A	A
TDA1551B	2 × 22 W BTL audio power amplifier	1	1	0	1	1	0	1
TDA1551Q	2 × 22 W BTL audio power amplifier	1	1	0	1	1	0	0
TDA4670	Picture signal improvement (PSI) circuit	1	0	0	0	1	0	0
TDA4670	Picture signal improvement (PSI) circuit	1	0	0	0	1	0	0
TDA4671	Picture signal improvement (PSI) circuit	1	0	0	0	1	0	0
TDA4672	Picture signal improvement (PSI) circuit	1	0	0	0	1	0	0
TDA4680	Video processor	1	0	0	0	1	0	0
TDA4685	Video processor	1	0	0	0	1	0	0
TDA4687	Video processor	1	0	0	0	1	0	0
TDA4688	Video processor	1	0	0	0	1	0	0
TDA4780	Video control with gamma control	1	0	0	0	1	0	0
TDA6360	Five-band equalizer for car radio	1	0	0	0	0	1	A
TDA8045	QAM-64 demodulator	0	0	0	1	1	A	A
TDA8363	Single chip NTSC decoder	1	0	0	0	1	0	0
TDA8366	One-chip multistandard video	1	0	0	0	1	0	1

Type number	Description	I²C slave address						
		A6	A5	A4	A3	A2	A1	A0
TDA8370	High/medium perf. sync. processor	1	0	0	0	1	1	0
TDA8376	One-chip multistandard video	1	0	0	0	1	0	1
TDA8405	Stereo/dual language decoder	1	0	0	0	0	1	0
TDA8415	TV/VCR stereo/dual sound processor	1	0	0	0	0	1	0
TDA8416	TV/VCR stereo/dual sound processor	1	0	1	1	0	1	0
TDA8417	TV/VCR stereo/dual sound processor	1	0	0	0	0	1	0
TDA8420	Audio processor with loudspeaker and headphone channel	1	0	0	0	0	0	A
TDA8421	Audio processor with loudspeaker and headphone channel	1	0	0	0	0	0	A
TDA8424	Audio processor with loudspeaker channel	1	0	0	0	0	0	1
TDA8425	Audio processor with loudspeaker channel	1	0	0	0	0	0	1
TDA8426	Hi-fi stereo audio processor	1	0	0	0	0	0	1
TDA8432	Sync. controller and deflection processor	1	0	0	0	1	1	A
TDA8433	TV deflection processor	1	0	0	0	1	1	A
TDA8440	Video/audio switch	1	0	0	1	A	A	A
TDA8442	Interface for colour decoder	1	0	0	0	1	0	0
TDA8443/A	YUV/RGB matrix switch	1	1	0	1	A	A	A
TDA8444	Octal 6-bit DAC	0	1	0	0	A	A	A
TDA8461	PAL/NTSC colour decoder with RGB processor	1	0	0	0	1	0	A
TDA8466	PAL/NTSC colour decoder with RGB processor	1	0	0	0	1	0	A
TDA8480	RGB gamma-correction processor	1	0	0	0	0	1	A
TDA8540	4 × 4 video switch matrix	1	0	0	1	A	A	A
TDA9140	Alignment-free multistandard decoder	1	0	0	0	1	A	1
TDA9141	Alignment-free multistandard decoder	1	0	0	0	1	A	1
TDA9145	Multistandard decoder	1	0	0	0	1	0	1
TDA9150	Deflection processor	1	0	0	0	1	1	0
TDA9160	Multistandard decoder/sync. processor	1	0	0	0	1	A	1
TDA9161	Bus-controlled decoder/sync. processor	1	0	0	0	1	0	1
TDA9162	Multistandard decoder/sync. processor	1	0	0	0	1	A	1
TDA9840/T	TV stereo/dual sound processor	1	0	0	0	0	1	0
TDA9860	Hi-fi audio processor	1	0	0	0	0	0	A
TEA6000	FM/IF and search tuning interface	1	1	0	0	0	0	1
TEA6100	FM/IF for computer-controlled radio	1	1	0	0	0	0	1
TEA6300	Sound fader control and preamplifier/source selector	1	0	0	0	0	0	0

Type number	Description	I²C slave address						
		A6	A5	A4	A3	A2	A1	A0
TEA6320	4-input tone/volume controller with fader control	1	0	0	0	0	0	0
TEA6330	Tone/volume controller	1	0	0	0	0	0	0
TEA6360	5-band equalizer	1	0	0	0	1	1	A
TSA5510	1.2 GHz PLL frequency synthesizer without AFC ADC	1	1	0	0	0	A	A
TSA5511	1.3 GHz PLL frequency synthesizer for TV	1	1	0	0	0	A	A
TSA5512	1.3 GHz PLL frequency synthesizer for TV	1	1	0	0	0	A	A
TSA5514	1.3 GHz PLL frequency synthesizer for TV	1	1	0	0	0	A	A
TSA5519	1.3 GHz PLL frequency synthesizer ADC	1	1	0	0	0	A	A
TSA6057	Radio tuning PLL frequency synthesizer	1	1	0	0	0	1	A
TSA6060	Radio tuning PLL frequency synthesizer	1	1	0	0	0	1	A
TSA6061	150 MHz PLL and IF-counter	1	1	0	0	0	1	A
UMA1000T	Data processor for mobile telephones	1	1	0	1	1	A	A
UMA1009	Frequency synthesizer for mobile telephones	1	1	0	0	0	A	A
UMA1010	Frequency synthesizer for mobile telephones	1	1	0	0	0	A	A
UMA1014T	Frequency synthesizer for mobile telephones	1	1	0	0	0	1	A
–	Reserved addresses	1	1	1	1	X	X	X

X = Don't care
A = Programmable address bit
P = Page selection bit

PHILIPS SEMICONDUCTORS I²C-BUS ADDRESS ALLOCATION TABLE

GROUP 0 (000)				
0	0	0	–	General call address
X	X	X	–	Reserved addresses
GROUP 1 (0001)				
1	A1	A0	TDA8045	QAM-64 demodulator
GROUP 2 (0010)				
0	0	A0	SAA4700	VPS dataline processor
0	0	1	SAA5240A	625-line teletext decoder; english/german/swedish
0	0	1	SAA5240B	625-line teletext decoder; french/italian/german
0	0	1	SAA5240P/F	625-line teletext decoder; hebrew
0	0	1	SAA5240P/D	625-line teletext decoder; spanish
0	0	1	SAA5241A	625-line teletext decoder; english/german/swedish
0	0	1	SAA5241B	625-line teletext decoder; french/italian/german
0	0	1	SAA5243P/H	Computer controlled teletext circuit
0	0	1	SAA5243P/K	Computer controlled teletext circuit
0	0	1	SAA5243P/L	Computer controlled teletext circuit
0	0	1	SAA5243P/E	Computer controlled teletext circuit
0	0	1	SAA5244	Integrated VIP and teletext
0	0	1	SAA5245	525-line teletext decoder/controller
0	0	1	SAA5246	Integrated VIP and teletext
0	0	1	SAA9041	Digital video text - backend
0	1	0	SAA5240P/C	625-line teletext decoder; arabic
0	1	0	SAB9070	PIP8 controller
0	A1	A0	SAF1134P	Dataline 16 decoder for VPS (gate array)
0	A1	A0	SAF1135P	Dataline 16 decoder for VPS (cell array)
1	0	0	SAA5252	Line 21 decoder
1	A1	A0	SAA9020	Field memory controller
GROUP 3 (0011)				
0	0	A0	SAA7250	General purpose digital audio signal processor
0	0	A0	SAA7370	CD-decoder plus digital servo processor
0	A1	A0	PCB5020	Digital audio signal processor for car radio incl. ROM
0	A1	A0	PCB5021	Digital audio signal processor for car radio excl. ROM
0	1	A0	SAA2510	Video-CD MPEG-audio/video decoder
1	0	0	SAA1136	PCM audio interface

GROUP 3 (0011)				
1	0	1	SAA2502	MPEG audio source decoder
1	A1	A0	PCF1810	8 × 8 cross-point matrix analog switch
1	1	A0	SAA1770	D2MAC decoder for satellite and cable TV
GROUP 4 (0100)				
0	0	A0	PCD4430	Programmable tone detector and DTMF generator
0	0	A0	SAA1137	PCM audio processor
0	0	A0	SAA7194	Digital video decoder/scaler
0	1	A0	PCA1070	Programmable speech transmission IC
0	A1	A0	SAA1300	Tuner switch circuit
1	0	A0	PCD3311C	DTMF/modem/musical tone generator
1	0	A0	PCD3312C	DTMF/modem/musical-tone generator
1	1	0	SAB3028	Remote control RC-5 transcoder
1	1	1	PCD5002	Pager decoder
A2	A1	A0	PCF8574	8-bit remote I/O port (I²C-bus to parallel converter)
A2	A1	A0	TDA8444	Octal 6-bit DAC
GROUP 7 (0111)				
0	0	A0	PCF8576	16-segment LCD driver 1:1 - 1:4 Mux rates
0	0	A0	SAA7140	High performance video scaler
0	1	A0	PCF2116	LCD controller/driver
0	1	0	PCF8577C	32/64-segment LCD display driver
0	A1	A0	SAA1064	4-digit LED driver
0	1	1	PCF8577A	32/64-segment LCD display driver
1	0	A0	PCF8568	LCD row driver for dot matrix displays
1	0	A0	PCF8569	LCD column driver for dot matrix displays
1	0	A0	PCF8578	Row/column LCD dot matrix driver/display
1	0	A0	PCF8579	Row/column LCD dot matrix driver/display
1	1	A0	PCF8566	96-segment LCD driver 1:1 - 1:4 Mux rates
A2	A1	A0	PCF8574A	8-bit remote I/O port (I²C-bus to parallel converter)
GROUP 8 (1000)				
0	0	A0	NE5751	Audio processor for RF communication
0	0	A0	TDA8420	Audio processor with loudspeaker and headphone channel
0	0	A0	TDA8421	Audio processor with loudspeaker and headphone channel
0	0	A0	TDA9860	Hi-fi audio processor
0	0	0	TEA6300	Sound fader control and preamplifier/source selector

GROUP 8 (1000)				
0	0	0	TEA6320	4-input tone/volume controller with fader control
0	0	0	TEA6330	Tone/volume controller
0	0	1	TDA8424	Audio processor with loudspeaker channel
0	0	1	TDA8425	Audio processor with loudspeaker channel
0	0	1	TDA8426	Hi-fi stereo audio processor
0	1	A0	TDA6360	Five-band equalizer for car radio
0	1	0	TDA8405	Stereo/dual language decoder
0	1	0	TDA8415	TV/VCR stereo/dual sound processor
0	1	0	TDA8417	TV/VCR stereo/dual sound processor
0	1	A0	TDA8480	RGB gamma-correction processor
0	1	0	TDA9840/T	TV stereo/dual sound processor
1	0	0	TDA4670	Picture signal improvement (PSI) circuit
1	0	0	TDA4670	Picture signal improvement circuit
1	0	0	TDA4671	Picture signal improvement circuit
1	0	0	TDA4672	Picture signal improvement (PSI) circuit
1	0	0	TDA4680	Video processor
1	0	0	TDA4685	Video processor
1	0	0	TDA4687	Video processor
1	0	0	TDA4688	Video processor
1	0	0	TDA4780	Video control with gamma control
1	0	0	TDA8363	Single chip NTSC decoder
1	0	0	TDA8442	Interface for colour decoder
1	0	A0	TDA8461	PAL/NTSC colour decoder with RGB processor
1	0	A0	TDA8466	PAL/NTSC colour decoder with RGB processor
1	0	1	TDA8366	One-chip multistandard video
1	0	1	TDA8376	One-chip multistandard video
1	0	1	TDA9145	Multistandard decoder
1	0	1	TDA9161	Bus-controlled decoder/sync. processor
1	1	0	SAA9060	Black and white PIP
1	1	0	TDA8370	High/medium perf. sync. processor
1	1	A0	TDA8432	Sync. controller and deflection processor
1	1	A0	TDA8433	TV deflection processor
1	1	0	TDA9150	Deflection processor
1	1	A0	TEA6360	5-band equalizer

GROUP 8 (1000)				
1	A1	1	SAA7151B	8-bit digital multistandard TV decoder
1	A1	1	SAA7191	Digital multistandard TV decoder
1	A1	1	SAA9051	Digital multistandard colour TV decoder
1	A1	1	SAA9053	Digital NTSC TV decoder
1	A1	1	SAA9056	Digital SECAM colour decoder
1	A1	1	TDA9140	Alignment-free multistandard decoder
1	A1	1	TDA9141	Alignment-free multistandard decoder
1	A1	1	TDA9160	Multistandard decoder/sync. processor
1	A1	1	TDA9162	Multistandard decoder/sync. processor
GROUP 9 (1001)				
1	1	A0	SAA7110	Digital multistandard decoder
A2	A1	A0	PCF8591	4-channel, 8-bit Mux ADC and one DAC
A2	A1	A0	TDA8440	Video/audio switch
A2	A1	A0	TDA8540	4 × 4 video switch matrix
GROUP A (1010)				
0	0	A0	PCF8583	256 × 8-bit RAM/clock/calendar
0	0	1	PCF8593	Low power clock calender
A2	P	P	PCX8598X-2	1024 × 8-bit CMOS EEPROM
A2	A1	A0	PCF8570/C	256 × 8-bit static RAM
A2	A1	A0	PCA8581/C	128 × 8-bit EEPROM
A2	A1	A0	PCF8582/A	256 × 8-bit CMOS EEPROM
A2	A1	P	PCX8594X-2	512 × 8-bit CMOS EEPROM
GROUP B (1011)				
0	0	A0	SAA7199B	Digital multistandard encoder
0	0	1	SAA7152	Digital comb filter
0	1	0	TDA8416	TV/VCR stereo/dual sound processor
1	0	1	PCA8510	Stand-alone OSD circuit
1	0	1	PCA8516	Stand-alone OSD IC
1	A1	0	SAA7186	Digital video scaler
1	1	1	SAA7165	Video enhancement D/A processor
1	1	1	SAA9065	Video enhancement and D/A processor

GROUP C (1100)				
0	0	1	TEA6000	FM/IF and search tuning interface
0	0	1	TEA6100	FM/IF for computer-controlled radio
0	A1	A0	SAB3035	Digital tuning circuit for computer-controlled TV
0	A1	A0	SAB3036	Digital tuning circuit for computer-controlled TV
0	A1	A0	SAB3037	Digital tuning circuit for computer-controlled TV
0	A1	A0	TSA5510	1.2 GHz PLL frequency synthesizer without AFC ADC
0	A1	A0	TSA5511	1.3 GHz PLL frequency synthesizer for TV
0	A1	A0	TSA5512	1.3 GHz PLL frequency synthesizer for TV
0	A1	A0	TSA5514	1.3 GHz PLL frequency synthesizer for TV
0	A1	A0	TSA5519	1.3 GHz PLL frequency synthesizer ADC
0	1	A0	TSA6057	Radio tuning PLL frequency synthesizer
0	1	A0	TSA6060	Radio tuning PLL frequency synthesizer
0	1	A0	TSA6061	150 MHz PLL and IF-counter
0	A1	A0	UMA1009	Frequency synthesizer for mobile telephones
0	A1	A0	UMA1010	Frequency synthesizer for mobile telephones
0	1	A0	UMA1014T	Frequency synthesizer for mobile telephones
GROUP D (1101)				
0	A1	A0	PCF8573	Clock/calendar
1	0	0	TDA1551Q	2 × 22 W BTL audio power amplifier
1	0	1	TDA1551B	2 × 22 W BTL audio power amplifier
1	1	A0	PCD4440	Analog voice scrambler/descrambler for mobile telephones
1	A1	A0	UMA1000T	Data processor for mobile telephones
A2	A1	A0	TDA8443/A	YUV/RGB matrix switch
GROUP E (1110)				
0	0	A0	SAA7192A	Digital colour space-converter
GROUP F (1111)				
X	X	X	–	Reserved addresses

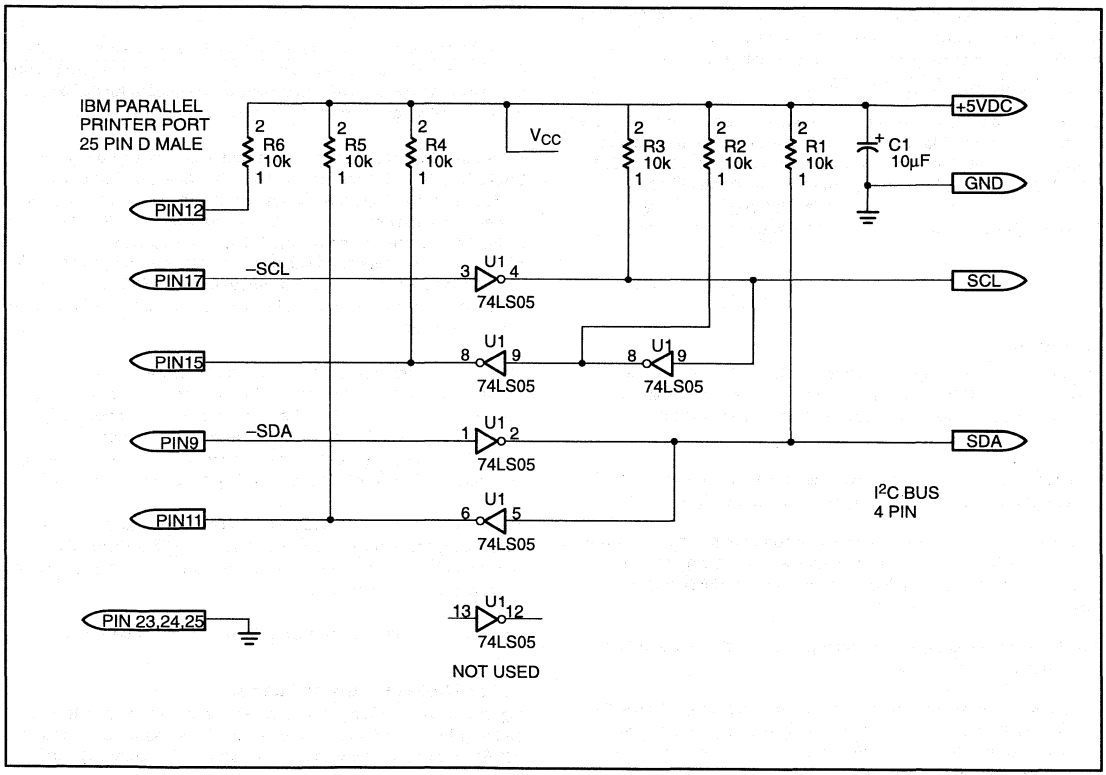
The Group number represents the hexadecimal equivalent of the four most significant bits (A6-A3) of the salve address.

X = Don't care
A = Programmable address bit
P = Page selection bit

I²C parallel printer port adaptor

The schematic below shows how Philips I²C software programs are able to communicate through any IBM-compatible PC parallel printer port using I²C serial protocol. The software toggles the SDA and SCL lines in a manner compatible with all I²C integrated circuits and I²C evaluation boards such as DTV7191 and DTV9051. Some variations of the four-wire I²C bus pinning have changed the order of the clock, data power and ground. Check the pinning required for each evaluation board connected using this type of interface. Power for the interface board must come from the application, not the PC printer port.

I²C PARALLEL PRINTER PORT ADAPTOR



Interfacing the PCF8584 I²C-bus controller to 80C51 family microcontrollers

AN425

DESCRIPTION

This application note shows how to use the PCF8584 I²C-bus controller with 80C51 family microcontrollers. One typical way of connecting the PCF8584 to an 80C31 is shown. Some basic software routines are described showing how to transmit and receive bytes in a single master system. An example is given of how to use these routines in an application that makes use of the I²C circuits on an I²C demonstration board.

The PCF8584 is used to interface between parallel microprocessor or microcontroller buses and the serial I²C bus. For a description of the I²C bus protocol refer to the I²C bus specification which is printed in the microcontroller user guide.

The PCF8584 controls the transmission and reception of data on the I²C bus, arbitration, clock speeds and transmission and reception of data on the parallel bus. The parallel bus is compatible with 80C51, 68000, 8085 and Z80 buses. Communication with the I²C-bus can be done on an interrupt or polled basis. This application note focuses on interfacing with 8051 microcontrollers in single master systems.

PCF8584

In Figure 1, a block diagram is shown of the PCF8584. Basically it consists of an I²C-interface similar to the one used in 84Cxx family microcontrollers, and a control block for interfacing to the microcontroller.

The control block can automatically determine whether the control signals are from 80xx or 68xxx type of microcontrollers.

This is determined after the first write action from the microcontroller to the PCF8584. The control block also contains a programmable divider which allows the selection of different PCF8584 and I²C clocks.

The I²C interface contains several registers which can be written and read by the microcontroller.

S1 is the control/status register. This register is accessed while the A0 input is 1. The meaning of the bits depends on whether the register is written to or read from. When used as a single master system the following bits are important:

PIN: Interrupt bit. This bit is made active when a byte is sent/received to/from the I²C-bus. When ENI is made active, PIN also controls the external INT line to interrupt the microcontroller.

ES0-ES2: These bits are used as pointer for addressing S0, S0', S2 and S3. Setting ES0 also enables the Serial I/O.

ENI: Enable Interrupt bit. Setting this bit enables the generation of interrupts on the INT line.

STA, STO: These bits allow the generation of START or STOP conditions.

ACK: With this bit set and the PCF8584 is in master/receiver mode, no acknowledge is generated by the PCF8584. The slave/transmitter now knows that no more data must be sent to the I²C-bus.

BER: This bit may be read to check if bus errors have occurred.

BB: This bit may be read to check whether the bus is free for I²C-bus transmission.

S2 is the clock register. It is addressed when A0 = 0 and ES0-ES2 = 010 in the previous write cycle to S1. With the bits S24-S20 it is possible to select 5 input clock frequencies and 4 I²C clock frequencies.

S3 is the interrupt vector register. It is addressed when A0 = 0 and ES0-ES2 = 001 in the previous write cycle to S1. This register is not used when an 80C51 family microcontroller is used. An 80C51 microcontroller has fixed interrupt vector addresses.

S0' is the own address register. It is addressed when A0 = 0 and ES0-ES2 = 000. This register contains the slave address of the PCF8584. In the single master system described here, this register has no functional use. However, by writing a value to S0', the PCF8584 determines whether an 80Cxx or 68xxx type microcontroller is the controlling microcontroller by looking at the $\overline{CS}$ and $\overline{WR}$ lines. So independent of whether the PCF8584 is used as master or slave, the microcontroller should always first write a value to S0' after reset.

S0 is the I²C data register. It is addressed when A0 = 0 and ES0-ES2 = 1x0. Transmission of a byte on the I²C bus is done by writing this byte to S0. When the transmission is finished, the PIN bit in S1 is reset and if ENI is set, an interrupt will be generated. Reception of a byte is signaled by resetting PIN and by generating an interrupt if ENI is set. The received byte can be read from S0.

The SDA and SCL lines have no protection diodes to V_{DD}. This is important for multimaster systems. A system with a PCF8584 can now be switched off without causing the I²C-bus to hang-up. Other masters still can use the bus.

For more information of the PCF8584 refer to the data sheet.

PCF8584/8031 Hardware Interface

Figure 2 shows a minimum system with an 8051 family controller and a PCF8584. In this example, an 80C31 is used. However any 80C51 family controller with external addressing capability can be used.

The software resides in EPROM U3. For addressing this device, latch U2 is necessary to demultiplex the lower address bits from the data bits. The PCF8584 is mapped in the external data memory area. It is selected when A1 = 0. Because in this example no external RAM or other mapped peripherals are used, no extra address decoding components are necessary. A0 is used by the PCF8584 for proper register selection in the PCF8584.

U5A is an inverter with Schmitt trigger input and is used to buffer the oscillator signal of the microcontroller. Without buffering, the rise and fall time specifications of the CLK signal are not met. It is also important that the CLK signal has a duty cycle of 50%. If this is not possible with certain resonators or microcontrollers, then an extra flip-flop may me necessary to obtain the correct duty cycle.

U5C and U5D are used to generate the proper reset signals for the microcontroller and the PCF8584.

Interfacing the PCF8584 I²C-bus controller to 80C51 family microcontrollers

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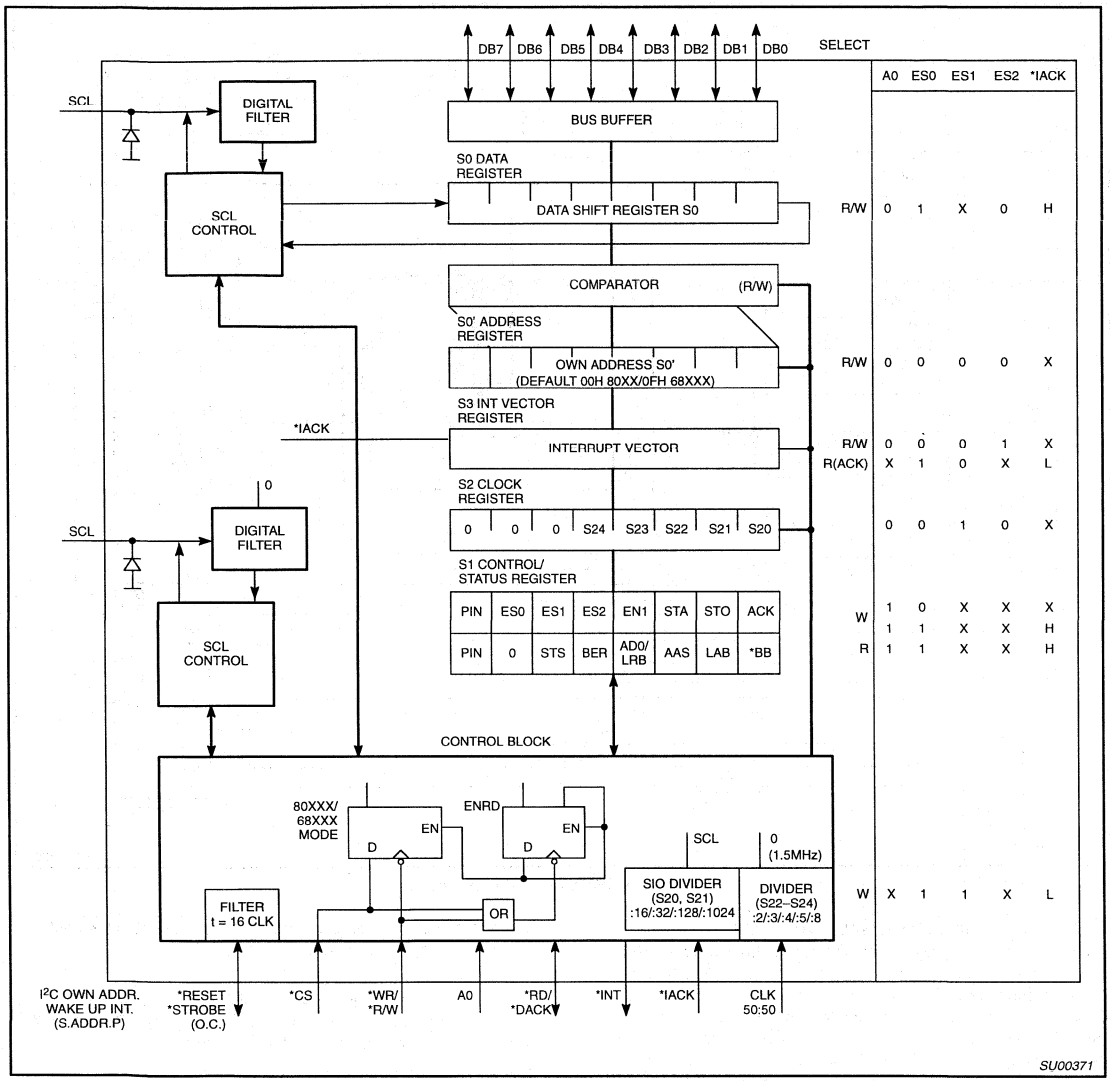

Figure 1. PCF8584 Block Diagram

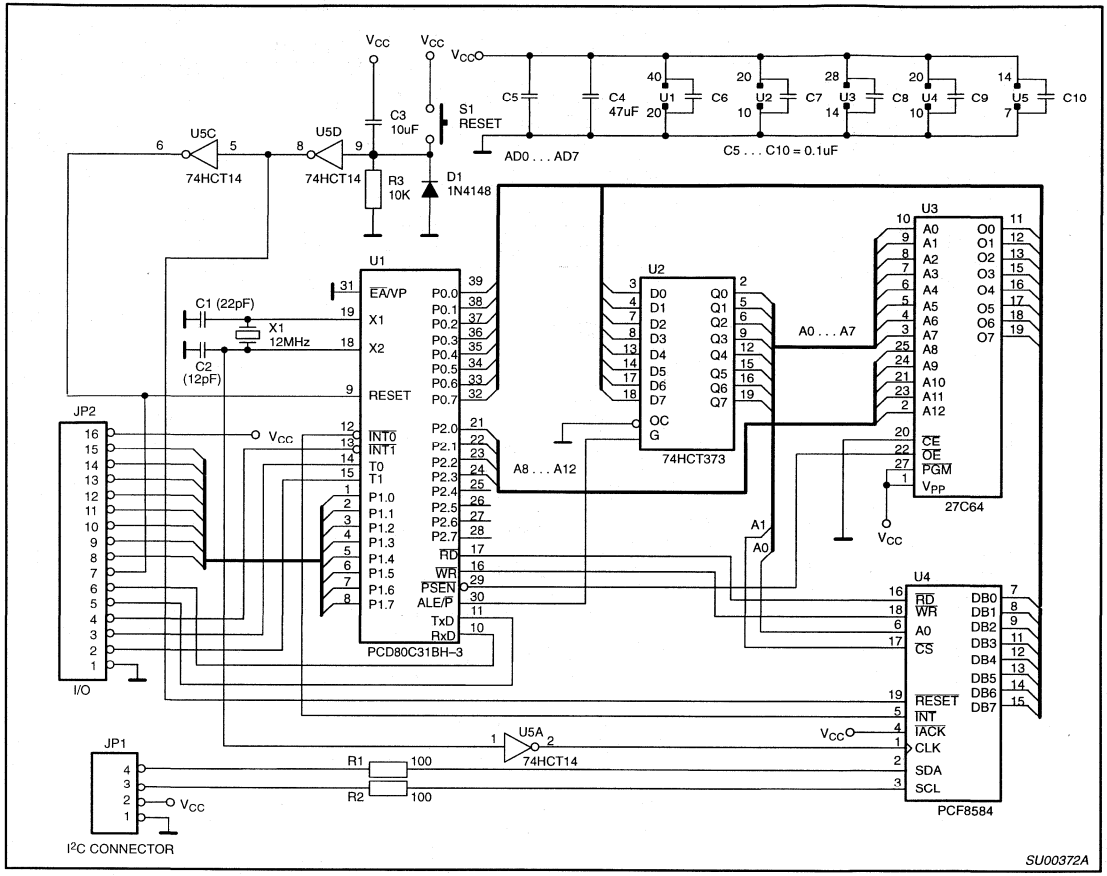

Figure 2. PCF8584 to 80C31 Interface

Basic PCF8584/8031 Driver Routines

In the listing section (page 6), some basic routines are shown. The routines are divided in two modules. The module ROUTINE contains the driver routines and initialization of the PCF8584. The module INTERR contains the interrupt handler. These modules may be linked to a module with the user program that uses the routines in INTERR and ROUTINE. In this application note, this module will be called USER. A description of ROUTINE and INTERR follows.

Module ROUTINE

Routine Sendbyte (Lines 17-20)—
This routine sends the contents of the accumulator to the PCF8584. The address is such that A0 = 0. Which register is accessed depends on the contents of ES0-ES2 of the control register. The address of the PCF8584 is in variable 'PCF8584'. This must have been previously defined in the user program. The DPTR is used as a pointer for addressing the peripheral. If the address is less than 255, then R0 or R1 may be used as the address pointer.

Routine Sendcontr (Lines 25, 26)—
This routine is similar to Sendbyte, except that now A0 = 1. This means that the contents of the accumulator are sent to the control register S1 in the PCF8584.

Routine Readbyte (Lines 30-33)—
This routine reads a register in the PCF8584 with A0 = 0. Which register depends on ES0-ES2 of the control register. The result of the read operation is returned in the accumulator.

Routine Readcontr (Lines 37-39)—
This routine is similar to Readbyte, except that now A0 = 1. This means that the accumulator will contain the value of status register S1 of the PCF8584.

Routine Start Lines (44-56)—
This routine generates a START-condition and the slave address with a R/W bit. In line 44, the variable IIC_CNT is reset. This variable is used as a byte counter to keep track of the number of bytes that are received or transmitted. IIC_CNT is defined in module INTERR.

Lines 45-46 increment the variable NR_BYTES if the PCF8584 must receive data. NR_BYTES is a variable that indicates how many bytes have to be received or transmitted. It must be given the correct value in the USER module. Receiving or transmitting is

distinguished by the value of the DIR bit. This must also be given the correct value in the USER module.

Then the status register of PCF8584 must be read to check if the I²C bus is free. First the status register must be addressed by giving ES0-ES2 of the control register the correct value (lines 47-48). Then the Bus Busy bit is tested until the bus is free (lines 49-50). If this is the case, the slave address is sent to data register S0 and the I2C_END bit is cleared (lines 51-53). The slave address is set by the user program in variable USER. The LSB of the slave address is the R/W bit. I2C_END can be tested by the user program whether an I2C reception/transmission is in progress or not.

Next the START condition will be generated and interrupt generation enabled by setting the appropriate bits in control register S1 (lines 54-55).

Now the routine will return back to the user program and other tasks may be performed. When the START condition, slave address and R/W bit are sent, and the ACK is received, the PCF8584 will generate an interrupt. The interrupt routine will determine if more bytes have to be received or transmitted.

Routine Stop (Lines 59-62) —
Calling this routine, a STOP condition will be sent to the I²C bus. This is done by sending the correct value to control register S1 (lines 59-61). After this the I2C_END bit is set, to indicate to the user program that a complete I²C sequence has been received or transmitted.

Routine I2C_Init (Lines 65-76)—
This routine initializes the PCF8584. This must be done directly after reset. Lines 67-70 write data to 'own address' register S0'. First the correct address of S0' is set in control register S1 (lines 67-68), then the correct value is written to it (lines 69-70). The value for S0' is in variable SLAVE_ADR and set by the user program. As noted previously, register S0' must always be the first register to be accessed after reset, because the PCF8584 now determines whether an 80Cxxx or 68xxx microcontroller is connected. Lines 72-76 set the clock register S2. The variable I2C_CLOCK is also set by the user program.

Module INTERR
This module contains the I²C interrupt routine. This routine is called every time a byte is received or transmitted on the I²C bus. In lines 12-15 RAM space for variables is reserved.

BASE is the start address in the internal 80C51 RAM where the data is stored that is received, or where the data is stored that has to be transmitted.

NR_BYTES, IIC_CNT and SLAVE were explained earlier. I2C_END and DIR are flags that are used in the program. I2C_END indicates whether an I²C transmission or reception is in progress. DIR indicates whether the PCF8584 has to receive or transmit bytes. The interrupt routine makes use of register bank 1.

The transmission part of the routine starts at line 42. In lines 42-43, a check is made whether IIC_CNT = NR_BYTES. If true, all bytes are sent and a STOP condition may be generated (lines 44-45).

Next the pointer for the internal RAM is restored (line 46) and the byte to be transmitted is fetched from the internal RAM (line 47). Then this byte is sent to the PCF8584 and the variables are updated (lines 47-49). The interrupt routine is left and the user program may proceed. The receive part starts from line 55. First a check is made if the next byte to be received is the last byte (lines 56-59). If true the ACK must be disabled when the last byte is received. This is accomplished by resetting the ACK bit in the control register S1 (lines 60-61).

Next the received byte may be read (line 62) from data register S0. The byte will be temporary stored in R4 (line 63). Then a check is made if this interrupt was the first after a START condition. If so, the byte read has no meaning and the interrupt routine will be left (lines 68-70). However by reading the data register S0 the next read cycle is started.

If valid data is received, it will be stored in the internal RAM addressed by the value of BASE (lines 71-73). Finally a check is made if all bytes are received. If true, a STOP condition will be sent (lines 75-78).

EXAMPLES
In the listing section (starting on page 10), some examples are shown that make use of the routines described before. The examples are transmission of a sequence, reception of I²C data and an example that combines both.

The first example sends bytes to the PCD8577 LCD driver on the OM1016 demonstration board. Lines 7 to 10 define the interface with the other modules and should be included in every user program. Lines 14 to 16 define the segments in the user module. It is completely up to the user how to organize this.

Lines 24 and 28 are the reset and interrupt vectors. The actual user program starts at line 33. Here three variables are defined that are used in the I²C driver routines. Note that PCF8584 must be an even address, otherwise the wrong internal registers will be accessed! Lines 37-42 initialize the interrupt logic of the microcontroller. Next the PCF8584 will be initialized (line 45).

The PCF8584 is now ready to transmit data. A table is made in the routine at line 61. For the PCD8577, the data is a control byte and the segment data. Note that the table does not contain the slave address of the LCD driver. In lines 51-54, variables are made ready to start the transmission. This consists of defining the direction of the transmission (DIR), the address where the data table starts (BASE), the number of bytes to transmit (NR_BYTES, without slave address!) and the slave address (SLAVE) of the I²C peripheral that has to be accessed.

In line 55 the transmission is started. Once the I²C transmission is started, the user program can do other tasks because the transmission works on interrupts. In this example a loop is performed (line 58). The user can check the end of the transmission during the other tasks, by testing the I2C_END bit regularly.

The second example program receives 2 bytes from the PCF8574P I/O expander on the OM1016 demonstration board. Until line 45 the program is identical to the transmit routine because it consists of initialization and variable definition. From line 48, the variables are set for I²C reception. The received bytes are stored in RAM area from label TABLE. During reception, the user program can do other tasks. By testing the I2C_END bit the user can determine when to start processing the data in the TABLE.

The third example program displays time from the PCF8583P clock/calendar/RAM on the LCD display driven by the PCD8577. The LED display (driven by SAA1064) shows the value of the analog inputs of the A/D converter PCF8591. The four analog inputs are scanned consecutively.

In this example, both transmit and receive sequences are implemented as shown in the previous examples. The main clock part is from lines 62-128. This contains the calls to the I²C routines. From lines 135-160, routines are shown that prepare the data to be transmitted. Lines 171 to 232 are the main program for the AD converter and LED display. Lines 239 to 340 contain routines used by the main program. This demo program can also be used with the I²C peripherals on the OM1016 demonstration board.

```
ASM51  TSW  ASSEMBLER   Routines for PCF8584

LOC   OBJ          LINE  SOURCE

                      1  $TITLE (Routines for PCF8584)
                      2  $PAGELENGTH(40)
                      3  ;Program written for PCF8584 as master
                      4  ;
                      5          PUBLIC READBYTE,READCONTR,SENDBYTE
                                 PUBLIC SENDCONTR,START,STOP
                      6          PUBLIC I2C_INIT
                      7          EXTRN  BIT(I2C_END,DIR)
                      8          EXTRN  DATA(SLAVE,IIC_CNT,NR_BYTES)
                      9          EXTRN  NUMBER(SLAVE_ADR,I2C_CLOCK,PCF8584)
                     10  ;
                     11  ;Define code segment
                     12  ROUTINE   SEGMENT CODE
----                 13            RSEG    ROUTINE
                     14  ;
                     15  ;SENDBYTE sends a byte to PCF8584 with A0=0
                     16  ;Byte to be send must be in accu
0000:           R    17  SENDBYTE:
0000: 900000    R    18          MOV DPTR,#PCF8584 ;Register address
0003: F0             19  SEND:    MOVX @DPTR,A     ;Send byte
0004: 22             20          RET
                     21  ;
                     22  ;SENDCONTR sends a byte to PCF8584 with A0=1
                     23  ;Byte to be send must be in accu
0005:                24  SENDCONTR:
0005: 900001    R    25          MOV DPTR,#PCF8584+01H ;Register address
0008: 80F9           26          JMP SEND
                     27  ;
                     28  ;READBYTE reads a byte from PCF8584 with A0=0
                     29  ;Received byte is stored in accu
000A:                30  READBYTE:
000A: 900000    R    31          MOV DPTR,#PCF8584 ;Register address
000D: E0             32  REC:     MOVX A,@DPTR     ;Receive byte
000E: 22             33          RET
                     34  ;
                     35  ;READCONTR reads a byte from PCF8584 with A0=1
                     36  ;Received byte is stored in accu
000F:                37  READCONTR:
000F: 900001    R    38          MOV DPTR,#PCF8584+01H ;Register address
0012: 80F9           39          JMP REC
                     40  ;
                     41  ;START tests if the I2C bus is ready. If ready a
                     42  ;START-condition will be sent, interrupt generation
                     43  ;and acknowledge will be enabled.
0014: 750000    R    44  START:   MOV IIC_CNT,#00 ;Clear  I2C byte counter
0017: 200002    R    45          JB DIR,PROCEED  ;If DIR is 'receive' then
001A: 0500      R    46          INC NR_BYTES    ;increment NR_BYTES
001C: 7440           47  PROCEED:MOV A,#40H       ; Read STATUS register of
                                                  ; 8584
001E: 120005    R    48          CALL SENDCONTR
0021: 12000F    R    49  TESTBB: CALL READCONTR
0024: 30E0FA         50          JNB ACC.0,TESTBB; Test BB/ bit
0027: E500      R    51          MOV A,SLAVE
0029: C200      R    52          CLR I2C_END      ;Reset I2C ready bit
002B: 120000    R    53          CALL SENDBYTE    ;Send slave address
002E: 744D           54          MOV A,#01001101B;Generate START, set ENI,
                                                  ;set ACK
0030: 120005    R    55          CALL SENDCONTR
0033: 22             56          RET
                     57  ;
                     58  ;STOP will generate a STOP condition and set the
                         ;I2C_END bit
0034: 74C3           59  STOP:    MOV A,#11000011B
```

```
0036: 120005    R     60          CALL SENDCONTR  ;Send STOP condition
0039: D200      R     61          SETB I2C_END    ;Set I2C_END bit
003B: 22              62          RET
                      63  ;
                      64  ;I2C_init does the initialization of the PCF8584
003C:                 65  I2C_INIT:
                      66  ;Write own slave address
003C: E4              67          CLR A
003D: 120005    R     68          CALL SENDCONTR  ;Write to control register
0040: 7400      R     69          MOV A,#SLAVE_ADR
0042: 120000    R     70          CALL SENDBYTE    ;Write to own slave
                                                   ;register
                      71  ;Write clock register
0045: 7420            72          MOV A,#20H
0047: 120005    R     73          CALL SENDCONTR  ;Write to control register
004A: 7400      R     74          MOV A,#I2C_CLOCK
004C: 120000    R     75          CALL SENDBYTE   ;Write to clock register
004F: 22              76          RET
                      77  ;
0050:                 78          END
```

```
ASM51  TSW  ASSEMBLER   I2C INTERRUPT ROUTINE

LOC   OBJ          LINE  SOURCE

                      1  $TITLE (I2C INTERRUPT ROUTINE)
                      2  $PAGELENGTH(40)
                      3  ;
                      4          PUBLIC INT0_SRV
                      5          PUBLIC DIR,I2C_END
                      6          PUBLIC BASE,NR_BYTES,IIC_CNT,SLAVE
                      7          EXTRN  CODE(SENDBYTE,SENDCONTR,STOP)
                                 EXTRN  CODE(READBYTE,READCONTR)
                      8  ;
                      9  ;Define variables in RAM
                     10  IIC_VAR SEGMENT DATA
----                 11          RSEG IIC_VAR
0000:           R    12  BASE:   DS 1             ;Pointer to I2C table (till
                                                  ;256)
0001:                13  NR_BYTES: DS 1           ;Number of bytes to rcv/trm
0002:                14  IIC_CNT:DS 1             ;I2C byte counter
0003:                15  SLAVE:  DS 1             ;Slave address after START
                     16  ;
                     17  ;Define variable segment
                     18  BIT_VAR SEGMENT DATA BITADDRESSABLE
----                 19          RSEG BIT_VAR
0000:           R    20  STATUS: DS 1             ;Byte with flags
0000            R    21  I2C_END BIT STATUS.0     ;Defines if a I2C
                                                  ;transmission is finished
                     22                           ;'1' is finished
                     23                           ;'0' is not ready
0000            R    24  DIR     BIT STATUS.3     ;Defines direction of I2C
                                                  ;transmission
                     25                           ;'1':Transmit    '0':Receive
                     26  ;
                     27  ;Define code segment for routine
                     28  IIC_INT SEGMENT CODE PAGE
----                 29          RSEG IIC_INT
                     30  ;
                     31  ;Program uses registers in RB1
                     32          USING 1
                     33  ;
0000:           R    34  INT0_SRV:
0000: C0E0           35          PUSH ACC         ;Save acc. en psw on stack
0002: C0D0           36          PUSH PSW
0004: 75D008         37          MOV PSW,#08H     ;Select register bank 1
0007: 300016    R    38          JNB DIR,RECEIVE ;Test direction bit
                     39                           ;8584 is MST/TRM
                     40
                     41  ;Program part to transmit bytes to IIC bus
000A: E502      R    42          MOV A,IIC_CNT    ;Compare IIC_CNT and
                                                  ;NR_BYTES
000C: B50105    R    43          CJNE A,NR_BYTES,PROCEED
000F: 120000    R    44          CALL STOP        ;All bytes transmitted
0012: 8032           45          JMP EXIT
0014: A800      R    46  PROCEED:MOV R0,BASE      ;RAM pointer
0016: E6             47          MOV A,@R0        ;Source is internal RAM
0017: 0500      R    48          INC BASE         ;Update pointer of table
0019: 120000    R    49          CALL SENDBYTE    ;Send byte to IIC bus
001C: 0502      R    50          INC IIC_CNT      ;Update byte counter
001E: 8026           51          JMP EXIT
                     52  ;
                     53  ;
                     54  ;Program to receive byte from IIC bus
0020:                55  RECEIVE:
0020: E502      R    56          MOV A,IIC_CNT    ;Test if last byte is to be
                                                  ;received
0022: 04             57          INC A
```

```
0023: 04            58          INC A
0024: B50105   R    59          CJNE A,NR_BYTES,PROC_RD
0027: 7448          60          MOV A,#01001000B;Last byte to be received.
                                                ;Disable ACK
0029: 120000   R    61          CALL SENDCONTR  ;Write control word to
                                                ;PCF8584
002C: 120000   R    62  PROC_RD:CALL READBYTE   ;Read I2C byte
002F: FC            63          MOV R4,A        ;Save accu
                    64  ;If RECEIVE is entered after the transmission of
                    65  ;START+address then the result of READBYTE is not
                    66  ;relevant. READBYTE is used to start the generation
                        ;of the clock pulses for the next byte to read.
                    67  ;This situation occurs when IIC_CNT is 0
0030: E4            68          CLR A           ;Test IIC_CNT
0031: B50202   R    69          CJNE A,IIC_CNT,SAVE
0034: 8006          70          JMP END_TEST    ;START is send. No relevant
                                                ;data in data reg. of 8584
0036: A800     R    71  SAVE:   MOV R0,BASE
0038: EC            72          MOV A,R4        ;Destination is internal RAM
0039: F6            73          MOV @R0,A
003A: 0500     R    74          INC BASE
003C: 0502     R    75  END_TEST:INC IIC_CNT    ;Test if all bytes are
                                                ;received
003E: E501     R    76          MOV A,NR_BYTES
0040: B50203   R    77          CJNE A,IIC_CNT,EXIT
0043: 120000   R    78          CALL STOP       ;All bytes received
                    79  ;
0046: D0D0          80  EXIT:   POP PSW         ;Restore PSW and accu
0048: D0E0          81          POP ACC
004A: 32            82          RETI
                    83  ;
004B:               84          END
```

```
ASM51  TSW  ASSEMBLER   Send a string of bytes to the PCD8577 on OM1016

LOC   OBJ          LINE  SOURCE

                      1  $TITLE (Send a string of bytes to the PCD8577 on
                             OM1016)
                      2  $PAGELENGTH(40)
                      3  ;
                      4  ;This program is an example to transmit bytes via
                         ;PCF8584
                      5  ;to the I2C-bus
                      6  ;
                      7          PUBLIC  SLAVE_ADR,I2C_CLOCK,PCF8584
                      8          EXTRN   CODE(I2C_INIT,INT0_SRV,START)
                      9          EXTRN   BIT(I2C_END,DIR)
                     10          EXTRN   DATA(BASE,NR_BYTES,IIC_CNT,SLAVE)
                     11  ;
                     12  ;
                     13  ;Define used segments
                     14  USER    SEGMENT CODE    ;Segment for user program
                     15  RAMTAB  SEGMENT DATA    ;Segment for table in
                                                 ;internal RAM
                     16  RAMVAR  SEGMENT DATA    ;Segment for RAM variables
                                                 ;in RAM
                     17  ;
                     18  ;
----                 19          RSEG    RAMVAR
0000:          R     20  STACK:  DS 20           ;Reserve stack area
                     21  ;
                     22  ;
----                 23          CSEG AT 00H
0000: 020000   R     24          JMP MAIN        ;Reset vector
                     25  ;
                     26  ;
----                 27          CSEG AT 03H
0003: 020000   R     28          JMP INT0_SRV    ;I2C interrupt vector
                                                 ;(INT0/)
                     29  ;
                     30  ;
----                 31          RSEG USER
                     32  ;Define I2C clock, own slave address and PCF8584
                         ;hardware address
0055                 33  SLAVE_ADR EQU 55H       ;Own slave address is 55H
001C                 34  I2C_CLOCK EQU 00011100B ;12.00MHz/90kHz
0000                 35  PCF8584   EQU 0000H     ;PCF8584 address with A0=0
                     36  ;
0000: 7581FF   R     37  MAIN:   MOV SP,#STACK-1 ;Initialize stack pointer
                     38  ;Initialize 8031 interrupt registers for I2C
                         ;interrupt
0003: D2A8           39          SETB EX0        ;Enable interrupt INT0/
0005: D2AF           40          SETB EA         ;Set global enable
0007: D2B8           41          SETB PX0        ;Priority level '1'
0009: D288           42          SETB IT0        ;INT0/ on falling edge
                     43  ;
                     44  ;Initialize PCF8584
000B: 120000   R     45          CALL I2C_INIT
                     46  ;
                     47  ;Make a table in RAM with data to be transmitted.
000E: 120021   R     48          CALL MAKE_TAB
                     49  ;
                     50  ;Set variables to control PCF8584
0011: D200     R     51          SETB DIR        ;DIR='transmission'
0013: 750000   R     52          MOV BASE,#TABLE ;Start address of I2C-data
0016: 750005   R     53          MOV NR_BYTES,#05H ;5 bytes must be
                                                 ;transferred
0019: 750074   R     54          MOV SLAVE,#01110100B ;Slave address PCD8577
                                                 ; + WR/
```

```
001C: 120000   R     55           CALL START       ;Start I2C transmission
                     56  ;
                     57  ;
001F: 80FE           58  LOOP:    JMP LOOP         ;Endless loop when program
                                                   ;is finished
                     59  ;
                     60  ;
0021:                61  MAKE_TAB:
0021: 7800     R     62           MOV R0,#TABLE    ;Make data ready for I2C
                                                   ;transmission
0023: 7600           63           MOV @R0,#00      ;Controlword PCD8577
0025: 08             64           INC R0
0026: 76FC           65           MOV @R0,#0FCH    ;'0'
0028: 08             66           INC R0
0029: 7660           67           MOV @R0,#60H     ;'1'
002B: 08             68           INC R0
002C: 76DA           69           MOV @R0,#0DAH    ;'2'
002E: 08             70           INC R0
002F: 76F2           71           MOV @R0,#0F2H    ;'3'
0031: 22             72           RET
                     73  ;
                     74  ;
----                 75           RSEG RAMTAB
0000:          R     76  TABLE:   DS 10            ;Reserve space in internal
                                                   ;data RAM
                     77                           ;for I2C data to transmit
                     78  ;
                     79  ;
000A:                80           END
```

```
ASM51  TSW  ASSEMBLER   Receive 2 bytes from the PCF8574P on OM1016

LOC   OBJ          LINE  SOURCE

                      1  $TITLE (Receive 2 bytes from the PCF8574P on OM1016)
                      2  $PAGELENGTH(40)
                      3  ;
                      4  ;This program is an example to receive bytes via
                         ;PCF8584
                      5  ;from the I2C-bus
                      6  ;
                      7           PUBLIC  SLAVE_ADR,I2C_CLOCK,PCF8584
                      8           EXTRN   CODE(I2C_INIT,INT0_SRV,START)
                      9           EXTRN   BIT(I2C_END,DIR)
                     10           EXTRN   DATA(BASE,NR_BYTES,IIC_CNT,SLAVE)
                     11  ;
                     12  ;
                     13  ;Define used segments
                     14  USER     SEGMENT CODE     ;Segment for user program
                     15  RAMTAB   SEGMENT DATA     ;Segment for table in
                                                   ;internal RAM
                     16  RAMVAR   SEGMENT DATA     ;Segment for RAM variables
                                                   ;in RAM
                     17  ;
                     18  ;
----                 19           RSEG    RAMVAR
0000:          R     20  STACK:   DS 20            ;Reserve stack area
                     21  ;
                     22  ;
----                 23           CSEG AT 00H
0000: 020000   R     24           JMP MAIN         ;Reset vector
                     25  ;
                     26  ;
----                 27           CSEG AT 03H
0003: 020000   R     28           JMP INT0_SRV     ;I2C interrupt vector
                                                   ;(INT0/)
                     29  ;
                     30  ;
----                 31           RSEG USER
                     32  ;Define I2C clock, own slave address and PCF8584
                         ;hardware address
0055                 33  SLAVE_ADR EQU 55H        ;Own slave address is 55H
001C                 34  I2C_CLOCK EQU 00011100B ;12.00MHz/90kHz
0000                 35  PCF8584   EQU 0000H      ;PCF8584 address with A0=0
                     36  ;
0000: 7581FF   R     37  MAIN:    MOV SP,#STACK-1 ;Initialize stack pointer
                     38  ;Initialize 8031 interrupt registers for I2C
                         ;interrupt
0003: D2A8           39           SETB EX0         ;Enable interrupt INT0/
0005: D2AF           40           SETB EA          ;Set global enable
0007: D2B8           41           SETB PX0         ;Priority level '1'
0009: D288           42           SETB IT0         ;INT0/ on falling edge
                     43  ;
                     44  ;Initialize PCF8584
000B: 120000   R     45           CALL I2C_INIT
                     46  ;
                     47  ;Set variables to control PCF8584
000E: C200     R     48           CLR  DIR         ;DIR='receive'
0010: 750000   R     49           MOV BASE,#TABLE ;Start address of I2C-data
0013: 750002   R     50           MOV NR_BYTES,#02H ;2 bytes must be received
0016: 75004F   R     51           MOV SLAVE,#01001111B ;Slave address PCF8574
                                                   ; + RD
0019: 120000   R     52           CALL START       ;Start I2C transmission
                     53  ;
                     54  ;
001C: 80FE           55  LOOP:    JMP LOOP         ;Endless loop when program
                                                   ;is finished
```

```
                      56  ;
                      57  ;
----                  58          RSEG RAMTAB
0000:           R     59  TABLE:  DS 10             ;Reserve space in internal
                                                    ;data RAM
                      60                          ;for received I2C data
                      61  ;
                      62  ;
000A:                 63          END
```

```
ASM51  TSW  ASSEMBLER   Demo program for PCF8584 I2C-routines

LOC   OBJ          LINE  SOURCE

                      1  $TITLE (Demo program for PCF8584 I2C-routines)
                      2  $PAGELENGTH(40)
                      3  ;Program displays on the LCD display  the time (with
                         ;PCF8583). Dots on LCD display blink every second.
                      5  ;On the LED display the values of the successive
                         ;analog input channels are shown.
                      7  ;Program reads analog channels of PCF8591P.
                      8  ;Channel number and channel value are displayed
                         ;successively.
                      9  ;Values are displayed on LCD and LED display on I2C
                         ;demo board.
                     10  ;
                     11          PUBLIC    SLAVE_ADR,I2C_CLOCK,PCF8584
                     12          EXTRN     CODE(I2C_INIT,INT0_SRV,START)
                     13          EXTRN     BIT(I2C_END,DIR)
                     14          EXTRN     DATA(BASE,NR_BYTES,IIC_CNT,SLAVE)
                     15  ;
                     16  ;
                     17  ;Define used segments
                     18  USER    SEGMENT   CODE    ;Segment for user program
                     19  RAMTAB  SEGMENT   DATA    ;Segment for table in
                                                   ;internal RAM
                     20  RAMVAR  SEGMENT   DATA    ;Segment for variables
                     21  ;
----                 22          RSEG RAMVAR
0000:          R     23  STACK:   DS 20             ;Stack area (20 bytes)
0014:                24  PREVIOUS: DS 1            ;Store for previous seconds
0015:                25  CHANNEL:DS 1              ;Channel number to be
                                                   ;sampled
0016:                26  AN_VAL: DS 1              ;Analog value sampled
                                                   ;channel
0017:                27  CONVAL: DS 3              ;Converted BCD value sampled
                                                   ;channel
                     28  ;
----                 29          CSEG AT 00H
0000: 020000   R     30          LJMP MAIN         ;Reset vector
                     31  ;
----                 32          CSEG AT 03H       ;INT0/
0003: 020000   R     33          LJMP INT0_SRV     ;Vector I2C-interrupt
                     34  ;
                     35  ;
----                 36          RSEG USER
                     37  ;Define I2C clock, own slave address and address for
                         ;main processor
0055                 38  SLAVE_ADR EQU 55H         ;Own slaveaddress is 55h
001C                 39  I2C_CLOCK EQU 00011100B ;12.00MHz/90kHz
0000                 40  PCF8584   EQU 0000H       ;Address of PCF8584. This
                                                   ;must be an EVEN number!!
                     41  ;Define addresses of I2C peripherals
00A3                 42  PCF8583R  EQU 10100011B ;Address PCF8583 with Read
                                                   ;active
00A2                 43  PCF8583W  EQU 10100010B ;Address PCF8583 with Write
                                                   ;active
009F                 44  PCF8591R  EQU 10011111B ;Address PCF8591 with Read
                                                   ;active
009E                 45  PCF8591W  EQU 10011110B ;Address PCF8591 with Write
                                                   ;active
0074                 46  PCD8577W  EQU 01110100B ;Address PCD8577 with Write
                                                   ;active
0076                 47  SAA1064W  EQU 01110110B ;Address SAA1064 with Write
                                                   ;active
                     48  ;
0000: 7581FF   R     49  MAIN:    MOV SP,#STACK-1 ;Define stack pointer
```

```
ASM51  TSW  ASSEMBLER   Demo program for PCF8584 I2C-routines

LOC   OBJ           LINE  SOURCE

                     50  ;Initialize 80C31 interrupt registers for I2C
                         ;interrupt (INT0/)
0003: D2A8           51          SETB EX0        ;Enable interrupt INT0/
0005: D2AF           52          SETB EA         ;Set global enable
0007: D2B8           53          SETB PX0        ;Priority level is '1'
0009: D288           54          SETB IT0        ;INT0/ on falling edge
                     55  ;Initialize PCF8584
000B: 120000    R    56          CALL I2C_INIT
                     57  ;
000E: 751500    R    58          MOV CHANNEL,#00 ;Set AD-channel
                     59  ;
                     60  ;Time must be read from PCF8583.
                     61  ;First write word address and control register of
                         ;PCF8583.
0011: D200      R    62          SETB DIR        ;DIR='transmission'
0013: 750000    R    63          MOV BASE,#TABLE ;Start address I2C data
0016: 750002    R    64          MOV NR_BYTES,#02H ;Send 2 bytes
0019: 7500A2    R    65          MOV SLAVE,#PCF8583W
001C: E4             66          CLR A
001D: F500      R    67          MOV TABLE,A     ;Data to be sent (word
                                                 ;address).
001F: F501      R    68          MOV TABLE+1,A   ;       "          (control
                                                 ;byte)
0021: 120000    R    69          CALL START      ;Start transmission.
0024: 3000FD    R    70  FIN_1:  JNB I2C_END,FIN_1 ;Wait till transmission
                                                 ;finished
                     71  ;Send word address before reading time
0027: D200      R    72  REPEAT: SETB DIR        ;'transmission
0029: 750000    R    73          MOV BASE,#TABLE ;I2C data
002C: 7500A2    R    74          MOV SLAVE,#PCF8583W
002F: 7401           75          MOV A,#01
0031: F500      R    76          MOV NR_BYTES,A  ;Send 1 byte
0033: F500      R    77          MOV TABLE,A     ;Data to be sent is '1'
0035: 120000    R    78          CALL START      ;Start I2C transmission
0038: 3000FD    R    79  FIN_2:  JNB I2C_END,FIN_2 ;Wait till transmission
                                                 ;finished
                     80  ;
                     81  ;Time can now be read from PCF8583. Data read is
                     82  ;hundredths of sec's, sec's, min's and hr's
003B: C200      R    83          CLR DIR         ;DIR='receive'
003D: 750000    R    84          MOV BASE,#TABLE ;I2C table
0040: 750004    R    85          MOV NR_BYTES,#04; 4 bytes to receive
0043: 7500A3    R    86          MOV SLAVE,#PCF8583R
0046: 120000    R    87          CALL START      ;Start I2C reception
0049: 3000FD    R    88  FIN_3:  JNB I2C_END,FIN_3 ;Wait till finished
                     89  ;
                     90  ;Transfer data to R2...R5
004C: 7800      R    91          MOV R0,#TABLE   ;Set pointers
004E: 7902           92          MOV R1,#02H     ;Pointer R2
0050: E6             93  TRANSFER:MOV A,@R0
0051: F7             94          MOV @R1,A
0052: 08             95          INC R0
0053: 09             96          INC R1
0054: D500F9    R    97          DJNZ NR_BYTES,TRANSFER
0057: ED             98          MOV A,R5        ;Mask of hour counter
0058: 543F           99          ANL A,#3FH
005A: FD            100          MOV R5,A
                    101  ;
                    102  ;Data must now be displayed on LCD display.
                    103  ;First minutes and hours (in R4 and R5) must be
                    104  ;converted from BCD to LCD segment data.The segment
                         ;data
                    105  ;will be transferred to TABLE. R0 is pointer to table
```

```
ASM51  TSW  ASSEMBLER   Demo program for PCF8584 I2C-routines

LOC   OBJ          LINE  SOURCE

005B: 7800     R   106          MOV R0,#TABLE
005D: 7600         107          MOV @R0,#00H     ;Control word for PCD8577
005F: 08           108          INC R0 0060: 120080   R   109          CALL CONV
                   110  ;
                   111  ;Switch on dp between hours and minutes
0063: 430301   R   112          ORL TABLE+3,#01H
                   113  ;If lsb of seconds is '0' then switch on dp.
0066: EB           114          MOV A,R3         ;Get seconds
0067: 13           115          RRC A            ;lsb in carry
0068: 4003         116          JC PROCEED
006A: 430101   R   117          ORL TABLE+1,#01H;switch on dp
                   118  ;
                   119  ;Now the time (hours,minutes) can be displayed on
                        ;the LCD
006D:              120  PROCEED:
006D: D200     R   121          SETB DIR         ;Direction 'transmit'
006F: 750000   R   122          MOV BASE,#TABLE
0072: 750005   R   123          MOV NR_BYTES,#05H
0075: 750074   R   124          MOV SLAVE,#PCD8577W
0078: 120000   R   125          CALL START       ;Start transmission
                   126  ;
007B: 3000FD   R   127  FIN_4:  JNB I2C_END,FIN_4
007E: 8026         128          JMP ADCON        ;Proceed with AD-conversion
                                                 ;part
                   129  ;
                   130 ;*************************************************************
                   131  ;Routines used by clock part of demo
                   132  ;
                   133  ;CONV converts hour and minute data to LCD data and stores
                   134  ;it in TABLE.
0080: 90009C   R   135  CONV:   MOV DPTR,#LCD_TAB ;Base for LCD segment table
0083: ED           136          MOV A,R5         ;Hours to accu
0084: C4           137          SWAP A           ;Swap nibbles
0085: 120096   R   138          CALL LCD_DATA    ;Convert 10's hours to LCD
                                                 ;data in table
0088: ED           139          MOV A,R5         ;Get hours
0089: 120096   R   140          CALL LCD_DATA
008C: EC           141          MOV A,R4         ;Get minutes
008D: C4           142          SWAP A
008E: 120096   R   143          CALL LCD_DATA    ;Convert 10's minutes
0091: EC           144          MOV A,R4
0092: 120096   R   145          CALL LCD_DATA    ;Convert minutes
0095: 22           146          RET
                   147  ;
                   148  ;LCD_DATA gets data from segment table and stores it in TABLE
0096: 540F         149  LCD_DATA:ANL A,#0FH      ;Mask off LS-nibble
0098: 93           150          MOVC A,@A+DPTR   ;Get LCD segment data
0099: F6           151          MOV @R0,A        ;Save data in table
009A: 08           152          INC R0
009B: 22           153          RET
                   154  ;
                   155  ;LCD_TAB is conversion table for LCD
009C:              156  LCD_TAB:
009C: FC60DA       157          DB 0FCH,60H,0DAH; '0','1','2'
009F: F266B6       158          DB 0F2H,66H,0B6H; '3','4','5'
00A2: 3EE0FE       159          DB 3EH,0E0H,0FEH; '6','7','8'
00A5: E6           160          DB 0E6H          ; '9'
                   161  ;
```

```
ASM51  TSW  ASSEMBLER   Demo program for PCF8584 I2C-routines

LOC   OBJ          LINE  SOURCE


                    162 ;*********************************************************************
                    163 ;
                    164 ;
                    165 ;These part of the program reads an analog input-channel.
                    166 ;Displaying is done on the LED-display
                    167 ;On odd-seconds the channel number will be displayed.
                    168 ;On even-seconds the analog value of this channel is displayed
                    169 ;Then the next channel is displayed.
                    170 ;
00A6: EB            171 ADCON:  MOV A,R3          ;Get seconds
00A7: 13            172         RRC A             ;lsb to carry
00A8: 503C          173         JNC NEW_MEAS      ;Even seconds; do a
                                                  ;measurement on the current channel
                    174 ;
                    175 ;Display and/or update channel
00AA: 33            176         RLC A             ;Restore accu
00AB: B51402    R   177         CJNE A,PREVIOUS,NEW_CH ;If new seconds,
                                                  ;update channel number
00AE: 800A          178         JMP DISP_CH
00B0: 0515      R   179 NEW_CH: INC CHANNEL
00B2: E515      R   180         MOV A,CHANNEL     ;If channel=4 then
                                                  ;channel:=0
00B4: B40403        181         CJNE A,#04,DISP_CH
00B7: 751500    R   182         MOV CHANNEL,#00
00BA: 8B14      R   183 DISP_CH:MOV PREVIOUS,R3 ;Update previous seconds
00BC: E515      R   184         MOV A,CHANNEL     ;Get segment value of
                                                  ;channel
00BE: 900193    R   185         MOV DPTR,#LED_TAB
00C1: 93            186         MOVC A,@A+DPTR
                    187 ;
00C2: 7800      R   188         MOV R0,#TABLE     ;Fill table with I2C data
00C4: 7600          189         MOV @R0,#00       ;SAA1064 instruction byte
00C6: 08            190         INC R0
00C7: 7677          191         MOV @R0,#77H      ;SAA1064 control byte
00C9: 08            192         INC R0
00CA: F6            193         MOV @R0,A         ;Channel number
00CB: E4            194         CLR A
00CC: 08            195         INC R0
00CD: F6            196         MOV @R0,A         ;Second digit
00CE: 08            197         INC R0
00CF: F6            198         MOV @R0,A         ;Third digit
00D0: 08            199         INC R0
00D1: F6            200         MOV @R0,A         ;Fourth byte
                    201 ;
00D2: D200      R   202         SETB DIR          ;I2C transmission of channel
                                                  ;number
00D4: 750000    R   203         MOV BASE,#TABLE
00D7: 750006    R   204         MOV NR_BYTES,#06H
00DA: 750076    R   205         MOV SLAVE,#SAA1064W
00DD: 120000    R   206         CALL START
                    207 ;
00E0: 3000FD    R   208 FIN_5:  JNB I2C_END,FIN_5
00E3: 020027    R   209         JMP REPEAT        ; Repeat clock and AD cycle
                                                  ; again
                    210 ;
                    211 ;
```

```
ASM51  TSW  ASSEMBLER   Demo program for PCF8584 I2C-routines

LOC   OBJ          LINE  SOURCE

                    212  ;Measure and display the value of an AD-channel
00E6: 120108   R    213  NEW_MEAS: CALL AD_VAL    ;Do measurement
                    214  ;Wait till values are available
00E9: 3000FD   R    215  FIN_6:  JNB I2C_END,FIN_6
                    216  ;Relevant byte in TABLE+1. Transfer to AN_VAL
00EC: 7801     R    217          MOV R0,#TABLE+1
00EE: 8616     R    218          MOV AN_VAL,@R0
00F0: E516     R    219          MOV A,AN_VAL     ;Channel value in accu for
                                                 ;conversion
                    220  ;AN_VAL is converted to BCD value of the measured
                         ;voltage.
                    221  ;Input value for CONVERT in accu
                    222  ;Address for MSByte in R1
00F2: 7917     R    223          MOV R1,#CONVAL
00F4: 120154   R    224          CALL CONVERT
                    225  ;Convert 3 bytes of CONVAL to LED-segments
00F7: 900193   R    226          MOV DPTR,#LED_TAB ;Base of segment table
00FA: 7817     R    227          MOV R0,#CONVAL
00FC: 12018A   R    228          CALL SEG_LOOP
                    229  ;Display value of channel to LED display
00FF: 12012C   R    230          CALL LED_DISP
0102: 3000FD   R    231  FIN_8:  JNB I2C_END,FIN_8 ;Wait till I2C
                                                   ;transmission is ended
0105: 020027   R    232          JMP REPEAT       ;Repeat clock and AD cycle
                    233  ;
                    234 ;*************************************************************
                    235  ;Routines used for AD converter.
                    236  ;
                    237  ;AIN reads an analog values from channel denoted by
                         ;CHANNEL.
                    238  ;Send controlbyte:
0108: D200     R    239  AD_VAL: SETB DIR          ;I2C transmission
010A: 7800     R    240          MOV R0,#TABLE    ;Define control word
010C: A615     R    241          MOV @R0,CHANNEL
010E: 750000   R    242          MOV BASE,#TABLE ;Set base at table
0111: 750001   R    243          MOV NR_BYTES,#01H ;Number of bytes to be
                                                   ;send
0114: 75009E   R    244          MOV SLAVE,#PCF8591W ;Slave address PCF8591
0117: 120000   R    245          CALL START       ;Start transmission of
                                                   ;controlword
011A: 3000FD   R    246  FIN_7:  JNB I2C_END,FIN_7 ;Wait until transmission is
                                                   ;finished
                    247  ;Read 2 data bytes from AD-converter
                    248  ;First data byte is from previous conversion and not
                    249  ;relevant
011D: C200     R    250          CLR DIR          ;I2C reception
011F: 750000   R    251          MOV BASE,#TABLE ;Bytes must be stored in
                                                   ;TABLE
0122: 750002   R    252          MOV NR_BYTES,#02H; Receive 3 bytes
0125: 75009F   R    253          MOV SLAVE,#PCF8591R ;Slave address PCF8591
0128: 120000   R    254          CALL START
012B: 22            255          RET
                    256  ;
                    257  ;LED_DISP displays the data of 3 bytes from address
                         ;CONVAL
012C:               258  LED_DISP:
012C: 431780   R    259          ORL CONVAL,#80H ;Set decimal point
012F: 7800     R    260          MOV R0,#TABLE
0131: 7917     R    261          MOV R1,#CONVAL
0133: 7600          262          MOV @R0,#00      ;SAA1064 instruction byte
0135: 08            263          INC R0
```

```
ASM51  TSW  ASSEMBLER   Demo program for PCF8584 I2C-routines

LOC   OBJ           LINE  SOURCE

0136: 7677          264          MOV @R0,#01110111B ;SAA1064 control byte
0138: 08            265          INC R0
0139: 7600          266          MOV @R0,#00      ;First LED digit
013B: 08            267          INC R0
013C: 120185   R    268          CALL GETBY       ;Second digit
013F: 120185   R    269          CALL GETBY       ;Third digit
0142: 120185   R    270          CALL GETBY       ;Fourth digit
0145: D200     R    271          SETB DIR         ;I2C transmission
0147: 750000   R    272          MOV BASE,#TABLE
014A: 750006   R    273          MOV NR_BYTES,#06
014D: 750076   R    274          MOV SLAVE,#01110110B
0150: 120000   R    275          CALL START       ;Start I2C transmission
0153: 22            276          RET
                    277  ;
                    278  ;CONVERT calculates the voltage of the analog value.
                    279  ;Analog value must be in accu
                    280  ;BCD result (3 bytes) is stored from address stored
                         ;in R1
                    281  ;Calculation: AN_VAL*(5/256)
0154: 75F005        282  CONVERT:MOV B,#05
0157: A4            283          MUL AB
                    284  ;b2..b0 of reg. B : 2E+2..2E0
                    285  ;b7..b0 of accu   : 2E-1..2E-8
0158: A7F0          286          MOV @R1,B        ;Store MSB (10E0-units)
015A: 09            287          INC R1
015B: 7700          288          MOV @R1,#00      ;Calculate 10E-1 unit
                                                  ;(10E-1 is 19h)
015D: B41C02        289  TEN_CH: CJNE A,#19H+03H,V1  ;Check if accu <= 0.11
0160: 8002          290          JMP TENS         ;accu=0.11; update tens
0162: 4006          291  V1:     JC NX_CON        ;accu<0.11; update hundreds
0164: C3            292  TENS:   CLR C           ;Calculate new value
0165: 9419          293          SUBB A,#19H
0167: 07            294          INC @R1          ;Update BCD byte
0168: 80F3          295          JMP TEN_CH
                    296  ;Correction may be necessary. With 8 bits '0.1' is
                         ;in fact 0.0976.
                    297  ;A digit of '0A' may appear. Correct this by
                         ;decrementing the digit.
                    298  ;The intermediate result result must be corrected
                         ;with 10*(0.1-0.0976)
                    299  ;This is 06H
016A: B70A03        300  NX_CON: CJNE @R1,#0AH,PROC_CON ; If digit is '0A'
                                                  ;then correct
016D: 17            301          DEC @R1
016E: 2419          302          ADD A,#19H
0170: 09            303  PROC_CON:INC R1
0171: 7700          304          MOV @R1,#00      ;Calculate 10E-2 units
0173: B40302        305  HUND:   CJNE A,#03H,V2  ;Check if accu <= 10E-2
0176: 8002          306          JMP HUNS         ;accu=10E-2; update hundreds
0178: 4006          307  V2:     JC FINISH        ;accu<10E-2; conversion
                                                  ;finished
017A: C3            308  HUNS:   CLR C           ;Calculate new value
017B: 9403          309          SUBB A,#03H
017D: 07            310          INC @R1          ;Update BCD byte
017E: 80F3          311          JMP HUND
0180: B70A01        312  FINISH: CJNE @R1,#0AH,FIN ;Check if result is '0A'.
                                                  ;Then correct.
0183: 17            313          DEC @R1
0184: 22            314  FIN:    RET
                    315  ;
                    316  ;CALLBY transfers byte from @R1 to @R0
0185: E7            317  GETBY:  MOV A,@R1
0186: F6            318          MOV @R0,A
```

```
ASM51  TSW  ASSEMBLER   Demo program for PCF8584 I2C-routines

LOC   OBJ          LINE  SOURCE

0187: 08           319          INC R0
0188: 09           320          INC R1
0189: 22           321          RET
                   322  ;
                   323  ;SEG_LOOP converts 3 values to segment values.
                   324  ;R0 contains address of source and destination
                   325  ;DPTR contains base of table
018A: 7903         326  SEG_LOOP: MOV R1,#03     ;Loop counter
018C: E6           327  INLOOP: MOV A,@R0      ;Get value to be displayed
018D: 93           328          MOVC A,@A+DPTR  ;Get segment value from
                                                ;table
018E: F6           329          MOV @R0,A       ;Store segment data
018F: 08           330          INC R0
0190: D9FA         331          DJNZ R1,INLOOP
0192: 22           332          RET
                   333  ;
                   334  ;
                   335  ;LED_TAB is conversion table for BCD to LED segments
0193:              336  LED_TAB:
0193: 7D483E       337          DB 7DH,48H,3EH  ; '0','1','2'
0196: 6E4B67       338          DB 6EH,4BH,67H  ; '3','4','5'
0199: 734C7F       339          DB 73H,4CH,7FH  ; '6','7','8'
019C: 4F           340          DB 4FH          ; '9'
                   341  ;
                   342 ;*************************************************************
                   343  ;
----               344          RSEG RAMTAB
0000:          R   345  TABLE:  DS 10
                   346  ;
000A:              347          END
```


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TTX-generator for the SAA7182/3 (EURO-DENC)

Author: John McNally

DESCRIPTION

The Teletext Module is used to provide digital data to the TTX pin of the SAA7182/3 for encoding onto its analog outputs in the correct form for further decoding inside a television.

A microcontroller reads the **TTX** data from an EPROM which contains six pages of Teletext data. It Is read out of the EPROM and into a FIFO line by line as each line is requested. The 8 bit data is converted to serial form, under control of the microcontroller and a multiplexer, before being stored in the FIFO. The write clock, write enable and **RSTW** are controlled by the microcontroller. The function of the FIFO is to decouple the slower write bit stream of the microcontroller from the fast 27MHz bit stream required by the DENC. The **RSTR** signal for the FIFO is signal **VS** from the DENC.

Signal **TTXREQ** from the DENC starts the process. When it goes high the data in the FIFO is read into the TTX pin of the DENC at the appropriate bit rate for encoding. When **TTXREQ** goes low it causes an interrupt. The microcontroller will then reset the write pointer and write the next line into the FIFO.

When Teletext is active the DENC will start to output bits 10.2 µS after the start of the sync pulse regardless of the data on the **TTX** input. Therefore it is up to the user to program **TTXREQ** to be active at a point that will allow the module to respond and send out the data such that the first bit encoded is the first bit of the run in code. The pipeline delay in the DENC is about 70 LLC clocks. The easiest method to get the correct position of **TTXREQ** is by using a scope with two inputs. One input is connected to **TTXREQ** which is used as the trigger. The other is connected to **Pin 73 CVBS** on the DENC. Register **TTXHS** can then be adjusted so that the run in and framing codes can be seen as a stationary sine wave on the scope. The remainder of the line will be continuously changing as the data changes. Register **TTXHE** can then be adjusted to give the correct length of **TTXREQ.**

PARTS LIST

TYPE	NUMBER
Semiconductors	
IC 74151 (Multiplexer)	1
TMS4C1070 (FIFO)	1
74HCT08 (AND-Gate)	1
27256 (256k PROM)	1
87C654 (microcontroller)	1
Capacitors	
100 nF	5
33 pF	2
2.2 µF	1
10 µF	1
Resistors	
10 kΩ	1
8 × 1 kΩ (Array)	2

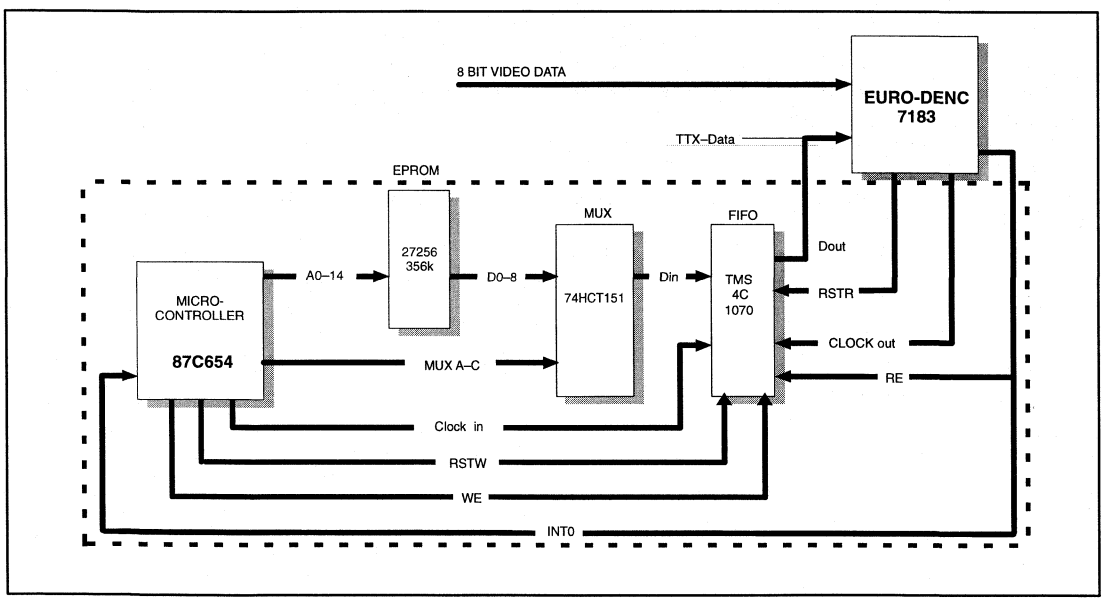


Figure 1. Block diagram of the TTX Module

ASSEMBLER CODE FOR THE 80C654

```
$TITLE(U.Bergmann TTX-MODUL fuer 87654)
; ENGLISH TRANSLATION BY JOHN MCNALLY
$DATE(08.05.1995)
;OPERATION:-
;THE MICRO INITIALIZES ITS PORTS AND REGISTERS THEN LOOPS FOREVER.
;WHEN AN INTERRUPT COMES FROM TTXREQ GOING LOW THE MICRO DISABLES FIFO
;READS THEN WRITES A LINE OF TEXT DATA INTO THE FIFO. THE DATA CONTAINS
;EVERYTHING REQUIRED BY A TEXT DECODER INCLUDING RUN IN AND FRAME BYTES.
;THE DATA IS WRITTEN ACCORDING TO THE EURO DENC PROTOCOL REGARDING THE
;NUMBER OF CLOCKS PER TTX BIT. IE THREE OR FOUR. THE DATA FROM THE
;EPROM IS SERIALIZED USING AN EIGHT TO ONE MUX CONTROLLED BY THE MICRO.
;THEN WHEN TTXREQ IS HIGH, THE DATA FOR A LINE IS READ OUT FROM
;THE FIFO WITH NO INTERVENTION FROM THE MICRO. THE READ POINTER IS RESET
;EVERY FIELD BY VS.
;*******************************************************************************
;REGISTER DEFINITION
;*******************************************************************************
RSTW       BIT   P1.3              ; RESET FIFO WRITE POINTER
SWCK       BIT   P1.4              ; FIFO WRITE CLOCK
READ       BIT   P1.5              ; FIFO READ ENABLE = READ*TTXREQ
L_ADR      EQU   DPL               ; EPROM LOW ADDRESS BYTE
H_ADR      EQU   DPH               ; EPROM HIGH ADDRESS BYTE
BYTE_NO    EQU   R0                ; TTX BYTE NUMBER. 1 TO 37
BYTES      EQU   R2                ; NO. OF BYTES TO SEND
NBR_BYTE   EQU   40H               ; ACTIVE BYTES PER LINE
NBR_BIT    EQU   08H               ; MUX BIT COUNT
NBR_OUT    EQU   04H               ; MAXIMUM NO OF COUNTS PER BIT
ADR_START  EQU   0200H             ; ROM START ADDRESS
L_ADR_END  EQU   00H               ; LAST LOW ADDRESS OF ROM
H_ADR_END  EQU   2CH               ; LAST HIGH ADDRESS OF ROM
;*******************************************************************************
;RESET AND INTERRUPT CALLS
;*******************************************************************************
ORG 0000H
RES:               LJMP MAIN       ; JUMP TO MAIN PROGRAM AFTER RESET
ORG 0003H
IN0:               LJMP INTERRUPT  ; JUMP TO THE INTERRUPT ROUTINE
                                   ; INT0 IS CONNECTED TO TTXREQ
ORG 000BH
TIF0:              RETI
ORG 0013H
IN1:               RETI
ORG 001BH
TIF1:              RETI
ORG 0023H
RITI:              RETI
ORG 0100H
```

```
;*******************************************************************************
;MAIN PROGRAM
;*******************************************************************************
MAIN:       CALL INIT               ; INIT
            SETB IE.7               ; ENABLE INTERRUPTS
            SETB IE.0               ; ENABLE INT0
LOOP:       JMP  LOOP               ; WAIT FOR AN INTERRUPT
;*******************************************************************************
;SUB ROUTINES
;*******************************************************************************
;*******************************************************************************
;REGISTER- AND BIT INITIALIZATION
;*******************************************************************************
INIT:       MOV P1,#00H                 ; PORT1 = 00H
            MOV P3,#00H                 ; PORT3 = 00H
            MOV DPTR,#ADR_START         ; RESET THE VARIABLES
            MOV BYTES,#00H              ; BYTE COUNTER = 00H
            MOV BYTE_NO,#01H            ; BYTE_NO = FIRST
            SETB IP.0                   ; SET  INTERRUPT PRIORITY LEVEL
            NOP
            SETB TCON.0                 ; ACTIVE LOW EDGE
                                        ; TRIGGERED INTERRUPT
            NOP
            RET
;*******************************************************************************
;WRITE A TTX-LINE
;*******************************************************************************
WRT_TXTLINE:
            MOV BYTES,#NBR_BYTE     ; LOAD BYTE COUNTER
            MOV BYTE_NO,#01H        ; BYTE_NO STARTS AT ONE
TXT_LOOP:
            MOV P0,L_ADR
            MOV P2,H_ADR            ; ADDRESS THE EPROM
MUX:
            MOV R6,#00H
MUX_LOOP:
            MOV P1,R6               ; PUT EACH BIT IN THE FIFO
VALUE:
            MOV R5,#NBR_OUT
HOWMANY:
            MOV A,#0AH
            XRL A,BYTE_NO
            JZ  THREETIMES
            MOV A,#13H              ; ALGORITHM TO DETERMINE
                                    ; WHETHER EACH BIT IS
            XRL A,BYTE_NO           ; CLOCKED THREE OR FOUR TIMES
                                    ; INTO THE FIFO
            JZ  THREETIMES
            MOV A,#1CH
            XRL A,BYTE_NO
            JZ  THREETIMES
            MOV A,#25H
            XRL A,BYTE_NO
```

```
                JZ  FULLBYTE_NO
                SJMP BIT_LOOP
FULLBYTE_NO:
                MOV BYTE_NO,#00H
THREETIMES:
                DEC  R5
BIT_LOOP:
                NOP
BIT_LOOP2:
                SETB SWCK           ; SET THE CLOCK-BIT
                NOP                 ; WAIT
                CLR SWCK            ; RESET THE CLOCK-BIT
                NOP                 ; WAIT
                DJNZ R5,BIT_LOOP2
                INC  BYTE_NO        ; BLOCK = 36+1
                INC  R6             ; INC MUX ADDRESS
                MOV  A,#NBR_BIT
                XRL  A,R6
                JNZ  MUX_LOOP
                INC  DPTR
                DJNZ BYTES,TXT_LOOP
                RET
;*************************************************************************
;INTERRUPT 0 ROUTINE
;*************************************************************************
INTERRUPT:
                CLR IE.7            ; DISABLE INTERRUPTS
RESET_FIFO:
                SETB RSTW           ; RESET FIFO WRITE POINTER
                SETB SWCK           ; SET THE CLOCK-BIT
                NOP
                CLR SWCK            ; RESET THE CLOCK-BIT
                CLR RSTW
DIS_READROM:
                CLR READ            ; DISABLE FIFO READ
                CALL WRT_TXTLINE    ; WRITE A TEXT LINE
EN_READROM:
                SETB READ           ; ENABLE FIFO READ
ADR_CHECK:
                MOV A,#H_ADR_END
                XRL A,H_ADR
                JNZ CHK_END
                MOV A,#L_ADR_END
                XRL A,L_ADR
                JNZ CHK_END
                MOV DPTR,#ADR_START ; RELOAD START ADDRESS
CHK_END:
                SETB IE.7           ; ENABLE INTERRUPTS
                SETB IE.0           ; ENABLE INT0
                RETI
;*************************************************************************
END
```

POSSIBLE REGISTER SETTINGS FOR THE SAA7182/83 IN TELETEXT MODE

```
REG 3a = c7
REG 42 = 6b
REG 43 = 0
REG 44 = 0
REG 45 = 52
REG 46 = 90
REG 47 = 12
REG 48 = 2a
REG 49 = 26
REG 4a = 90
REG 4b = 11
REG 4c = b6
REG 4d = a2
REG 4e = ea
REG 4f = 4a
REG 50 = 5e
REG 51 = d1
REG 52 = da
REG 53 = 70
REG 54 = a9
REG 55 = 70
REG 56 = ee
REG 57 = 90
REG 58 = 0
REG 59 = 0
REG 5a = 70
REG 5b = 7d
REG 5c = af
REG 5d = 2d
REG 5e = 3f
REG 5f = 3f
```

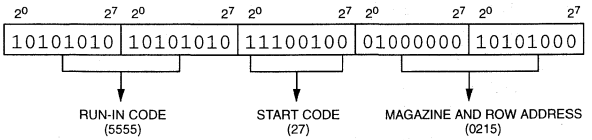
```
REG 60 = 70
REG 61 = 6
REG 62 = 4b
REG 63 = cb
REG 64 = 8a
REG 65 = 9
REG 66 = 2a
REG 67 = 55
REG 68 = 56
REG 69 = 67
REG 6a = 58
REG 6b = 12
REG 6c = 2a
REG 6d = 1
REG 6e = 20
REG 6f = 31
REG 70 = 80
REG 71 = e8
REG 72 = 10
REG 73 = 3e
REG 74 = b8
REG 75 = 61
REG 76 = 15
REG 77 = 16
REG 78 = 15
REG 79 = 16
REG 7a = 18
REG 7b = 38
REG 7c = 40
REG 7d = e0
```

TTX-generator for the SAA7182/3 (EURO-DENC)

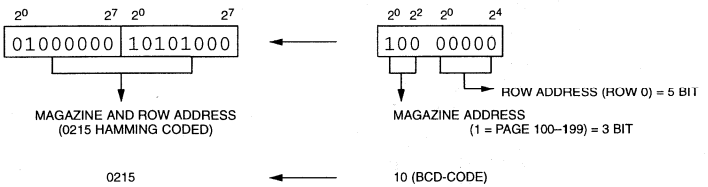
PAGE AND LINE ORGANIZATION FOR TELETEXT

A Teletext page consists of 24 rows of 45 bytes. The first row, the header or Row 0 is the leader row for the rest of the page. (Rows 1–23). The beginning (Byte 1–5) of each row has the same format, The first 3 bytes are used for bit and byte synchronization, where the first two bytes are the run-in-code (Bit synchronizing) and the 3rd byte the Start code (Byte synchronizing). Bytes 4 and 5 are Hamming-Coded with the 3-Bit Magazine number and a 5-Bit Row address.

Prefix:



Magazine and Row address:



Hamming Codes:

DECIMAL	HAMMING	DECIMAL	HAMMING
0	15	8	D0
1	02	9	C7
2	49	10	8C
3	5E	11	9B
4	64	12	A1
5	73	13	B6
6	38	14	FD
7	2F	15	EA

Example 1: Page 123 Row 0 hamming code 0215

Example 2: Page 123 Row 1 hamming code C715

Example 3: Page 123 Row 2 hamming code 0202

Example 4: Page 555 Row 15 hamming code B62F

TTX-generator for the SAA7182/3 (EURO-DENC)

BIT SEQUENCE IN THE FIFO

Within 52µs 45 Bytes (= 360 Bits) are written, giving a data rate of 6,923 Mbit/s. The data rate is however 6,9375 Mbit/s, which is 444 times the television line frequency of 15625 Hz. As the clock frequency of the EURO–DENC is 27 MHz, a frequency conversion is required. This can be achieved by using the conversion table shown below.

f = 6,9375 MHz * 144/37 = 27 MHz

BIT/CLOCK

1/1	7/25	113/49	**19/73**	25/97	31/121
1/2	7/26	13/50	**19/74**	25/98	32/122
1/3	7/27	13/51	20/75	26/99	32/123
1/4	7/28	14/52	20/76	26/100	32/124
2/5	8/29	14/53	20/77	26/101	32/125
2/6	8/30	14/54	20/78	26/102	33/126
2/7	8/31	14/55	21/79	27/103	33/127
2/8	8/32	15/56	21/80	27/104	33/128
3/9	9/33	15/57	21/81	27/105	33/129
3/10	9/34	15/58	21/82	27/106	34/130
3/11	9/35	15/58	22/83	**28/107**	34/131
3/12	9/36	16/60	22/84	**28/108**	34/132
4/13	**10/37**	16/61	22/85	**28/109**	34/133
4/14	**10/38**	16/62	22/86	29/110	35/134
4/15	**10/39**	16/63	23/87	29/111	35/135
4/16	11/40	17/64	23/88	29/112	35/136
5/17	11/41	17/65	23/89	29/113	35/137
5/18	11/42	17/66	23/90	30/114	36/138
5/19	11/43	17/67	24/91	30/115	36/139
5/20	12/44	18/68	24/92	30/116	36/140
6/21	12/45	18/69	24/93	30/117	36/141
6/22	12/46	18/70	24/94	31/118	**36/142**
6/23	12/47	18/71	25/95	31/119	**37/143**
6/24	13/48	**19/72**	25/96	31/120	**37/144**

CHARACTER-CODE TABLE

Character	Code (Hex)	Character	Code (Hex)
A	c1	a	61
B	c2	b	62
C	43	c	e3
D	c4	d	64
E	45	e	e5
F	46	f	e6
G	c7	g	67
H	c8	h	68
I	49	i	e9
J	4a	j	ea
K	cb	k	6b
L	4c	l	ec
M	cd	m	6d
N	ce	n	6e
O	4f	o	ef
P	d0	p	70
Q	51	q	f1
R	52	r	f2
S	d3	s	73
T	54	t	f4
U	d5	u	75
V	d6	v	76
W	57	w	f7
X	58	x	f8
Y	d9	y	79
Z	da	z	7a
1	31	␣	20
2	32	,	2c
3	b3	.	ae
4	b4	/	2f
5	b5	(	a8
6	b6	)	29
7	37	'	a7
8	38	*	2a
9	b9	–	ad
0	b0	+	ab
		;	bb

NOTES:

This Character–Code Table is only a part of the full Code-Table!
Bit 7 is the parity bit.

TTX-generator for the SAA7182/3 (EURO-DENC)

PART OF A TTX–PAGE– EPROM CODE

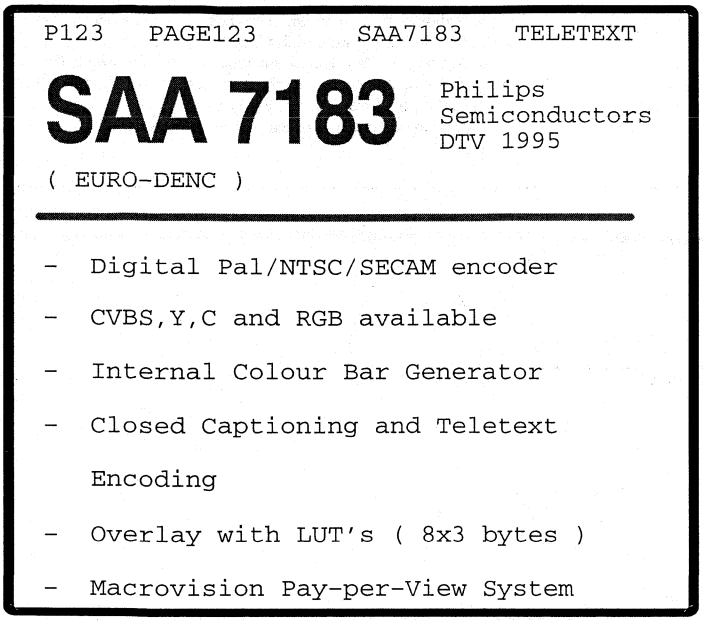
Page 333:

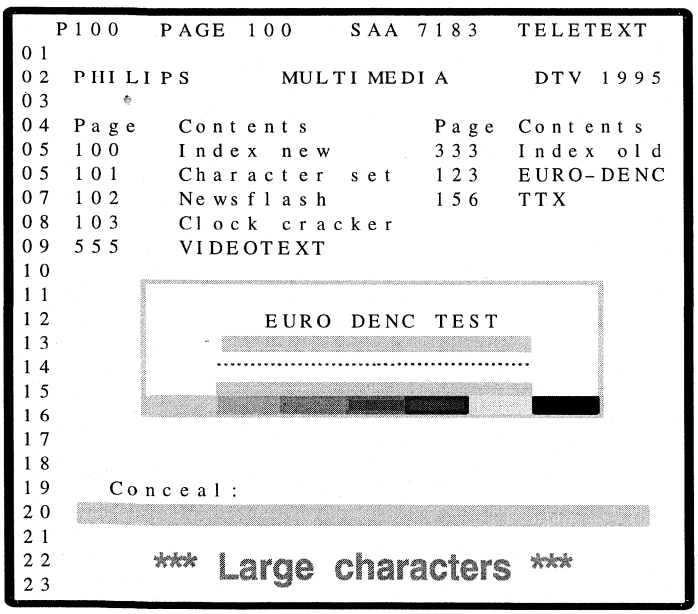
```
:10020000555527 5E15 5E5E 151515151515D0C1C718     Line 0
      *1 ◄┘  *2 ◄┘    └► *3
:100210004520B3B3B3202020D3C1C120373138B338
:10022000202054454C4554455854202020000000BF
:1002300000000000000000000000000000000000BE
:10024000555527 9B15B031202020202020202020 2C     Line 1
:10025000202020202020202020202020202020209E
:10026000202020202020202020202020000000EE
:1002700000000000000000000000000000000007E
:10028000555527 5E02B03220202049CEC445582063      Line 2
:10029000202020D0524FCD20D6E5F273E9EF6E201A
:1002A00031AEB020202020202020202000000007F
:1002B0000000000000000000000000000000003E
:1002C0005555279B02B0B3202020202020202020 3D      Line 3
:1002D000202020202020202020202020202020201E
:1002E000202020202020202020202020200000006E
:1002F0000000000000000000000000000000000FE
:10030000555527 5E49B034202020D06167E5202074      Line 4
:10031000202020 43EF6EF4E56EF47320202020208F
:10032000202020202020202020202020200000002D
:1003300000000000000000000000000000000000BD
:10034000555527 9B49B0B52020202031B0B0202042      Line 5
:10035000202020496E64E5F820202020202020 45
:10036000202020202020202020202020200000000ED
:1003700000000000000000000000000000000007D
:10038000555527 5E5EB0B62020202031B0312020A8      Line 6
:10039000202020436861F261E3F4E5F22073E558
:1003A000F4202020202020202020202020000000D9
:1003B0000000000000000000000000000000003D
:1003C0005555279B5EB0372020202031B0322020A9      Line 7
:1003D000202020 20CEE5F773E6EC61736820202012
:1003E000202020202020202020202020200000006D
:1003F0000000000000000000000000000000FD
:10040000555527 5E64B0382020202031B0B320201D      Line 8
:10041000202020 43ECEFE36B20E3F261E36BE567
:10042000F2202020202020202020202020000005A
:1004300000000000000000000000000000000BC
:10044000555527 9B64B0B920202020B5B5B5202094      Line 9
:10045000202020D649C4454F5445585420202000
:10046000202020202020202020202020200000EC
:1004700000000000000000000000000000000007C
:
```

NOTES:
*1 **framing code (includes: clock run in)**
*2 magazine and row address
*3 *page*

TTX-generator for the SAA7182/3 (EURO-DENC)

EXAMPLES OF TELETEXT PAGES:





Comb filter application

COMB FILTER APPLICATION

One of the functions that must be performed by a color video decoder is to separate the composite video signal into the luminance (brightness) and chrominance (hue and saturation) components. This is generally performed by one of two methods:

A bandpass/bandtrap method which results in removing the subcarrier frequency portion (and some surrounding frequencies) from the video signal, see Figure 1.

The disadvantage of this method is that luminance information that exists in the frequency domain close to that of the subcarrier is lost.

The second (and more expensive) method is to use a comb filter. Comb filters take advantage of the fact that, generally, the luminance content of a video signal does not change greatly from one line to the next and that the chrominance signal is inverted from one line to the next (this is due to the fact that the subcarrier frequency is an odd multiple of the half line frequency). See Figure 2.

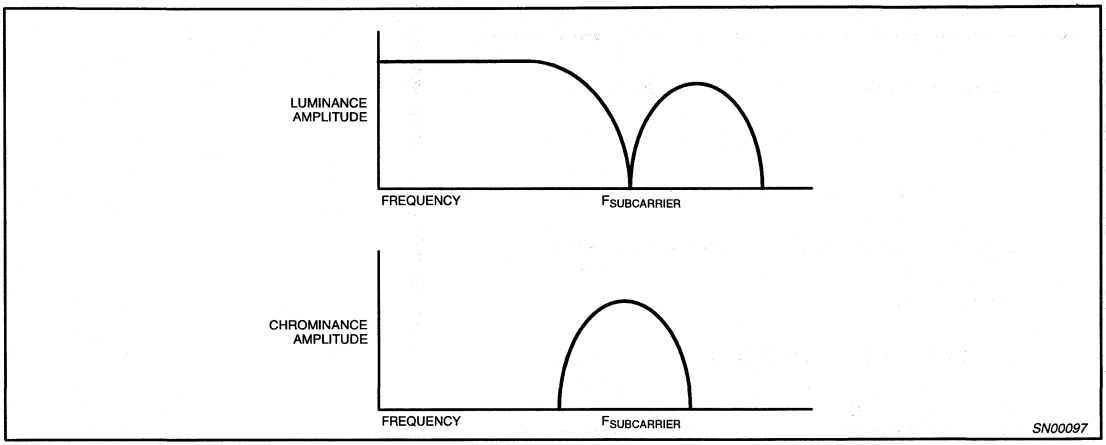


Figure 1.

Comb filter application

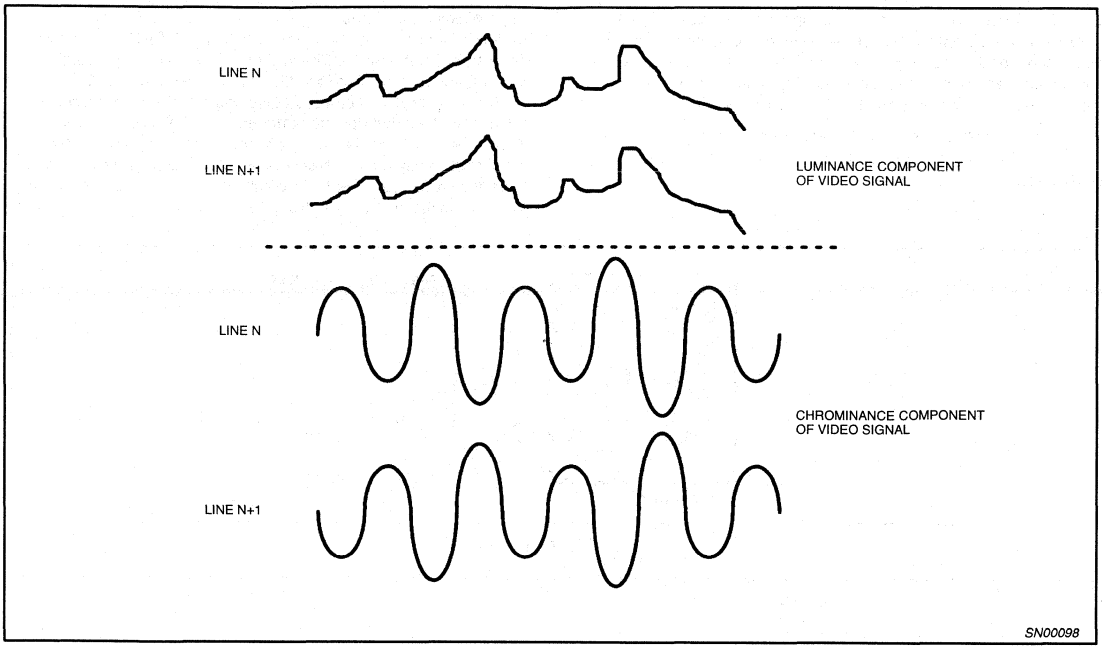


Figure 2.

Composite video is passed into the comb filter which stores one line of video (line N) and then compares the stored line with the next (line N+1).

Luminance is derived by summing the two lines and dividing by two. The luminance content is doubled (and subsequently divided by two) and the chrominance cancels out.

Chrominance is derived by inverting one line (line N) and summing lines N and N+1 with the luminance canceling out and the chrominance doubled (then normalized by dividing in half).

The advantage is that luminance information that consists of frequencies around that of the subcarrier, is maintained.

One drawback to comb filters is that in situations where the video signal does change greatly from one line to the next (as in the case when a horizontal object is depicted), certain artifacts may be created. This is especially true with horizontal graphics that are overlayed onto the video because, unlike camera images that exhibit some low frequency roll-off (due to the analog nature of the imager), graphics can create changes in the line to line video that are quite abrupt. As a result of the two-line summation/cancellation nature of the comb filter, if there is an abrupt change from one line to the next, un-cancelled subcarrier information (and un-cancelled luminance content) may remain. This can result in a softening of the edge of the horizontal structure (due to residual luminance) and a line of unsuppressed subcarrier at the transition, sometimes called "hanging dots". Some comb filters minimize this effect by detecting these abrupt transitions and switching momentarily from a comb filter mode to a chroma trap mode (the first separation method mentioned above). This is known as adaptive comb filtering.

Two types of comb filters are covered here, an analog glass delay line type, the CFM300 and switched capacitor delay line type, the SAA4961. Composite video is input to either of these devices and the Y/C output is input to the decoder which is programmed to process the input as S-Video (the decoder chroma notch is turned off).

The CFM300 is an integrated hybrid circuit module which is adjustment-free. The device consists of a precision-ground glass wave guide with two piezo-electric transducers bonded to two corners. One of these transducers is a transmitter. It converts the electronic video signal to an ultrasonic sound wave which is then propagated through the glass and received by the other transducer and converted back to video. The length of propagation time from transmitter to receiver is exactly one horizontal period. See Figure 3.

The reconverted and delayed video signal (line N) is then summed with the current video signal (line N+1) as described above to produce the luminance and chrominance signals. The CFM300 is not adaptive. The advantage of this type of comb filter is that it is inexpensive and will work with time-variant signals such as VCRs. The disadvantage is its size. However, a horizontal version is available, called the CFM330.

The other type of comb filter, The SAA4961 uses a switched capacitor delay line to produce the line-length delays required. This capacitor delay line is incremented by a clock running at the subcarrier frequency. This clock can either be derived from the input signal (easily done in the case of an analog decoder application, not easily done in the case of a digital decoder application) or from an oscillator. See Figure 4.

Comb filter application

The SAA4961 will perform comb filtering for either Pal or NTSC (the CFM300 is NTSC only). The subcarrier clock frequency must match that of the standard being combed. The SAA4961 is an adaptive comb filter that will switch to a chroma trap mode in the event of a discontinuity from the previous line to the next.

An application schematic for both comb filters is included with the DPC71 evaluation board application note (sheet 4 of the DPC71 schematics).

Applications in which the video is scaled down for display in a window or for compression (such as JPEG or MPEG) generally do not require comb filtering. The added resolution from the comb filtering process would be lost anyway (in the case of JPEG or MPEG compression, it could actually degrade the compression ratio). Also, because Pal subcarrier is at a substantially higher frequency than that of NTSC (4.43MHz as opposed to 3.58MHz), the chroma notch method has less of a detrimental effect on the luminance response. Therefore comb filtering is not as necessary for high luminance response from Pal.

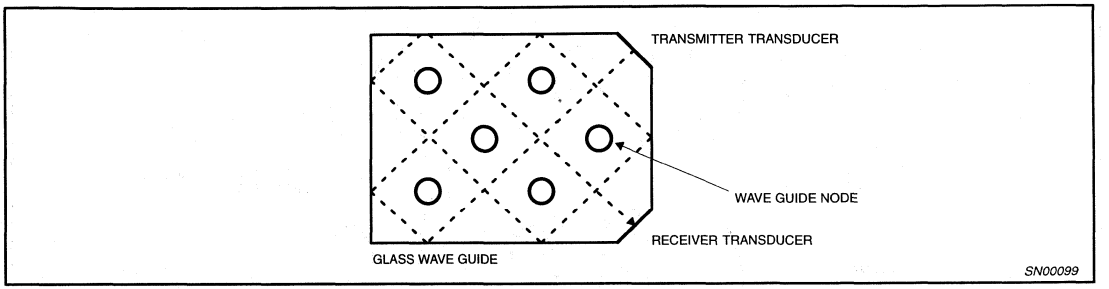


Figure 3.

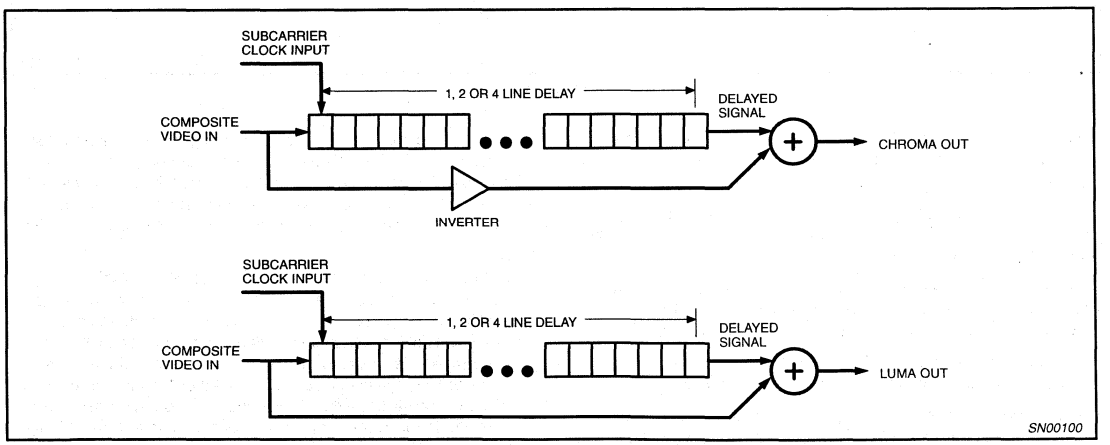


Figure 4.

ORDERING INFORMATION

CFM300	4322-027-06182	(vertical mounting)
CFM330	4322-027-06212	(horizontal mounting)

CONTACT INFORMATION

Philips Components
Marketing Communications
Building BAE-1
5600 MD
Eindhoven, The Netherlands
Fax. +31 40 27 24547

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Philips Road
Blackburn, United Kingdom BB1 5RZ
Tel. +44 1254 55241
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U.S.A Only

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Philips Components
1440 W. Indiantown Rd.
P.O. Box 689605
Jupiter, FL 33468-9605
Tel. +1 561 745 3300
Fax. +1 561 745 3601, +1 561 745 3602

DEVICE DATA

(in alphanumeric sequence)

1.0 INTRODUCTION

1.1 GENERAL DESCRIPTION

This document describes the Philips Semiconductors 90C24LC Windows Accelerated High Resolution VGA LCD Controller for Low Power Applications (hereinafter referred to as the 90C24LC Controller).

The Philips Semiconductors 90C24LC is a 0.9 micron CMOS VLSI device with the capability to drive flat panel displays and standard CRTs. The 90C24LC allows simultaneous display of a CRT and a monochrome dual-panel, or a CRT and a color panel. This device is backwards compatible with previous video standards including MDA, EGA, and CGA.

The 90C24LC provides enhanced power management with 3.3 VDC power input or a mix of 3.3 VDC and 5 VDC power input. Its performance-scaling capability makes it an ideal video solution for low battery drain portable computer applications.

1.2 FEATURES OF THE 90C24LC

- Hardware Windows Acceleration
- Hardware Bit Block Transfers (BITBLT)
- Hardware line draw
- Programmable Hardware Cursor (64 by 64 by 2)
- Simultaneous Display on all CRT and LCDs for all Standard Modes
- Programmable Power Management
- Support for 256K color STN and color TFT LCDs
- Single chip for 8-bit or 16-bit AT Bus Interface and 32-bit VESA VL-Bus (local bus) interface
- Supports 16-bit or 32-bit memory interface
- Integrated 16-bit High Color RAMDAC
- Integrated Programmable Pixel Clock Synthesizer
- Integrated Programmable Dithering Logic for the Highest Contrast Video with Utility Support.
- Support for 64K simultaneous colors on CRT, single-panel color STN LCD, and color TFT LCD
- Direct interface to single-panel (1/480) or dual-panel (1/240) monochrome STN LCD, single or dual panel color STN or color TFT LCD and plasma display
- Provides 64 True Shade gray scale support for monochrome STN LCD flat panel display
- Up to 65 MHz video clock for the CRT display, up to 65 MHz for color TFT LCD display, and up to 50 MHz video clock for the monochrome STN LCD display
- Up to 50 MHz memory clock
- Supports memory configuration of 256 Kbytes to 1 Mbyte with 256K by 16, or 256K by 4 DRAMs
- With 256K of DRAM installed, supports all IBM VGA modes for CRT and LCD display
- With 1 Mbyte of DRAM installed, supports high resolution graphics with up to 1024 by 768 by 256 colors in CRT and flat-panel modes.
- Provides host data bus interface for 8- or 16-bit CPU I/O and memory cycles.
- Supports high 16-bit color for CRT or flat panel display at up to 640 by 480 resolution for 64K color simultaneous display on one frame for CRT, color STN LCD, and color TFT LCD displays
- Fast page display memory fetching for both graphic and text modes
- Programmable virtual memory addressing for CPU memory address space
- Four levels of write cache for zero wait state CPU operation during memory write
- Emulates planar mode addressing for packed pixel mode operation to achieve faster block transfers

- Operates with 5 volt and 3.3 volt power supplies (mixed voltage operation)
- Intelligent power management control to reduce the power requirement for the display subsystem
- Supports 132-column text mode
- Provides a signature analyzer to help with IC and board-level test of video data output from the controller.
- PINSCAN I/O mapping allows the 90C24LC to enter a test mode to enable quick open and short checks for board-level test
- Uses 208-pin EIAJ package
- Directly drives all 640 by 480 (400) monochrome and color flat panel displays, such as STN, TFT, EL, and plasma displays without external components
- Provides a Dual panel (1/240) color STN LCD interface.
- Supports monochrome 640 by 480 single-panel (1/480) STN, 4-bit or 8--bit, flat-panel
- Provides algorithm enhancement to support vertical screen expansion in text mode. Raster lines are duplicated above or below the character block. This takes care of not creating breaks in continuous vertical lines.
- A Strip Line Draw algorithm is implemented in hardware to further improve Windows performance.
- I/O pins are remapped to improve the ICT (In-Circuit Test) of the device. Because there are more input pins than output pins, pairs of input pins had to be ORed to each output. There was a conflict in 3 pairs of pins in that they were next to each other, which would not allow for a "short test" on those pins. These 3 pairs of pins were AMD12 and AMD3, BMD12 and BMD3, and $\overline{\text{EBROM}}$ and $\overline{\text{VLBICS}}$.
- Supports hardware cursor for Dual panel (1/240) monochrome STN LCD panels.
- The PCLK output (pin 175) can now be turned off by a programmable bit to reduce EMI emissions.
- Configuration bit (CNF15) is added to accept the 2X clock from the new Intel S-series 486 microprocessors.
- Supports 800 by 600 color TFT panel.
- Supports enhanced power-down mode on VESA-VL local bus ($\overline{\text{REFLCL}}$)
- In Power-down mode, register PR4 bit 5 is used to turn off the panel data and control pins (XSCLK, RPTL/, WPTL/, UD(7:0), LD(7:0), FP, LP and FR). In the 90C24 these pins are tristated.

1.3 ORDERING INFORMATION

The 90C24LC controller is supplied in a 208-pin MQFP package under the following order number:

90C24LCZZ00

1.4 DOCUMENT SCOPE

In addition to this introduction to the 90C24LC controller, the following sections of this document provide a description of the controller architecture and related interfaces, memory configurations, signal descriptions, and internal register descriptions. In addition, this document contains application information for the hardware cursor, hardware BITBLT, hardware line drawing, embedded clock generator, internal RAMDAC, configuration registers, and associated application and program notes. Also included are the device specifications, timing information, and package dimensions. Special features of the 90C24LC including the signature analyzer, and I/O mapping for test purposes are also described.

This document includes the following two appendices:

Appendix A lists reference documents that may be useful to users of this document.

Appendix B provides a change history for this document.

2.0 ARCHITECTURE

2.1 INTRODUCTION

The 90C24LC controller is made up of the following major internal modules:

- CRT Controller
- Sequencer
- Graphics Controller
- Attribute Controller
- Flat Panel Controller and Interface
- VESA VL-Bus (Local Bus) Interface
- Hardware Cursor
- Dithering Engine
- Weight and Mapping Logic
- RAMDAC
- Clock Synthesizer
- Power-down Management
- Hardware Bit Block Transfer (BITBLT)
- Hardware Line Drawing
- Frame Buffer Controller

Each module is described in this section. Their interconnections are shown in Figures 2-1 and 2-2.

The 90C24LC uses a four-level write cache to achieve fast memory writes. Therefore, with a 32-bit display memory interface, zero wait states can be realized for most memory write operations.

Fast Page mode memory fetching is used to improve memory bandwidth. The 90C24LC uses a FIFO to provide the video display bandwidth necessary to interleave CPU accesses and display refresh cycles.

Weighting and Mapping Logic provides color-to-gray-scale mapping, and a dithering engine, that works like a digital DAC, generating the gray scale level for monochrome flat-panel displays. The dithering engine also generates colors for color flat-panel display. While driving the flat panel, a Row Buffer supports the split screen displays.

To support a split screen display when driving a flat panel and a CRT simultaneously, an external Frame Buffer may be required

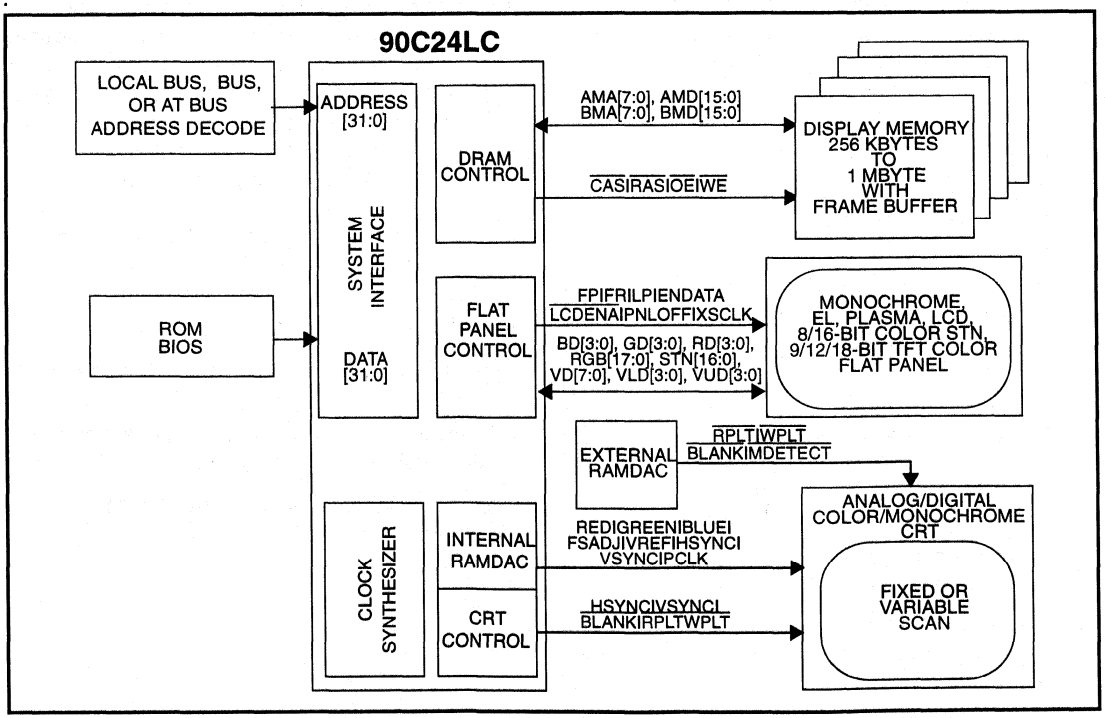


FIGURE 2-1. SYSTEM BLOCK DIAGRAM

2.2 CRT CONTROLLER

The CRT Controller performs the following functions:

- Generates horizontal sync (HSYNC) and vertical sync (VSYNC) for the CRT display monitor
- Simultaneous CRT and dual flat panel display is performed using frame buffer architecture
- Hidden display timing registers meet the fixed display timing for the flat panel display
- CRT display screen refresh is maintained for the various display modes defined by the BIOS ROM resident firmware
- Performs video split screen refresh and screen size mapping

2.3 SEQUENCER

The Sequencer performs the following functions:

- Timing generator for the display memory cycles
- Character clock in the alphanumeric mode, and the dot clock in the graphics mode
- Arbitrates between the video display refresh, memory refresh, and CRT access of the display memory for CRT only, flat panel only, or simultaneous CRT and single panel displays
- Arbitrates between the video display refresh, frame buffer access, memory refresh, and CRT access of the display memory for simultaneous CRT and dual panel displays
- Arbitrates cursor pattern access to the off-screen display memory when the hardware cursor is activated
- Provides the write cache control for CPU memory write to the video display memory

2.4 GRAPHICS CONTROLLER

The Graphics Controller manipulates the data flow between the CPU and the display memory for CPU write and read cycles. The Graphics Controller also controls data written to the CPU display memory.

2.5 ATTRIBUTE CONTROLLER

The Attribute Controller allows the following functions:

- Serializes the display memory data into a video data stream according to different display formats
- Controls the following features in all display modes:
  - Blinking
  - Underlining
  - Text cursor
  - Pixel panning
  - Reverse video
  - Background and foreground color
  - Border Controller

2.6 FLAT PANEL CONTROLLER AND INTERFACE

The Flat Panel Controller and Interface Module performs the following functions:

- Controls the video data flow after video data exits the RAMDAC palette RAM until the video data is output to the flat panel interface
- Generates the flat panel control signals:
  - Frame Rate (FR)
  - Frame Pulse (FP)
  - Latch Pulse (LP)
  - Shift Clock (XSCLK)
  - Data Enable (ENABLE)

These signals are generated with different timing and polarity in order to drive different types of panels without external components

- Split screen refresh for dual panel display and screen size mapping for both single and dual panel displays
- Performs split screen refresh and screen size mapping using frame buffer architecture (screen mapping includes vertical expansion and auto-centering)
- Controls the video data flow into and out of the row buffer (using frame buffer architecture)
- Controls the video data flow into and out of the frame buffer (using frame buffer architecture)

2.7 VESA VL-BUS INTERFACE

The 90C24LC provides a VESA VL-Bus (local bus) Interface for both the 486 and 386 CPU architectures. This interface can be implemented directly on the system motherboard or on a separate option card without adding extra glue logic. Through this interface, the 90C24LC connects directly to the host CPU address, data, and control lines. Using the VESA VL-Bus significantly improves system performance.

2.8 FRAME BUFFER CONTROLLER

The Frame Buffer Controller supports simultaneous display on a dual-flat panel or on a flat panel and CRT. This feature is fully supported for memory configuration 2 (refer to Section 4).

2.9 WEIGHT AND MAPPING LOGIC

For monochrome panel displays, the weight and mapping logic converts color information from the palette RAM into gray scale information using the following weighting equation:

I =.3R +.59G +.11B.

For monochrome display panels, the output code generated by the weighting equation selects gray shades depending on the modulation type:

- **Frame-Rate Modulation**

  The weighting code selects gray shades from the mapping RAM, which is loaded with 64 user-selected codes of shades with the optimum intensity.

- **Pulse-Width Modulation**

  The weighting code truncates or rounds off the shading information and sends it to the panel directly. With this information, the panel uses pulse-width modulation to generate related gray shades.

For color panel displays, the red, green, and blue color information that comes from the palette RAM provides the code for each color. Colors are selected depending on the color panel modulation type as follows:

- **Frame-Rate Modulation**

  The red, green, blue color data selects color shades from the dithering engine.

- **Pulse-Width Modulation**

  The color data can be sent directly to the panel or truncated and then sent to the panel.

2.10 DITHERING ENGINE

The Dithering Engine uses a dithering pattern and frame-rate modulation to constantly generate 64 gray shades. The dithering pattern for each shade is designed so that it creates minimum flicker on the panel screen.

2.11 HARDWARE BIT BLOCK TRANSFER (BITBLT)

The 90C24LC was designed with hardware support for Microsoft Windows, which supports accelerated Windows performance.

The 90C24LC Bit Block Transfer (BITBLT) increases speed. With BITBLT, blocks of pixels are transferred directly between regions of display memory and between display memory and system memory through a system I/O or memory port. For additional BITBLT information refer to Section 19.

2.12 HARDWARE LINE DRAWING

The 90C24LC provides a hardware line drawing engine that implements the Microsoft strip line algorithm. With this algorithm, the line draw engine interacts with software to determine the slope of the line and the number of pixels to be turned on. Line Draw operation is described in Section 20.

2.13 HARDWARE CURSOR

The Hardware Cursor provides up to a 64 by 64 pattern. Each pixel in the pattern is represented by two bits. These two bits determine how the cursor is displayed based on the color mode selected. The pattern is stored in the off-screen display memory. The hardware cursor is controlled by the following registers:

- Cursor Control
- Cursor Pattern Address

- Cursor Primary Color
- Cursor Secondary Color
- Cursor Auxiliary Color
- Cursor Origin
- Cursor Display Address X
- Cursor Display Address Y

The Cursor Display Address is the location for the origin of the cursor on the display screen. The Cursor Pattern Address is the starting memory location where the cursor pattern is stored in the display memory.

The Cursor Origin and the Cursor Display Address are used to calculate the cursor's starting display address. The cursor pattern is displayed on the window and the controller clips off the pattern. The pattern fetching request is sent to the sequencer. The cursor pattern is displayed when the display location matches the cursor start location. For additional information on the Hardware Cursor, refer to Section 18.

2.14 RAMDAC

The on-chip RAMDAC is low-power, PS/2-compatible with power-down control and built-in monitor detection logic with the following features:

- Three 256 by 6 RAMs as the R, G, B Color look-up tables
- Three 6-bit DACs
- Mask register
- Supports 16-bit high color

The 16 bits of video data are formed by five red bits, six green bits, and five blue bits, or five bits of each color with one bit ignored.

When in high color mode, video data bypasses the color palette RAM.

The LSB bit of the three DACs are forced to zero for 5-bit color configuration. The LSB bits of the Red DAC and Blue DAC are forced to zero for the 5-bit red, 6-bit green, and 5-bit blue configuration.

The DAC generates RS-343A/RS-170 compatible output and has 1/2 LSB of integral and differential linearity errors.

2.15 CLOCK SYNTHESIZER

The on-chip Clock Synthesizer is a dual clock generator for VGA applications. It simultaneously generates display memory clock (MCLK) and video dot clock (VCLK).

Both clock frequencies can be programmed by the user and are derived from the 14.318 MHz system clock available in the IBM PC/XT/AT and PS/2 computer systems.

The clock synthesizer has power-down control to achieve a low power consumption.

When programing a new clock frequency for both MCLK and VCLK, the Clock Synthesizer requires 20 ms to achieve a stable frequency. All the registers, palette RAM, and Mapping RAM must be reloaded after the clock frequency is stable.

2.16 POWER-DOWN MANAGEMENT

The 90C24LC provides four major power down modes:

- Deep Sleep Mode
- Suspend/Resume Mode (System Power-down Mode)
- General Power Down Mode (Internal)
- Display Idle Mode

Each of the power-down management modes is described briefly in the following paragraphs. Additional information about power-down management is provided in Section 26.

Deep Sleep Mode is used when the entire display subsystem can be turned off. This mode is designed to conserve the most power and also requires the most system overhead. In this mode, the 90C24LC current sink is less than 1 mA.

Suspend/Resume mode (also called System Power Down Mode) is used when a display is not required but minimum access to the display registers is required. In this mode, all supply voltages (VDD) remain active, but the Clock Synthesizers are shut down. For Suspend/Resume mode the 90C24LC current sink is less than 10 mA.

General Power Down Mode is used to turn off the display when the keyboard has been idle for a preset time interval. In this mode all the supply voltages (VDD) and the Clock Synthesizers remain on. The MCLK and VCLK clock rates can be slowed down to 1/8 of their normal frequency.

The Display Idle Mode is used to turn off the display when the keyboard has been idle for a preset time interval. The DAC and LCD panel interfaces are turned off in this mode. The CPU can access I/O registers of the 90C24LC, but it can not access display memory.

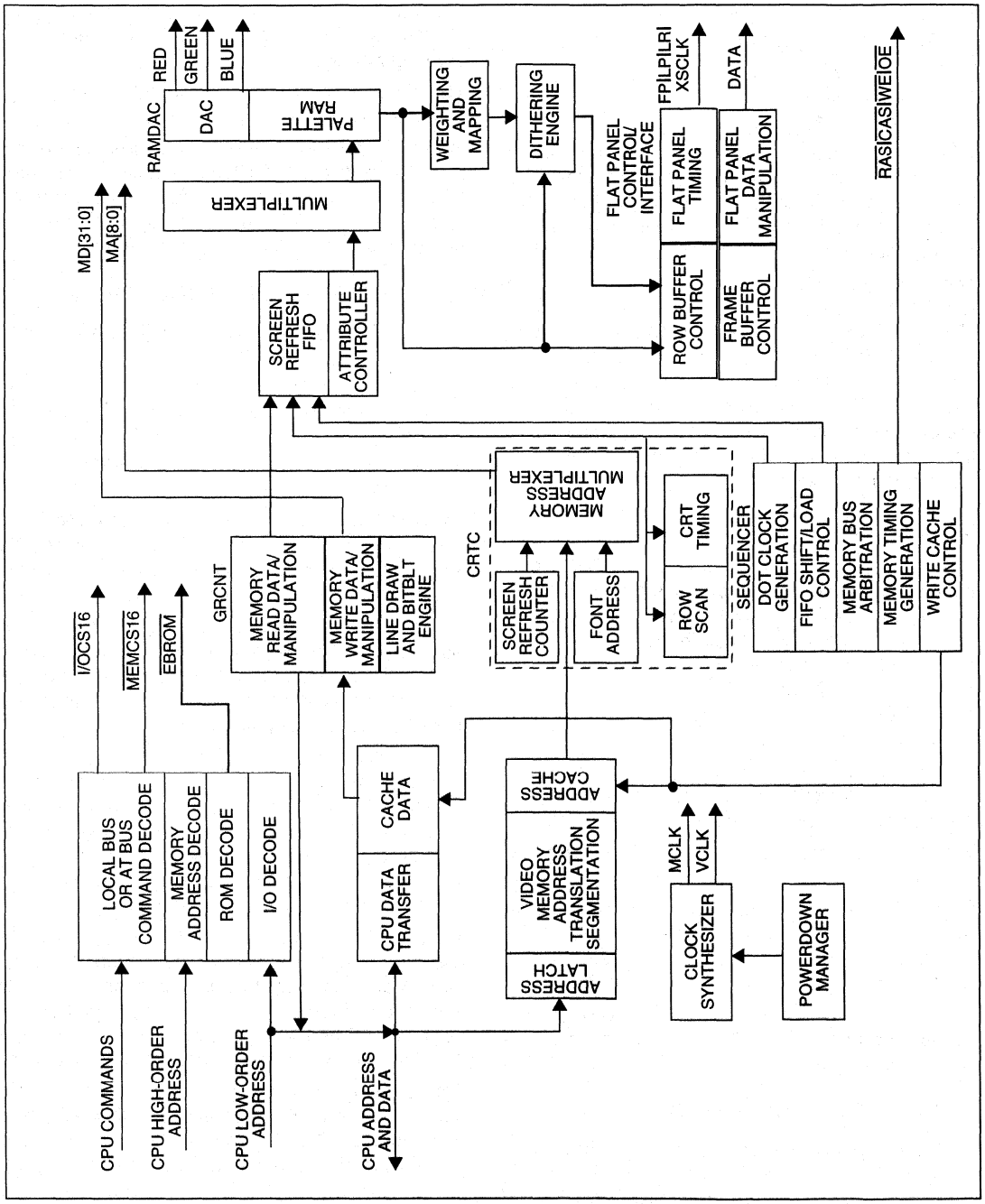


FIGURE 2-2. BLOCK DIAGRAM

3.0 INTERFACES

3.1 INTRODUCTION

The 90C24LC has five major interfaces, which are described in this section.

- System Interface
- BIOS ROM Interface
- Display Memory Interface
- ISA Bus Interface
- VESA VL-Bus Interface
- CRT Display Interface
- Flat Panel Display Interface

3.2 SYSTEM INTERFACE

The system interface operates with the following bus architectures:

- PC/XT/AT (ISA) bus (see Figure 3-1)
- VESA VL- Bus (local bus) (see Figure 3-3)
- Intel 386 DX local bus
- Intel 486 SX/DX local bus

The selection of the bus architecture depends on the setting of configuration bits CNF17 and CNF2 as listed in Table 3-1.

CNF17	CNF2	SYSTEM MODES
0	0	Reserved
0	1	ISA Bus
1	0	Reserved
1	1	Local Bus including VESA VL-Bus

TABLE 3-1. BUS ARCHITECTURE SELECTION

The bus architecture is selected during power-on and reset as described in Section 24 *90C24LC Configuration Registers.*

Other features of the system interface include:

- $\overline{\text{IOCS16}}$ and $\overline{\text{MEMCS16}}$ signals are generated to indicate 16-bit operation
- Minimal use of external circuitry
- Provides all signals, decodes all memory and I/O addresses to interface with any of the bus configurations in 8-bit or 16-bit mode.
- Decoding for video BIOS ROM while in extension card application (8-bit operation only)
- Reduced CPU wait states while writing to display memory with use of a display memory data and address write cache that holds CPU write data until it can be transferred to the display memory
- Improved performance of CPU display memory access -- PR0(A) and PR0(B) registers may be addressed indirectly
- Improved performance of CPU display memory access -- 32-bit memory data latch is addressable by the I/O port
- Sixteen segments of 1 Mbyte virtual memory addressing range or 32 segments of 512K-byte virtual memory addressing range for flexibility in memory allocation

3.3 BIOS ROM INTERFACE

The 90C24LC can be configured to provide an enable signal ($\overline{\text{EBROM}}$) for an external 8-bit video BIOS PROM. The 90C24LC is then configured to automatically map this video BIOS into the system memory map during power-on and reset. The external video BIOS can be selectively mapped out of system memory as required. Decodes are provided for 64 Kbytes of VGA video BIOS address space as defined in the VGA architecture.

3.4 DISPLAY MEMORY INTERFACE

For a 16-bit display memory interface, the following DRAM configurations can be used:

- One 256K by 16 DRAM or four 256K by 4 DRAMs
- Two 256K by 16 DRAMs

For a 32-bit memory interface, the following DRAM configurations can be used:

- Two 256K by 16 DRAMs
- Eight 256K by 4 DRAMs

Refer to Section 4 for a summary of display memory configurations.

In all cases, 90C24LC uses DRAM fast page mode for optimum performance.

3.4.1 Minimum Configuration

In the minimum configuration, which is one 256K by 16 DRAM, the 90C24LC can support all standard IBM VGA modes.

When additional DRAMs are installed, the 90C24LC is capable of supporting high color resolution video modes of up to 1024 by 768 by 256 colors, non-interlaced and 1280 by 1024 by 16 colors, interlaced.

3.4.2 Display Memory Features

- Supports 70 ns, 80 ns, and 100 ns DRAMs with the dedicated MCLK which can operate from 37.5 MHz to 44.3 MHz

NOTE

Longer DRAM access times require slower clock frequencies. Table 3-2 lists typical DRAM access times and memory clock limitations.

DRAM ACCESS TIME IN NANOSECONDS	MCLK FREQUENCY IN MEGAHERTZ (MAX)
70	44.3
80	39.8
100	37.5

TABLE 3-2. DRAM ACCESS TIME VERSUS MEMORY CLOCK FREQUENCY

- Fast page DRAM timing is used for all CPU access, graphics display and text display (a choice of page mode and non-page mode operation is provided to access fonts in text modes)
- Generates $\overline{CAS}$-before-$\overline{RAS}$ DRAM refresh for the display memory

3.4.3 VCLK to MCLK Ratio

The VCLK to MCLK ratio for the 90C24LC controller is specified as 1.6 or less. Exceeding this ratio may cause FIFO underflow problems.

The following table lists the VCLK and MCLK frequencies, their ratios, and recommended DRAM speed for two high resolution displays.

	RESOLUTION	
	1024X768X256 NON-INTERLACED (60 Hz)	1024X768X16 INTERLACED (43hZ)
VCLK (MHz)	65	44.5
MCLK (MHz)	44.3	39.8
VCLK/MCLK RATIO	1.5	1.1
DRAM SPEED (ns)	70	80

TABLE 3-3. VCLK TO MCLK RATIOS

3.5 ISA BUS INTERFACE

The 90C24LC interfaces to an ISA bus at bus clock rates of up to 12.5 MHz. The 90C24LC supports full 16-bit I/O and memory transfers. Support of 16-bit memory transfers is independent of whether the 90C24LC has an 8-bit or 16-bit display memory path, although increased performance occurs when a 16-bit display memory is available (See Figure 3-1).

LA(23:17) addresses are latched internal to the 90C24LC by the ALE signal to eliminate bus timing problems in some common system implementations.

I/O and memory operation (8/16-bit I/0 and 8/16 bit memory) can be separately enabled by selectively enabling $\overline{\text{IOCS16}}$ and $\overline{\text{MEMCS16}}$ bus interface signals.

The following ISA Bus signals are directly supported by the 90C24LC:

AEN	$\overline{\text{MEMR}}$
$\overline{\text{BALE}}$	$\overline{\text{MEMW}}$
LA[23:17]	$\overline{\text{0WS}}$
$\overline{\text{IOCHRDY}}$	$\overline{\text{REFRESH}}$
$\overline{\text{IOCS16}}$	RESET
$\overline{\text{IOR}}$	SA [16:0]
$\overline{\text{IOW}}$	$\overline{\text{SBHE}}$
$\overline{\text{MCS16}}$	SD[15:0]

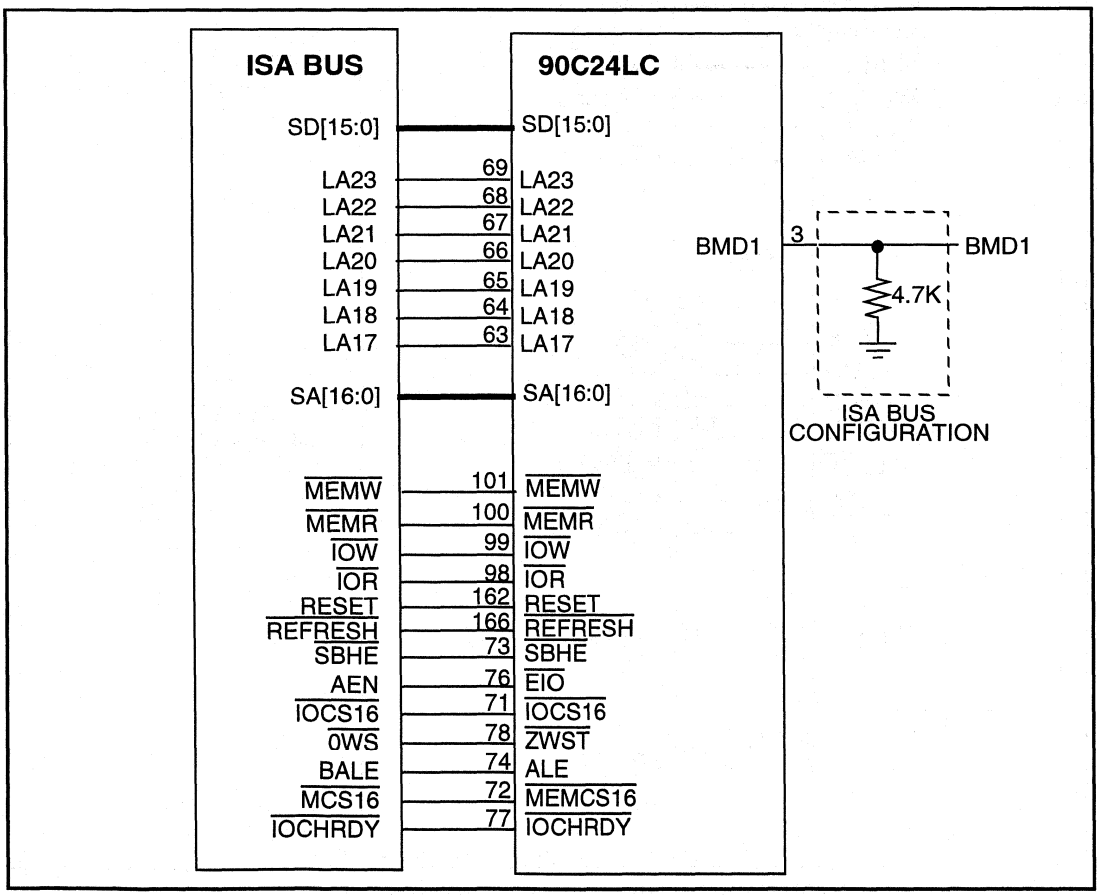


FIGURE 3-1. ISA BUS INTERFACE DIAGRAM

3.6 VESA VL-BUS INTERFACE

The 90C24LC directly supports the following VESA VL-Bus interface signals (see Figure 3-3).

ADR[31:2]	$\overline{LDEV}$
$\overline{ADS}$	$\overline{LRDY}$
$\overline{BE}$[3:0]	M/$\overline{IO}$
DAT[31:0]	$\overline{RESET}$
D/$\overline{C}$	$\overline{RDYRTN}$
LCLK	W/$\overline{R}$

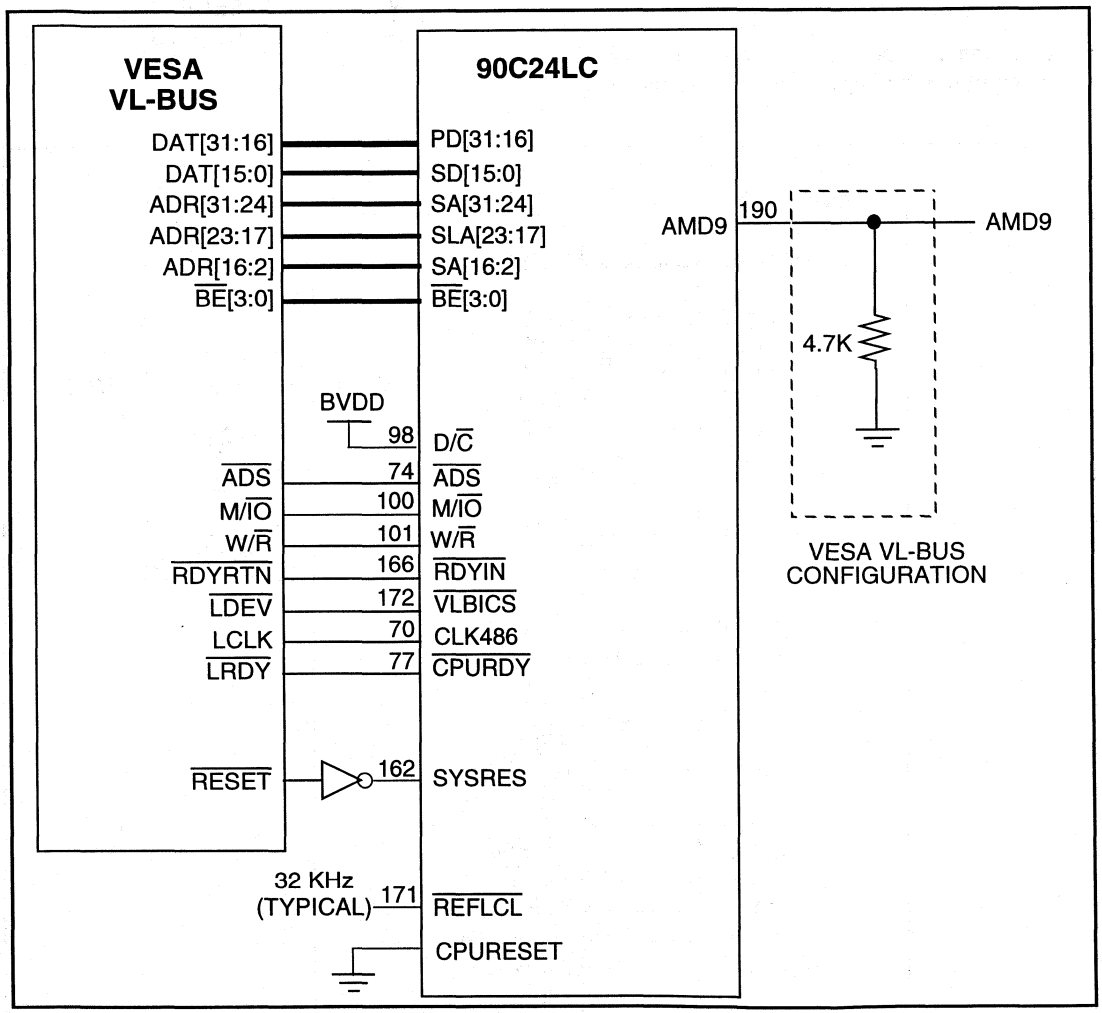


FIGURE 3-2. VESA VL-BUS INTERFACE DIAGRAM

3.7 CRT DISPLAY INTERFACE

- On-chip RAMDAC provides the RED, GREEN, and BLUE signals directly to the analog CRT monitor
- Provides HSYNC and VSYNC signals to control the monitor
- Allows use of an external RAMDAC to drive the CRT
- Supports Bt/471/478/476 compatible RAMDAC interface

3.8 FLAT PANEL DISPLAY INTERFACE

Features of the flat panel display interface include:

- Direct interface with 640 by 480 (400) STN, TFT, 1024 by 768 LCD, EL, and plasma panels
- Flat panel interface signals change function to support the panel type chosen
- Programmable timing and polarity for the flat panel control signals to meet the requirements of different panels
- Video data groupings to meet the requirements for different panels
- Controller supplies 8 pixels per shift clock with 8-bits of data for monochrome STN panels
- Controller supplies one pixel per shift clock with 4-bits of data for 16 shades for plasma panels
- Controller supplies 8-bit (2 and 2/3 pixel per shift clock) interface, and 16-bit (5 and 1/3 pixel per shift clock) interface for color STN panels
- Controller supplies 9-bit, 12-bit 18-bit (all are one pixel per shift clock) interface for TFT panels

4.0 MEMORY CONFIGURATIONS

4.1 MEMORY MODE SETUP

The following table defines how to set up the configuration registers for the desired memory mode. Refer to subsequent paragraphs for descriptions of the memory modes

The memory modes listed in Table 4-1 are selected at power-on or reset depending upon configuration bits CNF16, CNF14, and CNF13. For information about the configuration registers, refer to Section 24.

MODE	MEMORY DRAMS TYPE	MEMORY DRAMS QTY	CNF16 PR11[7]	CNF14 PR11[6]	CNF13 PR11[5]
1	256K by 16	1	1	0	1
2[3]	256K by 16	2	1	0	0

NOTES:
1. With CNF[16] set to 0, display memory uses 256K by 16 DRAMs.
2. CNF(16), CNF(14), and CNF(13) are readable via PR 11 bits 7, 6, and 5, respectively (refer to Section 24).
3. Mode 2 has no frame buffer.

TABLE 4-1. MEMORY MODE SETUP

In memory mode 1 the display memory data path is 16 bits wide.

Memory mode 2 is used with a 32-bit wide display memory data path, unless one of the DRAM banks is used as the LCD panel frame buffer. For example, one DRAM bank is used as the LCD panel frame buffer when simultaneous display with an LCD panel and CRT is used, and also when 16-bit dual-panel color STN is used.

4.2 MEMORY CONFIGURATION DESCRIPTIONS

Memory for the 90C24LC can be configured in two memory modes as listed in Table 4-1. Table 4-2 summarizes how the memory modes support combinations of memory configurations and displays. The following block diagrams are provided show how the external DRAMs are connected in typical memory configurations.

1. Single DRAM Memory Interface Configuration
2. Memory Configuration with 1 Mbyte.
3. Simultaneous Display Memory Configuration
4. High-Performance 512 Kbyte Simultaneous Display Memory Configuration

Table 4-2 lists the memory modes and which of the memory modes supports each display resolution. Where the memory mode is available, the table lists whether it supports CRT only, LCD only, or simultaneous displays (dual panel and CRT).

MEMORY CONFIGURATIONS	MEMORY MODES[1] 1[2]	MEMORY MODES[1] 2[3]
1024 x 768 x 256	---	C,L
1024 x 768 x 16	C,L	C,L
800 x 600 x 256	C	C
800 x 600 x 16	C,L	C,L
640 x 480 x 256	C,L	S,C,L
640 x 480 x 32K/64K	---	C,L
640 x 400 x 256	C,L	S,C,L
640 x 400 x 32K/64K	C,L	C,L
320 x 200 x 32K/64K	C,L	C,L
All IBM Standard Modes	S,C,L	S,C,L
Memory Data Bus Width	16 bits	32 bits

NOTES

S = Simultaneous display (dual panel and CRT)
C = CRT only
L = LCD only

1. These memory modes are also listed in Table 4-1.
2. Supports a 16-bit interface in C and L modes.
3. Supports a 32-bit interface in C and L modes.

TABLE 4-2. MEMORY CONFIGURATIONS AND MODES SUPPORTED

4.3 MEMORY MODE 1 INTERFACE CONFIGURATION

Figure 4-1 shows memory mode No. 1 with 512 Kbytes of display memory using one 256K by 16 DRAM.

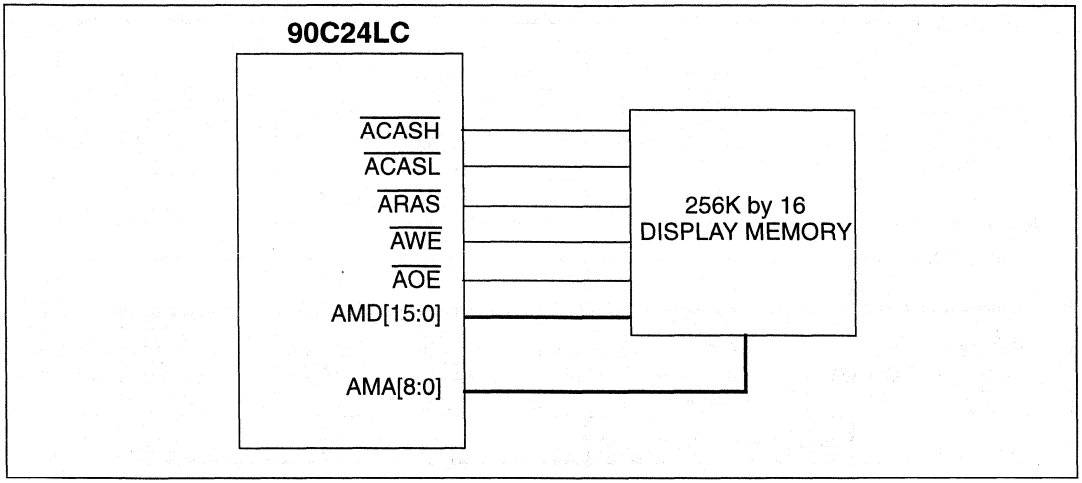


FIGURE 4-1. MEMORY MODE 1 INTERFACE CONFIGURATION

4.4 MEMORY MODE 2 INTERFACE CONFIGURATION

Figure 4-2 shows memory mode No. 2 with 1 Mbyte of display memory using two 256K by 16 DRAMs.

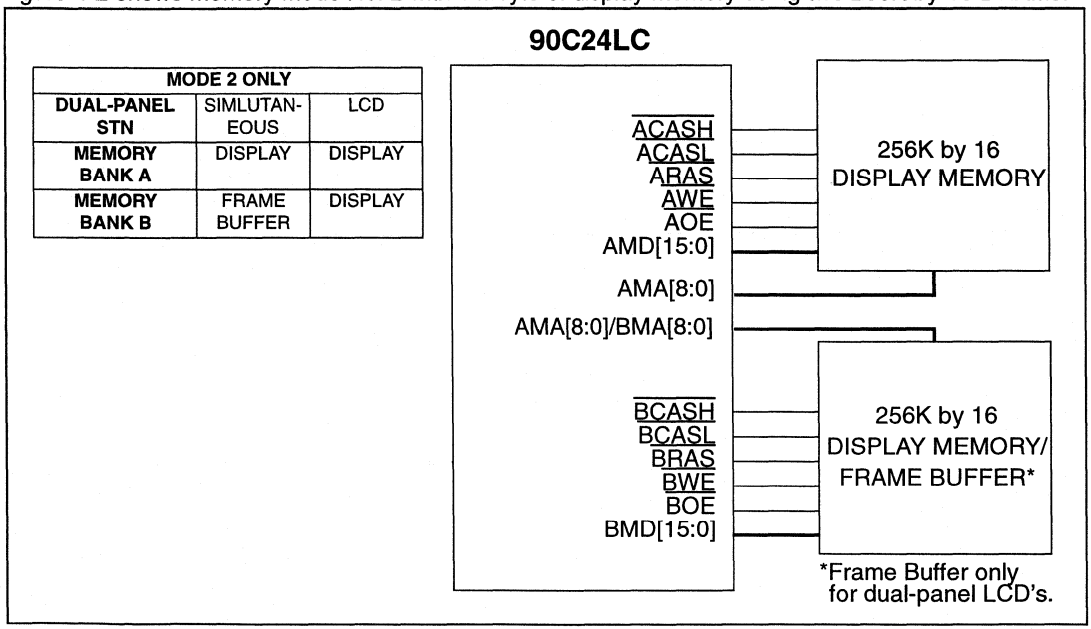


FIGURE 4-2. MEMORY MODE 2 INTERFACE CONFIGURATION USING TWO 256K BY 16 DRAMS

Figure 4-3 shows memory mode No. 2 with 1 Mbyte of display memory using eight 256K by 4 DRAMs.

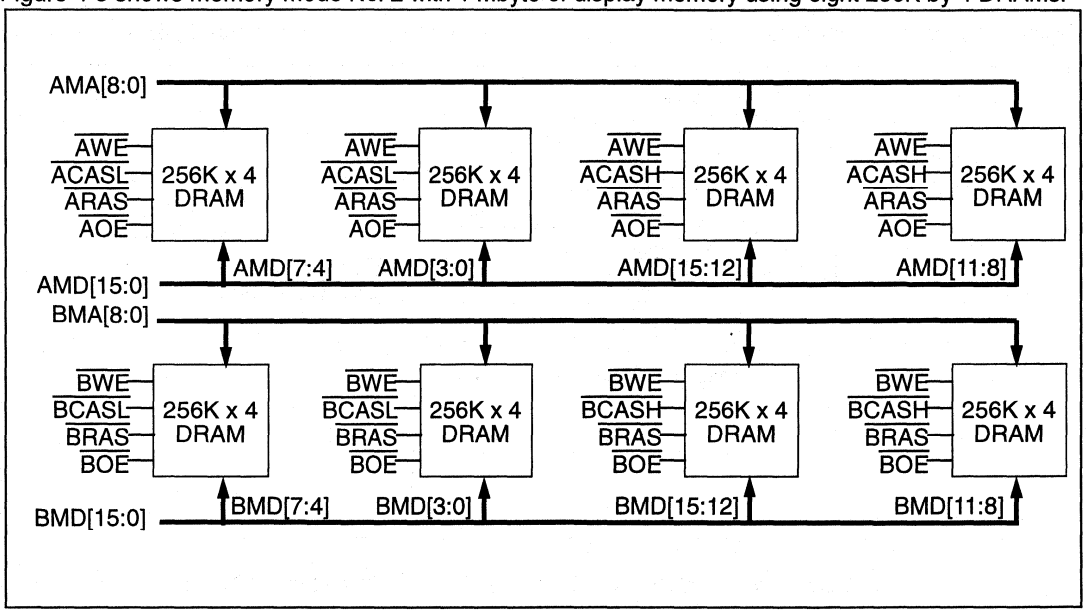


FIGURE 4-3. MEMORY MODE 2 INTERFACE CONFIGURATION USING EIGHT 256K BY 4 DRAMS

5.0 SIGNAL DESCRIPTIONS

5.1 INTRODUCTION

This section contains detailed information concerning signals and connector pins for the 90C24LC controller 208-pin MQFP package. The following information is contained in this section:

- Signal to Pin Location Table
- Signal and Pin Configuration Diagram
- Detailed Signal Descriptions
- Pin Multiplexing Reference Tables

NOTES FOR TABLE 5-1

Where multiple signal names are assigned to a pin, the names are separated by a vertical bar (I). The use for each pin depends on the bus that the pin is connected to. For additional information about the busses refer to Section 5-3. For additional information about pins with multiplexed signals, refer to Section 5.4.

[1] Indicates output only signal names.

[2] Indicates input only signal names.

[3] Indicates VDD and VSS supply pins.

Signal names not otherwise indicated are both input and output.

5.2 SIGNAL MNEMONIC TO PIN LOCATION

PIN - NAME	PIN - NAME	PIN - NAME	PIN - NAME
1 - BMD0	32 - BMA2[1]	63 - SLA17[2]	94 - SA13[2]
2 - BMD15	33 - BMA5[1]	64 - SLA18[2]	95 - SA14[2]
3 - BMD1	34 - BMA3[1]	65 - SLA19[2]	96 - SA15[2]
4 - BMD14	35 - BMA4[1]	66 - SLA20[2]	97 - SA16[2]
5 - VSS[3]	36 - VSS[3]	67 - SLA21[2]	98 - $\overline{IOR}$[2]ID/$\overline{C}$[2]
6 - BMD2	37 - PD29	68 - SLA22[2]	99 - $\overline{IOW}$[2]I$\overline{BE1}$[2]
7 - BMD13	38 - PD28	69 - SLA23[2]	100 - $\overline{MEMR}$[2]IM/$\overline{IO}$[2]
8 - BMD3	39 - PD27	70 - CLK486[2]	101 - $\overline{MEMW}$[2]IW/$\overline{R}$[2]
9 - BMD12	40 - PD26	71 - $\overline{IOCS16}$[1]I$\overline{BOFF}$[1]	102 - AVDD1[3]
10 - VDD[3]	41 - PD25	72 - $\overline{MEMCS16}$[1]IPD31	103 - XMCLK[2]
11 - BMD4	42 - PD24	73 - $\overline{SBHE}$[2]I CPURESET[2]	104 - MCAP[2]
12 - BMD11	43 - VDD[3]	74 - ALE[2]I$\overline{ADS}$[2]	105 - VCAP[2]
13 - BMD5	44 - PD23	75 - IRQ[1]IPD30	106 - VCLK2
14 - BMD10	45 - PD22	76 - $\overline{EIO}$[2]I$\overline{BE0}$[2]	107 - AVSS1[3]
15 - BMD6	46 - PD21	77 - $\overline{IOCHRDY}$[1]I $\overline{CPURDY}$[1]	108 - RVSS[3]
16 - BMD9	47 - PD20	78 - $\overline{ZWST}$[1]IVLBIBUSY	109 - SD0
17 - BMD7	48 - VSS[3]	79 - VSS[3]	110 - SD1
18 - BMD8	49 - PD19	80 - SA0[2]I$\overline{BE3}$[2]	111 - SD2
19 - MVDD[3]	50 - PD18	81 - SA1[2]I$\overline{BE2}$[2]	112 - SD3
20 - $\overline{BCASL}$[1]	51 - PD17	82 - SA2[2]	113 - BVDD[3]
21 - VSS[3]	52 - PD16	83 - SA3[2]	114 - SD4
22 - $\overline{BWE}$[1]	53 - SD15	84 - SA4[2]	115 - SD5
23 - $\overline{BCASH}$[1]	54 - SD14	85 - SA5[2]	116 - SD6
24 - $\overline{BRAS}$[1]	55 - SD13	86 - SA6[2]	117 - SD7
25 - $\overline{BOE}$[1]	56 - SD12	87 - SA7[2]	118 - VSS[3]
26 - VDD[3]	57 - BVDD[3]	88 - RVDD[3]	119 - XSCLK[1]IXSCLKL[1]I XSCLKU[1]IBD5[1]
27 - BMA8	58 - SD11	89 - SA8[2]	120 - $\overline{WPLT}$[1]IBD4[1]
28 - BMA0[1]	59 - SD10	90 - SA9[2]	121 - $\overline{RPLT}$[1]IBD3[1]I STN15[1] IUD7[1]
29 - BMA7[1]	60 - SD9	91 - SA10[2]	122 - STN14[1]IBD2[1]I UD6[1]
30 - BMA1[1]	61 - SD8	92 - SA11[2]	123 - STN13[1]IBD1[1]I IUD5[1]
31 - BMA6[1]	62 - VSS[3]	93 - SA12[2]	124 - STN12[1]IBD0[1]I IUD4[1]

NOTE: Refer to notes preceding this table.

TABLE 5-1. SIGNAL TO PIN LOCATION

PIN - NAME	PIN - NAME	PIN - NAME	PIN - NAME
125 - VDD[3]	146 - SA24[2]	167 - FPUSR0[1]	188 - AMD10
126 - STN11[1]|GD5[1]|UD3[1]	147 - SA25[2]	168 - VCLK1[1]| FPUSR1[1]	189 - AMD6
127 - STN10[1]|GD4[1]|UD2[1]	148 - SA26[2]	169 - PVDD[3]	190 - AMD9
128 - STN9[1]|RD5[1]|UD1[1]	149 - SA27[2]	170 - CKIN[2]|VCLK[2]	191 - AMD7
129 - STN8[1]|RD4[1]|UD0[1]	150 - SA28[2]	171 - $\overline{\text{EBROM}}$[1]| $\overline{\text{REFLCL}}$[2]	192 - AMD8
130 - FPVDD[3]	151 - SA29[2]	172 - $\overline{\text{VLBICS}}$[1]	193 - MVDD[3]
131 - VUD3[1]|D7[1]|RD3[1]|STN7[1]| STN0[1]|LD7[1]|VD7|P7[2]	152 - SA30[2]	173 - VSYNC[1]	194 - $\overline{\text{ACASL}}$[1]
132 - VUD2[1]|D6[1]|RD2[1]|STN6[1]| STN1[1]|LD6[1]|VD6|P6[2]	153 - SA31[2]	174 - HSYNC[1]	195 - VSS[3]
133 - VUD1[1]|D5[1]|RD1[1]|STN5[1]| STN2[1]|LD5[1]|VD5|P5[2]	154 - AVDD2[3]	175 - PCLK	196 - $\overline{\text{AWE}}$[1]
134 - VUD0[1]|D4[1]|RD0[1]| STN4[1]| STN3[1]|LD4[1]| VD4|P4[2]	155 - $\overline{\text{MDETECT}}$[2]|FSADJ[2]	176 - VSS[3]	197 - $\overline{\text{ACASH}}$[1]
135 - VLD3[1]|D3[1]|GD3[1]| STN3[1]| STN4[1]|LD3[1]| VD3|P3[2]	156 - VREF[2] (Analog)	177 - AMD0	198 - $\overline{\text{ARAS}}$[1]
136 - VLD2[1]|D2[1]|GD2[1]| STN2[1]| STN5[1]|LD2[1]| VD2|P2[2]	157 - BLUE[1] (Analog)	178 - AMD15	199 - $\overline{\text{AOE}}$[1]
137 - VLD1[1]|D1[1]|GD1[1]|STN1[1]| STN6[1]|LD1[1]| VD1|P1[2]	158 - GREEN[1] (Analog)	179 - AMD1	200 - AMA8[1]
138 - VLD0[1]| D0[1]|GD0[1]| STN0[1]| STN7[1]|LD0[1]| VD0|P0[2]	159 - RED[1] (Analog)	180 - AMD14	201 - AMA0[1]
139 - VSS[3]	160 - AVSS2[3]	181 - AMD2	202 - AMA7[1]
140 - XSCLK[1]|XSCLKL[1]| XSCLKU[1]	161 - EXCKEN[2]	182 - AMD13	203 - AMA1[1]
141 - RVDD[3]	162 - RESET[2]|SYSRES[2]	183 - AMD3	204 - AMA6[1]
142 - LP[1]	163 - $\overline{\text{PDOWN}}$[2]	184 - AMD12	205 - AMA2[1]
143 - FP[1]	164 - $\overline{\text{LCDENA}}$[1]	185 - AMD4	206 - AMA5[1]
144 - FR[1]|$\overline{\text{BLANK}}$[1]| ENDATA[1]	165 - PNLOFF[1]	186 - AMD11	207 - AMA3[1]
145 - RVSS[3]	166 - $\overline{\text{REFRESH}}$[2]| $\overline{\text{RDYIN}}$[2]	187 - AMD5	208 - AMA4[1]

NOTE: Refer to notes preceding this table.

TABLE 5-1 SIGNAL TO PIN LOCATIONS (Continued)

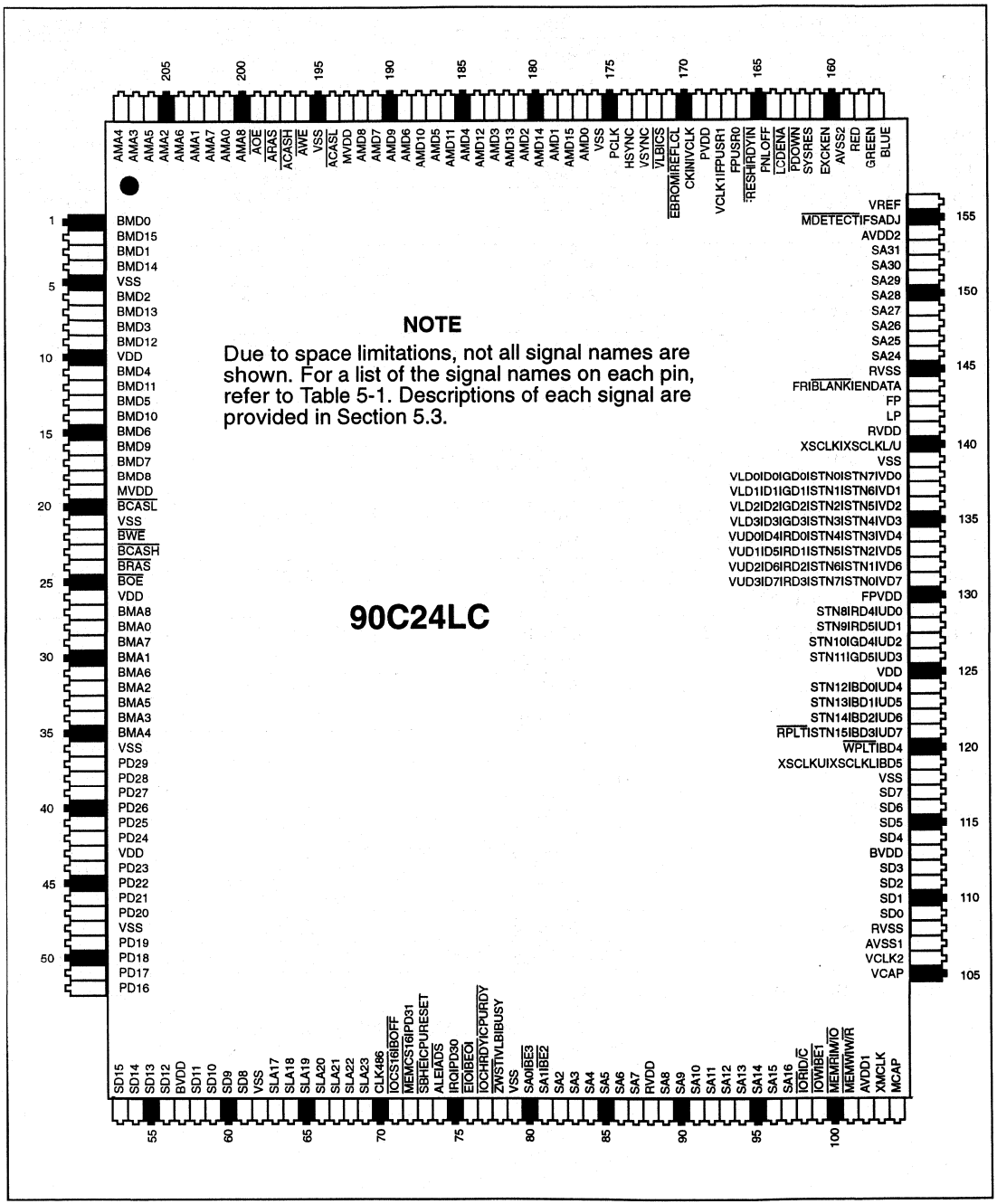


FIGURE 5-1. PIN CONFIGURATION

For more information contact your nearest Philips Components national organization.

PHILIPS

Desktop video module system B/G

FI1216 MK2

INTRODUCTION

The FI1216 MK2 is developed to receive off air, S-cable and hyberband TV channels for system B/G.

FEATURES

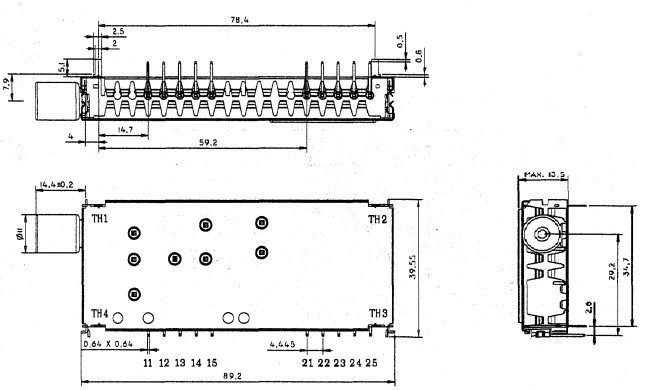
1. True 5V device (low power dissipation)
2. Full TV frequency range from channel 2 (48.25 MHz) to channel 69 (855.25 MHz)
3. True-synchronous vision IF demodulator (PLL)
4. Demodulated video output and AF sound output
5. I^2C-bus control of PLL tuning, address selection, AFC status information
6. Complies with CENELEC EN55020, EN55013
7. Small horizontally mounted metal housing
8. Second IF sound output for NICAM and 2 carrier stereo systems
9. Built-in 5V to 33V DC/DC converter for varicap voltage

ORDERING INFORMATION

TYPE	DESCRIPTION	CATALOGUE NUMBERS
FI1216 MK2/PH hm	Standard Phono	3139 147 13291
FI1216 MK2/I hm	IEC	3139 147 13301

PINNING

TERMINAL		DESCRIPTION
11	V_T	Tuning voltage (monitor)
12	V_S	Supply voltage tuner section +5V
13	SCL	I^2C-bus serial clock
14	SDA	I^2C-bus serial data
15	AS	I^2C-bus address select
21	-	Not Connected
22	2^{ND} IF O/P	Second IF sound output
23	CVBS	Composite video baseband signal (CVBS) output
24	V_{IF}	Supply voltage IF section +5V
25	AF O/P	AF sound output
TH1, TH2, TH3 and TH4	-	Mounting Tags (ground)



SPECIFICATION

TV Standard		B, G
Frequency Range	Low	48.25 to 170.00 MHz
	Mid	170.00 to 450.00 MHz
	High	450.00 to 855.25 MHz
Intermediate Frequency (IF)		PC CC SC1 SC2 NICAM 38.90 34.47 33.40 33.16 33.05 MHz
Input Connectors		IEC female or Standard Phono, 75 Ohm unbalanced
CVBS S/N ratio (unweighted)		45 dB typ.
Audio S/N ratio (CCIR weighted)		46 dB typ.
CVBS output		0.9V typ.
DC sync level		0.35V typ.
Supply voltage		5V

Desktop video module system L/L' and B/G

FI1216MF MK2

INTRODUCTION

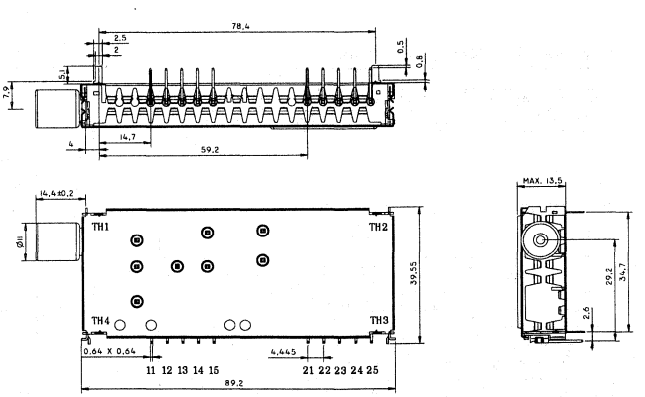
The FI1216MF MK2 multi-standard frontend is developed to receive off air, S-cable and hyberband TV channels for systems L/L' and B/G.

FEATURES

1. Full frequency range from channel 2 (48.25 MHz) to channel 69 (855.25 MHz)
2. True-synchronous vision IF demodulator (PLL)
3. Demodulated video output and AF sound output
4. I^2C-bus control of PLL tuning, address selection, AFC status information
5. Complies with CENELEC EN55020, EN55013
6. Small horizontally mounted metal housing
7. Software Selection between positive and negative modulation
8. Second IF sound output for NICAM and 2 carrier stereo systems
9. Built-in 5V to 33V DC/DC converter for varicap voltage

ORDERING INFORMATION

TYPE	DESCRIPTION	CATALOGUE NUMBERS
FI1216MF MK2/PH hm	Standard Phono	3139 147 13571
FI1216MF MK2/I hm	IEC	3139 147 13581



PINNING

TERMINAL		DESCRIPTION
11	V_T	Tuning voltage (monitor)
12	V_S	Supply voltage tuner section +5V
13	SCL	I^2C-bus serial clock
14	SDA	I^2C-bus serial data
15	AS	I^2C-bus address select
21	-	Not Connected
22	2^{ND} IF O/P	Second IF sound output
23	CVBS	Composite video baseband signal (CVBS) output
24	V_{IF}	Supply voltage IF section +5V
25	AF O/P	AF sound output
TH1, TH2, TH3 and TH4	-	Mounting Tags (ground)

SPECIFICATION

TV Standard		L, L', B/G			
Frequency Range	Low	48.25 to 170.00 MHz			
	Mid	170.00 to 450.00 MHz			
	High	450.00 to 855.25 MHz			
Intermediate Frequency (IF)		L	L'	B/G	
	Picture	38.90	33.95	38.90	MHz
	Colour	34.47	38.38	34.47	MHz
	Sound 1	32.40	40.45	33.40	MHz
	Sound 2	-	-	33.16	MHz
	NICAM	33.05	39.80	33.05	MHz
Input Connectors		IEC female or Standard Phono, 75 Ohm unbalanced			
CVBS S/N ratio (unweighted)		45 dB typ.			
Audio S/N ratio (CCIR weighted)		46 dB typ.			
CVBS output		0.9V typ.			
DC sync level		0.35V typ.			
Supply voltage		5V			

Desktop video module system M/N

FI1236 MK2

INTRODUCTION

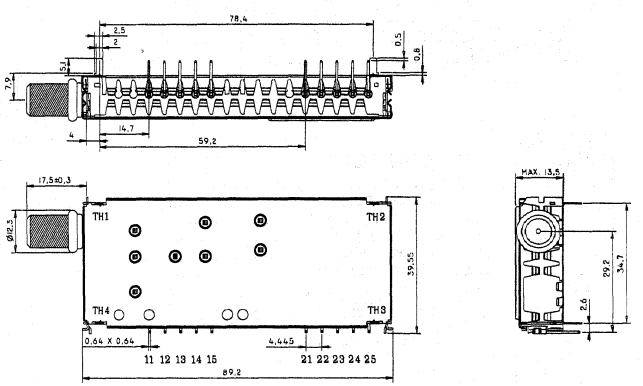
The FI1236 MK2 is developed to receive off air and cable TV channels for systems M and N.

FEATURES

1. True 5V device (low power dissipation)
2. Full TV frequency range from channel 2 (55.25 MHz) to channel 69 (801.25 MHz)
3. True-synchronous vision IF demodulator (PLL)
4. Demodulated video output and AF sound output
5. I^2C-bus control of PLL tuning, address selection, AFC status information
6. Complies with FCC and DOC regulations
7. Small horizontally mounted metal housing
8. Second IF sound output for 2 carrier stereo system (Korea)
9. Wide bandwidth AF output for MTS
10. Built-in 5V to 33V DC/DC converter for varicap voltage

ORDERING INFORMATION

TYPE	DESCRIPTION	CATALOGUE NUMBERS
FI1236 MK2/PH hm	Standard Phono	3139 147 13250
FI1236 MK2/F hm	F	3139 147 13260



PINNING

TERMINAL		DESCRIPTION
11	V_T	Tuning voltage (monitor)
12	V_S	Supply voltage tuner section +5V
13	SCL	I^2C-bus serial clock
14	SDA	I^2C-bus serial data
15	AS	I^2C-bus address select
21	-	Not Connected
22	2^{ND} IF O/P	Second IF sound output
23	CVBS	Composite video baseband signal (CVBS) output
24	V_{IF}	Supply voltage IF section +5V
25	AF O/P	AF sound output
TH1, TH2, TH3 and TH4	-	Mounting Tags (ground)

SPECIFICATION

TV Standard		M, N
Frequency Range	Low	55.25 to 160.00 MHz
	Mid	160.00 to 450.00 MHz
	High	450.00 to 801.25 MHz
Intermediate Frequency (IF)		PC CC SC 45.75 42.17 41.25 MHz
Input Connectors		F female or Standard Phono, 75 Ohm unbalanced
CVBS S/N ratio (unweighted)		45 dB typ.
Audio S/N ratio (CCIR weighted)		46 dB typ.
CVBS output		0.9V typ.
DC sync level		0.35V typ.
Supply voltage		5V

For more information contact your nearest Philips Components national organization.

PHILIPS

Desktop video module system I

FI1246 MK2

INTRODUCTION

The FI1246 MK2 is developed to receive off air and cable TV channels for system I.

FEATURES

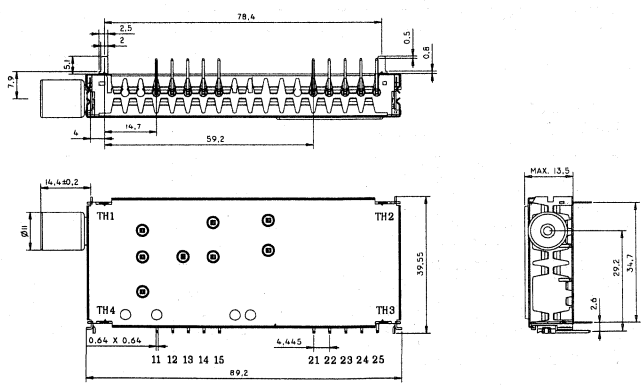
1. Full frequency range from channel A (45.25 MHz) to channel E69 (855.25 MHz)
2. True-synchronous vision IF demodulator (PLL)
3. Demodulated video output and AF sound output
4. I^2C-bus control of PLL tuning, address selection, AFC status information
5. Complies with CENELEC EN55020, EN55013
6. Small horizontally mounted metal housing
7. Second IF sound output for NICAM only
8. Built-in 5V to 33V DC/DC converter for varicap voltage

ORDERING INFORMATION

TYPE	DESCRIPTION	CATALOGUE NUMBERS
FI1246 MK2/PH hm	Standard Phono	3139 147 13721
FI1246 MK2/I hm	IEC	3139 147 13731

PINNING

TERMINAL		DESCRIPTION
11	V_T	Tuning voltage (monitor)
12	V_S	Supply voltage tuner section +5V
13	SCL	I^2C-bus serial clock
14	SDA	I^2C-bus serial data
15	AS	I^2C-bus address select
21	-	Not Connected
22	2ND IF O/P	Second IF sound output
23	CVBS	Composite video baseband signal (CVBS) output
24	V_{IF}	Supply voltage IF section +5V
25	AF O/P	AF sound output
TH1, TH2, TH3 and TH4	-	Mounting Tags (ground)



SPECIFICATION

TV Standard		I
Frequency Range	Low Mid High	48.25 to 170.00 MHz 170.00 to 450.00 MHz 450.00 to 855.25 MHz
Intermediate Frequency (IF)		PC CC SC NICAM 38.90 34.47 32.90 32.35 MHz
Input Connectors		IEC female or Standard Phono, 75 Ohm unbalanced
CVBS S/N ratio (unweighted)		45 dB typ.
Audio S/N ratio (CCIR weighted)		46 dB typ.
CVBS output		0.9V typ.
DC sync level		0.35V typ.
Supply Voltage		5V

For more information contact your nearest Philips Components national organization.

PHILIPS

Desktop video module system D/K

FI1256 MK2

INTRODUCTION

The FM1256 MK2 is developed to receive off air and cable TV channels for system D/K.

FEATURES

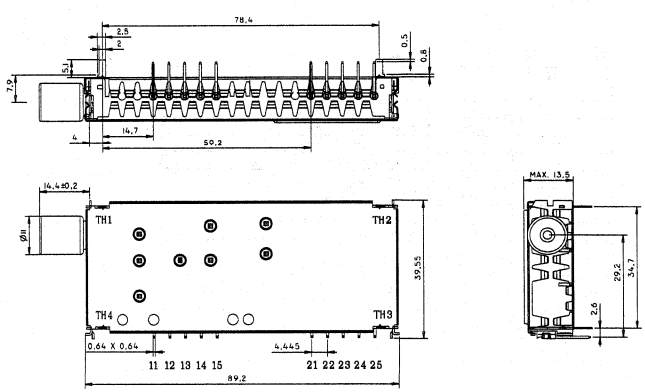
1. Full frequency range from 48.25 MHz to channel 863.25 MHz
2. True-synchronous vision IF demodulator (PLL)
3. Demodulated video output and AF sound output
4. I^2C-bus control of PLL tuning, address selection, AFC status information
5. Complies with CISPR 13 and CENELEC EN55020, EN55013
6. Small horizontally mounted metal housing
7. Second IF sound output for 2 carrier stereo system
8. Built-in 5V to 33V DC/DC converter for varicap voltage

ORDERING INFORMATION

TYPE	DESCRIPTION	CATALOGUE NUMBERS
FI1256 MK2/PH hm	Standard Phono	3139 147 13741
FI1256 MK2/I hm	IEC	3139 147 13751

PINNING

TERMINAL		DESCRIPTION
11	V_T	Tuning voltage (monitor)
12	V_S	Supply voltage tuner section +5V
13	SCL	I^2C-bus serial clock
14	SDA	I^2C-bus serial data
15	AS	I^2C-bus address select
21	-	Not Connected
22	2ND IF O/P	Second IF sound output
23	CVBS	Composite video baseband signal (CVBS) output
24	V_{IF}	Supply voltage IF section +5V
25	AF O/P	AF sound output
TH1, TH2, TH3 and TH4	-	Mounting Tags (ground)



SPECIFICATION

TV Standard	D, K
Frequency Range Low Mid High	48.25 to 170.00 MHz 170.00 to 450.00 MHz 450.00 to 863.25 MHz
Intermediate Frequency (IF)	PC CC SC1 SC2 38.90 34.47 32.40 32.16 MHz
Input Connectors	IEC female or Standard Phono, 75 Ohm unbalanced
CVBS S/N ratio (unweighted)	45 dB typ.
Audio S/N ratio (CCIR weighted)	46 dB typ.
CVBS output	0.9V typ.
DC sync level	0.35V typ.
Supply voltage	5V

For more information contact your nearest Philips Components national organization.

PHILIPS

Desktop video & radio module system B/G

FR1216

INTRODUCTION

The FR1216 is developed to receive off air, S-cable and hyberband TV channels for system B/G and FM radio.

FEATURES

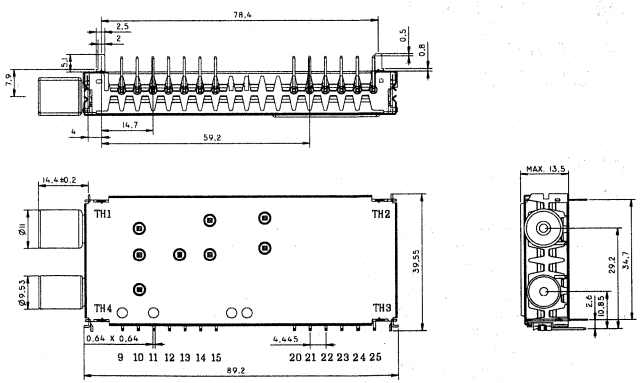
1. True 5V device (low power dissipation)
2. Full TV frequency range from channel 2 (48.25 MHz) to channel 69 (855.25 MHz)
3. FM band coverage from 87.5 to 108 MHz
4. Separate TV and FM antenna inputs
5. True-synchronous vision IF demodulator (PLL)
6. Demodulated video output and AF sound output
7. 10.7 MHz IF for external FM demodulation circuit
8. I^2C-bus control of PLL tuning, address selection, AFC status information
9. Complies with CISPR 13 and CENELEC EN55020, EN55013
10. Small horizontally mounted metal housing
11. Second IF sound output for NICAM and 2 carrier stereo systems
12. Built-in 5V to 33V DC/DC converter for varicap voltage

ORDERING INFORMATION

TYPE	DESCRIPTION	CATALOGUE NUMBERS
FR1216/PH hm	Standard Phono	3139 147 13351
FR1216/I hm	IEC	3139 147 13361

PINNING

TERMINAL		DESCRIPTION
9	AGC	Automatic gain control voltage
10	ADC	Analog-to-digital converter input
11	V_T	Tuning voltage (monitor)
12	V_S	Supply voltage tuner section +5V
13	SCL	I^2C-bus serial clock
14	SDA	I^2C-bus serial data
15	AS	I^2C-bus address select
20	P3	System switch
21	FM-IF	10.70 MHz output
22	2^{ND} IF O/P	Second IF sound output
23	CVBS	Composite video baseband signal (CVBS) output
24	V_{IF}	Supply voltage IF section +5V
25	AF O/P	AF sound output
TH1, TH2, TH3 and TH4	-	Mounting Tags (ground)



SPECIFICATION

TV Standard		B, G
Frequency Range	FM Radio	87.50 to 108 MHz
	TV Low Band	48.25 to 170.00 MHz
	Mid Band	170.00 to 450.00 MHz
	High Band	450.00 to 855.25 MHz
Intermediate Frequency (IF)		PC CC SC1 SC2 NICAM
	TV	38.90 34.47 33.40 33.10 33.05 MHz
	FM radio	10.7 MHz
Input Connectors		IEC female and IEC male or 2x Standard Phono, 75 Ohm unbalanced
CVBS S/N ratio (unweighted)		45 dB typ.
Audio S/N ratio (CCIR weighted)		46 dB typ.
CVBS output		0.9V typ.
DC sync level		0.35V typ.
FM radio gain		35 dB typ.
Supply voltage		5V

Desktop video & radio module system M/N

FR1236

INTRODUCTION

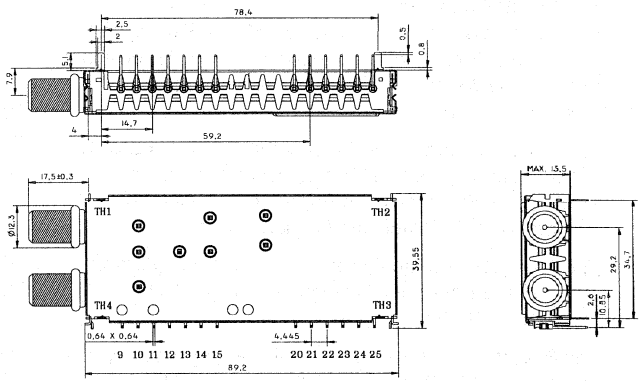
The FR1236 is developed to receive off air and cable TV channels for systems M and N, and FM radio.

FEATURES

1. True 5V device (low power dissipation)
2. Full TV frequency range from channel 2 (55.25 MHz) to channel 69 (801.25 MHz)
3. FM band coverage from 87.5 to 108 MHz
4. Separate TV and FM antenna inputs
5. True-synchronous vision IF demodulator (PLL)
6. Demodulated video output and AF sound output
7. 10.7 MHz IF for external FM demodulation circuit
8. I^2C-bus control of PLL tuning, address selection, AFC status information
9. Complies with FCC and DOC regulations
10. Small horizontally mounted metal housing
11. Second IF sound output for 2 carrier stereo system (Korea)
12. Wide bandwidth AF output for MTS
13. Built-in 5V to 33V DC/DC converter for varicap voltage

ORDERING INFORMATION

TYPE	DESCRIPTION	CATALOGUE NUMBERS
FR1236/PH hm	Standard Phono	3139 147 13391
FR1236/F hm	F	3139 147 13401



PINNING

TERMINAL		DESCRIPTION
9	AGC	Automatic gain control voltage
10	ADC	Analog-to-digital converter input
11	V_T	Tuning voltage (monitor)
12	V_S	Supply voltage tuner section +5V
13	SCL	I^2C-bus serial clock
14	SDA	I^2C-bus serial data
15	AS	I^2C-bus address select
20	P3	System switch
21	FM-IF	10.70 MHz output
22	2ND IF O/P	Second IF sound output
23	CVBS	Composite video baseband signal (CVBS) output
24	V_{IF}	Supply voltage IF section +5V
25	AF O/P	AF sound output
TH1, TH2, TH3 and TH4	-	Mounting Tags (ground)

SPECIFICATION

TV Standard		M, N
Frequency Range	FM Radio	87.50 to 108 MHz
	TV Low Band	55.25 to 160.00 MHz
	Mid Band	160.00 to 454.00 MHz
	High Band	454.00 to 801.25 MHz
Intermediate Frequency (IF)		PC CC SC
	TV	45.75 42.17 41.25 MHz
	FM radio	10.7 MHz
Input Connectors		2x F female or 2x Standard Phono, 75 Ohm unbalanced
CVBS S/N ratio (unweighted)		45 dB typ.
Audio S/N ratio (CCIR weighted)		46 dB typ.
CVBS output		0.9V typ.
DC sync level		0.35V typ.
FM radio gain		35 dB typ.
Supply voltage		5V

Desktop video & radio module system CCIR I

FR1246

FEATURES

- System CCIR I and FM radio broadcast
- True 5 V device (low power dissipation)
- Full TV frequency range from channel A (45.75 MHz) to channel 69 (855.25 MHz)
- FM band coverage from 87.5 to 108 MHz
- PLL controlled tuning
- True-synchronous vision IF demodulator (PLL)
- Demodulated video output, AF sound output, second sound IF output
- 10.70 MHz IF for external FM demodulation circuit
- I²C-bus control of tuning, address selection, AFC status information
- Complies with European regulations on radiation, signal handling and immunity *("CENELEC 55020, 55013")*
- Small horizontally mounted metal housing.

DESCRIPTION

The FR1246 desktop TV/radio RF module is a combination of an FM radio, a TV VHF/UHF tuner and an IF demodulator in one small size metal case. It is designed to meet a wide range of RF applications in the PC Multi-Media environment.

The FR1246 has two 75 Ω inputs for both TV and audio FM broadcast reception. The input connectors are available in either standard Phono (female/female sockets) or IEC (female for TV/male for FM).

The tuning, bandswitching and input switching (both for TV and FM) are performed through the built-in digitally controlled I²C-bus.

The PLL tuning system used enables tuning with step-size programmable between 31.25, 50.0 or 62.5 kHz. A DC-DC converter is built around the PLL synthesizer IC to provide the tuning voltage, thus making the FR1246 video & radio module a true 5 V device.

The FR1246 type offers a 10.70 MHz FM-IF output which can be connected to an external FM demodulation circuit. The automatic gain control (AGC) and analog-to-digital converter (ADC) functions are also made accessible via the pins in the FR1246 for external control of the overall gain and tuning in the FM mode.

The FR1246 meets the input immunity, signal handling and radiation requirements of *"CENELEC EN55020, EN55013"*.

ORDERING INFORMATION

TYPE	DESCRIPTION	CATALOGUE NUMBERS
FR1246/HM/PH	standard phono	3139 147 13761
FR1246/HM/IEC	IEC	3139 147 13771

MARKING

The following items of information are printed on a sticker that is on the top cover of the tuner:

- Type number
- Code number
- Origin letter of factory
- Change code
- Year and week code.

INTERMEDIATE FREQUENCIES

SYSTEM	FREQUENCY(1) (MHz)
	PAL I
Picture carrier	38.90
Colour	34.47
Sound	32.90
NICAM	32.348

Note

1. The oscillator frequency is above the input signal frequency.

CHANNEL COVERAGE

BAND	CHANNELS
FM band	87.50 to 108 MHz
Low band	45.75 to 170.00 MHz
Mid band	170.00 to 450.00 MHz
High band	450.00 to 855.25 MHz

For more information contact your nearest Philips Components national organization

Desktop video & radio module system CCIR I

FR1246

BLOCK DIAGRAM

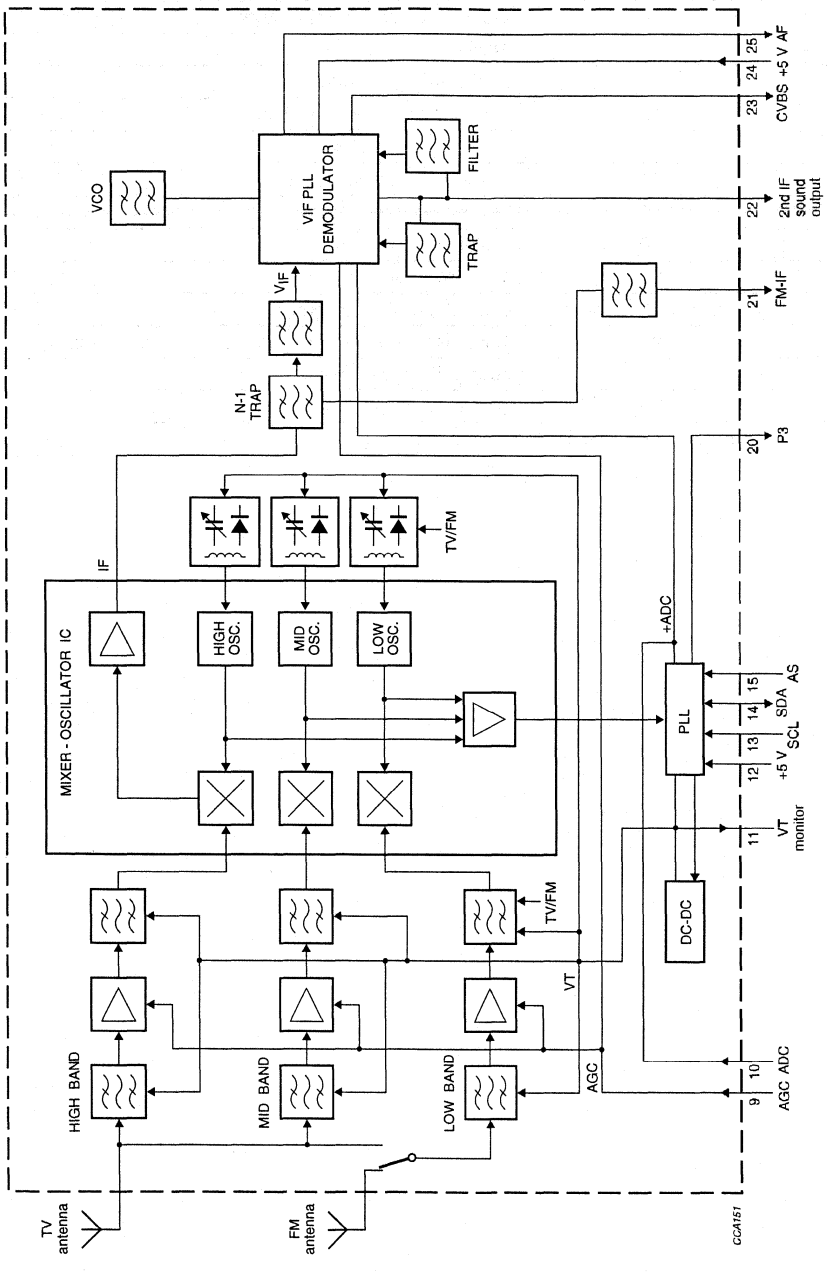
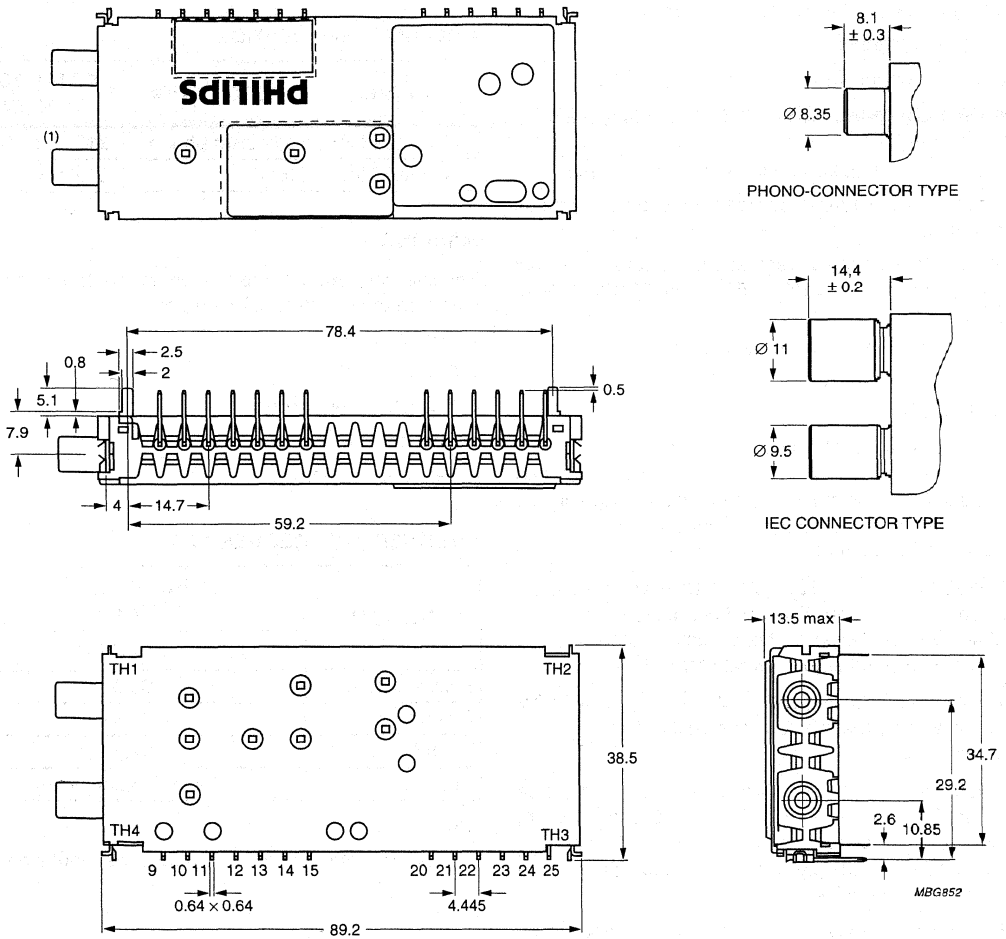


Fig.1 Electrical block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
AGC	9	automatic gain control voltage
ADC	10	analog-to-digital converter input
V_T	11	tuning voltage (monitor)
$V_{S(tuner)}$	12	supply voltage tuner section +5 V
SCL	13	I²C-bus serial clock
SDA	14	I²C-bus serial data
AS	15	I²C-bus address select
P3	20	system switch
FM-IF	21	10.70 MHz output
2nd IF O/P	22	second IF sound output
CVBS	23	Composite Video Baseband Signal (CVBS) output
$V_{S(IF)}$	24	supply voltage IF section +5 V
AF O/P	25	AF sound output
–	TH1, TH2, TH3 and TH4	mounting tags (ground)

MECHANICAL DATA



Dimensions in mm.

(1) Standard-phono socket female 75 Ω.

Fig.2 Mechanical outline.

Desktop video & radio module system CCIR D/K

FR1256

FEATURES

- System CCIR D/K and FM radio broadcast
- True 5 V device (low power dissipation)
- Full TV frequency range from channel 1(49.75 MHz) to channel 57 (863.25 MHz)
- FM band coverage from 87.5 to 108 MHz
- PLL controlled tuning
- True-synchronous vision IF demodulator (PLL)
- Demodulated video output, AF sound output, second sound IF output
- 10.70 MHz IF for external FM demodulation circuit
- I²C-bus control of tuning, address selection, AFC status information
- Complies with European regulations on radiation, signal handling and immunity *("CENELEC 55020, 55013"* and *"CISPR 13")*
- Small horizontally mounted metal housing.

DESCRIPTION

The FR1256 desktop TV/radio RF module is a combination of an FM radio, a TV VHF/UHF tuner and an IF demodulator in one small size metal case. It is designed to meet a wide range of RF applications in the PC Multi-Media environment.

The FR1256 has two 75 Ω inputs for both TV and audio FM broadcast reception. The input connectors are available in either standard Phono (female/female sockets) or IEC (female for TV/male for FM).

The tuning, bandswitching and input switching (both for TV and FM) are performed through the built-in digitally controlled I²C-bus.

The PLL tuning system used enables tuning with step-size programmable between 31.25, 50.0 or 62.5 kHz. A DC-DC converter is built around the PLL synthesizer IC to provide the tuning voltage, thus making the FR1256 video & radio module a true 5 V device.

The FR1256 type offers a 10.70 MHz FM-IF output which can be connected to an external FM demodulation circuit. The automatic gain control (AGC) and analog-to-digital converter (ADC) functions are also made accessible via the pins in the FR1256 for external control of the overall gain and tuning in the FM mode.

The FR1256 meets the input immunity, signal handling and radiation requirements of *"CENELEC EN55020, EN55013"* and *"CISPR 13"*.

ORDERING INFORMATION

TYPE	DESCRIPTION	CATALOGUE NUMBERS
FR1256/HM/PH	standard phono	3139 147 13781
FR1256/HM/IEC	IEC	3139 147 13791

MARKING

The following items of information are printed on a sticker that is on the top cover of the tuner:

- Type number
- Code number
- Origin letter of factory
- Change code
- Year and week code.

INTERMEDIATE FREQUENCIES

SYSTEM	FREQUENCY(1) (MHz)
	PAL D/K
Picture carrier	38.90
Colour	34.47
Sound 1	32.40
Sound 2	32.16 (if applicable)

Note

1. The oscillator frequency is above the input signal frequency.

CHANNEL COVERAGE

BAND	CHANNELS
FM band	87.50 to 108 MHz
Low band	49.75 to 170.00 MHz
Mid band	170.00 to 450.00 MHz
High band	450.00 to 863.25 MHz

For more information contact your nearest Philips Components national organization.

Desktop video & radio module system CCIR D/K

FR1256

BLOCK DIAGRAM

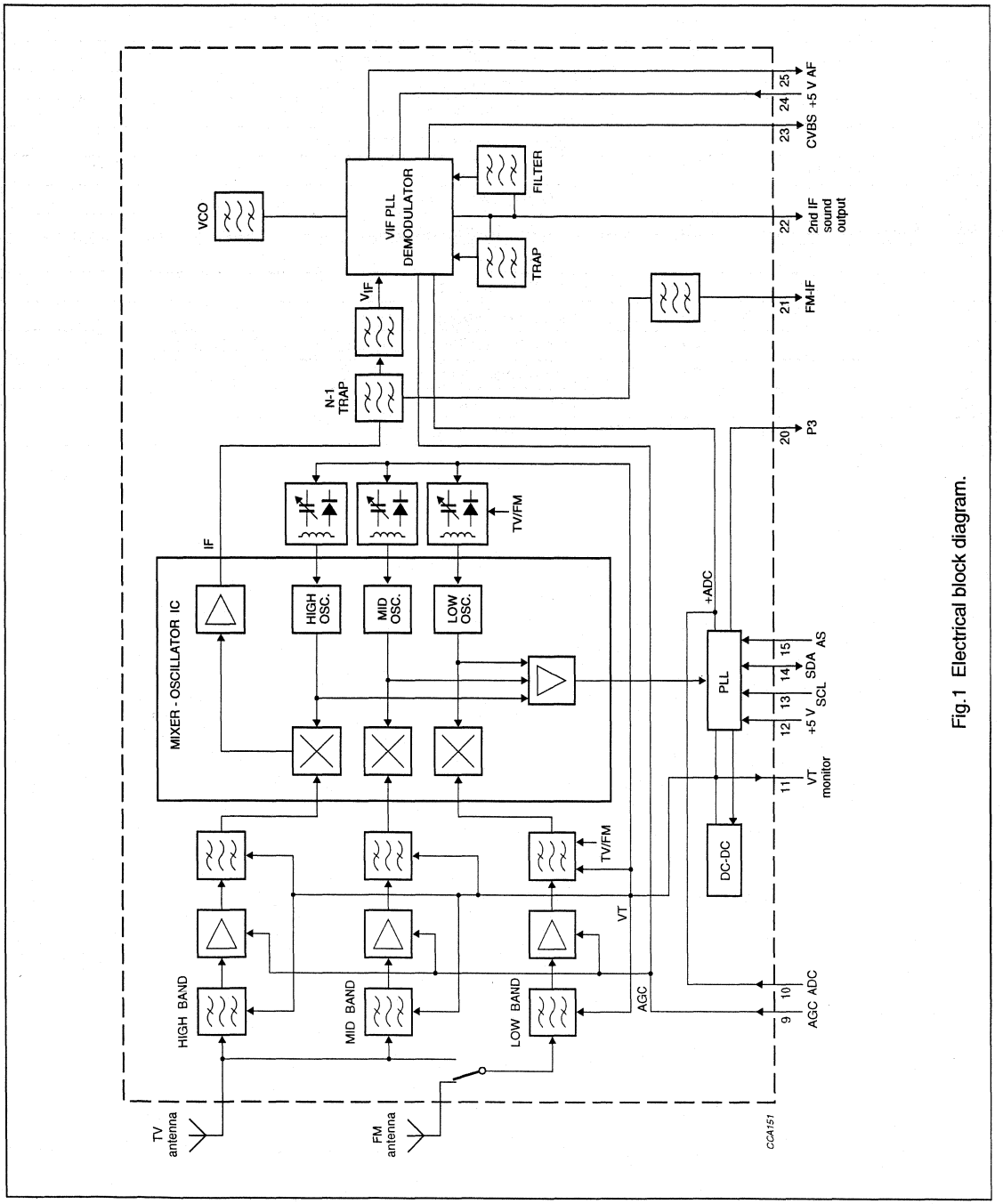


Fig.1 Electrical block diagram.

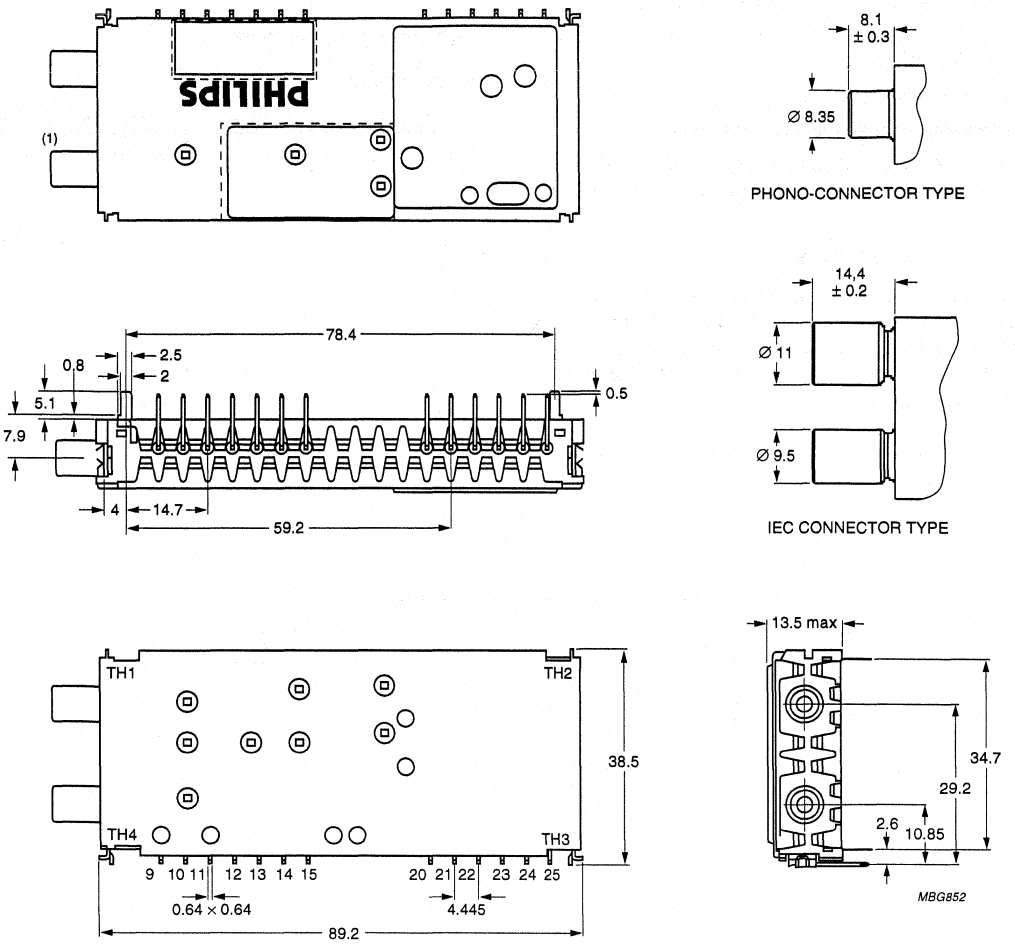
PINNING

SYMBOL	PIN	DESCRIPTION
AGC	9	automatic gain control voltage
ADC	10	analog-to-digital converter input
V_T	11	tuning voltage (monitor)
$V_{S(tuner)}$	12	supply voltage tuner section +5 V
SCL	13	I^2C-bus serial clock
SDA	14	I^2C-bus serial data
AS	15	I^2C-bus address select
P3	20	system switch
FM-IF	21	10.70 MHz output
2^{nd} IF O/P	22	second IF sound output
CVBS	23	Composite Video Baseband Signal (CVBS) output
$V_{S(IF)}$	24	supply voltage IF section +5 V
AF O/P	25	AF sound output
–	TH1, TH2, TH3 and TH4	mounting tags (ground)

Desktop video & radio module system CCIR D/K

FR1256

MECHANICAL DATA



Dimensions in mm.

(1) Standard-phono socket female 75 Ω.

Fig.2 Mechanical outline.

Multimedia radio tuner OM5604; OM5606

FEATURES

- Local/DX switching to improve large signal handling on FM when an outdoor antenna or cable network is connected
- Local/DX function provides different search levels which are useful for spectrum analyser functions
- Three extra I/O expander ports are available for general purpose (I^2C-bus only)
- RDS-MPX signal available
- The module meets the *"FCC regulations"*
- The OM5604; OM5606 is in accordance with *"CENELEC EN55022"* and *"CENELEC EN50082-1"*.

GENERAL DESCRIPTION

The OM5604; OM5606 is an FM-radio tuner which includes a brand new concept in tuning techniques. The new tuning concept combines the advantages of hand tuning together with electronic facilities and features. The tuner is I^2C-bus controlled.

ANTENNA CONNECTOR

RF connector

- OM5604: F-connector (FM input impedance = 75 Ω)
- OM5606: IEC-connector (FM input impedance = 75 Ω).

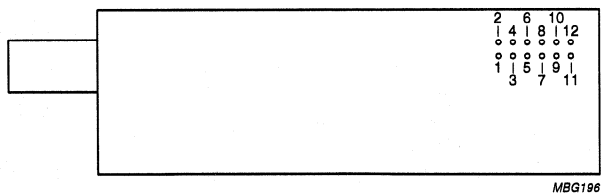


Fig.1 OM5604; OM5606 connector.

ORDERING INFORMATION

UNIT	FREQUENCY (MHz)	BUS	RF CONNECTOR
FM I^2C-bus	87.5 to 108	I^2C-bus	F-connector for OM5604
			IEC-connector for OM5606

PINNING

PIN	DESCRIPTION
1	port 5 PCF8574A (I²C-bus)
2	port 6 PCF8574A (I²C-bus)
3	port 7 PCF8574A (I²C-bus)
4	serial clock input[1]
5	stereo indicator
6	serial data input/output[1]
7	supply voltage (+5 V)
8	supply voltage (+12 V)
9	audio right output
10	ground
11	audio left output
12	MPX signal for RDS demodulation

Note

1. See *"The I²C-bus and how to use it"* (ordering number 9398 393 40011).

INTERFACE

- Digital driving: I²C-bus
- Audio output: typical 900 mV RMS (load 600 Ω) for FM Δf = 75 kHz
- Supply: 5 V ±10% current ≤30 mA and 12 V ±1%, ripple ≤1 V, current ≤2 mA
- RDS-MPX: DC coupled (load ≥39 kΩ), amplitude typical 150 mV (Δf = 75 kHz)
- RF input connector (75 Ω)
- 12 pin connector.

LIMITING VALUES

IEC publication 68-1; full specification; EMC behaviour: the module is designed to be FCC friendly (part 15).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
T	temperature		15	35	°C
RH	relative humidity		25	85	%
T_{amb}	operating ambient temperature	functional operation	−10	+60	°C
T_{stg}	storage temperature		−20	+70	°C
$V_{esd(pc)}$	electrostatic handling for pin connector	note 1	−	2	kV
		note 2	−	300	V
$V_{esd(RFc)}$	electrostatic handling for RF-connector	note 3	−	4	kV
		note 4	−	500	V

Notes

1. Class B: human body model (1.5 kΩ, 100 pF).
2. Class B: charge device model (0 Ω, 200 pF).
3. Class A: human body model (1.5 kΩ, 100 pF).
4. Class A: charge device model (0 Ω, 200 pF).

CHARACTERISTICS

Direct coaxial feed to 75 Ω RF-connector; signal generator impedance = 75 Ω; RF levels are EMF/2; Δf = 75 kHz; f_i = 98 MHz; f_{mod} = 1 kHz; left and right audio output; R_L = 600 Ω; audio filter = 22 Hz to 15 kHz; temperature range = 15 to 35 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FM mono						
Φ_{lim}	3 dB limiting sensitivity	$V_{11, 12}$ = –3 dB; $V_{11, 12}$ = 0 dB at V_{FMi} > 100 µV	–	3.5	5	µV
Φ_{RF}	RF sensitivity	(S + N)/N = 26 dB	–	2.2	4	µV
S/N	signal-to-noise ratio	V_{FMi} = 1 mV	–	71	–	dB
f_L	lower audio frequency bandwidth limit	measured lower limit (–3 dB); f_{ref} = 1 kHz; measured with pre-emphasis	–	40	70	Hz
f_H	upper audio frequency bandwidth limit	measured upper limit (–3 dB); f_{ref} = 1 kHz; measured with pre-emphasis	12.5	14	–	kHz
α_{AM}	AM suppression	AM modulation m = 30%; f_{AF} = 1 kHz	40	58	–	dB
THD	total harmonic distortion		–	1.5	3	%
V_{FMi}	search sensitivity	search stop bits 17 and 16 = 0	–	12	36	µV
V_{FMi}	large signal handling	DX mode; measured distortion = 10%	–	1000	–	mV
att_{RF}	RF attenuation in local mode		15	20	30	dB
V_{FM}	audio output voltage level	V_{FMi} = 1 mV; Δf = 75 kHz; f_{AF} = 400 Hz	700	850	–	mV
FM stereo						
S/N	signal-to-noise ratio	V_{FMi} = 1 mV	60	63	–	dB
α_{cs}	channel separation	f_{AF} = 1 kHz; V_{FMi} = 1 mV	22	28	–	dB
$\lvert\Delta I_O\rvert$	channel imbalance	f_{AF} = 1 kHz; V_{FMi} = 1 mV	–	0.5	3	dB
α_{19}	carrier and harmonic suppression		25	26	–	dB
α_{38}	carrier and harmonic suppression		25	27	–	dB
α	stereo blend function	V_{FMi} = 100 µV	5	10	–	dB
THD	total harmonic distortion		–	–	3	%

Multimedia radio tuner OM5608

FEATURES

- Local/DX switching to improve large signal handling on FM when an outdoor antenna or cable network is connected
- Local/DX function provides different search levels which are useful for spectrum analyser functions
- Three extra I/O expander ports are available for general purpose (I^2C-bus only)
- MPX signal available
- The module meets the *"FCC regulations"*
- The OM5608 operates in accordance with *"CENELEC EN55022"* and *"CENELEC EN50082-1"*.

GENERAL DESCRIPTION

The OM5608 is an FM-radio tuner which includes a brand new concept in tuning techniques. The new tuning concept combines the advantages of hand tuning together with electronic facilities and features. The tuner is I^2C-bus controlled and designed for the Japanese FM-band.

ANTENNA CONNECTOR

RF connector

- RF-connection: F-connector (FM input impedance = 75 Ω).

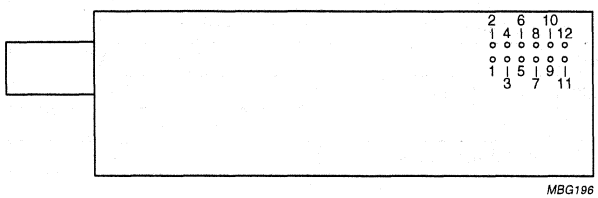


Fig.1 F-connector.

ORDERING INFORMATION

UNIT	FREQUENCY (MHz)	BUS	RF CONNECTOR
FM I^2C-bus	76 to 90	I^2C-bus	F-connector

PINNING

PIN	DESCRIPTION
1	port 5 PCF8574A (I^2C-bus)
2	port 6 PCF8574A (I^2C-bus)
3	port 7 PCF8574A (I^2C-bus)
4	SCL; serial clock input[1]
5	stereo indicator
6	SDA; serial data input/output[1]
7	supply voltage (+5 V)
8	supply voltage (+12 V)
9	audio right output
10	ground
11	audio left output
12	MPX signal

Note

1. See *"The I^2C-bus and how to use it"* (ordering number 9398 393 40011).

INTERFACE

- Digital driving: I^2C-bus
- Audio output: typical 900 mV RMS (load 600 Ω) for FM Δf = 75 kHz
- Supply:

  5 V ±10% current ≤30 mA and

  12 V ±1%, ripple ≤1 V, current ≤2 mA
- MPX: DC coupled (load ≥39 kΩ), amplitude typical 150 mV (Δf = 75 kHz)
- RF input connector (75 Ω)
- 12 pin connector.

LIMITING VALUES

IEC publication 68-1; full specification; EMC behaviour: the module is designed to be FCC friendly (part 15).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
T	temperature		15	35	°C
RH	relative humidity		25	85	%
T_{amb}	operating ambient temperature	functional operation	−10	+60	°C
T_{stg}	storage temperature		−20	+70	°C
$V_{esd(pc)}$	electrostatic handling for pin connector	note 1	–	2	kV
		note 2	–	300	V
$V_{esd(RFc)}$	electrostatic handling for RF-connector	note 3	–	4	kV
		note 4	–	500	V

Notes

1. Class B: human body model (1.5 kΩ, 100 pF).
2. Class B: charge device model (0 Ω, 200 pF).
3. Class A: human body model (1.5 kΩ, 100 pF).
4. Class A: charge device model (0 Ω, 200 pF).

CHARACTERISTICS

Direct coaxial feed to 75 Ω RF-connector with coax; signal generator impedance = 75 Ω; RF levels are EMF/2; Δf = 75 kHz; f_i = 85 MHz; f_{mod} = 1 kHz; left and right audio output; R_L = 600 Ω; audio filter = 22 Hz to 15 kHz; temperature range = 15 to 35 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FM mono						
Φ_{lim}	3 dB limiting sensitivity	$V_{11,12}$ = –3 dB; $V_{11,12}$ = 0 dB at V_{FMi} > 100 µV	–	3.5	5	µV
Φ_{RF}	RF sensitivity	(S + N)/N = 26 dB	–	2.2	4	µV
S/N	signal-to-noise ratio	V_{FMi} = 1 mV	–	71	–	dB
f_L	lower audio frequency bandwidth limit	pre-emphasis 75 µs; measured lower limit (–3 dB); f_{ref} = 1 kHz	–	40	70	Hz
f_H	upper audio frequency bandwidth limit	pre-emphasis 75 µs; measured upper limit (–3 dB); f_{ref} = 1 kHz	12.5	14	–	kHz
α_{AM}	AM suppression	AM modulation m = 30%; f_{AF} = 1 kHz	40	58	–	dB
THD	total harmonic distortion		–	1.5	3	%
V_{FMi}	search sensitivity	search stop bits 17 and 16 = 0	–	12	36	µV
V_{FMi}	large signal handling	DX mode; measured distortion = 10%	–	1000	–	mV
att_{RF}	RF attenuation in local mode		15	20	30	dB
V_{FM}	audio output voltage level	V_{FMi} = 1 mV; Δf = 75 kHz; f_{AF} = 400 Hz	700	850	–	mV
FM stereo						
S/N	signal-to-noise ratio	V_{FMi} = 1 mV	60	63	–	dB
α_{cs}	channel separation	f_{AF} = 1 kHz; V_{FMi} = 1 mV	22	28	–	dB
$\lvert\Delta I_O\rvert$	channel imbalance	f_{AF} = 1 kHz; V_{FMi} = 1 mV	–	0.5	3	dB
α_{19}	carrier and harmonic suppression		25	26	–	dB
α_{38}	carrier and harmonic suppression		25	27	–	dB
α	stereo blend function	V_{FMi} = 100 µV	5	10	–	dB
THD	total harmonic distortion		–	–	3	%

128 × 8-bit EEPROM with I²C-bus interface PCA8581; PCA8581C

FEATURES

- Operating supply voltage:
  - 4.5 to 5.5 V (PCA8581)
  - 2.5 to 6.0 V (PCA8581C)
- Integrated voltage multiplier and timer for writing (no external components required)
- Automatic erase before write
- Low standby current; maximum 10 μA
- 8-byte page write mode
- Serial input/output bus (I²C-bus)
- Address by 3 hardware address pins
- Automatic word address incrementing
- Designed for minimum 10000 write cycles per byte
- 10 years minimum non-volatile data retention
- Infinite number of read cycles
- Pin and address compatibility to PCF8570, PCF8571 and PCF8582
- Operating temperature: −25 to +85 °C.

GENERAL DESCRIPTION

The PCA8581 and PCA8581C are low power CMOS EEPROMs with standard and wide operating voltages:

4.5 to 5.5 V (PCA8581)

2.5 to 6.0 V (PCA8581C).

In the following text, the generic term 'PCA8581' is used to refer to both types in all packages except when otherwise specified.

The PCA8581 is organized as 128 words of 8-bytes.

Addresses and data are transferred serially via a two-line bidirectional bus (I²C-bus). The built-in word address register is incremented automatically after each written or read data byte. All bytes can be read in a single operation. Up to 8 bytes can be written in one operation, reducing the total write time per byte. Three address pins, A0, A1 and A2 are used to define the hardware address, allowing the use of up to 8 devices connected to the bus without additional hardware.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage				
	PCA8581		4.5	5.5	V
	PCA8581C		2.5	6.0	V
I_{DD}	supply current (standby)	f_{SCL} = 0 Hz	–	10	μA
T_{amb}	operating ambient temperature		−25	+85	°C
T_{stg}	storage temperature	without EEPROM retention	−65	+150	°C
		with EEPROM retention	−65	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCA8581P	8	DIP	plastic	SOT97-1
PCA8581CP	8	DIP	plastic	SOT97-1
PCA8581T	8	SO8	plastic	SOT96-1
PCA8581CT	8	SO8	plastic	SOT96-1

BLOCK DIAGRAM

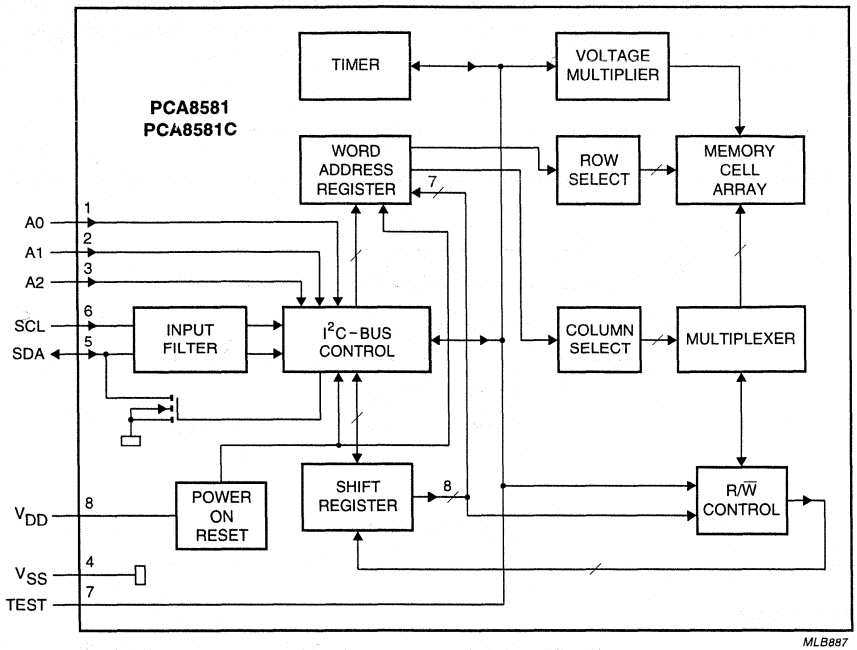


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
A0	1	hardware address input 0
A1	2	hardware address input 1
A2	3	hardware address input 2
V_{SS}	4	negative supply
SDA	5	serial data input/output
SCL	6	serial clock input
TEST	7	test output can be connected to V_{SS}, V_{DD} or left open-circuit
V_{DD}	8	positive supply

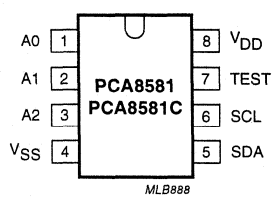


Fig.2 Pin configuration.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

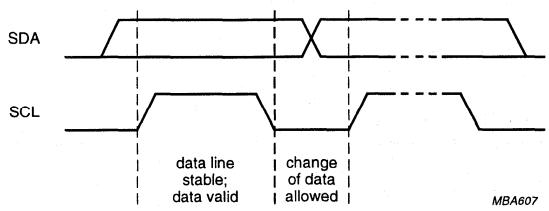


Fig.3 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

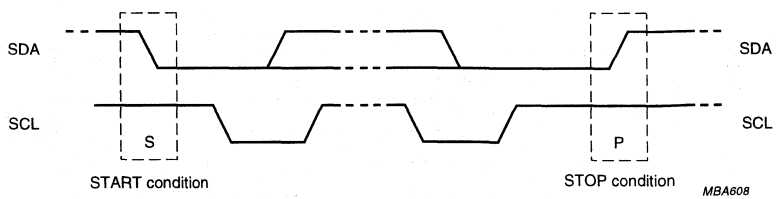


Fig.4 Definition of start and stop conditions.

System configuration

A device generating a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves'.

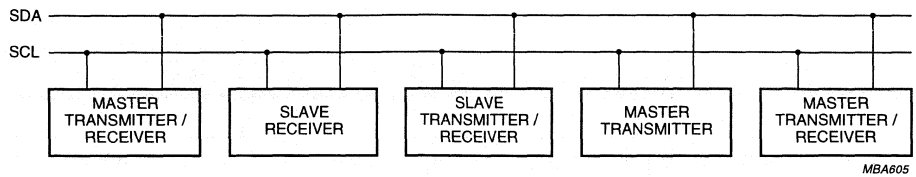


Fig.5 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

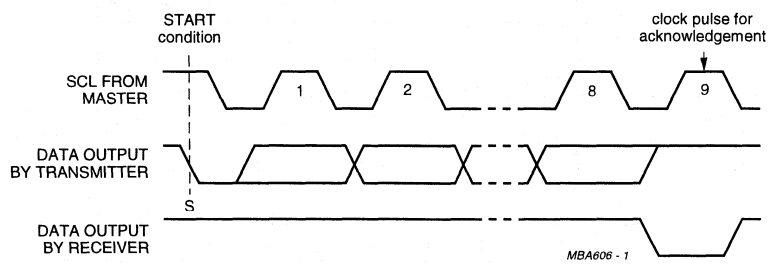


Fig.6 Acknowledgement on the I²C-bus.

I²C-bus protocol

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure. The I²C-bus configuration for the different PCA8581 WRITE and READ cycles is shown in Figs 7, 9 and 10.

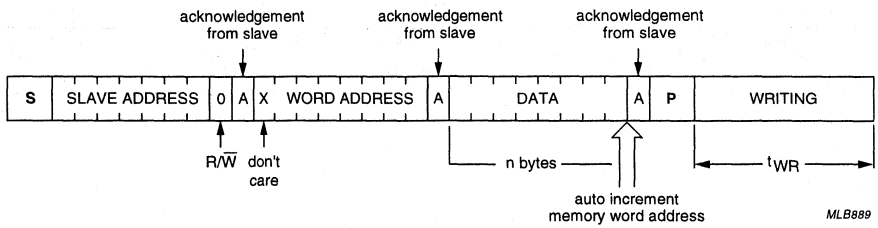
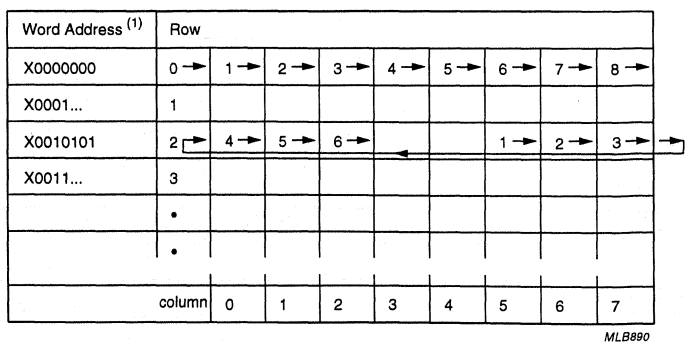


Fig.7 Master transmits to slave receiver (WRITE) mode.

After the word address, one-to-eight data bytes can be sent. The address is automatically incremented, but the four highest address bits (row) are internally latched. Therefore all bytes are written in the same row.

An example of writing eight bytes with word address X 0 0 0 0 0 0 0 and six bytes with word address X 0 0 1 0 1 0 1 is shown in Fig.8.



(1) X = don't care.

Fig.8 Writing eight and six bytes with different word addresses.

To transmit eight bytes in sequential order, begin with the lowest address bits 0 0 0. The data is written after a stop is detected. The data is only written if complete bytes have been received and acknowledged. Writing takes a time t_{WR} (6 to 10 ms) during which the device will not respond to its slave address. Note that to write the next row, a new write operation is required (start, slave address, row address, data and stop).

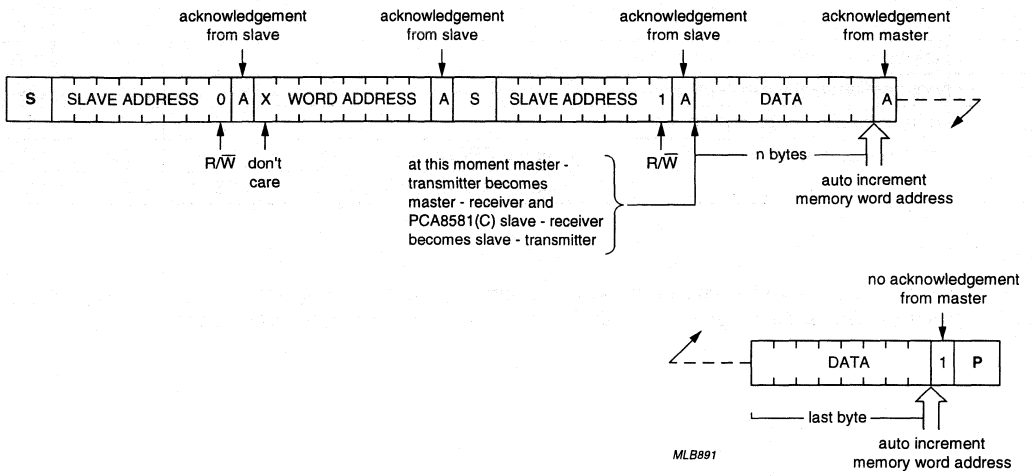


Fig.9 Master reads after setting word address (WRITE word address; READ data).

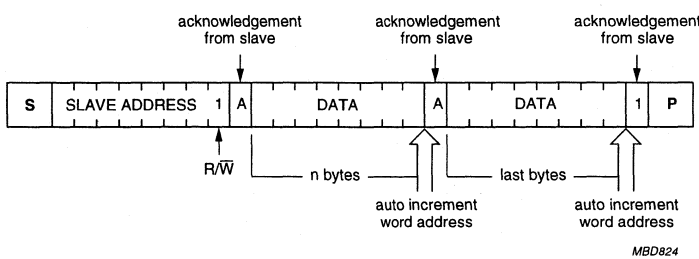


Fig.10 Master reads slave immediately after first byte (READ mode).

An unlimited number of data bytes can be read in one operation. The address is automatically incremented. If a read without setting the word address is performed after a write operation, the address pointer may point at a byte in the row after the previously written row. This occurs if, during writing, the three lowest address bits (column) rolled over.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage (pin 8)		−0.3	+7.0	V
V_I	input voltage (any input)	measured via a 500 Ω resistor	−0.8	V_{DD} + 0.8	V
I_I	DC input current		–	±10	mA
I_O	DC output current		–	±10	mA
P_{tot}	total power dissipation per package		–	150	mW
P_O	power dissipation per output		–	50	mW
T_{amb}	operating ambient temperature		−25	+85	°C
T_{stg}	storage temperature	without EEPROM retention	−65	+150	°C
		with EEPROM retention	−65	+85	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take precautions appropriate to handling MOS devices (see *"Handling MOS Devices"*).

DC CHARACTERISTICS

V_{DD} = 2.5 to 6.0 V (PCA8581C); V_{DD} = 4.5 to 5.5 V (PCA8581); V_{SS} = 0 V; T_{amb} = −25 to +85 °C; note 1; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage					
	PCA8581C		2.5	–	6.0	V
	PCA8581		4.5	–	5.5	V
I_{DD}	supply current					
	standby mode	f_{SCL} = 0 Hz; V_{IL} = 0 V; V_{IH} = V_{DD}	–	–	10	µA
	during read cycle	f_{SCL} = 100 Hz; V_{IL} = 0 V; V_{IH} = V_{DD}	–	–	400	µA
	during write cycle	V_{IL} = 0 V; V_{IH} = V_{DD}	–	–	1000	µA
Inputs A0, A1, A2, SDA and SCL						
V_{IL}	LOW level input voltage		–	–	0.3V_{DD}	V
V_{IH}	HIGH level input voltage		0.7V_{DD}	–	–	V
I_{LI}	input leakage current	V_I = V_{DD} or V_{SS}	–	–	1	µA
C_I	input capacitance	V_I = V_{SS}	–	–	7	pF
Output SDA						
I_{OL}	LOW level output current	V_{OL} = 0.4 V	3	–	–	mA
Erase/write data						
t_{WR}	write time		–	7	10	ms
t_{RET}	data retention time		10	–	–	years

Note

1. The PCA8581C is guaranteed to be programmed with all locations 'FF' (hexadecimal) provided the device has been stored within the temperature limits −65 to +85 °C.

AC CHARACTERISTICS

All timing values are valid within the operating supply voltage and ambient temperature range and reference to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
I²C-bus timing (see Fig.11; note 1)					
f_{SCL}	SCL clock frequency	–	–	100	kHz
t_{SP}	tolerable spike width on bus	–	–	100	ns
t_{BUF}	bus free time	4.7	–	–	µs
$t_{SU;STA}$	start condition set-up time	4.7	–	–	µs
$t_{HD;STA}$	start condition hold time	4.0	–	–	µs
t_{LOW}	SCL LOW time	4.7	–	–	µs
t_{HIGH}	SCL HIGH time	4.0	–	–	µs
t_r	SCL and SDA rise time	–	–	1.0	µs
t_f	SCL and SDA fall time	–	–	0.3	µs
$t_{SU;DAT}$	data set-up time	250	–	–	ns
$t_{HD;DAT}$	data hold time	0	–	–	ns
$t_{VD;DAT}$	SCL LOW to data out valid	–	–	3.4	µs
$t_{SU;STO}$	stop condition set-up time	4.0	–	–	µs

Note

1. A detailed description of the I²C-bus specification, with applications, is given in brochure *"The I²C-bus and how to use it"*. This brochure may be ordered using the code 9398 393 40011.

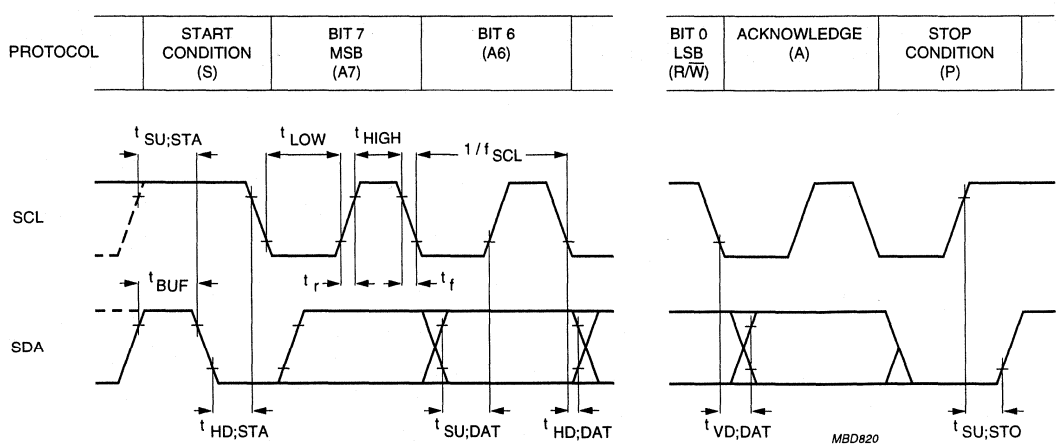


Fig.11 I²C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}.

APPLICATION INFORMATION

Slave address

The PCA8581 has a fixed combination 1 0 1 0 as group 1, while group 2 is fully programmable (see Fig.12).

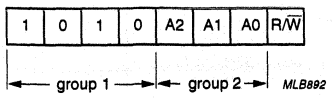
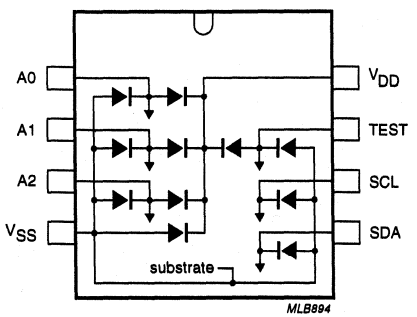


Fig.12 Slave address.

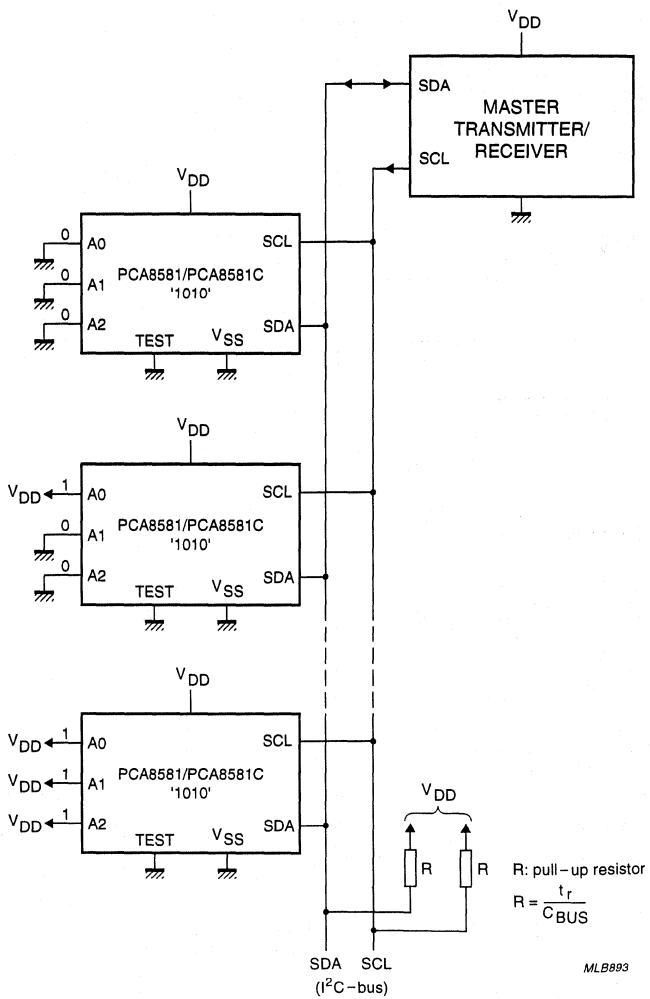
Diode protection



There is no connection between SCL and V_{DD}, and SDA and V_{DD}; this allows powering down the device without affecting I²C-bus operation.

Fig.13 Device diode protection.

Application example



Inputs A0, A1 and A2 must be connected to V_{DD} of V_{SS} but not left open-circuit.

Fig.14 Application diagram.

Remote 8-bit I/O expander for I²C-bus PCF8574

FEATURES

- Operating supply voltage 2.5 to 6 V
- Low standby current consumption of 10 μA maximum
- I²C to parallel port expander
- Open-drain interrupt output
- 8-bit remote I/O Port for the I²C-bus
- Compatible with most microcontrollers
- Latched outputs with high current drive capability for directly driving LEDs
- Address by 3 hardware address pins for use of up to 8 devices (up to 16 with PCF8574A)
- DIP16, space-saving SO16 or SSOP20 package.

GENERAL DESCRIPTION

The PCF8574 is a silicon CMOS circuit. It provides general purpose remote I/O expansion for most microcontroller families via the two-line bidirectional bus (I²C).

The device consists of an 8-bit quasi-bidirectional Port and an I²C interface. The PCF8574 has a low current consumption and includes latched outputs with high current drive capability for directly driving LEDs. It also possesses an interrupt line ($\overline{INT}$) which can be connected to the interrupt logic of the microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I²C-bus. This means that the PCF8574 can remain a simple slave device.

The PCF8574 and PCF8574A versions differ only in their slave address as shown in Fig.9.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8574P; PCF8574AP	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-1
PCF8574T; PCF8574AT	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1
PCF8574TS	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

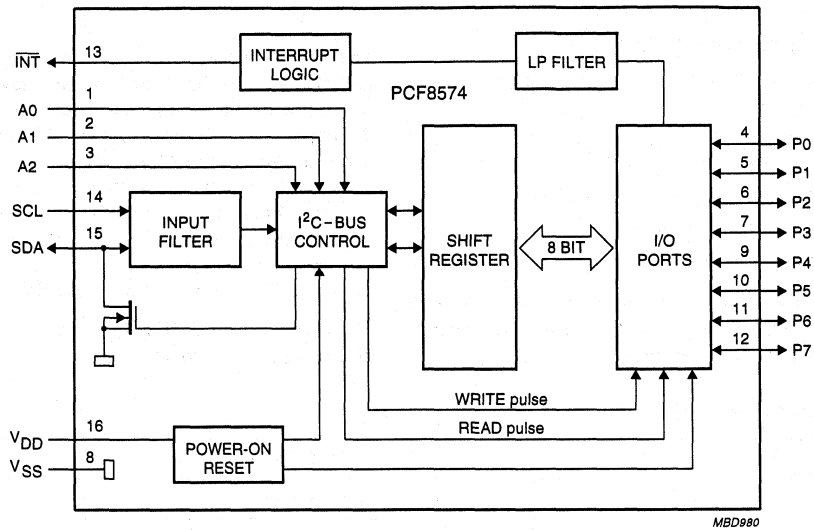


Fig.1 Block diagram (SOT38-1 and SOT162-1).

PINNING

SYMBOL	PIN		DESCRIPTION
	DIP16; SO16	SSOP20	
A0	1	6	address input 0
A1	2	7	address input 1
A2	3	9	address input 2
P0	4	10	quasi-bidirectional I/O Port 0
P1	5	11	quasi-bidirectional I/O Port 1
P2	6	12	quasi-bidirectional I/O Port 2
P3	7	14	quasi-bidirectional I/O Port 3
V_{SS}	8	15	supply ground
P4	9	16	quasi-bidirectional I/O Port 4
P5	10	17	quasi-bidirectional I/O Port 5
P6	11	19	quasi-bidirectional I/O Port 6
P7	12	20	quasi-bidirectional I/O Port 7
$\overline{INT}$	13	1	interrupt output (active LOW)
SCL	14	2	serial clock line
SDA	15	4	serial data line
V_{DD}	16	5	supply voltage
n.c.	–	3	not connected
n.c.	–	8	not connected
n.c.	–	13	not connected
n.c.	–	18	not connected

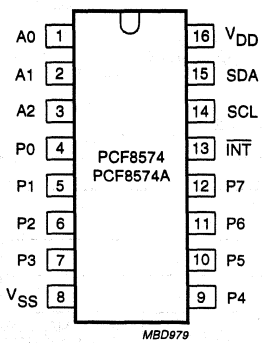


Fig.2 Pin configuration (DIP16; SO16).

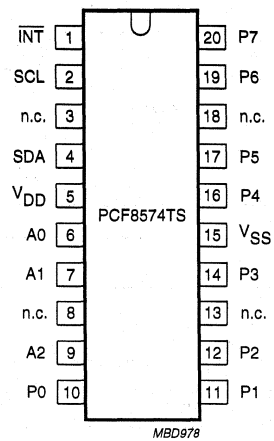


Fig.3 Pin configuration (SSOP20).

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Fig.4).

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S).
A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P) (see Fig.5).

System configuration

A device generating a message is a 'transmitter', a device receiving is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves' (see Fig.6).

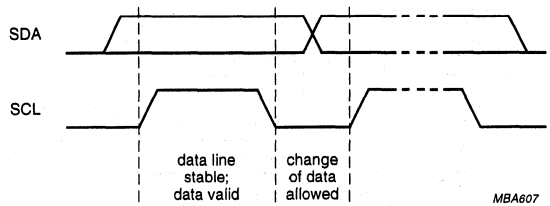


Fig.4 Bit transfer.

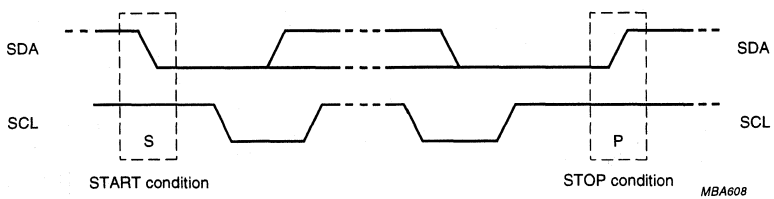


Fig.5 Definition of start and stop conditions.

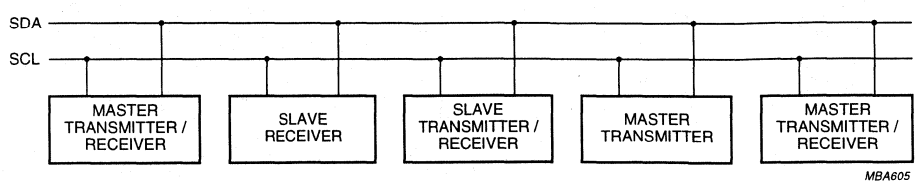


Fig.6 System configuration.

Acknowledge

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

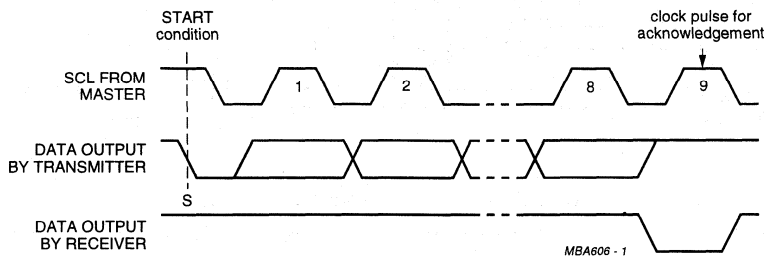


Fig.7 Acknowledgement on the I²C-bus.

FUNCTIONAL DESCRIPTION

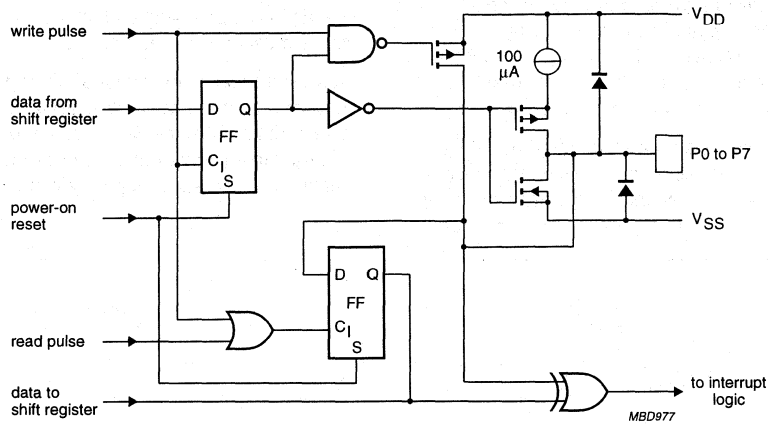
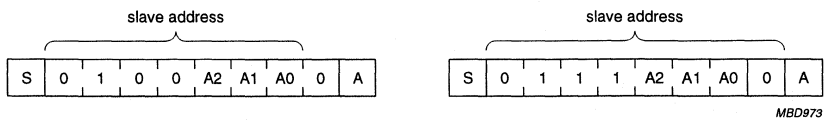


Fig.8 Simplified schematic diagram of each Port.

Addressing

For addressing see Figs 9, 10 and 11.



(a) PCF8574.
(b) PCF8574A.

Fig.9 PCF8574 and PCF8574A slave addresses.

Each bit of the PCF8574 I/O Port can be independently used as an input or output. Input data is transferred from the Port to the microcontroller by the READ mode (see Fig.11). Output data is transmitted to the Port by the WRITE mode (see Fig.10).

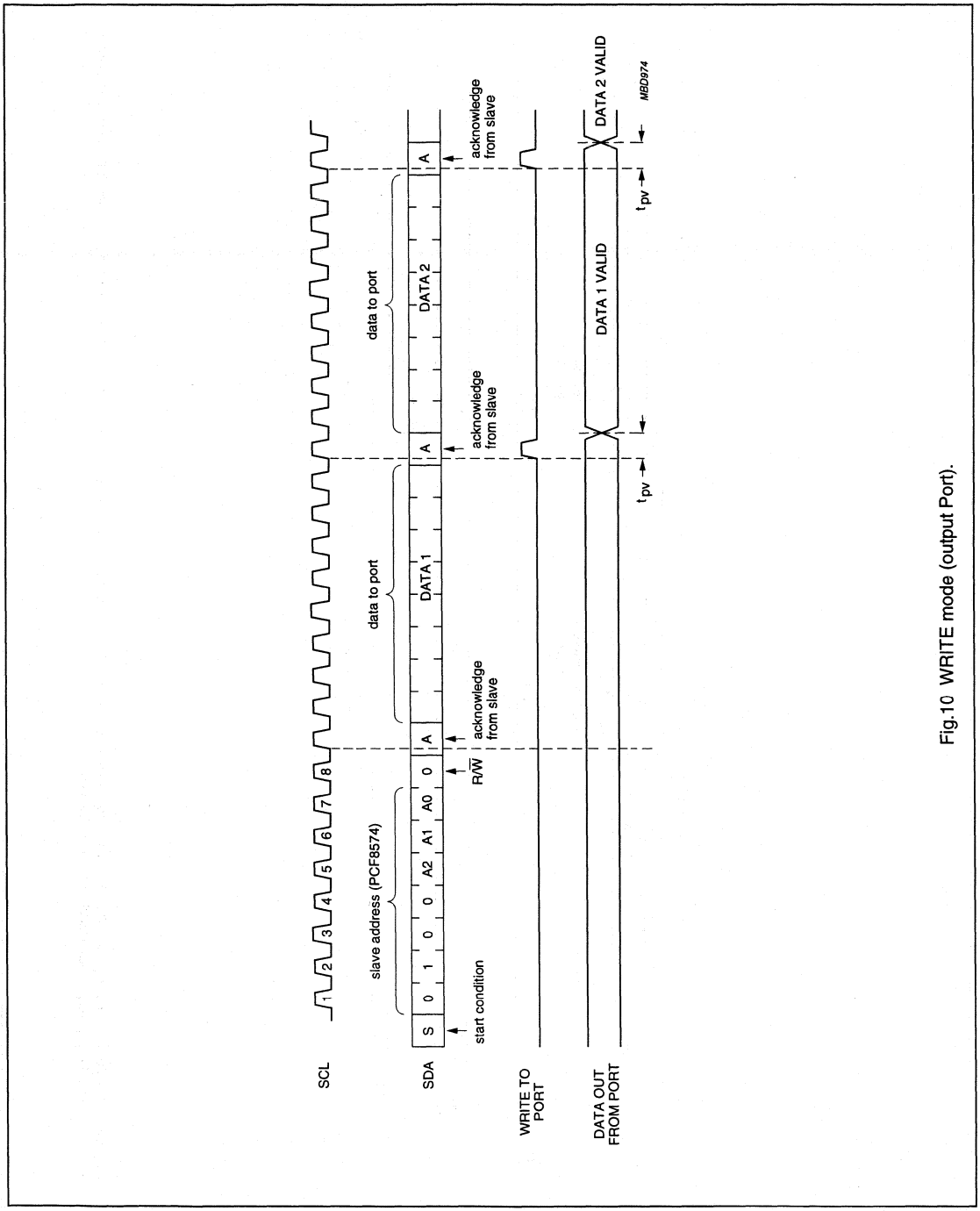
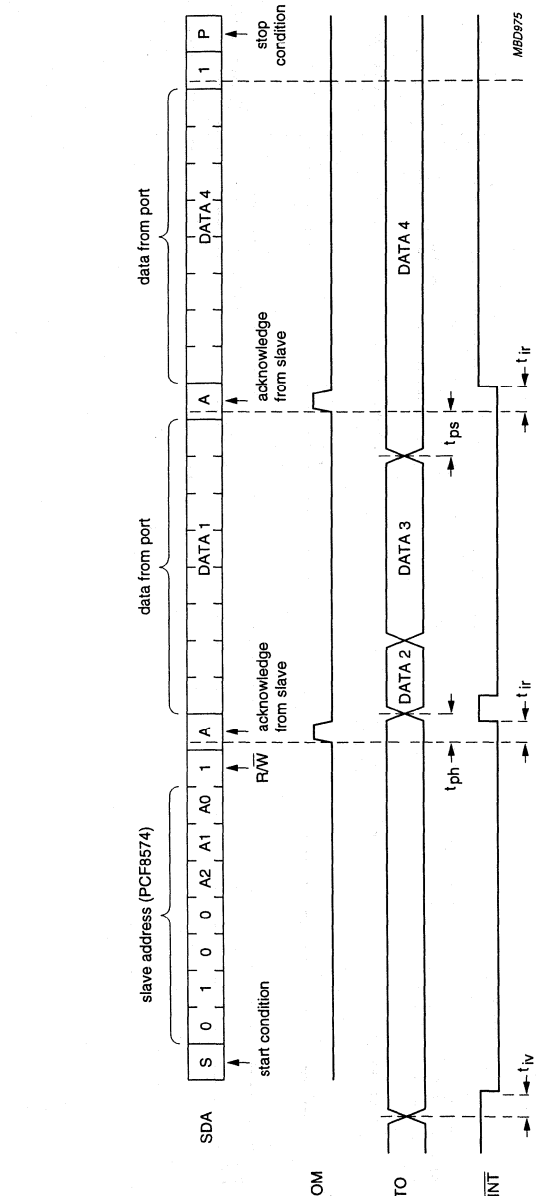


Fig.10 WRITE mode (output Port).



A LOW-to-HIGH transition of SDA, while SCL is HIGH is defined as the stop concition (P). Transfer of data can be stopped at any moment by a stop condition. When this occurs, data present at the last acknowledge phase is valid (output mode). Input data is lost.

Fig.11 READ mode (input Port).

Interrupt (see Figs 12 and 13)

The PCF8574 provides an open drain output ($\overline{INT}$) which can be fed to a corresponding input of the microcontroller. This gives these chips a type of master function which can initiate an action elsewhere in the system.

An interrupt is generated by any rising or falling edge of the Port inputs in the input mode. After time t_{iv} the signal $\overline{INT}$ is valid.

Resetting and reactivating the interrupt circuit is achieved when data on the Port is changed to the original setting or data is read from or written to the Port which has generated the interrupt.

Resetting occurs as follows:

- In the READ mode at the acknowledge bit after the rising edge of the SCL signal.
- In the WRITE mode at the acknowledge bit after the HIGH-to-LOW transition of the SCL signal.
- Interrupts which occur during the acknowledge clock pulse may be lost (or very short) due to the resetting of the interrupt during this pulse.

Each change of the Ports after the resettings will be detected and after the next rising clock edge, will be transmitted as $\overline{INT}$. Reading from or writing to another device does not affect the interrupt circuit.

Quasi-bidirectional I/O Ports (see Fig.14)

A quasi-bidirectional Port can be used as an input or output without the use of a control signal for data direction. At power-on the Ports are HIGH. In this mode only a current source to V_{DD} is active. An additional strong pull-up to V_{DD} allows fast rising edges into heavily loaded outputs. These devices turn on when an output is written HIGH, and are switched off by the negative edge of SCL. The Ports should be HIGH before being used as inputs.

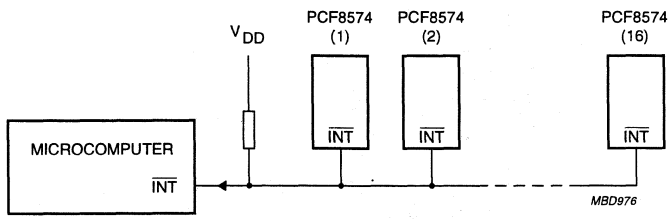


Fig.12 Application of multiple PCF8574s with interrupt.

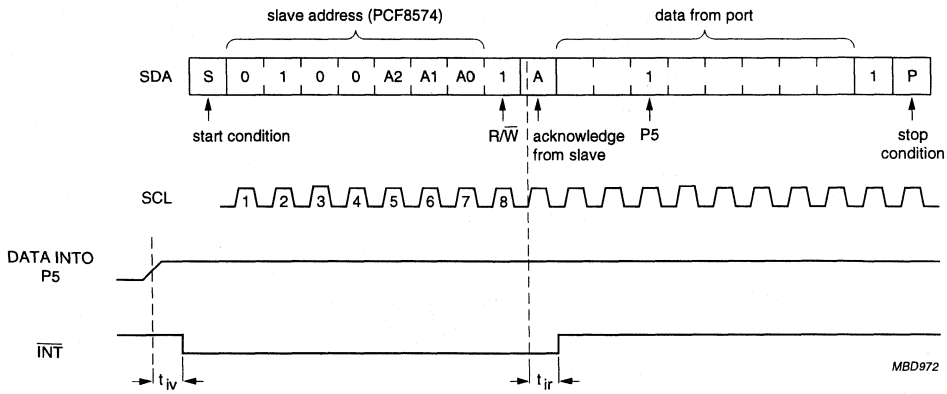


Fig.13 Interrupt generated by a change of input to Port P5.

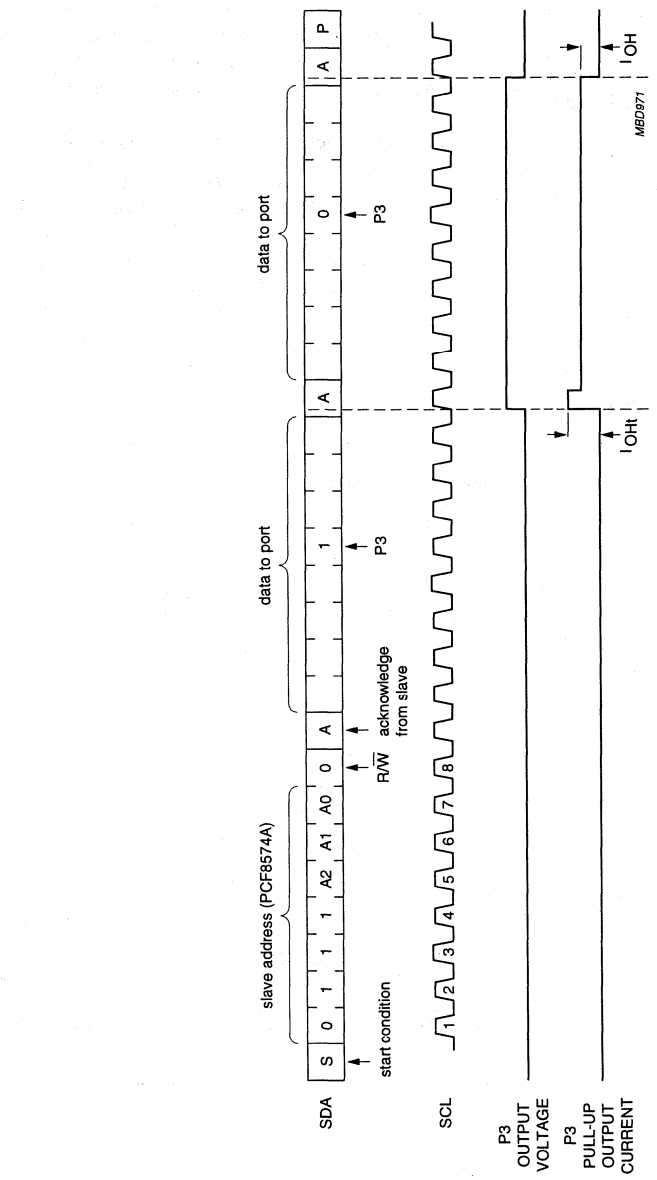


Fig.14 Transient pull-up current I_{OHt} while P3 changes from LOW-to-HIGH and back to LOW.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+7.0	V
V_I	input voltage	V_{SS} − 0.5	V_{DD} + 0.5	V
I_I	DC input current	−	±20	mA
I_O	DC output current	−	±25	mA
I_{DD}	supply current	−	±100	mA
I_{SS}	supply current	−	±100	mA
P_{tot}	total power dissipation	−	400	mW
P_O	power dissipation per output	−	100	mW
T_{stg}	storage temperature	−65	+150	°C
T_{amb}	operating ambient temperature	−40	+85	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see *"Handling MOS devices"*).

DC CHARACTERISTICS

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		2.5	−	6.0	V
I_{DD}	supply current	operating mode; V_{DD} = 6 V; no load; $V_I = V_{DD}$ or V_{SS}; f_{SCL} = 100 kHz	−	40	100	µA
I_{stb}	standby current	standby mode; V_{DD} = 6 V; no load; $V_I = V_{DD}$ or V_{SS}	−	2.5	10	µA
V_{POR}	power-on reset voltage	V_{DD} = 6 V; no load; $V_I = V_{DD}$ or V_{SS}; note 1	−	1.3	2.4	V
Input SCL; input/output SDA						
V_{IL}	LOW level input voltage		−0.5	−	$+0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	−	V_{DD} + 0.5	V
I_{OL}	LOW level output current	V_{OL} = 0.4 V	3	−	−	mA
$\|I_L\|$	leakage current	$V_I = V_{DD}$ or V_{SS}	−	−	1	µA
C_I	input capacitance	$V_I = V_{SS}$	−	−	7	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I/O Ports						
V_{IL}	LOW level input voltage		−0.5	–	$+0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	$V_{DD} + 0.5$	V
$I_{IHL(max)}$	maximum allowed input current through protection diode	$V_I \geq V_{DD}$ or $V_I \leq V_{SS}$	–	–	±400	μA
I_{OL}	LOW level output current	V_{OL} = 1 V; V_{DD} = 5 V	10	25	–	mA
I_{OH}	HIGH level output current	$V_{OH} = V_{SS}$	30	–	300	μA
I_{OHt}	transient pull-up current	HIGH during acknowledge (see Fig.14); $V_{OH} = V_{SS}$; V_{DD} = 2.5 V	–	−1	–	mA
C_I	input capacitance		–	–	10	pF
C_O	output capacitance		–	–	10	pF
Port timing (see Figs 10 and 11); **$C_L \leq$ 100 pF**						
t_{pv}	output data valid		–	–	4	μs
t_{su}	input data set-up time		0	–	–	μs
t_h	input data hold time		4	–	–	μs
Interrupt $\overline{INT}$ (see Fig.13)						
I_{OL}	LOW level output current	V_{OL} = 0.4 V	1.6	–	–	mA
$\|I_L\|$	leakage current	$V_I = V_{DD}$ or V_{SS}	–	–	1	μA
TIMING; $C_L \leq$ 100 pF						
t_{iv}	input data valid time		–	–	4	μs
t_{ir}	reset delay time		–	–	4	μs
Select inputs A0 to A2						
V_{IL}	LOW level input voltage		−0.5	–	$+0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	$V_{DD} + 0.5$	V
$\|I_{LI}\|$	input leakage current	pin at V_{DD} or V_{SS}	–	–	250	nA

Note

1. The power-on reset circuit resets the I²C-bus logic with $V_{DD} < V_{POR}$ and sets all Ports to logic 1 (with current source to V_{DD}).

I²C-BUS TIMING CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
I²C-BUS TIMING (see Fig.15; note 1)					
f_{SCL}	SCL clock frequency	–	–	100	kHz
t_{SW}	tolerable spike width on bus	–	–	100	ns
t_{BUF}	bus free time	4.7	–	–	µs
$t_{SU;STA}$	start condition set-up time	4.7	–	–	µs
$t_{HD;STA}$	start condition hold time	4.0	–	–	µs
t_{LOW}	SCL LOW time	4.7	–	–	µs
t_{HIGH}	SCL HIGH time	4.0	–	–	µs
t_r	SCL and SDA rise time	–	–	1.0	µs
t_f	SCL and SDA fall time	–	–	0.3	µs
$t_{SU;DAT}$	data set-up time	250	–	–	ns
$t_{HD;DAT}$	data hold time	0	–	–	ns
$t_{VD;DAT}$	SCL LOW to data out valid	–	–	3.4	µs
$t_{SU;STO}$	stop condition set-up time	4.0	–	–	µs

Note

1. All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

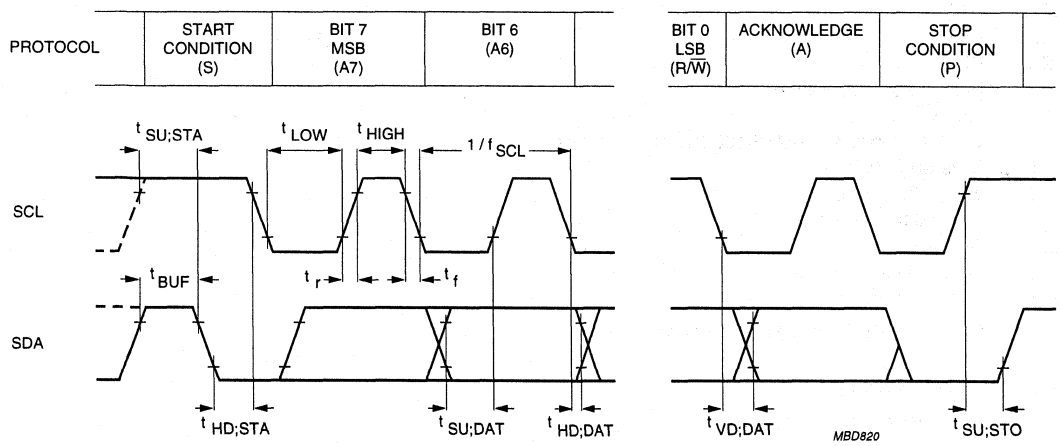


Fig.15 I²C-bus timing diagram.

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1 FEATURES

- Parallel-bus to I²C-bus protocol converter and interface
- Compatible with most parallel-bus microcontrollers/microprocessors including 8049, 8051, 6800, 68000, and Z80
- Both master and slave functions
- Automatic detection and adaption to bus interface type
- Programmable interrupt vector
- Multi-master capability
- I²C-bus monitor mode
- Long-distance mode (4-wire)
- Operating supply voltage 4.5 to 5.5 V
- Operating temperature range: –40 to +85 °C.

2 GENERAL DESCRIPTION

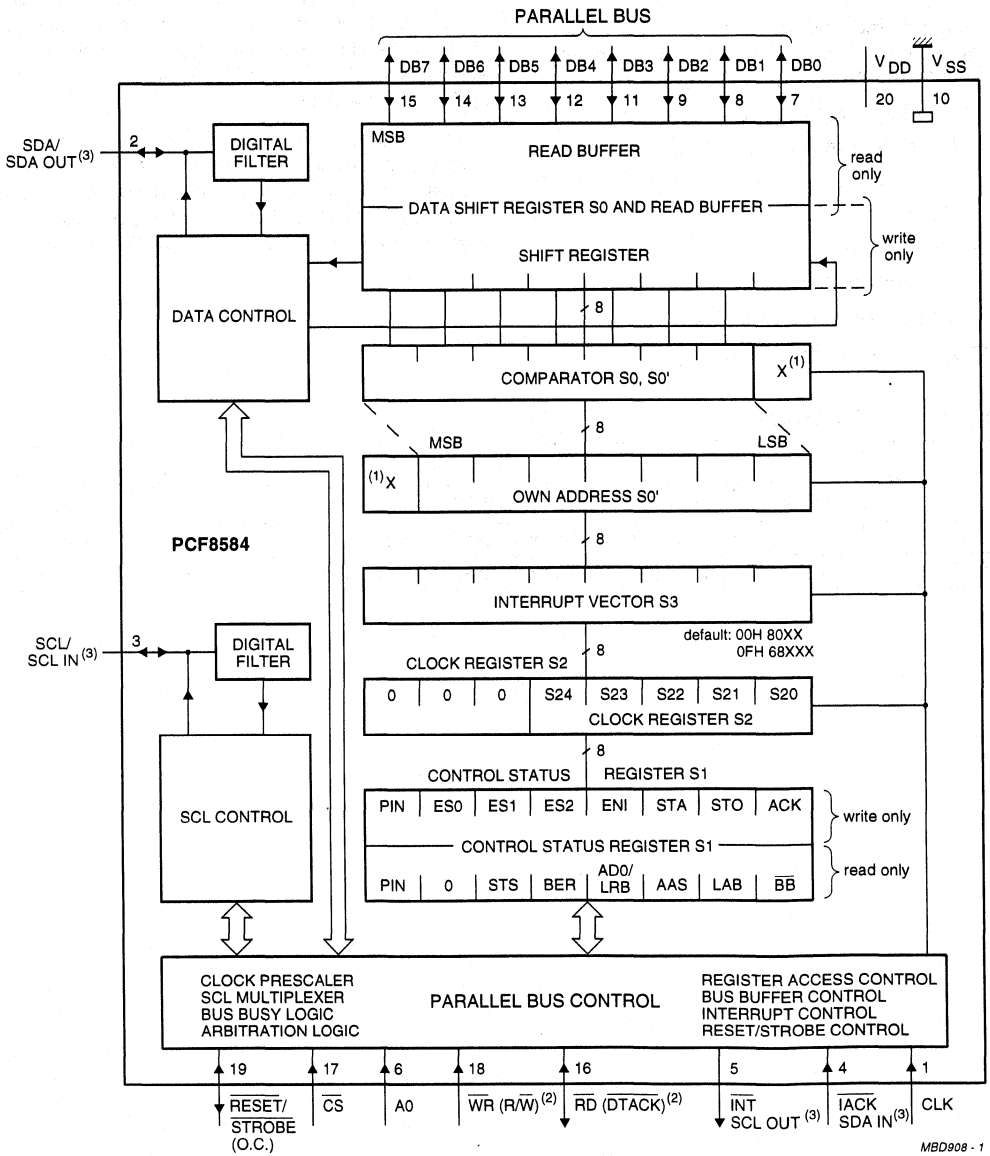
The PCF8584 is an integrated circuit designed in CMOS technology which serves as an interface between most standard parallel-bus microcontrollers/microprocessors and the serial I²C-bus. The PCF8584 provides both master and slave functions.

Communication with the I²C-bus is carried out on a byte-wise basis using interrupt or polled handshake. It controls all the I²C-bus specific sequences, protocol, arbitration and timing. The PCF8584 allows parallel-bus systems to communicate bidirectionally with the I²C-bus.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8584P	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
PCF8584T	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

4 BLOCK DIAGRAM

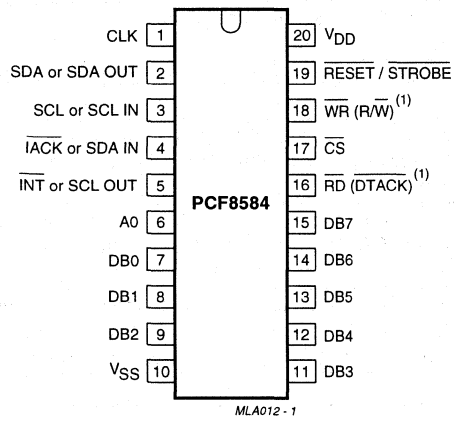


(1) X = don't care.
(2) Pin mnemonics between brackets indicate the 68000 mode pin designations.
(3) These pin mnemonics represent the long-distance mode pin designations.

Fig.1 Block diagram.

5 PINNING

SYMBOL	PIN	I/O	DESCRIPTION
CLK	1	I	clock input from microcontroller clock generator (internal pull-up)
SDA or SDA OUT	2	I/O	I²C-bus serial data input/output (open-drain). Serial data output in long-distance mode.
SCL or SCL IN	3	I/O	I²C-serial clock input/output (open-drain). Serial clock input in long-distance mode.
$\overline{IACK}$ or SDA IN	4	I	Interrupt acknowledge input (internal pull-up); when this signal is asserted the interrupt vector in register S3 will be available at the bus Port if the ENI flag is set. Serial data input in long-distance mode.
$\overline{INT}$ or SCL OUT	5	O	Interrupt output (open-drain); this signal is enabled by the ENI flag in register S1. It is asserted when the PIN flag is reset. (PIN is reset after 1 byte is transmitted or received over the I²C-bus). Serial clock output in long-distance mode.
A0	6	I	Register select input (internal pull-up); this input selects between the control/status register and the other registers. Logic 1 selects register S1, logic 0 selects one of the other registers depending on bits loaded in ESO, ES1, and ES2 of register S1.
DB0	7	I/O	bidirectional 8-bit bus Port 0
DB1	8	I/O	bidirectional 8-bit bus Port 1
DB2	9	I/O	bidirectional 8-bit bus Port 2
V_{SS}	10	–	ground
DB3	11	I/O	bidirectional 8-bit bus Port 3
DB4	12	I/O	bidirectional 8-bit bus Port 4
DB5	13	I/O	bidirectional 8-bit bus Port 5
DB6	14	I/O	bidirectional 8-bit bus Port 6
DB7	15	I/O	bidirectional 8-bit bus Port 7
$\overline{RD}$ ($\overline{DTACK}$)	16	I/(O)	$\overline{RD}$ is the read control input for MAB8049, MAB8051 or Z80-types. $\overline{DTACK}$ is the data transfer control output for 68000-types (open-drain).
$\overline{CS}$	17	I	chip select input (internal pull-up)
$\overline{WR}$ (R/$\overline{W}$)	18	I	$\overline{WR}$ is the write control input for MAB8048, MAB8051, or Z80-types (internal pull-up). R/$\overline{W}$ control input for 68000-types.
$\overline{RESET}$/ $\overline{STROBE}$	19	I/O	Reset input (open-drain); this input forces the I²C-bus controller into a predefined state; all flags are reset, except PIN, which is set. Also functions as strobe output.
V_{DD}	20	–	supply voltage



(1) Pin mnemonics between brackets indicate the 68000 mode pin designations.

Fig.2 Pin configuration.

6 FUNCTIONAL DESCRIPTION

6.1 General

The PCF8584 acts as an interface device between standard high-speed parallel buses and the serial I²C-bus. On the I²C-bus, it can act either as master or slave. Bidirectional data transfer between the I²C-bus and the parallel-bus microcontroller is carried out on a byte-wise basis, using either an interrupt or polled handshake. Interface to either 80XX-type (e.g. MAB8048, MAB8051, Z80) or 68000-type buses is possible. Selection of bus type is automatically performed (see Section 6.2).

Table 1 Control signals utilized by the PCF8584 for microcontroller/microprocessor interfacing

TYPE	R/$\overline{W}$	$\overline{WR}$	$\overline{R}$	$\overline{DTACK}$	$\overline{IACK}$
8048/ 8051	no	yes	yes	no	no
68000	yes	no	no	yes	yes
Z80	no	yes	yes	no	yes

The structure of the PCF8584 is similar to that of the I²C-bus interface section of the MABXXXX/PCF84(C)XX-series of microcontrollers, but with a modified control structure. The PCF8584 has five internal register locations. Three of these (own address register S0', clock register S2 and interrupt vector S3) are used for initialization of the PCF8584. Normally they are only written once directly after resetting of the PCF8584.

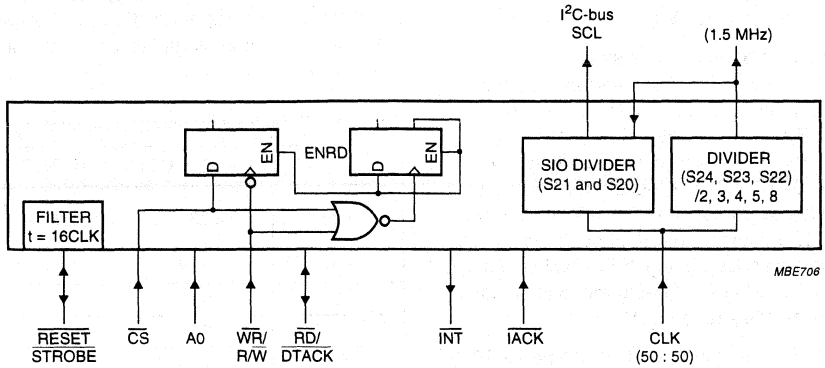
The remaining two registers function as double registers (data buffer/shift register S0, and control/status register S1) which are used during actual data transmission/reception. By using these double registers, which are separately write and read accessible, overhead for register access is reduced. Register S0 is a combination of a shift register and data buffer.

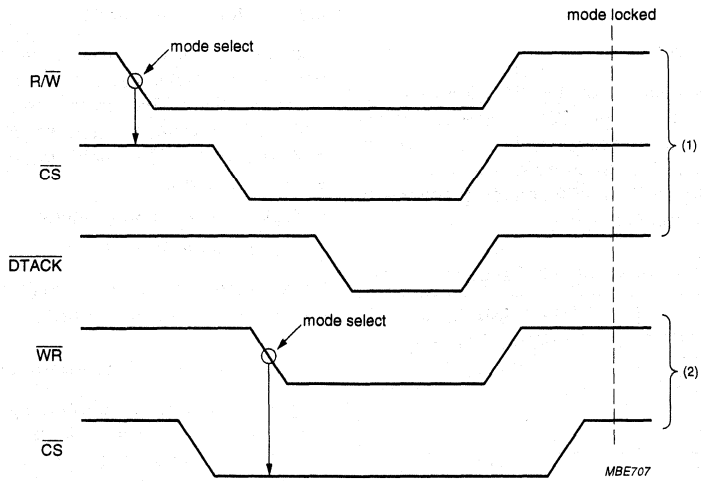
Register S0 performs all serial-to-parallel interfacing with the I²C-bus.

Register S1 contains I²C-bus status information required for bus access and/or monitoring.

6.2 Interface Mode Control (IMC)

Selection of either an 80XX mode or 68000 mode interface is achieved by detection of the first $\overline{WR}$-$\overline{CS}$ signal sequence. The concept takes advantage of the fact that the write control input is common for both types of interfaces. An 80XX-type interface is default. If a HIGH-to-LOW transition of $\overline{WR}$ (R/$\overline{W}$) is detected while $\overline{CS}$ is HIGH, the 68000-type interface mode is selected and the $\overline{DTACK}$ output is enabled. Care must be taken that $\overline{WR}$ and $\overline{CS}$ are stable after reset.





(1) Bus timing; 68000 mode write cycle.
(2) Bus timing; 80XX mode.

Fig.3 68000/80XX timing sequence utilized by the Interface Mode Control (IMC).

6.3 Set-up registers S0', S2 and S3

Registers S0', S2 and S3 are used for initialization of the PCF8584 (see Fig.5 'Initialization sequence' flowchart).

6.4 Own address register S0'

When the PCF8584 is addressed as slave, this register must be loaded with the 7-bit I²C-bus address to which the PCF8584 is to respond. During initialization, the own address register S0' must be written to, regardless whether it is later used. The Addressed As Slave (AAS) bit in status register S1 is set when this address is received (the value in S0 is compared with the value in S0'). Note that the S0 and S0' registers are offset by one bit; hence, programming the own address register S0' with a value of 55H will result in the value AAH being recognized as the PCF8584's slave address (see Fig.1).

Programming of S0' is accomplished via the parallel-bus when A0 is LOW, with the appropriate bit combinations set in control status register S1 (S1 is written when pin A0 = HIGH). Bit combinations for accessing all registers are given in Table 5. After reset, S0' has default address 00H (PCF8584 is thus initially in monitor mode, see Section 6.12).

6.5 Clock register S2

Register S2 provides control over chip clock frequency and SCL clock frequency. S20 and S21 provide a selection of 4 different I²C-bus SCL frequencies which are shown in Table 2. Note that these SCL frequencies are only obtained when bits S24, S23 and S22 are programmed to the correct input clock frequency (f_{clk}).

Table 2 Register S2 selection of SCL frequency

BIT		APPROXIMATE SCL FREQUENCY f_{SCL} (kHz)
S21	S20	
0	0	90
0	1	45
1	0	11
1	1	1.5

S22, S23 and S24 are used for control of the internal clock prescaler. Due to the possibility of varying microcontroller clock signals, the prescaler can be programmed to adapt to 5 different clock rates, thus providing a constant internal clock. This is required to provide a stable time base for the SCL generator and the digital filters associated with the I²C-bus signals SCL and SDA. Selection for adaption to external clock rates is shown in Table 3.

Programming of S2 is accomplished via the parallel-bus when A0 = LOW, with the appropriate bit combinations set in control status register S1 (S1 is written when A0 = HIGH). Bit combinations for accessing all registers are given in Table 5.

Table 3 Register S2 selection of clock frequency

INTERNAL CLOCK FREQUENCY			
S24	S23	S22	f_{clk} (MHz)
0	X[1]	X[1]	3
1	0	0	4.43
1	0	1	6
1	1	0	8
1	1	1	12

Note

1. X = don't care.

6.6 Interrupt vector S3

The interrupt vector register provides an 8-bit user-programmable vector for vectored-interrupt microcontrollers. The vector is sent to the bus port (DB7 to DB0) when an interrupt acknowledge signal is asserted and the ENI (enable interrupt) flag is set. Default vector values are:

- Vector is '00H' in 80XX mode
- Vector is '0FH' in 68000 mode.

On reset the PCF8584 is in the 80XX mode, thus the default interrupt vector is '00H'.

6.7 Data shift register/read buffer S0

Register S0 acts as serial shift register and read buffer interfacing to the I²C-bus. All read and write operations to/from the I²C-bus are done via this register. S0 is a combination of a shift register and a data buffer; parallel data is always written to the shift register, and read from the data buffer. I²C-bus data is always shifted in or out of shift register S0.

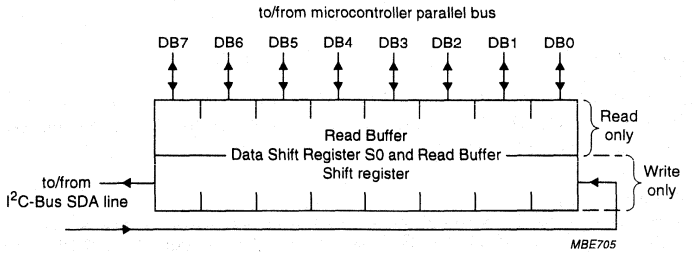


Fig.4 Data shift register/bus buffer S0.

In receiver mode the data from the shift register is copied to the read buffer during the acknowledge phase. Further reception of data is inhibited (SCL held LOW) until the S0 read buffer is read (see Section 6.8.1.1).

In the transmitter mode data is transmitted to the I²C-bus as soon as it is written to the S0 shift register if the serial I/O is enabled (ESO = 1).

Remarks:

1. A minimum of 6 clock cycles must elapse between consecutive parallel-bus accesses to the PCF8584 when the I²C-bus controller operates at 8 or 12 MHz. This may be reduced to 3 clock cycles for lower operating frequencies.
2. To start a read operation immediately after a write, it is necessary to read the S0 read buffer in order to invoke reception of the first byte ('dummy read' of the address). Immediately after the acknowledgement, this first byte will be transferred from the shift register to the read buffer. The **next** read will then transfer the correct value of the first byte to the microcontroller bus (see Fig.7).

6.8 Control/status register S1

Register S1 controls I²C-bus operation and provides I²C-bus status information. Register S1 is accessed by a HIGH signal on register select input A0. For more efficient communication between microcontroller/processor and the I²C-bus, register S1 has separate read and write functions for all bit positions (see Fig.3). The write-only section provides register access control and control over I²C-bus signals, while the read-only section provides I²C-bus status information.

Table 4 Control/status register S1

CONTROL/STATUS	BITS								MODE
Control[1]	PIN	ESO	ES1	ES2	ENI	STA	STO	ACK	write only
Status[2]	PIN	0[3]	STS	BER	AD0/ LRB	AAS	LAB	$\overline{BB}$	read only

Notes

1. For further information see Section 6.8.1.
2. For further information see Section 6.8.2.
3. Logic 1 if not-initialized.

6.8.1 Register S1 control section

The write-only section of S1 enables access to registers S0, S0', S1, S2 and S3, and controls I²C-bus operation; see Table 4.

6.8.1.1 PIN (Pending Interrupt Not)

When the PIN bit is written with a logic 1, all status bits are reset to logic 0. This may serve as a software reset function (see Figs 5 to 9). PIN is the only bit in S1 which may be both read and written to. PIN is mostly used as a status bit for synchronizing serial communication, see Section 6.8.2.

6.8.1.2 ESO (Enable Serial Output)

ESO enables or disables the serial I²C-bus I/O. When ESO is LOW, register access for initialization is possible. When ESO is HIGH, I²C-bus communication is enabled; communication with serial shift register S0 is enabled and the S1 bus status bits are made available for reading.

Table 5 Register access control; ESO = 0 (serial interface off) and ESO = 1 (serial interface on)

INTERNAL REGISTER ADDRESSING 2-WIRE MODE				
A0	**ES1**	**ES2**	**$\overline{\text{IACK}}$**	**FUNCTION**
ESO = 0; serial interface off(1)				
1	0	X	1(2)	R/W S1: control
0	0	0	1(2)	R/W S0': (own address)
0	0	1	1(2)	R/W S3: (interrupt vector)
0	1	0	1(2)	R/W S2: (clock register)
ESO = 0; serial interface on				
1	0	X	1	W S1: control
1	0	X	1	R S1; status
0	0	0	1	R/W S0: (data)
0	0	1	1	R/W S3: (interrupt vector)
X	0	X	0	R S3: (interrupt vector ACK cycle))

Notes

1. With ESO = 0, bits ENI, STA, STO and ACK of S1 can be read for test purposes.
2. 'X' if ENI = 0.

6.8.1.3 ES1 and ES2

ES1 and ES2 control selection of other registers for initialization and control of normal operation. After these bits are programmed for access to the desired register (shown in Table 5), the register is selected by a logic LOW level on register select pin A0.

6.8.1.4 ENI

This bit enables the external interrupt output $\overline{\text{INT}}$, which is generated when the PIN bit is active (logic 0).

This bit must be set to logic 0 before entering the long-distance mode, and remain at logic 0 during operation in long-distance mode.

6.8.1.5 STA and STO

These bits control the generation of the I²C-bus START condition and transmission of slave address and R/$\overline{W}$ bit, generation of repeated START condition, and generation of the STOP condition (see Table 7).

Table 6 Register access control; ESO = 1 (serial interface on) and ES1 = 1; long-distance (4-wire) mode; note 1

INTERNAL REGISTER ADDRESSING: LONG-DISTANCE (4-WIRE) MODE				
A0	**ES1**	**ES2**	**$\overline{IACK}$**	**FUNCTION**
1	1	X	1	W S1: control
1	1	X	X	R S1; status
0	1	X	X	R/W S0; (data)

Note

1. Trying to read from or write to registers other than S0 and S1 (setting ESO = 0) brings the PCF8584 out of the long-distance mode.

Table 7 Instruction table for serial bus control

STA	STO	PRESENT MODE	FUNCTION	OPERATION
1	0	SLV/REC	START	transmit START + address, remain MST/TRM if R/$\overline{W}$ = 0; go to MST/REC if R/$\overline{W}$ = 1
1	0	MST/TRM	REPEAT START	same as for SLV/REC
0	1	MST/REC; MST/TRM	STOP READ; STOP WRITE	transmit STOP go to SLV/REC mode; note 1
1	1	MST	DATA CHAINING	send STOP, START and address after last master frame without STOP sent; note 2
0	0	ANY	NOP	no operation; note 3

Notes

1. In master receiver mode, the last byte must be terminated with ACK bit HIGH ('negative acknowledge').
2. If both STA and STO are set HIGH simultaneously in master mode, a STOP condition followed by a START condition + address will be generated. This allows 'chaining' of transmissions without relinquishing bus control.
3. All other STA and STO mode combinations not mentioned in Table 7 are NOPs.

6.8.1.6 ACK

This bit must be set normally to a logic 1. This causes the I²C-bus controller to send an acknowledge automatically after each byte (this occurs during the 9th clock pulse). The bit must be reset (to logic 0) when the I²C-bus controller is operating in master/receiver mode and requires no further data to be sent from the slave transmitter. This causes a negative acknowledge on the I²C-bus, which halts further transmission from the slave device.

6.8.2 REGISTER S1 STATUS SECTION

The read-only section of S1 enables access to I²C-bus status information; see Table 4.

6.8.2.1 PIN bit

'Pending Interrupt Not' (MSB of register S1) is a status flag which is used to synchronize serial communication and is set to logic 0 whenever the PCF8584 requires servicing. The PIN bit is normally read in polled applications to determine when an I²C-bus byte transmission/reception is completed. The PIN bit may also be written, see Section 6.8.1.

Each time a serial data transmission is initiated (by setting the STA bit in the same register), the PIN bit will be set to logic 1 automatically (inactive). When acting as transmitter, PIN is also set to logic 1 (inactive) each time S0 is written. In receiver mode, the PIN bit is automatically set to logic 1 (inactive) each time the data register S0 is read.

After transmission or reception of one byte on the I²C-bus (9 clock pulses, including acknowledge), the PIN bit will be automatically reset to logic 0 (active) indicating a complete byte transmission/reception. When the PIN bit is subsequently set to logic 1 (inactive), all status bits will be reset to logic 0. PIN is also set to zero on a BER (bus error) condition.

In polled applications, the PIN bit is tested to determine when a serial transmission/reception has been completed. When the ENI bit (bit 4 of write-only section of register S1) is also set to logic 1 the hardware interrupt is enabled. In this case, the PIN flag also triggers an external interrupt (active LOW) via the $\overline{INT}$ output each time PIN is reset to logic 0 (active).

When acting as slave transmitter or slave receiver, while PIN = 0, the PCF8584 will suspend I²C-bus transmission by holding the SCL line LOW until the PIN bit is set to logic 1 (inactive). This prevents further data from being transmitted or received until the current data byte in S0 has been read (when acting as slave receiver) or the next data byte is written to S0 (when acting as slave transmitter).

PIN bit summary:

- The PIN bit can be used in polled applications to test when a serial transmission has been completed. When the ENI bit is also set, the PIN flag sets the external interrupt via the $\overline{INT}$ output.
- Setting the STA bit (start bit) will set PIN = 1 (inactive).
- In transmitter mode, after successful transmission of one byte on the I²C-bus the PIN bit will be automatically reset to logic 0 (active) indicating a complete byte transmission.
- In transmitter mode, PIN is set to logic 1 (inactive) each time register S0 is written.
- In receiver mode, PIN is set to logic 0 (active) on completion of each received byte. Subsequently, the SCL line will be held LOW until PIN is set to logic 1.
- In receiver mode, when register S0 is read, PIN is set to logic 1 (inactive).
- In slave receiver mode, an I²C-bus STOP condition will set PIN = 0 (active).
- PIN = 0 if a bus error (BER) occurs.

6.8.2.2 STS

When in slave receiver mode, this flag is asserted when an externally generated STOP condition is detected (used only in slave receiver mode).

6.8.2.3 BER

Bus error; a misplaced START or STOP condition has been detected. Resets $\overline{BB}$ (to logic 1; inactive), sets PIN = 0 (active).

6.8.2.4 LRB/AD0

'Last Received Bit' or 'Address 0 (General Call) bit'. This status bit serves a dual function, and is valid only while PIN = 0:

1. LRB holds the value of the last received bit over the I²C-bus while AAS = 0 (not addressed as slave). Normally this will be the value of the slave acknowledgement; thus checking for slave acknowledgement is done via testing of the LRB.
2. AD0; when AAS = 1 ('Addressed As Slave' condition), the I²C-bus controller has been addressed as a slave. Under this condition, this bit becomes the 'AD0' bit and will be set to logic 1 if the slave address received was the 'general call' (00H) address, or logic 0 if it was the I²C-bus controller's own slave address.

6.8.2.5 AAS

'Addressed As Slave' bit. Valid only when PIN = 0. When acting as slave receiver, this flag is set when an incoming address over the I²C-bus matches the value in own address register S0' (shifted by one bit, see Section 6.4), or if the I²C-bus 'General Call' address (00H) has been received ('General Call' is indicated when AD0 status bit is also set to logic 1, see Section 6.8.2.4).

6.8.2.6 LAB

'Lost Arbitration' Bit. This bit is set when, in multi-master operation, arbitration is lost to another master on the I²C-bus.

6.8.2.7 $\overline{BB}$

'Bus Busy' bit. This is a read-only flag indicating when the I²C-bus is in use. A zero indicates that the bus is busy, and access is not possible. This bit is set/reset (logic 1/logic 0) by STOP/START conditions.

6.9 Multi-master operation

To avoid conflict between data and repeated START and STOP operations, multi-master systems have some limitations:

- When powering up multiple PCF8584s in multi-master systems, the possibility exists that one node may power up slightly after another node has already begun an I²C-bus transmission; the Bus Busy condition will thus not have been detected. To avoid this condition, a delay should be introduced in the initialization sequence of each PCF8584 equal to the longest I²C-bus transmission, see flowchart 'PCF8584 initialization' (Fig.5).

6.10 Reset

A LOW level pulse on the $\overline{RESET}$ input forces the I²C-bus controller into a well-defined state. All flags in S1 are reset to logic 0, except the PIN flag, which is set to logic 1. S0' and S3 are set to 00H.

The $\overline{RESET}$ pin is also used for the $\overline{STROBE}$ output signal. Both functions are separated on-chip by a digital filter. The reset input signal has to be sufficiently long (minimum 30 clock cycles) to pass through the filter. The $\overline{STROBE}$ output signal is sufficiently short (8 clock cycles) to be blocked by the filter. For more detailed information on the strobe function see Section 6.12.

6.11 Comparison to the MAB8400 I²C-bus interface

The structure of the PCF8584 is similar to that of the MAB8400 series of microcontrollers, but with a modified control structure. Access to all I²C-bus control and status registers is done via the parallel-bus port in conjunction with register select input A0, and control bits ESO, ES1 and ES2.

6.11.1 DELETED FUNCTIONS

The following functions are not available in the PCF8584:

- Always selected (ALS flag)
- Access to the bit counter (BC0 to BC2)
- Full SCL frequency selection (2 bits instead of 5 bits)
- The non-acknowledge mode (ACK flag)
- Asymmetrical clock (ASC flag).

6.11.2 ADDED FUNCTIONS

The following functions either replace the deleted functions or are completely new:

- Chip clock prescaler
- Assert acknowledge bit (ACK flag)
- Register selection bits (ES1 and ES2 flags)
- Additional status flags (BER, 'bus error')
- Automatic interface control between 80XX and 68000-type microcontrollers
- Programmable interrupt vector
- Strobe generator
- Bus monitor function
- Long-distance mode [non-I²C-bus mode (4-wire); only for communication between parallel-bus processors using the PCF8584 at each interface point].

6.12 Special function modes

6.12.1 STROBE

When the I²C-bus controller receives its own address (or the '00H' general call address) followed immediately by a STOP condition (i.e. no further data transmitted after the address), a strobe output signal is generated at the $\overline{RESET}/\overline{STROBE}$ pin (pin 19). The $\overline{STROBE}$ signal consists of a monostable output pulse (active LOW), 8 clock cycles long (see Fig.9). It is generated after the STOP condition is received, preceded by the correct slave address. This output can be used as a bus access controller for multi-master parallel-bus systems.

6.12.2 LONG-DISTANCE MODE

The long-distance mode provides the possibility of longer-distance serial communication between parallel processors via two I²C-bus controllers. This mode is selected by setting ES1 to logic 1 while the serial interface is enabled (ESO = 1).

In this mode the I²C-bus protocol is transmitted over 4 unidirectional lines, SDA OUT, SCL IN, SDA IN and SCL IN (pins 2, 3, 4 and 5). These communication lines should be connected to line drivers/receivers (example: RS422) for long-distance applications. Hardware characteristics for long-distance transmission are then given by the chosen standard. Control of data transmission is the same as in normal I²C-bus mode. After reading or writing data to shift register S0, long-distance mode must be initialized by setting ESO and ES1 to logic 1. Because the interrupt output $\overline{INT}$ is not available in this operating mode, synchronization of data transmission/reception must be polled via the PIN bit.

Remarks:

Before entering the long-distance mode, ENI must be set to logic 0.

When powering up an PCF8584-node in long-distance mode, the PCF8584 must be isolated from the 4-wire bus via 3-state line drivers/receivers until the PCF8584 is properly initialized for long-distance mode. Failure to implement this precaution will result in system malfunction.

6.12.3 MONITOR MODE

When the 7-bit own address register S0' is loaded with all zeros, the I²C-bus controller acts as a passive I²C monitor. The main features of the monitor mode are:

- The controller is always selected.
- The controller is always in the slave receiver mode.
- The controller never generates an acknowledge.
- The controller never generates an interrupt request.
- A pending interrupt condition does not force SCL LOW.
- $\overline{BB}$ is set to logic 0 after detection of a START condition, and reset to logic 1 after a STOP condition.
- Received data is automatically transferred to the read buffer.
- Bus traffic is monitored by the PIN bit, which is reset to logic 0 after the acknowledge bit of an incoming byte has been received, and is set to logic 1 as soon as the first bit of the next incoming byte is detected. Reading the data buffer S0 sets the PIN bit to logic 1. Data in the read buffer is valid from PIN = 0 and during the next 8 clock pulses (until next acknowledge).
- AAS is set to logic 1 at every START condition, and reset at every 9th clock pulse.

7 SOFTWARE FLOWCHART EXAMPLES

7.1 Initialization

The flowchart of Fig.5 gives an example of a proper initialization sequence of the PCF8584. When implemented in 808X-type bus systems with peripherals sharing a common $\overline{WR}$ signal, this procedure should be executed first before communicating with other bus peripherals to avoid false programming of the PCF8584 (see Section 6.2)

7.2 Implementation

The flowcharts (Figs 6 to 9) illustrate proper programming sequences for implementing master transmitter, master receive, and master transmitter, repeated start and master receiver modes in polled applications.

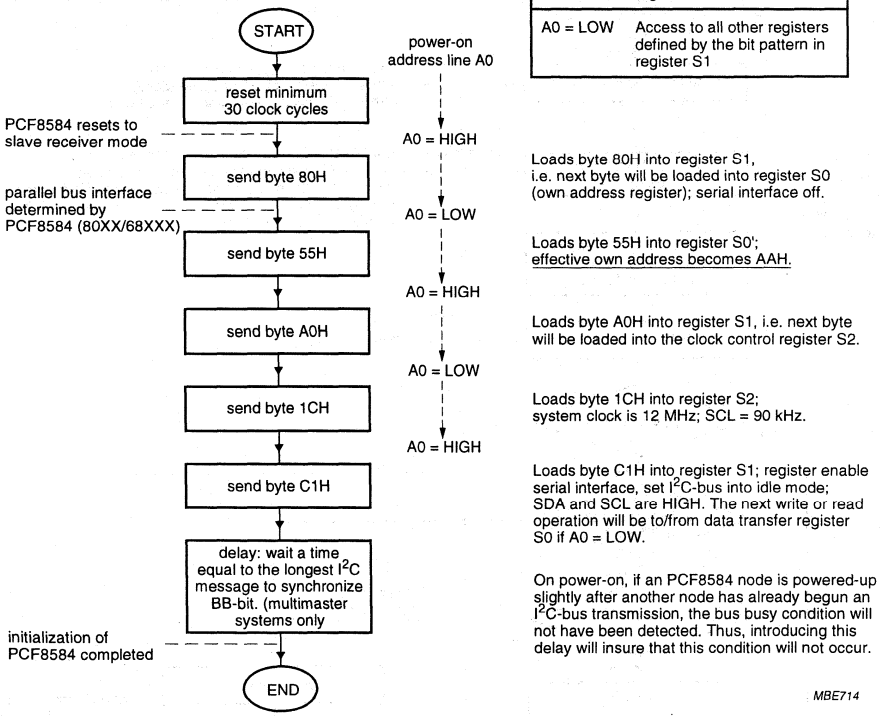


Fig.5 PCF8584 initialization sequence.

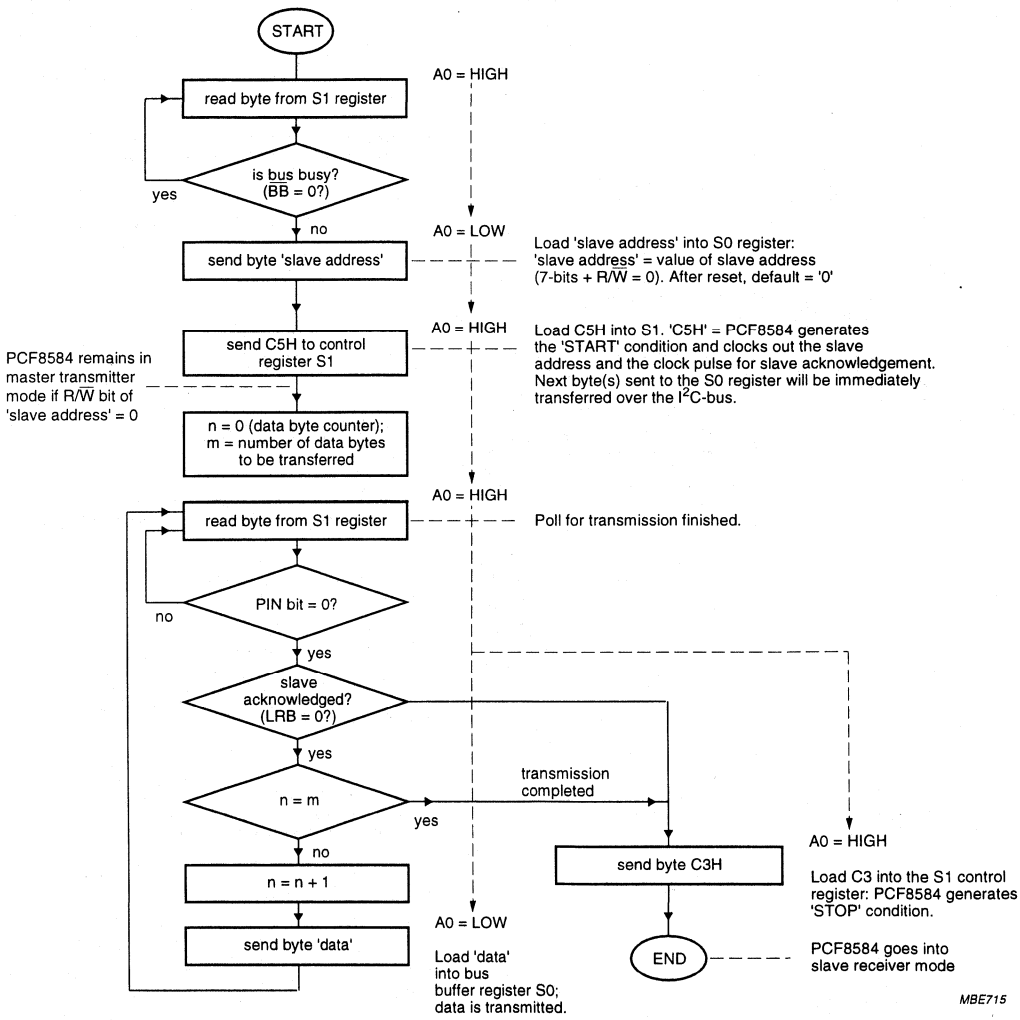


Fig.6 PCF8584 master transmitter mode.

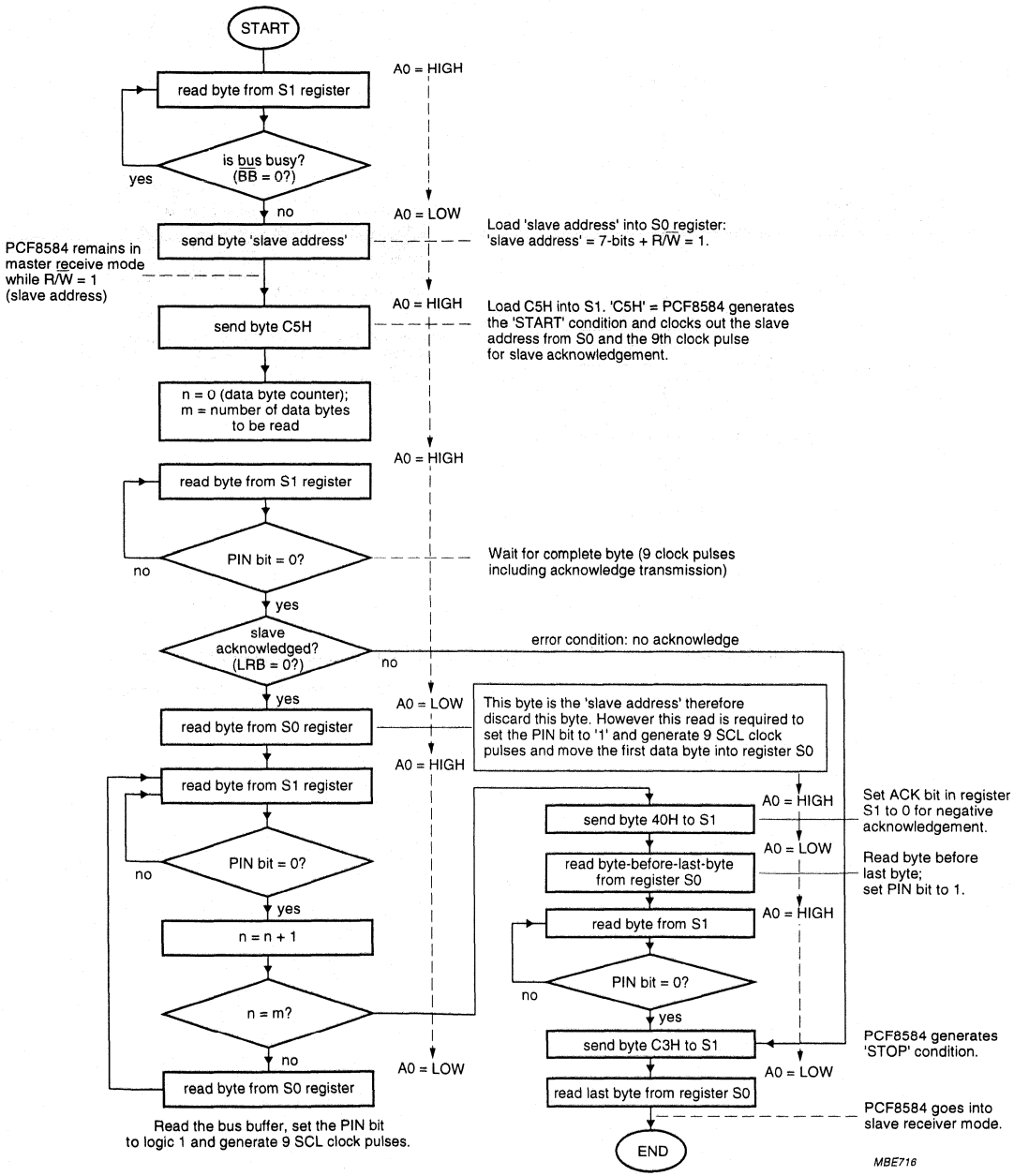


Fig.7 PCF8584 master receiver mode.

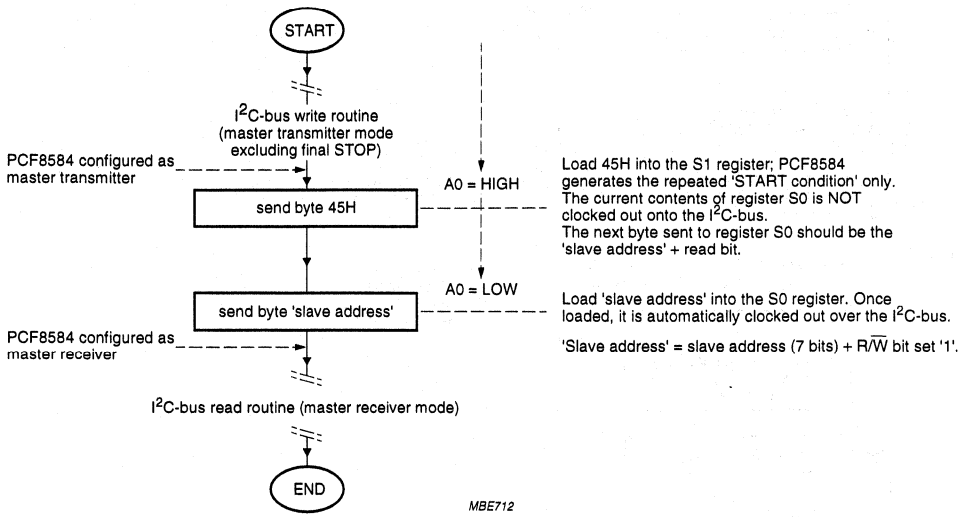


Fig.8 Master transmitter followed by repeated START and becoming master receiver.

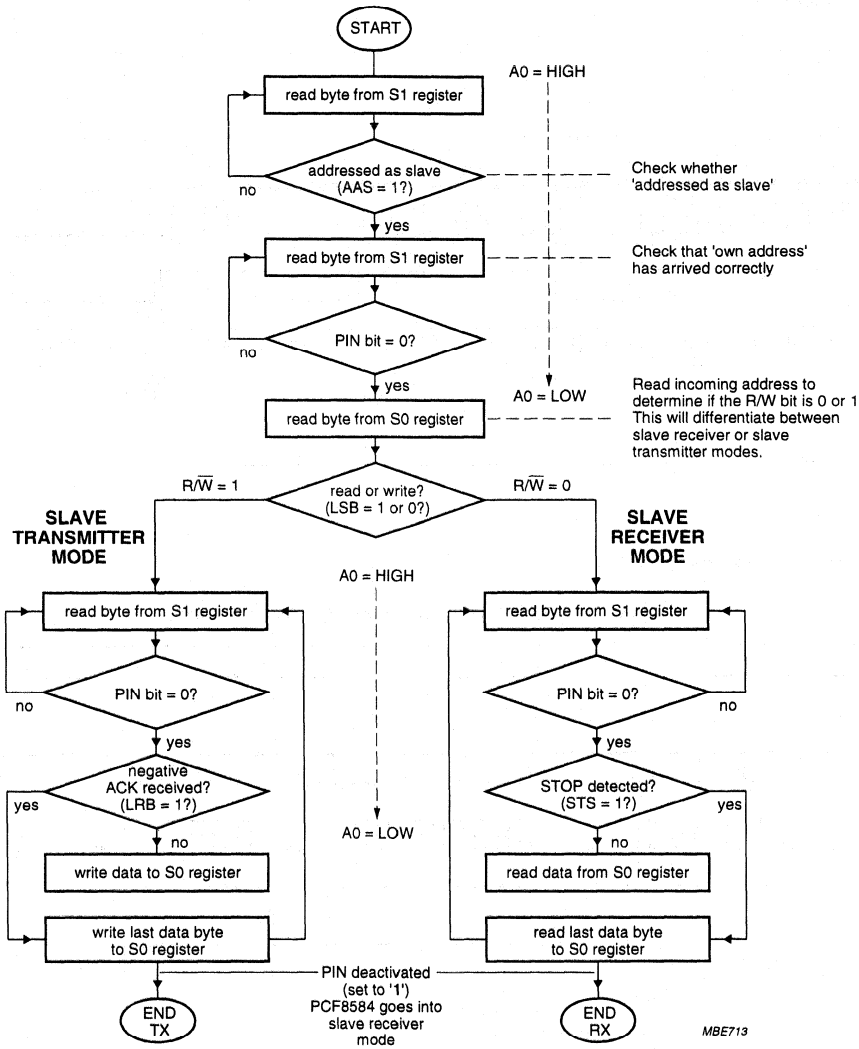
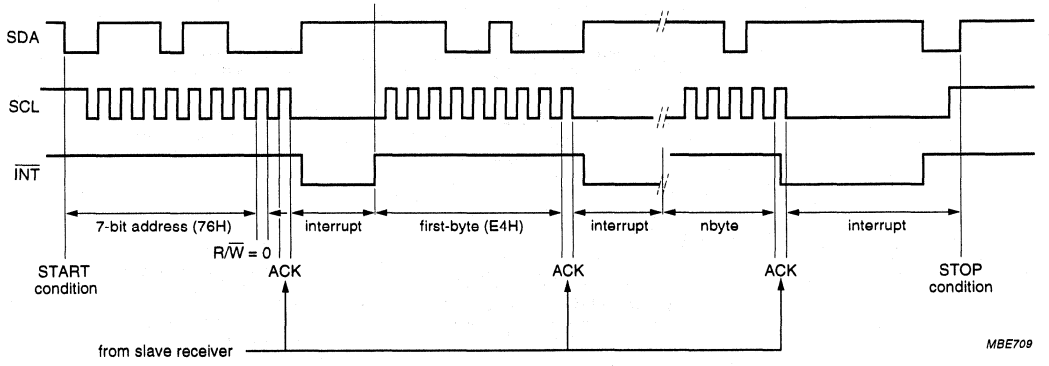


Fig.9 Slave receiver/slave transmitter modes.

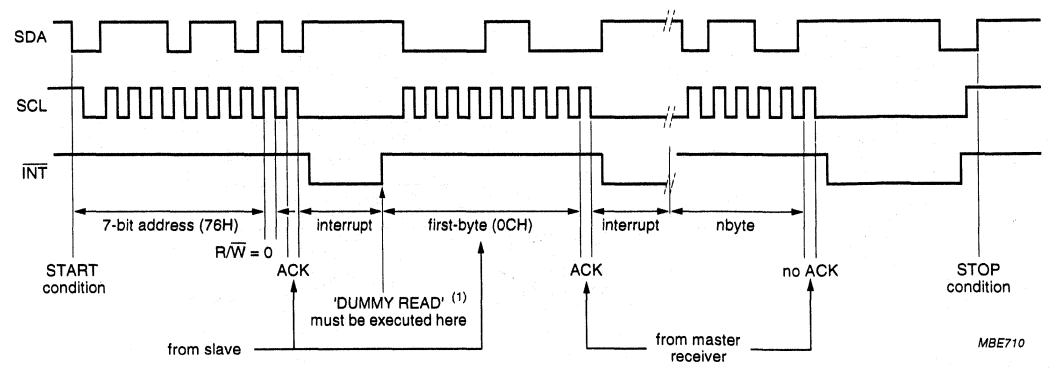
8 I²C-BUS TIMING DIAGRAMS

The diagrams (Figs 10 to 13) illustrate typical timing diagrams for the PCF8584 in master/slave functions. For detailed description of the I²C-bus protocol, please refer to *"The I²C-bus and how to use it"*; Philips document ordering number 9398 393 40011.



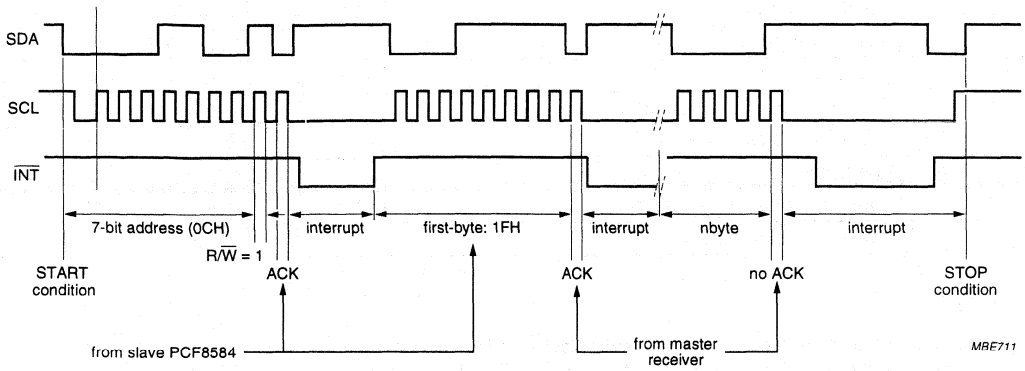
Master PCF8584 writes data to slave receiver.

Fig.10 Bus timing diagram; master transmitter mode.



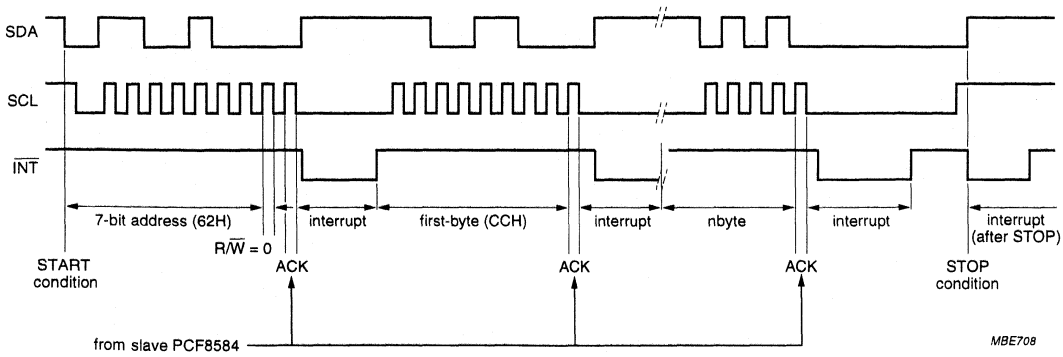
Master PCF8584 reads data from slave receiver.

Fig.11 Bus timing diagram; master receiver mode.



External master receiver reads data from PCF8584.

Fig.12 Bus timing diagram; slave transmitter mode.



Slave PCF8584 is written to by external master transmitter.

Fig.13 Bus timing diagram; slave receiver mode.

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.3	+7.0	V
V_I	voltage range (any input)	−0.8	V_{DD} + 0.5	V
I_I	DC input current (any input)	−10	+10	mA
I_O	DC output current (any output)	−10	+10	mA
P_{tot}	total power dissipation	−	300	mW
P_O	power dissipation per output	−	50	mW
T_{amb}	operating ambient temperature	−40	+85	°C
T_{stg}	storage temperature	−65	+150	°C

10 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is good practice to take normal precautions appropriate to handling MOS devices (see *"Handling MOS Devices"*).

11 DC CHARACTERISTICS

V_{DD} = 5 V ±10%; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		4.5	5.0	5.5	V
I_{DD}	supply current	standby; note 1	–	–	2.5	μA
		operating; notes 1 and 2	–	–	1.5	mA
Inputs						
CLK, $\overline{IACK}$, A0, $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{RESET}$ AND D0 to D7						
V_{IL}	LOW level input voltage	note 3	0	–	0.8	V
V_{IH}	HIGH level input voltage	note 3	2.0	–	V_{DD}	V
SDA AND SCL						
V_{IL}	LOW level input voltage	note 4	0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage	note 4	$0.7V_{DD}$	–	V_{DD}	V
R_i	resistance to V_{DD}	T_{amb} = 25 °C; note 5	25	–	100	kΩ
Outputs						
I_{OL}	LOW level output current	V_{OH} = 2.4 V; note 6	−2.4	–	–	mA
I_{OH}	HIGH level output current	V_{OL} = 0.4 V; note 6	3.0	–	–	mA
I_{OL}	leakage current	note 7	−1	–	+1	μA

Notes

1. Test conditions: 22 kΩ pull-up resistors on D0 to D7; 10 kΩ pull-up resistors on SDA, SCL, $\overline{RD}$; $\overline{RESET}$ connected to V_{SS}; remaining pins open-circuit.
2. CLK waveform of 12 MHz with 50% duty factor.
3. CLK, $\overline{IACK}$, A0, $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{RESET}$ and D0 to D7 are TTL level inputs.
4. SDA and SCL are CMOS level inputs.
5. CLK, $\overline{IACK}$, A0, $\overline{CS}$ and $\overline{WR}$.
6. D0 to D7.
7. D0 to D7 3-state, SDA, SCL, $\overline{INT}$, $\overline{RD}$, $\overline{RESET}$.

12 I²C-BUS TIMING SPECIFICATIONS

All the timing limits are valid within the operating supply voltage and ambient temperature range; V_{DD} = 5 V ±10%; T_{amb} = −40 to +85 °C; and refer to V_{IL} and V_{IH} with an input voltage of V_{SS} to V_{DD}.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
f_{SCL}	SCL clock frequency	–	–	100	kHz
t_{SW}	tolerable spike width on bus	–	–	100	ns
t_{BUF}	bus free time	4.7	–	–	µs
$t_{SU;STA}$	START condition set-up time	4.7	–	–	µs
$t_{HD;STA}$	START condition hold time	4.0	–	–	µs
t_{LOW}	SCL LOW time	4.7	–	–	µs
t_{HIGH}	SCL HIGH time	4.0	–	–	µs
t_r	SCL and SDA rise time	–	–	1.0	µs
t_f	SCL and SDA fall time	–	–	0.3	µs
$t_{SU;DAT}$	data set-up time	250	–	–	ns
$t_{HD;DAT}$	data hold time	0	–	–	ns
$t_{VD;DAT}$	SCL LOW to data out valid	–	–	3.4	µs
$t_{SU;STO}$	STOP condition set-up time	4.0	–	–	µs

13 PARALLEL INTERFACE TIMING

All the timing limits are valid within the operating supply voltage and ambient temperature range: V_{DD} = 5 V ±10%; T_{amb} = −40 to +85 °C; and refer to V_{IL} and V_{IH} with an input voltage of V_{SS} to V_{DD}. C_L = 100 pF; R_L = 1.5 kΩ (connected to V_{DD}) for open-drain and high-impedance outputs, where applicable (for measurement purposes only).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_r	clock rise time	see Fig.14	–	–	6	ns
t_f	clock fall time	see Fig.14	–	–	6	ns
t_{CLK}	input clock period (50% ±5% duty factor)	see Fig.14	83	–	333	ns
t_{CLRL}	$\overline{CS}$ set-up to $\overline{RD}$ LOW	see Fig.16 and note 1	20	–	–	ns
t_{CLWL}	$\overline{CS}$ set-up to $\overline{WR}$ LOW	see Fig.15 and note 1	20	–	–	ns
t_{RHCH}	$\overline{CS}$ hold from $\overline{RD}$ HIGH	see Fig.16	0	–	–	ns
t_{WHCH}	$\overline{CS}$ hold from $\overline{WR}$ HIGH	see Fig.15	0	–	–	ns
t_{AVWL}	A0 set-up to $\overline{WR}$ LOW	see Fig.15	10	–	–	ns
t_{AVRL}	A0 set-up to $\overline{RD}$ LOW	see Fig.16	10	–	–	ns
t_{WHAI}	A0 hold from $\overline{WR}$ HIGH	see Fig.15	20	–	–	ns
t_{RHAI}	A0 hold from $\overline{RD}$ HIGH	see Fig.16	10	–	–	ns
t_{WLWH}	$\overline{WR}$ pulse width	see Fig.15	250	–	1000	ns
t_{RLRH}	$\overline{RD}$ pulse width	see Fig.16	250	–	1000	ns
t_{DVWH}	data set-up before $\overline{WR}$ HIGH	see Fig.15	150	–	–	ns
t_{RLDV}	data valid after $\overline{RD}$ LOW	see Fig.16	–	160	230	ns
t_{WHDI}	data hold after $\overline{WR}$ HIGH	see Fig.15	20	–	–	ns
t_{RHDF}	data bus floating after $\overline{RD}$ HIGH	see Fig.16 and note 4	–	160	180	ns
t_{AVCL}	A0 set-up to $\overline{CS}$ LOW	see Figs 17 and 18	10	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{WLCL}	R/$\overline{WR}$ set-up to $\overline{CS}$ LOW	see Fig.17	10	–	–	ns
t_{RHCL}	R/$\overline{WR}$ set-up to $\overline{CS}$ LOW	see Fig.18	10	–	–	ns
t_{CLDV}	data valid after $\overline{CS}$ LOW	see Fig.18 and note 3	–	160	230	ns
t_{CLDL}	$\overline{DTACK}$ LOW after $\overline{CS}$ LOW	see Figs 17 and 18	–	$2t_{CLK}$ + 75	$3t_{CLK}$ + 150	ns
t_{CHAI}	A0 hold from $\overline{CS}$ HIGH	see Fig.18	0	–	–	ns
t_{CHRL}	R/$\overline{WR}$ hold from $\overline{CS}$ HIGH	see Fig.18	0	–	–	ns
t_{CHWH}	R/$\overline{WR}$ hold from $\overline{CS}$ HIGH	see Fig.17	0	–	–	ns
t_{CHDF}	data bus float after $\overline{CS}$ HIGH	see Fig.18 and note 4	–	160	180	ns
t_{CHDE}	$\overline{DTACK}$ HIGH from $\overline{CS}$ HIGH	see Figs 17 and 18	–	100	120	ns
t_{CHDI}	data hold after $\overline{CS}$ HIGH	see Fig.17 and note 4	0	–	–	ns
t_{DVCL}	data set-up to $\overline{CS}$ LOW	see Fig.17	0	–	–	ns
t_{ALIE}	$\overline{INT}$ HIGH from $\overline{IACK}$ LOW	see Figs 19 and 20	–	130	180	ns
t_{ALDV}	data valid after $\overline{IACK}$ LOW	see Figs 19 and 20	–	200	250	ns
t_{ALAE}	$\overline{IACK}$ pulse width	see Fig.20	280	–	–	ns
t_{AHDI}	data hold after $\overline{IACK}$ HIGH	see Fig.20	–	–	150	ns
t_{ALDL}	$\overline{DTACK}$ LOW from $\overline{IACK}$ LOW	see Fig.20	–	$2t_{CLK}$ + 75	$3t_{CLK}$ + 150	ns
t_{AHDE}	$\overline{DTACK}$ HIGH from $\overline{IACK}$ HIGH	see Fig.20	–	120	140	ns
t_{W4}	$\overline{RESET}$ pulse width	see Fig.21	$30t_{CLK}$	–	–	ns
t_{W5}	$\overline{STROBE}$ pulse width	see Fig.22	$8t_{CLK}$	$8t_{CLK}$ + 90	–	ns
t_{CLCL}	$\overline{CS}$ LOW	see Figs 17 and 18	–	t_{CLDL} + t_{CHDE}	–	ns

Notes

1. A minimum of 6 clock cycles must elapse between consecutive parallel-bus accesses when the I²C-bus controller operates at 8 or 12 MHz. This may be reduced to 3 clock cycles for lower operating frequencies.
2. After reset the chip clock default is 12 MHz.
3. Not for S1.
4. Not tested.

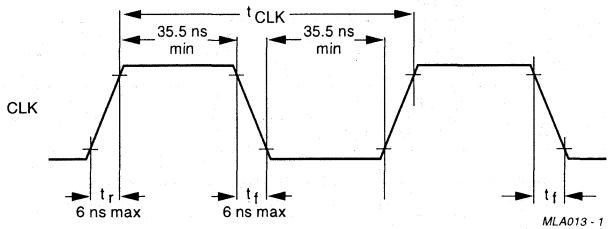


Fig.14 Clock input timing.

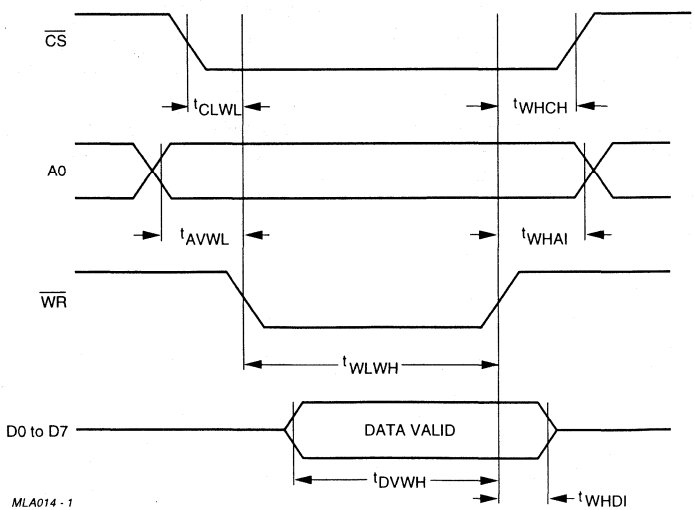


Fig.15 Bus timing (80XX mode); write cycle.

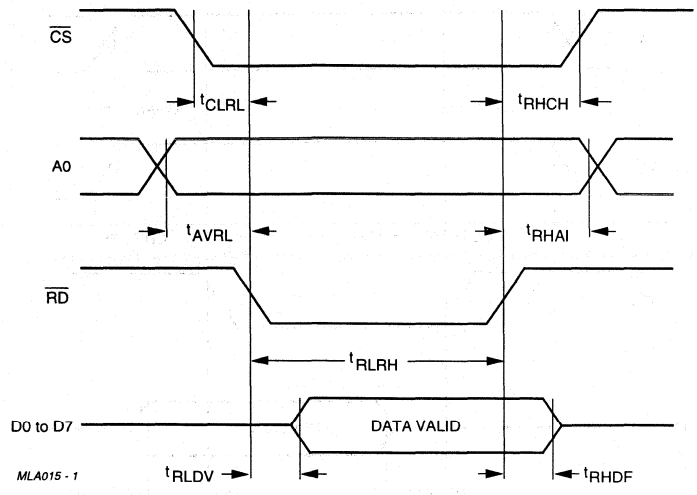


Fig.16 Bus timing (80XX mode); read cycle.

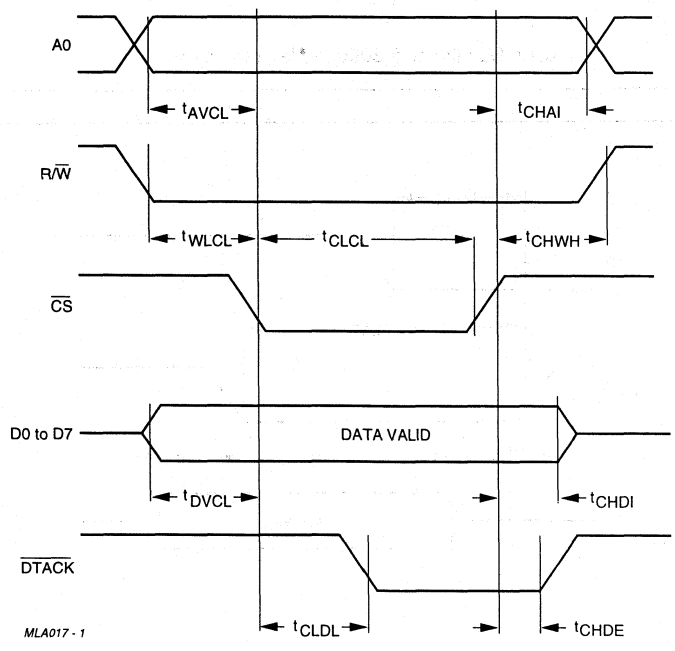


Fig.17 Bus timing (68000 mode); write cycle.

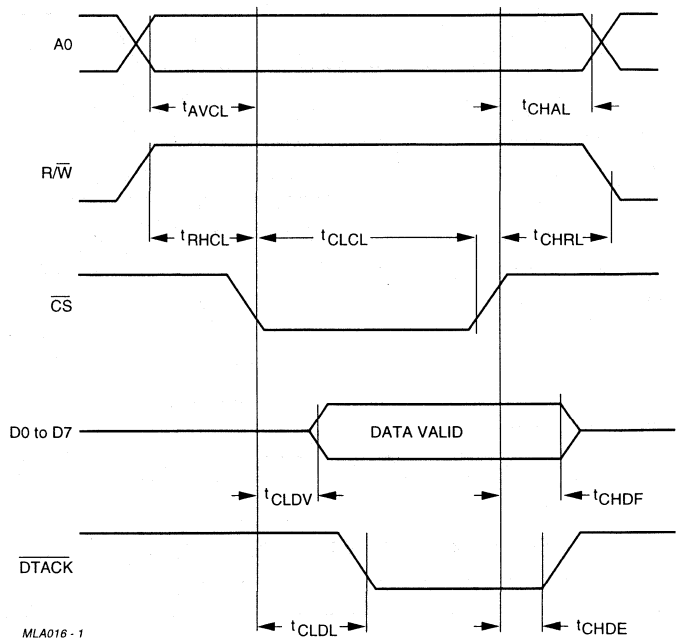


Fig.18 Bus timing (68000 mode); read cycle.

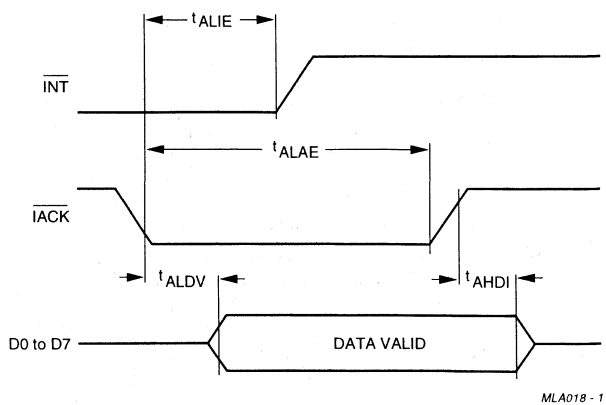


Fig.19 Interrupt timing (80XX mode).

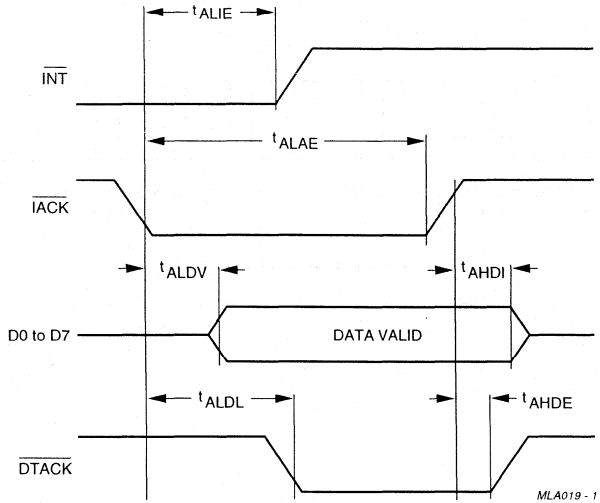


Fig.20 Interrupt timing (68000 mode).

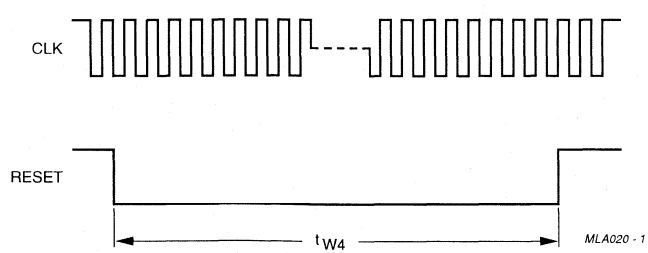


Fig.21 Reset timing.

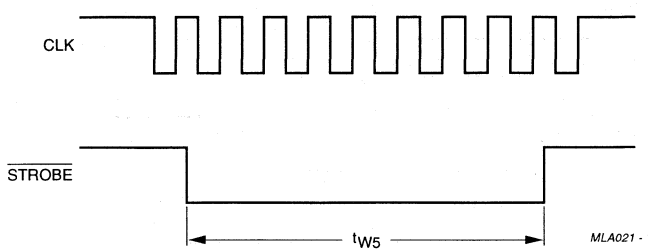


Fig.22 Strobe timing.

14 APPLICATION INFORMATION

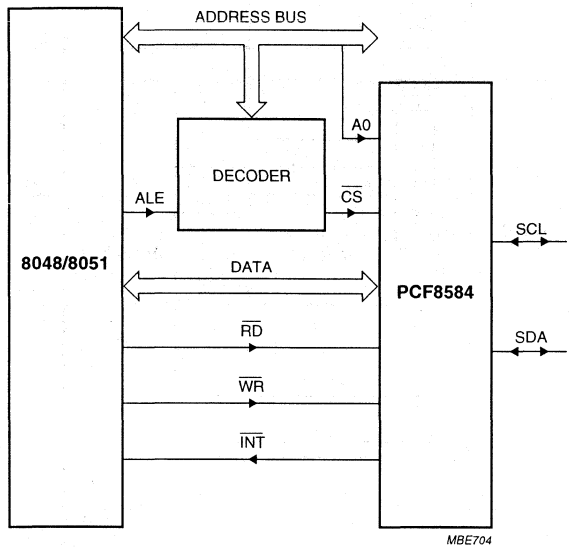


Fig.23 Application diagram using the 8048/8051.

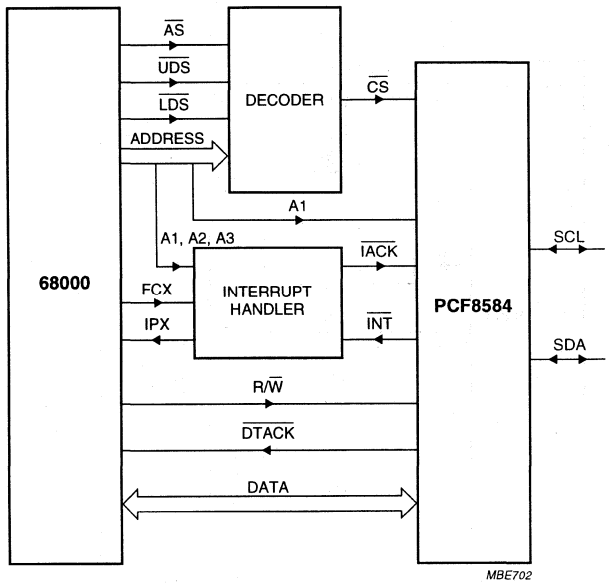


Fig.24 Application diagram using the 68000.

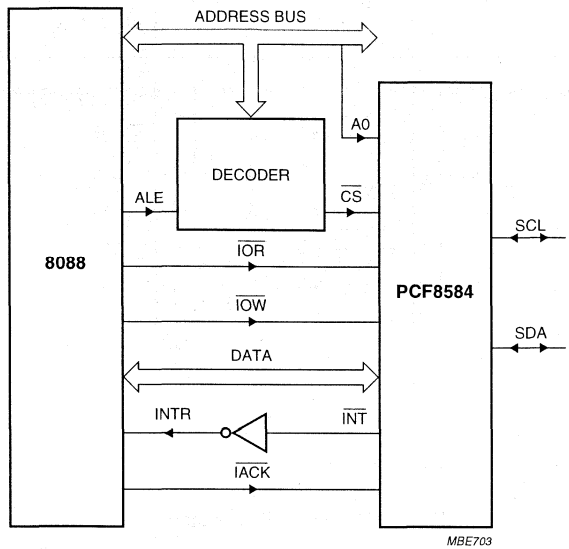
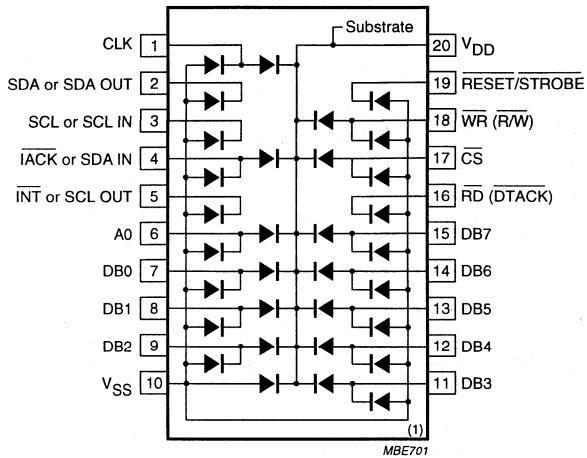


Fig.25 Application diagram using the 8088.

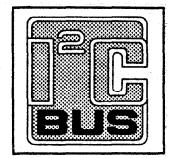


Maximum forward current: 5 mA; maximum reverse voltage: 5 V.

Fig.26 PCF8584 diode protection.

Integrated VIP and Teletext (IVT1.0)

SAA5246A



FEATURES

- Complete Teletext decoder in a 48-pin DIL, 52-pin shrink DIL, or 64-pin QFP, integrated circuit
- Single +5 V power supply
- Both video and scan related synchronization modes are supported
- RGB interface to standard colour decoder ICs, push-pull output drive
- Digital data slicer and display clock phase-locked loop reduce peripheral components to a minimum
- Data capture performance similar to SAA5231 (VIP2)
- Option for up to seven national languages
- Optional storage of packet 24 in the display memory
- Separate text and video signal quality detectors, 625/525 video status and language version all readable via I²C-bus
- Automatic $\overline{ODD}$/EVEN output control with override
- Control of display PLL free-run and rolling header via I²C-bus
- VCS to SCS mode for stable 525 line status display.

DESCRIPTION

The SAA5246A is a single-chip teletext decoder IC for decoding 625 line base World System Teletext transmissions. The teletext decoder hardware is based on the Enhanced Computer Controlled ECCT device (SAA5243) with some additional features.
The Video Input Processor section of the device uses mixed analog and digital designs in the data slicer and clock phase-locked-loop functions. As a result the number of external components are greatly reduced and no critical or adjustable components are required.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage	4.5	5.0	5.5	V
I_{DD}	supply current	–	64	128	mA
V_{syn}	sync amplitude	0.1	0.3	0.6	V
V_{vid}	video amplitude	0.7	1.0	1.4	V
f_{XTAL}	crystal frequency	–	27	–	MHz
T_{amb}	operating ambient temperature	−20	–	+70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA5246AP	48	DIL	plastic	SOT240A
SAA5246AZP	52	shrink DIL	plastic	SOT247
SAA5246AGP	64	QFP	plastic	SOT208A

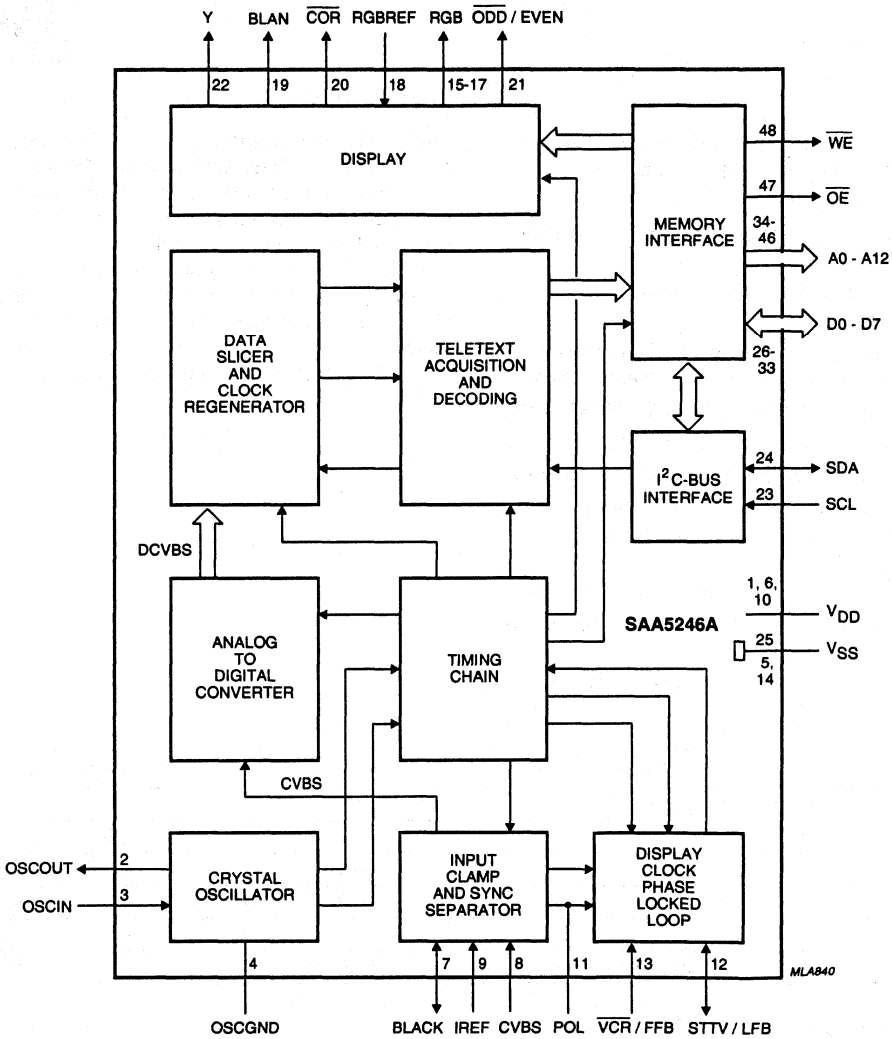


Fig.1 Block diagram for SOT240 (DIL48) package.

PINNING

SYMBOL	PIN			DESCRIPTION
	SOT240	SOT247	SOT208	
OSCOUT	2	1	27	27 MHz crystal oscillator output
OSCIN	3	2	28	27 MHz crystal oscillator input
OSCGND	4	3	29	0 V crystal oscillator ground
V_{SS}	5, 14, 25	4, 5, 15, 26	26, 30, 31, 43, 58	0 V ground
BLACK	7	8	35	video black level storage pin, connected to ground via a 100 nF capacitor
CVBS	8	9	36	composite video input pin. A positive-going 1 V (peak-to-peak) input is required, connected via a 100 nF capacitor
IREF	9	10	37	reference current input pin, connected to ground via a 27 kΩ resistor
V_{DD}	1, 6, 10	6, 11, 52	25, 32, 38	+5 V positive supply
POL	11	12	39	STTV/LFB/FFB polarity selection pin
STTV/LFB	12	13	40	sync to TV output pin/line flyback input pin. Function controlled by an internal register bit (scan sync mode)
$\overline{\text{VCR}}$/FFB	13	14	42	PLL time constant switch/field input pin. Function controlled by an internal register bit (scan sync mode)
R	15	16	44	dot rate character output of the RED colour information
G	16	17	45	dot rate character output of the GREEN colour information
B	17	18	47	dot rate character output of the BLUE colour information
RGBREF	18	19	48	input DC voltage to define the output high level on the RGB pins
BLAN	19	20	52	dot rate fast blanking output
$\overline{\text{COR}}$	20	21	53	programmable output to provide contrast reduction of the TV picture for mixed text and picture displays or when viewing newsflash/subtitle pages. Open-drain output
$\overline{\text{ODD}}$/EVEN	21	22	54	a 25 Hz output synchronized to the input CVBS field sync pulses to make a non-interlaced display by adjustment of the vertical deflection currents.
Y	22	23	55	dot rate character output of teletext foreground colour information. Open-drain output
SCL	23	24	56	serial clock input for I²C-bus. It can still be driven HIGH during power-down of the device
SDA	24	25	57	serial data port for the I²C-bus. Open drain output. It can still be driven HIGH during power-down of the device
D0-D5	26-31	27-32	60-64, 3	data ports for the page SRAM
n.c.	–	7, 33, 34	1, 2, 10, 11, 15, 18, 33, 34, 41, 46, 49 - 51, 59	not connected

SYMBOL	PIN			DESCRIPTION
	SOT240	SOT247	SOT208	
D6-D7	32, 33	35, 36	4, 5	data ports for the page SRAM
A0-A12	34-46	37-49	6-9, 12-14, 16, 17, 19-22	address output for the page SRAM
$\overline{OE}$	47	50	23	output enable for the page SRAM
$\overline{WE}$	48	51	24	write enable for the page SRAM

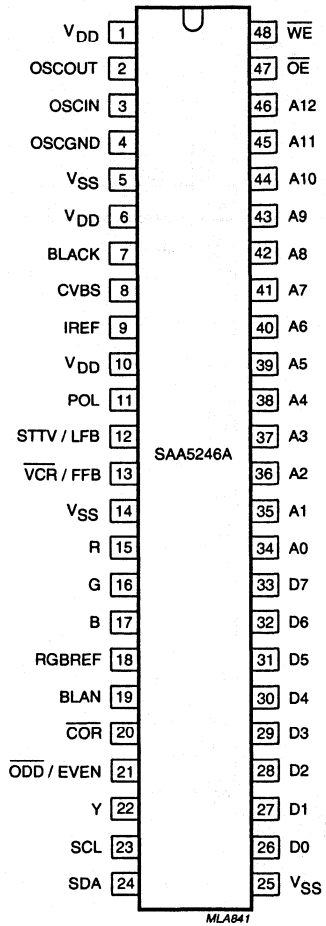


Fig.2 Pin configuration; SOT240 (DIL48).

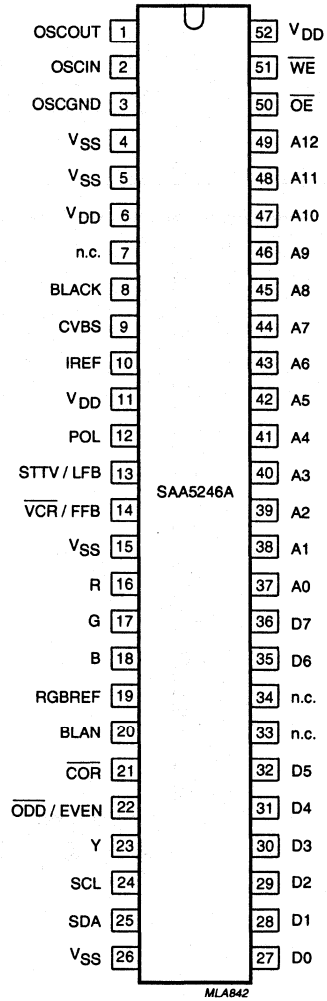


Fig.3 Pin configuration; SOT247 (SDIL52).

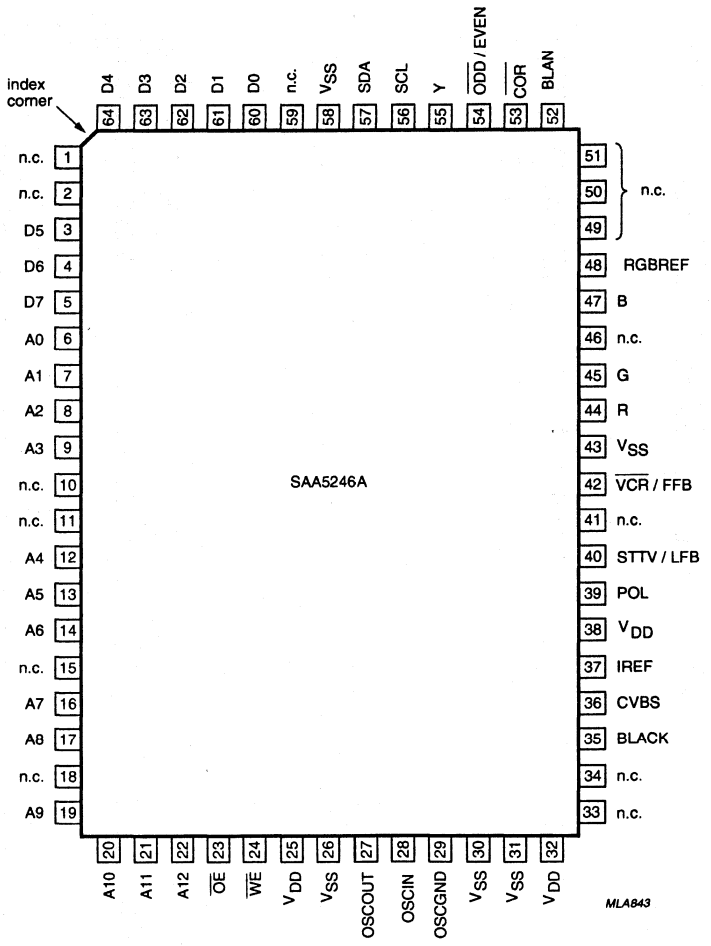


Fig.4 Pin configuration; SOT208 (QFP64).

Integrated VIP and teletext with Background Memory Controller (IVT1.1BMCX)

SAA5249

FEATURES

- Complete teletext decoder featuring a background memory controller in a single 48-pin DIP package. Capable of storing of up to 512 teletext pages in an external DRAM, giving instant access to the teletext data
- Automatic processing of extension packet 26 for widest possible language decoding. All our standard language options can be available, and the language option is readable via I²C-bus.
- 100% hardware compatible with the SAA5247 plug-in replacement and with the possibility of extra market in those countries with packet 26 transmissions. Still pin-aligned to SAA5254 and SAA5244A.
- 100% software compatible with the SAA5247, and SAA5244A, except if the special OSD symbols were used. Also 100% software compatible to SAA5254. In all events there is a change to the ROM ID number.
- The device is pin-aligned with the other members of the new Philips teletext decoder family, i.e. SAA5281 and the SAA5254, making one hardware solution for the whole range
- Low software overhead for the microprocessor
- RGB interface to standard colour decoder ICs, push-pull output drive.

GENERAL DESCRIPTION

The Integrated VIP and Teletext (IVT1.1BMCX) is a teletext decoder (contained within a single chip package) for decoding 625-line based World System Teletext transmissions. With its built-in background memory controller the device can store incoming teletext packets in the external 1M4 DRAM. With this large packet store which can be rapidly scanned, we can achieve near instantaneous access to all the pages transmitted by the broadcaster.

This version of the decoder also contains some extra hardware to process extension packet 26 automatically, extending the markets to which the TV chassis can be shipped and offering many more language options for the set maker.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	4.5	5.0	5.5	V
I_{DD}	supply current	–	90	120	mA
V_{syn}	sync amplitude	0.1	0.3	0.6	V
V_{vid}	video amplitude	0.7	1.0	1.4	V
f_{XTAL}	crystal frequency	–	27	–	MHz
T_{amb}	operating ambient temperature	–20	–	+70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA5249P/E	DIP48	plastic dual in-line package; 48 leads (600 mil)	SOT240-1
SAA5249GP/E	QFP64	plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 × 20 × 2.7 mm; high stand-off height	SOT319-1

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC02 OR DATA SHEET

BLOCK DIAGRAM

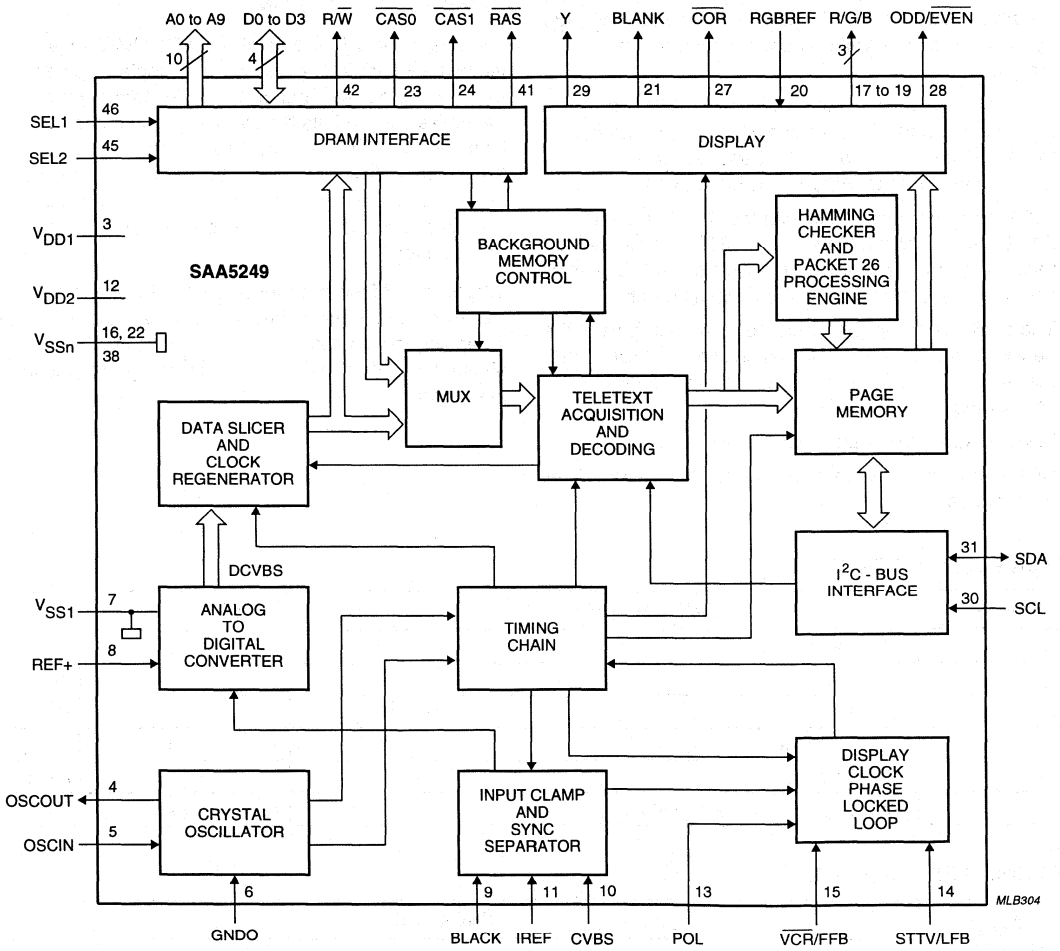


Fig.1 Block diagram for SOT240-1 (DIP48) package.

PINNING

SYMBOL	PIN		DESCRIPTION
	SOT240-1	SOT319-1[1]	
n.c.	1	1	not connected
n.c.	2	2	not connected
V_{DD1}	3	25	+5 V supply
OSCOUT	4	27	27 MHz crystal oscillator output
OSCIN	5	28	27 MHz crystal oscillator input
GNDO	6	29	0 V crystal oscillator ground
V_{SS1}	7	12	0 V ground
REF+	8	32	positive reference voltage; this pin should be connected to ground via a 100 nF capacitor
BLACK	9	35	video black level storage pin; this pin should be connected to ground via a 100 nF capacitor
CVBS	10	36	composite video input pin; a positive-going 1 V (p-p) input is required, connected via a 100 nF capacitor
IREF	11	37	reference current input pin; connected to ground via a 27 kΩ resistor
V_{DD2}	12	38	+5 V supply
POL	13	39	STTV/LFB/FFB polarity selection pin
STTV/LFB	14	40	sync to TV output pin/line flyback input pin; function controlled by an internal register bit (scan sync mode)
$\overline{VCR}$/FFB	15	42	PLL time constant switch/field input pin; function controlled by an internal register bit (scan sync mode)
V_{SS2}	16	30	0 V ground
REF–	–	31	negative reference voltage; this pin should be connected to REF+ via a 100 nF capacitor
R	17	49	dot rate character output of the RED colour information
G	18	50	dot rate character output of the GREEN colour information
B	19	51	dot rate character output of the BLUE colour information
RGBREF	20	52	input DC voltage to define the output high level on the RGB pins
BLANK	21	53	dot rate fast blanking output
V_{SS3}	22	54, 55	0 V ground; internally connected for SOT319
$\overline{CAS0}$	23	56	column address select to external DRAM for BMCX function
$\overline{CAS1}$	24	57	column address select to external DRAM for BMCX function for second DRAM where two 256 k × 4 devices are used
A4	25	58	address output to external DRAM for BMCX function
A3	26	59	address output to external DRAM for BMCX function
$\overline{COR}$	27	60	programmable output to provide contrast reduction of the TV picture for mixed text and picture displays or when viewing newsflash/subtitle pages; open drain output
ODD/$\overline{EVEN}$	28	61	25 Hz output synchronized with the CVBS input field sync pulses to produce a non-interlaced display by adjustment of the vertical deflection currents

SYMBOL	PIN		DESCRIPTION
	SOT240-1	SOT319-1[1]	
Y	29	62	dot rate character output of teletext foreground colour information; open drain output
SCL	30	63	serial clock input for I²C-bus; it can still be driven HIGH during power-down of the device
SDA	31	64	serial data port for the I²C-bus; open drain output. It can still be driven HIGH during power-down of the device
A5	32	4	address output to external DRAM for BMCX function
A2	33	5	address output to external DRAM for BMCX function
A6	34	6	address output to external DRAM for BMCX function
A1	35	8	address output to external DRAM for BMCX function
A7	36	9	address output to external DRAM for BMCX function
A0	37	11	address output to external DRAM for BMCX function
V_{SS4}	38	43	0 V ground
A8	39	13	address output to external DRAM for BMCX function
A9	40	14	address output to external DRAM for BMCX function
$\overline{RAS}$	41	15	row address select to external DRAM
R/$\overline{W}$	42	18	read/$\overline{write}$ for external DRAM
D2	43	19	data input/output for external DRAM
D0	44	20	data input/output for external DRAM
SEL2	45	21	RAM select input to choose external DRAM size
SEL1	46	22	RAM select input to choose external DRAM size
D3	47	23	data input/output for external DRAM
D1	48	24	data input/output for external DRAM

Note

1. The remaining pins for SOT319 are not connected.

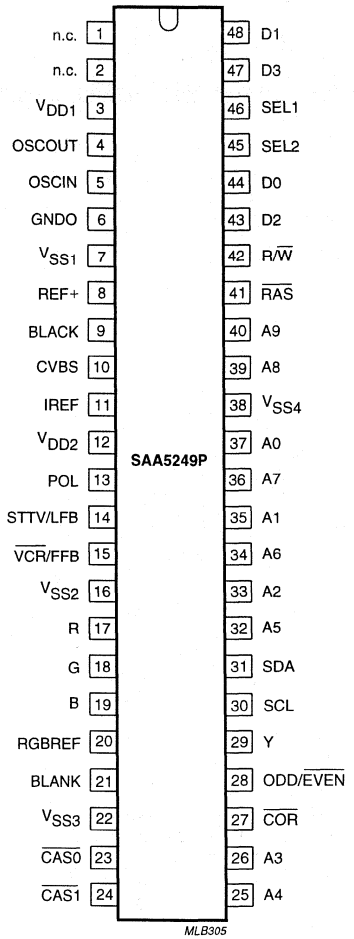


Fig.2 Pin configuration; SOT240-1 (DIP48).

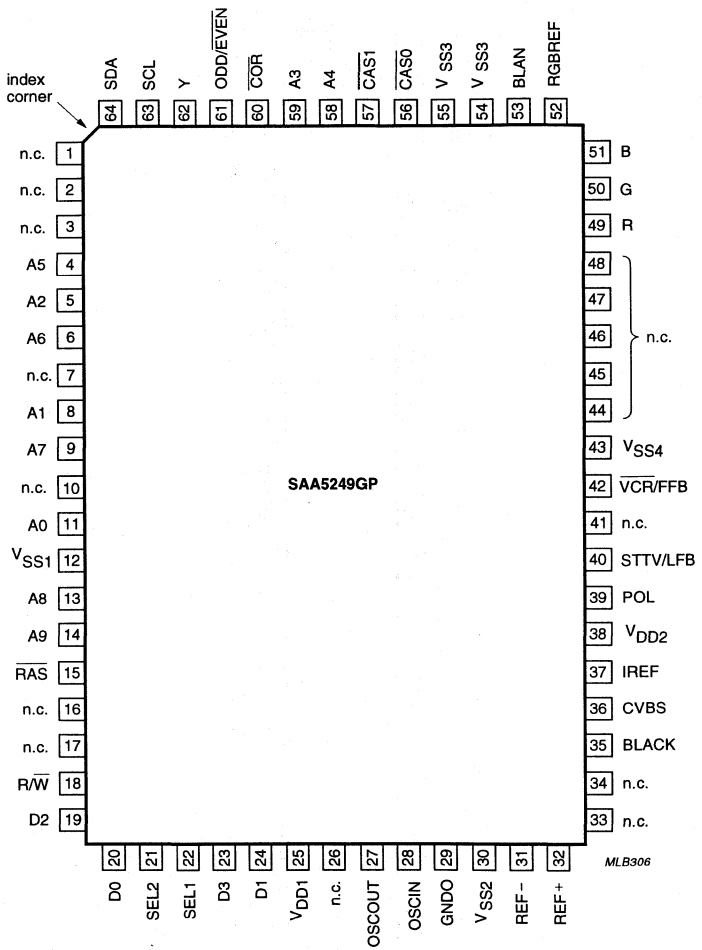


Fig.3 Pin configuration; SOT319-1 (QFP64).

Line twenty-one acquisition and display (LITOD)

SAA5252

FEATURES

- Complete 'stand-alone' Line 21 decoder in one package
- On-chip display RAM allowing full page Text mode
- Enhanced character display modes
- Full colour captions
- RGB interface for standard colour decoder ICs
- Automatic handling of Field 2 data
- Automatic selection of (1H, 1V), (2H, 1V) or (2H, 2V) scan modes
- Onboard OSD facility using Character generator
- RGB inputs to support existing OSD ICs
- I^2C-bus or 'stand-alone' pin control
- Automatic data-ready signal generation on data acquisition
- Can decode signals recorded on standard VHS and S-VHS tape.

GENERAL DESCRIPTION

The SAA5252 (LITOD) is a single-chip CMOS device, which will acquire, decode and display Line 21 Closed Captioning data from a 525-line composite video signal. Operation as an On-Screen Display (OSD) device is also possible. Normal and line progressive scan modes are supported.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	4.5	5.0	5.5	V
I_{DD}	supply current	–	30	–	mA
V_{syn}	CVBS sync amplitude	0.1	0.3	0.6	V
V_{vid}	CVBS video amplitude	0.7	1.0	1.4	V
T_{amb}	operating ambient temperature	–20	–	+70	°C
T_{stg}	storage temperature	–55	–	+125	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA5252P	DIP24	plastic dual in-line package; 24 leads (600 mil)	SOT101-1
SAA5252T	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC02 OR DATA SHEET

BLOCK DIAGRAM

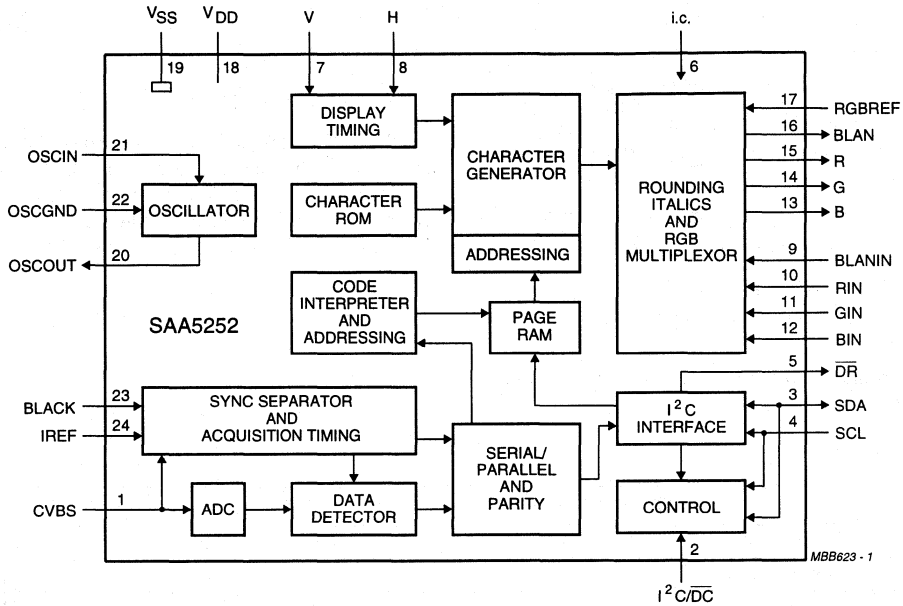


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
CVBS	1	composite video input; signal should be connected via a 100 nF capacitor
$I^2C/\overline{DC}$	2	input selects I^2C or Direct Control
SDA	3	serial data port for I^2C-bus or mode select input for direct control
SCL	4	serial clock input for I^2C-bus or mode select input for direct control
$\overline{DR}$	5	data-ready signal to microcontroller (active-LOW) or mode select input for direct control
i.c.	6	internally connected; connect to V_{SS} for normal operation
V	7	vertical reference input for display timing
H	8	horizontal reference input for display timing
BLANIN	9	video blanking input from external OSD device
RIN	10	RED video input from external OSD device
GIN	11	GREEN video input from external OSD device
BIN	12	BLUE video input from external OSD device
B	13	BLUE video output
G	14	GREEN video output
R	15	RED video output
BLAN	16	video blanking output
RGBREF	17	input voltage defining output HIGH level for RGB pins for closed captioning output
V_{DD}	18	+5 V supply
V_{SS}	19	0 V ground
OSCOUT	20	oscillator output
OSCIN	21	oscillator input
OSCGND	22	oscillator ground
BLACK	23	video black level storage input; connected to V_{SS} via 100 nF capacitor
IREF	24	reference current input; connected to V_{SS} via 27 kΩ resistor

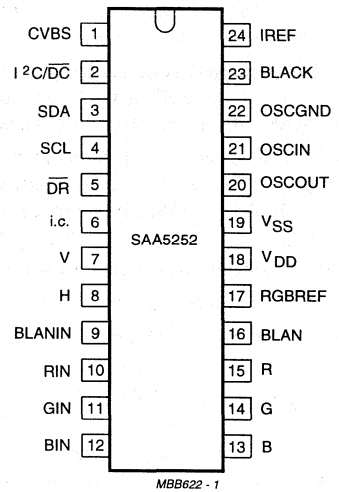


Fig.2 Pin configuration.

Integrated VIP and teletext decoder (IVT1.1X)

SAA5254

FEATURES

- Complete teletext decoder including page memory and FASTEXT links in a 40-pin DIP package
- Automatic processing of extension packet 26 for widest possible language decoding. All our standard language options can be available, and language option is readable via I²C-bus
- 100% hardware compatible with the SAA5244A; plug-in replacement and extra market
- 100% hardware compatible with the SAA5244A, except if the special OSD symbols were used with the SAA5244A, except ROM identification number
- The device is pin-aligned with the other members of the new Philips teletext decoder family, i.e. SAA5280 and the SAA5249, making one hardware solution for the full range
- Low software overhead for the control microprocessor
- Single page acquisition system
- RGB interface to standard colour decoder ICs, push-pull output drive
- Separate text and video signal quality detectors.

DESCRIPTION

The Integrated VIP and Teletext decoder (IVT1.1X) is designed to decode 625-line based World System Teletext transmissions. This single-chip teletext decoder hardware is based on the SAA5244A with which it is completely compatible.

Like the SAA5244A the device contains all the hardware necessary to decode the teletext, but the SAA5254 also contains extra hardware to process the extension packet 26 characters automatically, extending the markets to which the TV chassis can be shipped and opening the possibility of many more language options.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA5254P	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	4.5	5.0	5.5	V
I_{DD}	supply current	–	90	120	mA
V_{sync}	sync voltage amplitude	0.1	0.3	0.6	V
V_{video}	video voltage amplitude	0.7	1.0	1.4	V
f_{XTAL}	crystal frequency	–	27	–	MHz
T_{amb}	operating ambient temperature	−20	–	+70	°C

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC02 OR DATA SHEET

BLOCK DIAGRAM

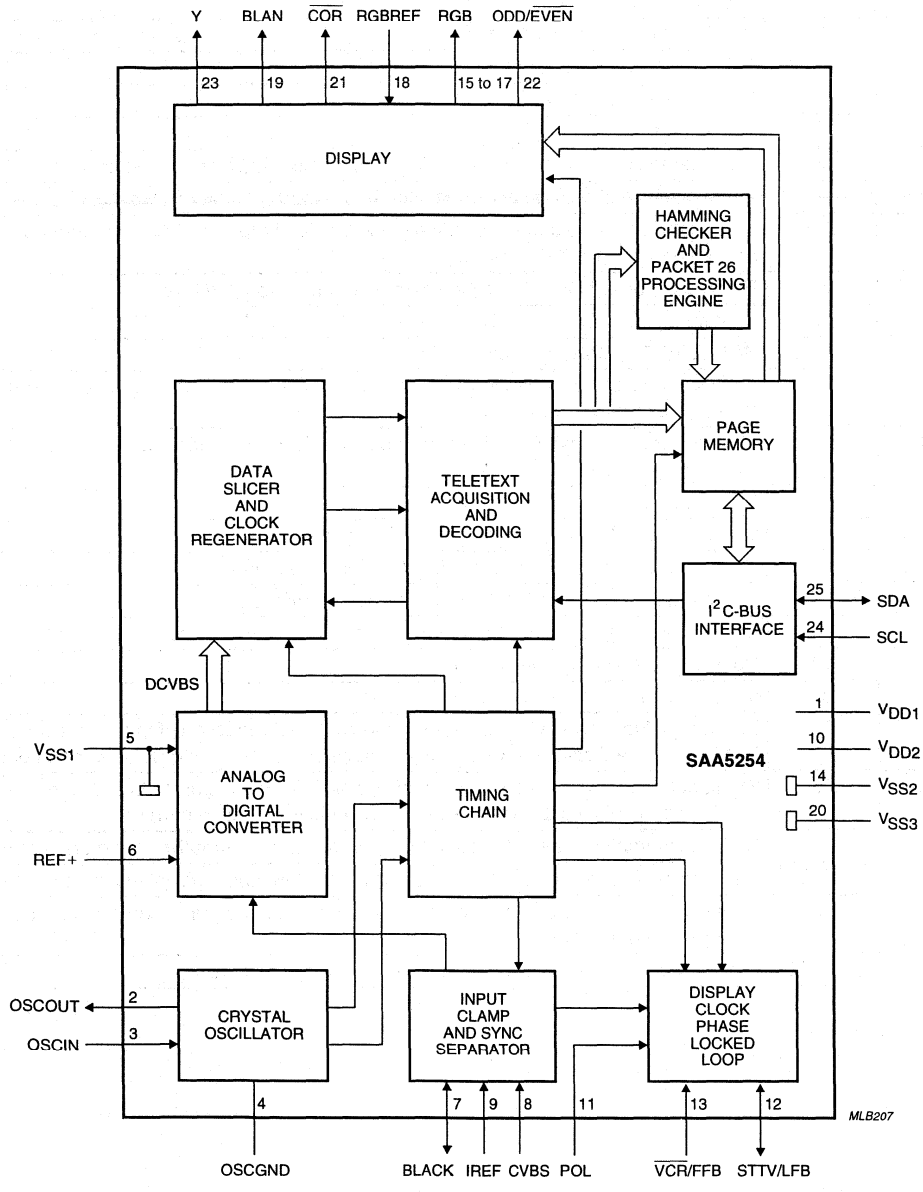


Fig.1 Block diagram; SOT129 (DIP40).

PINNING

SYMBOL	PIN	DESCRIPTION
V_{DD1}	1	+5 V supply 1
OSCOUT	2	27 MHz crystal oscillator output
OSCIN	3	27 MHz crystal oscillator input
OSCGND	4	0 V crystal oscillator ground
V_{SS1}	5	0 V ground 1
REF+	6	Positive reference voltage for the ADC. This pin should be connected to +5 V.
BLACK	7	Video black level storage pin, connected to ground via a 100 nF capacitor.
CVBS	8	Composite video input pin. A positive-going 1 V (peak-to-peak) input is required, connected via a 100 nF capacitor.
IREF	9	Reference current input pin, connected to ground via a 27 kΩ resistor.
V_{DD2}	10	+5 V supply 2
POL	11	STTV/LFB/FFB polarity selection pin
STTV/LFB	12	Sync to TV output pin/line flyback input pin. Function controlled by an internal register bit (scan sync mode).
$\overline{VCR}$/FFB	13	PLL time constant switch/field flyback input pin. Function controlled by an internal register bit (scan sync mode).
V_{SS2}	14	0 V ground 2
R	15	Dot rate character output of the RED colour information.
G	16	Dot rate character output of the GREEN colour information.
B	17	Dot rate character output of the BLUE colour information.
RGBREF	18	DC input voltage to define the output high level on the RGB pins.
BLAN	19	Dot rate fast blanking output.
V_{SS3}	20	0 V ground 3
$\overline{COR}$	21	Programmable active LOW output to provide contrast reduction of the TV picture for mixed text and picture displays or when viewing newsflash/subtitle pages; open drain output.
ODD/$\overline{EVEN}$	22	25 Hz output synchronized with the CVBS inputs field sync pulses to produce a non-interlaced display by adjustment of the vertical deflection currents.
Y	23	Dot rate character output of teletext foreground colour information; open drain output.
SCL	24	Serial clock input for the I^2C-bus. It can still be driven during power-down of the device.
SDA	25	Serial input/output data port for the I^2C-bus; open drain output. It can still be driven during power-down of the device.
i.c.	26 to 40	Internally connected. Must be left open-circuit in application.

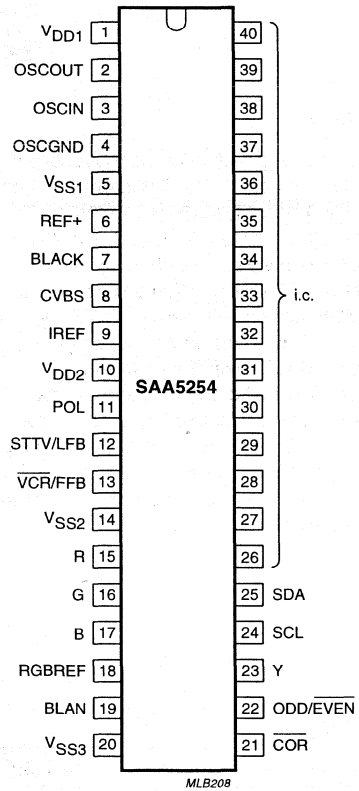


Fig.2 Pin configuration; SOT129 (DIP40).

Integrated Video input processor and Teletext decoder (IVT1.8*)

SAA5281

FEATURES

- Complete Teletext and VPS decoding in a single package
- Built-in 8K × 8 memory for up to 8 page storage
- Enhanced mode allows 7 Fastext pages and 8 pages of TOP to be captured
- Ability to request only subtitle pages
- Acquisition and decoding of VPS data
- Data valid output available to indicate reception of error-free VPS or packet 8/30/2 data
- Software and hardware compatible with SAA5246 and SAA5248
- Meshing display within boxes
- Separate data checking algorithms and pointers for each acquisition channel
- 24 : 18 Hamming checker
- Automatic packet 26 extension character processing
- Indication of Line 23 for external use
- 13.5 MHz clock output to drive external microcontroller
- Detection of Spanish transmissions to disable flicker-stopper
- Compatible with Philips' one-chip TV IC (TDA836X) for scan-locking applications.

DESCRIPTION

The IVT1.8* is a single-chip Teletext decoder IC for decoding 625-line based World System Teletext transmissions. The device is based on IVT1.0VPS and has reception facilities for the 5 MHz biphase VPS signal. It is intended for use in video recorders, in particular to implement the VPT facility (VCR programming via Teletext). With suitable software both VPT standards (EBU PDC System A and System B) can be accommodated to allow operation from any European VPT transmission. Automatic processing of packet 26 transmissions is also possible. No external memory is required as an 8K × 8 DRAM is included on-chip for up to 8 page storage. An enhanced mode allows 7 Fastext pages to be stored, with one chapter used to store extension packets.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA5281P	DIP48	plastic shrink dual in-line package; 32 leads (400 mil)	SOT240-1
SAA5281ZP	SDIP52	plastic shrink dual in-line package; 52 leads (600 mil)	SOT247-1
SAA5281GP	QFP64	plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT319-2

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	4.5	5.0	5.5	V
I_{DD}	supply current	–	75	150	mA
V_{sync}	sync voltage amplitude	0.1	0.3	0.6	V
$V_{vid(p-p)}$	video input voltage amplitude (peak-to-peak value)	0.7	1.0	1.4	V
f_{xtal}	crystal frequency	–	27	–	MHz
T_{amb}	operating ambient temperature	–20	–	+70	°C

BLOCK DIAGRAM

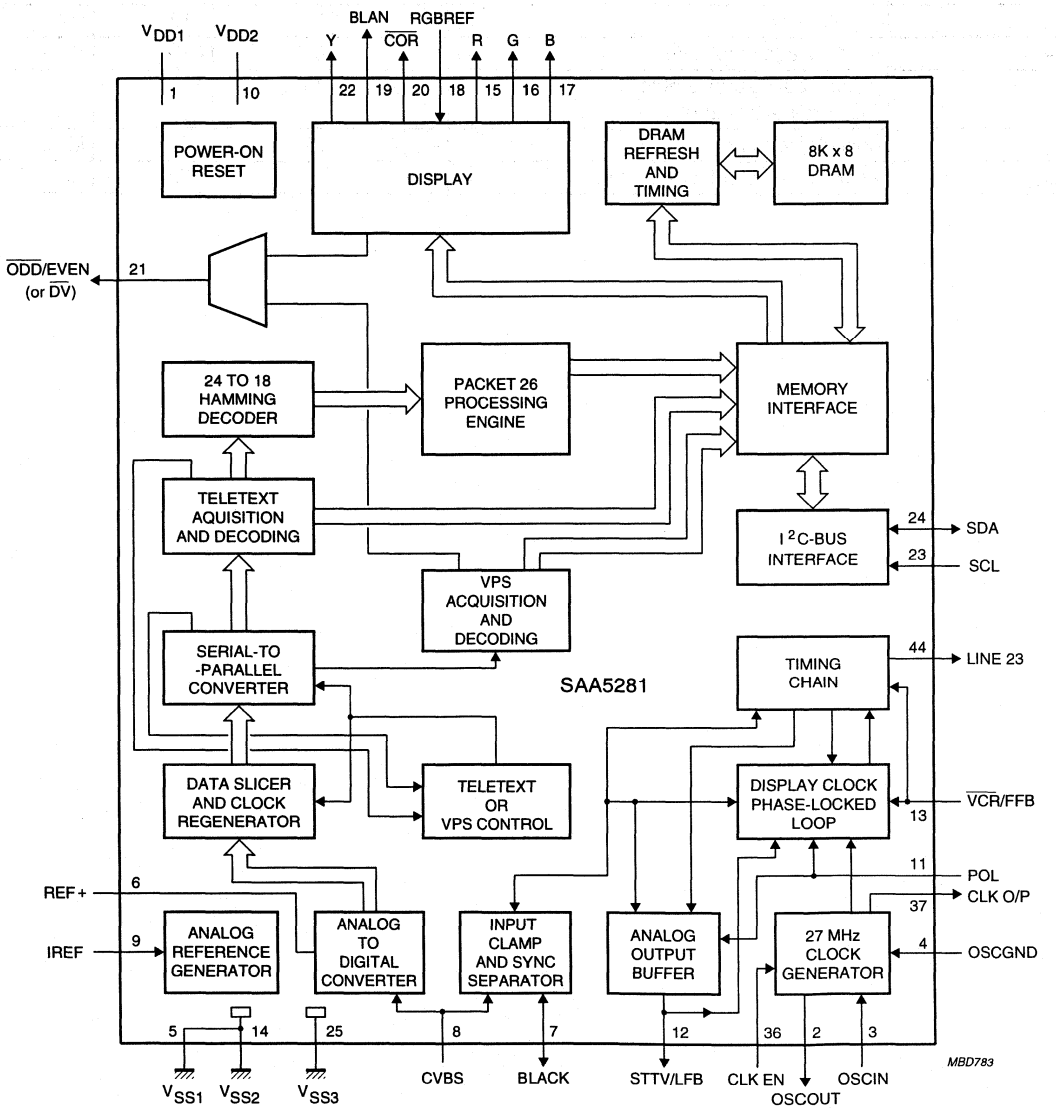


Fig.1 Block diagram; pin numbers for DIP48 (SOT240-1).

PINNING

SYMBOL	PIN			DESCRIPTION
	SOT240-1	SOT247-1	SOT319-2	
V_{DD1}	1	52	11	+5 V supply 1
OSCOUT	2	1	13	27 MHz crystal oscillator output
OSCIN	3	2	14	27 MHz crystal oscillator input
OSCGND	4	3	15	0 V crystal oscillator ground
V_{SS1}	5	4 and 5	16	0 V ground
REF+	6	6	18	positive reference voltage for ADC; this pin should be connected to ground via a 100 nF capacitor
BLACK	7	8	19	video black level storage input/output; this pin should be connected to ground via a 100 nF capacitor
CVBS	8	9	20	composite video input; a positive-going 1 V (peak-to-peak) input is required, connected via a 100 nF capacitor
IREF	9	10	21	reference current input, connected to ground via a 27 kΩ resistor
V_{DD2}	10	11	22	+5 V supply 2
POL	11	12	23	STTV/LFB/FFB polarity selection input
STTV/LFB	12	13	24	sync to TV output line flyback input; function controlled by an internal register bit (scan sync mode)
$\overline{VCR}$/FFB	13	14	27	PLL time constant switch/field input; function controlled by an internal register bit (scan sync mode)
V_{SS2}	14	15	28	0 V ground; connected to V_{SS1} for normal operation
R	15	16	30	dot rate character output of the RED colour information
G	16	17	32	dot rate character output of the GREEN colour information
B	17	18	33	dot rate character output of the BLUE colour information
RGBREF	18	19	34	input DC voltage to define the output high level on the RGB pins
BLAN	19	20	35	dot rate fast blanking output
$\overline{COR}$	20	21	36	programmable output to provide contrast reduction of the TV picture for mixed text and picture displays or when viewing newsflash/subtitle pages; open-drain output
$\overline{ODD}$/EVEN (or $\overline{DV}$)	21	22	37	in $\overline{ODD}$/EVEN mode a 25 Hz output synchronized with the CVBS input field sync pulses to produce a non-interlaced display by adjustment of the vertical deflection currents; in $\overline{DV}$ mode a VPT data valid signal is used to indicate reception of error-free VPS or 8/30 format 2 data
Y	22	23	38	dot rate character output of teletext foreground colour information; open-drain output
SCL	23	24	39	serial clock input for I²C-bus; it can still be driven HIGH during power-down of the device
SDA	24	25	40	serial data port for the I²C-bus, open-drain output; it can still be driven HIGH during power-down of the device
V_{SS3}	25	26	44	0 V ground

SYMBOL	PIN			DESCRIPTION
	SOT240-1	SOT247-1	SOT319-2	
i.c.	26 to 35, 38 to 43, 45 to 48	27 to 32, 35 to 38, 41 to 46, 48 to 51	1 to 3, 5 to 8, 45 to 53, 55, 61, 63 to 64	internally connected; normally open-circuit
CLK EN	36	39	56	clock enable input to enable the clock output (CLP O/P pin 37); internal pull-down normally disables clock
CLK O/P	37	40	59	13.5 MHz clock output to drive an external microcontroller
LINE 23	44	47	4	output for indication of Line 23 for use with external circuitry
n.c.	–	7, 33, 34	9, 10, 12, 17, 25, 26, 29, 31, 41 to 43, 54, 57, 58, 60, 62	not connected; normally open-circuit

Integrated Video input processor and Teletext decoder (IVT1.8*)

SAA5281

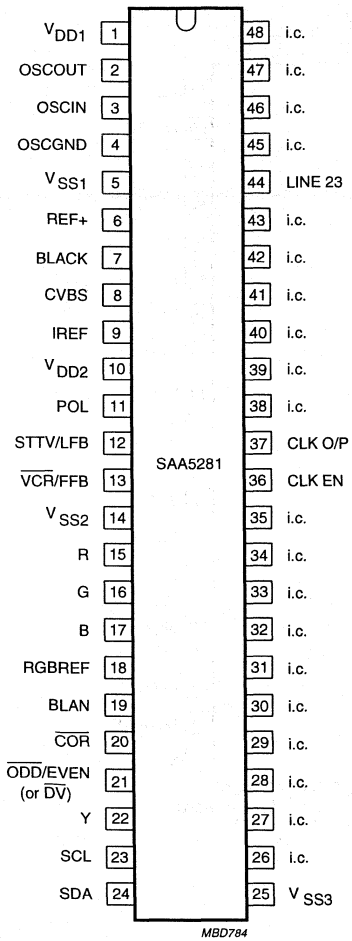


Fig.2 Pin configuration; SOT240-1 (DIP48).

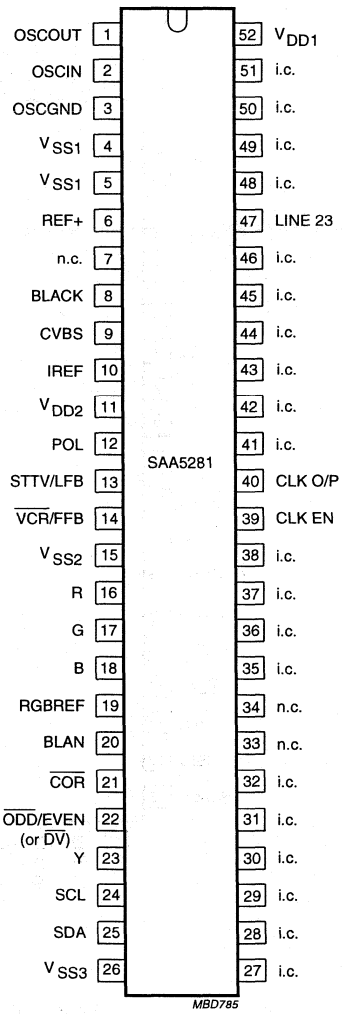


Fig.3 Pin configuration; SOT247-1 (SDIP52).

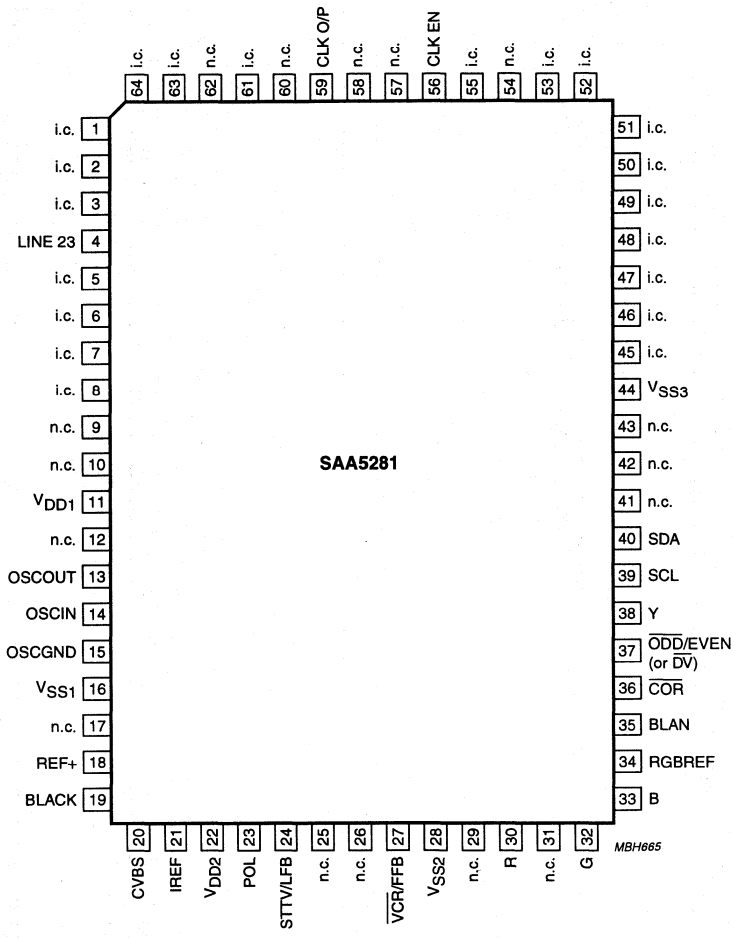


Fig.4 Pin configuration; SOT319-2 (QFP64).

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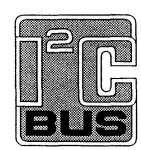


1 FEATURES

- Six analog inputs (6 × CVBS or 3 × Y/C or combinations)
- Three analog processing channels
- Three built-in analog anti-aliasing filters
- Analog signal adding of two channels
- Two 8-bit video CMOS analog-to-digital converters
- Fully programmable static gain for the main channels or automatic gain control for the selected CVBS/Y channel
- Selectable white peak control signal
- Luminance and chrominance signal processing for PAL B/G, NTSC M and SECAM
- Full range HUE control
- Automatic detection of 50/60 Hz field frequency, and automatic switching between standards PAL and NTSC, SECAM forceable
- Horizontal and vertical sync detection for all standards
- Cross-colour reduction by chrominance comb filtering for NTSC or special cross-colour cancellation for SECAM
- UV signal delay lines for PAL to correct chrominance phase errors
- The YUV-bus supports a data rate of:
  - $780 \times f_h$ = 12.2727 MHz for 60 Hz (NTSC)
  - $944 \times f_h$ = 14.75 MHz for 50 Hz (PAL/SECAM)
- Square pixel format with 768/640 active samples per line on the YUV-bus
- CCIR 601 level compatible
- 4 : 2 : 2 and 4 : 1 : 1 YUV output formats in 8-bit resolution
- User programmable luminance peaking for aperture correction
- Compatible with memory-based features (line-locked clock, square pixel)
- Requires only one crystal (26.8 MHz) for all standards
- Real time status information output (RTCO)
- Brightness Contrast Saturation (BCS) control for the YUV-bus
- Negation of picture possible
- One user programmable general purpose switch on an output pin
- Switchable between on-chip Clock Generation Circuit (CGC) and external CGC (SAA7197)
- Power-on control
- I²C-bus controlled.

2 APPLICATIONS

- Desktop video
- Multimedia
- Digital television
- Image processing
- Video phone
- Video picture grabbing.

3 GENERAL DESCRIPTION

The one chip front-end SAA7110; SAA7110A is a digital multistandard colour decoder (OCF1) on the basis of the DIG-TV2 system with two integrated Analog-to-Digital Converters (ADCs), a Clock Generation Circuit (CGC) and Brightness Contrast Saturation (BCS) control.

The CMOS circuit SAA7110; SAA7110A, analog front-end and digital video decoder, is a highly integrated circuit for desktop video applications. The decoder is based on the principle of line-locked clock decoding. It operates square-pixel frequencies to achieve correct aspect ratio. Monitor controls are provided to ensure best display. The circuit is I²C-bus controlled.

4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage	4.75	5.25	V
V_{DDD}	digital supply voltage	4.5	5.5	V
T_{amb}	operating ambient temperature	0	70	°C

5 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7110	PLCC68	plastic leaded chip carrier; 68 leads	SOT188-2
SAA7110A	PLCC68	plastic leaded chip carrier; 68 leads	SOT188-2

6 SYSTEM VIEW

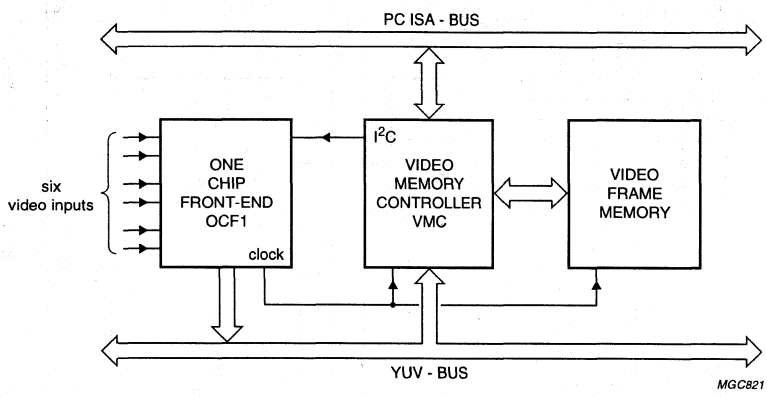


Fig.1 System diagram.

7 BLOCK DIAGRAM

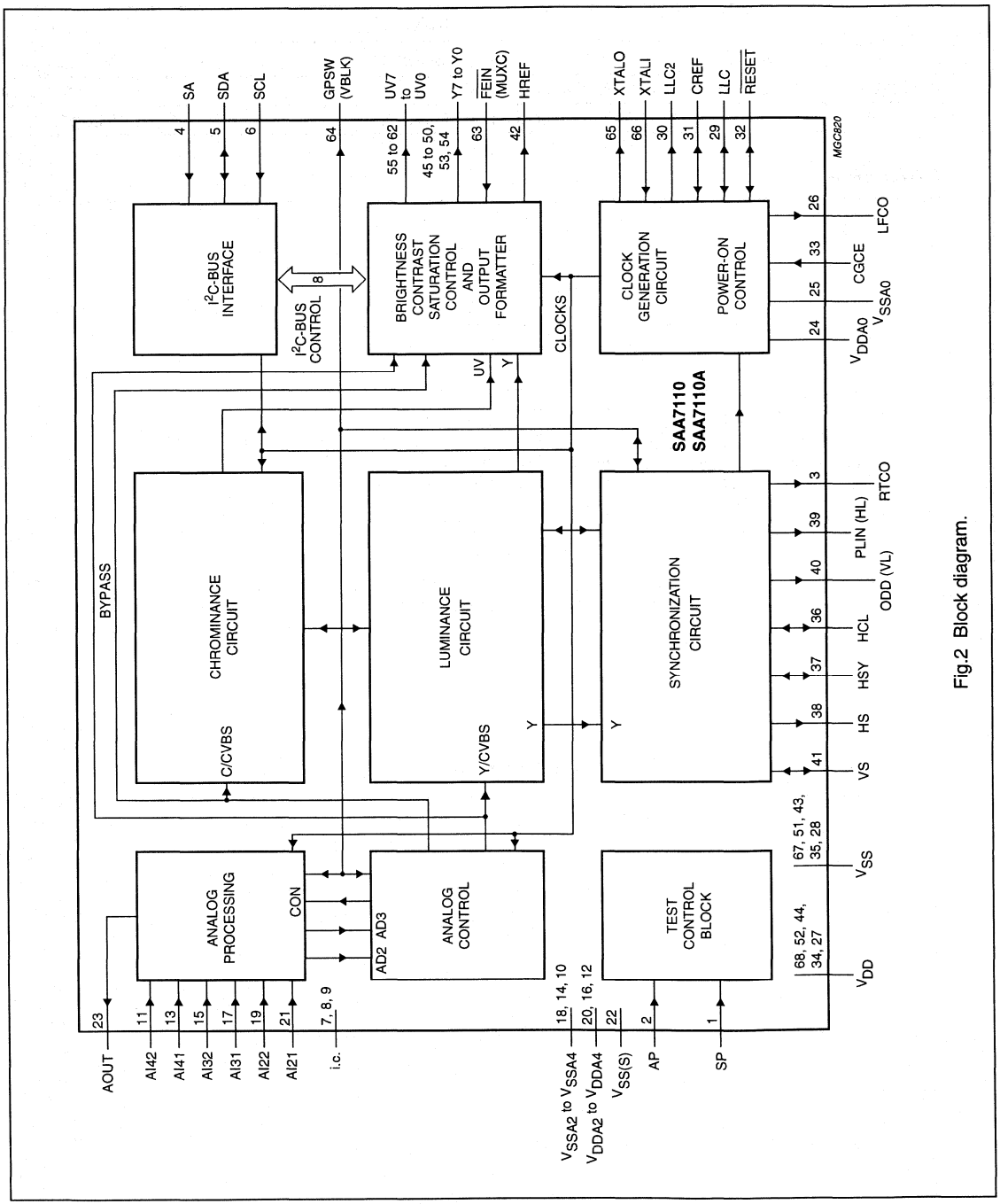


Fig.2 Block diagram.

8 PINNING

SYMBOL	PIN	DESCRIPTION
SP	1	test pin input; (shift pin) connect to ground for normal operation
AP	2	test pin input; (action pin) connect to ground for normal operation
RTCO	3	Real Time Control Output. This pin is used to fit serially the increments of the HPLL and FSC-PLL and information of the PAL or SECAM sequence.
SA	4	I^2C-bus slave address select input. LOW: slave address = 9CH for write, 9DH for read; HIGH = 9DH for write, 9FH for read.
SDA	5	I^2C-bus serial data input/output
SCL	6	I^2C-bus serial clock input
i.c.	7	reserved pin; do not connect
i.c.	8	reserved pin; do not connect
i.c.	9	reserved pin; do not connect
V_{SSA4}	10	ground for analog input 4
AI42	11	analog input 42
V_{DDA4}	12	supply voltage (+5 V) for analog input 4
AI41	13	analog input 41
V_{SSA3}	14	ground for analog input 3
AI32	15	analog input 32
V_{DDA3}	16	supply voltage (+5 V) for analog input 3
AI31	17	analog input 31
V_{SSA2}	18	ground for analog input 2
AI22	19	analog input 22
V_{DDA2}	20	supply voltage (+5 V) for analog input 2
AI21	21	analog input 21
$V_{SS(S)}$	22	substrate ground
AOUT	23	analog test output; do not connect
V_{DDA0}	24	supply voltage (+5 V) for internal CGC (Clock Generation Circuit)
V_{SSA0}	25	ground for internal CGC
LFCO	26	Line Frequency Control output; this is the analog clock control signal driving the external CGC. The frequency is a multiple of the actual line frequency (nominally 7.375/6.13636 MHz). The signal has a triangular form with 4-bit accuracy.
V_{DD}	27	supply voltage (+5 V)
V_{SS}	28	ground
LLC	29	Line-Locked Clock input/output (CGCE = 1, output; CGCE = 0, input). This is the system clock, its frequency is $1888 \times f_h$ for 50 Hz/625 lines per field systems and $1560 \times f_h$ for 60 Hz/525 lines per field systems; or variable input clock up to 32 MHz in input mode.
LLC2	30	Line-Locked Clock ½ output; $f_{LLC2} = 0.5 \times f_{LLC}$ (CGCE = 1, output; CGCE = 0, high impedance).
CREF	31	Clock reference input/output (CGCE = 1, output; CGCE = 0, input). This is a clock qualifier signal distributed by the internal or an external clock generator circuit (CGC). Using CREF all interfaces on the YUV-bus are able to generate a bus timing with identical phase.

SYMBOL	PIN	DESCRIPTION
$\overline{RESET}$	32	Reset active LOW input/output (CGCE = 1, output; CGCE = 0, input); sets the device into a defined state. All data outputs are in high impedance state. The I²C-bus is reset (waiting for START condition). Using the external CGC, the LOW period must be maintained for at least 30 LLC clock cycles.
CGCE	33	CGC Enable active HIGH input (CGCE = 1, on-chip CGC active; CGCE = 0, external CGC mode, use SAA7197).
V_{DD}	34	supply voltage (+5 V)
V_{SS}	35	ground
HCL	36	Horizontal Clamping input/output pulse (programmable via I²C-bus bit PULIO: PULIO = 1, output; PULIO = 0, input). This signal is used to indicate the black level clamping period for the analog input interface. The beginning and end of its HIGH period (only in the output mode) can be programmed via the I²C-bus registers 03H, 04H in 50 Hz mode and registers 16H, 17H in 60 Hz mode, active HIGH.
HSY	37	Horizontal Synchronization input/output indicator (programmable via I²C-bus bit PULIO: PULIO = 1, output; PULIO = 0, input). This signal is fed to the analog interface. The beginning and end of its HIGH period (only in the output mode) can be programmed via the I²C-bus registers 01H, 02H in 50 Hz mode and registers 14H, 15H in 60 Hz mode, active HIGH.
HS	38	Horizontal Synchronization output (programmable; the HIGH period is 128 LLC clock cycles). The position of the positive slope is programmable in 8 LLC increments over a complete line (64 µs) via the I²C-bus register 05H in 50 Hz mode or register 18H in 60 Hz mode.
PLIN (HL)	39	PAL Identifier Not output; marks for demodulated PAL signals the inverted line (PLIN = LOW) and a non-inverted line (PLIN = HIGH) and for demodulated SECAM the DR line (PLIN = LOW) and the DB line (PLIN = HIGH). Select PLIN function via I²C-bus bit RTSE = 0. (H-PLL locked output; a HIGH state indicates that the internal PLL has locked. Select HL function via I²C-bus bit RTSE = 1).
ODD (VL)	40	ODD/EVEN field identification output; a HIGH state indicates the odd field. Select ODD function via I²C-bus bit RTSE = 0. (Vertical Locked output; a HIGH state indicates that the internal Vertical Noise Limiter (VNL) is in a locked state. Select VL function via I²C-bus bit RTSE = 1).
VS	41	Vertical Synchronization input/output (programmable via I²C-bus bit OEHV: OEHV = 1, output; OEHV = 0, input). This signal indicates the vertical synchronization with respect to the YUV output. The high period of this signal is approximately six lines if the VNL function is active. The positive slope contains the phase information for a deflection controller, for example the TDA9150. In input mode this signal is used to synchronize the vertical gain and clamp blanking stage, active HIGH.
HREF	42	Horizontal Reference output; this signal is used to indicate data on the digital YUV-bus. The positive slope marks the beginning of a new active line. The HIGH period of HREF is either 768 Y samples or 640 Y samples long depending on the detected field frequency (50/60 Hz mode). HREF is used to synchronize data multiplexer/demultiplexers. HREF is also present during the vertical blanking interval.
V_{SS}	43	ground
V_{DD}	44	supply voltage (+5 V)

SYMBOL	PIN	DESCRIPTION
Y7	45	Upper 6 bits of the 8-bit luminance (Y) digital output. As part of the digital YUV-bus (data rate LLC/2), or A/D2(3) output (data rate LLC/2) selectable via I²C-bus bit SQPB = 1.
Y6	46	
Y5	47	
Y4	48	
Y3	49	
Y2	50	
V_{SS}	51	ground
V_{DD}	52	supply voltage (+5 V)
Y1	53	Lower 2 bits of the 8-bit luminance (Y) digital output. As part of the digital YUV-bus (data rate LLC/2), or A/D2(3) output (data rate LLC/2) selectable via I²C-bus bit SQPB = 1.
Y0	54	
UV7	55	8-bit digital UV (colour difference) output; multiplexed colour difference signal for U and V component of demodulated CVBS or chrominance signal. The format and multiplexing scheme can be selected via I²C-bus control. These signals are part of the digital YUV-bus (data rate LLC/2), or A/D3(2) output (data rate LLC/2) selectable via I²C-bus bit SQPB = 1.
UV6	56	
UV5	57	
UV4	58	
UV3	59	
UV2	60	
UV1	61	
UV0	62	
$\overline{\text{FEIN}}$ (MUXC)	63	Fast Enable input (active LOW); this signal is used to control fast switching on the digital YUV-bus. A high at this input forces the IC to set its Y and UV outputs to the high impedance state. To use this function set I²C-bus bits MS24 and MS34 and MUYC to LOW. (Multiplex Components input; control signal for the analog multiplexers for fast switching between locked Y/C signals or locked CVBS signals. FEIN automatically fixed to LOW (digital YUV-bus enabled), if one of the three MUXC functions are selected (MS24 or MS34 or MUYC = HIGH).
GPSW (VBLK)	64	General Purpose Switch output; the state of this signal is programmable via I²C-bus register 0Dh, bit 1. Select GPSW function via I²C-bus bit VBLKA = 0. (Vertical Blank test output; select VBLK via I²C-bus bit VBLKA = 1).
XTALO	65	Crystal oscillator output (to 26.8 MHz crystal); not used if TTL clock is used.
XTALI	66	Crystal oscillator input (from 26.8 MHz crystal) or connection of external oscillator with TTL compatible square wave clock signal.
V_{SS}	67	ground
V_{DD}	68	supply voltage (+5 V)

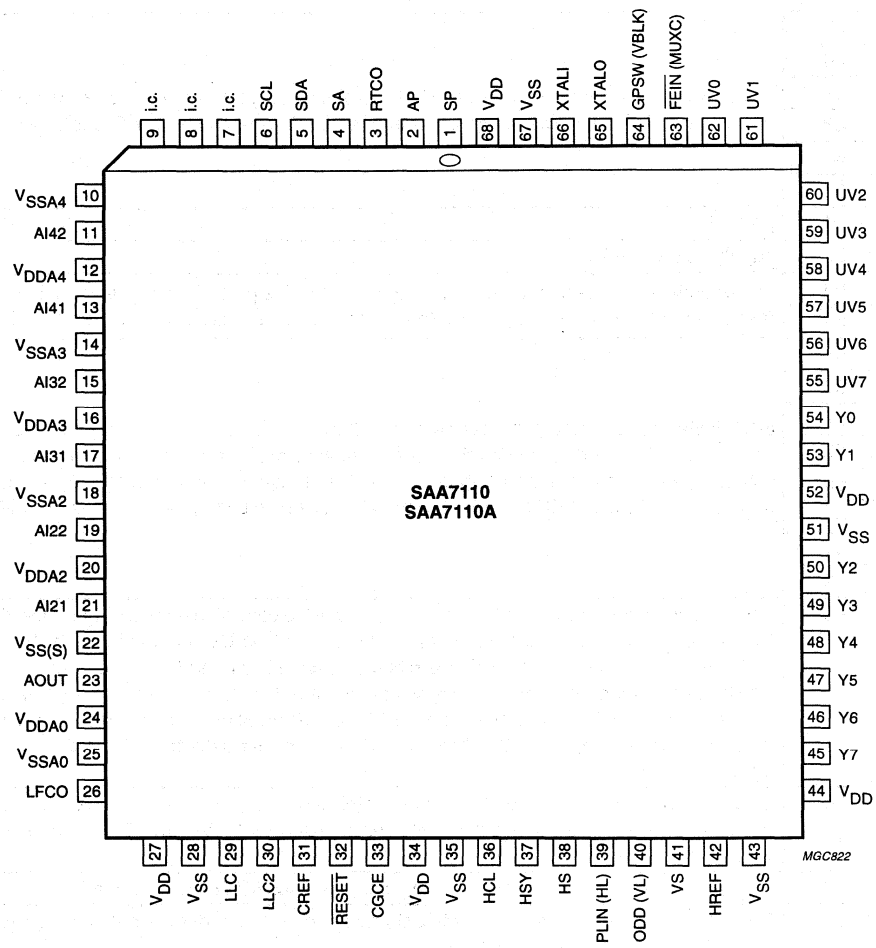


Fig.3 Pin configuration.

9 FUNCTIONAL DESCRIPTION

9.1 Analog input processing (see Fig.5)

The SAA7110; SAA7110A offers six analog signal inputs, two analog main channels with clamping circuit, analog amplifier, anti-alias filter and video CMOS ADC. A third analog channel also with clamping circuit, analog amplifier and anti-alias filter can be added or switched to both main channels directly before the ADCs.

9.2 Analog control circuits

The clamping control circuit controls the correct clamping of the analog input signals. The coupling capacitor is also used to store and filter the clamping voltage. The normal digital clamping level for luminance or CVBS signals is 64 and for chrominance signals is128.

The gain control circuits generate via I²C-bus the static gain levels for the three analog amplifiers or controls one of these amplifiers automatically via a built-in Automatic Gain Control (AGC). The AGC is used to amplify a CVBS or Y signal to the required signal amplitude, matched to the ADCs input voltage range.

The anti-alias filters are adapted to the clock frequency. The vertical blanking control circuit generates an I²C-bus programmable vertical blanking pulse. During the vertical blanking time gain and clamping control are frozen.

The fast switch control circuit is used for special applications.

9.2.1 CLAMPING

The coupling capacitor is used as clamp capacitance for each input. An internal digital clamp comparator generates the information concerning clamp-up or clamp-down. The clamping levels for the two ADC channels are adjustable over the 8-bit range (1 to 254). Clamping time in normal use is set with the HCL pulse at the back porch of the video signal. The clamping pulse HCL is user adjustable.

9.2.2 GAIN CONTROL (see Fig.4)

The luminance AGC can be used for every channel were luminance or CVBS is being received. AGC active time is the sync tip of the video signal. The sync tip pulse HSY is user adjustable. The AGC can be switched off and the gain for the three main input channels can be adjusted independently. Signal (white) peak control limits the gain at signal overshoots. The flow charts (see Figs 8 and 9) show more details of the AGC. The influence of supply voltage variation within the specified range is automatically eliminated by clamp and automatic gain control.

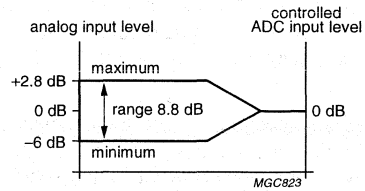


Fig.4 Automatic gain control range.

9.3 Chrominance processing (see Fig.6)

The 8-bit chrominance signal passes the input interface, the chrominance bandpass filter to eliminate DC components, and is finally fed to the multiplication inputs of a quadrature demodulator, where two subcarrier signals from the local oscillator DTO1 with 90 degrees phase shift are applied. The frequency is dependent on the present colour standard.

The multiplier operates as a quadrature demodulator for all PAL and NTSC signals; it operates as a frequency down mixer for SECAM signals.

The two multiplier output signals are converted to a serial UV data stream and applied to two low-pass filter stages, then to a gain controlled amplifier. A final multiplexed low-pass filter achieves, together with the preceding stages, the required bandwidth performance.

The PAL and NTSC originated signals are applied to a comb filter.

The signal originated from SECAM is fed through a Cloche filter (0 Hz centre frequency), a phase demodulator and a differentiator to obtain frequency demodulated colour difference signals. The SECAM signal is fed after de-emphasis to a cross-over switch, to provide both the serial transmitted colour difference signals. These signals are fed to the BCS control and finally to the output fomatter stage and to the output interface.

9.4 Luminance processing (see Fig.7)

The 8-bit luminance signal, a digital CVBS format or a luminance format (S-VHS, HI8), is fed through a switchable prefilter. High frequency components are emphasized to compensate for loss. The following chrominance trap filter (f_c = 4.43 or 3.58 MHz centre frequency selectable) eliminates most of the colour carrier signal, therefore, it must be bypassed for S-Video (S-VHS, HI8) signals.

The high frequency components of the luminance signal can be peaked (control for sharpness improvement via I²C-bus) in two bandpass filters with selectable transfer characteristics.

A coring circuit with selectable characteristics improves the signal once more. This signal is then added to the original (unpeaked) signal. A switchable amplifier achieves common DC amplification, because the DC gains are different in both chrominance trap modes.

The improved luminance signal is fed via the variable delay to the BCS control and the output interface.

9.5 YUV-bus (digital outputs)

The 16-bit YUV-bus transfers digital data from the output interfaces to a feature box, or a field memory, a digital colour space converter (SAA 7192 DCSC) or a video enhancement and digital-to-analog processor (SAA7165 VEDA2). The outputs are controlled by an output enable chain ($\overline{\text{FEIN}}$ on pin 63).

The YUV data rate equals LLC2. Timing is achieved by marking each second positive rising edge of the clock LLC in conjunction with CREF (clock reference).

The output signals Y7 to Y0 are the bits of the digital luminance signal. The output signals UV7 to UV0 are the bits of multiplexed colour difference signals (B–Y) and (R–Y). The frame in the format tables is the time, required to transfer a full set of samples. In the event of 4 : 2 : 2 format two luminance samples are transmitted in comparison to one U and one V sample within the frame. The time frames are controlled by the HREF signal.

Fast enable is achieved by setting input $\overline{\text{FEIN}}$ to LOW. The signal is used to control fast switching on the digital YUV-bus. HIGH on this pin forces the Y and UV outputs to a high-impedance state.

9.6 Synchronization (see Fig.7)

The pre-filtered luminance signal is fed to the synchronization stage. It's bandwidth is reduced to 1 MHz in a low-pass filter.

The synchronization pulses are sliced and fed to the phase detectors where they are compared with the sub-divided clock frequency. The resulting output signal is applied to the loop filter to accumulate all phase deviations. Adjustable output signals HCL and HSY are generated in accordance with analog front end requirements. The output signals HS, VS, and PLIN are locked to the timing reference, guaranteed between the input signal and the HREF signal, as further improvements to the circuit may change the total processing delay. It is therefore not recommended to use them for applications which require absolute timing accuracy to the input signals. The loop filter signal drives an oscillator to generate the line frequency control signal LFCO.

9.7 Clock generation circuit

The internal CGC generates all clock signals required for the one chip front-end. The output signal LFCO is a digital-to-analog converted signal provided by the horizontal PLL. It is the multiple of the line frequency (7.38 MHz = 472 × f_h in 50 Hz systems and 6.14 MHz = 360 × f_h in 60 Hz systems). Internally the LFCO signal is multiplied by a factor of 2 or 4 in the PLL circuit (including phase detector, loop filtering, VCO and frequency divider) to obtain the LLC and LLC2 output clock signals. The rectangular output clocks have a 50% duty factor.

It is also possible to operate the OCF1 with an external CGC (SAA7197) providing the signals LLC and CREF. The selection of the internal/external CGC will be controlled by the CGCE input signal.

9.8 Power-on reset

Power-on reset is activated at power-on (using only internal CGC), when the supply voltage decreases below 3.5 V. The indicator output $\overline{\text{RESET}}$ is LOW for a time. The $\overline{\text{RESET}}$ signal can be applied to reset other circuits of the digital TV system.

9.9 RTCO output

The real time control and status output signal contains serial information about actual system clock, subcarrier frequency and PAL/SECAM sequence. The signal can be used for various applications in external circuits, for example, in a digital encoder to achieve clean encoding.

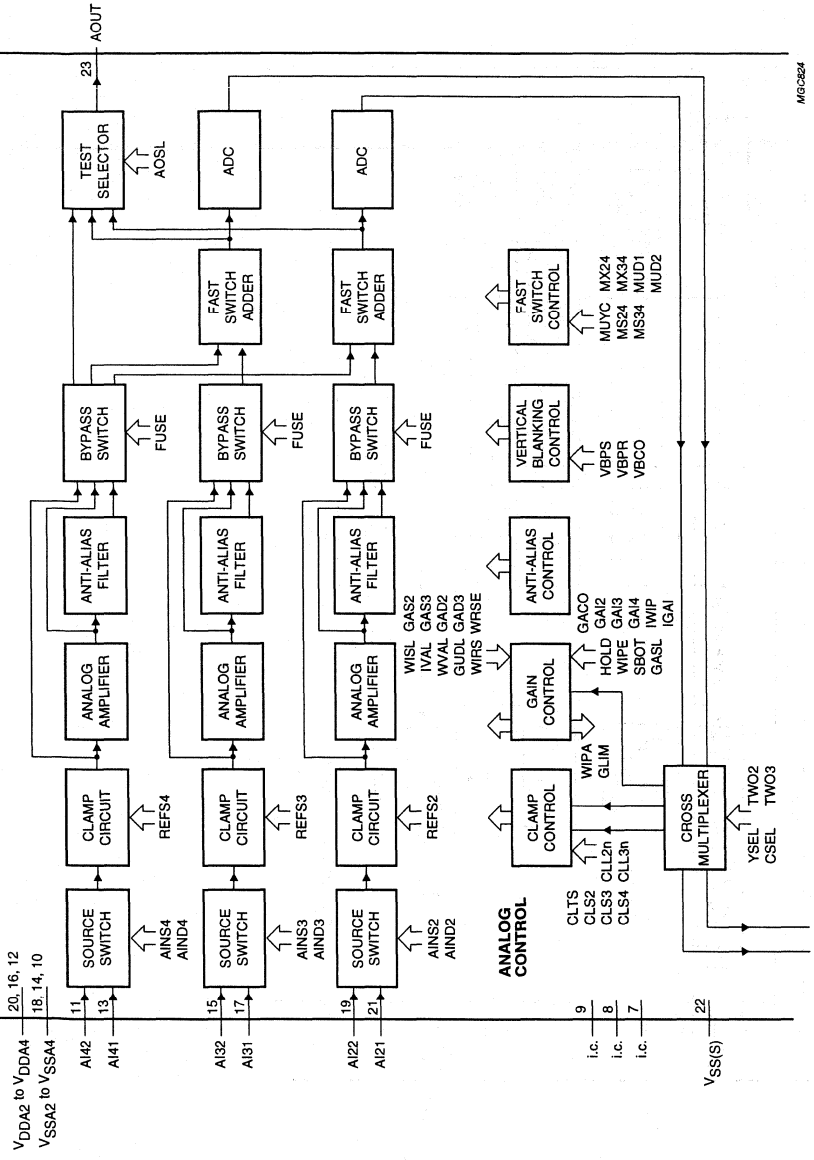


Fig.5 Analog input processing and analog control part.

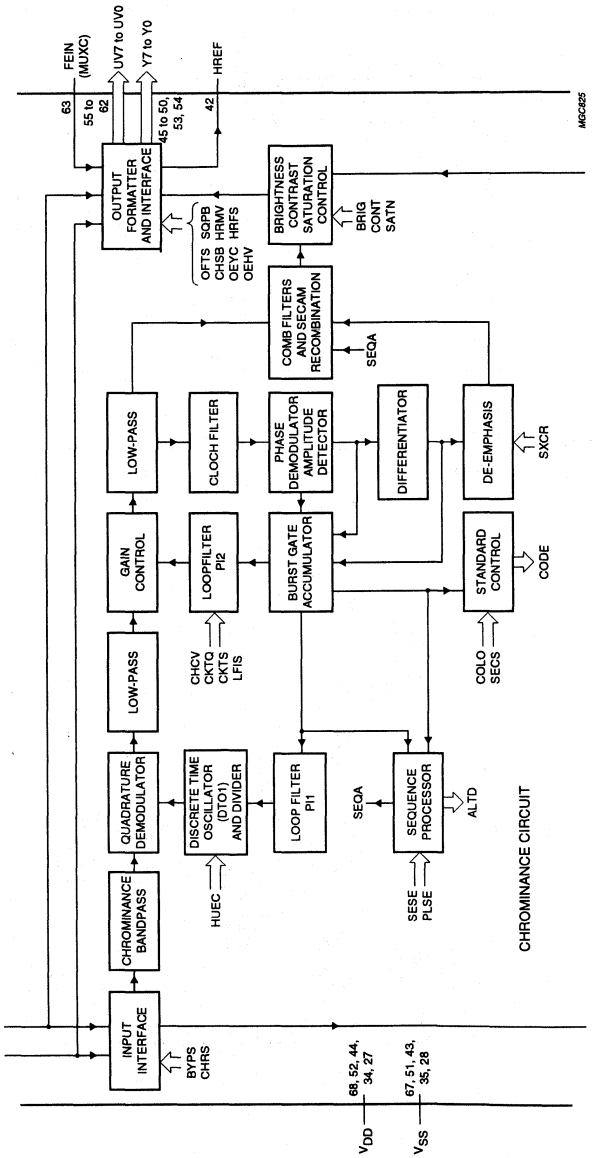


Fig.6 Multi-standard decoder part.

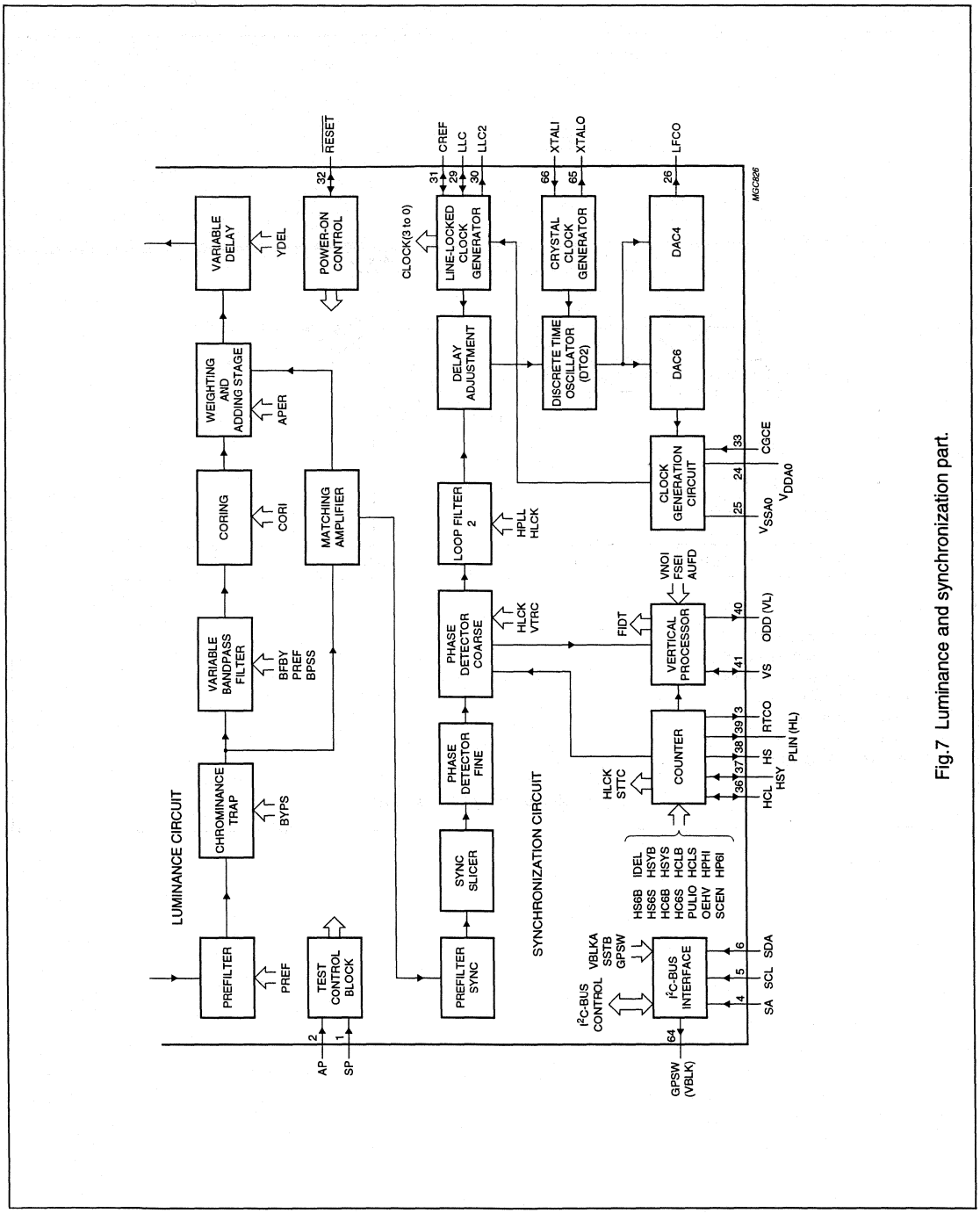
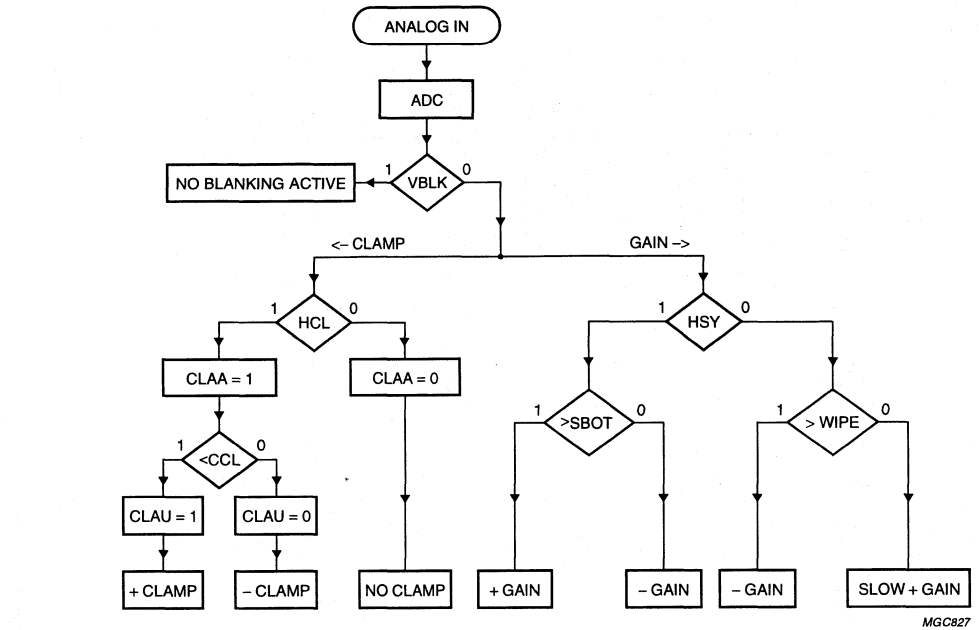


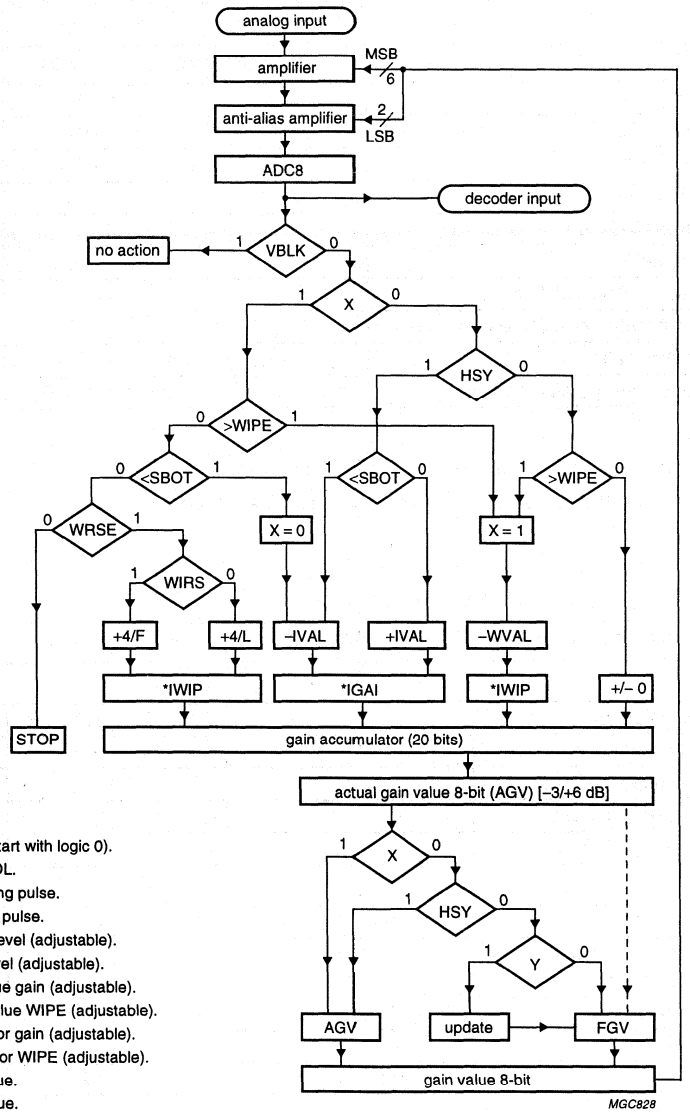
Fig.7 Luminance and synchronization part.

10 GAIN CHARTS



CLAU = clamp up.
VBLK = vertical blanking pulse.
WIPE = white peak level (adjustable).
SBOT = sync bottom level (adjustable).
CLL = clamp level (adjustable).
CLAA = clamp active.
HSY = horizontal sync pulse.
HCL = horizontal clamp pulse.

Fig.8 Clamp and gain flow chart.



X = system variable (start with logic 0).
Y = IAGV-FGVI > GUDL.
VBLK = vertical blanking pulse.
HSY = horizontal sync pulse.
SBOT = sync bottom level (adjustable).
WIPE = white peak level (adjustable).
IVAL = integration value gain (adjustable).
WVAL = integration value WIPE (adjustable).
IGAI = integration factor gain (adjustable).
IWIP = integration factor WIPE (adjustable).
AGV = actual gain value.
FGV = frozen gain value.
GUDL = gain update level (adjustable).
WRSE = white peak reset enable.
WIRS = white peak reset select.
L = line.
F = field.

Fig.9 Luminance AGC flow chart.

11 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); all ground pins and all supply pins connected together.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage		−0.5	+7.0	V
V_{DDD}	digital supply voltage		−0.5	+7.0	V
$V_{I(A)}$	analog input voltage		−0.5	+7.0	V
$V_{I(D)}$	digital input voltage		−0.5	+7.0	V
V_{diff}	voltage difference between V_{SSAall} and V_{SSall}		–	100	mV
T_{stg}	storage temperature		−65	+150	°C
T_{amb}	operating ambient temperature		0	70	°C
$T_{amb(bias)}$	operating ambient temperature under bias		−10	+80	°C
P_{tot}	total power dissipation	$V_{DDA} = V_{DDD} = 7$ V; note 1	–	2.5	W
V_{esd}	electrostatic discharge all pins	note 2	−2000	+2000	V

Note

1. Compare with typical total power consumption in Chapter "Characteristics".
2. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

12 CHARACTERISTICS

$V_{DDD} = 5$ V; $V_{DDA} = 5$ V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDA}	analog supply voltage		4.75	5.0	5.25	V
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
$I_{DDA(tot)}$	total analog supply current		–	–	150	mA
$I_{DDD(tot)}$	total digital supply current		–	–	250	mA
P_{tot}	total power dissipation		–	1.2	1.7	W
Analog part						
I_{clamp}	clamping current	$V_I = 1.25$ V DC	−2	–	+2	μA
$V_{i(p-p)}$	input voltage (peak-to-peak value), AC coupling required	$C_{couple} = 10$ nF	0.5	1.0	1.38	V
$\lvert Z_i \rvert$	input impedance	clamping current off	200	–	–	kΩ
C_i	input capacitance		–	–	10	pF
α_{ct}	channel crosstalk	$f_i < 5$ MHz	–	−50	–	dB
Analog-to-digital converters						
B	analog bandwidth	at −3 dB	–	15	–	MHz
ϕ_{diff}	differential phase	amplifier + AAF = bypass	–	2	–	deg
G_{diff}	differential gain	amplifier + AAF = bypass	–	2	–	%
f_{LLC}	ADC clock rate		11	–	16	MHz
DLE	DC differential linearity error		–	½	–	LSB
ILE	DC integral linearity error		–	1	–	LSB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital inputs						
V_{IL}	LOW level input voltage SDA and SCL		−0.5	–	+1.5	V
V_{IH}	HIGH level input voltage SDA and SCL		3.0	–	V_{DD} + 0.5	V
$V_{IL(clk)}$	LOW level input voltage for clocks		−0.5	–	+0.6	V
$V_{IH(clk)}$	HIGH level input voltage for clocks		2.4	–	V_{DD} + 0.5	V
$V_{IH(XTALI)}$	HIGH level input voltage XTALI		3.0	–	V_{DD} + 0.5	V
$V_{IL(n)}$	LOW level input voltage all other inputs		−0.5	–	+0.8	V
$V_{IH(n)}$	HIGH level input voltage all other inputs		2.0	–	V_{DD} + 0.5	V
I_{LI}	input leakage current		–	–	10	μA
$C_{i(clk)}$	input capacitance for clocks		–	–	10	pF
$C_{i(I/O)}$	input capacitance	I/Os at high impedance	–	–	8	pF
$C_{i(n)}$	input capacitance all other inputs		–	–	8	pF
Digital outputs						
V_{LFCO}	LFCO output voltage (peak-to-peak value)	note 1	1.4	–	2.6	V
V_{OL}	LOW level output voltage	note 2	0	–	0.6	V
V_{OH}	HIGH level output voltage	note 2	2.4	–	V_{DD}	V
$V_{OL(clk)}$	LOW level output voltage for clocks		−0.5	–	+0.6	V
$V_{OH(clk)}$	HIGH level output voltage for clocks		2.6	–	V_{DD} + 0.5	V
Clock input timing (LLC)						
T_{cy}	cycle time		31	–	45	ns
δ	duty factor for t_{LLCH}/T_{cy}		40	–	60	%
t_r	rise time	V_i = 0.6 to 2.4 V	–	–	5	ns
t_f	fall time	V_i = 2.4 to 0.6 V	–	–	5	ns
Control and CREF input timing (note 3)						
$t_{SU;DAT}$	input data set-up time		11	–	–	ns
$t_{HD;DAT}$	input data hold time		3	–	–	ns
$t_{HD;FEIN}$	input data hold time for $\overline{FEIN}$		3	–	–	ns
$t_{HD;OTHER}$	input data hold time all other inputs	note 3	6	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data and control output timing (note 4)						
$C_{L(data)}$	output load capacitance (data, HREF and VS)		15	–	50	pF
$C_{L(control)}$	output load capacitance (control)		7.5	–	25	pF
$t_{HD;DAT}$	output data hold time	C_L = 15 pF	13	–	–	ns
$t_{PD(data)}$	propagation delay from negative edge of LLC (data, HREF and VS)	C_L = 50 pF	–	–	29	ns
$t_{PD(control)}$	propagation delay from negative edge of LLC (control)	C_L = 25 pF	–	–	29	ns
$t_{PD(Z))}$	propagation delay from negative edge of LLC (to 3-state)	note 5	–	–	15	ns
Clock output timing (LLC and LLC2)						
$C_{L(LLC)}$	output load capacitance		15	–	40	pF
T_{cy}	cycle time	LLC	31.5	–	45	ns
		LLC2	63	–	90	ns
δ	duty factors for t_{LLCH}/t_{LLC} and t_{LLC2H}/t_{LLC2}		40	–	60	%
t_r	rise time	0.6 to 2.6 V	–	–	5	ns
t_f	fall time	2.6 to 0.6 V	–	–	5	ns
t_d	delay time LLC output to LLC2 output	V_i = 1.5 V; $C_{LLC/LLC2}$ = 40 pF; note 6	–	–	8	ns
Data qualifier output timing (CREF)						
$t_{HD;CREF}$	output hold time	C_L = 15 pF	4	–	–	ns
$t_{PD;CREF}$	propagation delay from positive edge of LLC	C_L = 40 pF	–	–	20	ns
Horizontal PLL						
f_{Hnom}	nominal line frequency	50 Hz field	–	15625	–	Hz
		60 Hz field	–	15734	–	Hz
$\Delta f_H/f_{Hnom}$	permissible static deviation	50 Hz field	–	–	5.6	%
		60 Hz field	–	–	6.7	%
Subcarrier PLL						
f_{Hnom}	nominal subcarrier frequency	PAL	–	4433618	–	Hz
		NTSC	–	3579545	–	Hz
$\Delta f_H/f_{Hnom}$	lock-in range		400	–	–	Hz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Crystal oscillator						
f_n	nominal frequency	3rd harmonic	–	26.8	–	MHz
$\Delta f/f_n$	permissible frequency deviation		-50×10^{-6}	–	$+50 \times 10^{-6}$	
$\Delta T/f_n$	permissible frequency deviation with temperature		-20×10^{-6}	–	$+20 \times 10^{-6}$	
CRYSTAL SPECIFICATION (X1); note 7						
T_{amb}	operating ambient temperature		0	–	70	°C
C_L	load capacitance		8	–	–	pF
R_s	series resonance resistance		–	50	80	Ω
C1	motional capacitance		–	1.1 ±20%	–	fF
C0	parallel capacitance		–	3.5 ±20%	–	pF

Notes

1. The LFCO output level must be measured with a load circuit of 10 kΩ in parallel with 15 pF.
2. The levels must be measured with load circuits, the loads depend on the type of output stage. Control outputs (except HREF and VS); 1.2 kΩ at 3 V (TTL load); C_L = 25 pF: data outputs (plus HREF and VS); 1.2 kΩ at 3 V (TTL load); C_L = 50 pF.
3. Other control input signals are CGCE, VS, SA, HCL and HSY.
4. Data output signals are YUV (15 to 0). Control output signals are HREF, VS, HS, HSY, HCL, RTCO, PLIN (HL), ODD (VL) and GPSW0 (VBLK). The effects of rise and fall times are included in the calculation of $t_{HD;DAT}$, t_{PD} and t_{PDZ}. Timings and levels refer to drawings and conditions illustrated in Fig.10.
5. The minimum propagation delay from 3-state to data active related to falling edge of LLC is 0 ns.
6. LLC2 is not active while CGCE = 0.
7. Philips catalogue number 9922 520 30004.

Table 1 Processing delay

FUNCTION	TYPICAL ANALOG DELAY AI21 TO ADCIN (AOUT) (ns)	DIGITAL DELAY ADCIN (AOUT) TO YUVOUT (1/LLC) (YDEL = 0; CAD2/3 = 1)
Without amplifier or anti-alias filter	10	248
With amplifier, without anti-alias filter	30	
With amplifier plus anti-alias filter (50 Hz)	30 + 40	
With amplifier plus anti-alias filter (60 Hz)	30 + 50	

13 TIMING

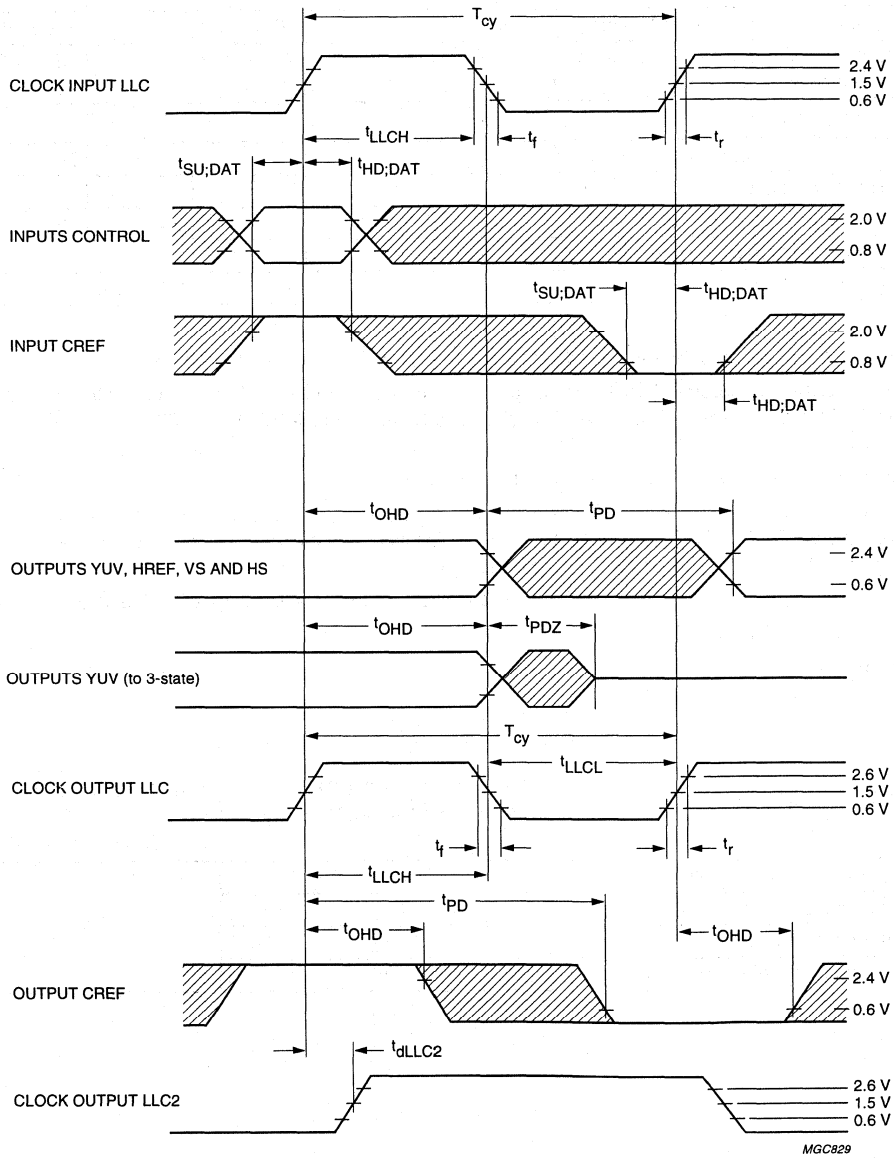
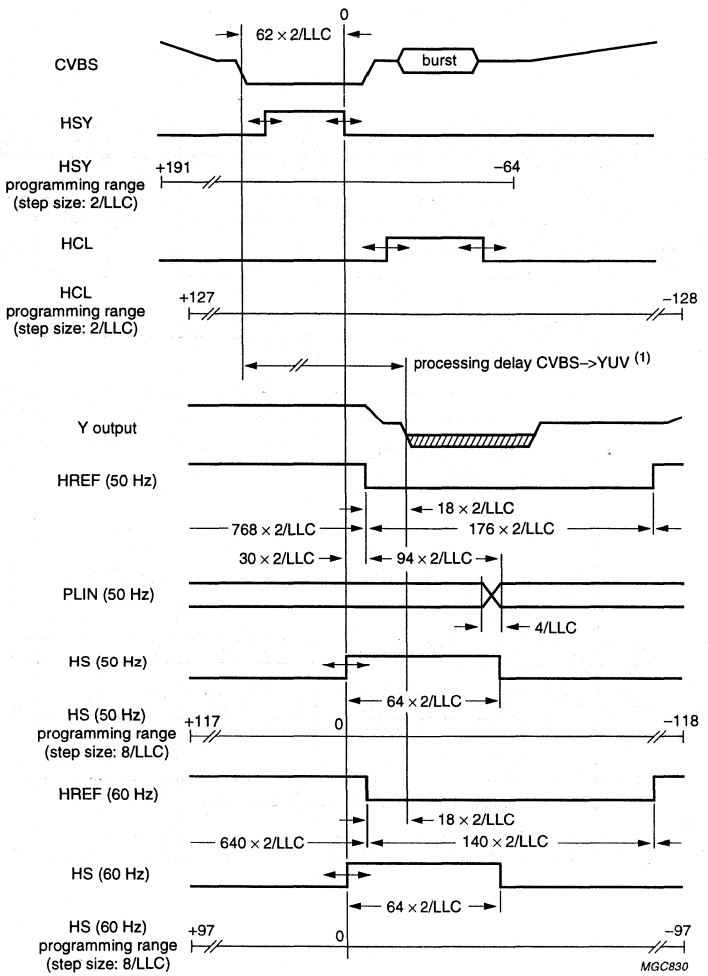


Fig.10 Clock/data timing.



(1) See Table 1.
HRMV = 1 and HRFS = 0.

Fig.11 Horizontal timing.

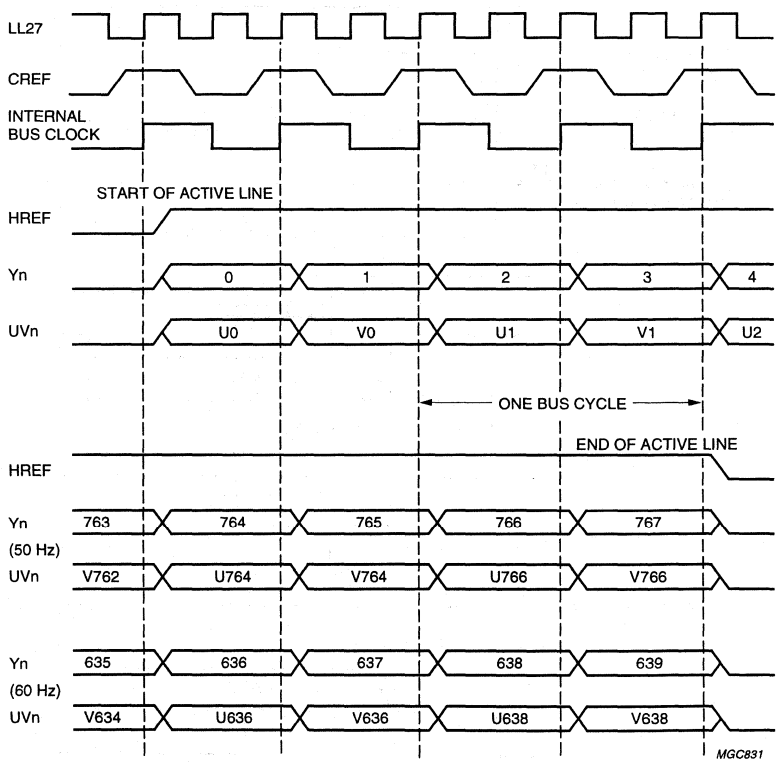
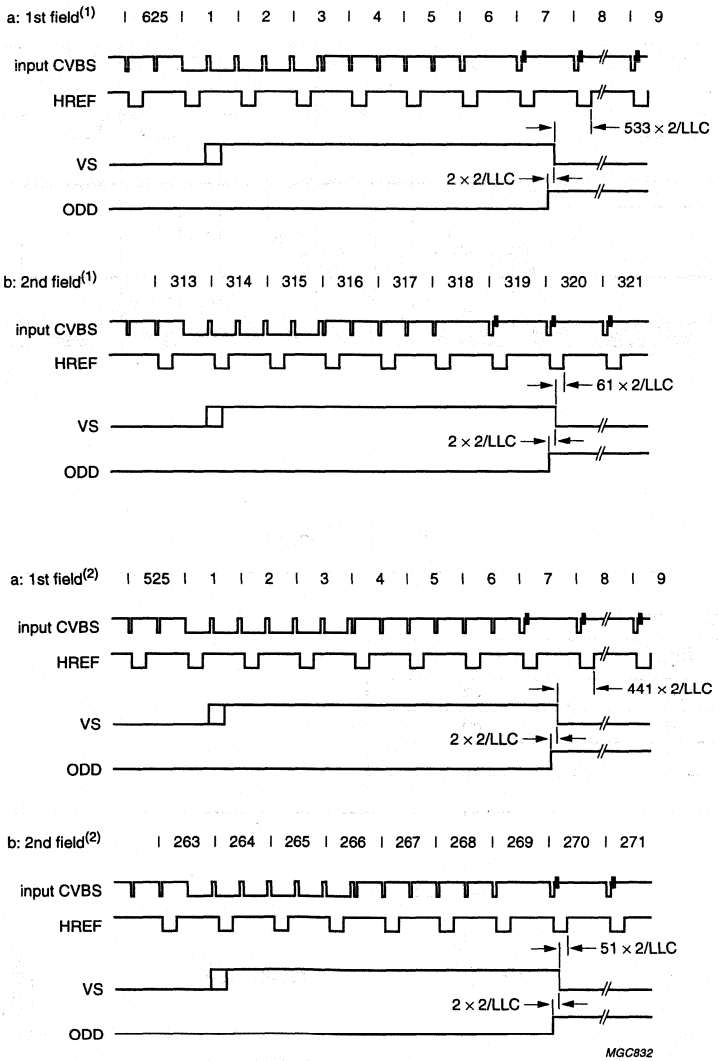


Fig.12 HREF timing.



(1) Nominal input signal 50 Hz.
(2) Nominal input signal 60 Hz.
HRMV = 1 and HRFS = 0.

Fig.13 Vertical timing.

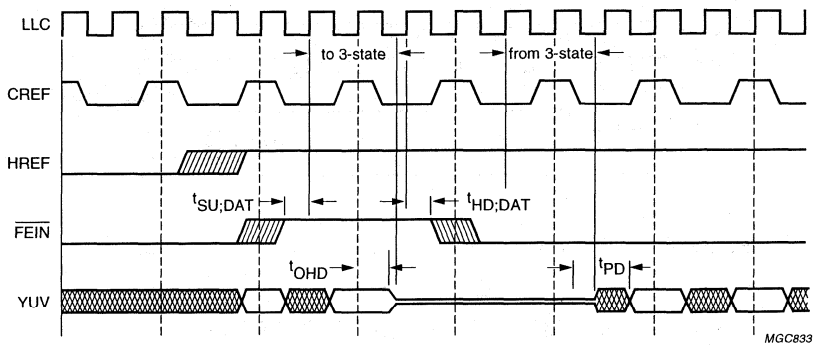
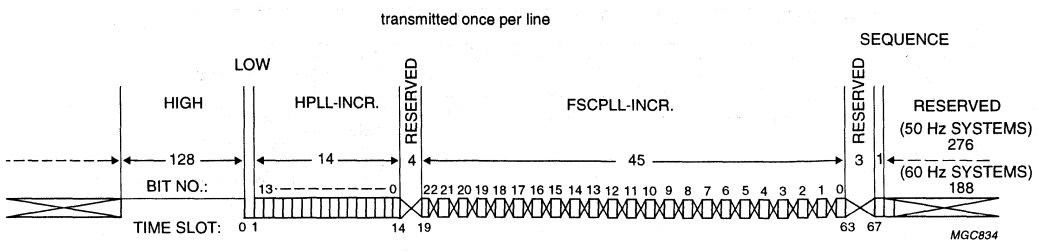


Fig.14 $\overline{\text{FEIN}}$ timing.

Table 2 Digital output control

OEYC	$\overline{\text{FEIN}}$	YUV (15 : 0)
0	0	Z
1	0	active
X	1	Z



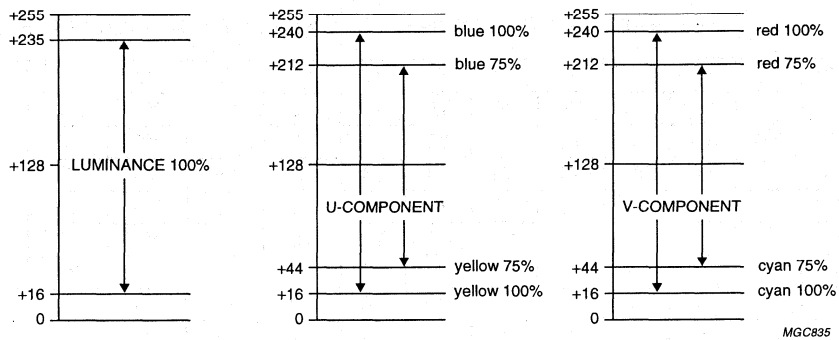
RTCO sequence is generated in LLC/4.
For transmission LLC/2 timing is required.

Fig.15 Real time control output timing.

14 OUTPUT FORMATS

Table 3 Output formats

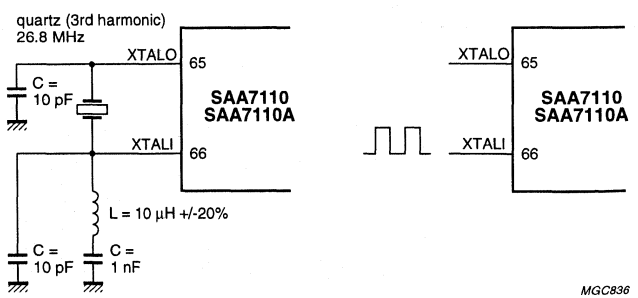
BUS SIGNAL	PIXEL BYTE SEQUENCE 4 : 1 : 1 FORMAT								PIXEL BYTE SEQUENCE 4 : 2 : 2 FORMAT					
Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7
Y6	Y6	Y7	Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6
Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5
Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4
Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3
Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2
Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1
Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0
UV7	U7	U5	U3	U1	U7	U5	U3	U1	U7	V7	U7	V7	U7	V7
UV6	U6	U4	U2	U0	U6	U4	U2	U0	U6	V6	U6	V6	U6	V6
UV5	V7	V5	V3	V1	V7	V5	V3	V1	U5	V5	U5	V5	U5	V5
UV4	V6	V4	V2	V0	V6	V4	V2	V0	U4	V4	U4	V4	U4	V4
UV3	0	0	0	0	0	0	0	0	U3	V3	U3	V3	U3	V3
UV2	0	0	0	0	0	0	0	0	U2	V2	U2	V2	U2	V2
UV1	0	0	0	0	0	0	0	0	U1	V1	U1	V1	U1	V1
UV0	0	0	0	0	0	0	0	0	U0	V0	U0	V0	U0	V0
Y frame	0	1	2	3	4	5	6	7	0	1	2	3	4	5
UV frame	0				4				0		2		4	
	data rate				sample frequency				data rate		sample frequency			
Y	LLC2				LLC2				LLC2		LLC2			
U					LLC4						LLC8			
V					LLC4						LLC8			



a. Y output range. b. U output range (B–Y). c. Y output range (R–Y).

CCIR 601 digital levels.

Fig.16 YUV output signal range.



a. with quartz crystal. b. with external clock.

Fig.17 Oscillator application.

15 CLOCK SYSTEM

15.1 Clock generation circuit

The internal CGC generates the system clocks LLC, LLC2 and the clock reference signal CREF. The internally generated LFCO (triangular waveform) is multiplied by four via the analog PLL (including phase detector, loop filter, VCO and frequency divider). The rectangular output signals have a 50% duty factor.

Table 4 System clock frequencies

CLOCK	FREQUENCY (MHz)	
	50 Hz	60 Hz
XTAL	26.8	26.8
LLC	29.5	24.545454
LLC2	14.75	12.272727
LLC4	7.375	6.136136
LLC8	3.6875	3.068181

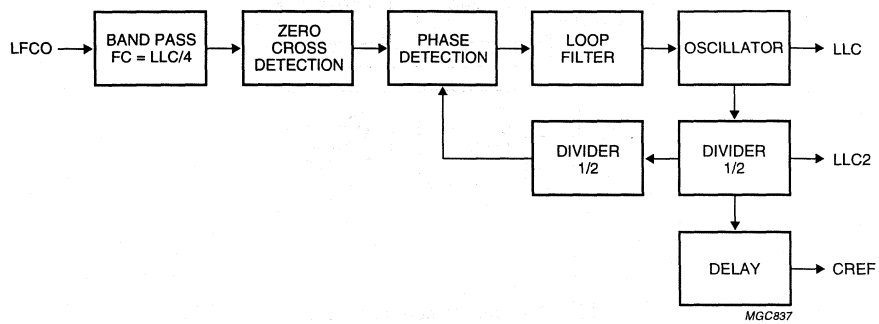


Fig.18 Clock generation circuit.

15.2 Power-on control

Power-on reset is activated at power-on (using only internal CGC) and if the supply voltage falls below 3.5 V. The $\overline{\text{RESET}}$ signal can be applied to reset other circuits of the digital TV system.

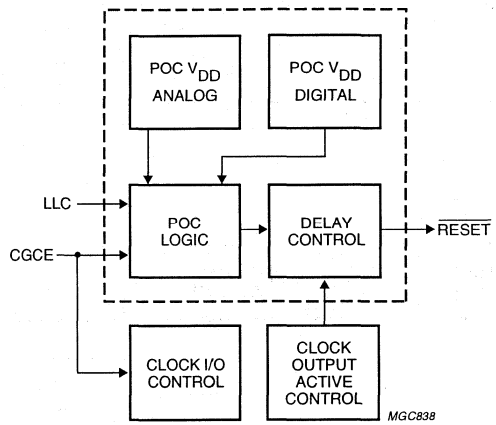


Fig.19 Power-on control circuit.

Table 5 Power-on control sequence

INTERNAL POWER-ON CONTROL SEQUENCE	PIN OUTPUT STATUS	FUNCTION
Directly after power-on asynchronous reset	Y7 to Y0, UV7 to UV0, RTCO, PLIN, ODD, GPSW, SDA, HREF, HS, VS, HCL and HSY in high impedance state LLC, LLC2 and CREF in HIGH state	direct switching to high impedance (outputs) or input mode (I/Os) for 20 to 200 ms
Start synchronous I^2C-bus reset sequence	LLC, LLC2 and CREF active	starting I^2C-bus reset sequence
Status after I^2C-bus reset	Y7 to Y0, UV7 to UV0, HREF and HS held in high impedance state VS, HCL and HSY held in input function mode	**SA0DH = 7DH** (VTRC = 0, RTSE = 1, HRMV = 1, SSTB = 0, SECS = 1) **SA0EH = 00H** (HPLL = 0, OEHV = 0, OEYC = 0, CHRS = 0, GPSW = 0) **SA31H = 00H** (AOSL 1 : 0 = 00, WIRS = 0, WRSE = 0, SQPB = 0, VBLKA = 0, PULIO = 0)
Status after power-on control sequence	RTCO, PLIN, ODD, GPSW and SDA active	after power-on (reset sequence) a complete I^2C-bus transmission is required

16 I²C-BUS DESCRIPTION

16.1 I²C-bus format

S	SLAVE ADDRESS	ACK	SUBADDRESS	ACK	DATA (n bytes)	ACK	P

Table 6 Description of I²C-bus format

CODE	DESCRIPTION
S	START condition
Slave address	1001 110Xb (SA = LOW) or 1001 111Xb (SA = HIGH)
ACK	acknowledge generated by the slave
Subaddress	subaddress byte, see Table 7
Data	data byte, see Table 7; note 1
P	STOP condition
X	read/write control bit: X = 0, order to write (the circuit is slave receiver) X = 1, order to read (the circuit is slave transmitter)
Slave address	9CH for write, 9DH for read (SA = 0)
	9EH for write, 9FH for read (SA = 1
Subaddress	00H to 19H decoder part
	1AH to 1FH reserved
	20H to 34H front-end part

Note

1. If more than one byte DATA is transmitted then the auto-increment of the subaddress is performed.

16.2 I²C-bus receiver/transmitter tables

Table 7 OCF1 RECEIVER

Slave address 10011100b, 9CH (SA = 0) and 10011110b, 9EH (SA = 1)

REGISTER FUNCTION	SUB ADD[1]	DATA BYTE[2]							
		D7	D6	D5	D4	D3	D2	D1	D0
DMSD-SQP + BSC slave receiver (SU 00H to 19H)									
Increment delay	00	007 IDEL7	006 IDEL6	005 IDEL5	004 IDEL4	003 IDEL3	002 IDEL2	001 IDEL1	000 IDEL0
HSY begin 50 Hz	01	015 HSYB7	014 HSYB6	013 HSYB5	012 HSYB4	011 HSYB3	010 HSYB2	009 HSYB1	008 HSYB0
HSY stop 50 Hz	02	023 HSYS7	022 HSYS6	021 HSYS5	020 HSYS4	019 HSYS3	018 HSYS2	017 HSYS1	016 HSYS0
HCL begin 50 Hz	03	031 HCLB7	030 HCLB6	029 HCLB5	028 HCLB4	027 HCLB3	026 HCLB2	025 HCLB1	024 HCLB0
HCL stop 50 Hz	04	039 HCLS7	038 HCLS6	037 HCLS5	036 HCLS4	035 HCLS3	034 HCLS2	033 HCLS1	032 HCLS0
HSY after PHI1 50 Hz	05	047 HPHI7	046 HPHI6	045 HPHI5	044 HPHI4	043 HPHI3	042 HPHI2	041 HPHI1	040 HPHI0
Luminance control	06	055 BYPS	054 PREF	053 BPSS1	052 BPSS0	051 CORI1	050 CORI0	049 APER1	048 APER0
Hue control	07	063 HUEC7	062 HUEC6	061 HUEC5	060 HUEC4	059 HUEC3	058 HUEC2	057 HUEC1	056 HUEC0
Colour killer threshold QUAM (PAL/NTSC)	08	071 CKTQ4	070 CKTQ3	069 CKTQ2	068 CKTQ1	067 CKTQ0	066 XXX	065 XXX	064 XXX
Colour killer threshold SECAM	09	079 CKTS4	078 CKTS3	077 CKTS2	076 CKTS1	075 CKTS0	074 XXX	073 XXX	072 XXX
PAL switch sensitivity	0A	087 PLSE7	086 PLSE6	085 PLSE5	084 PLSE4	083 PLSE3	082 PLSE2	081 PLSE1	080 PLSE0
SECAM switch sensitivity	0B	095 SESE7	094 SESE6	093 SESE5	092 SESE4	091 SESE3	090 SESE2	089 SESE1	088 SESE0
Gain control chrominance	0C	103 COLO	102 LFIS1	101 LFIS0	100 XXX	099 XXX	098 XXX	097 XXX	096 XXX
Standard/mode control	0D	111 VTRC	110 XXX	109 XXX	108 XXX	107 RTSE	106 HRMV	105 SSTB	104 SECS
I/O and clock control	0E	119 HPLL	118 XXX	117 XXX	116 OEHV	115 OEYC	114 CHRS	113 XXX	112 GPSW
Control #1	0F	127 AUFD	126 FSEL	125 SXCR	124 SCEN	123 XXX	122 YDEL2	121 YDEL1	120 YDEL0
Control #2	10	135 XXX	134 XXX	133 XXX	132 XXX	131 XXX	130 HRFS	129 VNOI1	128 VNOI0
Chrominance gain reference	11	143 CHCV7	142 CHCV6	141 CHCV5	140 CHCV4	139 CHCV3	138 CHCV2	137 CHCV1	136 CHCV0
Chrominance saturation	12	151 SATN7	150 SATN6	149 SATN5	148 SATN4	147 SATN3	146 SATN2	145 SATN1	144 SATN0

REGISTER FUNCTION	SUB ADD[1]	DATA BYTE[2]							
		D7	D6	D5	D4	D3	D2	D1	D0
Luminance contrast	13	159 CONT7	158 CONT6	157 CONT5	156 CONT4	155 CONT3	154 CONT2	153 CONT1	152 CONT0
HSY begin 60 Hz	14	167 HS6B7	166 HS6B6	165 HS6B5	164 HS6B4	163 HS6B3	162 HS6B2	161 HS6B1	160 HS6B0
HSY stop 60 Hz	15	175 HS6S7	174 HS6S6	173 HS6S5	172 HS6S4	171 HS6B3	170 HS6S2	169 HS6S1	168 HS6S0
HCL begin 60 Hz	16	183 HC6B7	182 HC6B6	181 HC6B5	180 HCLB4	179 HC6B3	178 HC6B2	177 HC6B1	176 HC6B0
HCL stop 60 Hz	17	191 HC6S7	190 HC6S6	189 HC6S5	188 HC6S4	187 HC6S3	186 HC6S2	185 HC6S1	184 HC6S0
HSY after PHI1 60 Hz	18	199 HP6I7	198 HP6I6	197 HP6I5	196 HP6I4	195 HP6I3	194 HP6I2	193 HP6I1	192 HP6I0
Luminance brightness	19	207 BRIG7	206 BRIG6	205 BRIG5	204 BRIG4	203 BRIG3	202 BRIG2	201 BRIG1	200 BRIG0
DUAD slave receiver (SU 20H to 32H)									
Analog control #1	20	007 AIND4	006 AIND3	005 AIND2	004 FUSE1	003 FUSE0	002 AINS4	001 AINS3	000 AINS2
Analog control #2	21	015 VBCO	014 MS34	013 MX241	012 MX240	011 MS24	010 REFS4	009 REFS3	008 REFS2
Mixer control #1	22	023 GACO1	022 GACO0	021 CSEL	020 YSEL	019 MUYC	018 CLTS	017 MX341	016 MX340
Clamping level control 21	23	031 CLL217	030 CLL216	029 CLL215	028 CLL214	027 CLL213	026 CLL212	025 CLL211	024 CLL210
Clamping level control 22	24	039 CLL227	038 CLL226	037 CLL225	036 CLL224	035 CLL223	034 CLL222	033 CLL221	032 CLL220
Clamping level control 31	25	047 CLL317	046 CLL316	045 CLL315	044 CLL314	043 CLL313	042 CLL312	041 CLL311	040 CLL310
Clamping level control 32	26	055 CLL327	054 CLL326	053 CLL325	052 CLL324	051 CLL323	050 CLL322	049 CLL321	048 CLL320
Gain control analog #1	27	063 HOLD	062 GASL	061 GAI25	060 GAI24	059 GAI23	058 GAI22	057 GAI21	056 GAI20
White peak control	28	071 WIPE7	070 WIPE6	069 WIPE5	068 WIPE4	067 WIPE3	066 WIPE2	065 WIPE1	064 WIPE0
Sync bottom control	29	079 SBOT7	078 SBOT6	077 SBOT5	076 SBOT4	075 SBOT3	074 SBOT2	073 SBOT1	072 SBOT0
Gain control analog #2	2A	087 IWIP1	086 IWIP0	085 GAI35	084 GAI34	083 GAI33	082 GAI32	081 GAI31	080 GAI30
Gain control analog #3	2B	095 IGAI1	094 IGAI0	093 GAI45	092 GAI44	091 GAI43	090 GAI42	089 GAI41	088 GAI40
Mixer control #2	2C	103 CLS4	102 XXX	101 CLS3	100 CLS2	099 XXX	098 XXX	097 TWO3	096 TWO2
Integration value gain	2D	111 IVAL7	110 IVAL6	109 IVAL5	108 IVAL4	107 IVAL3	106 IVAL2	105 IVAL1	104 IVAL0

REGISTER FUNCTION	SUB ADD[1]	DATA BYTE[2]							
		D7	D6	D5	D4	D3	D2	D1	D0
Vertical blanking pulse set	2E	119 VBPS7	118 VBPS6	117 VBPS5	116 VBPS4	115 VBPS3	114 VBPS2	113 VBPS1	112 VBPS0
Vertical blanking pulse reset	2F	127 VBPR7	126 VBPR6	125 VBPR5	124 VBPR4	123 VBPR3	122 VBPR2	121 VBPR1	120 VBPR0
ADCs gain control	30	135 XXX	134 WISL	133 GAS3	132 GAD31	131 GAD30	130 GAS2	129 GAD21	128 GAD20
Mixer control #3	31	143 AOSL1	142 AOSL0	141 WIRS	140 WRSE	139 SQPB	138[3] AFCCS	137 VBLKA	136 PULIO
Integration value white peak	32	151 WVAL7	150 WVAL6	149 WVAL5	148 WVAL4	147 WVAL3	146 WVAL2	145 WVAL1	144 WVAL0
Mixer control #4	33	159 OFTS	158 XXX	157 CHSB	156 XXX	155 CAD3	154 CAD2	153 XXX	152 XXX
Gain update level	34	167 MUD2	166 MUD1	165 GUDL5	164 GUDL4	163 GUDL3	162 GUDL2	161 GUDL1	160 GUDL0

Notes

1. Subaddresses to be reset: 0D to 7DH, 0E and 31 to 00H after $\overline{\text{RESET}}$ = 0 (CGCE = 0) or power-on (CGCE = 1).
2. All reserved XXX-bits must be set to LOW, XX-bit is don't care.
3. AFCCS bit does not exist in SAA7110A due to advanced anti-alias filter characteristic, don't care (XX).

Table 8 OCF1 TRANSMITTER: Byte number 0 (transmitted if SSTB = 0 or after $\overline{\text{RESET}}$ has been 0)
Slave address 10011101b, 9DH (SA = 0) and 10011111b, 9FH (SA = 1

VERSION STATUS BYTE	D7	D6	D5	D4	D3	D2	D1	D0
ID7 to ID0; note 1	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Note

1. ID7 to ID0 indicates the version number of the IC, for example SAA7110A V1 = 01H.

Table 9 OCF1 TRANSMITTER: Byte number 1 (transmitted if SSTB = 1)
Slave address 10011101b, 9DH (SA = 0) and 10011111b, 9FH (SA = 1)

STATUS BYTE FUNCTION	D7	D6	D5	D4	D3	D2	D1	D0
See Table 10 for explanation of bits	STTC	HLCK	FIDT	GLIM	XXX	WIPA	ALTD	CODE

Table 10 Explanation of bits shown in Table 9

BIT	DESCRIPTION
STTC	Status bit for horizontal time constant: LOW = TV time constant; HIGH = VCR time constant.
HLCK	Status bit for locked horizontal frequency: LOW = locked; HIGH = unlocked.
FIDT	Identification bit for detected field frequency: LOW = 50 Hz; HIGH = 60 Hz.
GLIM	Gain value for active luminance is limited (maximum or minimum), active HIGH.
XXX	reserved
WIPA	White peak loop is activated, active HIGH.
ALTD	Status HIGH: line alternating colour burst has been detected (PAL or SECAM).
CODE	Status HIGH: any colour signal has been detected.

16.3 I²C-bus detail

The I²C-bus receiver slave address is 9CH/9EH.

DMSD-SQP slave receiver (SU 00H to 19H).

16.3.1 SUBADDRESS 00 (DATA BYTE 007 to 000)

Table 11 Increment delay IDEL

DECIMAL MULTIPLIER	DELAY TIME (STEP SIZE = 4/LLC)	CONTROL BITS[1]							
		IDEL7	IDEL6	IDEL5	IDEL4	IDEL3	IDEL2	IDEL1	IDEL0
–1	–4	1	1	1	1	1	1	1	1
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
–195	–780 max. value for 60 Hz	0	0	1	1	1	1	0	1
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
–236	–944 max. value for 50 Hz	0	0	0	1	0	1	0	0
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
–256	–1024 outside central counter[2]	0	0	0	0	0	0	0	0

Notes

1. A sign bit, designated A08 and internally set to HIGH, indicates values are always negative.
2. The horizontal PLL does not operate in this condition. The system clock frequency is set to a value fixed by the last update and is within ±7.1% of the nominal frequency.

16.3.2 SUBADDRESS 01 (DATA BYTE 015 to 008)

Table 12 Horizontal synchronization begin 50 Hz (HSYB)

DECIMAL MULTIPLIER	DELAY TIME (STEP SIZE = 2/LLC)	CONTROL BITS							
		HSYB7	HSYB6	HSYB5	HSYB4	HSYB3	HSYB2	HSYB1	HSYB0
+191	−382	1	0	1	1	1	1	1	1
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
−64	+128	1	1	0	0	0	0	0	0

16.3.3 SUBADDRESS 02 (DATA BYTE 023 to 016)

Table 13 Horizontal synchronization stop 50 Hz (HSYS)

DECIMAL MULTIPLIER	DELAY TIME (STEP SIZE = 2/LLC)	CONTROL BITS							
		HSYS7	HSYS6	HSYS5	HSYS4	HSYS3	HSYS2	HSYS1	HSYS0
+191	−382	1	0	1	1	1	1	1	1
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
−64	+128	1	1	0	0	0	0	0	0

16.3.4 SUBADDRESS 03 (DATA BYTE 031 to 024)

Table 14 Horizontal clamping begin 50 Hz (HCLB)

DECIMAL MULTIPLIER	DELAY TIME (STEP SIZE = 2/LLC)	CONTROL BITS							
		HCLB7	HCLB6	HCLB5	HCLB4	HCLB3	HCLB2	HCLB1	HCLB0
+127	−254	0	1	1	1	1	1	1	1
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
−128	+256	1	0	0	0	0	0	0	0

16.3.5 SUBADDRESS 04 (DATA BYTE 039 to 032)

Table 15 Horizontal clamping stop 50 Hz (HCLS)

DECIMAL MULTIPLIER	DELAY TIME (STEP SIZE = 2/LLC)	CONTROL BITS							
		HCLS7	HCLS6	HCLS5	HCLS4	HCLS3	HCLS2	HCLS1	HCLS0
+127	−254	0	1	1	1	1	1	1	1
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
−128	+256	1	0	0	0	0	0	0	0

16.3.6 SUBADDRESS 05 (DATA BYTE 047 to 040)

Table 16 Horizontal synchronization start after PHI1 50 Hz (HPHI)

DECIMAL MULTIPLIER	DELAY TIME (STEP SIZE = 8/LLC)	CONTROL BITS							
		HPHI7	HPHI6	HPHI5	HPHI4	HPHI3	HPHI2	HPHI1	HPHI0
+127	forbidden; outside available central counter range	0	1	1	1	1	1	1	1
↓		↓	↓	↓	↓	↓	↓	↓	↓
+118		0	1	1	1	0	1	1	0
+117	−32 µs (max. negative value)	0	1	1	1	0	1	0	1
−118	+31.7 µs (max. positive value)	1	0	0	0	1	0	1	0
−119	forbidden; outside available central counter range	1	0	0	0	1	0	0	1
↓		↓	↓	↓	↓	↓	↓	↓	↓
−128		1	0	0	0	0	0	0	0

16.3.7 SUBADDRESS 06 (DATA BYTE 055 to 048)

Table 17 Luminance control

FUNCTION		CONTROL BITS
Aperture factor (APER); data bits D1 and D0		
0	0	APER1 = 0; APER0 = 0
1	0.25	APER1 = 0; APER0 = 1
2	0.5	APER1 = 1; APER0 = 0
3	1.0	APER1 = 1; APER0 = 1
Corner correction (CORI) ±LSBs in 8-bit; data bits D3 and D2		
0	0 (OFF)	CORI1 = 0; CORI0 = 0
1	1	CORI1 = 0; CORI0 = 1
2	2	CORI1 = 1; CORI0 = 0
3	3	CORI1 = 1; CORI0 = 1
Aperture bandpass; centre frequency (BPSS); data bits D4 and D5		
4.6 MHz (50 Hz)	3.8 MHz (60 Hz)	BPSS1 = 0; BPSS0 = 0
4.3 MHz (50 Hz)	3.4 MHz (60 Hz)	BPSS1 = 0; BPSS0 = 1
3.0 MHz (50 Hz)	2.5 MHz (60 Hz)	BPSS1 = 1; BPSS0 = 0
3.2 MHz (50 Hz)	2.7 MHz (60 Hz)	BPSS1 = 1; BPSS0 = 1
Prefilter active (PREF); data bit D6		
Bypassed		PREF = 0
Active		PREF = 1
Chrominance trap bypass (BYPS); data bit D7		
Active	CVBS mode	BYPS = 0
Bypassed	S-Video mode	BYPS = 1

16.3.8 SUBADDRESS 07 (DATA BYTE 063 to 056)

Table 18 Hue phase control HUEC

HUE PHASE (DEGREES)	CONTROL BITS							
	HUEC7	HUEC6	HUEC5	HUEC4	HUEC3	HUEC2	HUEC1	HUEC0
+178.6	0	1	1	1	1	1	1	1
↓	↓	↓	↓	↓	↓	↓	↓	↓
0	0	0	0	0	0	0	0	0
↓	↓	↓	↓	↓	↓	↓	↓	↓
−180	1	0	0	0	0	0	0	0

16.3.9 SUBADDRESS 08 CONTROL NUMBER 1 (DATA BYTE 071 to 064)

Table 19 Colour killer threshold QUAM (PAL/NTSC)

THRESHOLD (reference is nominal burst amplitude = 0 dB)	CONTROL BITS				
	CKTQ4	CKTQ3	CKTQ2	CKTQ1	CKTQ0
–30 dB	1	1	1	1	1
↓	↓	↓	↓	↓	↓
–24 dB	1	0	0	0	0
↓	↓	↓	↓	↓	↓
–18 dB	0	0	0	0	0

16.3.10 SUBADDRESS 09 CONTROL NUMBER 2 (DATA BYTE 079 to 072)

Table 20 Colour killer threshold SECAM

THRESHOLD (reference is nominal burst amplitude = 0 dB)	CONTROL BITS				
	CKTS4	CKTS3	CKTS2	CKTS1	CKTS0
–30 dB	1	1	1	1	1
↓	↓	↓	↓	↓	↓
–24 dB	1	0	0	0	0
↓	↓	↓	↓	↓	↓
–18 dB	0	0	0	0	0

16.3.11 SUBADDRESS 0A (DATA BYTE 087 to 080)

Table 21 PAL switch sensitivity

SENSITIVITY	CONTROL BITS							
	PLSE7	PLSE6	PLSE5	PLSE4	PLSE3	PLSE2	PLSE1	PLSE0
Low	1	1	1	1	1	1	1	1
Medium	1	0	0	0	0	0	0	0
High[1]	0	0	0	0	0	0	0	0

Note

1. Sensitivity HIGH means immediate sequence correction.

16.3.12 SUBADDRESS 0B (DATA BYTE 095 to 088)

Table 22 SECAM switch sensitivity

SENSITIVITY	CONTROL BITS							
	SESE7	SESE6	SESE5	SESE4	SESE3	SESE2	SESE1	SESE0
Low	1	1	1	1	1	1	1	1
Medium	1	0	0	0	0	0	0	0
High[1]	0	0	0	0	0	0	0	0

Note

1. Sensitivity HIGH means immediate sequence correction.

16.3.13 SUBADDRESS 0C (DATA BYTE 103 to 096)

Table 23 Gain control chrominance

FUNCTION	CONTROL BITS
AGC loop filter (LFIS); data bits D6 and D5	
Slow time constant	LFIS1 = 0; LFIS0 = 0
Medium time constant	LFIS1 = 0; LFIS0 = 1
Fast time constant	LFIS1 = 1; LFIS0 = 0
Actual chrominance gain frozen	LFIS1 = 1; LFIS0 = 1
Colour on (COLO); data bit D7	
Automatic colour killer	COLO = 0
Colour forced on	COLO = 1

16.3.14 SUBADDRESS 0D (DATA BYTE 111 to 104)

Table 24 Standard/mode control

FUNCTION	CONTROL BITS
SECAM mode bit (SECS); data bit D0	
Other standards	SECS = 0
SECAM mode	SECS = 1
Status byte select (SSTB); data bit D1	
Status byte = 0 (see transmitter)	SSTB 0
Status byte = 1 (see transmitter)	SSTB = 1
HREF position select (HRMV); data bit D2	
HREF position as SAA7191 (8 LLC2 later)	HRMV = 0
HREF normal position	HRMV = 1
Real time outputs mode select (RTSE); data bit D3	
PLIN switched to output pin 39 ODD switched to output pin 40	RTSE = 0
HL switched to output pin 39 VL switched to output pin 40	RTSE = 1
TV/VCR mode select (VTRC); data bit D7	
TV mode	VTRC = 0
VTR mode	VTRC = 1

16.3.15 SUBADDRESS 0E (DATA BYTE 119 to 112)

Table 25 I/O and clock control

FUNCTION	CONTROL BITS
General purpose switch (GPSW); data bit D0	
Switches directly pin 64 GPSW (application dependent); VBLKA = 0	GPSW = 0
	GPSW = 1
Select chrominance input (CHRS); data bit D2	
Controlled by BYPS (subaddress 06) normal position	CHRS = 0
Digital chrominance input switched to second input channel (see Fig.20)	CHRS = 1
Output enable YUV-data (OEYC); data bit D3	
YUV bus high impedance/input	OEYC = 0
Output YUV-bus active	OEYC = 1
Output enable horizontal/vertical synchronization (OEHV); data bit D4	
HS, HREF and VS high impedance/inputs	OEHV = 0
Output HS, HREF and VS active	OEHV = 1
Horizontal PLL clock (HPLL); data bit D7	
PLL closed	HPLL = 0
PLL open, horizontal frequency fixed	HPLL = 1

16.3.16 SUBADDRESS 0F (DATA BYTE 127 to 120)

Table 26 Control number 1

FUNCTION	CONTROL BITS
Luminance delay compensation; steps in 2/LLC (YDEL); data bits D2, D1 and D0	
0 steps	YDEL2 = 0; YDEL1 = 0; YDEL0 = 0
3 steps	YDEL2 = 0; YDEL1 = 1; YDEL0 = 1
–4 steps	YDEL2 = 1; YDEL1 = 0 YDEL1 = 0
Enable or disable of sync and clamp pulses; HSY and HCL (SCEN); data bit D4	
Disable sync and clamp (set to HIGH)	SCEN = 0
Enable sync and clamp	SCEN = 1
SECAM cross colour reduction (SXCR); data bit D5	
Reduction off	SXCR = 0
Reduction on	SXCR = 1
Field selection (FSEL); data bit D6	
50 Hz, 625 lines	FSEL = 0
60 Hz, 525 lines	FSEL = 1
Automatic field detection(AUFD); data bit D7	
Field state directly controlled via FSEL	AUFD = 0
Automatic field detection	AUFD = 1

16.3.17 SUBADDRESS 10 (DATA BYTE 135 to 128)

Table 27 Control number 2

FUNCTION	CONTROL BITS
Vertical noise reduction (VNOI); data bits D1 and D0	
Normal mode	VNOI1 = 0; VNOI0 = 0
Search mode	VNOI1 = 0; VNOI0 = 1
Free running mode	VNOI1 = 1; VNOI0 = 0
Vertical noise reduction bypassed	VNOI1 = 1; VNOI0 = 1
HREF select HRFS (HRFS); data bit D2	
HREF matched to YUV output	HRFS = 0
HREF matched to CVBS input	HRFS = 1

16.3.18 SUBADDRESS 11 (DATA BYTE 143 to 136)

Table 28 Chrominance gain reference value

REFERENCE VALUE	CONTROL BITS							
	CHCV7	CHCV6	CHCV5	CHCV4	CHCV3	CHCV2	CHCV1	CHCV0
Maximum	1	1	1	1	1	1	1	1
CCIR-level for PAL	0	1	0	1	1	0	0	1
CCIR-level for NTSC	0	0	1	0	1	1	0	0
Minimum	0	0	0	0	0	0	0	0

16.3.19 SUBADDRESS 12 (DATA BYTE 150 to 144)

Table 29 Chrominance saturation control

GAIN	CONTROL BITS							
	SATN7	SATN6	SATN5	SATN4	SATN3	SATN2	SATN1	SATN0
1.999 Maximum	0	1	1	1	1	1	1	1
1 CCIR-level	0	1	0	0	0	0	0	0
0 colour off	0	0	0	0	0	0	0	0
–1 inverse chrominance	1	1	0	0	0	0	0	0
–2 inverse chrominance	1	0	0	0	0	0	0	0

16.3.20 SUBADDRESS 13 (DATA BYTE 158 to 152)

Table 30 Luminance contrast control

GAIN	CONTROL BITS							
	CONT7	CONT6	CONT5	CONT4	CONT3	CONT2	CONT1	CONT0
1.999 Maximum	0	1	1	1	1	1	1	1
70 CCIR-level	0	1	0	0	0	1	1	0
1	0	1	0	0	0	0	0	0
0 luminance off	0	0	0	0	0	0	0	0
−1 inverse luminance	1	1	0	0	0	0	0	0
−2 inverse luminance	1	0	0	0	0	0	0	0

16.3.21 SUBADDRESS 14 (DATA BYTE 167 to 160)

Table 31 Horizontal synchronization begin 60 Hz (HS6B)

DECIMAL MULTIPLIER	DELAY TIME (step size = 2/LLC)	CONTROL BITS							
		HS6B7	HS6B6	HS6B5	HS6B4	HS6B3	HS6B2	HS6B1	HS6B0
+191	−382	1	0	1	1	1	1	1	1
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
−64	+128	1	1	0	0	0	0	0	0

16.3.22 SUBADDRESS 15 (DATA BYTE 175 to 168)

Table 32 Horizontal synchronization stop 60 Hz (HS6S)

DECIMAL MULTIPLIER	DELAY TIME (step size = 2/LLC)	CONTROL BITS							
		HS6S7	HS6S6	HS6S5	HS6S4	HS6S3	HS6S2	HS6S1	HS6S0
+191	−382	1	0	1	1	1	1	1	1
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
−64	+128	1	1	0	0	0	0	0	0

16.3.23 SUBADDRESS 16 (DATA BYTE 183 to 176)

Table 33 Horizontal clamping begin 60 Hz (HC6B)

DECIMAL MULTIPLIER	DELAY TIME (step size = 2/LLC)	CONTROL BITS							
		HC6B7	HC6B6	HC6B5	HC6B4	HC6B3	HC6B2	HC6B1	HC6B0
+127	−254	0	1	1	1	1	1	1	1
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
−128	+256	1	0	0	0	0	0	0	0

16.3.24 SUBADDRESS 17 (DATA BYTE 191 to 184)

Table 34 Horizontal clamping stop 60 Hz (HC6S)

DECIMAL MULTIPLIER	DELAY TIME (step size = 2/LLC)	CONTROL BITS							
		HC6S7	HC6S6	HC6S5	HC6S4	HC6S3	HC6S2	HC6S1	HC6S0
+127	−254	0	1	1	1	1	1	1	1
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
−128	+256	1	0	0	0	0	0	0	0

16.3.25 SUBADDRESS 18 (DATA BYTE 199 to 192)

Table 35 Horizontal synchronization start after PHI1 60 Hz (HP6I)

DECIMAL MULTIPLIER	DELAY TIME (step size = 8/LLC)	CONTROL BITS							
		HP6I7	HP6I6	HP6I5	HP6I4	HP6I3	HP6I2	HP6I1	HP6I0
+127	forbidden; outside available central counter range	0	1	1	1	1	1	1	1
↓		↓	↓	↓	↓	↓	↓	↓	↓
+98		0	1	1	0	0	0	1	0
+97	−32 µs (max. negative value)	0	1	1	0	0	0	0	1
−97	+31.7 µs (max. positive value)	1	0	0	1	1	1	1	1
−98	forbidden; outside available central counter range	1	0	0	1	1	1	1	0
↓		↓	↓	↓	↓	↓	↓	↓	↓
−128		1	0	0	0	0	0	0	0

16.3.26 SUBADDRESS 19 (DATA BYTE 207 to 200)

Table 36 Luminance brightness control

OFFSET	CONTROL BITS							
	BRIG7	BRIG6	BRIG5	BRIG4	BRIG3	BRIG2	BRIG1	BRIG0
255 (bright)	1	1	1	1	1	1	1	1
139 (CCIR-level)	1	0	0	0	1	0	1	1
128	1	0	0	0	0	0	0	0
0 (dark)	0	0	0	0	0	0	0	0

16.4 I²C-bus detail (continued)

DUAD slave receiver (SU 20H to 32H).

16.4.1 SUBADDRESS 20 (DATA BYTE 007 to 000)

Table 37 Analog control #1

FUNCTION	CONTROL BITS
Analog input select 2 (AINS2); data bit D0	
Analog input AI22 selected	AINS2 = 0
Analog input AI21 selected	AINS2 = 1
Analog input select 3 (AINS3); data bit D1	
Analog input AI32 selected	AINS3 = 0
Analog input AI31 selected	AINS3 = 1
Analog input select 4 (AINS4); data bit D2	
Analog input AI42 selected	AINS4 = 0
Analog input AI41 selected	AIND4 = 1
Analog function select (FUSE); data bits D4 and D3	
Amplifier plus anti-alias filter bypassed	FUSE1 = 0; FUSE0 = 0
	FUSE1 = 0; FUSE0 = 1
Amplifier active	FUSE1 = 1; FUSE0 = 0
Amplifier plus anti-alias filter active	FUSE1 = 1; FUSE0 = 1
Analog input disable 2 (AIND2); data bit D5	
Analog inputs 2 enabled	AIND2 = 0
Analog inputs 2 disabled	AIND2 = 1
Analog input disable 3 (AIND3); data bit D6	
Analog inputs 3 enabled	AIND3 = 0
Analog inputs 3 disabled	AIND3 = 1
Analog input disable 4 (AIND4); data bit D7	
Analog inputs 4 enabled	AIND4 = 0
Analog inputs 4 disabled	AIND4 = 1

16.4.2 SUBADDRESS 21 (DATA BYTE 015 to 008)

Table 38 Analog control #2

FUNCTION	CONTROL BITS
Reference select channel 2 (REFS2); data bit D0	
Automatic clamping active	REFS2 = 0
Reference level selected	REFS2 = 1
Reference select channel 3 (REFS3); data bit D1	
Automatic clamping active	REFS3 = 0
Reference level selected	REFS3 = 1
Reference select channel 4 (REFS4); data bit D2	
Automatic clamping active	REFS4 = 0
Reference level selected	REFS4 = 1
MUXC select channel 24 (MS24); data bit D3	
Analog MUX2 controlled by MX24	MS24 = 0
Analog MUX2 controlled by MUXC	MS24 = 1
Analog MUX2 control (MX24); data bits D5 and D4	
Adder mode	MX241 = 0; MX240 = 0
Channel 2 on; channel 4 off	MX241 = 0; MX240 = 1
Channel 2 off; channel 4 on	MX241 = 1; MX240 = 0
Both channels off	MX241 = 1; MX240 = 1
MUXC select channel 34 (MS34); data bit D6	
Analog MUX3 controlled by MX34	MS34 = 0
Analog MUX3 controlled by MUXC	MS34 = 1
Vertical blanking control off (VBCO); data bit D7	
Vertical blanking on	VBCO = 0
Vertical blanking off	VBCO = 1

16.4.3 SUBADDRESS 22 (DATA BYTE 023 to 016)

Table 39 Mixer control #1

FUNCTION	CONTROL BITS
Analog MUX3 control (MX34); data bits D1 and D0	
Adder mode	MX341 = 0; MX340 = 0
Channel 3 on; channel 4 off	MX341 = 0; MX340 = 1
Channel 3 off; channel 4 on	MX341 = 1; MX340 = 0
Both channels off	MX341 = 1; MX340 = 1
Clamping function test (CLTS); data bit D2	
Normal clamping mode	CLTS = 0
CLAAn and CLAUn adjusted via CLL32 value for testing (do not use)	CLTS = 1
Fast digital multiplexing channel 2/3 active (MUYC); data bit D3	
Normal mode on CHR channel	MUYC = 0
Multiplex mode on CHR channel for test purposes only (do not use)	MUYC = 1
Luminance select (YSEL); data bit D4	
ADC 2 to CVBS	YSEL = 0
ADC 3 to CVBS	YSEL = 1
Chrominance select (CSEL); data bit D5	
ADC 3 to CHR (MUXC not inverse; MUYC = 1)	CSEL = 0
ADC 2 to CHR (MUXC inverse; MUYC = 1)	CSEL = 1
Automatic gain control (GACO); data bits D7 and D6	
Automatic gain control off	GACO1 = 0; GACO0 = 0
Automatic gain control channel 2	GACO1 = 0; GACO0 = 1
Automatic gain control channel 3	GACO1 = 1; GACO0 = 0
Automatic gain control channel 4	GACO1 = 1; GACO0 = 1

16.4.4 SUBADDRESS 23 (DATA BYTE 031 to 024)

Table 40 Clamping level control 21 CLL21

DECIMAL CLAMP LEVEL	CONTROL BITS							
	CLL217	CLL216	CLL215	CLL214	CLL213	CLL212	CLL211	CLL210
1	0	0	0	0	0	0	0	1
↓	↓	↓	↓	↓	↓	↓	↓	↓
64	0	1	0	0	0	0	0	0
↓	↓	↓	↓	↓	↓	↓	↓	↓
128	1	0	0	0	0	0	0	0
↓	↓	↓	↓	↓	↓	↓	↓	↓
254	1	1	1	1	1	1	1	0

16.4.5 SUBADDRESS 24 (DATA BYTE 039 to 032)

Table 41 Clamping level control 22 CLL22

DECIMAL CLAMP LEVEL	CONTROL BITS							
	CLL227	CLL226	CLL225	CLL224	CLL223	CLL222	CLL221	CLL220
1	0	0	0	0	0	0	0	1
↓	↓	↓	↓	↓	↓	↓	↓	↓
64	0	1	0	0	0	0	0	0
↓	↓	↓	↓	↓	↓	↓	↓	↓
128	1	0	0	0	0	0	0	0
↓	↓	↓	↓	↓	↓	↓	↓	↓
254	1	1	1	1	1	1	1	0

16.4.6 SUBADDRESS 25 (DATA BYTE 047 to 040)

Table 42 Clamping level control 31 CLL31

DECIMAL CLAMP LEVEL	CONTROL BITS							
	CLL317	CLL316	CLL315	CLL314	CLL313	CLL312	CLL311	CLL310
1	0	0	0	0	0	0	0	1
↓	↓	↓	↓	↓	↓	↓	↓	↓
64	0	1	0	0	0	0	0	0
↓	↓	↓	↓	↓	↓	↓	↓	↓
128	1	0	0	0	0	0	0	0
↓	↓	↓	↓	↓	↓	↓	↓	↓
254	1	1	1	1	1	1	1	0

16.4.7 SUBADDRESS 26 (DATA BYTE 055 to 048)

Table 43 Clamping level control 32 CLL32

DECIMAL CLAMP LEVEL	CONTROL BITS							
	CLL327	CLL326	CLL325	CLL324	CLL323	CLL322	CLL321	CLL320
1	0	0	0	0	0	0	0	1
↓	↓	↓	↓	↓	↓	↓	↓	↓
64	0	1	0	0	0	0	0	0
↓	↓	↓	↓	↓	↓	↓	↓	↓
128	1	0	0	0	0	0	0	0
↓	↓	↓	↓	↓	↓	↓	↓	↓
254	1	1	1	1	1	1	1	0

16.4.8 SUBADDRESS 27 (DATA BYTE 063 to 056); GAIN CONTROL ANALOG #1

Table 44 Static gain control channel 2 (GAI2); data bits D5 to D0

DECIMAL MULTIPLIER	GAIN (step size = 0.19 dB)	CONTROL BITS					
		GAI25	GAI24	GAI23	GAI22	GAI21	GAI20
0	−2.82 dB	0	0	0	0	0	0
↓	↓	↓	↓	↓	↓	↓	↓
15	0 dB	0	0	1	1	1	1
↓	↓	↓	↓	↓	↓	↓	↓
31	3 dB	0	1	1	1	1	1
↓	↓	↓	↓	↓	↓	↓	↓
47	6 dB	1	0	1	1	1	1
↓	↓	↓	↓	↓	↓	↓	↓
63	9 dB	1	1	1	1	1	1

Table 45 Gain mode select (GASL); data bit D6

FUNCTION	CONTROL BIT GASL
Difference value integration	0
Fix value integration	1

Table 46 Automatic control integration (HOLD); data bit D7

FUNCTION	CONTROL BIT HOLD
AGC active	0
AGC integration hold (freeze)	1

16.4.9 SUBADDRESS 28 (DATA BYTE 071 to 064)

Table 47 White peak control WIPE

DECIMAL WHITE PEAK LEVEL	CONTROL BITS							
	WIPE7	WIPE6	WIPE5	WIPE4	WIPE3	WIPE2	WIPE1	WIPE0
128	1	0	0	0	0	0	0	0
↓	↓	↓	↓	↓	↓	↓	↓	↓
254	1	1	1	1	1	1	1	0
255 (white peak control off)	1	1	1	1	1	1	1	1

16.4.10 SUBADDRESS 29 (DATA BYTE 079 to 072)

Table 48 Sync bottom control SBOT

DECIMAL SYNC BOTTOM LEVEL	CONTROL BITS							
	SBOT7	SBOT6	SBOT5	SBOT4	SBOT3	SBOT2	SBOT1	SBOT0
1	0	0	0	0	0	0	0	1
↓	↓	↓	↓	↓	↓	↓	↓	↓
254	1	1	1	1	1	1	1	0

16.4.11 Subaddress 2A (data byte 087 to 080); gain control analog #2

Table 49 Static gain control channel 3 (GAI3); data bits D5 to D0

DECIMAL MULTIPLIER	GAIN (step size = 0.19 dB)	CONTROL BITS					
		GAI35	GAI34	GAI33	GAI32	GAI31	GAI30
0	−2.82 dB	0	0	0	0	0	0
↓	↓	↓	↓	↓	↓	↓	↓
15	0 dB	0	0	1	1	1	1
↓	↓	↓	↓	↓	↓	↓	↓
31	3 dB	0	1	1	1	1	1
↓	↓	↓	↓	↓	↓	↓	↓
47	6 dB	1	0	1	1	1	1
↓	↓	↓	↓	↓	↓	↓	↓
63	9 dB	1	1	1	1	1	1

Table 50 Integration factor white peak (IWIP); data bits D7 and D6

FUNCTION	CONTROL BITS
Fast selection	IWIP1 = 0; IWIP0 = 0
	IWIP1 = 0; IWIP0 = 1
	IWIP1 = 1; IWIP0 = 0
Slow selection	IWIP1 = 1; IWIP0 = 1

16.4.12 Subaddress 2B (data byte 095 to 088); gain control analog #3

Table 51 Static gain control channel 4 (GAI4); data bits D5 to D0

DECIMAL MULTIPLIER	GAIN (step size = 0.19 dB)	CONTROL BITS					
		GAI45	GAI44	GAI43	GAI42	GAI41	GAI40
0	−2.82 dB	0	0	0	0	0	0
↓	↓	↓	↓	↓	↓	↓	↓
15	0 dB	0	0	1	1	1	1
↓	↓	↓	↓	↓	↓	↓	↓
31	3 dB	0	1	1	1	1	1
↓	↓	↓	↓	↓	↓	↓	↓
47	6 dB	1	0	1	1	1	1
↓	↓	↓	↓	↓	↓	↓	↓
63	9 dB	1	1	1	1	1	1

Table 52 Integration factor normal gain (IGAI); data bits D7 and D6

FUNCTION	CONTROL BITS
Slow selection	IGAI1 = 0; IGAI0 = 0
	IGAI1 = 0; IGAI0 = 1
	IGAI1 = 1; IGAI0 = 0
Fast selection	IGAI1 = 1; IGAI0 = 1

16.4.13 SUBADDRESS 2C (DATA BYTE 103 to 096)

Table 53 Mixer control #2

FUNCTION	CONTROL BITS
Two's complement channel 2 (TWO2); data bit D0	
Unipolar	TWO2 = 0
Two's complement (normal mode)	TWO2 = 1
Two's complement channel 3 (TWO3); data bit D1	
Unipolar	TWO3 = 0
Two's complement (normal mode)	TWO3 = 1
Clamping level select channel 2 (CLS2); data bit D4	
CLL21 active	CLS2 = 0
CLL22 active	CLS2 = 1
Clamping level select channel 3 (CLS3); data bit D5	
CLL31 active	CLS3 = 0
CLL32 active	CLS3 = 1
Clamping level select channel 4 (CLS4); data bit D7	
CLL2n active	CLS4 = 0
CLL3n active	CLS4 = 1

16.4.14 SUBADDRESS 2D (DATA BYTE 111 to 104)

Table 54 Integration value gain (IVAL)

DECIMAL INTEGRATION VALUE GAIN	CONTROL BITS							
	IVAL7	IVAL6	IVAL5	IVAL4	IVAL3	IVAL2	IVAL1	IVAL0
1	0	0	0	0	0	0	0	1
↓	↓	↓	↓	↓	↓	↓	↓	↓
255	1	1	1	1	1	1	1	1

16.4.15 SUBADDRESS 2E (DATA BYTE 119 to 112)

Table 55 Blanking pulse VBLK-set (VBPS)

DECIMAL MULTIPLIER	SET LINE NUMBER (step size = 2)	CONTROL BITS							
		VBPS7	VBPS6	VBPS5	VBPS4	VBPS3	VBPS2	VBPS1	VBPS0
0	0 after rising edge of VS	0	0	0	0	0	0	0	0
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
131[1]	262 after rising edge of VS	1	0	0	0	0	0	1	1
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
156[2]	312 after rising edge of VS	1	0	0	1	1	1	0	0

Notes

1. Maximum for 60 Hz.
2. Maximum for 50 Hz.

16.4.16 SUBADDRESS 2F (DATA BYTE 127 to 120)

Table 56 Blanking pulse VBLK-reset (VBPR)

DECIMAL MULTIPLIER	RESET LINE NUMBER (step size = 2)	CONTROL BITS							
		VBPR7	VBPR6	VBPR5	VBPR4	VBPR3	VBPR2	VBPR1	VBPR0
0	0 after rising edge of VS	0	0	0	0	0	0	0	0
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
131[1]	262 after rising edge of VS	1	0	0	0	0	0	1	1
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
156[2]	312 after rising edge of VS	1	0	0	1	1	1	0	0

Notes

1. Maximum for 60 Hz.
2. Maximum for 50 Hz.

16.4.17 SUBADDRESS 30 (DATA BYTE 135 to 128)

Table 57 ADCs gain control

FUNCTION	CONTROL BITS
Fix gain ADC channel 2 (GAD2); data bits D1 and D0	
0 dB	GAD21 = 0; GAD20 = 0
0.05 dB	GAD21 = 0; GAD20 = 1
0.10 dB	GAD21 = 1; GAD20 = 0
0.15 dB	GAD21 = 1; GAD20 = 1
Gain ADC select channel 2 (GAS2); data bit D2	
Fix gain via I²C-bus GAD2	GAS2 = 0
Automatic gain via loop	GAS2 = 1
Fix gain ADC channel 3 (GAD3); data bits D4 and D3	
0 dB	GAD31 = 0; GAD30 = 0
0.05 dB	GAD31 = 0; GAD30 = 1
0.10 dB	GAD31 = 1; GAD30 = 0
0.15 dB	GAD31 = 1; GAD30 = 1
Gain ADC select channel 3 (GAS3); data bit D5	
Fix gain via I²C-bus GAD3	GAS3 = 0
Automatic gain via loop	GAS3 = 1
White peak mode select (WISL); data bit D6	
Difference value integration	WISL = 0
Fix value integration	WISL = 1

16.4.18 SUBADDRESS 31 (DATA BYTE 143 to 136)

Table 58 Mixer control #3

FUNCTION	CONTROL BITS
Pulses I/O control (PULIO); data bit D0	
HCL and HSY to input pins	PULIO = 0
HCL and HSY to output pins	PULIO = 1
Pin function switch (VBLKA); data bit D1	
GPSW active (normal)	VBLKA = 0
VBLK test output active	VBLKA = 1
DMSD-SQP bypassed (SQPB); data bit D3	
DMSD data to YUV output	SQPB = 0
A/D data to YUV output for test purposes only (do not use)	SQPB = 1
White peak slow up integration enable (WRSE); data bit D4	
Hold in white peak mode	WRSE = 0
Slow up integration with 1 value in H or V (dependent on WIRS)	WRSE = 1
White peak slow up integration select (WIRS); data bit D5	
Slow up integration with 1 value per line	WRIS = 0
Slow up integration with 1 value per field	WRIS = 1
Analog test select (AOSL); data bits D7 and D6	
AOUT connected to ground	AOSL1 = 0; AOSL0 = 0
AOUT connected to input AD2	AOSL1 = 0; AOSL0 = 0
AOUT connected to input AD3	AOSL1 = 1; AOSL0 = 1
AOUT connected to channel 4	AOSL1 = 1; AOSL0 = 1

16.4.19 SUBADDRESS 32 (DATA BYTE 151 to 144)

Table 59 Integration value white peak (WVAL)

DECIMAL INTEGRATION VALUE WHITE PEAK	CONTROL BITS							
	WVAL7	WVAL6	WVAL5	WVAL4	WVAL3	WVAL2	WVAL1	WVAL0
1	0	0	0	0	0	0	0	1
↓	↓	↓	↓	↓	↓	↓	↓	↓
127 (max.)	0	1	1	1	1	1	1	1

16.4.20 SUBADDRESS 33 (DATA BYTE 159 to 152)

Table 60 Mixer control #4

FUNCTION	CONTROL BITS
Clock select AD2 (CAD2); data bit D2	
LLC for test purposes only (do not use)	CAD2 = 0
LLC/2	CAD2 = 1
Clock select AD3 (CAD3); data bit D3	
LLC for test purposes only (do not use)	CAD3 = 0
LLC/2	CAD3 = 1
Change sign bit UV data (CHSB); data bit D5	
UV output unipolar	CHSB = 0
UV output two's complement	CHSB = 1
Output format select (OFTS); data bit D7	
4 : 1 : 1 format	OFTS = 0
4 : 2 : 2 format	OFTS = 1

16.4.21 SUBADDRESS 34 (DATA BYTE 167 to 160)

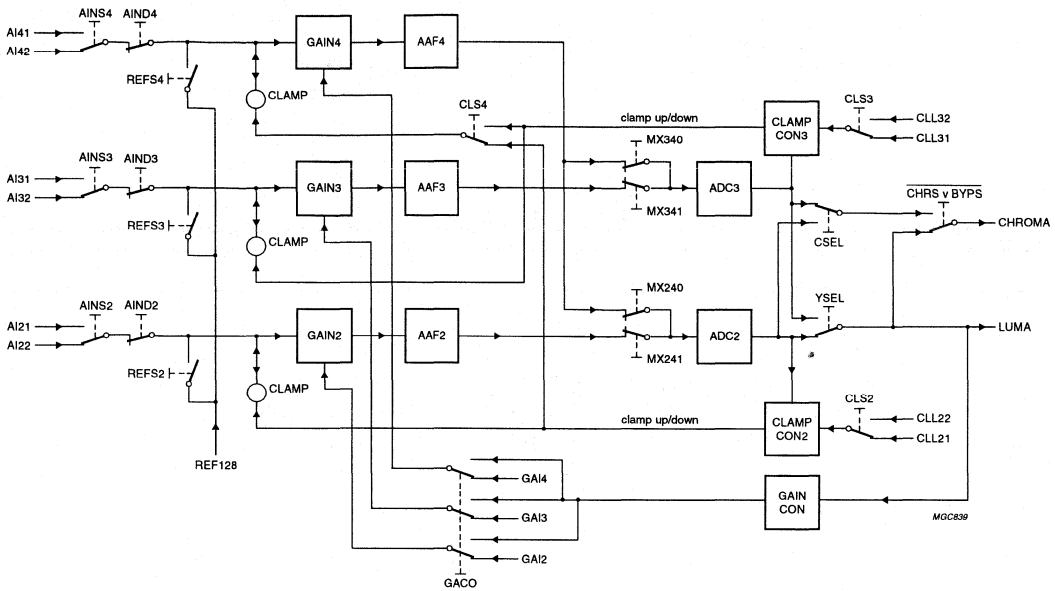
Table 61 Gain update level (GUDL; data bits D5 to D0

DECIMAL	HYSTERESIS FOR 8-BIT GAIN	UPDATE NEW GAIN - OLD GAIN	CONTROL BITS					
			GUDL5	GUDL4	GUDL3	GUDL2	GUDL1	GUDL0
0	0 LSB	>0	0	0	0	0	0	0
↓	↓	↓	↓	↓	↓	↓	↓	↓
7	±7 LSB	>7	0	0	0	1	1	1
↓	↓	↓	↓	↓	↓	↓	↓	↓
>31	off	always	1	X	X	X	X	X

Table 62 MUXC phase delay (MUD2); data bits D7 and D6

FUNCTION	CONTROL BIT MUD
No phase delay	MUD2 = 0; MUD1 = 0
1 LLC cycle phase delay for CLAA path	MUD2 = 0; MUD1 = 1
2 LLC cycle phase delay for CLAA path	MUD2 = 1; MUD1 = 0
3 LLC cycle phase delay for CLAA path	MUD2 = 1; MUD1 = 1

17 SOURCE SELECTION MANAGEMENT



All switch control bits set to LOW.

Fig.20 Source selection overview.

Table 63 Source selection management examples

INPUT	EXAMPLE 1		EXAMPLE 2		EXAMPLE 3		EXAMPLE 4	
	SIGNAL	MODE	SIGNAL	MODE	SIGNAL	MODE	SIGNAL	MODE
AIN21	CVBS1	0	CVBS1	0	Y1	6	Y1	6
AIN22	CVBS2	1	C2	7	C2	7	CVBS2	1
AIN31	CVBS3	2	Y2	7	Y2	7	CVBS3	2
AIN32	CVBS4	3	C3	8	C3	8	CVBS4	3
AIN41	CVBS5	4	Y3	8	Y3	8	CVBS5	4
AIN42	CVBS6	5	CVBS6	5	C1	6	C1	6

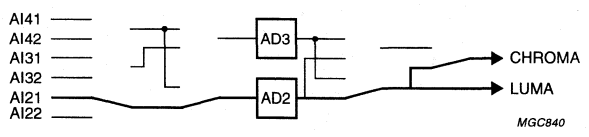


Fig.21 Mode 0; CVBS1.

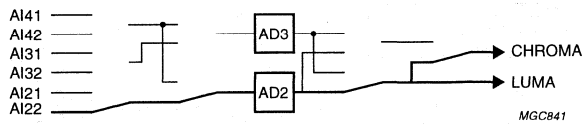


Fig.22 Mode 1; CVBS2.

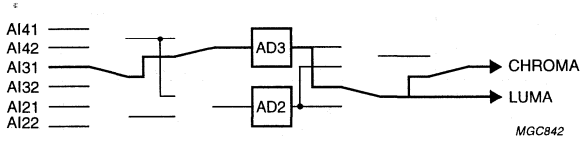


Fig.23 Mode 2; CVBS3.

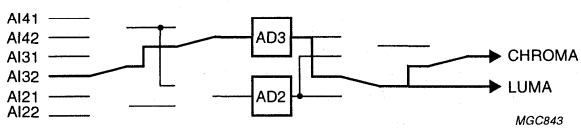


Fig.24 Mode 3; CVBS4.

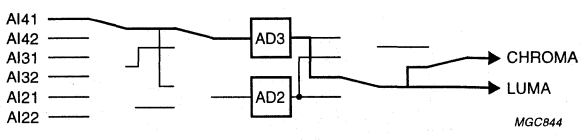


Fig.25 Mode 4; CVBS5.

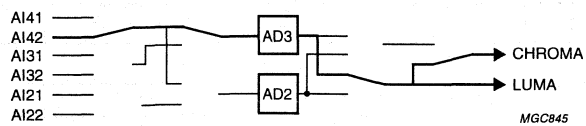


Fig.26 Mode 5; CVBS6.

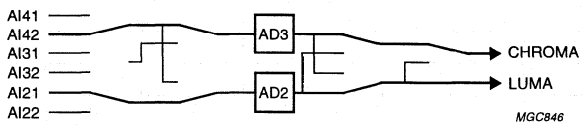


Fig.27 Mode 6; Y1 + C1.

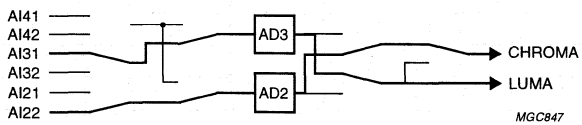


Fig.28 Mode 7; Y2 + C2.

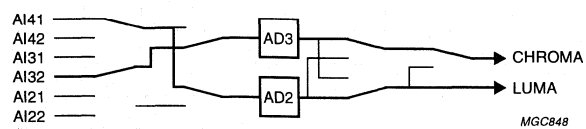


Fig.29 Mode 8; Y3 + C3.

Table 64 I²C-bus control

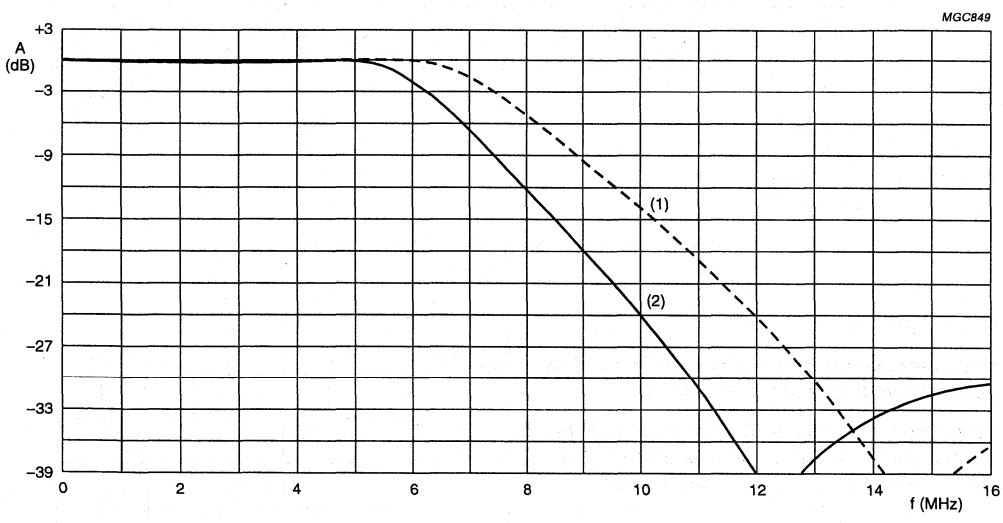
CONTROL INPUT(1)	MODE									
	0	1	2	3	4	5	6	7	8	9
Subaddress 20										
AIND4	1	1	1	1	0	0	0	1	0	–
AIND3	1	1	0	0	1	1	1	0	0	–
AIND2	0	0	1	1	1	1	0	0	1	–
FUSE1	1	–	–	–	–	–	–	–	–	–
FUSE0	1	–	–	–	–	–	–	–	–	–
AINS4	X	X	X	X	1	0	0	X	1	–
AINS3	X	X	1	0	X	X	0	1	0	–
AINS2	1	0	X	X	X	X	1	0	X	–
Subaddress 21										
VBCO	0	–	–	–	–	–	–	–	–	–
MS34	0	–	–	–	–	–	–	–	–	–
MX241	0	0	X	X	X	X	0	0	1	–
MX240	0	0	X	X	X	X	0	0	1	–
MS24	0	–	–	–	–	–	–	–	–	–
REFS4	1	1	1	1	0	0	0	1	0	–
REFS3	1	1	0	0	1	1	1	0	0	–
REFS2	0	0	1	1	1	1	0	0	1	–
Subaddress 22										
GACO1	0	0	1	1	1	1	0	1	1	–
GACO0	1	1	0	0	1	1	1	0	1	–
CSEL	X	X	X	X	X	X	0	1	0	–
YSEL	0	0	1	1	1	1	0	1	0	–
MUYC	0	–	–	–	–	–	–	–	–	0
CLTS	0	–	–	–	–	–	–	–	–	0
MX341	X	X	0	0	1	1	1	0	0	–
MX340	X	X	1	1	0	0	0	1	1	–
Subaddress 2C										
CLS4	X	X	X	X	1	1	1	X	0	–
GABL	0	–	–	–	–	–	–	–	–	–
CLS3	X	X	0	0	0	0	1	0	1	–
CLS2	0	0	X	X	X	X	0	1	X	–
4LSB	0011	–	–	–	–	–	–	–	–	0011
BYPS	0	0	0	0	0	0	1	1	1	–
Subaddresses SU										
20H	D9H	D8H	BAH	B8H	7CH	78H	59H	9AH	3CH	–
21H	16H	16H	05H	05H	03H	03H	12H	14H	21H	–

CONTROL INPUT(1)	MODE									
	0	1	2	3	4	5	6	7	8	9
22H	40H	40H	91H	91H	D2H	D2H	42H	B1H	C1H	–
2CH	03H	03H	03H	03H	83H	83H	A3H	13H	23H	–
06H	0XXXXXXX						1XXXXXXX			–
30H(2)	44H	44H	60H	60H	60H	60H	44H	60H	44H	–

Notes

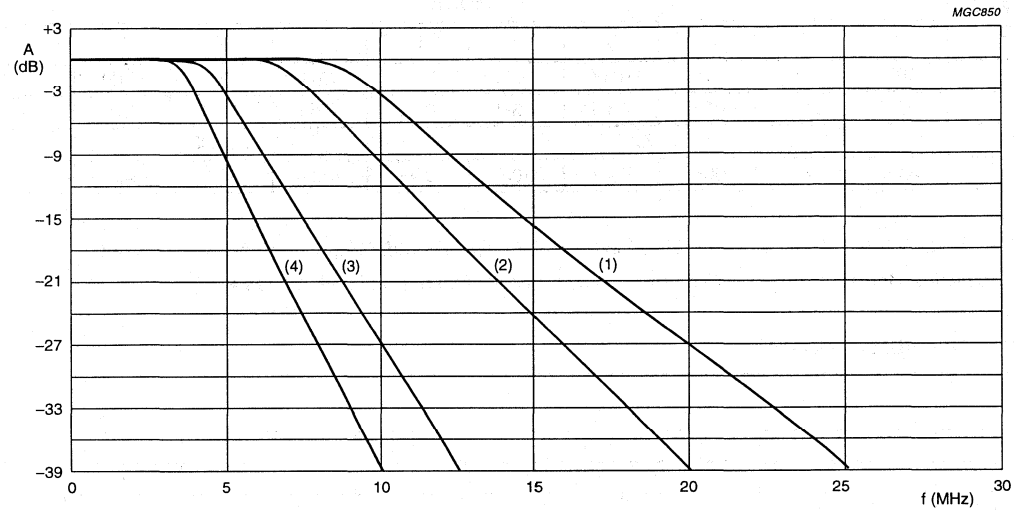
1. CLL21 = 65d, CLL22 = 128d, CLL31 = 65d, CLL32 = 128d, GAI4 = 15d, GAI3 = 15dGAI2 = 15d; X set 0.
2. Optional: values for AD gain (+2 LSB's gain resolution) active [not active: for all modes 40H].

18 ANTI-ALIAS FILTER GRAPHS



(1) 50 Hz.
(2) 60 Hz.

Fig.30 Anti-alias filter graph for **SAA7110A**.



(1) 50 HZ, AFCCS = 0, LLC = 29.50 MHz.
(2) 50 HZ, AFCCS = 1, LLC = 29.50 MHz.
(3) 60 HZ, AFCCS = 0, LLC = 24.54 MHz.
(3) 60 HZ, AFCCS = 1, LLC = 24.54 MHz.

Fig.31 Anti-alias filter graph for **SAA7110**.

19 CORING FUNCTION

19.1 Coring function adjustment by subaddress 06H to affect band filter output adjustment

The thresholds are related to the 13-bit word width in the luminance processing part and influence the 1 to 3 LSB (Yo to Y2) with respect to the 8-bit luminance output.

Table 65 CORI control settings a, b and c of Fig.32

	CONTROL BITS	
	CORI1	**CORI0**
a	0	1
b	1	0
c	1	1

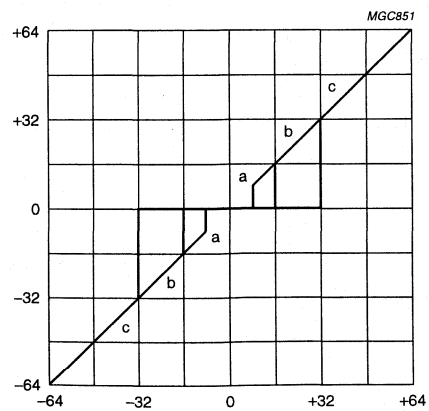


Fig.32 Coring function.

20 LUMINANCE FILTER GRAPHS

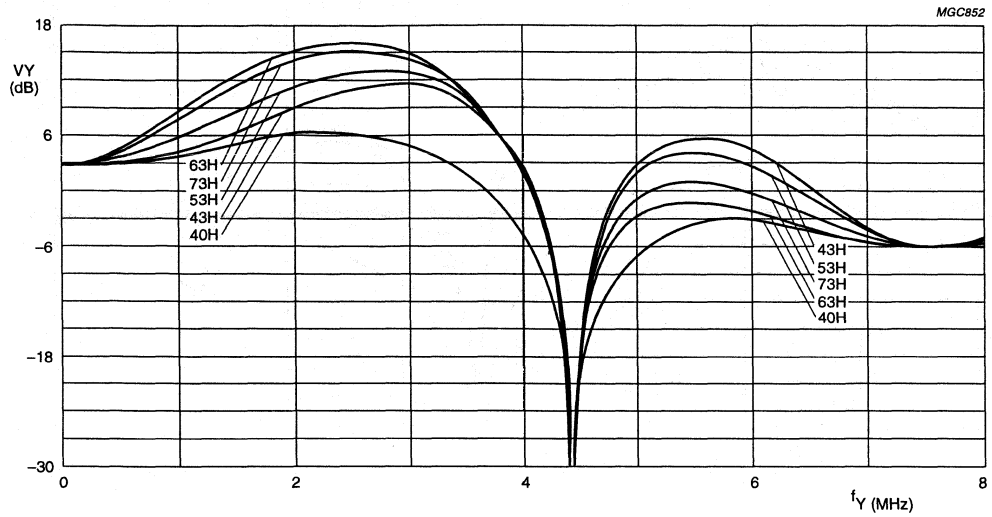


Fig.33 Luminance control: SU06H, 50 Hz/CVBS mode, prefilter on and coring off (40 to 63H).

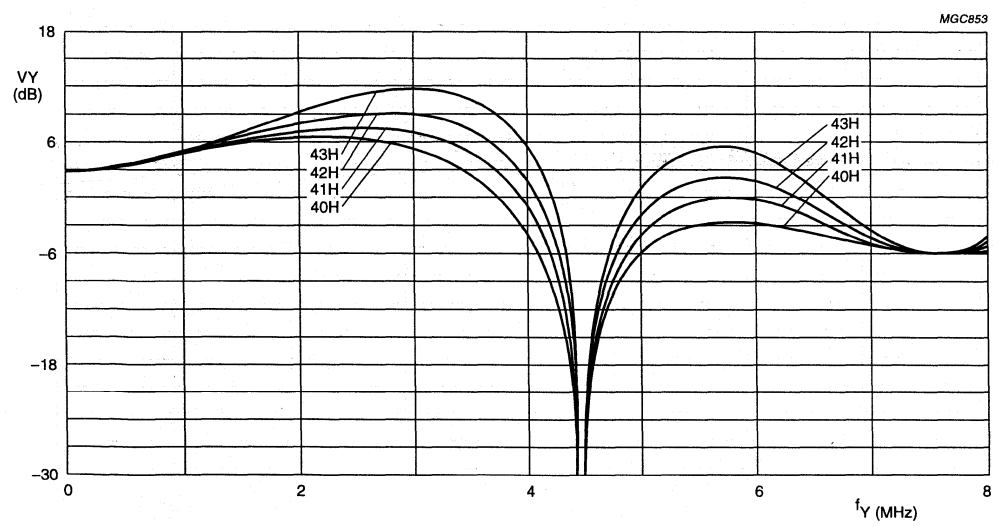


Fig.34 Luminance control: SU06H, 50 Hz/CVBS mode, prefilter on and coring off (40 to 43H).

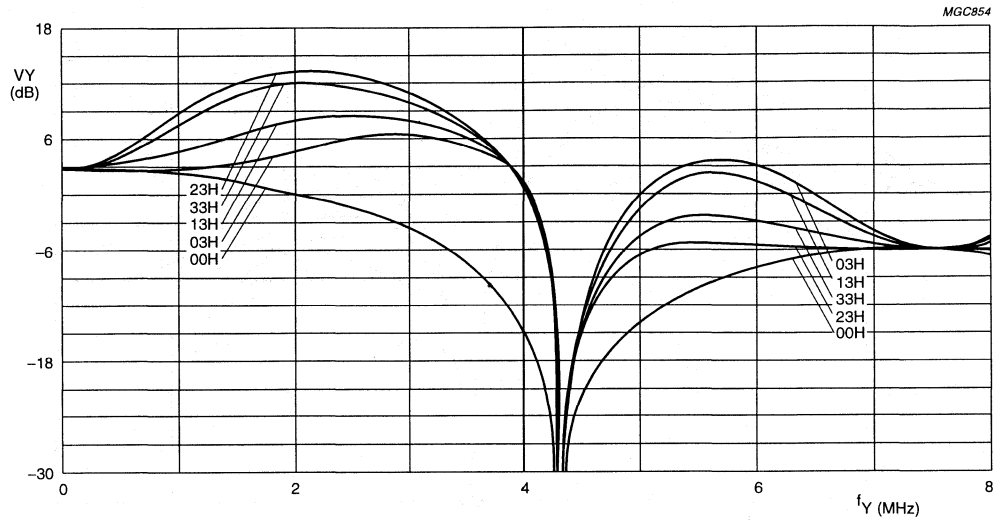


Fig.35 Luminance control: SU06H, 50 Hz/CVBS mode, prefilter off and coring off.

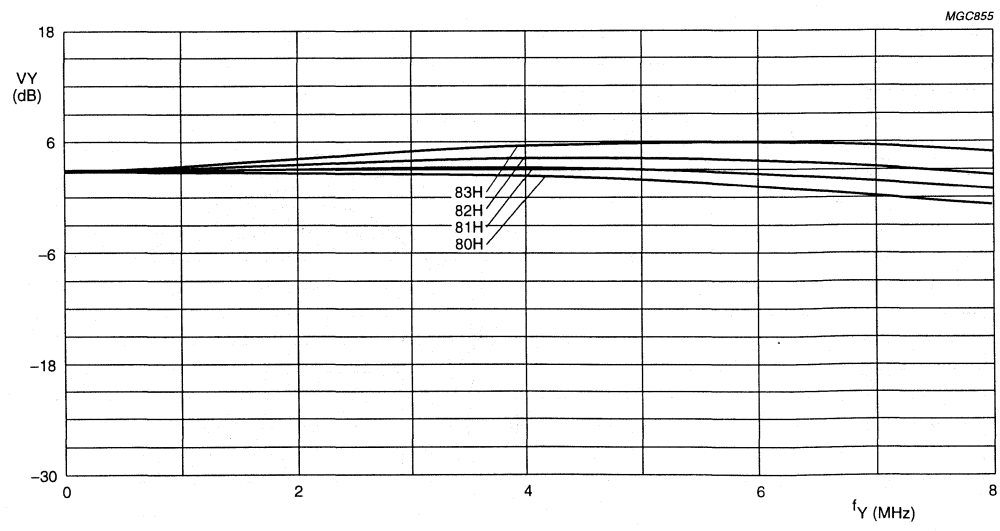


Fig.36 Luminance control: SU06H, 50 Hz/Y + C mode, prefilter off and coring off.

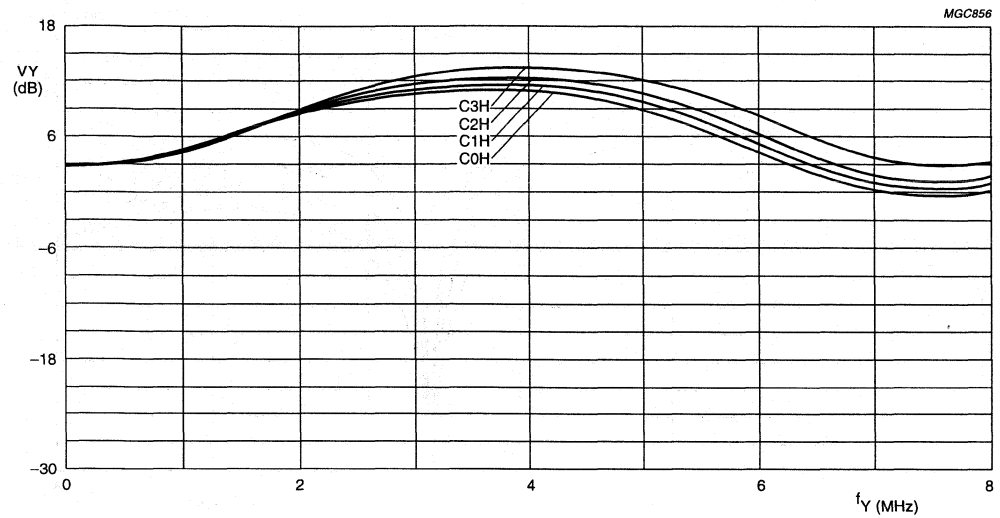


Fig.37 Luminance control: SU06H, 50 Hz/Y + C mode, prefilter on and coring off.

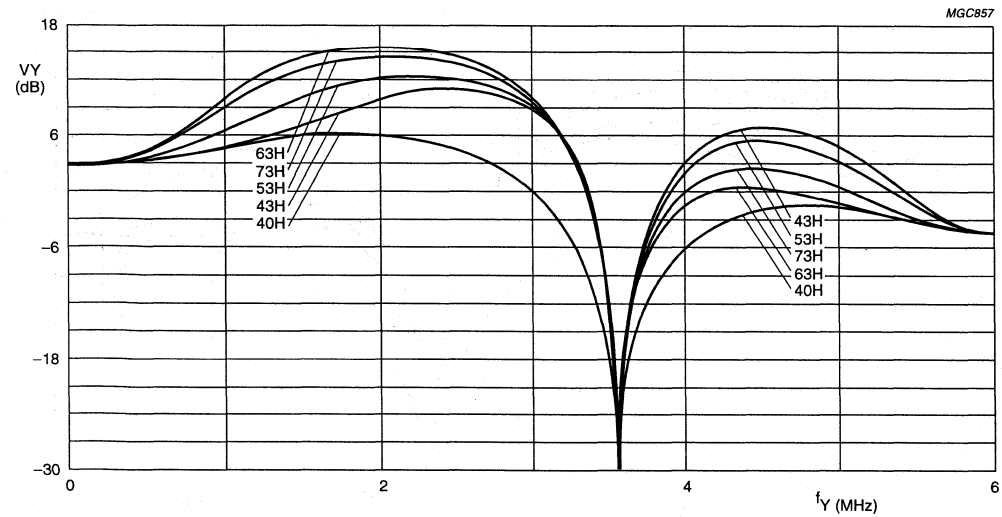


Fig.38 Luminance control: SU06H, 60 Hz/CVBS mode, prefilter on and coring off.

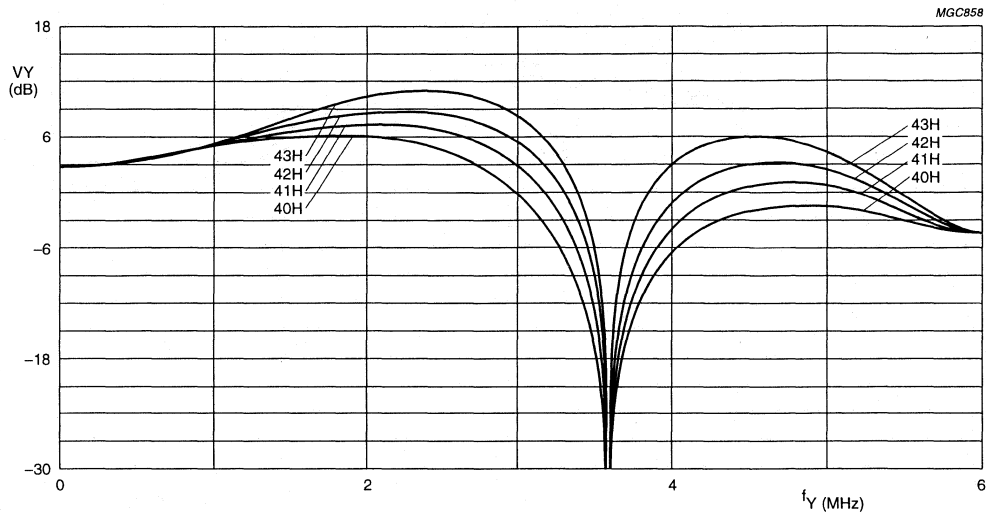


Fig.39 Luminance control: SU06H, 60 Hz/CVBS mode, prefilter on and coring off.

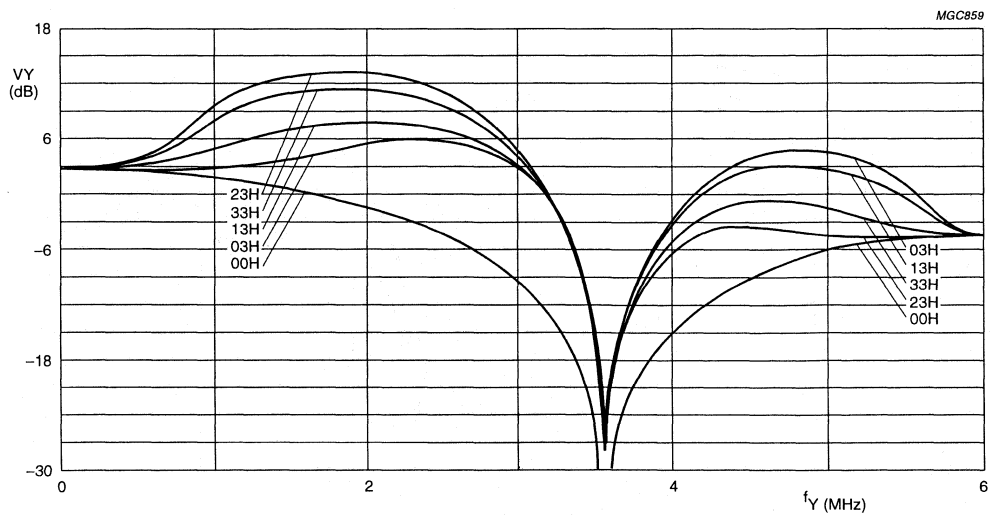


Fig.40 Luminance control: SU06H, 60 Hz/CVBS mode, prefilter off and coring off.

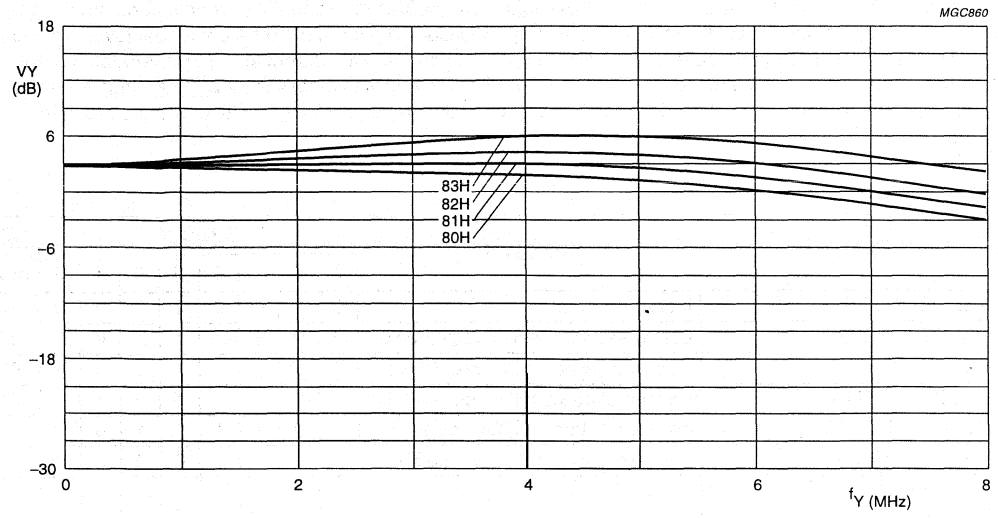


Fig.41 Luminance control: SU06H, 60 Hz/Y + C mode, prefilter off and coring off.

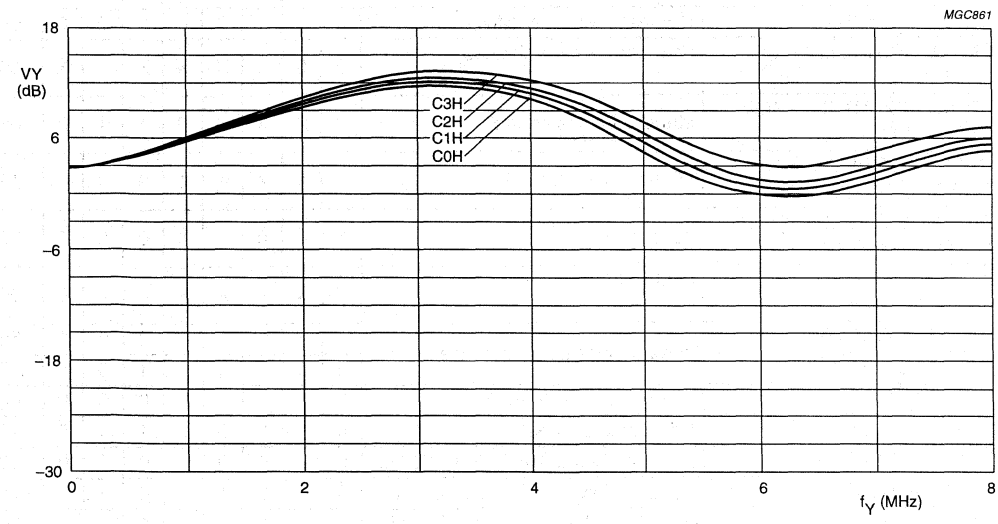


Fig.42 Luminance control: SU06H, 60 Hz/Y + C mode, prefilter on and coring off.

21 I²C-BUS START SET-UP

The values shown in Table 66 are optimized for the EBU colour bar (100% white and 75% chrominance amplitude) signal. The decoder output signal level fulfils the CCIR 601 specification. The input of 100% colour bar level is possible, but the signal (white) peak function reduces the digital luminance output. With a different set-up it is possible to proceed 100% colour bar signal without luminance colour bar reduction. The method is to modify the AD input range for this input level by reducing the gain reference value (SBOT > 06h) and adjusting the digital Y output level with contrast and brightness control.

Table 66 I²C-bus start set-up

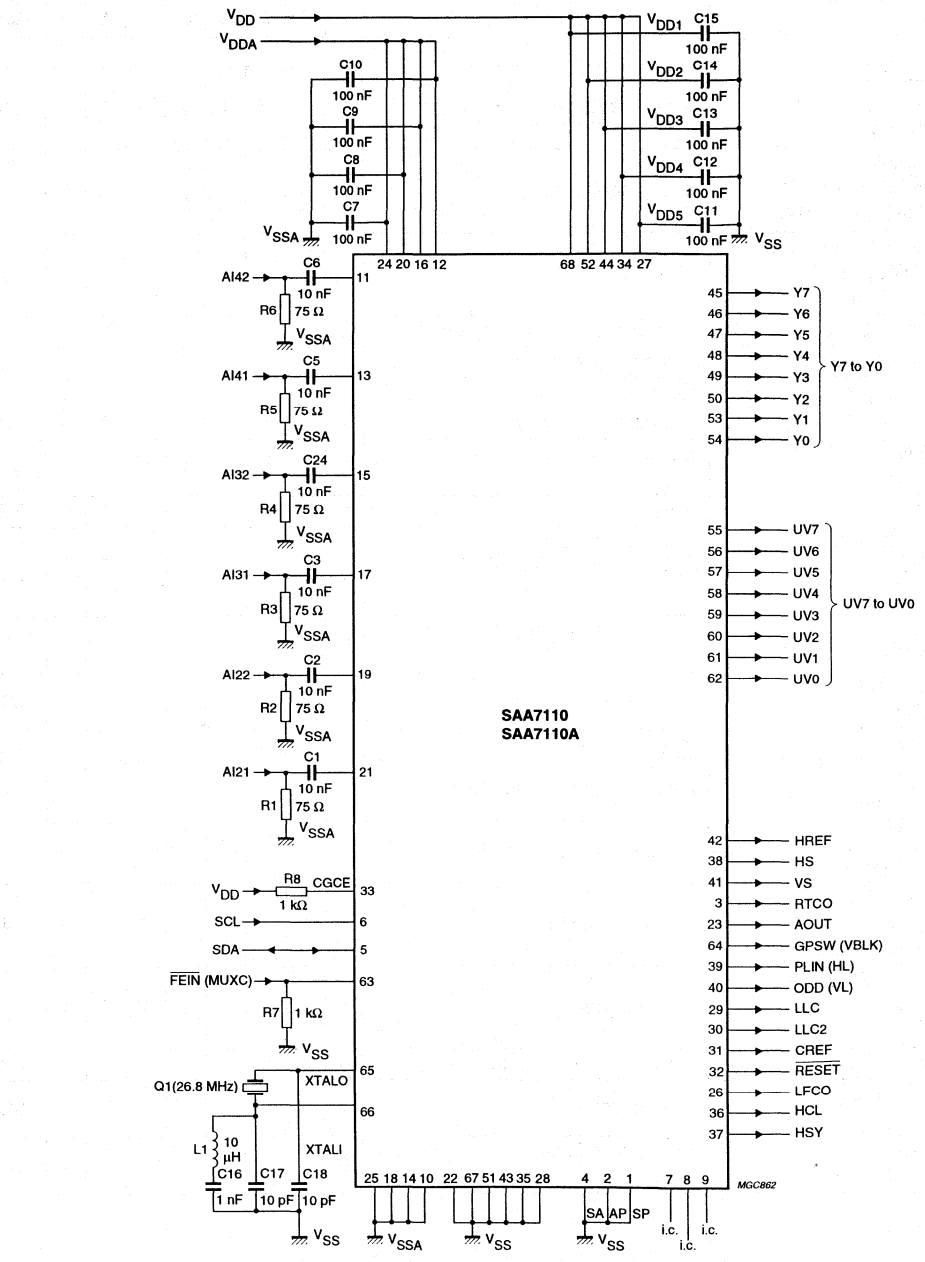
SU	NAME	FUNCTION	BINARY								HEX
			7	6	5	4	3	2	1	0	start
00	IDEL7 to IDEL0	increment delay	0	1	0	0	1	1	0	0	4C
01	HSYB7 to HSYB0	horizontal sync (HSY) begin 50 Hz	0	0	1	1	1	1	0	0	3C
02	HSYS7 to HSYS0	horizontal sync (HSY) stop 50 Hz	0	0	0	0	1	1	0	1	0D
03	HCLB7 to HCLB0	horizontal clamp (HCL) begin 50 Hz	1	1	1	0	1	1	1	1	EF
04	HCLS7 to HCLS0	horizontal clamp (HCL) stop 50 Hz	1	0	1	1	1	1	0	1	BD
05	HPHI7 to HPHI0	horizontal sync after PHI1 50 Hz	1	1	1	1	0	0	0	0	F0
06	BYPS, PREF, BPSS1 to BPSS0, CORI1 to CORI0, APER1 to APER0	luminance control	0	0	0	0	0	0	0	0	00
07	HUEC7 to HUEC0	hue control	0	0	0	0	0	0	0	0	00
08	CKTQ4 to CKTQ0, XXX	colour killer threshold PAL	1	1	1	1	1	X	X	X	F8
09	CKTS4 to CKTS0, XXX	colour killer threshold SECAM	1	1	1	1	1	X	X	X	F8
0A	PLSE7 to PLSE0	PAL switch sensitivity	0	1	1	0	0	0	0	0	60
0B	SESE7 to SESE0	SECAM switch sensitivity	0	1	1	0	0	0	0	0	5B
0C	COLO, LFIS1 to LFIS0, XXXXX	gain control chrominance	0	0	0	X	X	X	X	X	00
0D	VTRC, XXX, RTSE, HRMV, SSTB, SECS	standard/mode control	0	X	X	X	0	1	1	0	06
0E	HPLL, XX, OEHV, OEYC, CHRS, X, GPSW	I/O and clock control	0	X	X	1	1	0	X	0	18
0F	AUFD, FSEL, SXCR, SCEN, X, YDEL2 to YDEL0	control #1	1	0	0	1	X	0	0	0	90
10	XXXXX, HRFS, VNOI1 to VNOI0	control #2	X	X	X	X	X	0	0	0	00
11	CHCV7 to CHCV0 PAL	chrominance gain reference	0	1	0	1	1	0	0	1	59
	CHCV7 to CHCV0 NTSC		0	0	1	0	1	1	0	0	2C
12	SATN7 to SATN0	chrominance saturation	0	1	0	0	0	0	0	0	40
13	CONT7 to CONT0	luminance contrast	0	1	0	0	0	1	1	0	46
14	HS6B7 to HS6B70	horizontal sync (HSY) begin 60 Hz	0	1	0	0	0	0	1	0	42
15	HS6S7 to HS6S0	horizontal sync (HSY) stop 60 Hz	0	0	0	1	1	0	1	0	1A
16	HC6B7 to HC6B0	horizontal clamp (HCL) begin 60 Hz	1	1	1	1	1	1	1	1	FF
17	HC6S7 to HC6S0	horizontal clamp (HCL) stop 60 Hz	1	1	0	1	1	0	1	0	DA
18	HP6I7 to HP6I0	horizontal sync after PHI1 60 Hz	1	1	1	1	0	0	0	0	F0
19	BRIGI7 to BRIG0	luminance brightness	1	0	0	0	1	0	1	1	8B

SU	NAME	FUNCTION	BINARY								HEX
			7	6	5	4	3	2	1	0	start
1A-1F	reserved										
20	AIND4, AIND3, AIND2, FUSE1 to FUSE0, AINS4, AINS3, AINS2	analog control #1	1	1	0	1	1	0	0	1	D9
21	VBCO, MS34, MX241 to MX240, MS24, REFS4, REFS3, REFS2	analog control #2	0	0	0	1	0	1	1	0	16
22	GACO1 to GACO0, CSEL, YSEL, MUYC, CLTS, MX341 to MX340	mixer control #1	0	1	0	0	0	0	0	0	40
23	CLL217 to CLL210	clamping level control channel 21	0	1	0	0	0	0	0	1	41
24	CLL227 to CLL220	clamping level control channel 22	1	0	0	0	0	0	0	0	80
25	CLL317 to CLL310	clamping level control channel 31	0	1	0	0	0	0	0	1	41
26	CLL327 to CLL320	clamping level control channel 32	1	0	0	0	0	0	0	0	80
27	HOLD, GASL, GAI25 to GAI20	gain control analog #1	0	1	0	0	1	1	1	1	4F
28	WIPE7 to WIPE0	white peak control	1	1	1	1	1	1	1	0	FE
29	SBOT7 to SBOT0	sync bottom control	0	0	0	0	0	0	0	1	01
2A	IWIP1 to IWIP0, GAI35 to GAI30	gain control analog #2	1	1	0	0	1	1	1	1	CF
2B	IGAI1 to IGAI0, GAI45 to GAI40	gain control analog #3	0	0	0	0	1	1	1	1	0F
2C	CLS4, X, CLS3, CLS2, TWO3, TWO2	mixer control #2	0	X	0	0	X	X	1	1	03
2D	IVAL7 to IVAL0	integration value gain	0	0	0	0	0	0	0	1	01
2E	VBPS7 to VBPS0; 50 Hz	vertical blanking pulse SET	1	0	0	1	1	0	1	0	9A
	VBPS7 to VBPS0; 60 Hz		1	0	0	0	0	0	0	1	81
2F	VBPR7 to VBPR0; 50 Hz	vertical blanking pulse RESET	0	0	0	0	0	0	1	1	03
	VBPR7 to VBPR0; 60 Hz		0	0	0	0	0	0	1	1	
30	X, WISL, GAS3, GAD31 to GAD30, GAS2, GAD21 to GAD20	ADCs gain control	X	1	0	0	0	0	0	0	44
31	AOSL1 to AOSL0, WIRS, WRSE, SQPB, X, VBLKA, PULIO	mixer control #3	0	1	1	1	0	X*	0	1	71
32	WVAL7 to WVAL0	integration value white peak	0	0	0	0	0	0	1	0	02
33	OFTS, X, CHSB, X, CAD3, CAD2, XX	mixer control #4	1	X	0	X	1	1	X	X	8C
34	MUD2, MUD1, GUDL5 to GUDL0	gain update level	0	0	0	0	0	0	1	1	03

21.1 **Remarks to** Table 66

Values recommended for a CVBS (PAL or NTSC) signal, input AI21 via A/D channel 2 (MODE 0), and 4 : 2 : 2 CCIR output signal level; all X values must be set LOW, X* value is don't care; HPHI and HP6I are application dependent.

22 APPLICATION INFORMATION



Unused analog inputs should not be connected.

Fig.43 Application diagram.

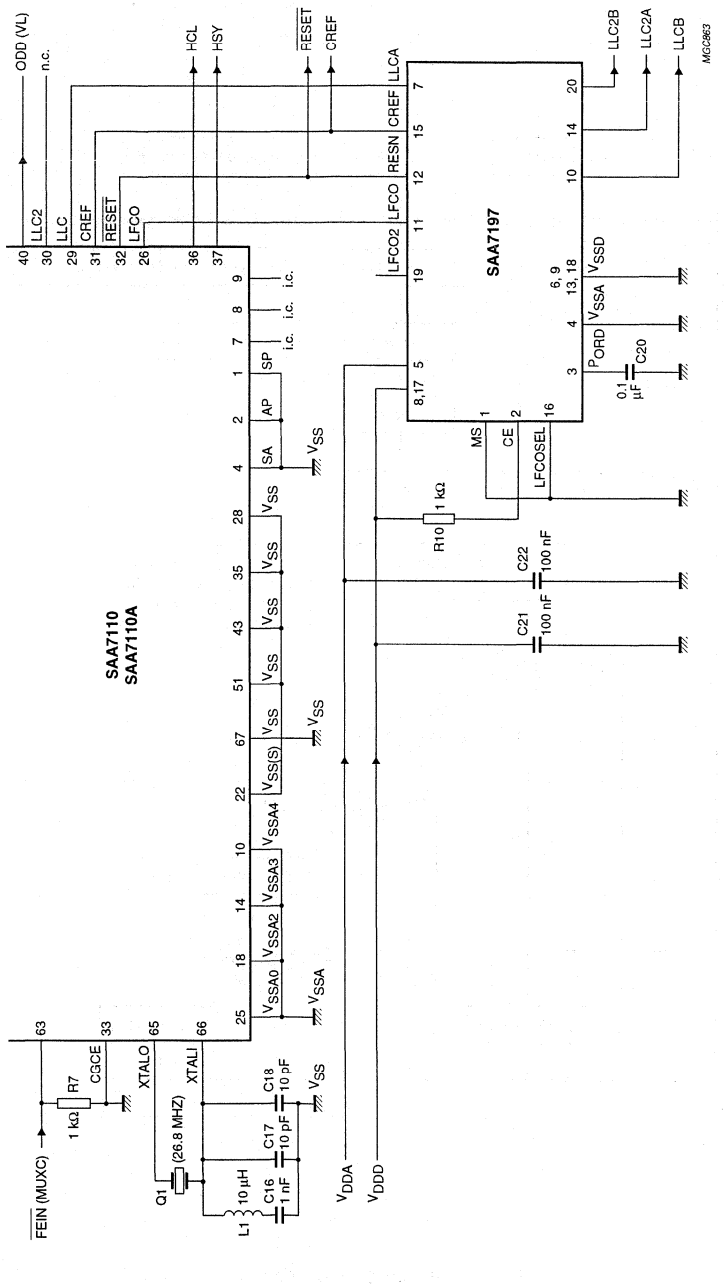


Fig.44 Application diagram with external Clock Generator Circuit (CGC).

The OCF1 supports for special applications the use of an external CGC (SAA7197). For normal operation the built-in CGC fulfils all requirements.

23 START-UP, SOURCE SELECT AND STANDARD DETECTION FLOW EXAMPLE

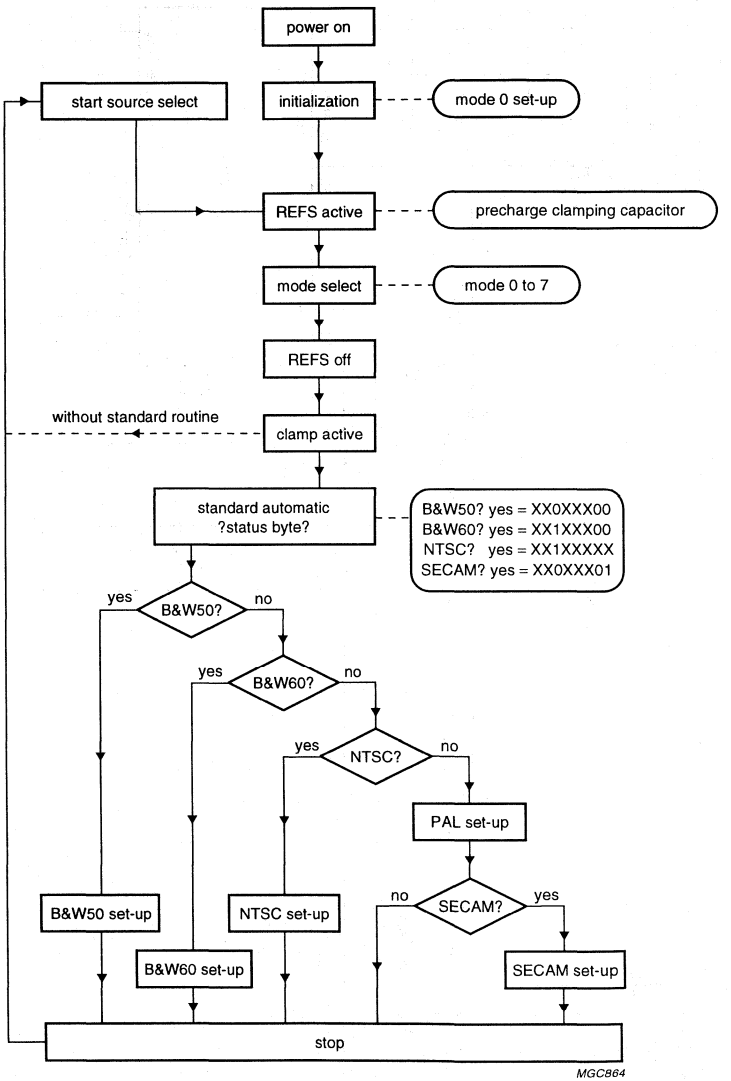


Fig.45 Software flow example.

23.1 CODE 0 STARTUP and STANDARD Procedure

```
SLAVE 9C            !OCF1 NTSC-setup
SUB 00 WRITE
4C 3C 0D EF BD F0 00 00
F8 F8 60 60 00 06 18 90
00 2C 40 46 42 1A FF DA
F0 8B 00 00 00 00 00 00
D9 17 40 41 80 41 80 4F
FE 01 CF 0F 03 01 81 03
44 75 01 8C 03
SUB 21 WRITE 16     !REFS OFF CLAMP AKTIV
READ 1              !Status?
#STANDARD
IF 1 @XX0XXX00      !NO COLOR
THEN GOTO BW_50Hz
ENDIF
IF 1 @XX1XXX00      !NO COLOR
THEN GOTO BW_60Hz
ENDIF
SUB 06 WRITE 00
ENDIF
IF 1 @XX1XXXXX      !60Hz
THEN GOTO NTSC
ENDIF
IF 1 @XX0XXXXX      !50Hz
THEN GOTO PAL
ENDIF
#BW_50Hz
PRINT "BLACK&WHITE"
SUB 06 WRITE 80
SUB 2E WRITE 9A     !VBPS
GOTO STOP
#BW_60Hz
PRINT "BLACK&WHITE"
SUB 06 WRITE 80
SUB 2E WRITE 81     !VBPS
GOTO STOP
#NTSC
SUB 0D WRITE 06     !SECS -> 0
SUB 11 WRITE 2C     !CHCV
SUB 2E WRITE 81     !VBPS
PRINT "NTSC"
GOTO STOP
#PAL
SUB 0D WRITE 06     !SECS -> 0
SUB 11 WRITE 59     !CHCV
SUB 2E WRITE 9A     !VBPS
PAUSE %150          !150ms
IF 1 @XX0XXX01
THEN GOTO SECAM
ELSE PRINT "PAL"
GOTO STOP
#SECAM
SUB 0D WRITE 07     !SECS -> 1
PRINT "SECAM"
GOTO STOP
#STOP
```

23.2 MODE 0 Source Select Procedure

```
SLAVE 9C            !OCF1
SUB 06 WRITE 00     !CVBS MODE 0
SUB 20 WRITE D9     !AI21 ACTIVE
SUB 21 WRITE 17     !REFS ON
SUB 22 WRITE 40     !AD2->LUMA and CHROMA
SUB 2C WRITE 03     !CLAMP SELECT
SUB 30 WRITE 44     !Gain AD2 active
SUB 31 WRITE 75     !AOSL -> 01b
SUB 21 WRITE 16     !REFS OFF CLAMP AKTIV
```

23.3 MODE 1 Source Select Procedure

```
SLAVE 9C            !OCF1
SUB 06 WRITE 00     !CVBS MODE 1
SUB 20 WRITE D8     !AI22 ACTIVE
SUB 21 WRITE 17     !REFS ON
SUB 22 WRITE 40     !AD2->LUMA and CHROMA
SUB 2C WRITE 03     !CLAMP SELECT
SUB 30 WRITE 44     !Gain AD2 active
SUB 31 WRITE 75     !AOSL -> 01b
SUB 21 WRITE 16     !REFS OFF CLAMP AKTIV
```

23.4 MODE 2 Source Select Procedure

```
SLAVE 9C            !OCF1
SUB 06 WRITE 00     !CVBS MODE 2
SUB 20 WRITE BA     !AI31 ACTIVE
SUB 21 WRITE 07     !REFS ON
SUB 22 WRITE 91     !AD3->LUMA and CHROMA
SUB 2C WRITE 03     !CLAMP SELECT
SUB 30 WRITE 60     !Gain AD3 active
SUB 31 WRITE B5     !AOSL -> 10b
SUB 21 WRITE 05     !REFS OFF CLAMP AKTIV
```

23.5 MODE 3 Source Select Procedure

```
SLAVE 9C            !OCF1
SUB 06 WRITE 00     !CVBS MODE 3
SUB 20 WRITE B8     !AI32 ACTIVE
SUB 21 WRITE 07     !REFS ON
SUB 22 WRITE 91     !AD3->LUMA and CHROMA
SUB 2C WRITE 03     !CLAMP SELECT
SUB 30 WRITE 60     !Gain AD3 active
SUB 31 WRITE B5     !AOSL -> 10b
SUB 21 WRITE 05     !REFS OFF CLAMP AKTIV
```

23.6 MODE 4 Source Select Procedure

```
SLAVE 9C            !OCF1
SUB 06 WRITE 00     !CVBS MODE 4
SUB 20 WRITE 7C     !AI41 ACTIVE
SUB 21 WRITE 07     !REFS ON
SUB 22 WRITE D2     !AD3->LUMA and CHROMA
SUB 2C WRITE 83     !CLAMP SELECT
SUB 30 WRITE 60     !Gain AD3 active
SUB 31 WRITE B5     !AOSL -> 10b
SUB 21 WRITE 03     !REFS OFF CLAMP AKTIV
```

23.7 MODE 5 Source Select Procedure

```
SLAVE 9C            !OCF1
SUB 06 WRITE 00     !CVBS MODE 5
SUB 20 WRITE 78     !AI41 ACTIVE
SUB 21 WRITE 07     !REFS ON
SUB 22 WRITE D2     !AD3->LUMA and CHROMA
SUB 2C WRITE 83     !CLAMP SELECT
SUB 30 WRITE 60     !Gain AD3 active
SUB 31 WRITE B5     !AOSL -> 10b
SUB 21 WRITE 03     !REFS OFF CLAMP AKTIV
```

23.8 MODE 6 Source Select Procedure

```
SLAVE 9C            !OCF1
SUB 06 WRITE 80     !Y+C MODE 6
SUB 20 WRITE 59     !AI21=Y, AI42=C
SUB 21 WRITE 17     !REFS ON
SUB 22 WRITE 42     !AD2->LUMA, AD3->CHR
SUB 2C WRITE A3     !CLAMP SELECT
SUB 30 WRITE 44     !Gain AD2 active
SUB 31 WRITE 75     !AOSL -> 01
SUB 21 WRITE 12     !REFS OFF CLAMP AKTIV
```

23.9 MODE 7 Source Select Procedure

```
SLAVE 9C            !OCF1
SUB 06 WRITE 80     !Y+C MODE 7
SUB 20 WRITE 9A     !AI31=Y, AI22=C
SUB 21 WRITE 17     !REFS ON
SUB 22 WRITE B1     !AD3->LUMA, AD2->CHR
SUB 2C WRITE 13     !CLAMP SELECT
SUB 30 WRITE 60     !Gain AD3 active
SUB 31 WRITE B5     !AOSL -> 10b
SUB 21 WRITE 14     !REFS OFF CLAMP AKTIV
```

23.10 MODE 8 Source Select Procedure

```
SLAVE 9C            !OCF1
SUB 06 WRITE 80     !Y+C MODE 8
SUB 20 WRITE 3C     !AI41=Y, AI32=C
SUB 21 WRITE 27     !REFS ON
SUB 22 WRITE C1     !AD2->LUMA, AD3->CHR
SUB 2C WRITE 23     !CLAMP SELECT
SUB 30 WRITE 44     !Gain AD2 active
SUB 31 WRITE 75     !AOSL -> 01
SUB 21 WRITE 21     !REFS OFF CLAMP AKTIV
```

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1 FEATURES

- Four analog inputs, internal analog source selectors, e.g. 4 × CVBS or 2 × Y/C or (1 × Y/C and 2 × CVBS)
- Two analog preprocessing channels
- Fully programmable static gain for the main channels or automatic gain control for the selected CVBS or Y/C channel
- Switchable white peak control
- Two built-in analog anti-aliasing filters
- Two 8-bit video CMOS analog-to-digital converters (ADCs)
- On-chip clock generator
- Line-locked system clock frequencies
- Digital PLL for H-sync processing and clock generation
- Requires only one crystal (24.576 MHz) for all standards
- Horizontal and vertical sync detection
- Automatic detection of 50/60 Hz field frequency, and automatic switching between standards PAL and NTSC
- Luminance and chrominance signal processing for PAL BGHI, PAL N, PAL M, NTSC M, NTSC N and NTSC 4.43
- User programmable luminance peaking or aperture correction
- Cross-colour reduction for NTSC by chrominance comb filtering
- PAL delay line for correcting PAL phase errors
- Real time status information output (RTCO)
- Brightness Contrast Saturation (BCS) control on-chip
- The YUV (CCIR-601) bus supports a data rate of:
  - $864 \times f_H = 13.5$ MHz for 625 line sources
  - $858 \times f_H = 13.5$ MHz for 525 line sources
- Data output streams for 16, 12 or 8-bit width with the following formats:
  - 411 YUV (12-bit)
  - 422 YUV (16-bit)
  - 422 YUV [CCIR-656] (8-bit)
  - 565 RGB (16-bit) with dither
  - 888 RGB (24-bit) with special application
- 720 active samples per line on the YUV bus
- One user programmable general purpose switch on an output pin
- Built in line-21 text slicer
- Power-on control
- Two switchable outputs for the digitized CVBS or Y/C input signals AD1 (7 to 0) and AD2 (7 to 0) via the I²C-bus
- Chip enable function (reset for the clock generator)
- Compatible with memory-based features (line-locked clock)
- Boundary scan test circuit complies with the *"IEEE Std. 1149.1 – 1990"* (ID-Code = 0 7111 02 B)
- I²C-bus controlled (full read-back ability by an external controller).

2 APPLICATIONS

- Desktop video
- Multimedia
- Digital television
- Image processing
- Video phone.

3 GENERAL DESCRIPTION

The Video Input Processor (VIP) is a combination of a two-channel analog preprocessing circuit including source selection, anti-aliasing filter and ADC, an automatic clamp and gain control, a Clock Generation Circuit (CGC), a digital multi-standard decoder (PAL BGHI, PAL M, PAL N, NTSC M and NTSC N), a brightness/contrast/saturation control circuit and a colour space matrix (see Fig.1).

The CMOS circuit SAA7111, analog front-end and digital video decoder, is a highly integrated circuit for desktop video applications. The decoder is based on the principle of line-locked clock decoding and is able to decode the colour of PAL and NTSC signals into CCIR-601 compatible colour component values. The SAA7111 accepts as analog inputs CVBS or S-video (Y/C) from TV or VTR sources. The circuit is I²C-bus controlled.

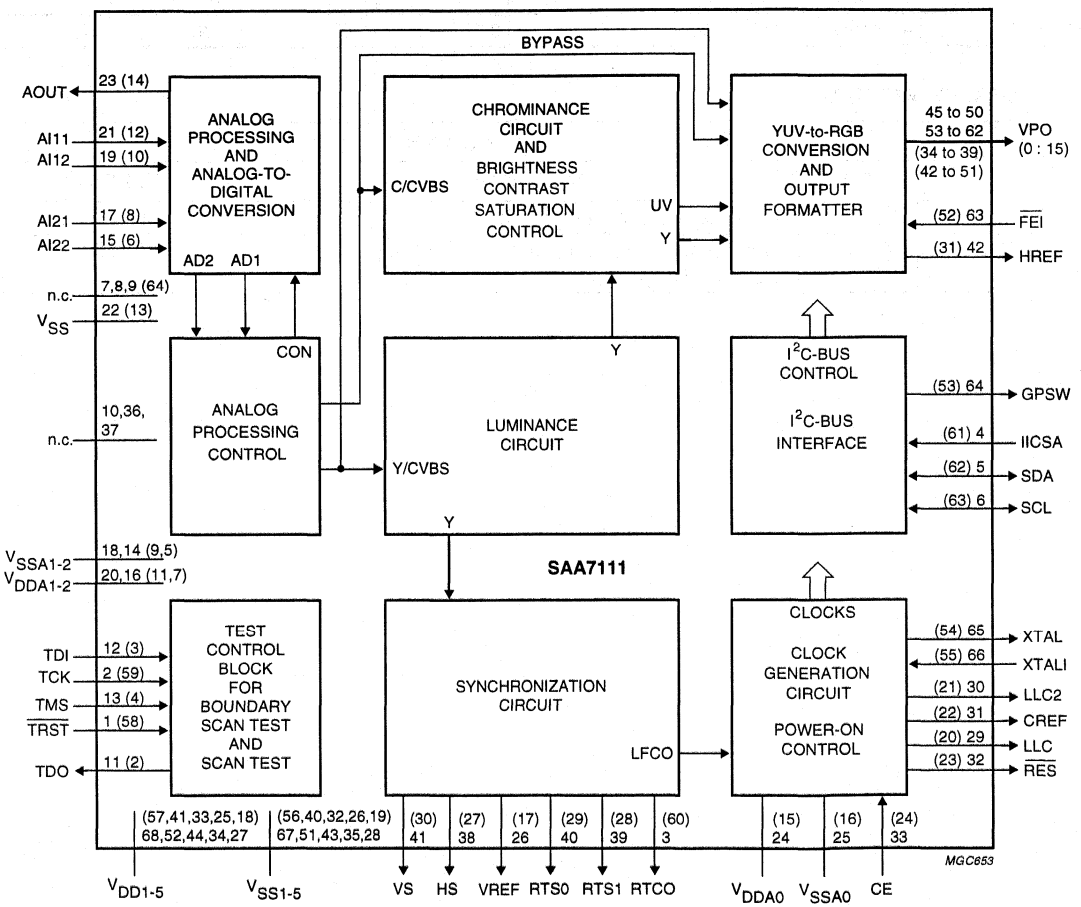
4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage	4.5	5.0	5.5	V
V_{DDA}	analog supply voltage	4.75	5.0	5.25	V
T_{amb}	operating ambient temperature	0	25	70	°C
P_{A+D}	analog and digital power	0.77	1.0	1.26	W

5 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7111	PLCC68	plastic leaded chip carrier; 68 leads	SOT188-2
SAA7111	QFP64	plastic quad flat package; 64 leads (lead length 1.6 mm); body 14 × 14 × 2.7 mm	SOT393-1

6 BLOCK DIAGRAM



The pin numbers given in parenthesis refer to the 64-pin package.

Fig.1 Block diagram.

7 PINNING

SYMBOL	PINS		I/O	DESCRIPTION
	PLCC68	QFP64		
$\overline{TRST}$	1	58	I	Test reset input not (active LOW), for boundary scan test; notes 1, 2, 3 and 4.
TCK	2	59	I	Test clock input for boundary scan test; note 3>
RTCO	3	60	O	Real time control output: contains information about actual system clock frequency, subcarrier frequency and phase and PAL sequence>
IICSA	4	61	I	I²C-bus slave address select input; 0 = > 48h for write, 49h for read, 1 = > 4Ah for write, 4Bh for read.
SDA	5	62	I/O	I²C-bus serial data input/output.
SCL	6	63	I/O	I²C-bus serial clock input/output.
n.c.	7	64	–	Not connected.
n.c.	8	–	–	Not connected.
n.c.	9	–	–	Not connected.
n.c.	10	1	–	Not connected.
TDO	11	2	O	Test data output for boundary scan test; note 3.
TDI	12	3	I	Test data input for boundary scan test; note 3.
TMS	13	4	I	Test mode select input for boundary scan test or scan test; note 3.
V_{SSA2}	14	5	GND	Ground for analog supply voltage channel 2.
AI22	15	6	I	Analog input 22.
V_{DDA2}	16	7	P	Positive supply voltage (+5 V) for analog channel 2.
AI21	17	8	I	Analog input 21.
V_{SSA1}	18	9	GND	Ground for analog supply voltage channel 1.
AI12	19	10	I	Analog input 12.
V_{DDA1}	20	11	P	Positive supply voltage (+5 V) for analog channel 1.
AI11	21	12	I	Analog input 11.
V_{SSS}	22	13	GND	Substrate (connected to analog ground).
AOUT	23	14	O	Analog test output; for testing the analog input channels.
V_{DDA0}	24	15	P	Positive supply voltage (+5 V) for internal CGC.
V_{SSA0}	25	16	GND	Ground for internal CGC.
VREF	26	17	O	Vertical reference output signal (I²C-bit COMPO = 0) or inverse composite blank signal (I²C-bit COMPO = 1) (enabled via I²C-bit OEHV).
V_{DD5}	27	18	P	Positive digital supply voltage 5 (+5 V).
V_{SS5}	28	19	GND	Digital ground for positive supply voltage 5.
LLC	29	20	O	Line-locked system clock output (27 MHz).
LLC2	30	21	O	Line-locked clock ½ output (13.5 MHz).
CREF	31	22	O	Clock reference output: this is a clock qualifier signal distributed by the CGC for a data rate of LLC2. Using CREF all interfaces on the VPO-bus are able to generate a bus timing with identical phase. If CCIR-656 format is selected (OFTS0 = 1 and OFTS1 = 1) an inverse composite blank signal (pixel qualifier) is provided on this pin.

SYMBOL	PINS		I/O	DESCRIPTION
	PLCC68	QFP64		
$\overline{RES}$	32	23	O	Reset output (active LOW); sets the device into a defined state. All data outputs are in high impedance state. The I²C-bus is reset (waiting for start condition) note 4.
CE	33	24	I	Chip enable; connection to ground forces a reset.
V_{DD4}	34	25	P	Positive digital supply voltage 4 (+5 V).
V_{SS4}	35	26	GND	Digital ground for positive supply voltage 4.
n.c.	36	–	–	Not connected.
n.c.	37	–	–	Not connected.
HS	38	27	O	Horizontal sync output signal (programmable); the positions of the positive and negative slopes are programmable in 8 LLC increments over a complete line (= 64 µs) via I²C-bus bytes HSB and HSS. Fine position adjustment in 2 LLC increments can be performed via I²C-bits HDEL1 and HDEL0.
RTS1	39	28	O	Two functions output; controlled by I²C-bit RTSE1. RTSE1 = 0: PAL line identifier (LOW = PAL line); indicates the inverted and non-inverted R – Y component for PAL signals. RTSE1 = 1: H-PLL locked indicator; a high state indicates that the internal horizontal PLL has locked.
RTS0	40	29	O	Two functions output; controlled by I²C-bit RTSE0. RTSE0 = 0: odd/even field identification (HIGH = odd field). RTSE0 = 1: vertical locked indicator; a HIGH state indicates that the internal VNL has locked.
VS	41	30	O	Vertical sync output signal (enabled via I²C-bit OEHV); this signal indicates the vertical sync with respect to the YUV output. The HIGH period of this signal is approximately six lines if the vertical noise limiter (VNL) function is active. The positive slope contains the phase information for a deflection controller.
HREF	42	31	O	Horizontal reference output signal (enabled via I²C-bit OEHV); this signal is used to indicate data on the digital YUV bus. The positive slope marks the beginning of a new active line. The HIGH period of HREF is 720 Y samples long. HREF can be used to synchronize data multiplexer/demultiplexers. HREF is also present during the vertical blanking interval.
V_{SS3}	43	32	GND	Digital ground for positive supply voltage 3.
V_{DD3}	44	33	P	Positive digital supply voltage 3 (+5 V).
VPO (15 to 10)	45 to 50	34 to 39	O	Digital VPO-bus (Video Port Out) output signal; higher bits of the 16-bit YUV-bus or the 16-bit RGB-bus output signal. The output data rate, the format and multiplexing scheme of the VPO-bus are controlled via I²C-bits OFTS0 and OFTS1. With I²C-bit VIPB = 1 the six MSBs of the digitized input signal (AD1 [7 to 2]) are connected to these outputs.
V_{SS2}	51	40	GND	Digital ground for positive supply voltage 2.
V_{DD2}	52	41	P	Positive digital supply voltage 2 (+5 V).

SYMBOL	PINS		I/O	DESCRIPTION
	PLCC68	QFP64		
VPO (9 to 0)	53 to 62	42 to 51	O	Digital VPO-bus output signal; lower bits of the 16-bit YUV-bus or the 16-bit RGB-bus output signal. The output data rate, the format and multiplexing schema of the VPO-bus are controlled via I²C-bits OFTS0 and OFTS1. With I²C-bit VIPB = 1 the digitized input signals (AD1 [1 and 0] and AD2 [7 to 0]) are connected to these outputs.
$\overline{FEI}$	63	52	I	Fast enable input signal (active LOW); this signal is used to control fast switching on the digital YUV-bus. A HIGH at this input forces the IC to set its Y and UV outputs to the high impedance state; note 4.
GPSW	64	53	O	General purpose switch output; the state of this signal is set via I²C-bus control and the levels are TTL compatible.
XTAL	65	54	O	Second output terminal of crystal oscillator; not connected if external clock signal is used.
XTALI	66	55	I	Input terminal for 24.576 MHz crystal oscillator or connection of external oscillator with CMOS compatible square wave clock signal.
V_{SS1}	67	56	GND	Digital ground for positive supply voltage 1.
V_{DD1}	68	57	P	Positive digital supply voltage 1 (+5 V).

Notes

1. For board design without boundary scan implementation (pin compatibility with the SAA7110) connect the $\overline{TRST}$ pin to ground.
2. This pin provides easy initialization of BST circuit. $\overline{TRST}$ can be used to force the TAP (Test Access Port) controller to the Test-Logic-Reset state (normal operation) at once.
3. In accordance with the *"IEEE1149.1"* standard the pads TCK, TDI, TMS and $\overline{TRST}$ are input pads with an internal pull-up transistor and TDO a 3-state output pad.
4. All pin names that carry an 'overscore' have been renamed due to Philips pin name conventions. In previous data sheet versions these pins were marked by the suffix 'N', e.g. $\overline{TRST}$ = TRSTN.

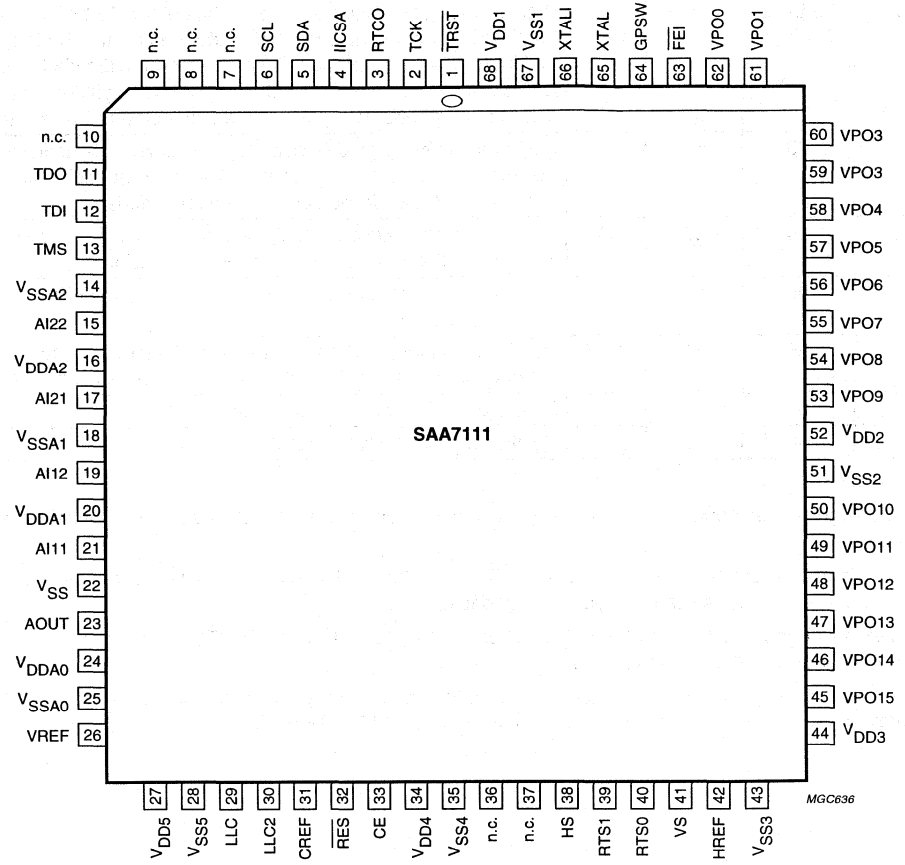


Fig.2 Pin configuration (PLCC68).

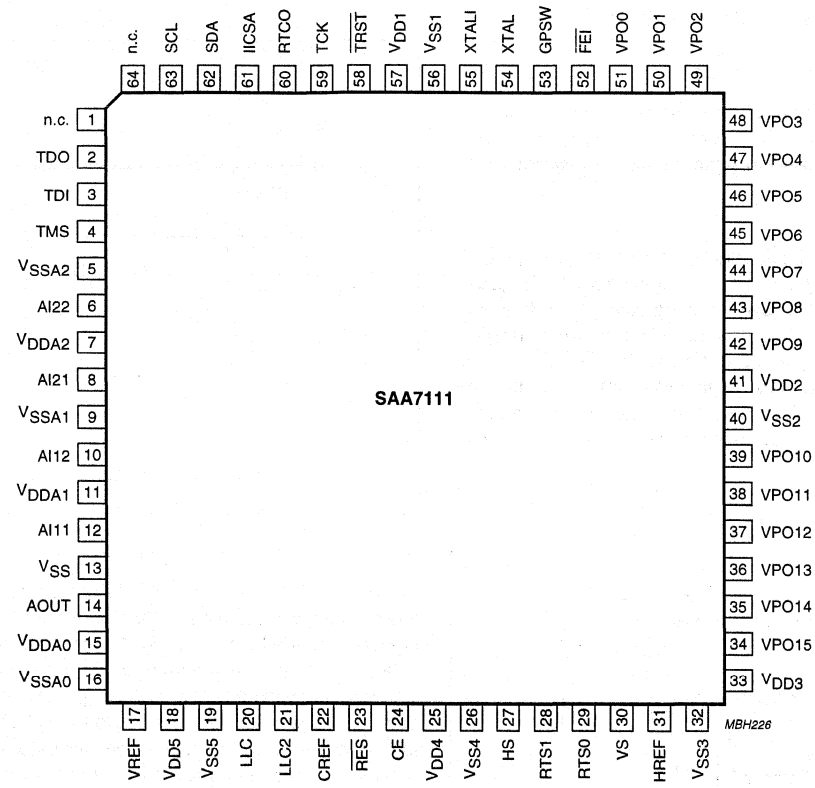


Fig.3 Pin configuration (QFP64).

8 FUNCTIONAL DESCRIPTION

8.1 Analog input processing

The SAA7111 offers four analog signal inputs, two analog main channels with clamp circuit, analog amplifier, anti-alias filter and video CMOS ADC (see Fig.6).

8.2 Analog control circuits

The anti-alias filters are adapted to the line-locked clock frequency with help from a filter control. During the vertical blanking, time gain and clamping control are frozen.

8.2.1 CLAMPING

The clamp control circuit controls the correct clamping of the analog input signals. The coupling capacitor is also used to store and filter the clamping voltage. An internal digital clamp comparator generates the information with respect to clamp-up or clamp-down. The clamping levels for the two ADC channels are fixed for luminance (60) and chrominance (128). Clamping time in normal use is set with the HCL pulse at the back porch of the video signal.

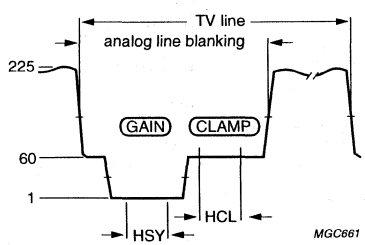


Fig.4 Analog line with clamp (HCL) and gain range (HSY).

8.2.2 GAIN CONTROL

Signal (white) peak control limits the gain at signal overshoots. The flow charts (see Figs 10 and 11) show more details of the AGC. The influence of supply voltage variation within the specified range is automatically eliminated by clamp and automatic gain control.

The gain control circuit receives (via the I²C-bus) the static gain levels for the two analog amplifiers or controls one of these amplifiers automatically via a built-in automatic gain control (AGC) as part of the Analog Input Control (AICO). The AGC (automatic gain control for luminance) is used to amplify a CVBS or Y signal to the required signal amplitude, matched to the ADCs input voltage range. The AGC active time is the sync bottom of the video signal.

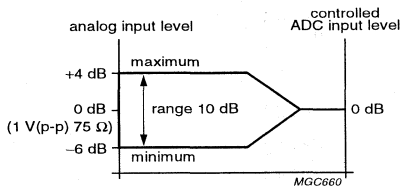


Fig.5 Automatic gain range.

8.3 Chrominance processing

The 8-bit chrominance signal is fed to the multiplication inputs of a quadrature demodulator, where two subcarrier signals from the local oscillator DTO1 are applied (0 and 90° phase relationship to the demodulator axis). The frequency is dependent on the present colour standard. The output signals of the multipliers are low-pass filtered (four programmable characteristics) to achieve the desired bandwidth for the colour difference signals.

The colour difference signals are fed to the Brightness/Contrast/Saturation block (BCS), which includes the following five functions;

1. AGC (automatic gain control for chrominance).
2. Chroma amplitude matching [different gain factors for (R–Y) and (B–Y) to achieve CCIR-601 levels Cr and Cb].
3. Chroma saturation control.
4. Luminance contrast and brightness.
5. Limiting YUV to the values 1 (min.) and 254 (max.) to fulfil CCIR-601 requirements.

The burst processing block provides the feedback loop of the chroma PLL and contains;

- Burst gate accumulator
- Colour identification and killer
- Comparison nominal/actual burst amplitude
- Loop filter chroma gain control
- Loop filter chroma PLL
- PAL sequence generation
- Increment generation for DTO1 with divider to generate stable subcarrier for non-standard signals.

The chroma comb filter block eliminates crosstalk between the chrominance channels in accordance with the PAL standard requirements. For NTSC colour standards the chroma comb filter can be used to eliminate crosstalk from luminance to chrominance (cross-colour) for vertical structures. The comb filter can be switched off if desired.

The resulting signals are fed to the variable Y-delay compensation, RGB matrix, dithering circuit and output interface, which contains the VPO output formatter and the output control logic (see Fig.7).

8.4 Luminance processing

The 8-bit luminance signal, a digital CVBS format or a luminance format (S-VHS, HI8), is fed through a switchable prefilter. High frequency components are emphasized to compensate for loss. The following chrominance trap filter (f_0 = 4.43 or 3.58 MHz centre frequency selectable) eliminates most of the colour carrier signal, therefore, it must be bypassed for S-video (S-VHS, HI8) signals.

The high frequency components of the luminance signal can be peaked (control for sharpness improvement via I²C-bus) in two band-pass filters with selectable transfer characteristic. This signal is then added to the original (unpeaked) signal. A switchable amplifier achieves common DC amplification, because the DC gains are different in both chrominance trap modes. The improved luminance signal is fed to the BCS control located in the chrominance processing block (see Fig.8).

8.5 RGB matrix

Y data and Cr, Cb data are converted after interpolation into RGB data in accordance with CCIR-601 recommendation. The realized matrix equations consider the digital quantization:

$R = Y + 1.371\ Cr$

$G = Y - 0.336\ Cb - 0.698\ Cr$

$B = Y + 1.732\ Cb$

After dithering (noise shaping) the RGB data is fed to the output interface within the VPO-bus output formatter.

8.6 VPO-bus (digital outputs)

The 16-bit VPO-bus transfers digital data from the output interfaces to a feature box or a field memory, a digital colour space converter (SAA7192 DCSC), a video enhancement and digital-to-analog processor (SAA7165 VEDA2) or a colour graphics board (Targa-format) as a graphical user interface.

The output data formats are controlled via the I²C-bus bits OFTS0, OFTS1 and RGB888. Timing for the data stream formats, 411 YUV (12-bit), 422 YUV (16-bit), 565 RGB (16-bit) and 888 RGB (24-bit) with an LLC2 data rate, is achieved by marking each second positive rising edge of the clock LLC in conjunction with CREF (clock reference) (except RGB 888, see special application in Fig.27). The higher output signals VPO15 to VPO8 in the YUV format perform the digital luminance signal. The lower output signals VPO7 to VPO0 in the YUV format are the bits of the multiplexed colour difference signals (B–Y) and (R–Y). The arrangement of the RGB 565 and RGB 888 data stream bits on the VPO-bus is given in Table 5.

The data stream format 422 YUV (the 8 higher output signals VPO15 to VPO8) in LLC data rate fulfils the CCIR-656 standard with its own timing reference code at the start and end of each video data block.

A pixel in the format tables is the time required to transfer a full set of samples. In the event of a 4 : 2 : 2 format two luminance samples are transmitted in comparison to one (B–Y) and one (R–Y) sample within a pixel. The time frames are controlled by the HREF signal.

Fast enable is achieved by setting input $\overline{FEI}$ to LOW. The signal is used to control fast switching on the digital VPO-bus. HIGH on this pin forces the YUV outputs to a high-impedance state (see Figs 15 and 17).

The digitized analog PAL or NTSC signals AD1 (7 to 0) and AD2 (7 to 0) are connected directly to the VPO-bus via I²C-bit VIPB = 1.

AD1 (7 to 0) -> VPO (15 to 8) and
AD2 (7 to 0) ->VPO (7 to 0)

The selection of the analog input channels are controlled via I²C-bus subaddress 02 MODE select.

8.7 Synchronization

The prefiltered luminance signal is fed to the synchronization stage. Its bandwidth is reduced to 1 MHz in a low-pass filter. The sync pulses are sliced and fed to the phase detectors where they are compared with the sub-divided clock frequency. The resulting output signal is applied to the loop filter to accumulate all phase deviations. Internal signals (e. g. HCL and HSY) are generated in accordance with analog front-end requirements. The output signals HS, VS, and PLIN are locked to the timing reference, guaranteed between the input signal and the HREF signal, as further improvements to the circuit may change the total processing delay. It is therefore not recommended to use them for applications which require absolute timing accuracy on the input signals. The loop filter signal drives an oscillator to generate the line frequency control signal LFCO (see Fig.8).

8.8 Clock generation circuit

The internal CGC generates all clock signals required for the video input processor. The internal signal LFCO is a digital-to-analog converted signal provided by the horizontal PLL. It is the multiple of the line frequency (6.75 MHz = 432 × f_h). Internally the LFCO signal is multiplied by a factor of 2 or 4 in the PLL circuit (including phase detector, loop filtering, VCO and frequency divider) to obtain the LLC and LLC2 output clock signals. The rectangular output clocks have a 50% duty factor (see Fig.22).

8.9 Power-on reset and CE input

A missing clock, insufficient digital or analog V_{DDA0} supply voltages (below 3.5 V) will initiate the reset sequence; all outputs are forced to 3-state. The indicator output $\overline{RES}$ is LOW for approximately 128 LLC after the internal reset and can be applied to reset other circuits of the digital TV system.

It is possible to force a reset by pulling the CE (chip enable) to ground. After the rising edge of CE and sufficient power supply voltage, the outputs LLC, LLC2, CREF, RTCO, RTS0, RTS1, GPSW and SDA return from 3-state to active, while HREF, VREF, HS and VS remain in 3-state and have to be activated via I²C-bus programming (see Table 4).

8.10 RTCO output

The real time control and status output signal contains serial information about the actual system clock (increment of the HPLL), subcarrier frequency [increment and phase (via reset) of the FSC-PLL] and PAL sequence bit. The signal can be used for various applications in external circuits, e.g. in a digital encoder to achieve clean encoding (see Fig.16).

8.11 The Line-21 text slicer

The text slicer block detects and acquires Line-21 Closed Captioning data from a 525-line CVBS signal. Extended data services on Line-21 Field 2 are also supported. If valid data is detected the two data bytes are stored in two I²C-bus registers. A parity check is also performed and the result is stored in the MSB of the corresponding byte. A third I²C-bus register is provided for data valid and data ready flags. The two bits F1VAL and F2VAL indicate that the input signal carries valid Closed Captioning data on the corresponding fields. The data ready bits F1RDY and F2RDY have to be evaluated if asynchronous I²C-bus reading is used.

8.11.1 Suggestions for I²C-bus interface of the display software reading Line-21 data

There are two methods by which the software can acquire the data;

1. Synchronous reading once per frame (or once per field): It can use either the rising edge (Line-21 Field 1) or both edges (Line-21 Field 1 or 2) of the ODD signal (pin RTSO) to initiate an I²C-bus read transfer of the three registers 1A, 1B and 1C.
2. Asynchronous reading: It can poll either the F1RDY bit (Line-21 Field 1) or both F1RDY/F2RDY bits (Line-21 Field 1 or 2). After valid data has been read the corresponding F*RDY bit is set to LOW until new data has arrived. The polling frequency has to be slightly higher than the frame or field frequency, respectively.

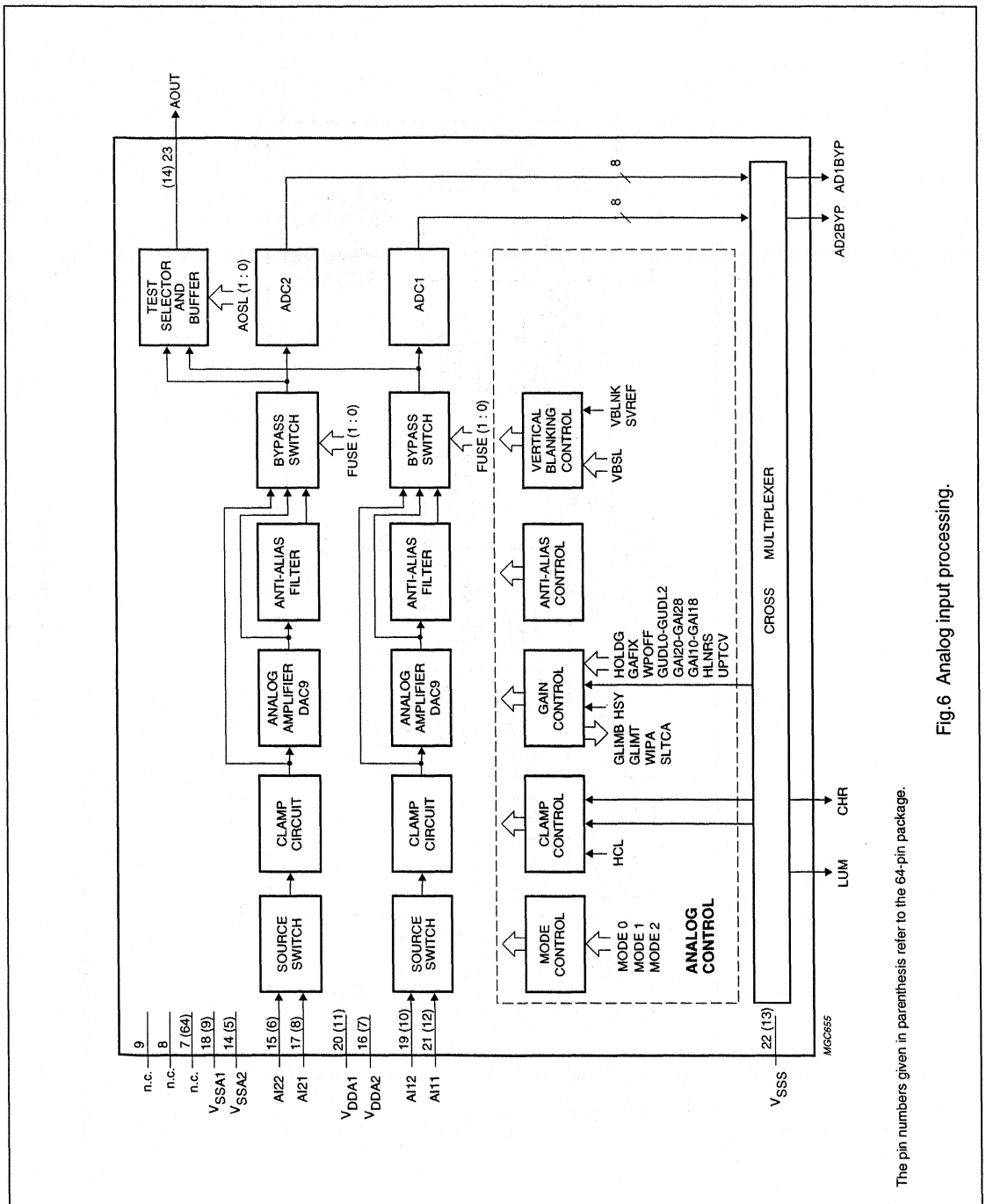


Fig.6 Analog input processing.

The pin numbers given in parenthesis refer to the 64-pin package.

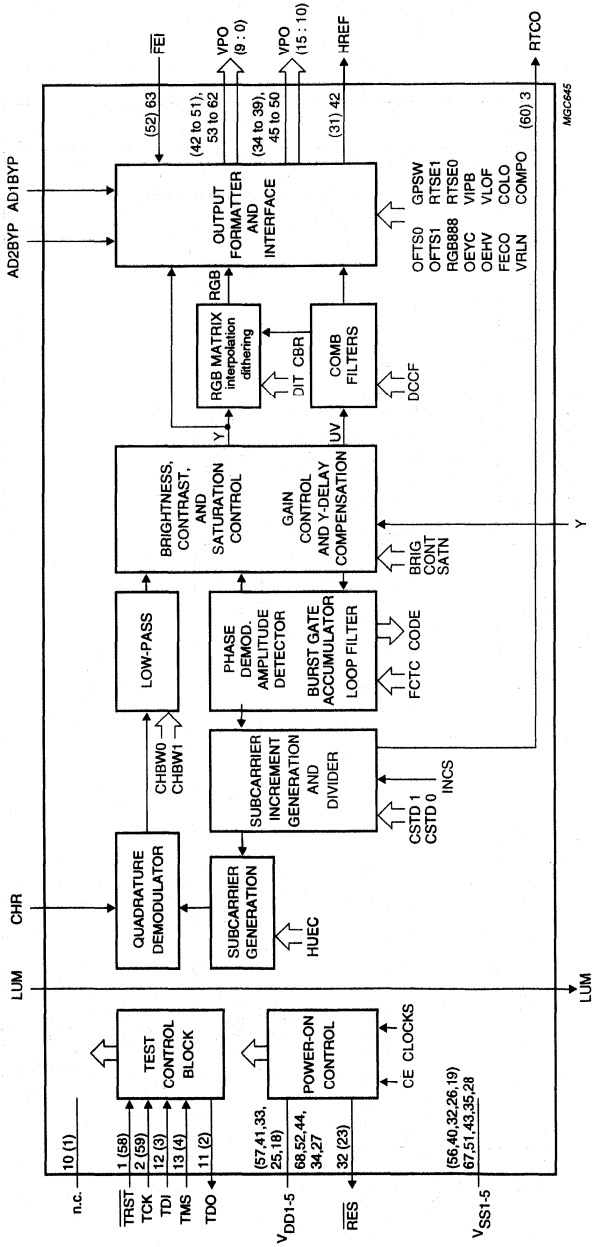
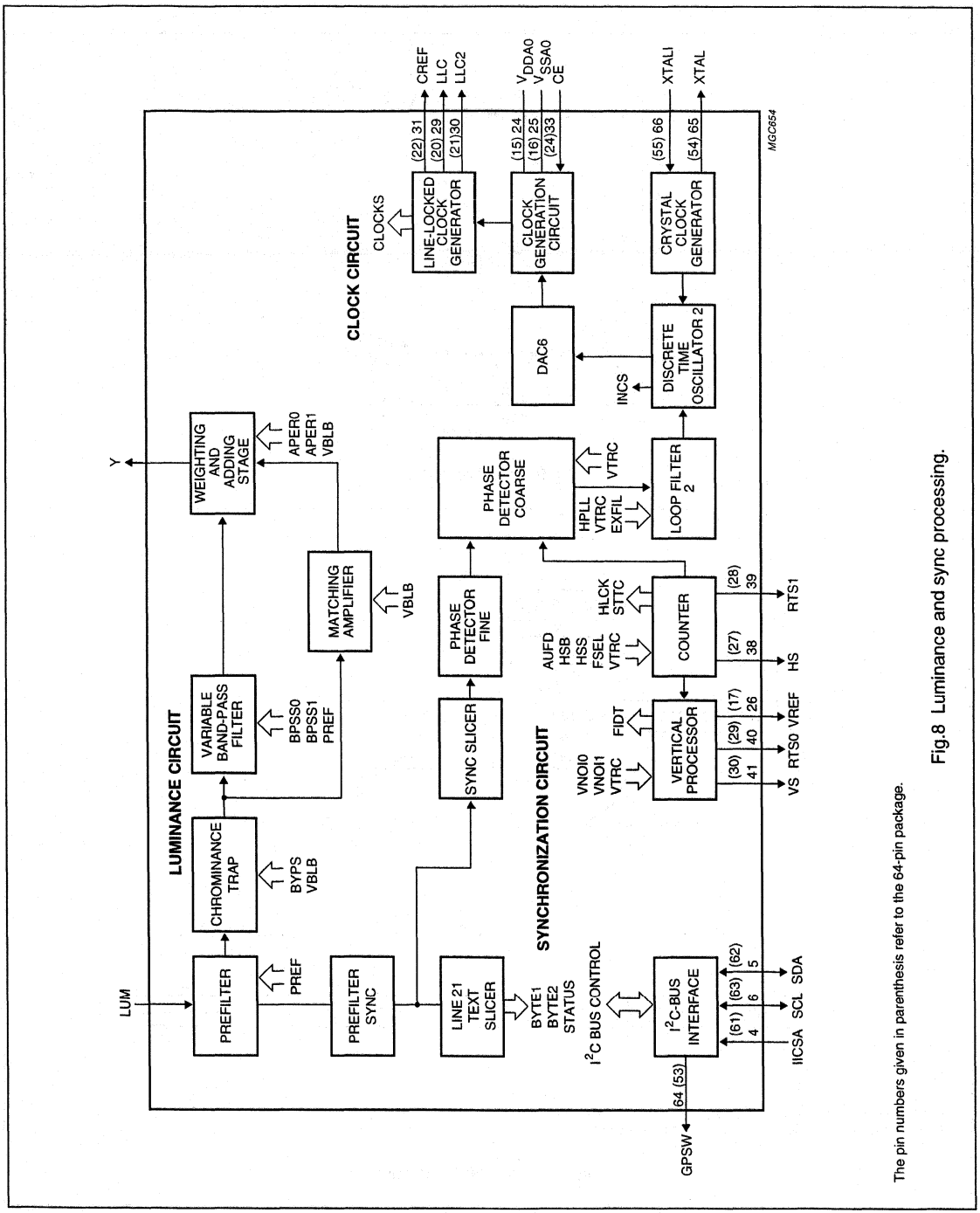


Fig.7 Chrominance circuit.

The pin numbers given in parenthesis refer to the 64-pin package.



The pin numbers given in parenthesis refer to the 64-pin package.

Fig.8 Luminance and sync processing.

9 GAIN CHARTS

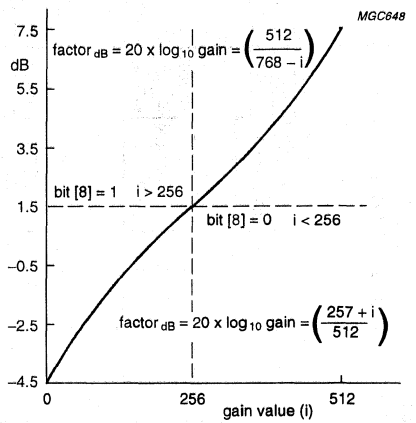
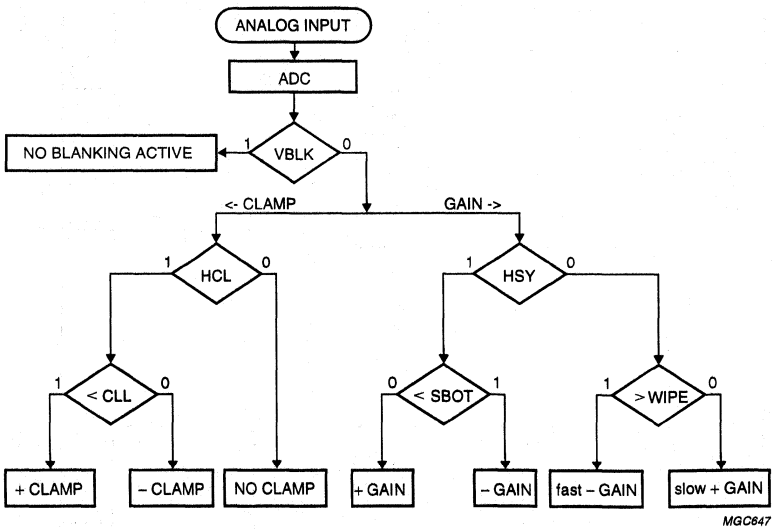
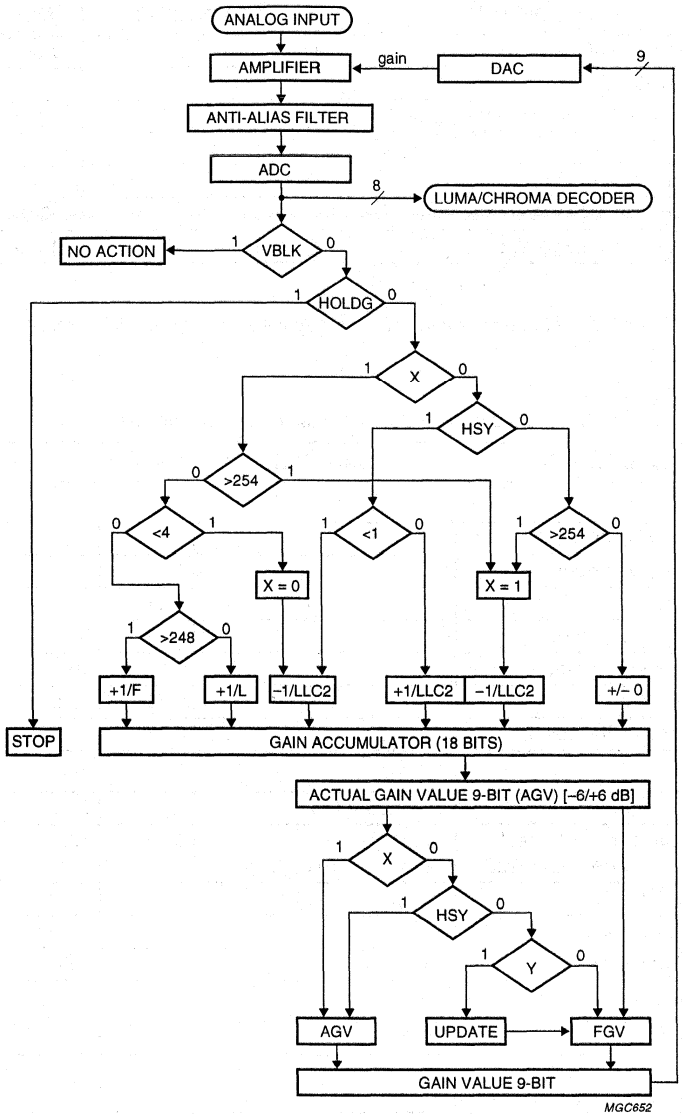


Fig.9 Amplifier curve.



WIPE = white peak level (254); SBOT = sync bottom level (1); CLL = clamp level [60 Y (128 C)];
HSY = horizontal sync pulse; HCL = horizontal clamp pulse.

Fig.10 Clamp and gain flow.



X = system variable; Y = AGV − FGVI > GUDL; VBLK = vertical blanking pulse;
HSY = horizontal sync pulse; AGV = actual gain value; FGV = frozen gain value.

Fig.11 Gain flow chart.

10 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDD}	digital supply voltage		−0.5	+6.5	V
V_{DDA}	analog supply voltage		−0.5	+6.5	V
V_{diff}	voltage difference between V_{SSAall} and V_{SSall}		−	100	mV
T_{stg}	storage temperature		−65	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C
$T_{amb(bias)}$	operating ambient temperature under bias		−10	+80	°C
V_{esd}	electrostatic discharge all pins	note 1	−2000	+2000	V

Note

1. Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor.

11 CHARACTERISTICS

V_{DDD} = 4.5 to 5.5 V; V_{DDA} = 4.75 to 5.25 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
I_{DDD}	digital supply current		100	130	160	mA
P_D	digital power		0.45	0.65	0.88	W
V_{DDA}	analog supply voltage		4.75	5.0	5.25	V
I_{DDA}	analog supply current		60	70	80	mA
P_A	analog power		0.32	0.35	0.38	W
P_{A+D}	analog and digital power		0.77	1.0	1.26	W
Analog part						
I_{clamp}	clamping current	V_I = 1.25 V DC	−	2	−	μA
$V_{i(p-p)}$	input voltage (peak-to-peak value), AC coupling required	coupling capacitor = 10 nF; note 1	0.55	1.0	1.5	V
$\|Z_i\|$	input impedance	clamping current off	200	−	−	kΩ
C_i	input capacitance		−	−	10	pF
α_{cs}	channel crosstalk	f_i = 5 MHz	−	−50	−	dB
Analog-to-digital converters						
B	bandwidth	at −3 dB	−	15	−	MHz
ϕ_{diff}	differential phase (amplifier plus anti-alias filter = bypass)		−	2	−	deg
G_{diff}	differential gain (amplifier plus anti-alias filter = bypass)		−	2	−	%
f_{ADC}	ADC clock frequency		11	−	16	MHz
DLE	DC differential linearity error		−	0.5	−	LSB
ILE	DC integral linearity error		−	1	−	LSB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital inputs						
V_{IL}	LOW level input voltage pins SDA and SCL		−0.5	−	+1.5	V
V_{IH}	HIGH level input voltage pins SDA and SCL		$0.7V_{DDD}$	−	V_{DDD} + 0.5	V
$V_{IL(xtall)}$	LOW level CMOS input voltage pin XTALI		−	−	$0.3V_{DDD}$	V
$V_{IH(xtall)}$	HIGH level CMOS input voltage pin XTALI		$0.7V_{DDD}$	−	−	V
V_{ILn}	LOW level input voltage all other inputs		−0.5	−	+0.8	V
V_{IHn}	HIGH level input voltage all other inputs		2.0	−	V_{DDD} + 0.5	V
I_{LI}	input leakage current		−	−	1	μA
$C_{i(I/O)}$	input capacitance	inputs and outputs at high-impedance	−	−	8	pF
$C_{i(n)}$	input capacitance all other inputs		−	−	8	pF
Digital outputs						
V_{OL}	LOW level output voltage pins SDA and SCL	SDA/SCL at 3 mA sink current	−	−	0.4	V
V_{OL}	LOW level output voltage	note 2	0	−	0.6	V
V_{OH}	HIGH level output voltage	note 2	2.4	−	V_{DDD}	V
$V_{OL(clk)}$	LOW level output voltage for clocks		−0.5	−	+0.6	V
$V_{OH(clk)}$	HIGH level output voltage for clocks		2.6	−	V_{DDD} + 0.5	V
$\overline{FEI}$ input timing						
$t_{SU;DAT}$	input data set-up time		13	−	−	ns
$t_{HD;DAT}$	input data hold time		3	−	−	ns
Data and control output timing						
C_L	output load capacitance		15	−	50	pF
$t_{OHD;DAT}$	output hold time	C_L = 15 pF	5	−	−	ns
t_{PD}	propagation delay	C_L = 40 pF	−	−	21	ns
t_{PDZ}	propagation delay to 3-state		−	−	21	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Clock output timing (LLC and LLC2)						
$C_{L(LLC)}$	output load capacitance		15	–	40	pF
T_{cy}	cycle time	LLC	35	–	39	ns
		LLC2	70	–	78	ns
δLLC	duty factors for t_{LLCH}/t_{LLC} and t_{LLC2H}/t_{LLC2}	C_L = 40 pF	40	–	60	%
t_r	rise time	V_i = 0.6 to 2.6 V	–	–	5	ns
t_f	fall time	V_i = 2.6 to 0.6 V	–	–	5	ns
t_{dLLC2}	delay time LLC output to LLC2 output	V_i = 1.5 V; LLC/LLC2 = 40 pF	−1	–	+1	ns
Data qualifier output timing (CREF)						
$t_{OHD;CREF}$	output hold time	C_L = 15 pF	4	–	–	ns
$t_{PD;CREF}$	propagation delay from positive edge of LLC	C_L = 40 pF	–	–	20	ns
Clock input timing (XTALI)						
δXTALI	duty factor for t_{XTALIH}/t_{XTALI}	nominal frequency	40	–	60	%
Horizontal PLL						
f_{Hn}	nominal line frequency	50 Hz field	–	15625	–	Hz
		60 Hz field	–	15734	–	Hz
$\Delta f_H/f_{Hn}$	permissible static deviation		–	–	5.7	%
Subcarrier PLL						
f_{SCn}	nominal subcarrier frequency	PAL BGHI, NTSC 443	–	4433619	–	Hz
		NTSC M	–	3579545	–	Hz
		PAL M	–	3575612	–	Hz
		PAL N	–	3582056	–	Hz
$\Delta f_{SCH}/f_{SCHn}$	lock-in range		±400	–	–	Hz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Crystal oscillator						
f_n	nominal frequency	3rd harmonic	–	24.576	–	MHz
$\Delta f/f_n$	permissible nominal frequency deviation		–	–	±50	10^{-6}
$\Delta Tf/f_n$	permissible nominal frequency deviation with temperature		–	–	±20	10^{-6}
CRYSTAL SPECIFICATION (X1)						
T_{ambX1}	operating ambient temperature		0	–	70	°C
C_L	load capacitance		8	–	–	pF
R_S	series resonance resistor		–	40	80	Ω
C_1	motional capacitance		–	1.5 ±20%	–	fF
C_0	parallel capacitance			3.5 ±20%		pF

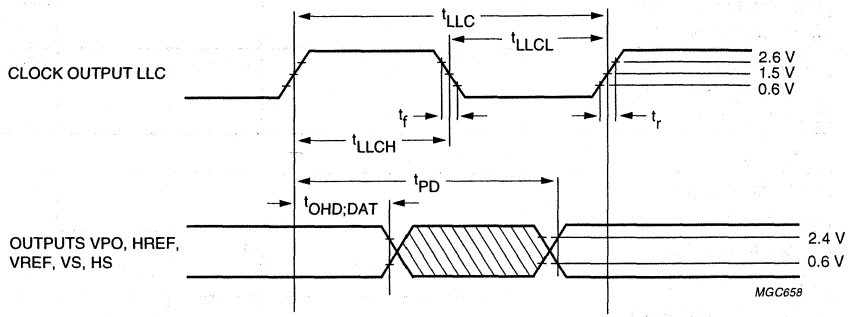
Notes

1. The levels must be measured with load circuits; 1.2 kΩ at 3 V (TTL load); C_L = 50 pF.
2. The effects of rise and fall times are included in the calculation of $t_{OHD;DAT}$, t_{PD} and t_{PDZ}. Timings and levels refer to drawings and conditions illustrated in Figs 12 and 13.

Table 1 Processing delay

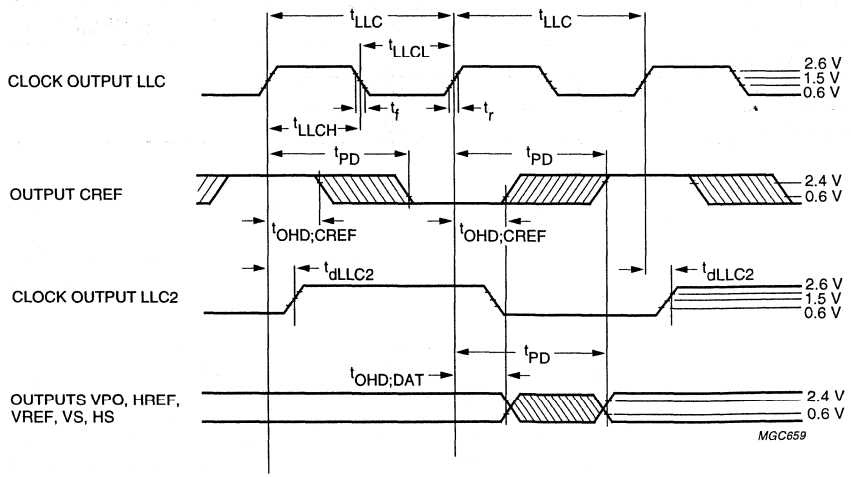
FUNCTION	TYPICAL ANALOG DELAY AI22 –> ADCIN (AOUT) (ns)	DIGITAL DELAY ADCIN -> VPO (LLC-CLOCKS) [YDEL(2 to 0) = 000]
Without amplifier or anti-alias filter	14	139
With amplifier, without anti-alias filter	30	
With amplifier plus anti-alias filter	72	

12 TIMING DIAGRAMS



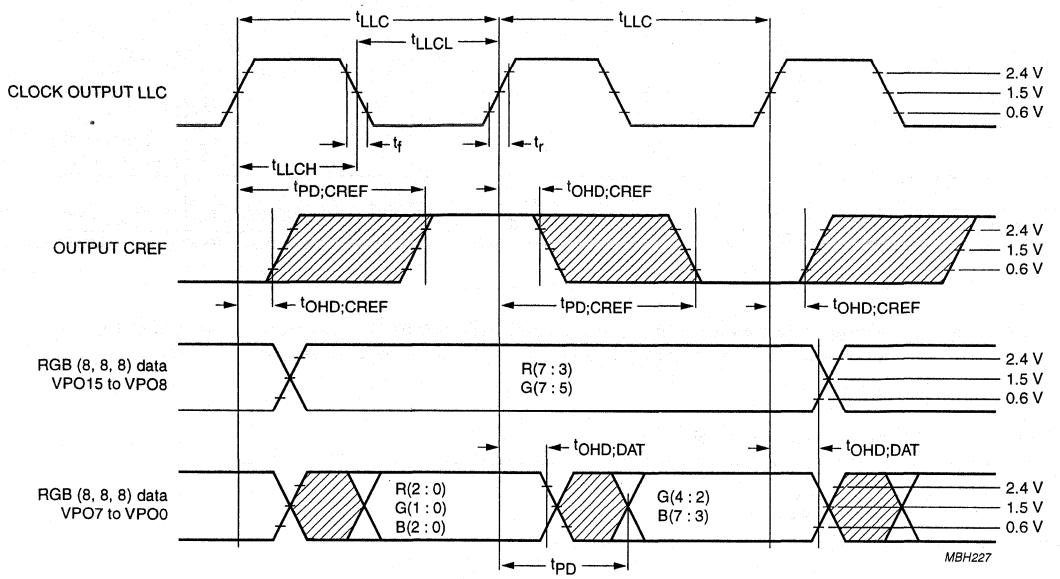
An explanation of the output formats is given in Table 5.

Fig.12 Clock/data timing (8-bit CCIR-656 format of the VPO-bus).



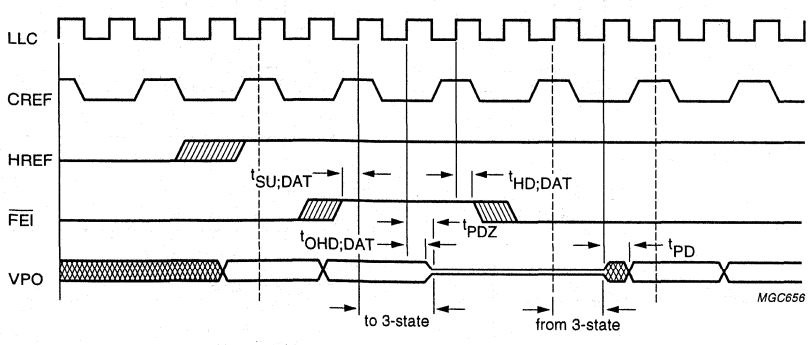
An explanation of the output formats is given in Table 5. The $\overline{FEI}$ timing of the VPO-bus is illustrated in Figs 15 and 17.

Fig.13 Clock/data timing (12/16-bit CCIR-601 format of the VPO-bus).



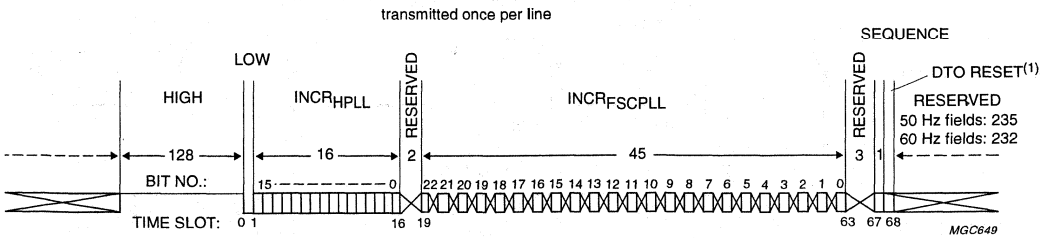
An explanation of the output formats is given in Table 5.

Fig.14 Clock/data timing for RGB888 output format.



I²C-bit FECO = 1.

Fig.15 $\overline{FEI}$ timing diagram ($\overline{FEI}$ sampling at CREF = HIGH).



(1) Set to zero for one transmission, if a phase reset of the f_{sc} - DTO is applied via I²C-bit CDTO. RTCO sequence is generated in LLC/4.

The HPLL increment represents the actual LFCO frequency ($f_{LFCO} \times 4 = f_{LLC}$); 16 LSB from 20, upper four bits are fixed to 0100b

$$f_{LFCO} = \frac{INCR_{HPLL} \times f_{XTAL}}{2^{\text{word length DTO2}}}$$

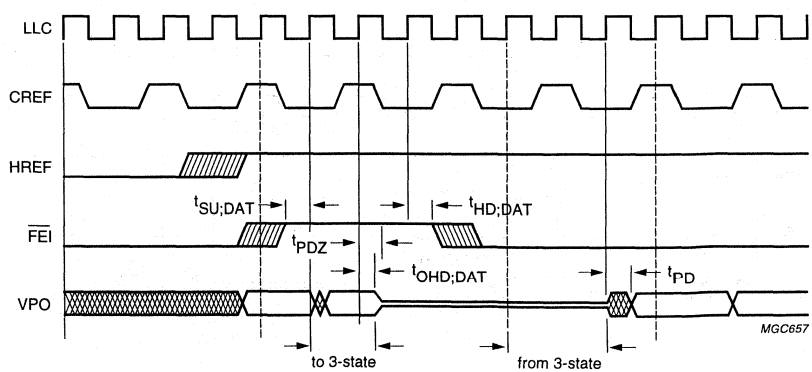
Where: f_{XTAL} = 24.576 MHz, word length DTO2 = 20 bits.

The f_{sc} increment represents the actual subcarrier frequency (related to the actual clock); 23 LSB from 24, MSB is 0b.

$$f_{sc} = \frac{INCR_{FSCPLL} \times f_{XTAL}}{2^{\text{word length DTO1}}} \times \frac{INCR_{HPLL}}{2^{19}}$$

Where: word length DTO1 = 24 bits.

Fig.16 Real time control output.



Timing is compatible with SAA7110; I²C-bit FECO = 0.

Fig.17 $\overline{FEI}$ timing diagram ($\overline{FEI}$ sampling at CREF = LOW).

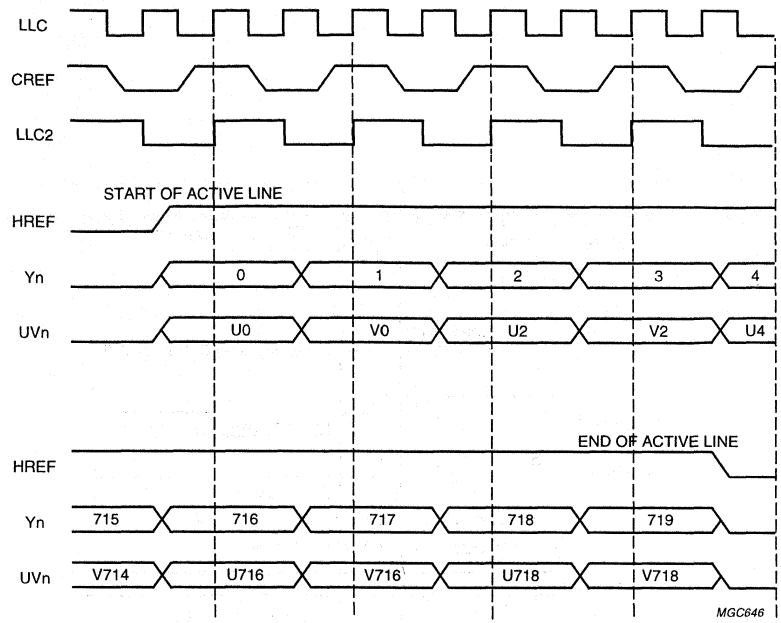
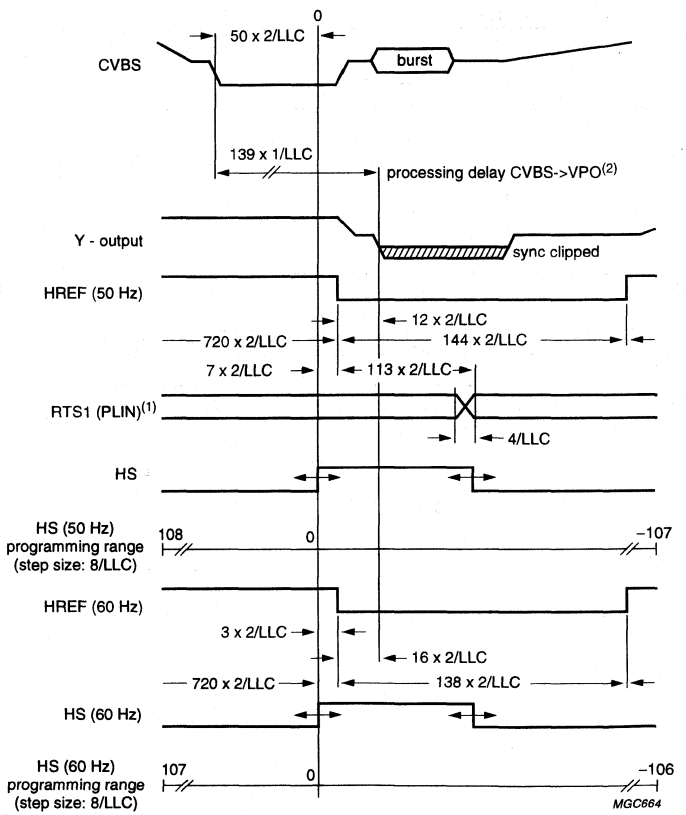
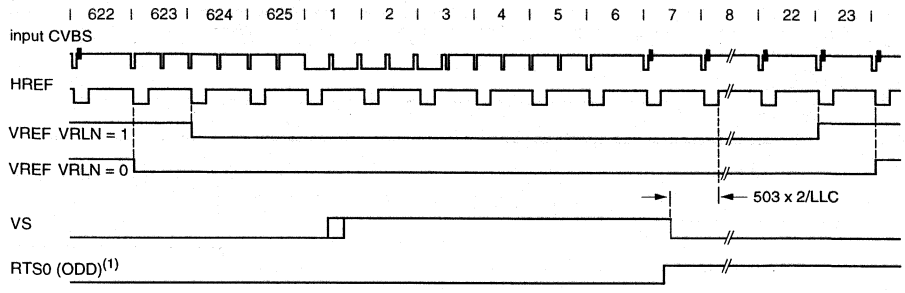


Fig.18 HREF timing diagram.

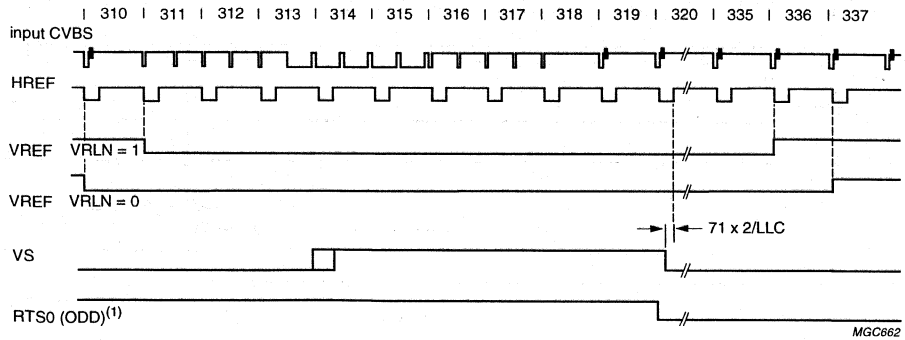


(1) PLIN is switched to output RTS1 via I²C-bit RTSE1 = 0.
(2) See Table 1.

Fig.19 Horizontal timing diagram.



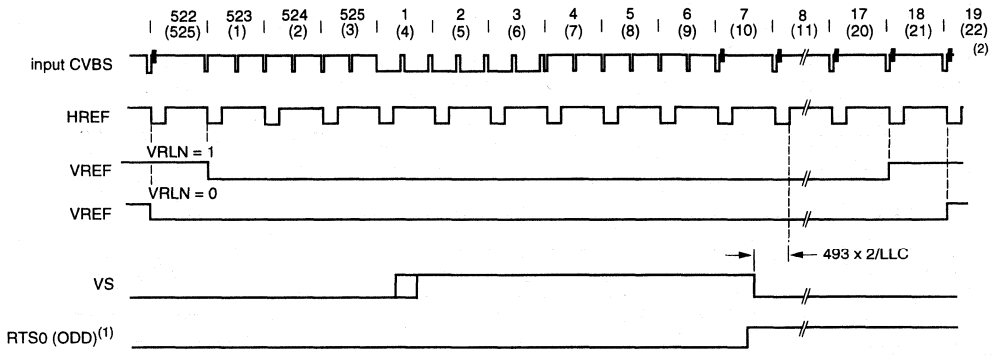
a: 1st field



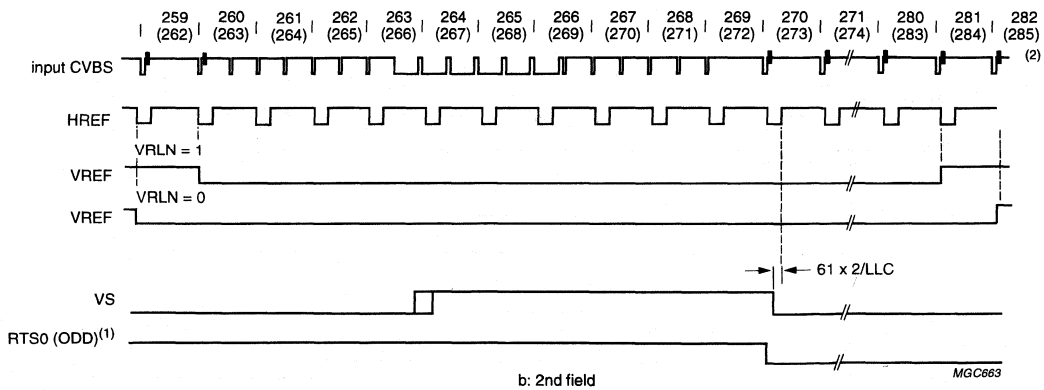
b: 2nd field

(1) ODD is switched to output RTS0 via I²C-bit RTSE0 = 0.
The luminance peaking and the chrominance trap are bypassed during VREF = 0 if I²C-bit VBLB is set to logic 1.
The chrominance delay line (chroma-comb filter for NTSC, phase error correcting for PAL) is disabled during VREF = 0.

Fig.20 Vertical timing diagram for 50 Hz [nominal input signal VNL in normal mode (VNOI = 00b)].



a: 1st field



b: 2nd field

(1) ODD is switched to output RTS0 via I²C-bit RTSE0 = 0.

(2) Line numbers in parenthesis refer to CCIR line counting.

The luminance peaking and the chrominance trap are bypassed during VREF = 0 if I²C-bit VBLB is set to logic 1.

The chrominance delay line (chroma-comb filter for NTSC, phase error correcting for PAL) is disabled during VREF = 0.

Fig.21 Vertical timing diagram for 60 Hz [nominal input signal VNL in normal mode (VNOI = 00b)].

Table 2 Digital output control

OEYC	$\overline{FEI}$	VPO		
		15 to 0[1]	15 to 8 [2]	7 to 0[2]
0	0	Z	Z	Z
1	0	active	active	Z
0	1	Z	Z	Z
1	1	Z	active	Z

Notes

1. OFTS(1 : 0) = 10 or 01 or 00.
2. OFTS(1 : 0) = 11.

13 CLOCK SYSTEM

13.1 Clock generation circuit

The internal CGC generates the system clocks LLC, LLC2 and the clock reference signal CREF. The internal generated LFCO (triangular waveform) is multiplied by 2 or 4 via the analog PLL (including phase detector, loop filter, VCO and frequency divider). The rectangular output signals have a 50% duty factor.

Table 3 Clock frequencies

CLOCK	FREQUENCY (MHz)
XTAL	24.576
LLC	27
LLC2	13.5
LLC4	6.75
LLC8	3.375

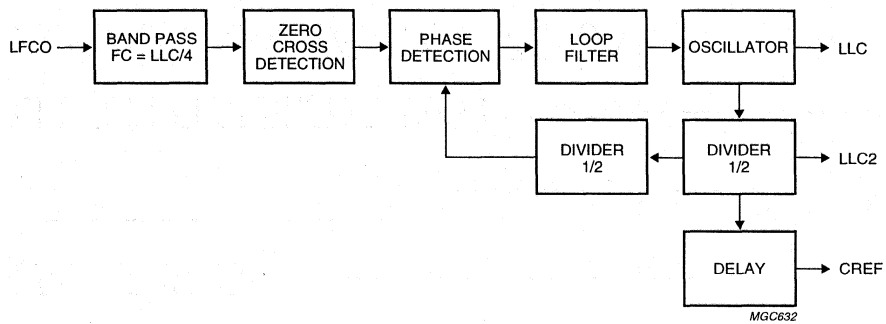
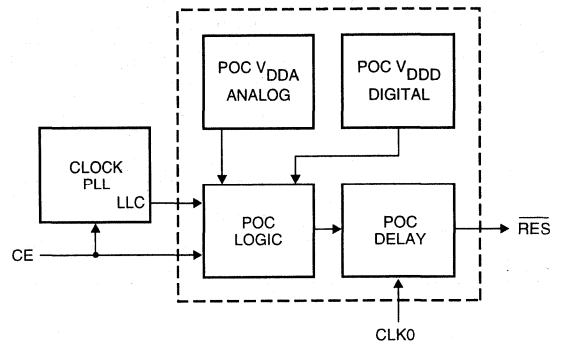
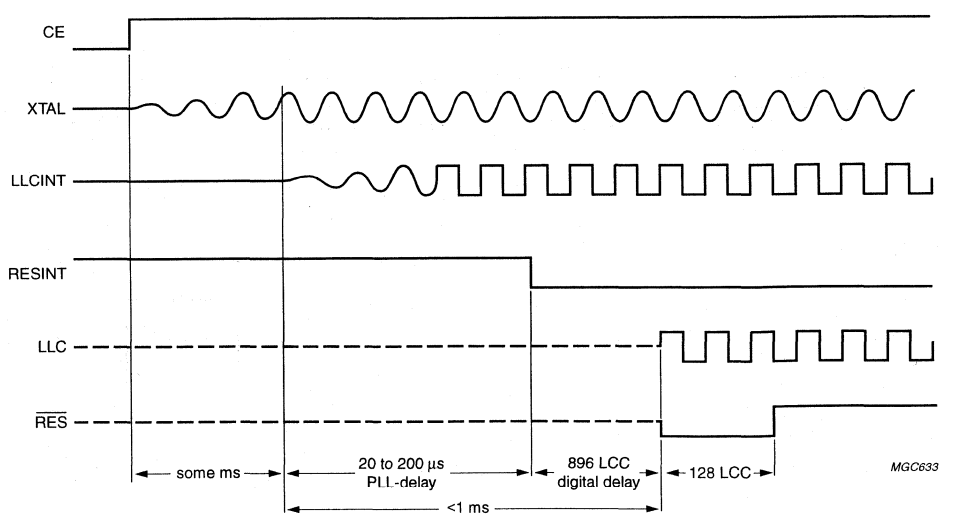


Fig.22 Block diagram of clock generation circuit.

13.2 Power-on control

Power-on reset is activated at power-on, chip enable, PLL clock generation failure and if the supply voltage falls below 3.5 V. The $\overline{RES}$ signal can be applied to reset other circuits of the digital picture processing system.





CE = chip enable input; XTAL = crystal oscillator output; LLCINT = internal system clock; RESINT = internal reset; LLC = line-locked system clock output; $\overline{RES}$ = reset output (active LOW).

Fig.23 Power-on control circuit.

Table 4 Power-on control sequence

INTERNAL POWER-ON CONTROL SEQUENCE	PIN OUTPUT STATUS	FUNCTION
Directly after power-on asynchronous reset	VPO15 to VPO0, RTCO, RTS0, RTS1, GPSW, HREF, VREF, HS, VS, LLC, LLC2 and CREF are in high-impedance state	direct switching to high impedance for 20 to 200 ms
Synchronous reset sequence	LLC, LLC2, CREF, RTCO, RTS0, RTS1, GPSW and SDA become active; VPO15 to VPO0, HREF, VREF, HS and VS are held in high-impedance state	internal reset sequence
Status after power-on control sequence	VPO15 to VPO0, HREF, VREF, HS and VS are held in high-impedance state	after power-on (reset sequence) a complete I²C-bus transmission is required

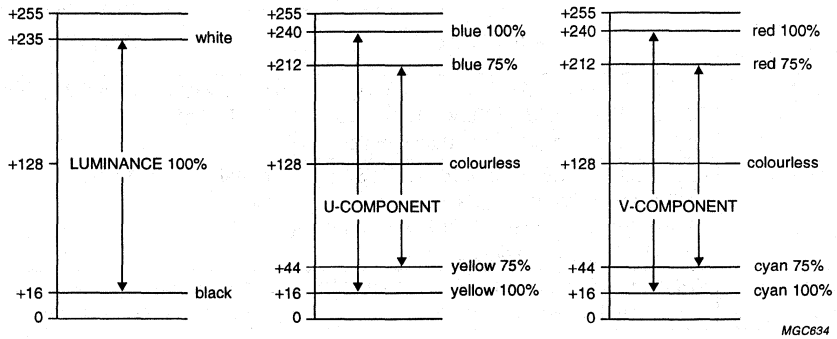
14 OUTPUT FORMATS

Table 5 Output formats

BUS SIGNAL	411 (12-BIT)				422 (16-BIT)(1)		CCIR-656 (8-BIT)(2)				RGB (16-BIT)(3)	RGB (24-BIT)(3)	
VPO15	Y_{07}	Y_{17}	Y_{27}	Y_{37}	Y_{07}	Y_{17}	U_{07}	Y_{07}	V_{07}	Y_{17}	R4	R7	R7
VPO14	Y_{06}	Y_{16}	Y_{26}	Y_{36}	Y_{06}	Y_{16}	U_{06}	Y_{06}	V_{06}	Y_{16}	R3	R6	R6
VPO13	Y_{05}	Y_{15}	Y_{25}	Y_{35}	Y_{05}	Y_{15}	U_{05}	Y_{05}	V_{05}	Y_{15}	R2	R5	R5
VPO12	Y_{04}	Y_{14}	Y_{24}	Y_{34}	Y_{04}	Y_{14}	U_{04}	Y_{04}	V_{04}	Y_{14}	R1	R4	R4
VPO11	Y_{03}	Y_{13}	Y_{23}	Y_{33}	Y_{03}	Y_{13}	U_{03}	Y_{03}	V_{03}	Y_{13}	R0	R3	R3
VPO10	Y_{02}	Y_{12}	Y_{22}	Y_{32}	Y_{02}	Y_{12}	U_{02}	Y_{02}	V_{02}	Y_{12}	G5	G7	G7
VPO9	Y_{01}	Y_{11}	Y_{21}	Y_{31}	Y_{01}	Y_{11}	U_{01}	Y_{01}	V_{01}	Y_{11}	G4	G6	G6
VPO8	Y_{00}	Y_{10}	Y_{20}	Y_{30}	Y_{00}	Y_{10}	U_{00}	Y_{00}	V_{00}	Y_{10}	G3	G5	G5
VPO7	U_{07}	U_{05}	U_{03}	U_{01}	U_{07}	V_{07}	X	X	X	X	G2	G4	R2
VPO6	U_{06}	U_{04}	U_{02}	U_{00}	U_{06}	V_{06}	X	X	X	X	G1	G3	R1
VPO5	V_{07}	V_{05}	V_{03}	V_{01}	U_{05}	V_{05}	X	X	X	X	G0	G2	R0
VPO4	V_{06}	V_{04}	V_{02}	V_{00}	U_{04}	V_{04}	X	X	X	X	B4	B7	G1
VPO3	X	X	X	X	U_{03}	V_{03}	X	X	X	X	B3	B6	G0
VPO2	X	X	X	X	U_{02}	V_{02}	X	X	X	X	B2	B5	B2
VPO1	X	X	X	X	U_{01}	V_{01}	X	X	X	X	B1	B4	B1
VPO0	X	X	X	X	U_{00}	V_{00}	X	X	X	X	B0	B3	B0
Pixel order Y	0	1	2	3	0	1	0		1		–	note 5	note 4
Pixel order UV	0				0		0				–	–	
Data rates	LLC2				LLC2		LLC				LLC2	LLC	
I²C-bus control signals	OFTS0 = 0				OFTS0 = 1		OFTS0 = 1				OFTS0 = 0	OFTS0 = 0	
	OFTS1 = 1				OFTS1 = 0		OFTS1 = 1				OFTS1 = 0	OFTS1 = 0	
	RGB888 = X				RGB888 = X		RGB888 = X				RGB888 = 0	RGB888 = 1	

Notes

1. Values in accordance with CCIR-601.
2. Before and after the video data, video timing codes are inserted in accordance with CCIR-656.
3. Values not defined during HREF = LOW.
4. CREF = 1 (see Fig.14).
5. CREF = 0 (see Fig.14).



(a) Y output range. (b) U output range (Cb). (c) V output range (Cr).

CCIR Rec. 602 digital levels.

Equations for modification to the YUV levels via BCS control I²C bytes BRIG, CONT and SATN.

Luminance:

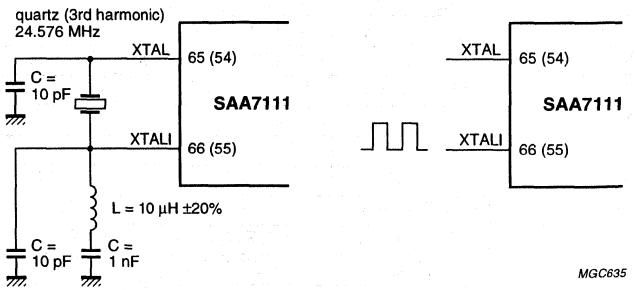
$$Y_{OUT} = Int\left[\frac{CONT}{71} \times (Y - 128)\right] + BRIG$$

Chrominance:

$$UV_{OUT} = Int\left[\frac{SATN}{64} \times (Cr, Cb - 128)\right] + 128$$

It should be noted that the resulting levels are limited to 1 to 254 in accordance with CCIR-601/656 standard.

Fig.24 VPO output signal range with default BCS settings.

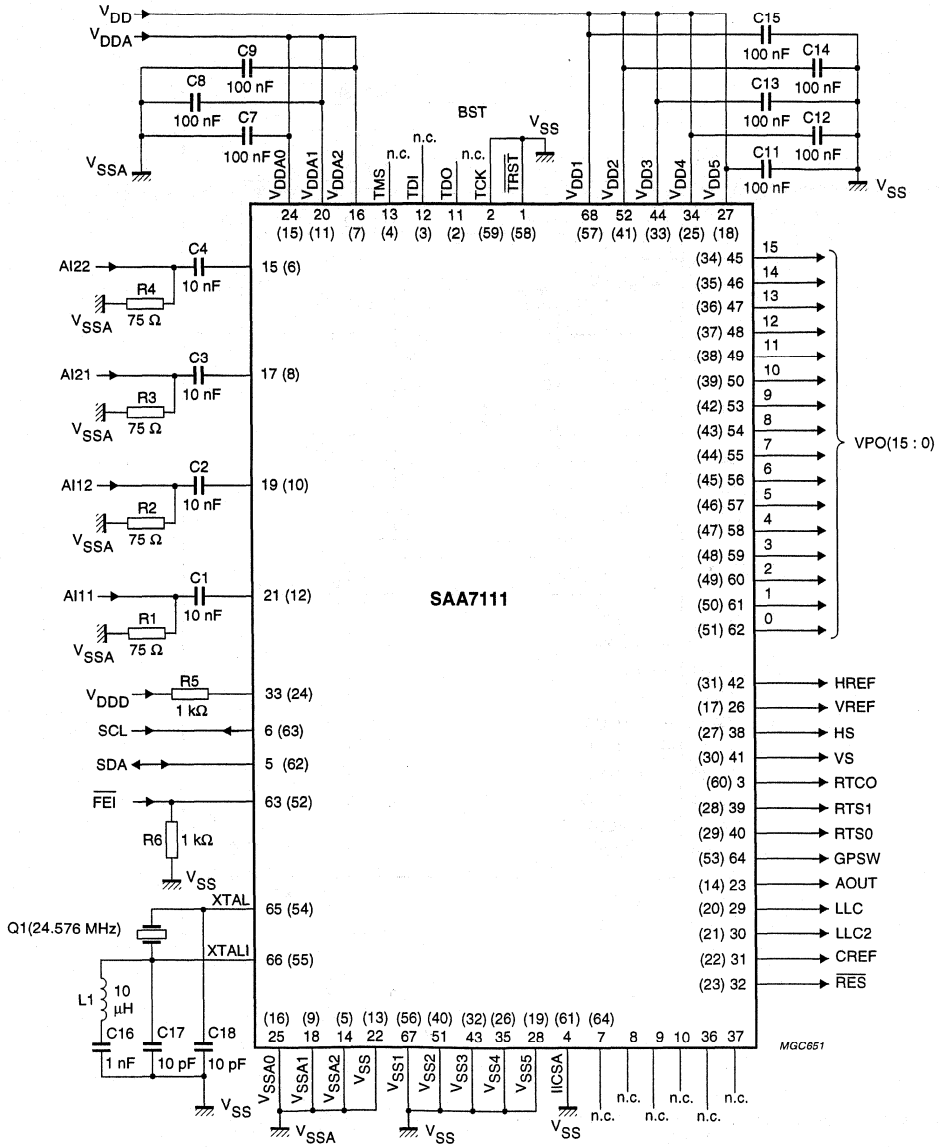


(a) With quartz crystal. (b) With external clock.

The pin numbers given in parenthesis refer to the 64-pin package.

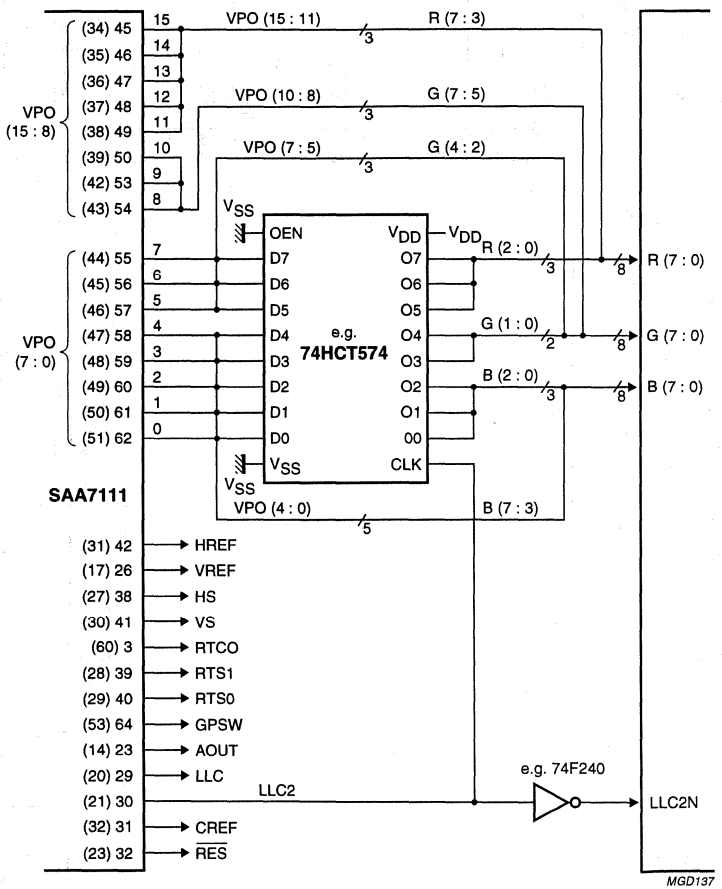
Fig.25 Oscillator application.

15 APPLICATION INFORMATION



The pin numbers given in parenthesis refer to the QFP64 package.

Fig.26 Application diagram.



The pin numbers given in parenthesis refer to the QFP64 package.

I²C-bus control bits:

OFTS(1 : 0) = 00 (subaddress 10h, bits D7 and D6).

RGB888 = 1 (subaddress 12h, bit D3).

Fig.27 Application diagram for RGB 24-bit output format.

16 I²C-BUS DESCRIPTION

16.1 I²C-bus format

Table 6 Write procedure

S	SLAVE ADDRESS W	ACK s	SUBADDRESS	ACK s	DATA (N BYTES)	ACK s	P

Table 7 Read procedure (combined format)

S	SLAVE ADDRESS W	ACK s	SUBADDRESS	ACK s	
Sr	SLAVE ADDRESS R	ACK s	DATA (N BYTES)	ACK m	P

Table 8 Description of I²C-bus format

CODE	DESCRIPTION	
S	START condition	
Sr	repeated START condition	
Slave address W	0100 1000b (IICSA = LOW) or 0100 1010b (IICSA = HIGH)	
Slave address R	0100 1001b (IICSA = LOW) or 0100 1011b (IICSA = HIGH)	
ACK s	acknowledge generated by the slave	
ACK m	acknowledge generated by the master	
Subaddress	subaddress byte, see Table 9	
Data	data byte, see Table 9; note 1	
P	STOP condition	
X = LSB slave address	read/write control bit; X = 0, order to write (the circuit is slave receiver); X = 1, order to read (the circuit is slave transmitter)	
Slave address	read = 49h or 4Bh; note 2	
	write = 48h or 4Ah	
	IICSA = 0 or 1	
Subaddress	00h chip version	read and write; note 3
	01h reserved	–
	02h to 05h front-end part	read and write
	06h to 12h decoder part	read and write
	13h to 19h reserved	–
	1Ah to 1Ch Line-21 text slicer part	read only
	1Dh to 1Eh reserved	–
	1Fh status byte	read only

Notes

1. If more than one byte DATA is transmitted then the auto-increment of the subaddress is performed.
2. During slave transmitter mode the SCL-LOW period may be extended by pulling SCL to LOW (in accordance with the I²C-bus specification).
3. The I²C-bus subaddress 00 has to be initialized with 0 before being read.

Table 9 I²C-bus receiver/transmitter overview

SLAVE ADDRESS		READ		WRITE		IICSA			
		49H and 4BH		48H and 4AH		0 and 1			
REGISTER FUNCTION	SUB-ADDR.	D7	D6	D5	D4	D3	D2	D1	D0
Chip version	00	ID07	ID06	ID05	ID04	ID03	ID02	ID01	ID00
Reserved	01	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)
Analog input control 1	02	FUSE1	FUSE0	GUDL2	GUDL1	GUDL0	MODE2	MODE1	MODE0
Analog input control 2	03	(1)	HLNRS	VBSL	WPOFF	HOLDG	GAFIX	GAI28	GAI18
Analog input control 3	04	GAI17	GAI16	GAI15	GAI14	GAI13	GAI12	GAI11	GAI10
Analog input control 4	05	GAI27	GAI26	GAI25	GAI24	GAI23	GAI22	GAI21	GAI20
Horizontal sync start	06	HSB7	HSB6	HSB5	HSB4	HSB3	HSB2	HSB1	HSB0
Horizontal sync stop	07	HSS7	HSS6	HSS5	HSS4	HSS3	HSS2	HSS1	HSS0
Sync control	08	AUFD	FSEL	EXFIL	(1)	VTRC	HPLL	VNOI1	VNOI0
Luminance control	09	BYPS	PREF	BPSS1	BPSS0	VBLB	UPTCV	APER1	APER0
Luminance brightness	0A	BRIG7	BRIG6	BRIG5	BRIG4	BRIG3	BRIG2	BRIG1	BRIG0
Luminance contrast	0B	CONT7	CONT6	CONT5	CONT4	CONT3	CONT2	CONT1	CONT0
Chroma saturation	0C	SATN7	SATN6	SATN5	SATN4	SATN3	SATN2	SATN1	SATN0
Chroma Hue control	0D	HUEC7	HUEC6	HUEC5	HUEC4	HUEC3	HUEC2	HUEC1	HUEC0
Chroma control	0E	CDTO	CM99	CSTD1	CSTD0	DCCF	FCTC	CHBW1	CHBW0
Reserved	0F	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)
Format/delay control	10	OFTS1	OFTS0	HDEL1	HDEL0	VRLN	YDEL2	YDEL1	YDEL0
Output control 1	11	GPSW	(1)	FECO	COMPO	OEYC	OEHV	VIPB	COLO
Output control 2	12	RTSE1	RTSE0	(1)	CBR	RGB888	DIT	AOSL1	AOSL0
Output control 3	13	VCTR1	VCTR0	CCTR1	CCTR0	BCHI1	BCHI0	BCLO1	BCLO0
Reserved	14	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)
V_GATE1_START	15	VSTA7	VSTA6	VSTA5	VSTA4	VSTA3	VSTA2	VSTA1	VSTA0
V_GATE1_STOP	16	VSTO7	VSTO6	VSTO5	VSTO4	VSTO3	VSTO2	VSTO1	VSTO0
V_GATE1_MSB	17	(1)	(1)	(1)	(1)	(1)	(1)	VSTO8	VSTA8
Reserved	18-19	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)
Text slicer status	1A	(1)	(1)	(1)	(1)	F2VAL	F2RDY	F1VAL	F1RDY
Decoded bytes of the text slicer	1B	P1	BYTE16	BYTE15	BYTE14	BYTE13	BYTE12	BYTE11	BYTE10
	1C	P2	BYTE26	BYTE25	BYTE24	BYTE23	BYTE22	BYTE21	BYTE20
Reserved	1D-1E	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)
Status byte	1F	STTC	HLCK	FIDT	GLIMT	GLIMB	WIPA	SLTCA	CODE

Note

1. All unused control bits must be programmed with 0.

16.2 I²C-bus detail

The I²C-bus receiver slave address is 48h/49h. Subaddresses 0F, 1D, 1E and 13 to 19 are reserved; subaddress 01 is reserved for chip version.

16.2.1 SUBADDRESS 00

Table 10 Chip version SA 00, D7 to D0

FUNCTION	CONTROL BITS							
	ID07	ID06	ID05	ID04	ID03	ID02	ID01	ID00
Chip version in read mode(1)	0	0	0	0	X	X	X	X
	chip version number				reserved for chip name			

Note

1. The I²C-bus subaddress 00 has to be initialized with 0 prior to reading it.

16.2.2 SUBADDRESS 02

Table 11 Analog control 1 (Mode select; see Figs 28 to 35) SA 02, D2 to D0

FUNCTION	CONTROL BITS D2 TO D0		
	MODE 2	MODE 1	MODE 0
Mode 0: CVBS (automatic gain)	0	0	0
Mode 1: CVBS (automatic gain)	0	0	1
Mode 2: CVBS (automatic gain)	0	1	0
Mode 3: CVBS (automatic gain)	0	1	1
Mode 4: Y (automatic gain) + C (gain channel 2 fixed to GAI2 level)	1	0	0
Mode 5: Y (automatic gain) + C (gain channel 2 fixed to GAI2 level)	1	0	1
Mode 6: Y (automatic gain) + C (gain channel 2 adapted to Y gain)	1	1	0
Mode 7: Y (automatic gain) + C (gain channel 2 adapted to Y gain)	1	1	1

Table 12 Analog control 1 SA 02, D5 to D3 (see Fig.11)

DECIMAL VALUE	UPDATE HYSTERESIS FOR 9-BIT GAIN	CONTROL BITS D5 TO D3		
		GUDL 2	GUDL 1	GUDL 0
0....	off	0	0	0
....7	±7 LSB	1	1	1

Table 13 Analog control 1 SA 02, D7 and D6

ANALOG FUNCTION SELECT FUSE	CONTROL BITS D7 AND D6	
	FUSE 1	FUSE 0
Amplifier plus anti-alias filter bypassed	0	0
	0	1
Amplifier active	1	0
Amplifier plus anti-alias filter active	1	1

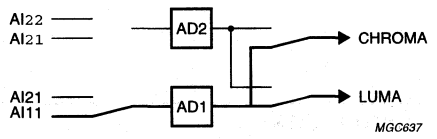


Fig.28 Mode 0; CVBS (automatic gain).

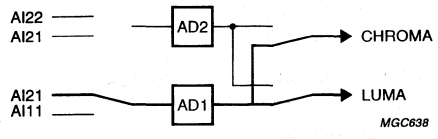


Fig.29 Mode 1; CVBS (automatic gain).

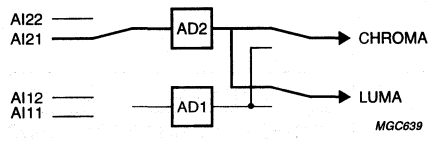


Fig.30 Mode 2; CVBS (automatic gain).

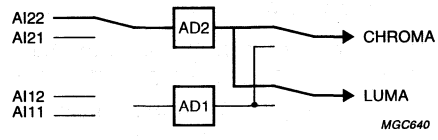


Fig.31 Mode 3; CVBS (automatic gain).

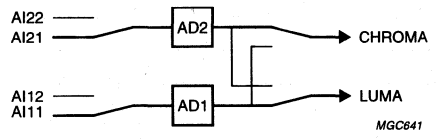


Fig.32 Mode 4 Y (automatic gain) + C (gain channel 2 fixed to GAI1 level).

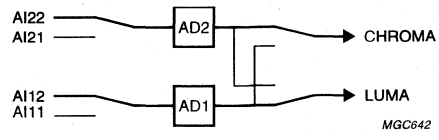


Fig.33 Mode 5 Y (automatic gain) + C (gain channel 2 fixed to GAI1 level).

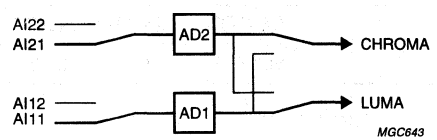


Fig.34 Mode 6 Y (automatic gain) + C (gain channel 2 adapted to Y gain).

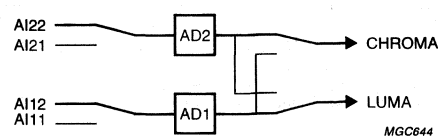


Fig.35 Mode 7 Y (automatic gain) + C (gain channel 2 adapted to Y gain).

16.2.3 SUBADDRESS 03

Table 14 Analog control 2 (AICO2)

FUNCTION	LOGIC LEVEL	DATA BIT
Static gain control channel 1 (GAI18)		
Sign bit of gain control	see Table 15	D0
Static gain control channel 2 (GAI28)		
Sign bit of gain control	see Table 16	D1
Gain control fix (GAFIX)		
Automatic gain controlled by MODE 1 and MODE 0	0	D2
Gain control is user programmable via GAI1 + GAI2	1	D2
Automatic gain control integration (HOLDG)		
AGC active	0	D3
AGC integration hold (freeze)	1	D3
White peak off (WPOFF)		
White peak control active	0	D4
White peak off	1	D4
Vertical blanking select (VBSL)		
Long vertical blanking	0	D5
Short vertical blanking	1	D5
HL not reference select (HLNRS)		
Normal clamping by HL not	0	D6
Reference select by HL not	1	D6

16.2.4 SUBADDRESS 04

Table 15 Gain control analog (AIC03); static gain control channel 1 GAI1 SA 04, D7 to D0

DECIMAL VALUE	GAIN (dB)	SIGN BIT	CONTROL BITS D7 TO D0							
		GAI18	GAI17	GAI16	GAI15	GAI14	GAI13	GAI12	GAI11	GAI10
0....	−5.98	0	0	0	0	0	0	0	0	0
....255	0	0	1	1	1	1	1	1	1	1
256....	0	1	0	0	0	0	0	0	0	0
....511	5.98	1	1	1	1	1	1	1	1	1

16.2.5 SUBADDRESS 05

Table 16 Gain control analog (AIC04); static gain control channel 2 GAI2 SA 05

DECIMAL VALUE	GAIN (dB)	SIGN BIT (SA 03, D1)	CONTROL BITS D7 to D0							
		GAI28	GAI27	GAI26	GAI25	GAI24	GAI23	GAI22	GAI21	GAI20
0....	–5.98	0	0	0	0	0	0	0	0	0
....255	0	0	1	1	1	1	1	1	1	1
256....	0	1	0	0	0	0	0	0	0	0
....511	5.98	1	1	1	1	1	1	1	1	1

16.2.6 SUBADDRESS 06

Table 17 Horizontal sync begin SA 06, D7 to D0

DELAY TIME (STEP SIZE = 8/LLC)	CONTROL BITS D7 to D0							
	HSB7	HSB6	HSB5	HSB4	HSB3	HSB2	HSB1	HSB0
–128...–108	forbidden (outside available central counter range)							
–107...	1	0	0	1	0	1	0	1
...108	0	1	1	0	1	1	0	0
109...127	forbidden (outside available central counter range)							

16.2.7 SUBADDRESS 07

Table 18 Horizontal sync stop SA 07

DELAY TIME (STEP SIZE = 8/LLC)	CONTROL BITS D7 to D0							
	HSS7	HSS6	HSS5	HSS4	HSS3	HSS2	HSS1	HSS0
–128...–108	forbidden (outside available central counter range)							
–107...	1	0	0	1	0	1	0	1
...108	0	1	1	0	1	1	0	0
109...127	forbidden (outside available central counter range)							

16.2.8 SUBADDRESS 08

Table 19 Sync control SA 08, D7 to D5, D3 to D0

FUNCTION	VNOI BITS	LOGIC LEVELS	DATA BITS
Vertical noise reduction (VNOI)			
Normal mode	VNOI1	0	D1
	VNOI0	0	D0
Searching mode	VNOI1	0	D1
	VNOI0	1	D0
Free running mode	VNOI1	1	D1
	VNOI0	0	D0
Vertical noise reduction bypassed	VNOI1	1	D1
	VNOI0	1	D0
Horizontal PLL (HPLL)			
PLL closed	–	0	D2
PLL open, horizontal frequency fixed	–	1	D2
TV/VTR mode select (VTRC)			
TV mode (recommended for poor quality TV signals only)	–	0	D3
VTR mode (recommended as default setting)	–	1	D3
Extended loop filter (EXFIL)			
Word width of the loop filter (LF2) amplification = 16-bit	–	0	D5
Word width of the loop filter (LF2) amplification = 14-bit	–	1	D5
Field selection (FSEL)			
50 Hz, 625 lines	–	0	D6
60 Hz, 525 lines	–	1	D6
Automatic field detection (AUFD)			
Field state directly controlled via FSEL	–	0	D7
Automatic field detection	–	1	D7

16.2.9 SUBADDRESS 09

Table 20 Luminance control

FUNCTION	APER/BPSS BITS	LOGIC LEVELS	DATA BITS
Aperture factor (APER)			
Aperture factor = 0	APER1	0	D1
	APER0	0	D0
Aperture factor = 0.25	APER1	0	D1
	APER0	1	D0
Aperture factor = 0.5	APER1	1	D1
	APER0	0	D0
Aperture factor = 1.0	APER1	1	D1
	APER0	1	D0
Update time interval for AGC value (UPTCV)			
Horizontal update (once per line)	–	0	D2
Vertical update (once per field)	–	1	D2
Vertical blanking luminance bypass (VBLB			
Active luminance processing	–	0	D3
Luminance bypass during vertical blanking	–	1	D3
Aperture band pass (centre frequency) (BPSS) D5 and D4			
Centre frequency = 4.1 MHz	BPSS1	0	D5
	BPSS0	0	D4
Centre frequency = 3.8 MHz; note 1	BPSS1	0	D5
	BPSS0	1	D4
Centre frequency = 2.6 MHz; note 1	BPSS1	1	D5
	BPSS0	0	D4
Centre frequency = 2.9 MHz; note 1	BPSS1	1	D5
	BPSS0	1	D4
Prefilter active (PREF)			
Bypassed	–	0	D6
Active	–	1	D6
Chrominance trap bypass (BYPS)			
Chrominance trap active; default for CVBS mode	–	0	D7
Chrominance trap bypassed; default for S-Video mode	–	1	D7

Note

1. Not to be used with bypassed chrominance trap.

16.2.10 SUBADDRESS 0A

Table 21 Luminance brightness control BRIG7 to BRIG0 SA 0A

OFFSET	CONTROL BITS D7 to D0							
	BRIG7	BRIG6	BRIG5	BRIG4	BRIG3	BRIG2	BRIG1	BRIG0
255 (bright)	1	1	1	1	1	1	1	1
128 (CCIR level)	1	0	0	0	0	0	0	0
0 (dark)	0	0	0	0	0	0	0	0

16.2.11 SUBADDRESS 0B

Table 22 Luminance contrast control CONT7 to CONT0 SA 0B

GAIN	CONTROL BITS D7 to D0							
	CONT7	CONT6	CONT5	CONT4	CONT3	CONT2	CONT1	CONT0
1.999 (maximum)	0	1	1	1	1	1	1	1
1.109 (CCIR level)	0	1	0	0	0	1	1	1
1.0	0	1	0	0	0	0	0	0
0 (luminance off)	0	0	0	0	0	0	0	0
−1 (inverse luminance)	1	1	0	0	0	0	0	0
−2 (inverse luminance)	1	0	0	0	0	0	0	0

16.2.12 SUBADDRESS 0C

Table 23 Chrominance saturation control SATN7 to SATN0 SA 0C

GAIN	CONTROL BITS D7 to D0							
	SATN7	SATN6	SATN5	SATN4	SATN3	SATN2	SATN1	SATN0
1.999 (maximum)	0	1	1	1	1	1	1	1
1.0 (CCIR level)	0	1	0	0	0	0	0	0
0 (colour off)	0	0	0	0	0	0	0	0
−1 (inverse chroma)	1	1	0	0	0	0	0	0
−2 (inverse chroma)	1	0	0	0	0	0	0	0

16.2.13 SUBADDRESS 0D

Table 24 Chrominance hue control HUEC7 to HUEC0 SA 0D

HUE PHASE (DEG)	CONTROL BITS D7 to D0							
	HUEC7	HUEC6	HUEC5	HUEC4	HUEC3	HUEC2	HUEC1	HUEC0
+178.6....	0	1	1	1	1	1	1	1
....0....	0	0	0	0	0	0	0	0
....−180	1	0	0	0	0	0	0	0

16.2.14 SUBADDRESS 0E

Table 25 Chrominance control SA 0E

FUNCTION	CHBW/CSTD	LOGIC LEVELS	DATA BITS
Chroma bandwidth (CHBW0 and CHBW1)			
Small bandwidth (≈ 620 kHz)	CHBW1	0	D1
	CHBW0	0	D0
Nominal bandwidth (≈ 800 kHz)	CHBW1	0	D1
	CHBW0	1	D0
Medium bandwidth (≈ 920 kHz)	CHBW1	1	D1
	CHBW0	0	D0
Wide bandwidth (≈ 1000 kHz)	CHBW1	1	D1
	CHBW0	1	D0
Fast colour time constant (FCTC)			
Nominal time constant	–	0	D2
Fast time constant	–	1	D2
Disable chroma comb filter (DCCF)			
Chroma comb filter on (during VREF = 1) (see Figures 20 and 21)	–	0	D3
Chroma comb filter off	–	1	D3
Colour standard (CSTD0 and CSTD1)			
Colour standard control automatic switching between PAL BGHI and NTSC M	CSTD1	0	D5
	CSTD0	0	D4
Colour standard control automatic switching between NTSC 4.43 (50 Hz) and PAL 4.43 (60 Hz)	CSTD1	0	D5
	CSTD0	1	D4
Colour standard control automatic switching between PAL N and NTSC 4.43 (60 Hz)	CSTD1	1	D5
	CSTD0	0	D4
Colour standard control automatic switching between NTSC N and PAL M	CSTD1	1	D5
	CSTD0	1	D4
CM99 compatibility to SAA7199			
Default value	–	0	D6
To be set if SAA7199 (digital encoder) is used for re-encoding in conjunction with RTCO	–	1	D6
Clear DTO (CDTO)			
Disabled	–	0	D7
Every time CDTO is set, the internal subcarrier DTO phase is reset to 0° and the RTCO output generates a logic 0 at time slot 68 (see RTCO description Fig.16). So an identical subcarrier phase can be generated by an external device (e.g. an encoder).	–	1	D7

16.2.15 SUBADDRESS 10

Table 26 Format/delay control SA 10

LUMINANCE DELAY COMPENSATION (STEPS IN 2/LLC)	CONTROL BITS D2 to D0		
	YDEL2	YDEL1	YDEL0
–4...	1	0	0
...0...	0	0	0
...3	0	1	1

Table 27 VREF pulse position and length VRLN SA 10 (D3)

VRLN	VREF at 60 HZ 525 LINES(1)				VREF at 50 HZ 625 LINES			
	0		1		0		1	
Length	240		242		286		288	
Line number	first	last	first	last	first	last	first	last
Field 1	19 (22)	258 (261)	18 (21)	259 (262)	24	309	23	310
Field 2	282 (285)	521 (524)	281 (284)	522 (525)	337	622	336	623

Note

1. The numbers given in parenthesis refer to CCIR line counting.

Table 28 Fine position of HS HDEL0 and HDEL1 SA 10

FINE POSITION OF HS WITH A STEP SIZE OF 2/LLC	CONTROL BITS D5 and D4	
	HDEL1	HDEL0
0	0	0
1	0	1
2	1	0
3	1	1

Table 29 Output format selection OFTS0 and OFTS1 SA 10

FORMATS	CONTROL BITS D7 and D6	
	OFTS1	OFTS0
RGB 565, RGB 888 (dependent on control bit RGB888) see Table 31	0	0
YUV 422 16 bits	0	1
YUV 411 12 bits	1	0
YUV CCIR-656 8 bits	1	1

16.2.16 SUBADDRESS 11

Table 30 Output control 1 SA 11

FUNCTION	LOGIC LEVELS	DATA BIT
Colour on (COLO)		
Automatic colour killer	0	D0
Colour forced on	1	D0
Decoder VIP bypassed (VIPB)		
DMSD data to YUV output	0	D1
ADC data to YUV output; dependent on mode settings	1	D1
Output enable horizontal/vertical sync (OEHV)		
HS, HREF, VREF and VS high impedance inputs	0	D2
Outputs HS, HREF, VREF and VS active	1	D2
Output enable YUV data (OEYC)		
VPO-bus high-impedance inputs	0	D3
Output VPO-bus active	1	D3
Inverse composite blank (COMPO)		
VREF is vertical reference	0	D4
∀REF is inverse composite blank	1	D4
$\overline{\text{FEI}}$ control (FECO)		
$\overline{\text{FEI}}$ sampling at CREF = LOW (SAA7110 compatible; see Fig.17	0	D5
$\overline{\text{FEI}}$ sampling at CREF = HIGH	1	D5
General purpose switch (GPSW)		
Switches directly pin 64 (53) GPSW; note 1	0	D7
	1	D7

Note

1. The pin number given in parenthesis refers to the 64-pin package.

16.2.17 SUBADDRESS 12

Table 31 Output control 2 SA 12

FUNCTION	AOSL BITS	LOGIC LEVELS	DATA BITS
Analog test select (AOSL)			
AOUT connected to internal test point 1	AOSL1	0	D1
	AOSL0	0	D0
AOUT connected to input AD1	AOSL1	0	D1
	AOSL0	1	D0
AOUT connected to input AD2	AOSL1	1	D1
	AOSL0	0	D0
AOUT connected to internal test point 2	AOSL1	1	D1
	AOSL0	1	D0
Dithering (noise shaping) control (DIT)			
Dithering off	–	0	D2
Dithering on	–	1	D2
RGB output format selection (RGB888)			
RGB565	–	0	D3
RGB888	–	1	D3
Chroma interpolation filter function (CBR)			
Cubic interpolation (default)	–	0	D4
Linear interpolation (lower bandwidth)	–	1	D4
Real time outputs mode select (RTSE0)			
ODD switched to output pin 40 (29); note 1	–	0	D6
VL switched to output pin 40 (29); note 1	–	1	D6
Real time outputs mode select (RTSE1)			
PLIN switched to output pin 39 (28); note 1	–	0	D7
HL switched to output pin 39 (28); note 1	–	1	D7

Note

1. The pin number given in parenthesis refers to the 64-pin package.

16.2.18 Subaddress 1A (read-only register)

Table 32 Line-21 text slicer status SA 1A

I²C-BUS CONTROL BITS	FUNCTION	DATA BIT
F1RDY	new data on field 1 has been acquired (for asynchronous reading); active HIGH	D0
F1VAL	Line-21 of field 1 carries valid data; active HIGH	D1
F2RDY	new data on field 2 has been acquired (for asynchronous reading); active HIGH	D2
F2VAL	Line-21 of field 2 carries valid data; active HIGH	D3

16.2.19 Subaddress 1B (read-only register)

Table 33 First decoded data byte of the text slicer SA 1B,

I²C-BUS CONTROL BITS	FUNCTION	DATA BIT
BYTE1 (6 to 0)	data bit 6 to 0 of first data byte	D6 to D0
P1	parity error flag bit; bit goes HIGH when a parity error has occurred	D7

16.2.20 Subaddress 1C (read-only register)

Table 34 Second decoded data byte of the text slicer SA 1C

I²C-BUS CONTROL BITS	FUNCTION	DATA BIT
BYTE2 (6:0)	data bit 6 to 0 of second data byte	D6 to D0
P2	parity error flag bit; bit goes HIGH when a parity error has occurred	D7

16.2.21 Subaddress 1F (read-only register)

Table 35 Status byte SA 1F

I²C-BUS CONTROL BITS	FUNCTION	DATA BIT
CODE	colour signal according to selected standard has been detected; active HIGH	D0
SLTCA	slow time constant active in WIPA-mode; active HIGH	D1
WIPA	white peak loop is activated; active HIGH	D2
GLIMB	gain value for active luminance channel is limited [min (bottom)]; active HIGH	D3
GLIMT	gain value for active luminance channel is limited [max (top)]; active HIGH	D4
FIDT	identification bit for detected field frequency; LOW = 50 Hz, HIGH = 60 Hz	D5
HLCK	status bit for locked horizontal frequency; LOW = locked, HIGH = unlocked	D6
STTC	status bit for horizontal phase loop; LOW = TV time-constant, HIGH = VTR time-constant	D7

17 FILTER CURVES

17.1 Anti-alias filter curve

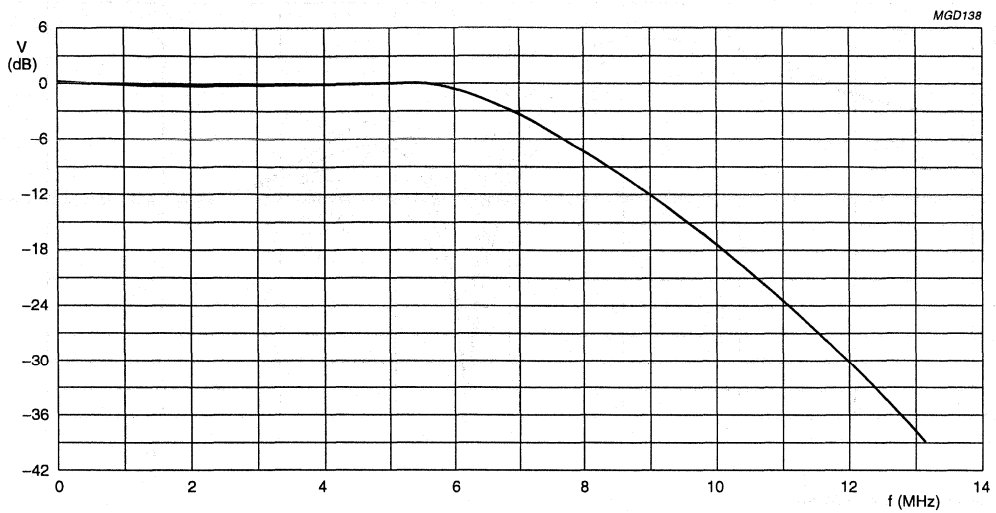
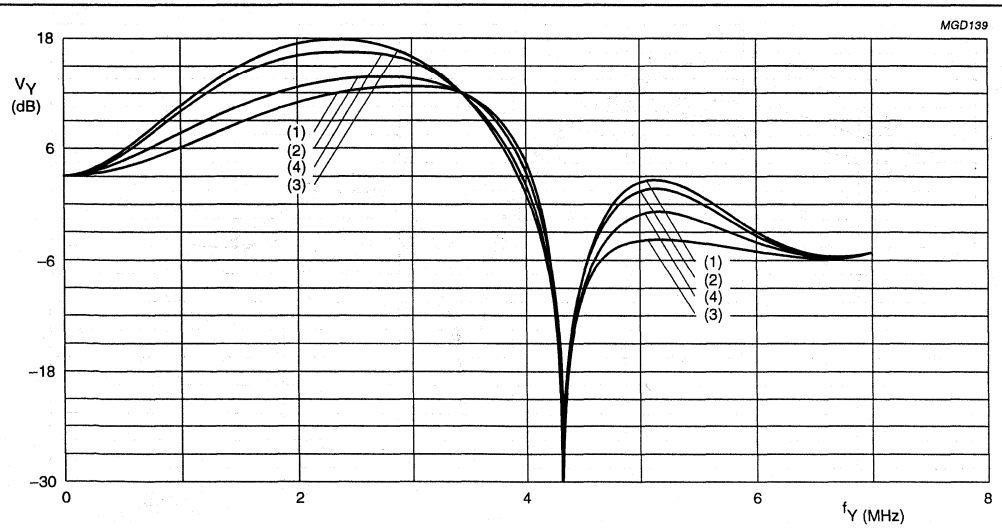


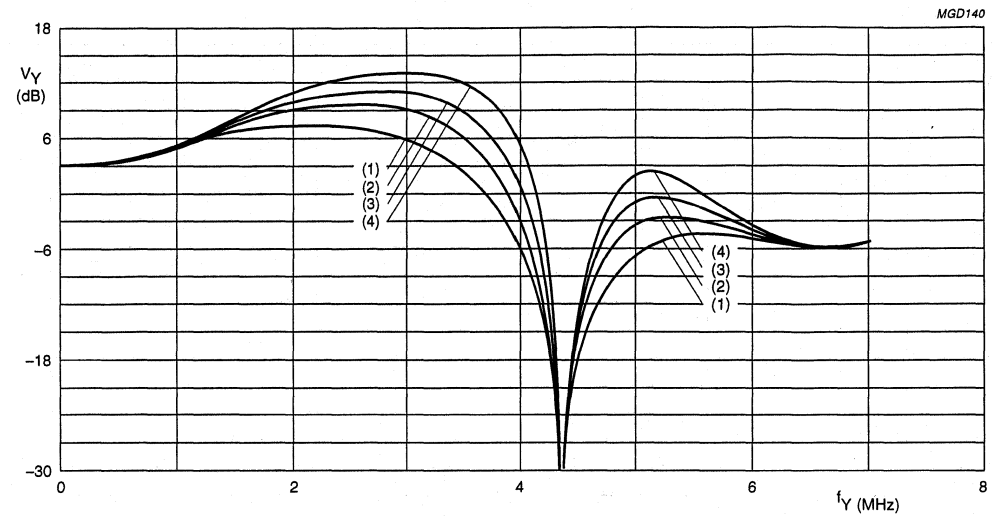
Fig.36 Anti-alias filter.

17.2 Luminance filter curves



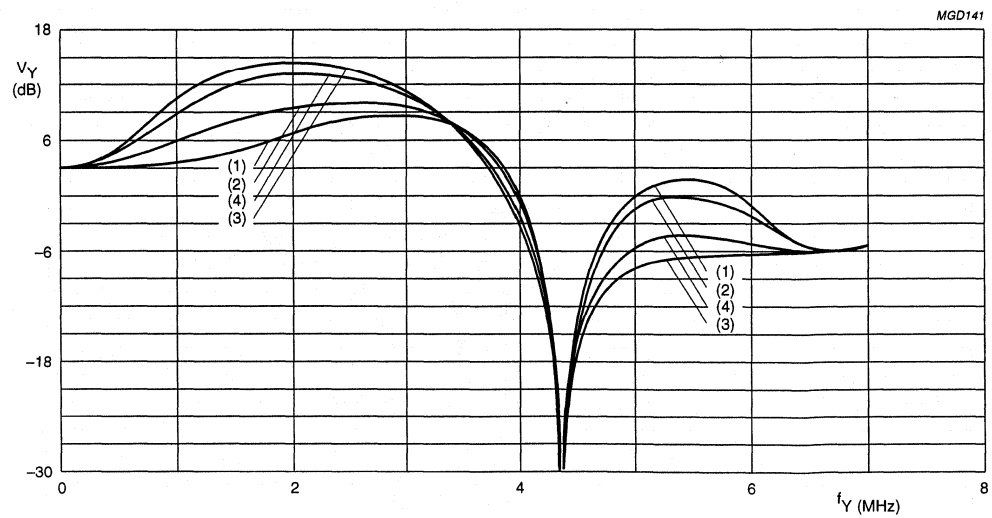
(1) = 43h; (2) = 53h; (3) = 63h; (4) = 73h.

Fig.37 Luminance control SA 09h, 4.43 MHz Trap/CVBS mode, prefilter on, different aperture band-pass centre frequencies.



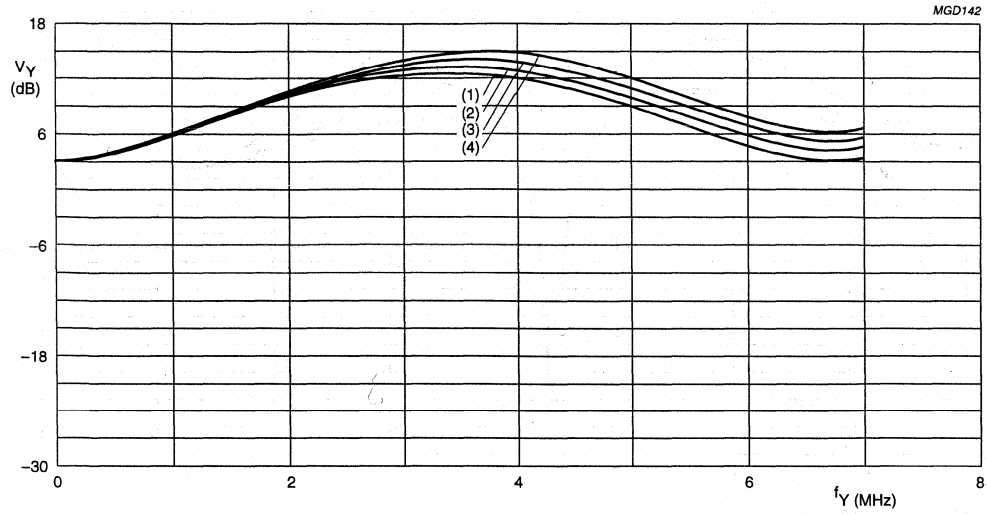
(1) = 40h; (2) = 41h; (3) = 42h; (4) = 43h.

Fig.38 Luminance control SA 09h, 4.43 MHz Trap/CVBS mode, prefilter on, different aperture factors.



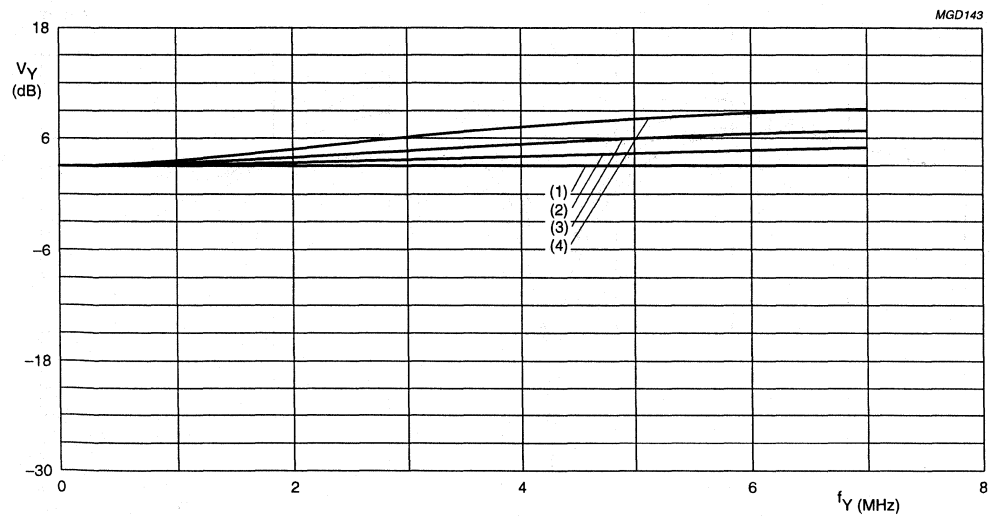
(1) = 03h; (2) = 13h; (3) = 23h; (4) = 33h.

Fig.39 Luminance control SA 09h, 4.43 MHz Trap/CVBS mode, prefilter off, different aperture band-pass centre frequencies.



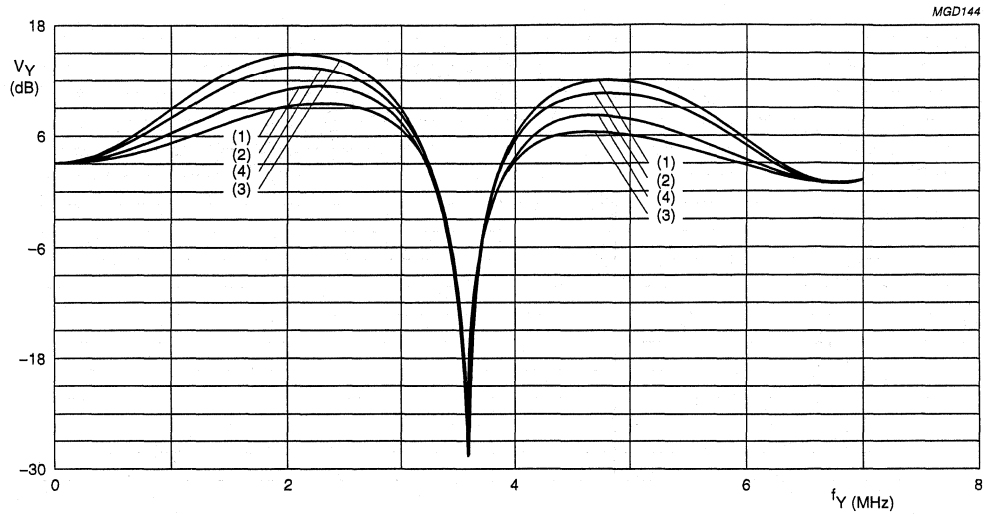
(1) = C0h; (2) = C1h; (3) = C2h; (4) = C3h.

Fig.40 Luminance control SA 09h, Y/C mode, prefilter on, different aperture factors.



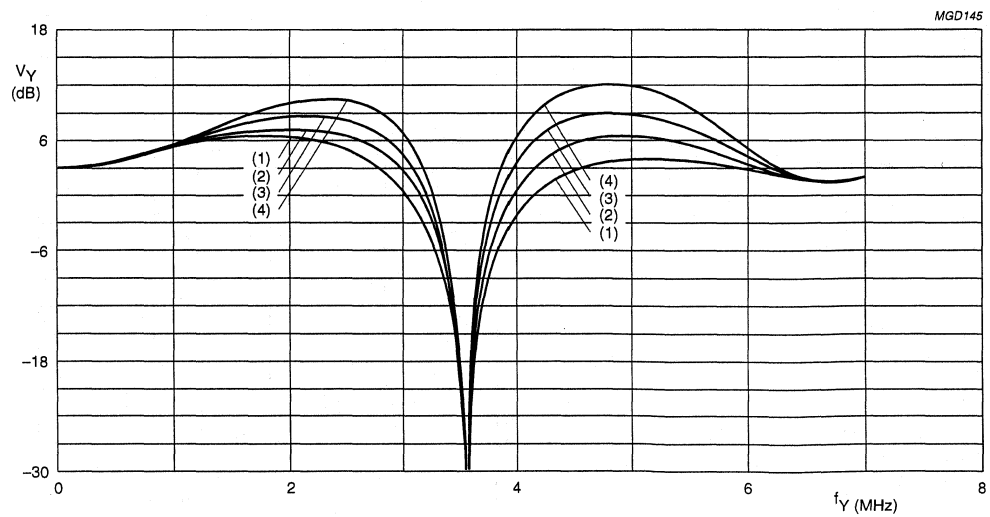
(1) = 80h; (2) = 81h; (3) = 82h; (4) = 83h.

Fig.41 Luminance control SA 09h, Y/C mode, prefilter off, different aperture factors.



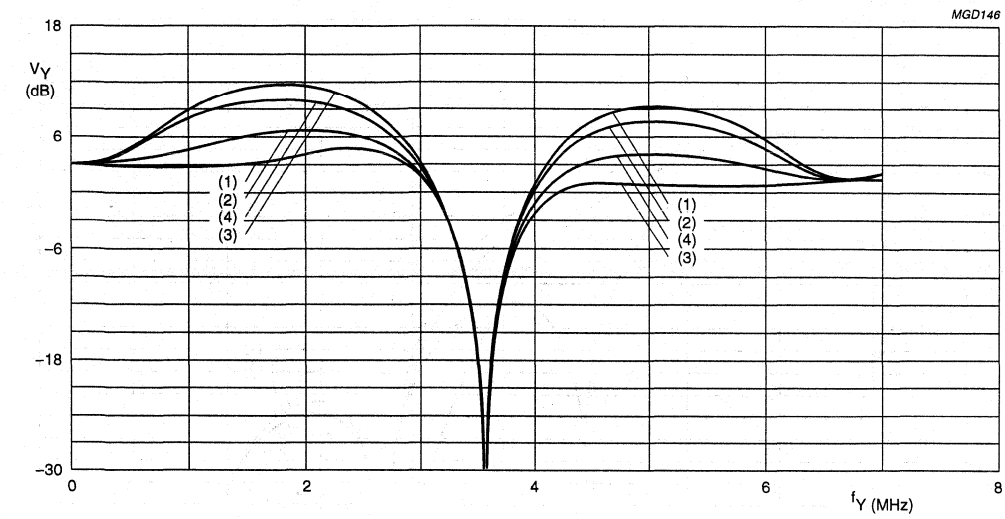
(1) = 43h; (2) = 53h; (3) = 63h; (4) = 73h.

Fig.42 Luminance control SA 09h, 3.58 MHz Trap/CVBS mode, prefilter on, different aperture band-pass centre frequencies.



(1) = 40h; (2) = 41h; (3) = 42h; (4) = 43h.

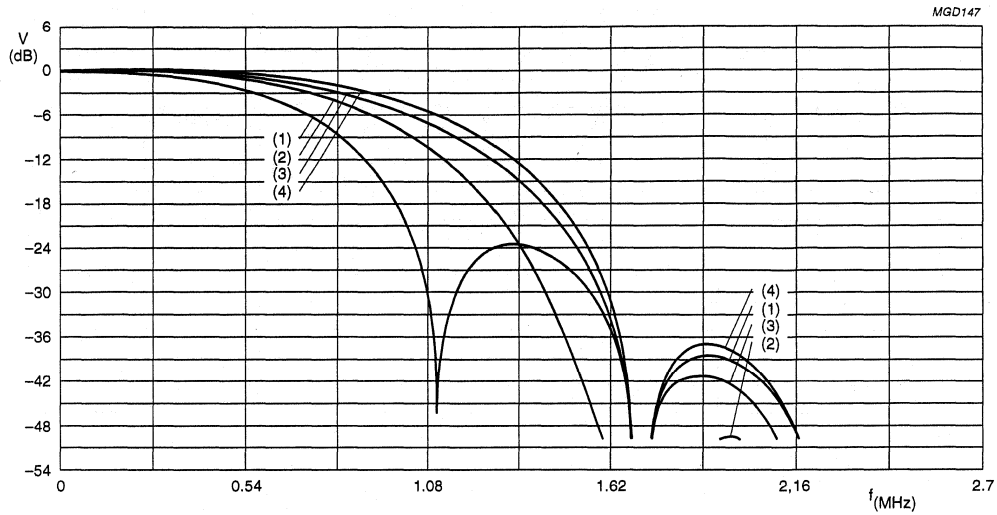
Fig.43 Luminance control SA 09h, 3.58 MHz Trap/CVBS mode, prefilter on, different aperture factors.



(1) = 03h; (2) = 13h; (3) = 23h; (4) = 33h.

Fig.44 Luminance control SA 09h, 3.58 MHz Trap/CVBS mode, prefilter off, different aperture band-pass centre frequencies.

17.3 Chrominance filter curves



Transfer characteristics of the chroma low-pass dependent on CHBW[1:0] settings.
(1) CHBW [1 : 0] = 00; (2) CHBW [1 : 0] = 01; (3) CHBW [1 : 0] = 10; (4) CHBW [1 : 0] = 11.

Fig.45 Chrominance filter.

18 I²C-BUS START SET-UP

- The given values force the following behaviour of the SAA7111:
  - the analog input AI11 expects a signal in CVBS format; analog anti-alias filter active
  - automatic field detection
  - YUV 422/16-bit output format enabled
  - outputs HS, HREF, VREF and VS active
  - contrast, brightness and saturation control in accordance with CCIR standards
  - chrominance processing with nominal bandwidth (800 kHz).

Table 36 I²C-bus start set-up values

SUB (HEX)	FUNCTION	NAME[1]	VALUES (BIN)								(HEX)
			7	6	5	4	3	2	1	0	START
00	chip version	ID0(7 : 0); note 2	0	0	0	0	0	0	0	0	00
01	reserved		0	0	0	0	0	0	0	0	00
02	analog input control 1	FUSE(1 : 0), GUDL(2 : 0), MODE(2 : 0)	1	1	0	0	0	0	0	0	C0
03	analog input control 2	X, HLNRS, VBSL, WPOFF, HOLDG, GAFIX, GAI28, GAI18	0	0	1	0	0	0	1	1	23
04	analog input control 3	GAI(17 : 10)	0	0	0	0	0	0	0	0	00
05	analog input control 4	GAI(27 : 20)	0	0	0	0	0	0	0	0	00
06	horizontal sync start	HSB(7 : 0)	1	1	1	0	1	0	1	1	EB
07	horizontal sync stop	HSS(7 : 0)	1	1	1	0	0	0	0	0	E0
08	sync control	AUFD, FSEL, EXFIL, X, VTRC, HPLL, VNOI(1 : 0)	1	0	0	0	1	0	0	0	88
09	luminance control	BYPS, PREF, BPSS(1 : 0), VBLB, UPTCV, APER(1 : 0)	0	0	0	0	0	0	0	1	01
0A	luminance brightness	BRIG(7 : 0)	1	0	0	0	0	0	0	0	80
0B	luminance contrast	CONT(7 : 0)	0	1	0	0	0	1	1	1	47
0C	chrominance saturation	SATN(7 : 0)	0	1	0	0	0	0	0	0	40
0D	chroma hue control	HUEC(7 : 0)	0	0	0	0	0	0	0	0	00
0E	chrominance control	CDTO, CM99, CSTD(1 : 0), DCCF, FCTC, CHBW(1 : 0)	0	0	0	0	0	0	0	1	01
0F	reserved		0	0	0	0	0	0	0	0	00
10	format/delay control	OFTS(1 : 0), HDEL(1 : 0), VRLN, YDEL(2 : 0)	0	1	0	0	0	0	0	0	40
11	output control 1	GPSW, X, FECO, COMPO, OEYC, OEHV, VIPB, COLO	0	0	0	1	1	1	0	0	1C
12	output control 2	RTSE(1 : 0), X, CBR, RGB888, DIT, AOSL(1 : 0)	0	0	0	0	0	0	0	1	01
13-19	reserved		0	0	0	0	0	0	0	0	00
1A	text slicer status	0, 0, 0, 0, F2VAL, F2RDY, F1VAL, F1RDY	read only register								
1B	decoded bytes of the text slicer	P1, BYTE1(6 : 0)									
1C		P2, BYTE2(6 : 0)									
1D-1E	reserved		0	0	0	0	0	0	0	0	00
1F	status byte	STTC, HLCK, FIDT, GLIMT, GLIMB, WIPA, SLTCA, CODE	read only register								

Notes

1. All X values must be set to LOW.
2. The I²C-bus subaddress 00 has to be initialized with 0 prior to reading.

Enhanced Video Input Processor (EVIP) SAA7111A

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Enhanced Video Input Processor (EVIP) SAA7111A

1 FEATURES

- Four analog inputs, internal analog source selectors, e.g. 4 × CVBS or 2 × Y/C or (1 × Y/C and 2 × CVBS)
- Two analog preprocessing channels
- Fully programmable static gain for the main channels or automatic gain control for the selected CVBS or Y/C channel
- Switchable white peak control
- Two built-in analog anti-aliasing filters
- Two 8-bit video CMOS analog-to-digital converters
- On-chip clock generator
- Line-locked system clock frequencies
- Digital PLL for horizontal-sync processing and clock generation
- Requires only one crystal (24.576 MHz) for all standards
- Horizontal and vertical sync detection
- Automatic detection of 50 and 60 Hz field frequency, and automatic switching between PAL and NTSC standards
- Luminance and chrominance signal processing for PAL BGHI, PAL N, PAL M, NTSC M, NTSC N, NTSC 4.43, NTSC-Japan and SECAM
- User programmable luminance peaking or aperture correction
- Cross-colour reduction for NTSC by chrominance comb filtering
- PAL delay line for correcting PAL phase errors
- Real time status information output (RTCO)
- Brightness Contrast Saturation (BCS) control on-chip
- The YUV (CCIR-601) bus supports a data rate of:
  - $864 \times f_H = 13.5$ MHz for 625 line sources
  - $858 \times f_H = 13.5$ MHz for 525 line sources
- Data output streams for 16, 12 or 8-bit width with the following formats:
  - YUV 4 : 1 : 1 (12-bit)
  - YUV 4 : 2 : 2 (16-bit)
  - YUV 4 : 2 : 2 (CCIR-656) (8-bit)
  - RGB (5, 6, 5) (16-bit) with dither
  - RGB (8, 8, 8) (24-bit) with special application
- Odd/even field identification by a non interlace CVBS input signal
- Fix level for RGB output format during horizontal blanking
- 720 active samples per line on the YUV bus
- One user programmable general purpose switch on an output pin
- Built in line-21 text slicer
- A 27 MHz Vertical Blanking Interval (VBI) data bypass programmable by I²C-bus for INTERCAST applications
- Power-on control
- Two via I²C-bus switchable outputs for the digitized CVBS or Y/C input signals AD1 (7 to 0) and AD2 (7 to 0)
- Chip enable function (reset for the clock generator)
- Compatible with memory-based features (line-locked clock)
- Boundary scan test circuit complies with the *IEEE Std. 1149.1 – 1990* (ID-Code = 0 F111 02 B)
- I²C-bus controlled (full read-back ability by an external controller)
- Low power (<0.5 W), low voltage (3.3 V), small package (LQFP64)
- 5 V compatible I²C-bus voltage
- 5 V tolerant digital I/O ports.

2 APPLICATIONS

- Desktop/Notebook (PCMCIA) video
- Multimedia
- Digital television
- Image processing
- Video phone
- Intercast.

3 GENERAL DESCRIPTION

The Enhanced Video Input Processor (EVIP) is a combination of a two-channel analog preprocessing circuit including source selection, anti-aliasing filter and ADC, an automatic clamp and gain control, a Clock Generation Circuit (CGC), a digital multi-standard decoder (PAL BGHI, PAL M, PAL N, NTSC M, NTSC-Japan NTSC N and SECAM),
a brightness/contrast/saturation control circuit, a colour space matrix (see Fig.1) and a 27 MHz VBI-data bypass.

The pure 3.3 V CMOS circuit SAA7111A, analog front-end and digital video decoder, is a highly integrated circuit for desktop video applications. The decoder is based on the principle of line-locked clock decoding and is able to decode the colour of PAL, SECAM and NTSC signals into CCIR-601 compatible colour component values. The SAA7111A accepts as analog inputs CVBS or S-video (Y/C) from TV or VTR sources. The circuit is I^2C-bus controlled.
The SAA7111A then supports several text features as Line 21 data slicing and a high-speed VBI data bypass for Intercast.

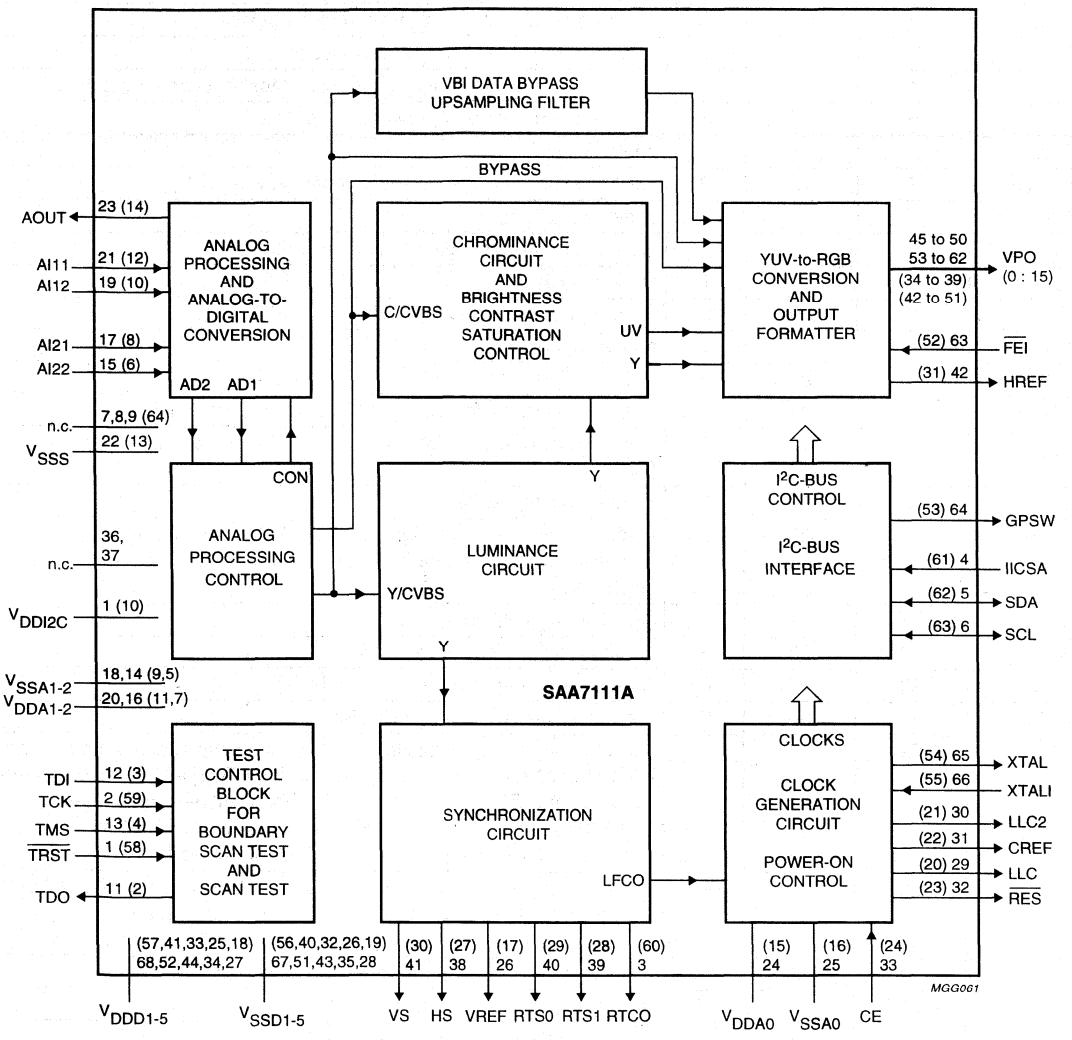
4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage	3.0	3.3	3.6	V
V_{DDA}	analog supply voltage	3.1	3.3	3.5	V
T_{amb}	operating ambient temperature	0	25	70	°C
P_{A+D}	analog and digital power	–	0.5	–	W

5 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7111A	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
SAA7111AH	QFP64	plastic quad flat package; 64 leads (lead length 1.6 mm); body 14 × 14 × 2.7 mm	SOT393-1
SAA7111AWP	PLCC68	plastic leaded chip carrier; 68 leads; body 24 × 24 × 4.5 mm	SOT188-2

6 BLOCK DIAGRAM



The pin numbers given in parenthesis refer to the 64-pin package.

Fig.1 Block diagram.

7 PINNING

SYMBOL	PINS		I/O/P	DESCRIPTION
	(L)QFP64	PLCC68		
V_{DDI2C}	1	10	P	open for 3.3 V I²C-bus, connected to 5 V for 5 V I²C-bus compatibility
TDO	2	11	O	test data output for boundary scan test; note 3
TDI	3	12	I	test data input for boundary scan test; note 3
TMS	4	13	I	test mode select input for boundary scan test or scan test; note 3
V_{SSA2}	5	14	P	ground for analog supply voltage channel 2
AI22	6	15	I	analog input 22
V_{DDA2}	7	16	P	positive supply voltage for analog channel 2 (+3.3 V)
AI21	8	17	I	analog input 21
V_{SSA1}	9	18	P	ground for analog supply voltage channel 1
AI12	10	19	I	analog input 12
V_{DDA1}	11	20	P	positive supply voltage for analog channel 1 (+3.3 V)
AI11	12	21	I	analog input 11
V_{SSS}	13	22	P	substrate ground connection
AOUT	14	23	O	analog test output; for testing the analog input channels
V_{DDA0}	15	24	P	positive supply voltage for internal Clock Generator Circuit (CGC) (+3.3 V)
V_{SSA0}	16	25	P	ground for internal CGC
VREF	17	26	O	vertical reference output signal (I²C-bit COMPO = 0) or inverse composite blanking signal (I²C-bit COMPO = 1) (enabled via I²C-bus bit OEHV)
V_{DDD5}	18	27	P	digital supply voltage 5 (+3.3 V)
V_{SSD5}	19	28	P	ground for digital supply voltage 5
LLC	20	29	O	line-locked system clock output (27 MHz)
LLC2	21	30	O	line-locked clock ½ output (13.5 MHz)
CREF	22	31	O	clock reference output: this is a clock qualifier signal distributed by the internal CGC for a data rate of LLC2. Using CREF all interfaces on the VPO bus are able to generate a bus timing with identical phase. If CCIR 656 format is selected (OFTS0 = 1 and OFTS1 = 1) an inverse composite blanking signal (pixel qualifier) is provided on this pin.
$\overline{RES}$	23	32	O	reset output (active LOW); sets the device into a defined state. All data outputs are in high impedance state. The I²C-bus is reset (waiting for start condition).
CE	24	33	I	chip enable; connection to ground forces a reset
V_{DDD4}	25	34	P	digital supply voltage input 4 (+3.3 V)
V_{SSD4}	26	35	P	ground for digital supply voltage input 4
HS	27	38	O	horizontal sync output signal (programmable); the positions of the positive and negative slopes are programmable in 8 LLC increments over a complete line (= 64 µs) via I²C-bus bytes HSB and HSS. Fine position adjustment in 2 LLC increments can be performed via I²C-bus bits HDEL1 and HDEL0.

SYMBOL	PINS		I/O/P	DESCRIPTION
	(L)QFP64	PLCC68		
RTS1	28	39	O	two functions output; controlled by I²C-bus bit RTSE1. RTSE1 = 0: PAL line identifier (LOW = PAL line); indicates the inverted and non-inverted R–Y component for PAL signals. RTSE1 = 1: H-PLL locked indicator; a high state indicates that the internal horizontal PLL has locked.
RTS0	29	40	O	two functions output; controlled by I²C-bus bit RTSE0. RTSE0 = 0: odd/even field identification (HIGH = odd field). RTSE0 = 1: vertical locked indicator; a HIGH state indicates that the internal Vertical Noise Limiter (VNL) has locked.
VS	30	41	O	vertical sync signal (enabled via I²C-bus bit OEHV); this signal indicates the vertical sync with respect to the YUV output. The HIGH period of this signal is approximately six lines if the VNL function is active. The positive slope contains the phase information for a deflection controller.
HREF	31	42	O	horizontal reference output signal (enabled via I²C-bus bit OEHV); this signal is used to indicate data on the digital YUV bus. The positive slope marks the beginning of a new active line. The HIGH period of HREF is 720 Y samples long. HREF can be used to synchronize data multiplexer/demultiplexer. HREF is also present during the vertical blanking interval.
V_{SSD3}	32	43	P	ground for digital supply voltage input 3
V_{DDD3}	33	44	P	digital supply voltage 3 (+3.3 V)
VPO (15 to 10)	34 to 39	45 to 50	O	digital VPO-bus (Video Port Out) signal; higher bits of the 16-bit VPO-bus or the 16-bit RGB-bus output signal. The output data rate, the format and multiplexing scheme of the VPO-bus are controlled via I²C-bus bits OFTS0 and OFTS1. If I²C-bus bit VIPB = 1 the six MSBs of the digitized input signal are connected to these outputs, configured by the I²C-bus 'MODE' bits (see Figs 33 to 40): LUMA -> VPO15 to VPO8, CHROMA -> VPO7 to VPO0.
V_{SSD2}	40	51	P	ground for digital supply voltage input 2
V_{DDD2}	41	52	P	digital supply voltage 2 (+3.3 V)
VPO (9 to 0)	42 to 51	53 to 62	O	digital VPO-bus output signal; lower bits of the 16-bit YUV-bus or the 16-bit RGB-bus output signal. The output data rate, the format and multiplexing schema of the VPO-bus are controlled via I²C-bus bits OFTS0 and OFTS1. If I²C-bus bit VIPB = 1 the digitized input signal are connected to these outputs, configured by the I²C-bus 'MODE' bits (see Figs 33 to 40): LUMA -> VPO15 to VPO8, CHROMA -> VPO7 to VPO0.
$\overline{FEI}$	52	63	I	fast enable input signal (active LOW); this signal is used to control fast switching on the digital YUV-bus. A HIGH at this input forces the IC to set its Y and UV outputs to the high impedance state.
GPSW	53	64	O	general purpose switch output; the state of this signal is set via I²C-bus control and the levels are TTL compatible
XTAL	54	65	O	second terminal of crystal oscillator; not connected if external clock signal is used
XTALI	55	66	I	input terminal for 24.576 MHz crystal oscillator or connection of external oscillator with CMOS compatible square wave clock signal
V_{SSD1}	56	67	P	ground for digital supply voltage input 1

SYMBOL	PINS		I/O/P	DESCRIPTION
	(L)QFP64	PLCC68		
V_{DDD1}	57	68	P	digital supply voltage input 1 (+3.3 V)
$\overline{TRST}$	58	1	I	test reset input not (active LOW), for boundary scan test; notes 1, 2, 3
TCK	59	2	I	test clock for boundary scan test; note 3
RTCO	60	3	O	real time control output: contains information about actual system clock frequency, subcarrier frequency and phase and PAL sequence
IICSA	61	4	I	I^2C-bus slave address select; 0 = 48H for write, 49H for read 1 = 4AH for write, 4BH for read
SDA	62	5	I/O	serial data input/output (I^2C-bus)
SCL	63	6	I/O	serial clock input/output (I^2C-bus)
n.c.	64	7, 8, 9, 36 and 37	–	not connected

Notes

1. For board design without boundary scan implementation (pin compatibility with the SAA7110) connect the $\overline{TRST}$ pin to ground.
2. This pin provides easy initialization of BST circuit. $\overline{TRST}$ can be used to force the TAP (Test Access Port) controller to the Test-Logic-Reset state (normal operation) at once.
3. In accordance with the *IEEE1149.1* standard the pads TCK, TDI, TMS and $\overline{TRST}$ are input pads with an internal pull-up transistor and TDO a 3-state output pad.

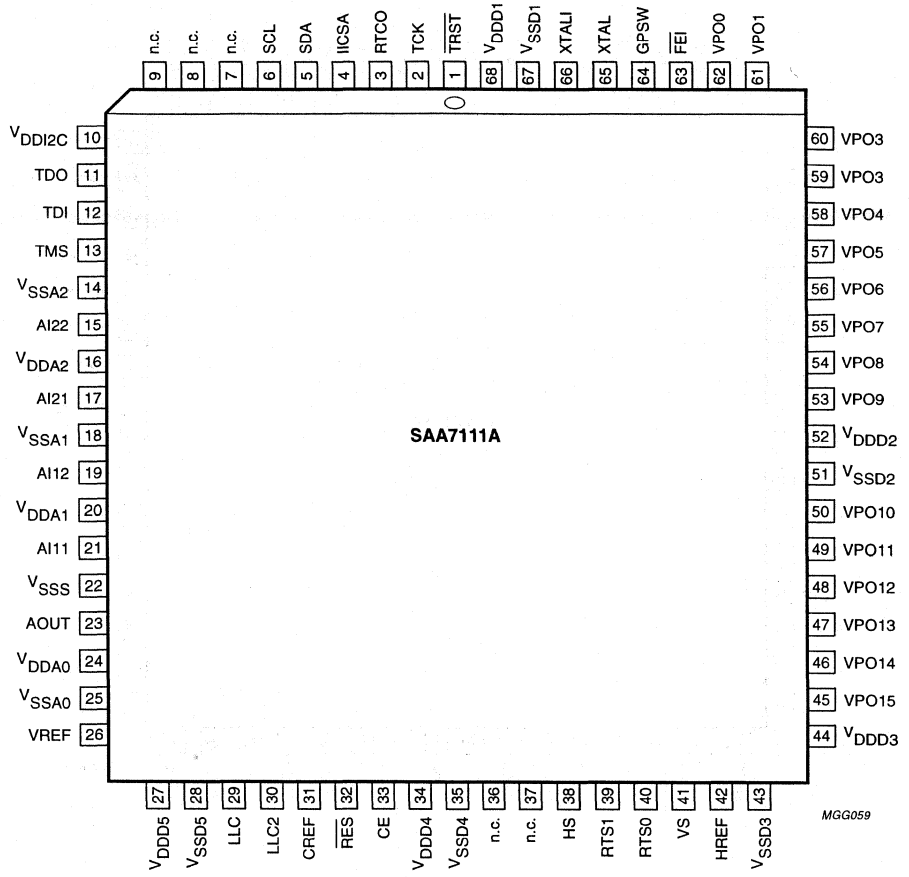


Fig.2 Pin configuration (PLCC68).

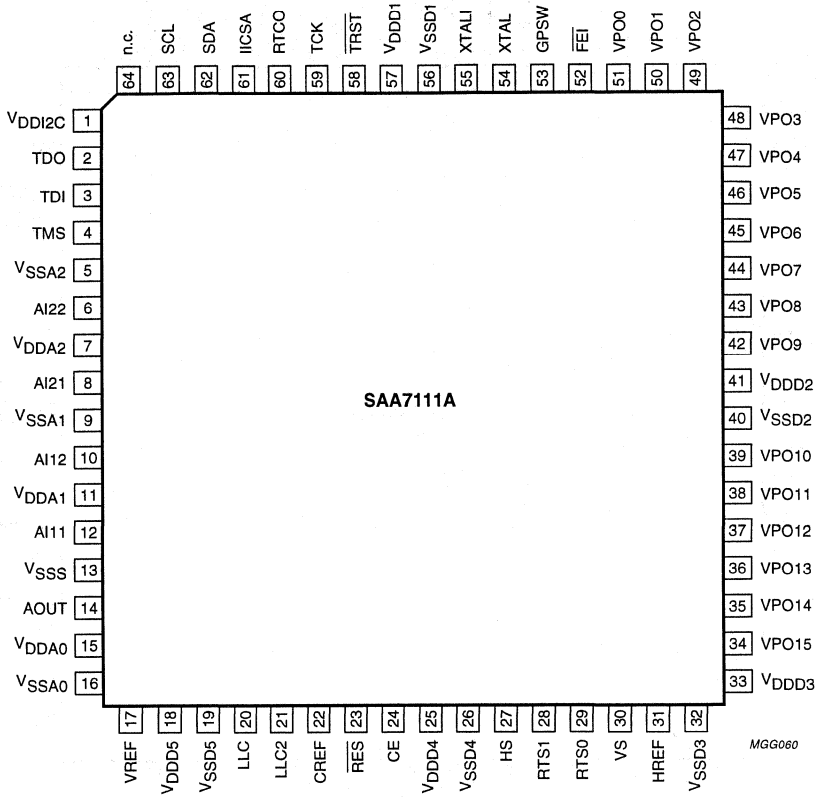


Fig.3 Pin configuration (LQFP64/QFP64).

8 FUNCTIONAL DESCRIPTION

8.1 Analog input processing

The SAA7111A offers four analog signal inputs, two analog main channels with source switch, clamp circuit, analog amplifier, anti-alias filter and video CMOS ADC (see Fig.9).

8.2 Analog control circuits

The anti-alias filters are adapted to the line-locked clock frequency via a filter control circuit. During the vertical blanking time, gain and clamping control are frozen.

8.2.1 CLAMPING

The clamp control circuit controls the correct clamping of the analog input signals. The coupling capacitor is also used to store and filter the clamping voltage. An internal digital clamp comparator generates the information with respect to clamp-up or clamp-down. The clamping levels for the two ADC channels are fixed for luminance (60) and chrominance (128). Clamping time in normal use is set with the HCL pulse at the back porch of the video signal.

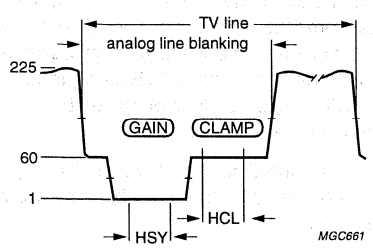


Fig.4 Analog line with clamp (HCL) and gain range (HSY).

8.2.2 GAIN CONTROL

Signal (white) peak control limits the gain at signal overshoots. The flow charts (see Figs 13 and 14) show more details of the AGC. The influence of supply voltage variation within the specified range is automatically eliminated by clamp and automatic gain control.

The gain control circuit receives (via the I^2C-bus) the static gain levels for the two analog amplifiers or controls one of these amplifiers automatically via a built-in automatic gain control (AGC) as part of the Analog Input Control (AICO).

The AGC (automatic gain control for luminance) is used to amplify a CVBS or Y signal to the required signal amplitude, matched to the ADCs input voltage range. The AGC active time is the sync bottom of the video signal.

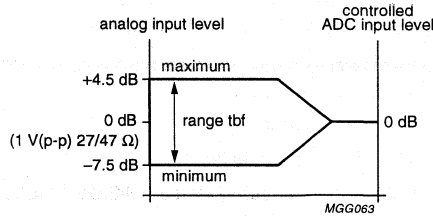


Fig.5 Automatic gain range.

8.3 Chrominance processing

The 8-bit chrominance signal is fed to the multiplication inputs of a quadrature demodulator, where two subcarrier signals from the local oscillator DTO1 are applied (0 and 90° phase relationship to the demodulator axis). The frequency is dependent on the present colour standard. The output signals of the multipliers are low-pass filtered (four programmable characteristics) to achieve the desired bandwidth for the colour difference signals (PAL, NTSC) or the 0 and 90° FM-signals (SECAM).

The colour difference signals are fed to the Brightness/Contrast/Saturation block (BCS), which includes the following five functions:

- AGC (Automatic Gain Control for chrominance PAL and NTSC)
- Chrominance amplitude matching (different gain factors for R–Y and B–Y to achieve CCIR-601 levels Cr and Cb for all standards)
- Chrominance saturation control
- Luminance contrast and brightness.
- Limiting YUV to the values 1 (min.) and 254 (max.) to fulfil CCIR-601 requirements.

The SECAM-processing contains the following blocks:

- Baseband 'bell' filters to reconstruct the amplitude and phase equalized 0 and 90° FM-signals
- Phase demodulator and differentiator (FM-demodulation)
- De-emphasis filter to compensate the pre-emphasised input signal, including frequency offset compensation (DB or DR white carrier values are subtracted from the signal, controlled by the SECAM-switch signal).

The burst processing block provides the feedback loop of the chroma PLL and contains;

- Burst gate accumulator
- Colour identification and killer
- Comparison nominal/actual burst amplitude (PAL/NTSC standards only)
- Loop filter chrominance gain control (PAL/NTSC standards only)
- Loop filter chrominance PLL (only active for PAL/NTSC standards)
- PAL/SECAM sequence detection, H/2-switch generation
- Increment generation for DTO1 with divider to generate stable subcarrier for non-standard signals.

The chrominance comb filter block eliminates crosstalk between the chrominance channels in accordance with the PAL standard requirements. For NTSC colour standards the chrominance comb filter can be used to eliminate crosstalk from luminance to chrominance (cross-colour) for vertical structures. The comb filter can be switched off if desired. The embedded line delay is also used for SECAM recombination (cross-over switches).

The resulting signals are fed to the variable Y-delay compensation, RGB matrix, dithering circuit and output interface, which contains the VPO output formatter and the output control logic (see Fig.10).

8.4 Luminance processing

The 8-bit luminance signal, a digital CVBS format or a luminance format (S-VHS, HI8), is fed through a switchable prefilter. High frequency components are emphasized to compensate for loss. The following chrominance trap filter (f_0 = 4.43 or 3.58 MHz centre frequency selectable) eliminates most of the colour carrier signal, therefore, it must be bypassed for S-video (S-VHS, HI8) signals.

The high frequency components of the luminance signal can be peaked (control for sharpness improvement via I²C-bus) in two band-pass filters with selectable transfer characteristic. This signal is then added to the original (unpeaked) signal. A switchable amplifier achieves common DC amplification, because the DC gains are different in both chrominance trap modes. The improved luminance signal is fed to the BCS control located in the chrominance processing block (see Fig.11).

8.5 RGB matrix

Y, Cr and Cb data are converted after interpolation into RGB data in accordance with CCIR-601 recommendations. The realized matrix equations consider the digital quantization:

$$R = Y + 1.371\ Cr$$

$$G = Y - 0.336\ Cb - 0.698\ Cr$$

$$B = Y + 1.732\ Cb$$

After dithering (noise shaping) the RGB data is fed to the output interface within the VPO-bus output formatter.

8.6 VBI-data bypass

For a 27 MHz VBI-data bypass the offset binary CVBS signal is upsampled behind the ADCs. Upsampling of the CVBS signal from 13.5 to 27 MHz is possible, because the ADCs deliver high performance at 13.5 MHz sample clock. Suppressing of the back folded CVBS frequency components after upsampling is achieved by an interpolation filter (see Fig.42).

The TUF block on the digital top level performs the upsampling and interpolation for the bypassed CVBS signal (see Fig.10).

8.7 VPO-bus (digital outputs)

The 16-bit VPO-bus transfers digital data from the output interfaces to a feature box or a field memory, a digital colour space converter (SAA7192 DCSC), a video enhancement and digital-to-analog processor (SAA7165 VEDA2) or a colour graphics board (Targa-format) as a graphical user interface.

The output data formats are controlled via the I²C-bus bits OFTS0, OFTS1 and RGB888. Timing for the data stream formats, YUV (4,: 1 : 1) (12-bit), YUV (4,: 2 : 2) (16-bit), RGB (5, 6, 5) (16-bit) and RGB (8, 8, 8) (24-bit) with an LLC2 data rate, is achieved by marking each second positive rising edge of the clock LLC in conjunction with CREF (clock reference) (except RGB (8, 8, 8), see special application in Fig.32).

The higher output signals VPO15 to VPO8 in the YUV format perform the digital luminance signal. The lower output signals VPO7 to VPO0 in the YUV format are the bits of the multiplexed colour difference signals (B–Y) and (R–Y). The arrangement of the RGB (5, 6, 5) and RGB (8, 8, 8) data stream bits on the VPO-bus is given in Table 5.

The data stream format YUV 4 : 2 : 2 (the 8 higher output signals VPO15 to VPO8) in LLC data rate fulfils the CCIR-656 standard with its own timing reference code at the start and end of each video data block.

A pixel in the format tables is the time required to transfer a full set of samples. If 16-bit 4 : 2 : 2 format is selected two luminance samples are transmitted in comparison to one (B–Y) and one (R–Y) sample within a pixel.The time frames are controlled by the HREF signal.

Fast enable is achieved by setting input $\overline{FEI}$ to LOW. The signal is used to control fast switching on the digital VPO-bus. HIGH on this pin forces the VPO outputs to a high-impedance state (see Figs 18 and 19). The I²C-bus bit OEYC has to be set HIGH to use this function.

The digitized PAL, SECAM or NTSC signals AD1 (7 to 0) and AD2 (7 to 0) are connected directly to the VPO-bus via I²C-bus bit VIPB = 1 and MODE = 4, 5, 6 or 7.

AD1 (7 to 0) -> VPO (15 to 8) and
AD2 (7 to 0) -> VPO (7 to 0)

The selection of the analog input channels is controlled via I²C-bus subaddress 02 MODE select.

The upsampled 8-bit offset binary CVBS signal (VBI-data bypass) is multiplexed under control of the I²C-bus to the digital VPO-bus (see Fig.6).

8.8 Reference signals HREF, VREF and CREF

- HREF: The positive slope of the HREF output signal indicates the beginning of a new active video line. The high period is 720 luminance samples long and is also present during the vertical blanking. The description of timing and position from HREF is illustrated in Figs 15, 16, 21 and 23.
- VREF: The VREF output delivers a vertical reference signal or an inverse composite blank signal controlled via the I²C-bus [subaddress 11, inverse composite blank (COMPO)]. Furthermore four different modes of vertical reference signals are selectable via the I²C-bus [subaddress 13, vertical reference output control (VCTR1 and VCTR0)]. The description of VREF timing and position is illustrated in Figs 15, 16, 24 and 25.
- CREF: The CREF output delivers a clock/pixel qualifier signal for external interfaces to synchronize to the VPO-bus data stream.

  Four different modes for the clock qualifier signal are selectable via the I²C-bus [subaddress 13, clock reference output control (CCTR1 and CCTR0]. The description of CREF timing and position is illustrated in Figs 16, 18, 20 and 21.

8.9 Synchronization

The prefiltered luminance signal is fed to the synchronization stage. Its bandwidth is reduced to 1 MHz in a low-pass filter. The sync pulses are sliced and fed to the phase detectors where they are compared with the sub-divided clock frequency. The resulting output signal is applied to the loop filter to accumulate all phase deviations. Internal signals (e. g. HCL and HSY) are generated in accordance with analog front-end requirements. The output signals HS, VS, and PLIN are locked to the timing reference, guaranteed between the input signal and the HREF signal, as further improvements to the circuit may change the total processing delay. It is therefore not recommended to use them for applications which require absolute timing accuracy on the input signals. The loop filter signal drives an oscillator to generate the line frequency control signal LFCO (see Fig.11).

8.10 Clock generation circuit

The internal CGC generates all clock signals required for the video input processor. The internal signal LFCO is a digital-to-analog converted signal provided by the horizontal PLL. It is the multiple of the line frequency (6.75 MHz = 429/432 × f_H). Internally the LFCO signal is multiplied by a factor of 2 or 4 in the PLL circuit (including phase detector, loop filtering, VCO and frequency divider) to obtain the LLC and LLC2 output clock signals. The rectangular output clocks have a 50% duty factor (see Fig.26).

8.11 Power-on reset and CE input

A missing clock, insufficient digital or analog V_{DDA0} supply voltages (below 2.7 V) will initiate the reset sequence; all outputs are forced to 3-state. The indicator output $\overline{RES}$ is LOW for approximately 128LLC after the internal reset and can be applied to reset other circuits of the digital TV system.

It is possible to force a reset by pulling the chip enable (CE) to ground. After the rising edge of CE and sufficient power supply voltage, the outputs LLC, LLC2, CREF, RTCO, RTS0, RTS1, GPSW and SDA return from 3-state to active, while HREF, VREF, HS and VS remain in 3-state and have to be activated via I²C-bus programming (see Table 4).

8.12 RTCO output

The real time control and status output signal contains serial information about the actual system clock (increment of the HPLL), subcarrier frequency [increment and phase (via reset) of the FSC-PLL] and PAL sequence bit. The signal can be used for various applications in external circuits, e.g. in a digital encoder to achieve clean encoding (see Fig.20).

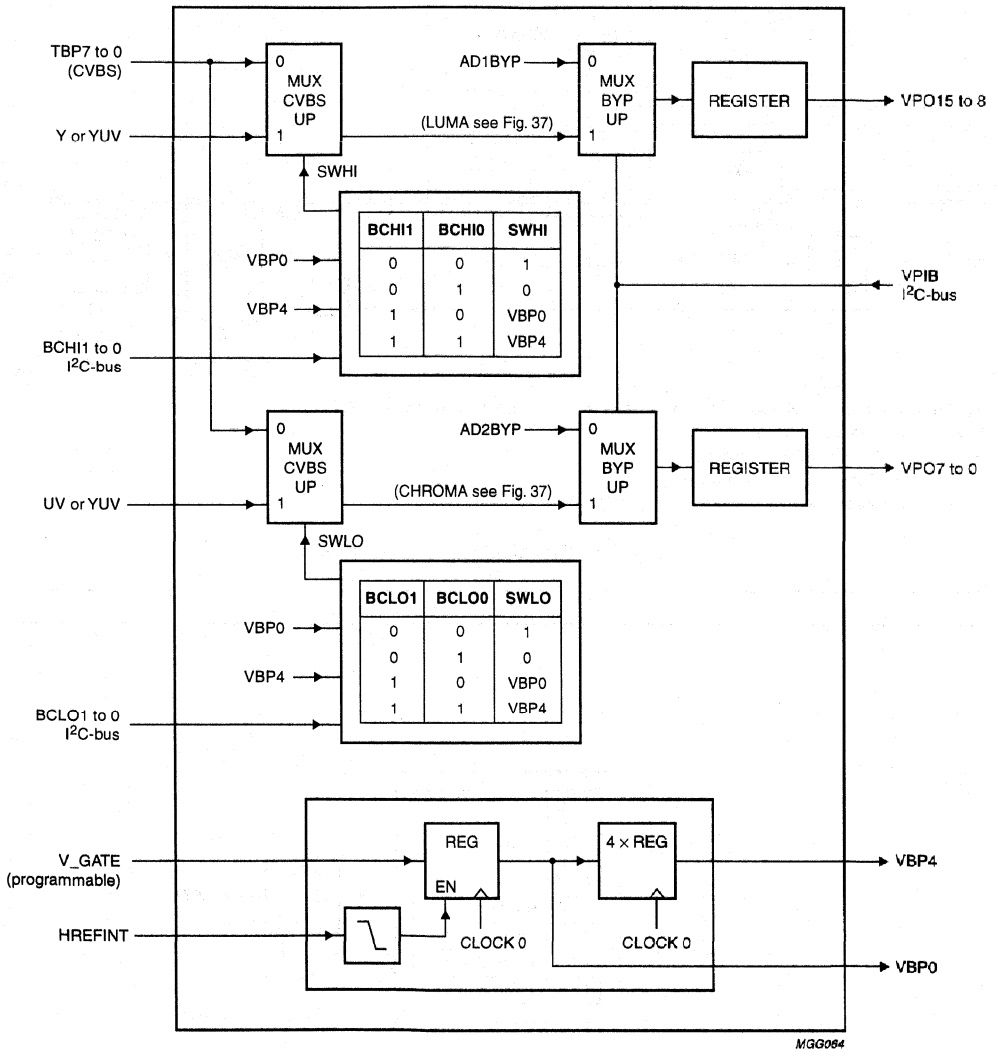
8.13 The Line-21 text slicer

The text slicer block detects and acquires Line-21 Closed Captioning data from a 525-line CVBS signal. Extended data services on Line-21 Field 2 are also supported.
If valid data is detected the two data bytes are stored in two I²C-bus registers. A parity check is also performed and the result is stored in the MSB of the corresponding byte.
A third I²C-bus register is provided for data valid and data ready flags. The two bits F1VAL and F2VAL indicate that the input signal carries valid Closed Captioning data in the corresponding fields. The data ready bits F1RDY and F2RDY have to be evaluated if asynchronous I²C-bus reading is used.

8.13.1 Suggestions for I²C-bus interface of the display software reading Line-21 data

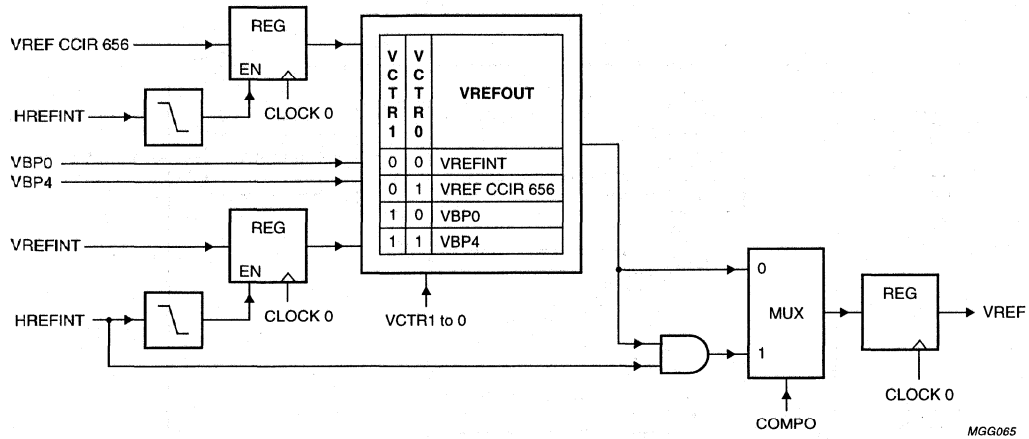
There are two methods by which the software can acquire the data:

1. Synchronous reading once per frame (or once per field); It can use either the rising edge (Line-21 Field 1) or both edges (Line-21 Field 1 or 2) of the ODD signal (pin RTSO) to initiate an I²C-bus read transfer of the three registers 1A, 1B and 1C.
2. Asynchronous reading; It can poll either the F1RDY bit (Line-21 Field 1) or both F1RDY/F2RDY bits (Line-21 Field 1 or 2). After valid data has been read the corresponding F*RDY bit is set to LOW until new data has arrived. The polling frequency has to be slightly higher than the frame or field frequency, respectively.



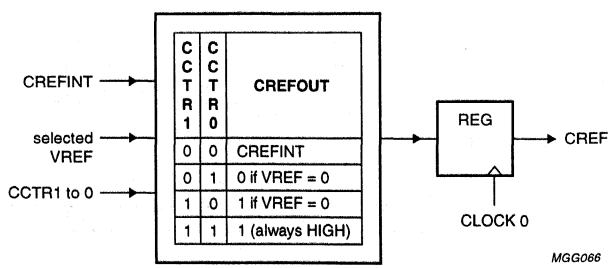
HREFINT = internal horizontal reference.
TBP = upsampled CVBS input data (27 MHz).
AD1BYP/AD2BYP = digitized CVBS input data and Y/C input data (13.5 MHz).
VBP0 = programmable vertical reference signal.
VBP4 = delayed programmable vertical reference signal (4LLC clocks delay).

Fig.6 Multiplexing of the CVBS signal to the VPO-bus.



VREF_CCIR 656 = vertical reference signal referring to the field interval definitions of CCIR656.
HREFINT = internal horizontal reference signal.
VREFINT = internal vertical reference signal.
VBP0 = programmable vertical reference signal.
VBP4 = delayed programmable vertical reference signal (4LLC clocks delay).

Fig.7 VREF output signal generation.



CREFINT = internal clock qualifier signal.

Fig.8 CREF output signal generation.

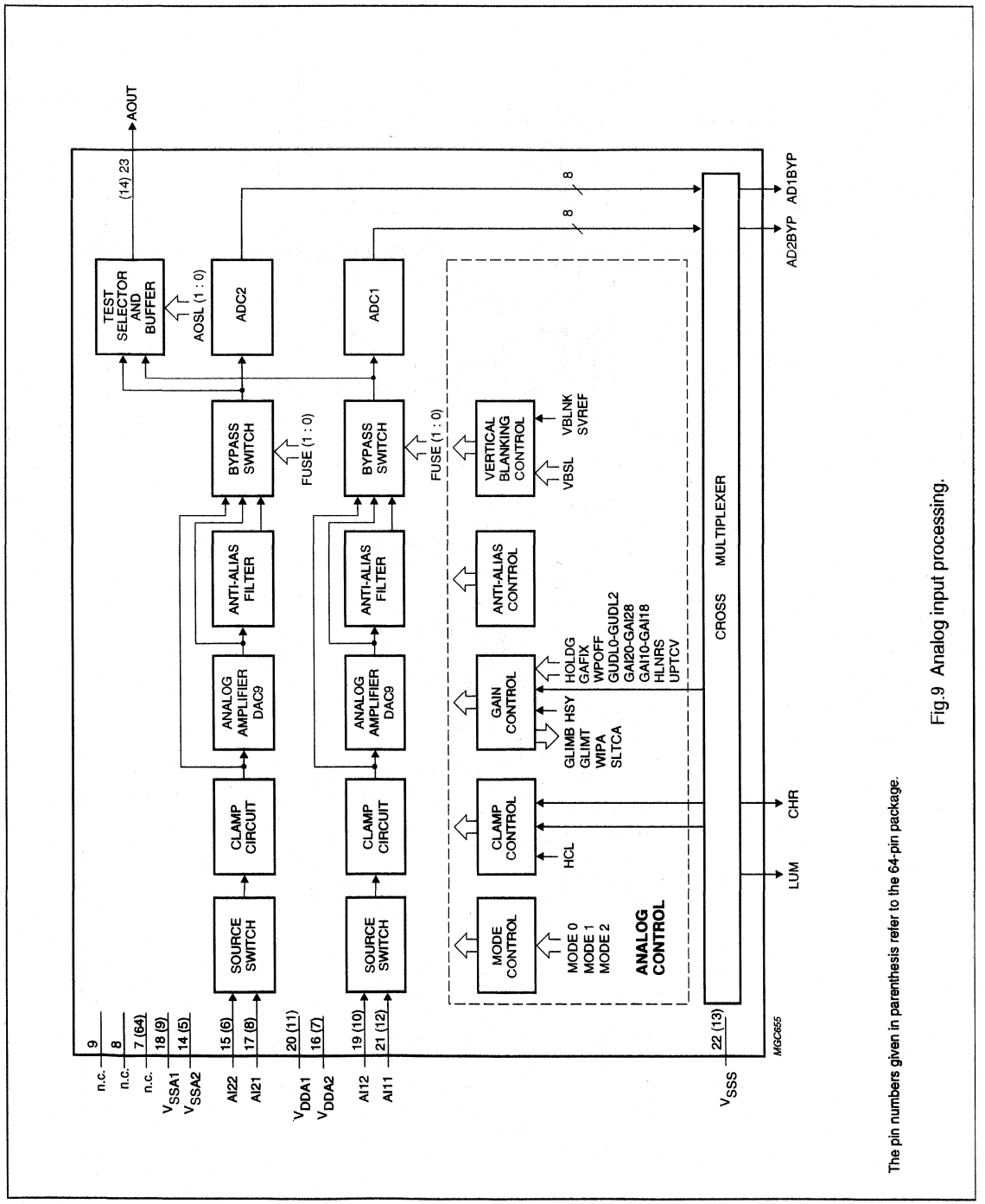


Fig.9 Analog input processing.

The pin numbers given in parenthesis refer to the 64-pin package.

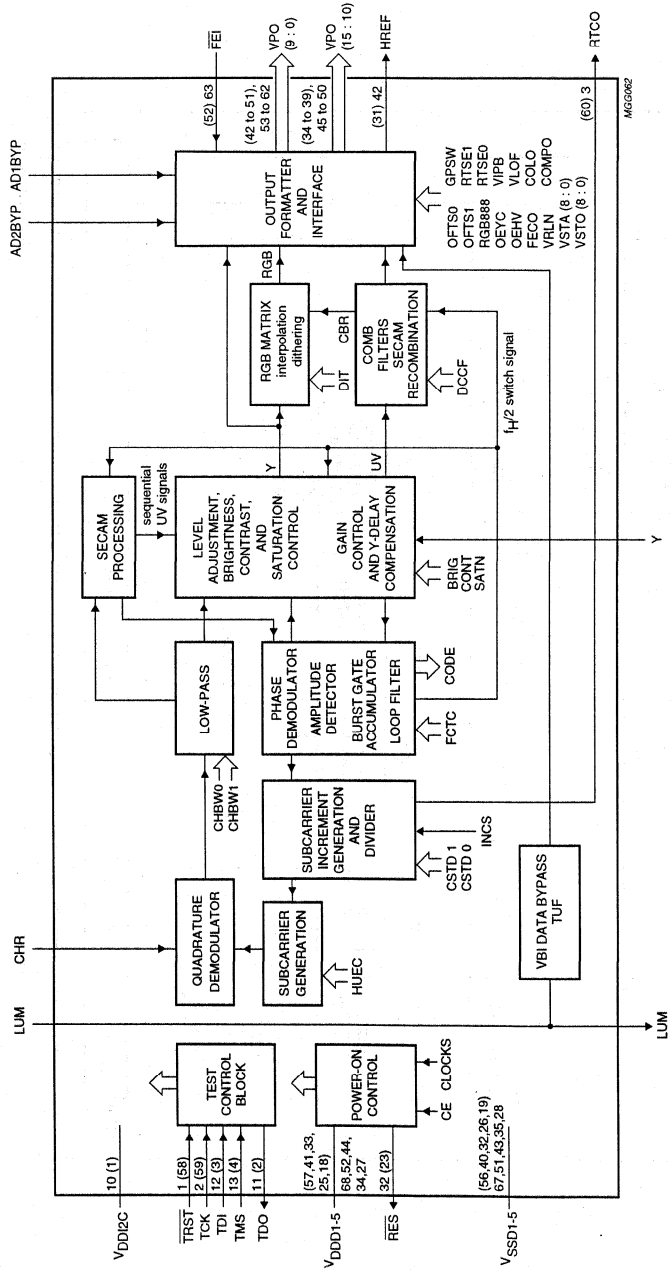


Fig.10 Chrominance circuit.

The pin numbers given in parenthesis refer to the 64-pin package.

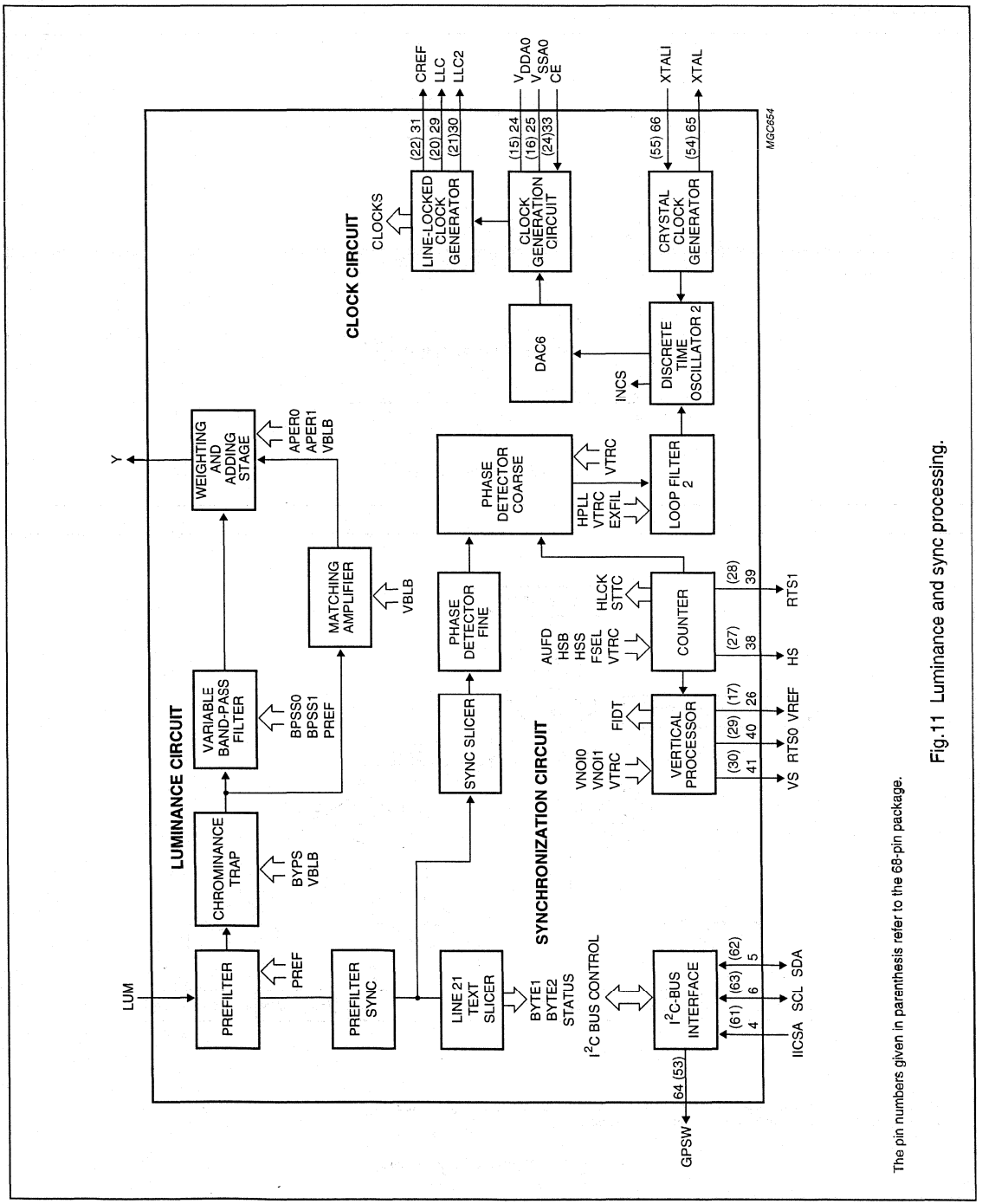


Fig.11 Luminance and sync processing.

The pin numbers given in parenthesis refer to the 68-pin package.

9 GAIN CHARTS

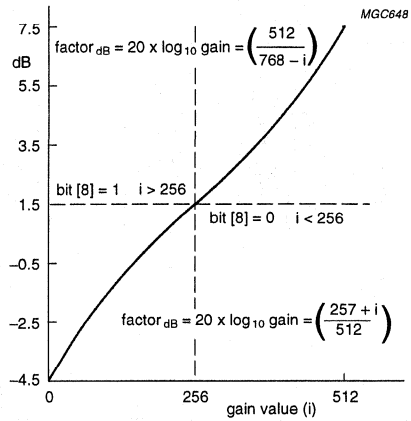
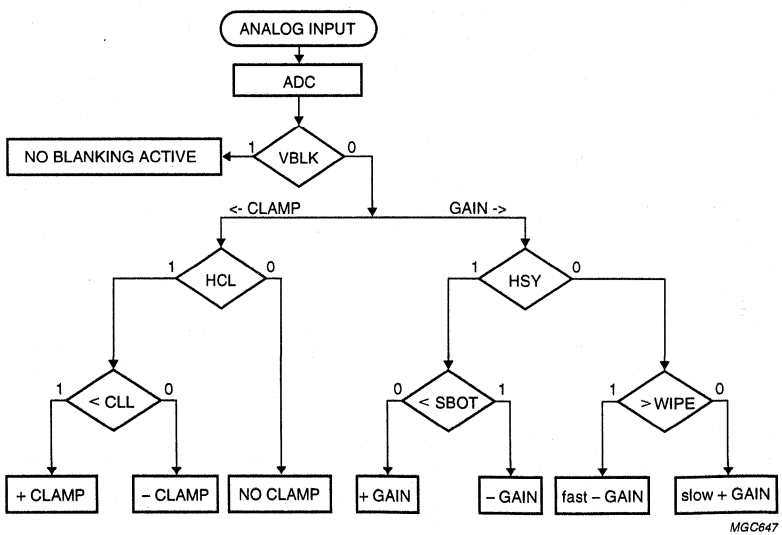
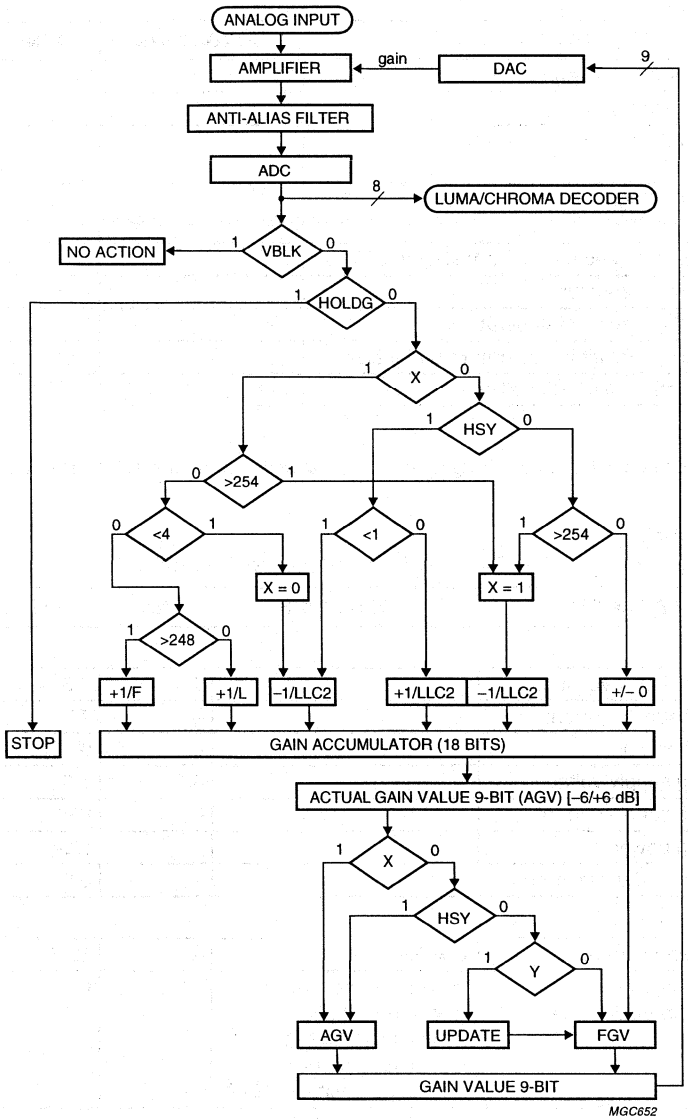


Fig.12 Amplifier curve.



WIPE = white peak level (254); SBOT = sync bottom level (1); CLL = clamp level [60 Y (128 C)];
HSY = horizontal sync pulse; HCL = horizontal clamp pulse.

Fig.13 Clamp and gain flow.



X = system variable; Y = IAGV − FGVI > GUDL; VBLK = vertical blanking pulse; HSY = horizontal sync pulse; AGV = actual gain value; FGV = frozen gain value.

Fig.14 Gain flow chart.

10 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); all ground pins connected together and all supply pins connected together.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDD}	digital supply voltage		−0.5	+4.6	V
V_{DDA}	analog supply voltage		−0.5	+4.6	V
V_i	input voltage		−0.5	V_{DD} + 0.5 (4.6 max)	V
V_o	output voltage		−0.5	V_{DD} + 0.5 (4.6 max)	V
ΔV_{SS}	voltage difference between V_{SSAall} and V_{SSall}		−	100	mV
T_{stg}	storage temperature		−65	+150	°C
T_{amb}	operating ambient temperature		0	70	°C
$T_{amb(bias)}$	operating ambient temperature under bias		−10	+80	°C
V_{esd}	electrostatic discharge all pins	note 1	−2000	+2000	V

Note

1. Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor.

11 CHARACTERISTICS

V_{DDD} = 3.0 to 3.6 V; V_{DDA} = 3.1 to 3.5 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDD}	digital supply voltage		3.0	3.3	3.6	V
I_{DDD}	digital supply current		−	70	75	mA
P_D	digital power		−	0.26	−	W
V_{DDA}	analog supply voltage		3.1	3.3	3.5	V
I_{DDA}	analog supply current		−	69	−	mA
P_A	analog power		−	0.24	−	W
P_{A+D}	analog and digital power		−	0.5	−	W
Analog part						
I_{clamp}	clamping current	V_I = 0.9 V DC	−	±3.5	−	µA
$V_{i(p-p)}$	input voltage (peak-to-peak value)	for normal video levels [1 V (p-p)]; −3 dB termination 27/47 Ω and AC coupling required; coupling capacitor = 22 nF	0.3	0.7	1.2	V
$\|Z_i\|$	input impedance	clamping current off	200	−	−	kΩ
C_i	input capacitance		−	−	10	pF
α_{cs}	channel crosstalk	f_i = 5 MHz	−	−	−50	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog-to-digital converters						
B	bandwidth	at −3 dB	–	15	–	MHz
ϕ_{diff}	differential phase (amplifier plus anti-alias filter = bypass)		–	2	–	deg
G_{diff}	differential gain (amplifier plus anti-alias filter = bypass)		–	2	–	%
f_{clkADC}	ADC clock frequency		12.8	–	14.3	MHz
DLE	DC differential linearity error		–	0.7	–	LSB
ILE	DC integral linearity error		–	1	–	LSB
Digital inputs						
$V_{IL(SCL,SDA)}$	LOW level input voltage pins SDA and SCL		−0.5	–	$+0.3V_{DDD}$	V
V_{IH}	HIGH level input voltage pins SDA and SCL		$0.7V_{DDD}$	–	$V_{DDD} + 0.5$	V
$V_{IL(xtal)}$	LOW level CMOS input voltage pin XTALI		–	–	–	V
$V_{IH(xtal)}$	HIGH level CMOS input voltage pin XTALI		–	–	–	V
V_{ILn}	LOW level input voltage all other inputs		−0.3	–	+0.8	V
V_{IHn}	HIGH level input voltage all other inputs		2.0	–	$V_{DDD} + 0.3$	V
I_{LI}	input leakage current		–	–	1	µA
C_i	input capacitance	inputs and outputs at high-impedance	–	–	8	pF
$C_{i(n)}$	input capacitance all other inputs		–	–	5	pF
Digital outputs						
$V_{OL(SCL,SDA)}$	LOW level output voltage pins SDA and SCL	SDA/SCL at 3 mA (6 mA) sink current	–	–	0.4 (0.6)	V
V_{OL}	LOW level output voltage	V_{DDD} = min, I_{OL} = −2 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	V_{DDD} = min, I_{OL} = −2 mA	$0.85V_{DDD}$	–	–	V
$V_{OL(clk)}$	LOW level output voltage for clocks		−0.5	–	+0.6	V
$V_{OH(clk)}$	HIGH level output voltage for clocks		2.4	–	$V_{DDD} + 0.5$	V
$\overline{FEI}$ input timing						
$t_{SU;DAT}$	input data set-up time		13	–	–	ns
$t_{HD;DAT}$	input data hold time		3	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data and control output timing; note 1						
C_L	output load capacitance		15	–	40	pF
$t_{OHD;DAT}$	output hold time	C_L = 15 pF	4	–	–	ns
t_{PD}	propagation delay	C_L = 25 pF	–	–	20	ns
t_{PDZ}	propagation delay to 3-state		–	–	20	ns
Clock output timing (LLC and LLC2); note 2						
$C_{L(LLC)}$	output load capacitance		15	–	40	pF
T_{cy}	cycle time	LLC	35	–	39	ns
		LLC2	70	–	78	ns
δ_{LLC}	duty factors for t_{LLCH}/t_{LLC} and t_{LLC2H}/t_{LLC2}	C_L = 25 pF	40	–	60	%
t_r	rise time LLC, LLC2		–	–	5	ns
t_f	fall time LLC, LLC2		–	–	5	ns
t_d	delay time LLC output to LLC2 output	at 1.5 V; LLC/LLC2 = 25 pF	−4	–	+8	ns
Data qualifier output timing (CREF)						
$t_{OHD;CREF}$	output hold time	C_L = 15 pF	4	–	–	ns
$t_{PD;CREF}$	propagation delay from positive edge of LLC	C_L = 25 pF	–	–	20	ns
Clock input timing (XTALI)						
δ_{XTALI}	duty factor for t_{XTALIH}/t_{XTALI}	nominal frequency	40	–	60	%
Horizontal PLL						
f_{Hn}	nominal line frequency	50 Hz field	–	15625	–	Hz
		60 Hz field	–	15734	–	Hz
$\Delta f_H/f_{Hn}$	permissible static deviation		–	–	5.7	%
Subcarrier PLL						
f_{SCn}	nominal subcarrier frequency	PAL BGHI	–	4433619	–	Hz
		NTSC M; NTSC-Japan	–	3579545	–	Hz
		PAL M	–	3575612	–	Hz
		PAL N	–	3582056	–	Hz
Δf_{SC}	lock-in range		±400	–	–	Hz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Crystal oscillator						
f_n	nominal frequency	3rd harmonic; note 3	–	24.576	–	MHz
$\Delta f/f_n$	permissible nominal frequency deviation		–	–	±50	10^{-6}
$\Delta Tf/f_n$	permissible nominal frequency deviation with temperature		–	–	±20	10^{-6}
CRYSTAL SPECIFICATION (X1)						
$T_{amb(X1)}$	operating ambient temperature		0	–	70	°C
C_L	load capacitance		8	–	–	pF
R_s	series resonance resistor		–	40	80	Ω
C_1	motional capacitance		–	1.5 ±20%	–	fF
C_0	parallel capacitance		–	3.5 ±20%	–	pF

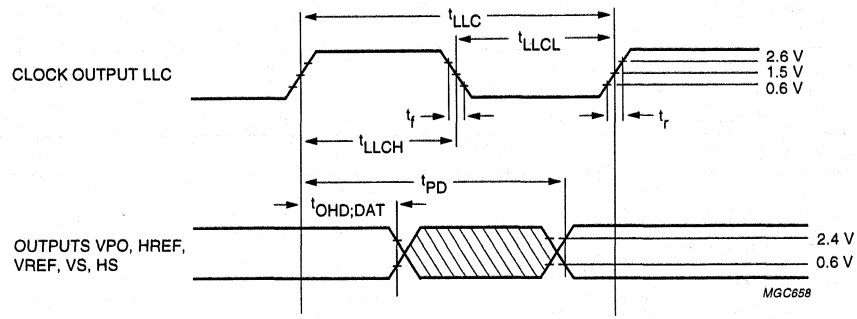
Notes

1. The levels must be measured with load circuits; 1.2 kΩ at 3 V (TTL load); C_L = 50 pF.
2. The effects of rise and fall times are included in the calculation of $t_{OHD;DAT}$, t_{PD} and t_{PDZ}. Timings and levels refer to drawings and conditions illustrated in Figs 15 and 16.
3. Order number: Philips 4322 143 05291.

Table 1 Processing delay

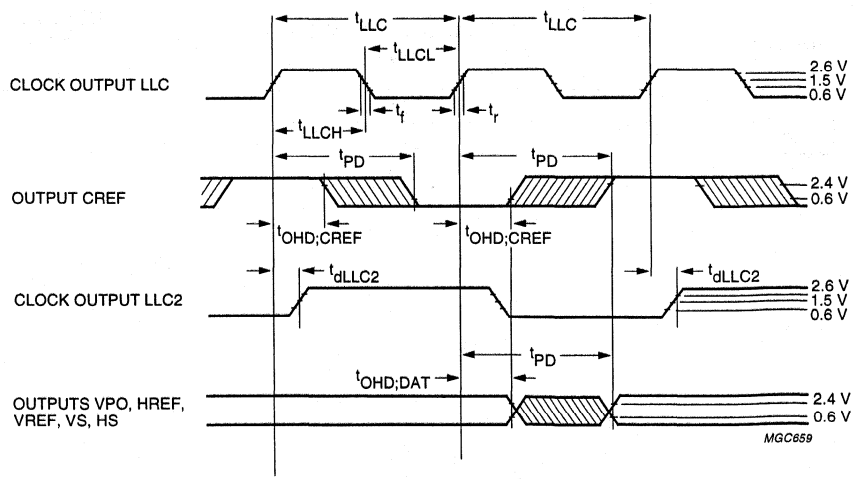
FUNCTION	TYPICAL ANALOG DELAY AI22 –> ADCIN (AOUT) (ns)	DIGITAL DELAY ADCIN –> VPO (LLC CLOCKS) [YDEL(2 to 0) = 000]
Without amplifier or anti-alias filter	15	179
With amplifier, without anti-alias filter	25	
With amplifier and anti-alias filter	75	

12 TIMING DIAGRAMS



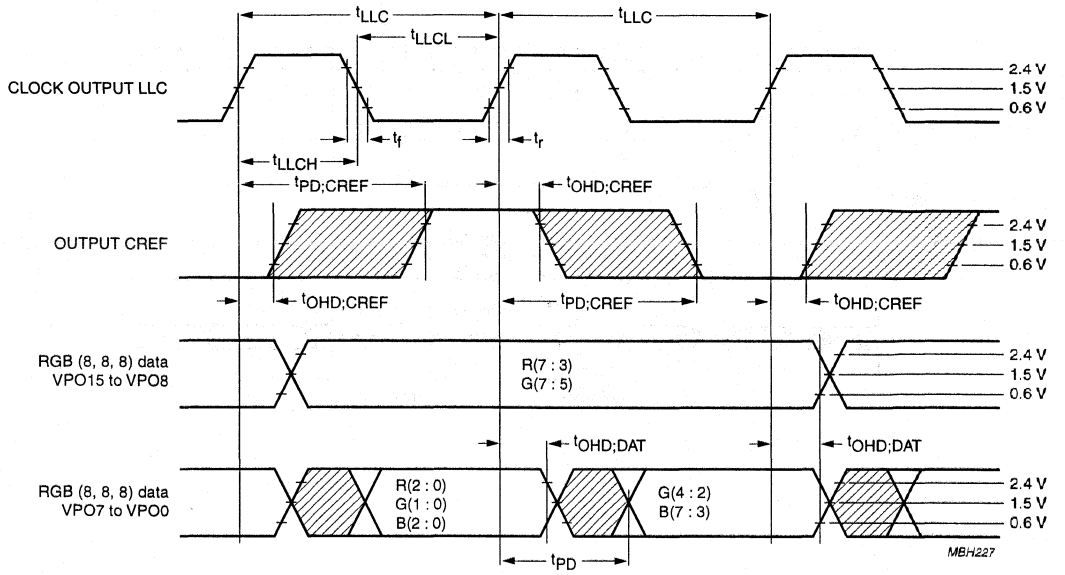
An explanation of the output formats is given in Table 5.

Fig.15 Clock/data timing (8-bit CCIR-656 format of the VPO-bus).



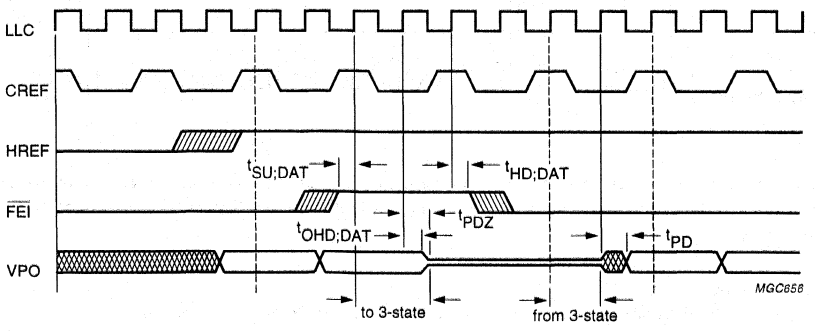
An explanation of the output formats is given in Table 5. The $\overline{FEI}$ timing of the VPO-bus is illustrated in Figs 18 and 19.

Fig.16 Clock/data timing (12 and 16-bit CCIR-601 format of the VPO-bus).



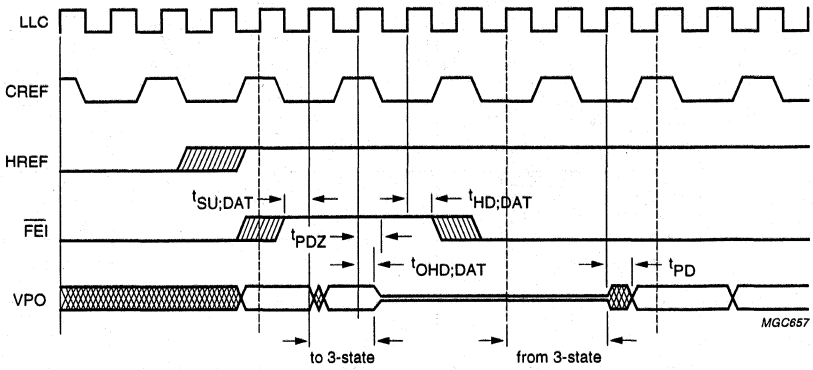
An explanation of the output formats is given in Table 5.

Fig.17 Clock/data timing for RGB (8, 8, 8) output format.



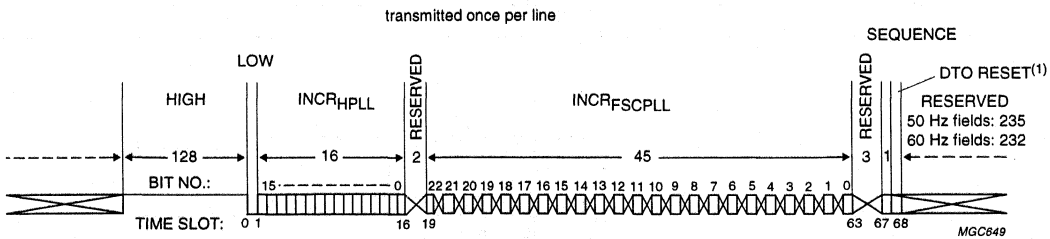
I²C-bus bit FECO = 1.

Fig.18 $\overline{FEI}$ timing diagram ($\overline{FEI}$ sampling at CREF = HIGH) for OFTS = 0, 1 or 2).



Timing is compatible with SAA7110; I²C-bus bit FECO = 0.

Fig.19 $\overline{FEI}$ timing diagram ($\overline{FEI}$ sampling at CREF = LOW) for OFTS = 0, 1 or 2).



(1) Set to zero for one transmission, if a phase reset of the f_{sc} - DTO is applied via I²C-bus bit CDTO. RTCO sequence is generated in LLC/4.

The HPLL increment represents the actual LFCO frequency ($f_{LFCO} \times 4 = f_{LLC}$); 16 LSB from 20, upper four bits are fixed to 0100b

$$f_{LFCO} = \frac{INCR_{HPLL} \times f_{XTAL}}{2^{\text{word length DTO2}}}$$

Where: f_{XTAL} = 24.576 MHz, word length DTO2 = 20 bits.

The f_{sc} increment represents the actual subcarrier frequency (related to the actual clock); 23 LSB from 24, MSB is 0b.

$$f_{sc} = \frac{INCR_{FSCPLL} \times f_{XTAL}}{2^{\text{word length DTO1}}} \times \frac{INCR_{HPLL}}{2^{19}}$$

Where: word length DTO1 = 24 bits.

Fig.20 Real time control output.

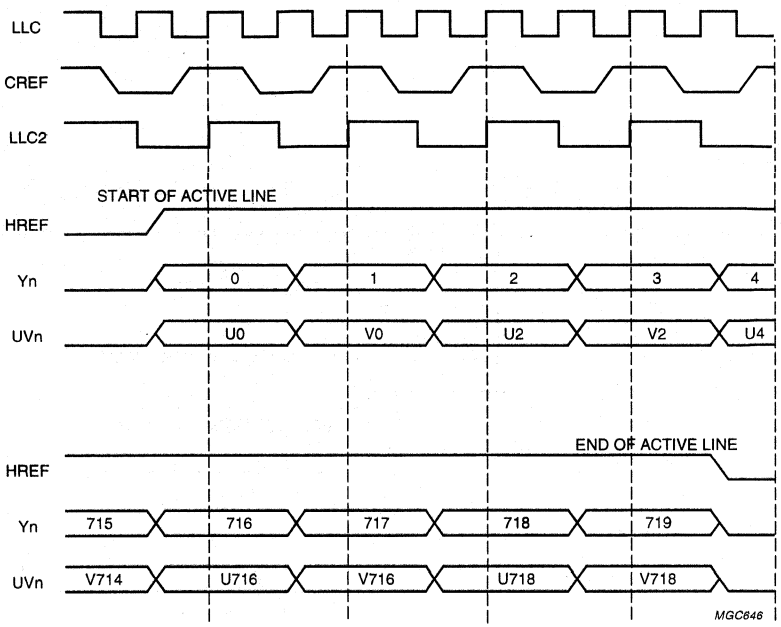


Fig.21 HREF timing diagram.

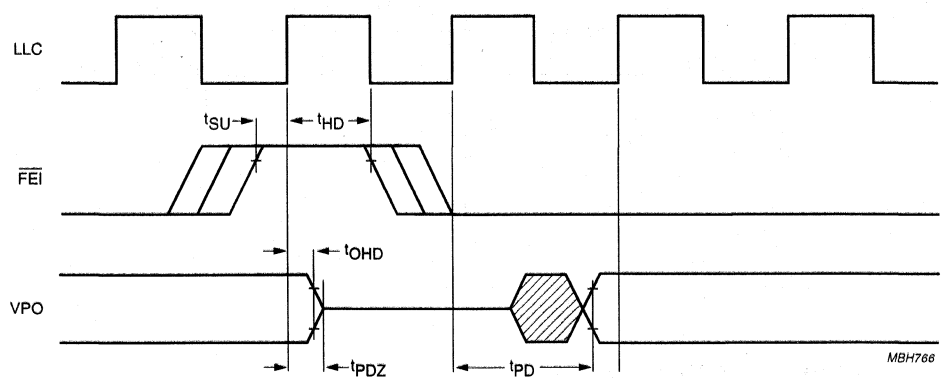
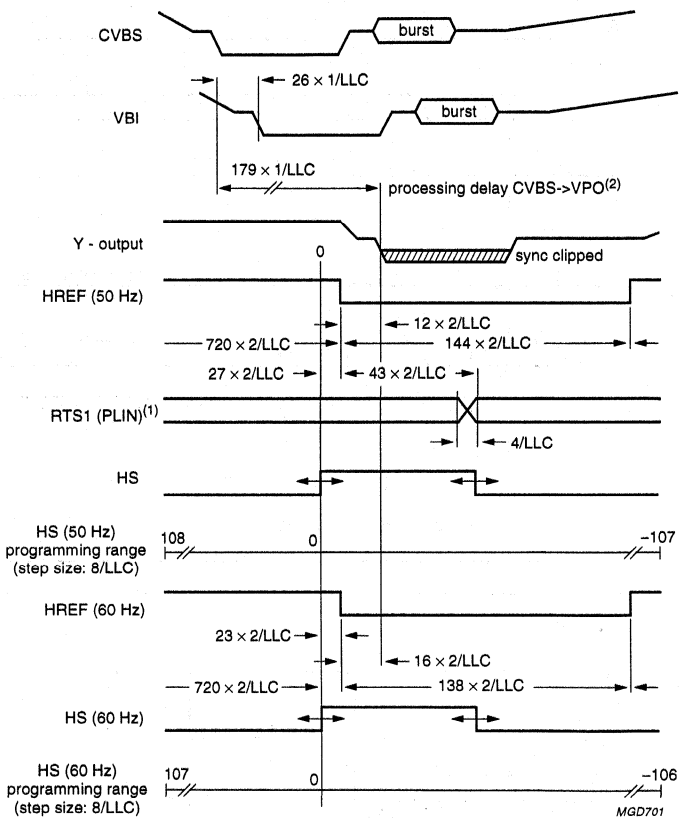
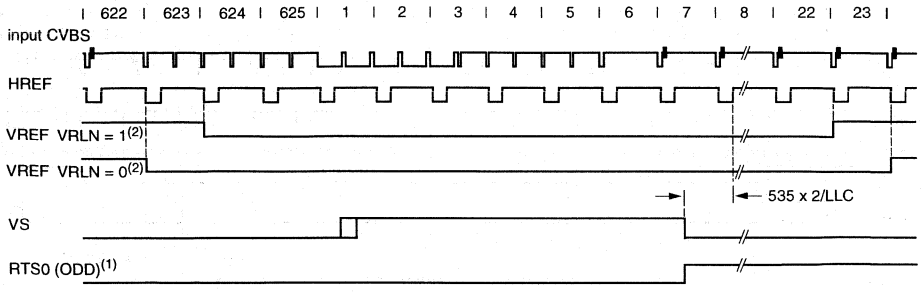


Fig.22 $\overline{FEI}$ timing in CCIR 656 mode [OFTS (1 : 0) = 3].

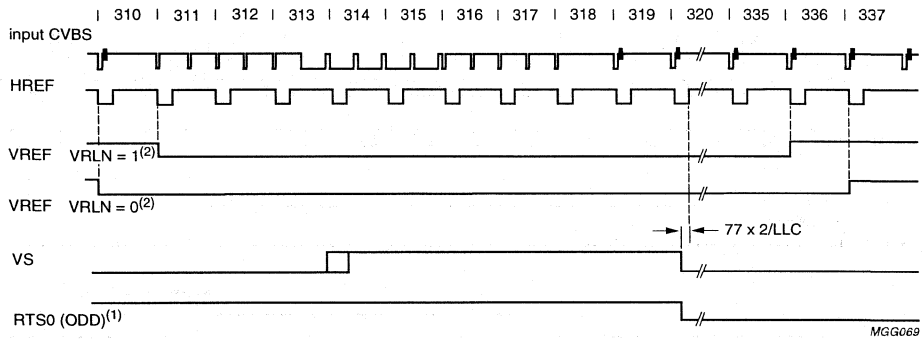


(1) PLIN is switched to output RTS1 via I²C-bus bit RTSE1 = 0.
(2) See Table 1.
(3) HDEL (1 : 0) = 0 0, YDEL (2 : 0) = 0 0 0.

Fig.23 Horizontal timing diagram.



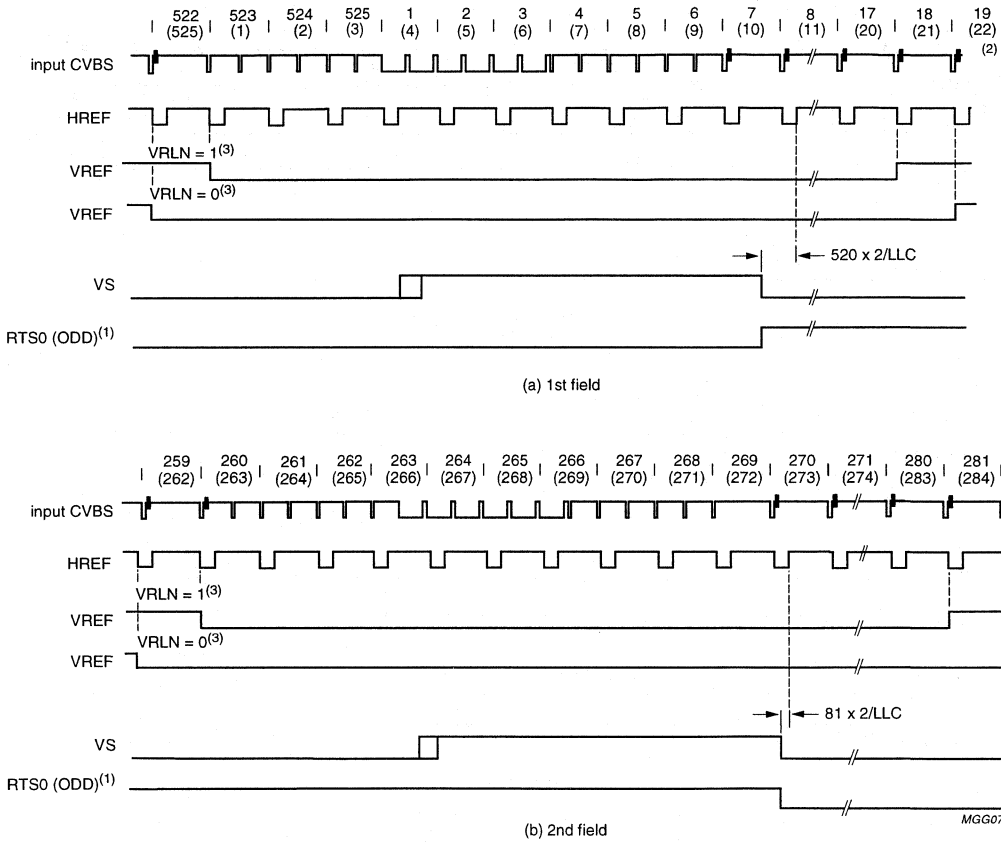
(a) 1st field



(b) 2nd field

(1) ODD is switched to output RTS0 via I²C-bus bit RTSE0 = 0.
(2) Additional VREF positions can be achieved via I²C-bits VCTR1 and VCTR0 (see Fig.7).
The luminance peaking and the chrominance trap are bypassed during VREF = 0 if I²C-bus bit VBLB is set to logic 1.
The chrominance delay line (chrominance-comb filter for NTSC, phase error correcting for PAL) is disabled during VREF = 0.

Fig.24 Vertical timing diagram for 50 Hz [nominal input signal VNL in normal mode (VNOI = 00b)].



(1) ODD is switched to output RTS0 via I²C-bus bit RTSE0 = 0.

(2) Line numbers in parenthesis refer to CCIR line counting.

(3) Additional VREF positions can be achieved via I²C-bus bits VCTR1 and VCTR0 (see Fig.7).

The luminance peaking and the chrominance trap are bypassed during VREF = 0 if I²C-bus bit VBLB is set to logic 1.

The chrominance delay line (chrominance-comb filter for NTSC, phase error correcting for PAL) is disabled during VREF = 0.

Fig.25 Vertical timing diagram for 60 Hz [nominal input signal VNL in normal mode (VNOI = 00b)].

Table 2 Digital output control

OEYC	$\overline{FEI}$	VPO
		15 to 0
0	0	Z
1	0	active
0	1	Z
1	1	Z

Table 3 Clock frequencies

CLOCK	FREQUENCY (MHz)
XTAL	24.576
LLC	27
LLC2	13.5
LLC4	6.75
LLC8	3.375

13 CLOCK SYSTEM

13.1 Clock generation circuit

The internal CGC generates the system clocks LLC, LLC2 and the clock reference signal CREF. The internally generated LFCO (triangular waveform) is multiplied by 2 or 4 via the analog PLL (including phase detector, loop filter, VCO and frequency divider). The rectangular output signals have a 50% duty factor.

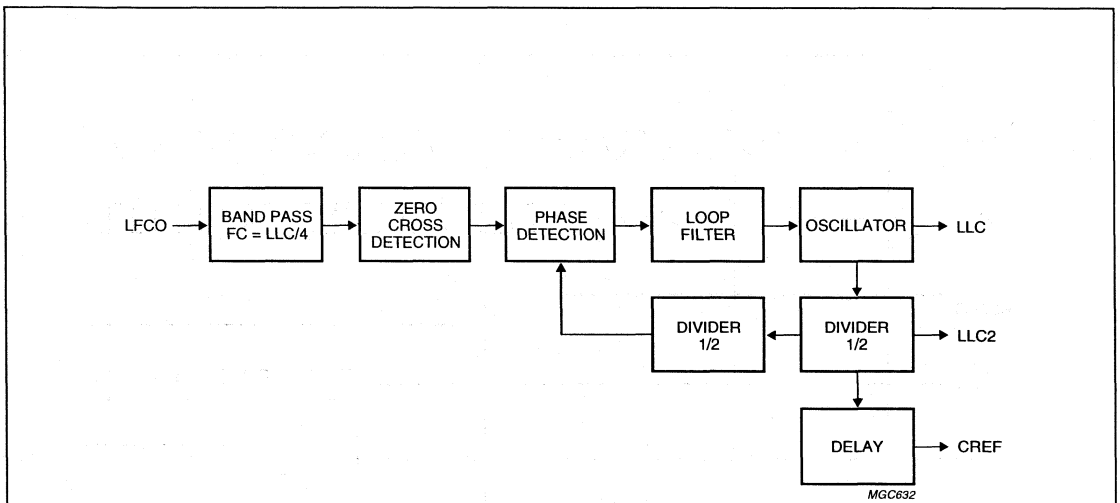
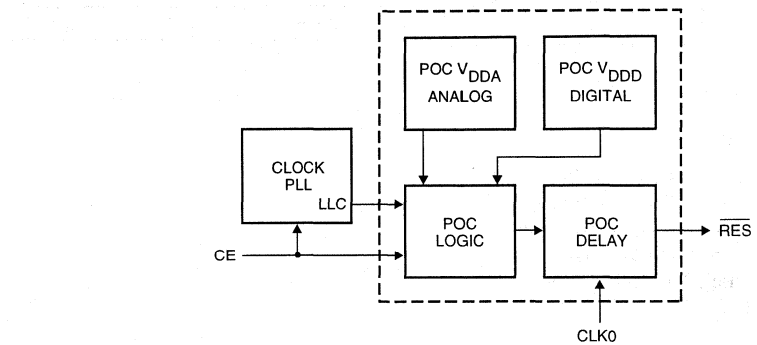
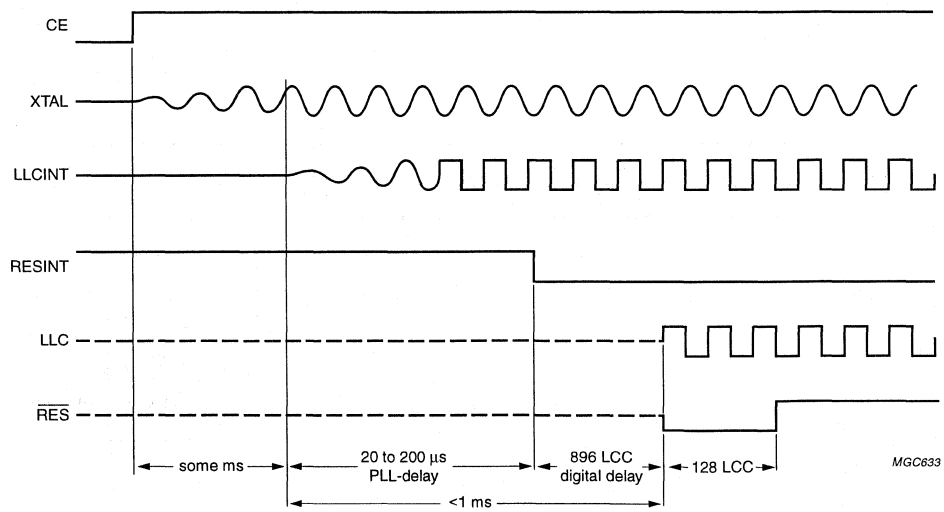


Fig.26 Block diagram of clock generation circuit.

13.2 Power-on control

Power-on reset is activated at power-on, chip enable, PLL clock generation failure and if the supply voltage falls below 2.7 V. The $\overline{RES}$ signal can be applied to reset other circuits of the digital picture processing system.





CE = chip enable input; XTAL = crystal oscillator output; LLCINT = internal system clock; RESINT = internal reset; LLC = line-locked clock output; $\overline{RES}$ = reset output (active LOW).

Fig.27 Power-on control circuit.

Table 4 Power-on control sequence

INTERNAL POWER-ON CONTROL SEQUENCE	PIN OUTPUT STATUS	FUNCTION
Directly after power-on asynchronous reset	VPO15 to VPO0, RTCO, RTS0, RTS1, GPSW, HREF, VREF, HS, VS, LLC, LLC2 and CREF are in high-impedance state	direct switching to high impedance for 20 to 200 ms
Synchronous reset sequence	LLC, LLC2, CREF, RTCO, RTS0, RTS1, GPSW and SDA become active; VPO15 to VPO0, HREF, VREF, HS and VS are held in high-impedance state	internal reset sequence
Status after power-on control sequence	VPO15 to VPO0, HREF, VREF, HS and VS are held in high-impedance state	after power-on (reset sequence) a complete I²C-bus transmission is required

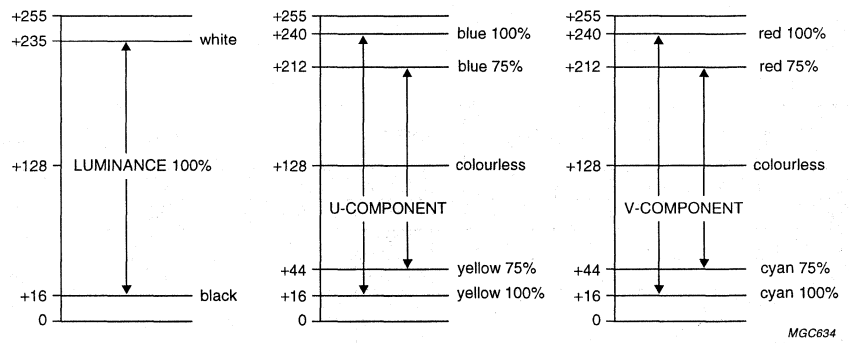
14 OUTPUT FORMATS

Table 5 Output formats

BUS SIGNAL	411 (12-BIT)				422 (16-BIT)(1)		CCIR-656 (8-BIT)(2)				RGB (16-BIT)(3)	RGB (24-BIT)(3)	
VPO15	Y_{07}	Y_{17}	Y_{27}	Y_{37}	Y_{07}	Y_{17}	U_{07}	Y_{07}	V_{07}	Y_{17}	R4	R7	R7
VPO14	Y_{06}	Y_{16}	Y_{26}	Y_{36}	Y_{06}	Y_{16}	U_{06}	Y_{06}	V_{06}	Y_{16}	R3	R6	R6
VPO13	Y_{05}	Y_{15}	Y_{25}	Y_{35}	Y_{05}	Y_{15}	U_{05}	Y_{05}	V_{05}	Y_{15}	R2	R5	R5
VPO12	Y_{04}	Y_{14}	Y_{24}	Y_{34}	Y_{04}	Y_{14}	U_{04}	Y_{04}	V_{04}	Y_{14}	R1	R4	R4
VPO11	Y_{03}	Y_{13}	Y_{23}	Y_{33}	Y_{03}	Y_{13}	U_{03}	Y_{03}	V_{03}	Y_{13}	R0	R3	R3
VPO10	Y_{02}	Y_{12}	Y_{22}	Y_{32}	Y_{02}	Y_{12}	U_{02}	Y_{02}	V_{02}	Y_{12}	G5	G7	G7
VPO9	Y_{01}	Y_{11}	Y_{21}	Y_{31}	Y_{01}	Y_{11}	U_{01}	Y_{01}	V_{01}	Y_{11}	G4	G6	G6
VPO8	Y_{00}	Y_{10}	Y_{20}	Y_{30}	Y_{00}	Y_{10}	U_{00}	Y_{00}	V_{00}	Y_{10}	G3	G5	G5
VPO7	U_{07}	U_{05}	U_{03}	U_{01}	U_{07}	V_{07}	X	X	X	X	G2	G4	R2
VPO6	U_{06}	U_{04}	U_{02}	U_{00}	U_{06}	V_{06}	X	X	X	X	G1	G3	R1
VPO5	V_{07}	V_{05}	V_{03}	V_{01}	U_{05}	V_{05}	X	X	X	X	G0	G2	R0
VPO4	V_{06}	V_{04}	V_{02}	V_{00}	U_{04}	V_{04}	X	X	X	X	B4	B7	G1
VPO3	X	X	X	X	U_{03}	V_{03}	X	X	X	X	B3	B6	G0
VPO2	X	X	X	X	U_{02}	V_{02}	X	X	X	X	B2	B5	B2
VPO1	X	X	X	X	U_{01}	V_{01}	X	X	X	X	B1	B4	B1
VPO0	X	X	X	X	U_{00}	V_{00}	X	X	X	X	B0	B3	B0
Pixel order Y	0	1	2	3	0	1	0		1		–	note 5	note 4
Pixel order UV	0				0		0				–	–	
Data rates	LLC2				LLC2		LLC				LLC2	–	
I²C-bus control signals	OFTS0 = 0				OFTS0 = 1		OFTS0 = 1				OFTS0 = 0	OFTS0 = 0	
	OFTS1 = 1				OFTS1 = 0		OFTS1 = 1				OFTS1 = 0	OFTS1 = 0	
	RGB888 = X				RGB888 = X		RGB888 = X				RGB888 = 0	RGB888 = 1	

Notes to Table 5

1. Values in accordance with CCIR 601.
2. Before and after the video data, video timing codes are inserted in accordance with CCIR 656.
   a) VPO15 to VPO8 = VPO7 to VPO0 = CCIR 656 data if I²C-bus bit TCLO = 0
   b) VPO15 to VPO8 = CCIR 656 data, VPO7 to VPO0 = 3-state if I²C-bus bit TCLO = 1.
3. During HREF = LOW RGB levels are set to 16 (10 hex). RGB 16-bit is achieved by dropping the LSBs of the 8-bit signals (after dithering if desired).
4. CREF = 1 (see Fig.17).
5. CREF = 0 (see Fig.17).



(a) Y output range. (b) U output range (Cb). (c) V output range (Cr).

CCIR Rec. 602 digital levels.

Equations for modification to the YUV levels via BCS control I²C-bus bytes BRIG, CONT and SATN.

Luminance:

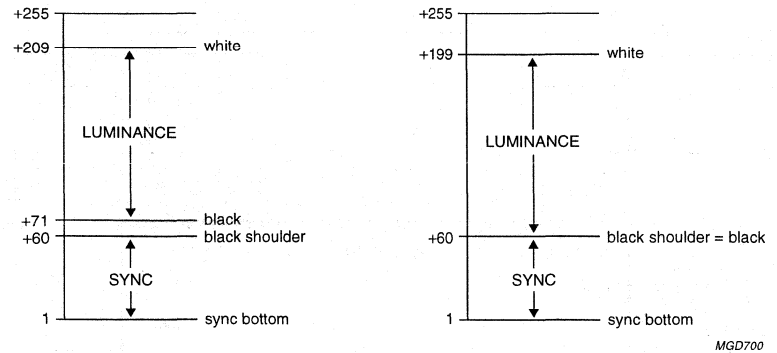
$$Y_{OUT} = Int\left[\frac{CONT}{71} \times (Y - 128)\right] + BRIG$$

Chrominance:

$$UV_{OUT} = Int\left[\frac{SATN}{64} \times (Cr, Cb - 128)\right] + 128$$

It should be noted that the resulting levels are limited to 1 to 254 in accordance with CCIR-601/656 standard.

Fig.28 VPO output signal range with default BCS settings.

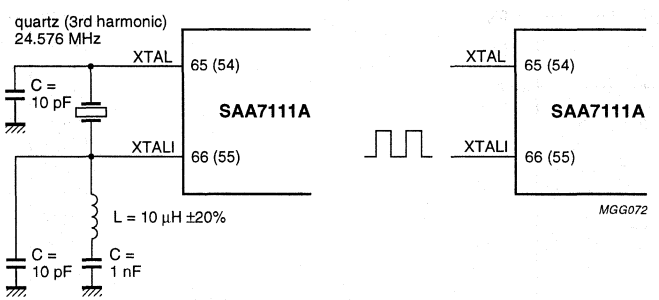


(a) For sources containing 7.5 IRE black level offset (e.g. NTSC–M).

(b) For sources not containing black level offset.

VBI data levels are **not** dependent on BCS settings.

Fig.29 VBI data bypass output range.



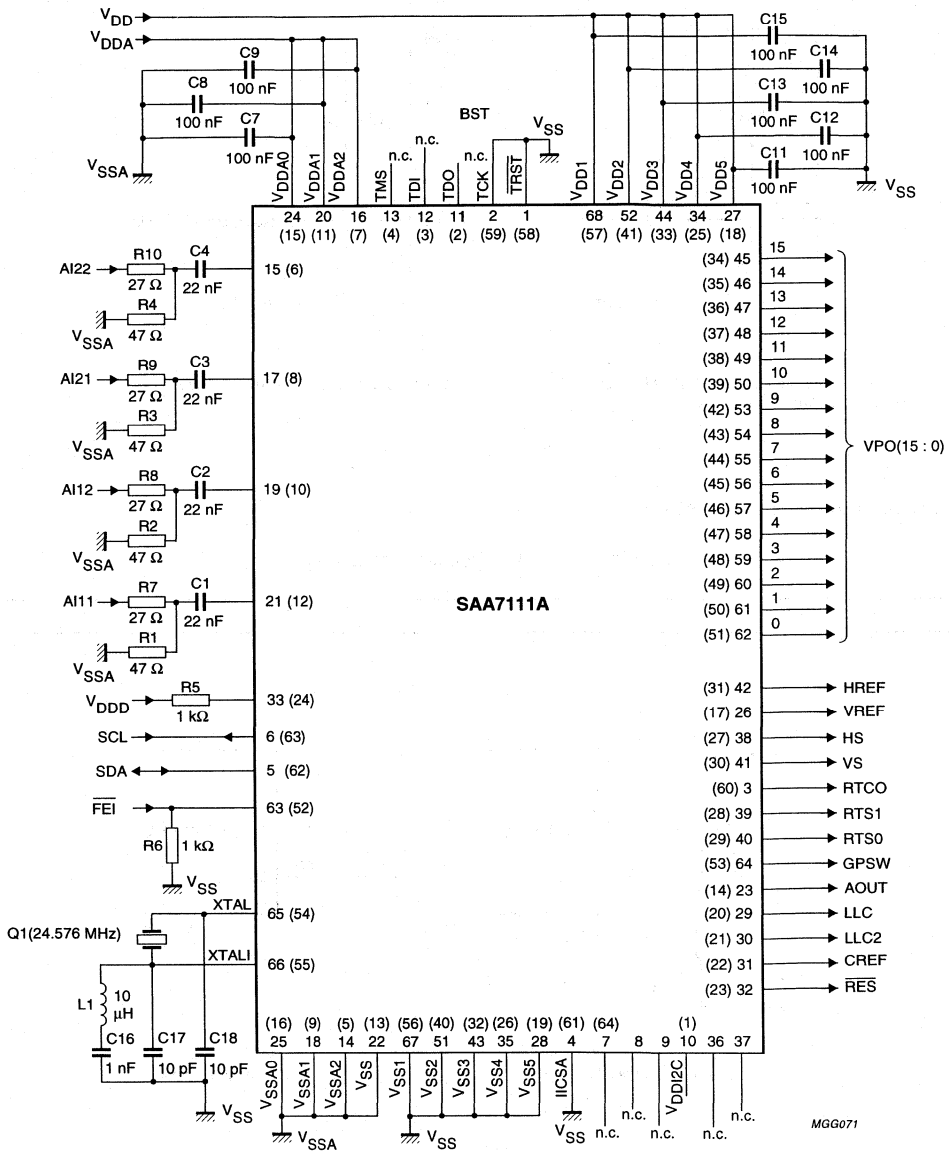
(a) With quartz crystal.

(b) With external clock.

The pin numbers given in parenthesis refer to the 64-pin package.
Order number: Philips 4322 143 05291.

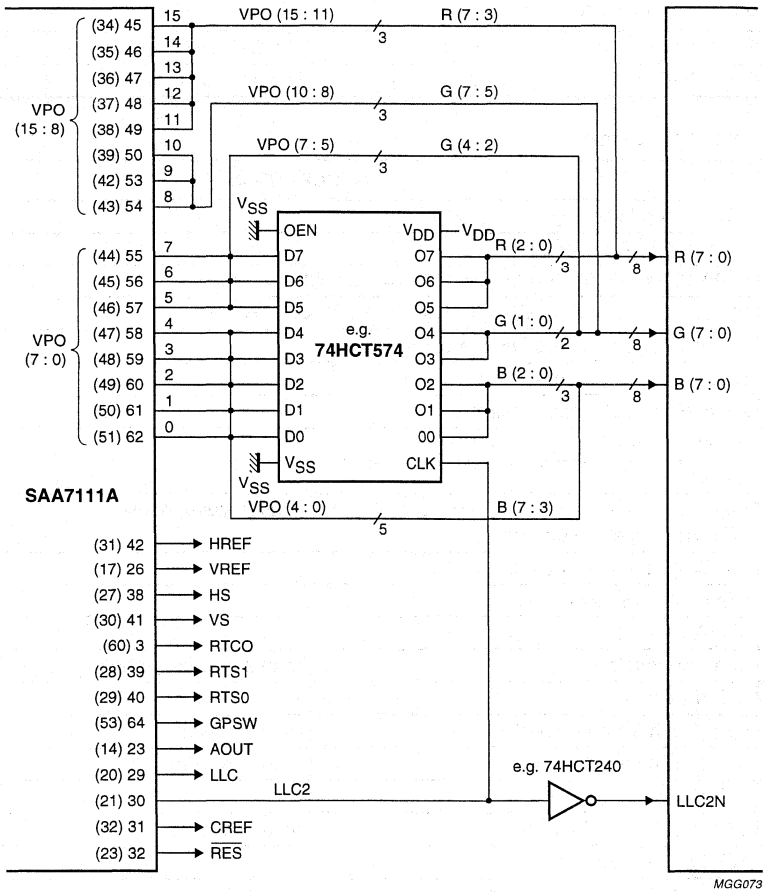
Fig.30 Oscillator application.

15 APPLICATION INFORMATION



The pin numbers given in parenthesis refer to the 64-pin package.

Fig.31 Application diagram.



The pin numbers given in parenthesis refer to the QFP64 package.
I²C-bus control bits:
OFTS(1 : 0) = 00 (subaddress 10H, bits D7 and D6).
RGB888 = 1 (subaddress 12H, bit D3).

Fig.32 Application diagram for RGB 24-bit output format.

16 I²C-BUS DESCRIPTION

16.1 I²C-bus format

Table 6 Write procedure

S	SLAVE ADDRESS W	ACK s	SUBADDRESS	ACK s	DATA (N BYTES)	ACK s	P

Table 7 Read procedure (combined format)

S	SLAVE ADDRESS W	ACK s	SUBADDRESS	ACK s	
Sr	SLAVE ADDRESS R	ACK s	DATA (N BYTES)	ACK m	P

Table 8 Description of I²C-bus format

CODE	DESCRIPTION	
S	START condition	
Sr	repeated START condition	
Slave address W	0100 1000b (IICSA = LOW) or 0100 1010b (IICSA = HIGH)	
Slave address R	0100 1001b (IICSA = LOW) or 0100 1011b (IICSA = HIGH)	
ACK s	acknowledge generated by the slave	
ACK m	acknowledge generated by the master	
Subaddress	subaddress byte, see Table 9	
Data	data byte, see Table 9; note 1	
P	STOP condition	
X = LSB slave address	read/write control bit; X = 0, order to write (the circuit is slave receiver); X = 1, order to read (the circuit is slave transmitter)	
Slave address	read = 49h or 4Bh; note 2	
	write = 48h or 4Ah	
	IICSA = 0 or 1	
Subaddresses	00h chip version	read and write; note 3
	01h reserved	–
	02h to 05h front-end part	read and write
	06h to 13h decoder part	read and write
	14h reserved	–
	15h to 17h decoder part	read and write
	18h to 19h reserved	–
	1Ah to 1Ch Line-21 text slicer part	read only
	1Dh to 1Eh reserved	–
	1Fh status byte	read only

Notes

1. If more than one byte DATA is transmitted then the auto-increment of the subaddress is performed.
2. During slave transmitter mode the SCL-LOW period may be extended by pulling SCL to LOW (in accordance with the I²C-bus specification).
3. The I²C-bus subaddress 00 has to be initialized with 0 before being read.

Table 9 I²C-bus receiver/transmitter overview

SLAVE ADDRESS		READ		WRITE		IICSA			
		49H 4BH		48H 4AH		0 1			
REGISTER FUNCTION	**SUB-ADDR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Chip version	00	ID07	ID06	ID05	ID04	ID03	ID02	ID01	ID00
Reserved	01	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)
Analog input contr 1	02	FUSE1	FUSE0	GUDL2	GUDL1	GUDL0	MODE2	MODE1	MODE0
Analog input contr 2	03	(1)	HLNRS	VBSL	WPOFF	HOLDG	GAFIX	GAI28	GAI18
Analog input contr 3	04	GAI17	GAI16	GAI15	GAI14	GAI13	GAI12	GAI11	GAI10
Analog input contr 4	05	GAI27	GAI26	GAI25	GAI24	GAI23	GAI22	GAI21	GAI20
Horizontal sync start	06	HSB7	HSB6	HSB5	HSB4	HSB3	HSB2	HSB1	HSB0
Horizontal sync stop	07	HSS7	HSS6	HSS5	HSS4	HSS3	HSS2	HSS1	HSS0
Sync control	08	AUFD	FSEL	EXFIL	(1)	VTRC	HPLL	VNOI1	VNOI0
Luminance control	09	BYPS	PREF	BPSS1	BPSS0	VBLB	UPTCV	APER1	APER0
Luminance brightness	0A	BRIG7	BRIG6	BRIG5	BRIG4	BRIG3	BRIG2	BRIG1	BRIG0
Luminance contrast	0B	CONT7	CONT6	CONT5	CONT4	CONT3	CONT2	CONT1	CONT0
Chroma saturation	0C	SATN7	SATN6	SATN5	SATN4	SATN3	SATN2	SATN1	SATN0
Chroma Hue control	0D	HUEC7	HUEC6	HUEC5	HUEC4	HUEC3	HUEC2	HUEC1	HUEC0
Chroma control	0E	CDTO	CSTD2	CSTD1	CSTD0	DCCF	FCTC	CHBW1	CHBW0
Reserved	0F	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)
Format/delay control	10	OFTS1	OFTS0	HDEL1	HDEL0	VRLN	YDEL2	YDEL1	YDEL0
Output control 1	11	GPSW	CM99	FECO	COMPO	OEYC	OEHV	VIPB	COLO
Output control 2	12	RTSE1	RTSE0	TCLO	CBR	RGB888	DIT	AOSL1	AOSL0
Output control 3	13	VCTR1	VCTR0	CCTR1	CCTR0	BCHI1	BCHI0	BCLO1	BCLO0
Reserved	14	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)
V_GATE1_START	15	VSTA7	VSTA6	VSTA5	VSTA4	VSTA3	VSTA2	VSTA1	VSTA0
V_GATE1_STOP	16	VSTO7	VSTO6	VSTO5	VSTO4	VSTO3	VSTO2	VSTO1	VSTO0
V_GATE1_MSB	17	(1)	(1)	(1)	(1)	(1)	(1)	VSTO8	VSTA8
Reserved	18-19	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)
Text slicer status	1A	(1)	(1)	(1)	(1)	F2VAL	F2RDY	F1VAL	F1RDY
Decoded bytes of the text slicer	1B	P1	BYTE16	BYTE15	BYTE14	BYTE13	BYTE12	BYTE11	BYTE10
	1C	P2	BYTE26	BYTE25	BYTE24	BYTE23	BYTE22	BYTE21	BYTE20
Reserved	1D-1E	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)
Status byte	1F	STTC	HLCK	FIDT	GLIMT	GLIMB	WIPA	SLTCA	CODE

Note

1. All unused control bits must be programmed with logic 0.

16.2 I²C-bus detail

The I²C-bus receiver slave address is 48H/49H. Subaddresses 0F, 14, 18, 19, 1D and 1E are reserved; subaddress 01 is reserved for chip version.

16.2.1 SUBADDRESS 00

Table 10 Chip version SA00

FUNCTION		LOGIC LEVELS							
		ID07	ID06	ID05	ID04	ID03	ID02	ID01	ID00
Chip version	V1	0	0	0	1	X	X	X	X
	V2	0	0	1	0	X	X	X	X

Note

1. X = reserved.

16.2.2 SUBADDRESS 02

Table 11 Analog control 1 SA02

FUNCTION[1]	CONTROL BITS D2 TO D0		
	MODE 2	MODE 1	MODE 0
Mode 0: CVBS (automatic gain)	0	0	0
Mode 1: CVBS (automatic gain)	0	0	1
Mode 2: CVBS (automatic gain)	0	1	0
Mode 3: CVBS (automatic gain)	0	1	1
Mode 4: Y (automatic gain) + C (gain channel 2 fixed to GAI2 level)	1	0	0
Mode 5: Y (automatic gain) + C (gain channel 2 fixed to GAI2 level)	1	0	1
Mode 6: Y (automatic gain) + C (gain channel 2 adapted to Y gain)	1	1	0
Mode 7: Y (automatic gain) + C (gain channel 2 adapted to Y gain)	1	1	1

Note

1. Mode select (see Figures 33 to 40).

Table 12 Analog control 1 SA 02, D5 to D3 (see Fig.14)

DECIMAL VALUE	UPDATE HYSTERESIS FOR 9-BIT GAIN	CONTROL BITS D5 TO D3		
		GUDL 2	GUDL 1	GUDL 0
0....	off	0	0	0
....7	±7 LSB	1	1	1

Table 13 Analog control

ANALOG FUNCTION SELECT FUSE	CONTROL BITS D7 AND D6	
	FUSE 1	FUSE 0
Amplifier plus anti-alias filter bypassed	0	0
	0	1
Amplifier active	1	0
Amplifier plus anti-alias filter active	1	1

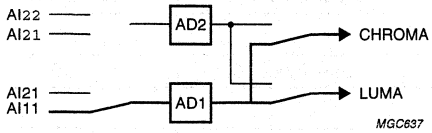


Fig.33 Mode 0; CVBS (automatic gain).

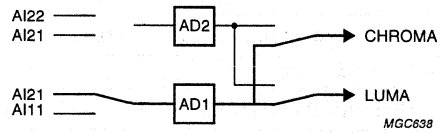


Fig.34 Mode 1; CVBS (automatic gain).

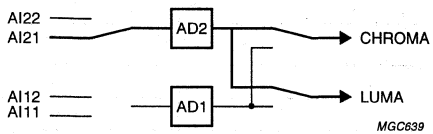


Fig.35 Mode 2; CVBS (automatic gain).

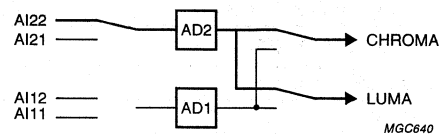


Fig.36 Mode 3; CVBS (automatic gain).

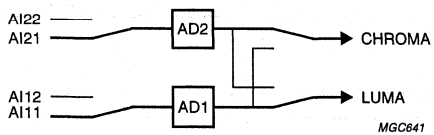


Fig.37 Mode 4 Y (automatic gain) + C
(gain channel 2 fixed to GAI2 level).

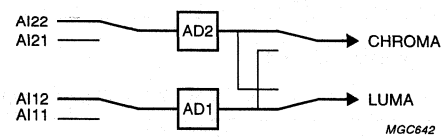


Fig.38 Mode 5 Y (automatic gain) + C
(gain channel 2 fixed to GAI2 level).

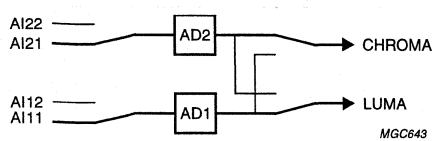


Fig.39 Mode 6 Y (automatic gain) + C
(gain channel 2 adapted to Y gain).

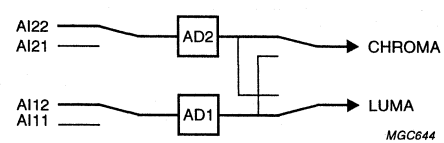


Fig.40 Mode 7 Y (automatic gain) + C
(gain channel 2 adapted to Y gain).

16.2.3 SUBADDRESS 03

Table 14 Analog control 2 (AICO2) SA03

FUNCTION	LOGIC LEVEL	DATA BIT
Static gain control channel 1 (GAI18) (see SA04)		
Sign bit of gain control	see Table 15	D0
Static gain control channel 2 (GAI28) (see SA05)		
Sign bit of gain control	see Table 16	D1
Gain control fix (GAFIX)		
Automatic gain controlled by MODE 1 and MODE 0	0	D2
Gain control is user programmable via GAI1 + GAI2	1	D2
Automatic gain control integration (HOLDG)		
AGC active	0	D3
AGC integration hold (freeze)	1	D3
White peak off (WPOFF)		
White peak control active	0	D4
White peak off	1	D4
Vertical blanking select (VBSL)		
Long vertical blanking	0	D5
Short vertical blanking	1	D5
HL not reference select (HLNRS)		
Normal clamping by HL not	0	D6
Reference select by HL not	1	D6

16.2.4 SUBADDRESS 04

Table 15 Gain control analog (AIC03); static gain control channel 1 GAI1 SA 04, D7 to D0

DECIMAL VALUE	GAIN (dB)	SIGN BIT	CONTROL BITS D7 TO D0							
		GAI18	GAI17	GAI16	GAI15	GAI14	GAI13	GAI12	GAI11	GAI10
0....	–5.98	0	0	0	0	0	0	0	0	0
....255	0	0	1	1	1	1	1	1	1	1
256....	0	1	0	0	0	0	0	0	0	0
....511	5.98	1	1	1	1	1	1	1	1	1

16.2.5 SUBADDRESS 05

Table 16 Gain control analog (AIC04); static gain control channel 2 GAI2 SA 05, D7 to D0

DECIMAL VALUE	GAIN (dB)	SIGN BIT (SA 03, D1)	CONTROL BITS D7 to D0							
		GAI28	GAI27	GAI26	GAI25	GAI24	GAI23	GAI22	GAI21	GAI20
0....	–5.98	0	0	0	0	0	0	0	0	0
....255	0	0	1	1	1	1	1	1	1	1
256....	0	1	0	0	0	0	0	0	0	0
....511	5.98	1	1	1	1	1	1	1	1	1

16.2.6 SUBADDRESS 06

Table 17 Horizontal sync begin SA 06, D7 to D0

DELAY TIME (STEP SIZE = 8/LLC)	CONTROL BITS D7 to D0							
	HSB7	HSB6	HSB5	HSB4	HSB3	HSB2	HSB1	HSB0
–128...–108	forbidden (outside available central counter range)							
–107...	1	0	0	1	0	1	0	1
...108	0	1	1	0	1	1	0	0
109...127	forbidden (outside available central counter range)							

16.2.7 SUBADDRESS 07

Table 18 Horizontal sync stop SA 07, D7 to D0

DELAY TIME (STEP SIZE = 8/LLC)	CONTROL BITS D7 to D0							
	HSS7	HSS6	HSS5	HSS4	HSS3	HSS2	HSS1	HSS0
–128...–108	forbidden (outside available central counter range)							
–107...	1	0	0	1	0	1	0	1
...108	0	1	1	0	1	1	0	0
109...127	forbidden (outside available central counter range)							

16.2.8 SUBADDRESS 08

Table 19 Sync control SA 08, D7 to D5, D3 to D0

FUNCTION	VNOI BITS	LOGIC LEVELS	DATA BITS
Vertical noise reduction (VNOI)			
Normal mode	VNOI1	0	D1
	VNOI0	0	D0
Searching mode	VNOI1	0	D1
	VNOI0	1	D0
Free running mode	VNOI1	1	D1
	VNOI0	0	D0
Vertical noise reduction bypassed	VNOI1	1	D1
	VNOI0	1	D0
Horizontal PLL (HPLL)			
PLL closed	HPLL	0	D2
PLL open, horizontal frequency fixed	HPLL	1	D2
TV/VTR mode select (VTRC)			
TV mode (recommended for poor quality TV signals only)	VTRC	0	D3
VTR mode (recommended as default setting)	VTRC	1	D3
Extended loop filter (EXFIL)			
Word width of the loop filter (LF2) amplification = 16-bit	EXFIL	0	D5
Word width of the loop filter (LF2) amplification = 14-bit	EXFIL	1	D5
Field selection (FSEL)			
50 Hz, 625 lines	FSEL	0	D6
60 Hz, 525 lines	FSEL	1	D6
Automatic field detection (AUFD)			
Field state directly controlled via FSEL	AUFD	0	D7
Automatic field detection	AUFD	1	D7

16.2.9 SUBADDRESS 09

Table 20 Luminance control SA 09, D7 to D0

FUNCTION	APER/BPSS BITS	LOGIC LEVELS	DATA BITS
Aperture factor (APER)			
Aperture factor = 0	APER1	0	D1
	APER0	0	D0
Aperture factor = 0.25	APER1	0	D1
	APER0	1	D0
Aperture factor = 0.5	APER1	1	D1
	APER0	0	D0
Aperture factor = 1.0	APER1	1	D1
	APER0	1	D0
Update time interval for AGC value (UPTCV)			
Horizontal update (once per line)	UPTCV	0	D2
Vertical update (once per field)	UPTCV	1	D2
Vertical blanking luminance bypass (VBLB)			
Active luminance processing	VBLB	0	D3
Luminance bypass during vertical blanking	VBLB	1	D3
Aperture band pass (centre frequency) (BPSS)			
Centre frequency = 4.1 MHz	BPSS1	0	D5
	BPSS0	0	D4
Centre frequency = 3.8 MHz; note 1	BPSS1	0	D5
	BPSS0	1	D4
Centre frequency = 2.6 MHz; note 1	BPSS1	1	D5
	BPSS0	0	D4
Centre frequency = 2.9 MHz; note 1	BPSS1	1	D5
	BPSS0	1	D4
Prefilter active (PREF)			
Bypassed	PREF	0	D6
Active	PREF	1	D6
Chrominance trap bypass (BYPS)			
Chrominance trap active; default for CVBS mode	BYPS	0	D7
Chrominance trap bypassed; default for S-Video mode	BYPS	1	D7

Note

1. Not to be used with bypassed chrominance trap.

16.2.10 SUBADDRESS 0A

Table 21 Luminance brightness control BRIG7 to BRIG0 SA 0A

OFFSET	CONTROL BITS D7 to D0							
	BRIG7	BRIG6	BRIG5	BRIG4	BRIG3	BRIG2	BRIG1	BRIG0
255 (bright)	1	1	1	1	1	1	1	1
128 (CCIR level)	1	0	0	0	0	0	0	0
0 (dark)	0	0	0	0	0	0	0	0

16.2.11 SUBADDRESS 0B

Table 22 Luminance contrast control CONT7 to CONT0 SA 0B

GAIN	CONTROL BITS D7 to D0							
	CONT7	CONT6	CONT5	CONT4	CONT3	CONT2	CONT1	CONT0
1.999 (maximum)	0	1	1	1	1	1	1	1
1.109 (CCIR level)	0	1	0	0	0	1	1	1
1.0	0	1	0	0	0	0	0	0
0 (luminance off)	0	0	0	0	0	0	0	0
–1 (inverse luminance)	1	1	0	0	0	0	0	0
–2 (inverse luminance)	1	0	0	0	0	0	0	0

16.2.12 SUBADDRESS 0C

Table 23 Chrominance saturation control SATN7 to SATN0 SA 0C

GAIN	CONTROL BITS D7 to D0							
	SATN7	SATN6	SATN5	SATN4	SATN3	SATN2	SATN1	SATN0
1.999 (maximum)	0	1	1	1	1	1	1	1
1.0 (CCIR level)	0	1	0	0	0	0	0	0
0 (colour off)	0	0	0	0	0	0	0	0
–1 (inverse chrominance)	1	1	0	0	0	0	0	0
–2 (inverse chrominance)	1	0	0	0	0	0	0	0

16.2.13 SUBADDRESS 0D

Table 24 Chrominance hue control HUEC7 to HUEC0 SA 0D

HUE PHASE (DEG)	CONTROL BITS D7 to D0							
	HUEC7	HUEC6	HUEC5	HUEC4	HUEC3	HUEC2	HUEC1	HUEC0
+178.6....	0	1	1	1	1	1	1	1
....0....	0	0	0	0	0	0	0	0
....–180	1	0	0	0	0	0	0	0

16.2.14 SUBADDRESS 0E

Table 25 Chrominance control SA 0E

FUNCTION	CHBW/CSTD BITS	LOGIC LEVELS	DATA BITS
Chroma bandwidth (CHBW0 and CHBW1)			
Small bandwidth (≈ 620 kHz)	CHBW1	0	D1
	CHBW0	0	D0
Nominal bandwidth (≈ 800 kHz)	CHBW1	0	D1
	CHBW0	1	D0
Medium bandwidth (≈ 920 kHz)	CHBW1	1	D1
	CHBW0	0	D0
Wide bandwidth (≈ 1000 kHz)	CHBW1	1	D1
	CHBW0	1	D0
Fast colour time constant (FCTC)			
Nominal time constant	FCTC	0	D2
Fast time constant	FCTC	1	D2
Disable chrominance comb filter (DCCF)			
Chrominance comb filter on (during VREF = 1) (see Figs 24 and 25)	DCCF	0	D3
Chrominance comb filter off	DCCF	1	D3
Colour standard (CSTD0 to CSTD2); logic levels 100, 110 and 111 are reserved, do not use			
Colour standard control automatic switching between PAL BGHI and NTSC M (NTSC-Japan with special level adjustment; luminance brightness subaddress 0A = 95H, luminance contrast subaddress 0BH = 48H)	CSTD2	0	D6
	CSTD1	0	D5
	CSTD0	0	D4
Colour standard control automatic switching between NTSC 4.43 (50 Hz) and PAL 4.43 (60 Hz)	CSTD2	0	D6
	CSTD1	0	D5
	CSTD0	1	D4
Colour standard control automatic switching between PAL N and NTSC 4.43 (60 Hz)	CSTD2	0	D6
	CSTD1	1	D5
	CSTD0	0	D4
Colour standard control automatic switching between NTSC N and PAL M	CSTD2	0	D6
	CSTD1	1	D5
	CSTD0	1	D4
Colour standard control automatic switching between SECAM and PAL 4.43 (60 Hz)	CSTD2	1	D6
	CSTD1	0	D5
	CSTD0	1	D4
Clear DTO (CDTO)			
Disabled	CDTO	0	D7
Every time CDTO is set, the internal subcarrier DTO phase is reset to 0° and the RTCO output generates a logic 0 at time slot 68 (see RTCO description Fig.20). So an identical subcarrier phase can be generated by an external device (e.g. an encoder).	CDTO	1	D7

16.2.15 SUBADDRESS 10

Table 26 Format/delay control SA 10

LUMINANCE DELAY COMPENSATION (STEPS IN 2/LLC)	CONTROL BITS D2 to D0		
	YDEL2	YDEL1	YDEL0
–4...	1	0	0
...0...	0	0	0
...3	0	1	1

Table 27 VREF pulse position and length VRLN SA 10 (D3)

VRLN	VREF at 60 Hz 525 LINES(2)				VREF at 50 Hz 625 LINES(2)			
	0		1		0		1	
Length	240		242		286		288	
Line number	first	last	first	last	first	last	first	last
Field 1(1)	19 (22)	258 (261)	18 (21)	259 (262)	24	309	23	310
Field 2(1)	282 (285)	521 (524)	281 (284)	522 (525)	337	622	336	623

Notes

1. The numbers given in parenthesis refer to CCIR line counting.
2. Additional VREF positions can be achieved via I²C-bus bits VCTR1 and VCTR0 (see Fig.7).

Table 28 Fine position of HS HDEL0 and HDEL1 SA 10

FINE POSITION OF HS WITH A STEP SIZE OF 2/LLC	CONTROL BITS D5 and D4	
	HDEL1	HDEL0
0	0	0
1	0	1
2	1	0
3	1	1

Table 29 Output format selection OFTS0 and OFTS1 SA 10

FORMATS	CONTROL BITS D7 and D6	
	OFTS1	OFTS0
RGB (5, 6, 5), RGB (8, 8, 8) (dependent on control bit RGB888) see Table 31	0	0
YUV 422 16 bits	0	1
YUV 411 12 bits	1	0
YUV CCIR-656 8 bits	1	1

16.2.16 SUBADDRESS 11

Table 30 Output control 1 SA 11

FUNCTION	BITS	LOGIC LEVELS	DATA BIT
Colour on (COLO)			
Automatic colour killer	COLO	0	D0
Colour forced on	COLO	1	D0
Decoder VIP bypassed (VIPB)			
DMSD data to YUV output	VIPB	0	D1
ADC data to YUV output; dependent on mode settings	VIPB	1	D1
Output enable horizontal/vertical sync (OEHV)			
HS, HREF, VREF and VS high-impedance inputs	OEHV	0	D2
Outputs HS, HREF, VREF and VS active	OEHV	1	D2
Output enable YUV data (OEYC)			
VPO-bus high-impedance inputs	OEYC	0	D3
Output VPO-bus active	OEYC	1	D3
Inverse composite blank (COMPO)			
VREF is vertical reference	COMPO	0	D4
VREF is inverse composite blank	COMPO	1	D4
$\overline{\text{FEI}}$ control (FECO)			
$\overline{\text{FEI}}$ sampling at CREF = LOW (SAA7110 compatible; (see Fig.19)	FECO	0	D5
$\overline{\text{FEI}}$ sampling at CREF = HIGH	FECO	1	D5
CM99 compatibility to SAA7199 (CM99)			
Default value	CM99	0	D6
To be set if SAA7199 (digital encoder) is used for re-encoding in conjunction with RTCO	CM99	1	D6
General purpose switch (GPSW)			
Switches directly pin 64 GPSW	GPSW	0	D7
	GPSW	1	D7

16.2.17 SUBADDRESS 12

Table 31 Output control 2 SA 12, D7 to D6, D4 to D0

FUNCTION	AOSL BITS	LOGIC LEVELS	DATA BITS
Analog test select (AOSL)			
AOUT connected to internal test point 1	AOSL1	0	D1
	AOSL0	0	D0
AOUT connected to input AD1	AOSL1	0	D1
	AOSL0	1	D0
AOUT connected to input AD2	AOSL1	1	D1
	AOSL0	0	D0
AOUT connected to internal test point 2	AOSL1	1	D1
	AOSL0	1	D0
Dithering (noise shaping) control (DIT)			
Dithering off	DIT	0	D2
Dithering on	DIT	1	D2
RGB output format selection (RGB888)			
RGB (5, 6, 5)	RGB888	0	D3
RGB (8, 8, 8)	RGB888	1	D3
Chrominance interpolation filter function (CBR)			
Cubic interpolation (default)	CBR	0	D4
Linear interpolation (lower bandwidth)	CBR	1	D4
3-state control VPO7 to VPO0 (TCLO)			
VPO7 to VPO0 depends on OEYC, $\overline{\text{FEI}}$ only (default)	TCLO	0	D5
VPO7 to VPO0 in 3-state [and OFTS (1 : 0) = 3]	TCLO	1	D5
Real time outputs mode select (RTSE0)			
ODD switched to output pin 40	RTSE0	0	D6
VL switched to output pin 40	RTSE0	1	D6
Real time outputs mode select (RTSE1)			
PLIN switched to output pin 39	RTSE1	0	D7
HL switched to output pin 39	RTSE1	1	D7

16.2.18 SUBADDRESS 13

Table 32 Output control 3 SA 13

FUNCTION	BITS	LOGIC LEVELS	DATA BITS
Bypass control LOW for VPO7 to VPO0			
No bypass	BCLO1	0	D1
	BCLO0	0	D0
Permanent bypass	BCLO1	0	D1
	BCLO0	1	D0
Bypass controlled by V_GATE	BCLO1	1	D1
	BCLO0	0	D0
Bypass controlled by delayed V_GATE	BCLO1	1	D1
	BCLO0	1	D0
Bypass control HIGH for VPO15 to VPO8			
No bypass	BCHI1	0	D3
	BCHI0	0	D2
Permanent bypass	BCHI1	0	D3
	BCHI0	1	D2
Bypass controlled by V_GATE	BCHI1	1	D3
	BCHI0	0	D2
Bypass controlled by delayed V_GATE	BCHI1	1	D3
	BCHI0	1	D2
Clock Reference Output Control			
CREF is independent of VREF	CCTR1	0	D5
	CCTR0	0	D4
CREF is LOW if VREF = 0	CCTR1	0	D5
	CCTR0	1	D4
CREF is HIGH if VREF = 0	CCTR1	1	D5
	CCTR0	0	D4
CREF always = 1	CCTR1	1	D5
	CCTR0	1	D4
Vertical Reference Output Control (VREF)			
Internal VREF	VCTR1	0	D7
	VCTR0	0	D6
VREF_CCIR	VCTR1	0	D7
	VCTR0	1	D6
Programmable V_GATE	VCTR1	1	D7
	VCTR0	0	D6
Delayed programmable V_GATE	VCTR1	1	D7
	VCTR0	1	D6

16.2.19 SUBADDRESS 15

Table 33 Start of decoded data on VPO-port SA 15; note 1

FIELD		Frame line[2] counting	Decimal value	MSB (SA 17, D0)	CONTROL BITS D7 to D0							
				VSTA8	VSTA 7	VSTA 6	VSTA 5	VSTA 4	VSTA 3	VSTA 2	VSTA 1	VSTA 0
50 Hz	1st	1	312	1	0	0	1	1	1	0	0	0
	2nd	314										
	1st	2	0....	0	0	0	0	0	0	0	0	0
	2nd	315										
	1st	312	310	1	0	0	1	1	0	1	1	1
	2nd	625										
60 Hz	1st	1 (4)	262	1	0	0	0	0	0	1	1	0
	2nd	264 (267)										
	1st	2 (5)	0....	0	0	0	0	0	0	0	0	0
	2nd	265 (268)										
	1st	262 (265)	260	1	0	0	0	0	0	1	0	1
	2nd	525 (3)										

Notes

1. Start of decoded data on VPO-port (end of bypassed region; start of VREF if selected by VCTR1 and VCTR0).
2. Line numbers in brackets refer to CCIR line counting.

16.2.20 SUBADDRESS 16

Table 34 Start of decoded data on VPO-port SA 16; note 1

FIELD		Frame line[2] counting	Decimal value	MSB (SA 17, D0)	CONTROL BITS D7 to D0							
				VSTO8	VSTO 7	VSTO 6	VSTO 5	VSTO 4	VSTO 3	VSTO 2	VSTO 1	VSTO 0
50 Hz	1st	1	312	1	0	0	1	1	1	0	0	0
	2nd	314										
	1st	2	0....	0	0	0	0	0	0	0	0	0
	2nd	315										
	1st	312	310	1	0	0	1	1	0	1	1	1
	2nd	625										
60 Hz	1st	1 (4)	262	1	0	0	0	0	0	1	1	0
	2nd	264 (267)										
	1st	2 (5)	0....	0	0	0	0	0	0	0	0	0
	2nd	265 (268)										
	1st	262 (265)	260	1	0	0	0	0	0	1	0	1
	2nd	525 (3)										

Notes

1. Start of decoded data on VPO-port (begin of bypassed region; stop of VREF if selected by VCTR1 and VCTR0).
2. Line numbers in brackets refer to CCIR line counting.

16.2.21 SUBADDRESS 17

Table 35 Sign bits of the VBI-data stream control

FUNCTION	LOGIC LEVELS	CONTROL BITS
VBI-data stream start (VSTA8); see SA 15		
Sign bit VBI-data stream start	see Table 33	D0
VBI-data stream stop (VSTA8); see SA 16		
Sign bit VBI-data stream stop	see Table 34	D1

16.2.22 Subaddress 1A (read-only register)

Table 36 Line-21 text slicer status SA 1A, D3 to D0

I²C-BUS CONTROL BITS	FUNCTION	DATA BIT
F1RDY	new data on field 1 has been acquired (for asynchronous reading); active HIGH	D0
F1VAL	Line-21 of field 1 carries valid data; active HIGH	D1
F2RDY	new data on field 2 has been acquired (for asynchronous reading); active HIGH	D2
F2VAL	Line-21 of field 2 carries valid data; active HIGH	D3

16.2.23 Subaddress 1B (read-only register)

Table 37 First decoded data byte of the text slicer SA 1B

I²C-BUS CONTROL BITS	FUNCTION	DATA BIT
BYTE1 (6 to 0)	data bit 6 to 0 of first data byte	D6 to D0
P1	parity error flag bit; bit goes HIGH when a parity error has occurred	D7

16.2.24 Subaddress 1C (read-only register)

Table 38 Second decoded data byte of the text slicer SA 1C

I²C-BUS CONTROL BITS	FUNCTION	DATA BIT
BYTE2 (6 to 0)	data bit 6 to 0 of second data byte	D6 to D0
P2	parity error flag bit; bit goes HIGH when a parity error has occurred	D7

16.2.25 Subaddress 1F (read-only register)

Table 39 Status byte SA 1F

I²C-BUS CONTROL BITS	FUNCTION	DATA BIT
CODE	colour signal in accordance with selected standard has been detected; active HIGH	D0
SLTCA	slow time constant active in WIPA-mode; active HIGH	D1
WIPA	white peak loop is activated; active HIGH	D2
GLIMB	gain value for active luminance channel is limited [min (bottom)]; active HIGH	D3
GLIMT	gain value for active luminance channel is limited [max (top)]; active HIGH	D4
FIDT	identification bit for detected field frequency; LOW = 50 Hz, HIGH = 60 Hz	D5
HLCK	status bit for locked horizontal frequency; LOW = locked, HIGH = unlocked	D6
STTC	status bit for horizontal phase loop; LOW = TV time-constant, HIGH = VTR time-constant	D7

17 FILTER CURVES

17.1 Anti-alias filter curve

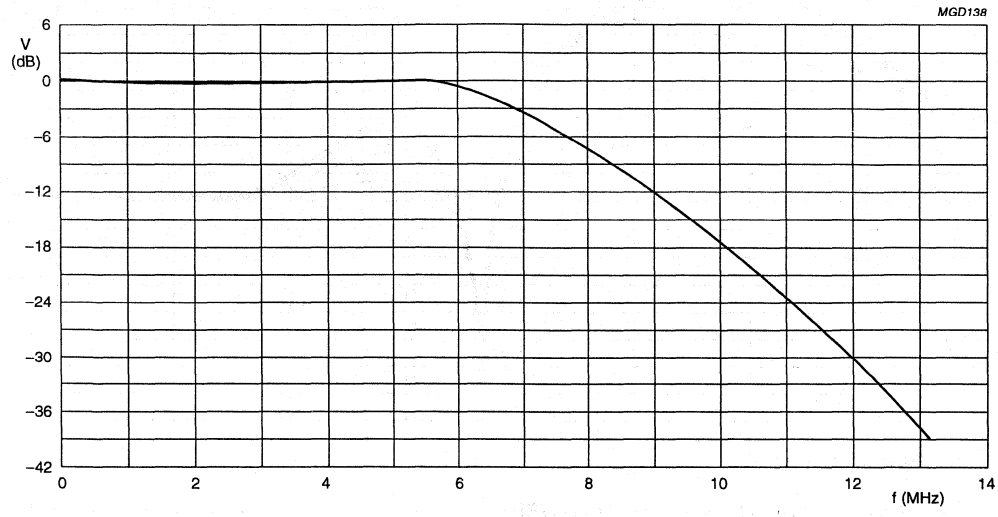


Fig.41 Anti-alias filter.

17.2 TUF-block filter curve

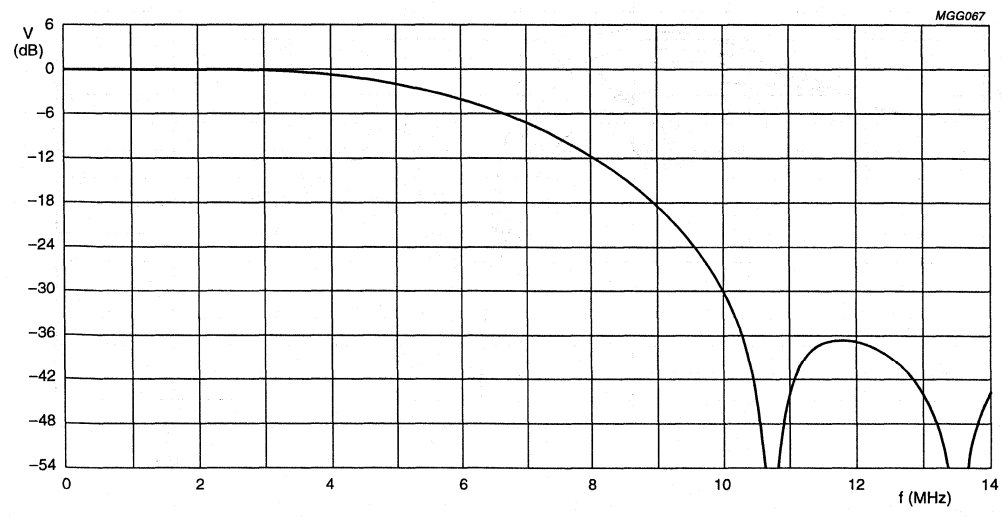
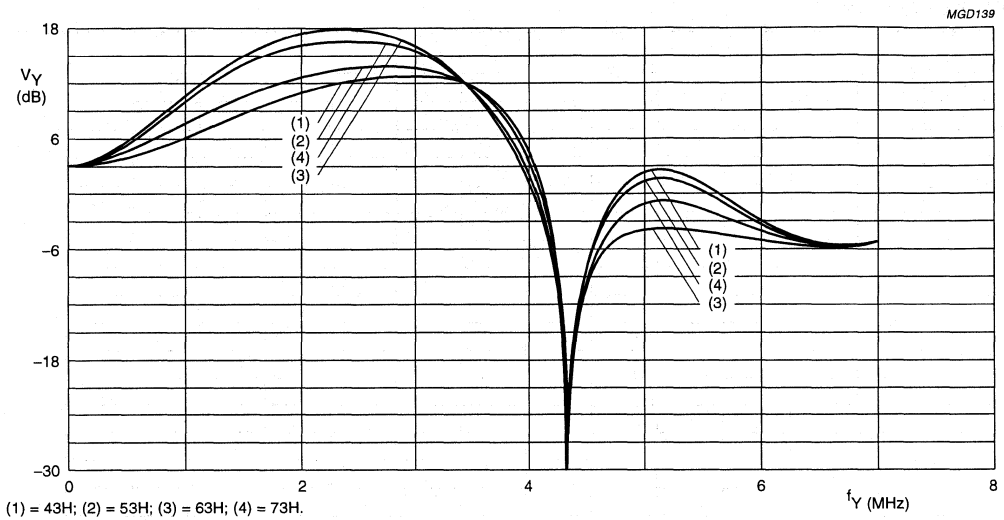


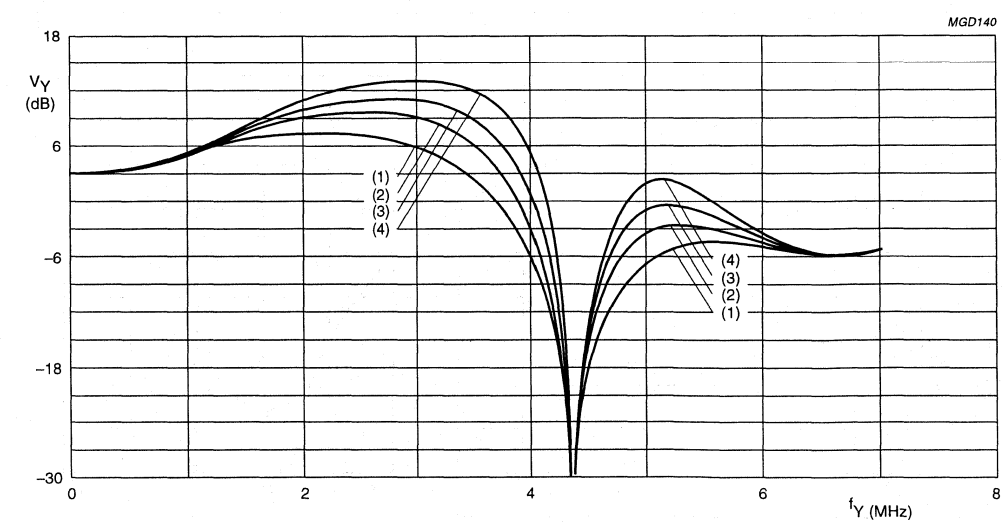
Fig.42 Interpolation filter for the upsampled CVBS-signal.

17.3 Luminance filter curves



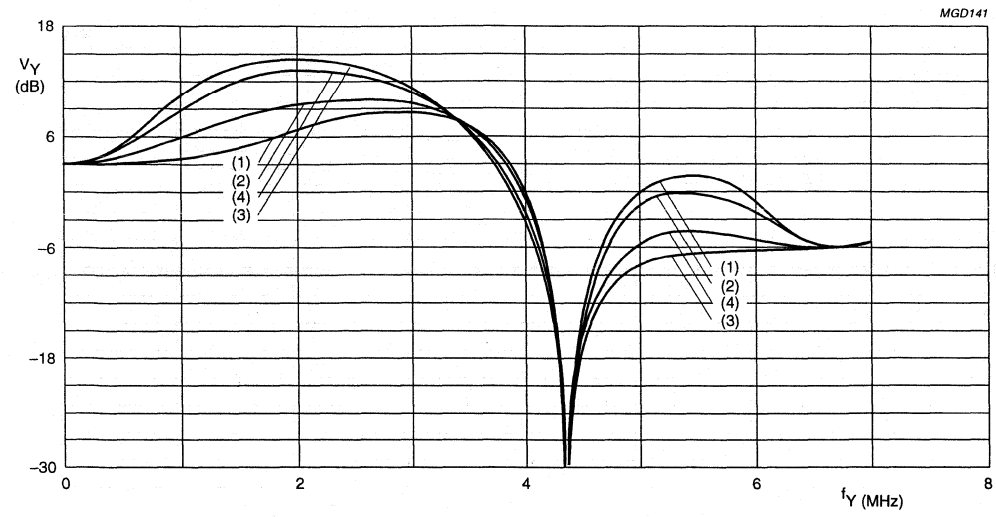
(1) = 43H; (2) = 53H; (3) = 63H; (4) = 73H.

Fig.43 Luminance control SA 09H, 4.43 MHz Trap/CVBS mode, prefilter on, different aperture bandpass centre frequencies.



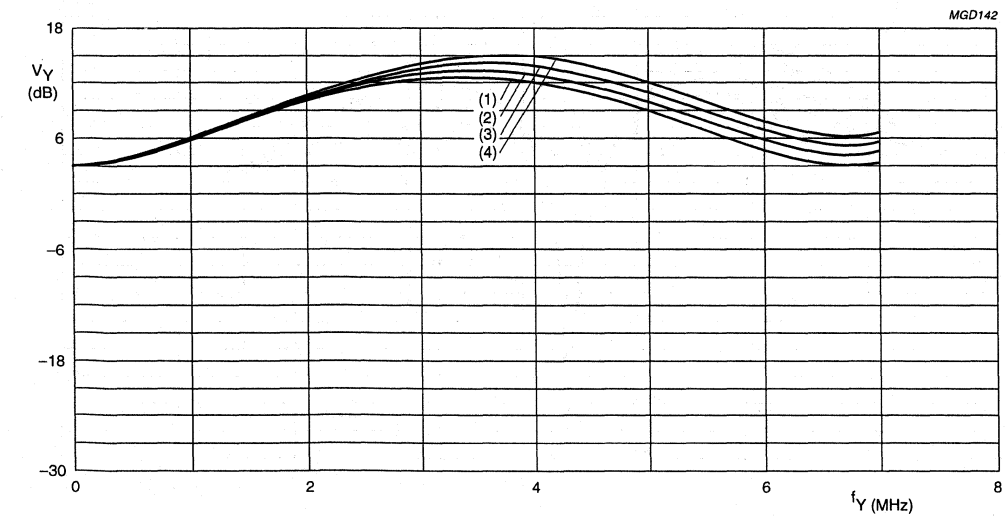
(1) = 40H; (2) = 41H; (3) = 42H; (4) = 43H.

Fig.44 Luminance control SA 09H, 4.43 MHz Trap/CVBS mode, prefilter on, different aperture factors.



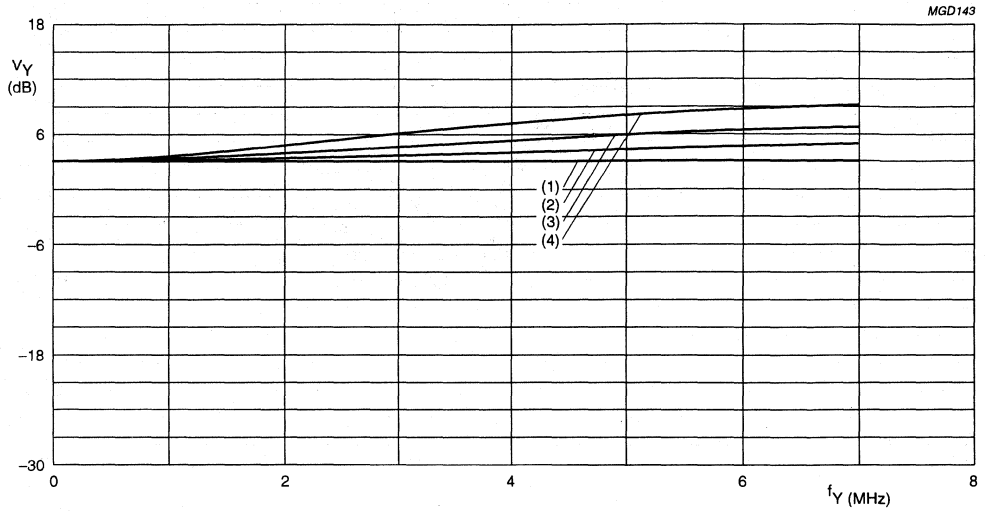
(1) = 03H; (2) = 13H; (3) = 23H; (4) = 33H.

Fig.45 Luminance control SA 09H, 4.43 MHz Trap/CVBS mode, prefilter off, different aperture band-pass centre frequencies.



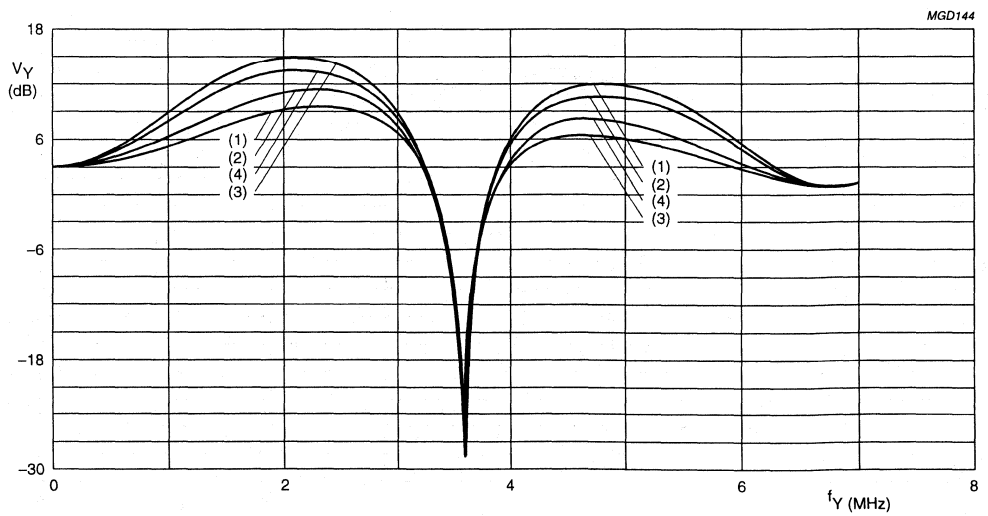
(1) = C0H; (2) = C1H; (3) = C2H; (4) = C3H.

Fig.46 Luminance control SA 09H, Y/C mode, prefilter on, different aperture factors.



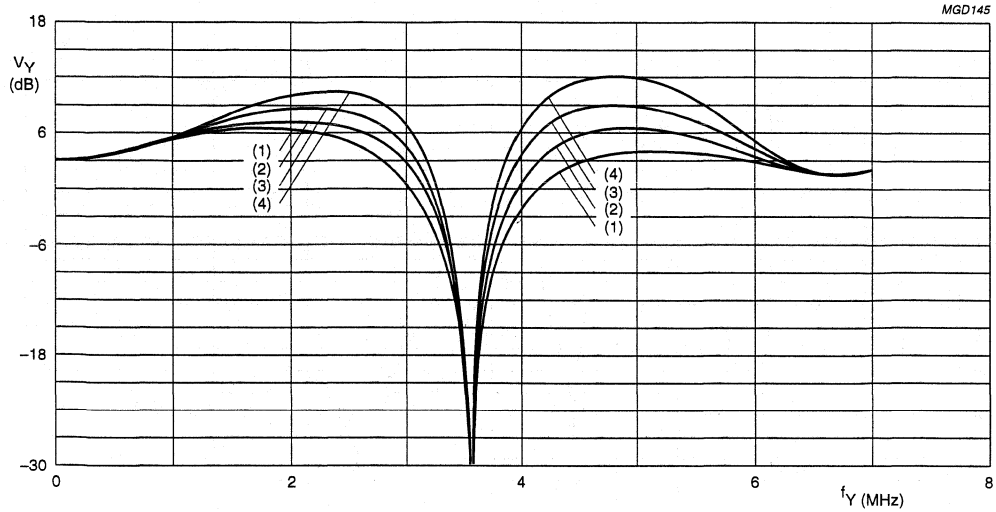
(1) = 80H; (2) = 81H; (3) = 82H; (4) = 83H.

Fig.47 Luminance control SA 09H, Y/C mode, prefilter off, different aperture factors.



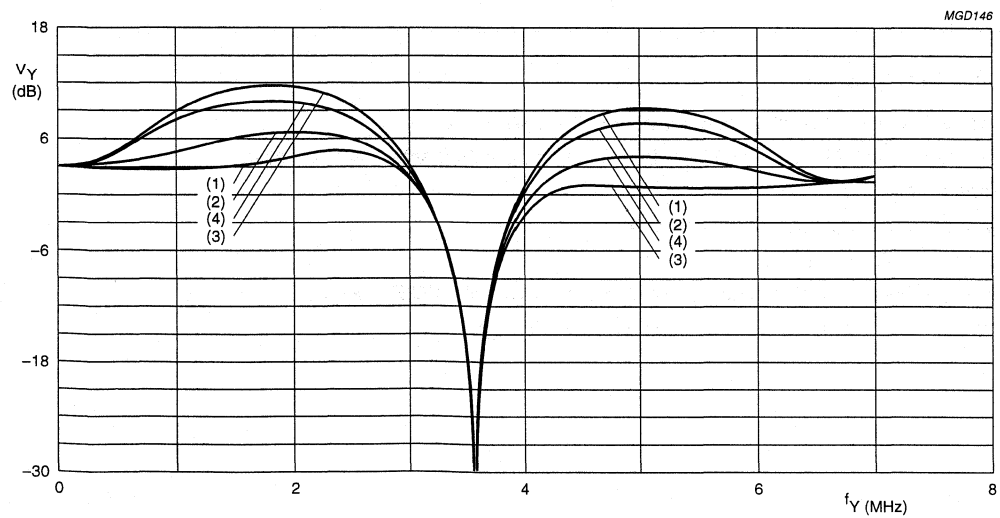
(1) = 43H; (2) = 53H; (3) = 63H; (4) = 73H.

Fig.48 Luminance control SA 09H, 3.58 MHz Trap/CVBS mode, prefilter on, different aperture band-pass centre frequencies.



(1) = 40H; (2) = 41H; (3) = 42H; (4) = 43H.

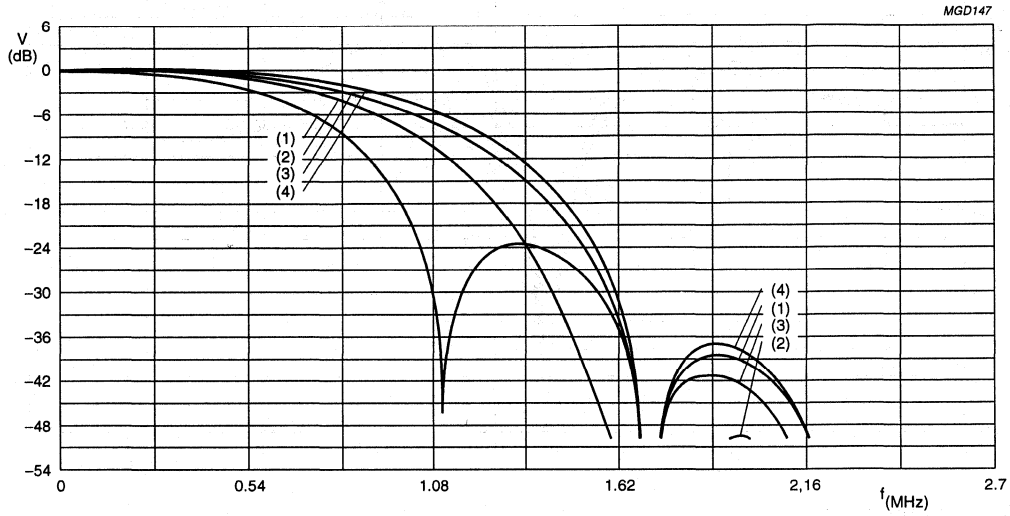
Fig.49 Luminance control SA 09H, 3.58 MHz Trap/CVBS mode, prefilter on, different aperture factors.



(1) = 03H; (2) = 13H; (3) = 23H; (4) = 33H.

Fig.50 Luminance control SA 09H, 3.58 MHz Trap/CVBS mode, prefilter off, different aperture band-pass centre frequencies.

17.4 Chrominance filter curves



Transfer characteristics of the chrominance low-pass dependent on CHBW[1 : 0] settings.
(1) CHBW [1 : 0] = 00; (2) CHBW [1 : 0] = 01; (3) CHBW [1 : 0] = 10; (4) CHBW [1 : 0] = 11.

Fig.51 Chrominance filter.

18 I²C-BUS START SET-UP

- The given values force the following behaviour of the SAA7111A:
  - the analog input AI11 expects a signal in CVBS format; analog anti-alias filter active
  - automatic field detection
  - YUV 4 : 2 : 2 16-bit output format enabled
  - outputs HS, HREF, VREF and VS active
  - contrast, brightness and saturation control in accordance with CCIR standards
  - chrominance processing with nominal bandwidth (800 kHz).

Table 40 I²C-bus start set-up values

SUB (HEX)	FUNCTION	NAME[1]	VALUES (BIN)								(HEX)
			7	6	5	4	3	2	1	0	START
00	chip version	ID07 to ID00; see Table 8	read only								
01	reserved		0	0	0	0	0	0	0	0	00
02	analog input control 1	FUSE1 and FUSE0, GUDL2 to GUDL0, MODE2 to MODE0	1	1	0	0	0	0	0	0	C0
03	analog input control 2	X, HLNRS, VBSL, WPOFF, HOLDG, GAFIX, GAI28, GAI18	0	0	1	0	0	0	1	1	23
04	analog input control 3	GAI17 to GAI10	0	0	0	0	0	0	0	0	00
05	analog input control 4	GAI27 to GAI20	0	0	0	0	0	0	0	0	00
06	horizontal sync start	HSB7 to HSB0	1	1	1	0	1	0	1	1	EB
07	horizontal sync stop	HSS7 to HSS0	1	1	1	0	0	0	0	0	E0
08	sync control	AUFD, FSEL, EXFIL, X, VTRC, HPLL, VNOI1 and VNOI0	1	0	0	0	1	0	0	0	88
09	luminance control	BYPS, PREF, BPSS1 and BPSS0, VBLB, UPTCV, APER1 and APER0	0	0	0	0	0	0	0	1	01
0A	luminance brightness	BRIG7 to BRIG0	1	0	0	0	0	0	0	0	80
0B	luminance contrast	CONT7 to CONT0	0	1	0	0	0	1	1	1	47
0C	chrominance saturation	SATN7 to SATN0	0	1	0	0	0	0	0	0	40
0D	chroma hue control	HUEC7 to HUEC0	0	0	0	0	0	0	0	0	00
0E	chrominance control	CDTO, CSTD2 to CSTD0, DCCF, FCTC, CHBW1 and CHBW0	0	0	0	0	0	0	0	1	01
0F	reserved		0	0	0	0	0	0	0	0	00
10	format/delay control	OFTS1 and OFTS0, YDEL2 to YDEL0 HDEL1 and HDEL0, VRLN	0	1	0	0	0	0	0	0	40
11	output control 1	GPSW, CM99, FECO, COMPO, OEYC, OEHV, VIPB, COLO	0	0	0	1	1	1	0	0	1C
12	output control 2	RTSE1 and RTSE0, TCLO, CBR, RGB888 DIT, AOSL1 and AOSL0	0	0	0	0	0	0	0	1	01
13	output control 3	CCTR1 and CCTR0, BCHI1 and BCHI0, BCLO1 and BCLO0, VCTR1 and VCTR0	0	0	0	0	0	0	0	0	00
14	reserved		0	0	0	0	0	0	0	0	00
15	VBI-data stream start	VSTA7 to VSTA0	0	0	0	0	0	0	0	0	00
16	VBI-data stream stop	VSTO7 to VSTO0	0	0	0	0	0	0	0	0	00
17	MSBs for VBI control	X, X, X, X, X, X, VSTO8, VSTA8	0	0	0	0	0	0	0	0	00
18-19	reserved		0	0	0	0	0	0	0	0	00
1A	text slicer status	0, 0, 0, 0, F2VAL, F2RDY, F1VAL, F1RDY	read only register								
1B	decoded bytes of the text slicer	P1, BYTE1(6 to 0)									
1C		P2, BYTE2(6 to 0)									
1D-1E	reserved		0	0	0	0	0	0	0	0	00
1F	status byte	STTC, HLCK, FIDT, GLIMT, GLIMB, WIPA, SLTCA, CODE	read only register								

Note

1. All X values must be set to LOW.

Decoder with High-Performance Scaler (HPS) for Image Port (PELICAN)

SAA7112

FEATURES

The PELICAN SAA7112 is a video capture device for application at the image port of a VGA controller, with following feature highlights:

Video Decoder

- Six analog inputs, internal analog source selectors, (e.g. 6 × CVBS or(2 × YC and 2 × CVBS) or (1 × YC and 4 × CVBS)
- Two analog preprocessing channels, including built in analog anti-alias filters
- Fully programmable static gain for the main channels or Automatic Gain Control (AGC) for the selected CVBS/Y channel
- Two 8 bit video CMOS Analog-to-Digital Converters (ADCs)
- Automatic Clamp Control (ACC) for CVBS, Y and C
- Switchable white peak control
- On-chip line locked clock generation in accordance with CCIR-601
- Digital PLL for synchronization and clock generation from all standards and non-standard video sources, e.g. consumer grade VTR
- Requires only one crystal (32.11 MHz) for all standards
- Horizontal and vertical sync detection
- Automatic detection of 50/60Hz field frequency, and automatic switching between standards PAL and NTSC
- Luminance and chrominance signal processing for PAL BGHI, PAL N, PAL M, NTSC M, NTSC N, NTSC 4.43 and SECAM
- User programmable luminance peaking or aperture correction
- Cross-colour reduction for NTSC by chrominance combination filtering
- PAL delay line for correcting PAL phase errors
- Real time status information output (RTCO)
- Independent Brightness Contrast Saturation (BCS) adjustment for decoder part.

Video Scaler

- Horizontal and vertical down-scaling and up-scaling to randomly sized windows
- Horizontal and vertical scaling range: 2 (zoom) to $1/64$ (icon); vertical zoom might be restricted
- Anti-alias- and accumulating filter for horizontal scaling
- Vertical scaling with linear phase interpolation (6-bit phase accuracy) and accumulating filter for anti-aliasing
- Horizontal phase correct up- and down-scaling for improved signal quality of scaled data, especially for compression and video phone applications, with 6-bit phase accuracy
- Two independent programming sets for scaler part, to define two 'ranges' per field or per frame
- Field-wise switching between decoder-part and expansion port input
- Brightness, contrast and saturation controls for scaled outputs.

VBI-data decoder and text slicer

- versatile VBI-data decoder, slicer, clock regeneration and byte synchronization; e.g. for WST, NABST, Close Caption, WSS, etc.

Audio clock generation

- Generation of a field locked audio master clock to support a constant number of audio clocks per video field
- Generation of an audio serial and left/right (channel) clock signal.

Digital I/O interfaces

- Real time signal port (R-port), including continuous line locked reference clock and real time status information
- Bidirectional expansion port (X-port) with half duplex functionality (D1), 8-bit YUV
  - output from decoder part, real time, or
  - input to scaler part, e.g. video from MPEG-decoder
- Video image port (I-port) configurable for 8-bit (16-bit) data in master mode (own clock), or slave mode (external clock), with auxiliary timing and hand shake signals
- 8-bit data Host port (H-port) for 16-bit extension of I-port
- Discontinuous data streams supported
- 32-word × 4 bytes FIFO register for video output data

Decoder with High-Performance Scaler (HPS) for Image Port (PELICAN)

SAA7112

- 16-word × 4 bytes FIFO register for decoded VBI output data

  Scaled 4 : 2 : 2, 4 : 1 : 1 YUV output
- Scaled 8-bit luminance only and raw data output
- Decoded VBI data output.

miscellaneous

- Power-on control
- Programming via I²C-bus, or parallel image data port (full read-back ability by an external controller)
- Chip enable function (reset for the clock generator).

APPLICATIONS

- Desktop video
- Multimedia
- Digital television
- Image processing
- Video phone.

GENERAL DESCRIPTION

The PELICAN SAA7112 is a video capture device for applications at the image port of VGA controllers.

The SAA7112 is a combination of a two channel analog preprocessing circuit including source-selection, anti-aliasing filter and ADC, an automatic clamp and gain control, a Clock Generation Circuit (CGC), a digital multistandard decoder and a SAA7140B based scaler, including variable horizontal and vertical up and down scaling and a brightness, contrast and saturation control circuit (see Fig.1).

It is a highly integrated circuit for desktop video applications. The decoder is based on the principle of line-locked clock decoding and is able to decode the colour of PAL, SECAM and NTSC signals into CCIR-601 compatible colour component values. The SAA7112 accepts as analog inputs CVBS or S-video (Y–C) from TV or VCR sources, including weak and distorted signals. An Expansion port for digital video (bidirectional half duplex, D1 compatible) is also supported to connect to MPEG or video phone CODEC. At the so called image port the SAA7112 supports 8-bit (16-bit) wide output data with auxiliary reference data for interfacing to VGA controllers

The target application for PELICAN is to capture and scale video images, to be provided as digital video stream through the image port of a VGA controller, for display via VGAs frame buffer, or for capture to system memory.

In parallel the SAA7112 incorporates also provisions for capturing the serially coded data in the vertical blanking interval (VBI-data). Two principal functions are available: to capture raw video samples and a versatile data slicer (data recovery) unit.

The SAA7112 incorporates also a field locked audio clock generation. This function ensures that there is always the same number of audio samples associated with a field, or a set of fields. This prevents the loss of synchronization between video and audio, during capture or playback.

The circuit can be controlled via the I²C-bus or via its fast parallel programming mode of the image port interface (full write/read capability).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDD}	digital supply voltage	3.0	3.6	V
V_{DDA}	analog supply voltage	3.0	3.6	V
T_{amb}	ambient temperature	0	70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7112	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1

BLOCK DIAGRAMS

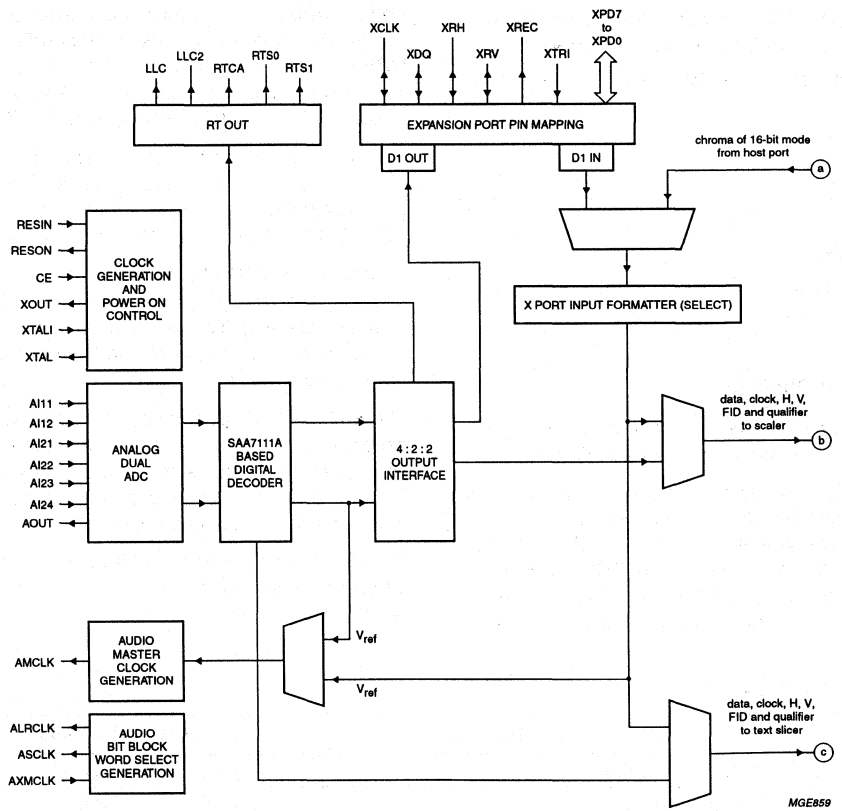


Fig.1 Block diagram (continued in Fig.2).

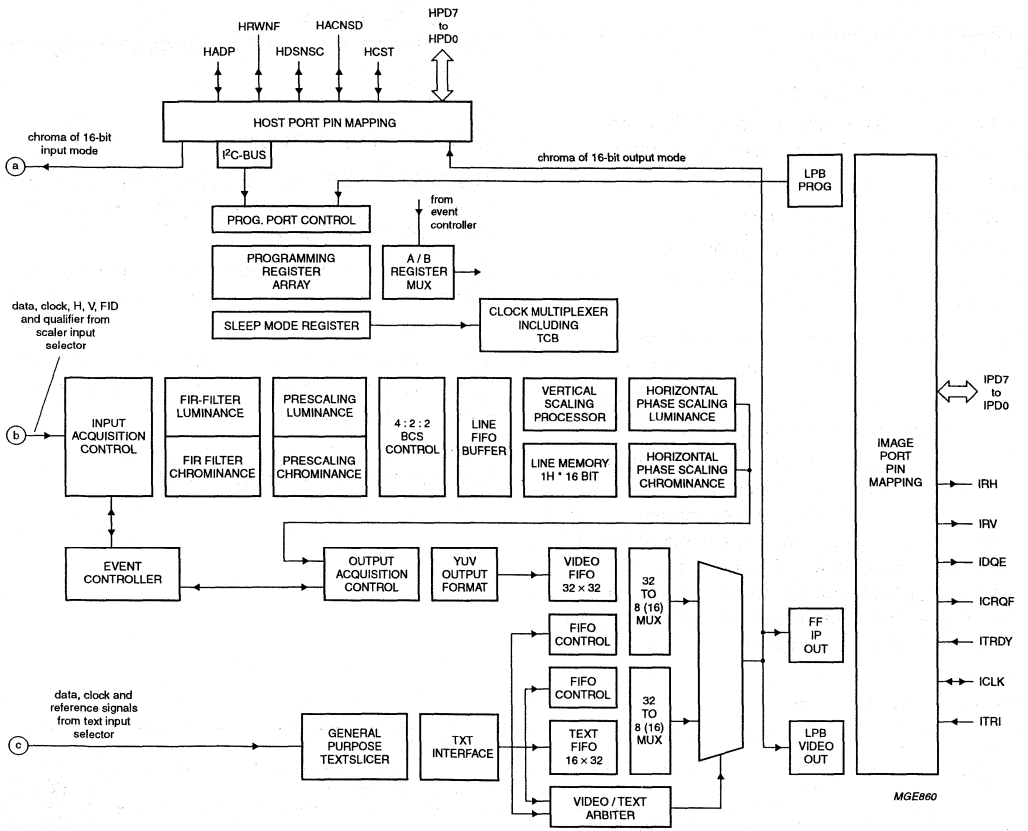


Fig.2 Block diagram (continued from Fig.1).

Digital Video Encoder (ECO-DENC) SAA7124; SAA7125

FEATURES

- Monolithic CMOS 5 V device
- Digital PAL/NTSC encoder
- System pixel frequency 13.5 MHz
- Accepts MPEG decoded data on 8-bit wide input port. Input data format Cb, Y, Cr etc. *"(CCIR 656)"*
- Four DACs for CVBS (10-bit resolution), RGB (9-bit resolution) operating at 27 MHz; RGB sync on CVBS
- Optionally 2 times CVBS and Y, C (all 10-bit resolution) available simultaneously
- Closed captioning encoding
- On-chip YUV to RGB dematrix optionally to be by-passed for Cr, Y, Cb output on RGB DACs
- Fast I²C-bus control port (400 kHz)
- Encoder can be master or slave
- Programmable horizontal and vertical input synchronization phase, via input pins or auxiliary codes at MP data port
- Programmable horizontal sync output phase
- Internal 100/75 Colour Bar Generator (CBG)
- Macrovision Pay-per-View copy protection system as option, also partly used for RGB output.

  This applies to SAA7124 only. The device is protected by USA patent numbers 4631603, 4577216 and 4819098 and other intellectual property rights. Use of the Macrovision anti-copy process in the device is licensed for non-commercial home use only. Reverse engineering or disassembly is prohibited. Please contact your nearest Philips Semiconductor sales office for more information
- Controlled rise and fall times of output syncs and blanking
- Down-mode of DACs
- LQFP64 (V1 devices only), QFP80 or PLCC84 package.

GENERAL DESCRIPTION

The SAA7124; SAA7125 encodes digital YUV video data to an NTSC or PAL CVBS plus RGB or alternatively to S-Video and CVBS output.

Optionally, the YUV to RGB dematrix can be by-passed providing the digital-to-analog converted Cb, Y, Cr signals instead of RGB.

The circuit accepts CCIR compatible YUV data with 720 active pixels per line in 4 : 2 : 2 multiplexed formats, for example MPEG decoded data.

It includes a sync/clock generator and on-chip Digital-to-Analog Converters (DACs).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE[1]		
	NAME	DESCRIPTION	VERSION
SAA7124WP; SAA7125WP	PLCC84	plastic leaded chip carrier; 84 leads	SOT189-2
SAA7124HZ; SAA7125HZ	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
SAA7124H; SAA7125H	QFP80	plastic quad flat package; 80 leads (lead length 2.35 mm); body 14 × 20 × 2.8 mm	SOT318-3

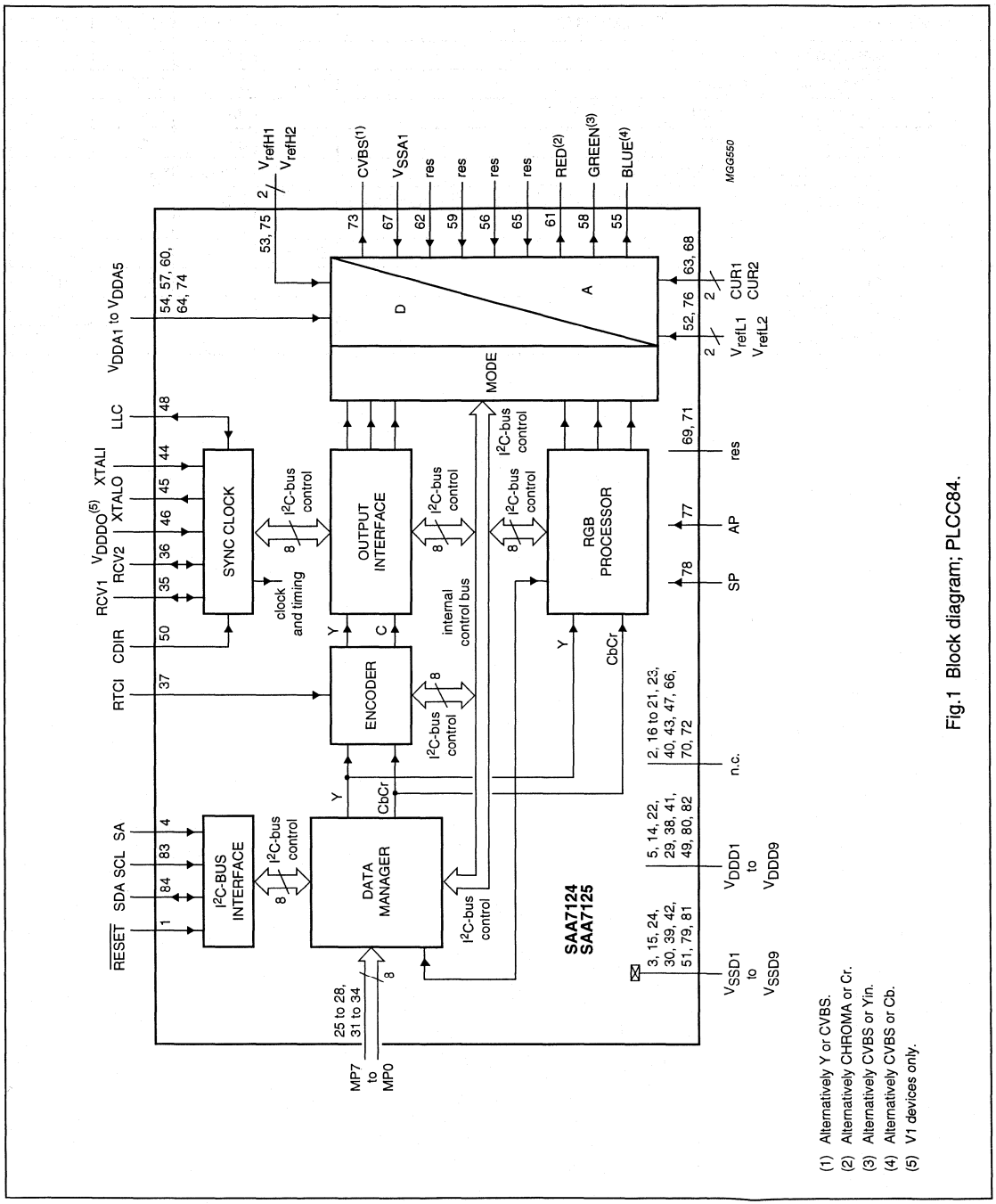
Note

1. LQFP64 package for V1 devices only.

QUICK REFERENCE DATA

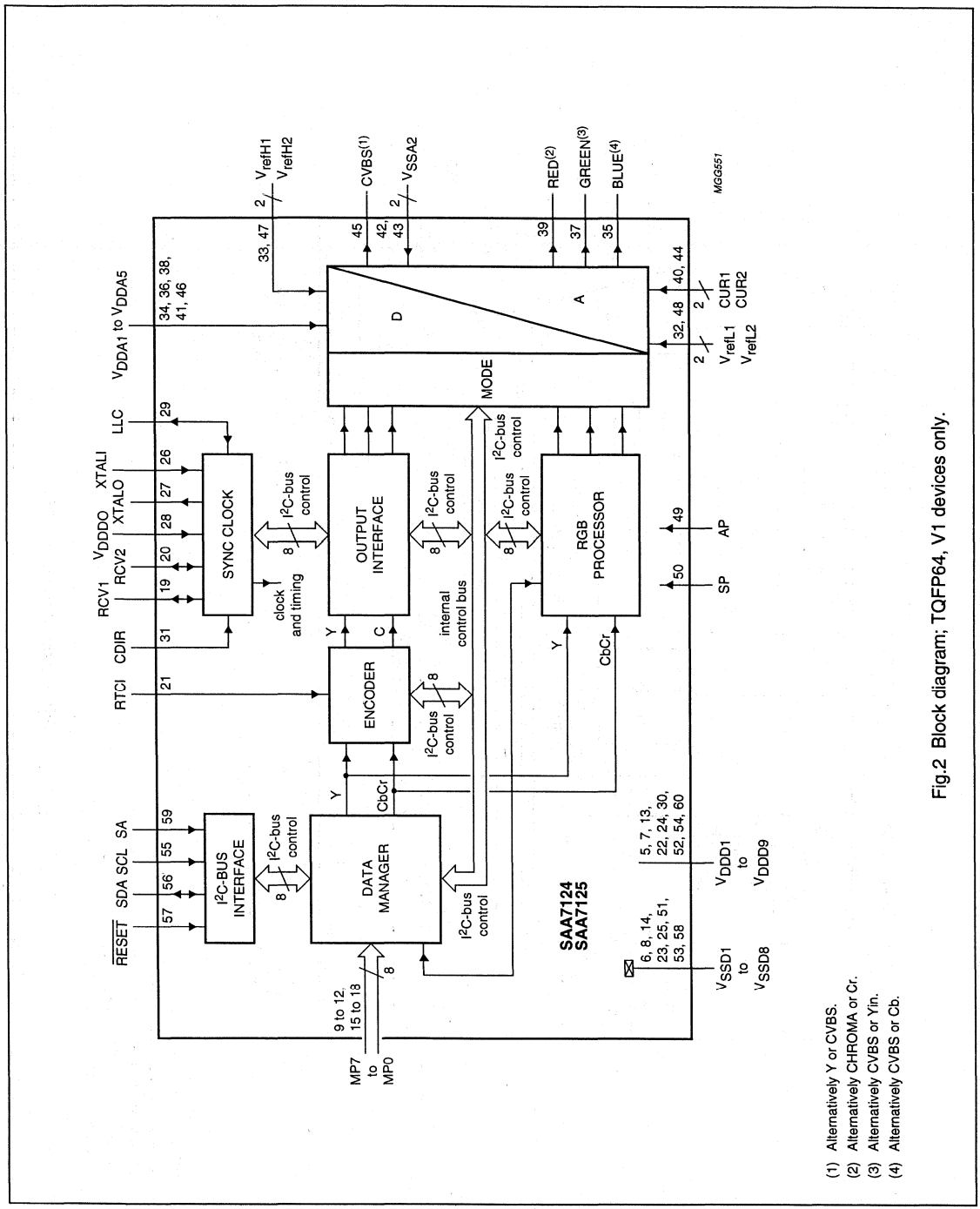
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage	4.75	5.0	5.25	V
V_{DDD}	digital supply voltage	4.75	5.0	5.25	V
I_{DDA}	analog supply current	–	tbf	60	mA
I_{DDD}	digital supply current	–	tbf	100	mA
V_i	input signal voltage levels	TTL compatible			
$V_{o(p-p)}$	analog output signal voltages Y, C, CVBS and RGB without load (peak-to-peak value)	–	2.0	–	V
R_L	load resistance	80	–	–	Ω
ILE	LF integral linearity error	–	–	±4	LSB
DLE	LF differential linearity error	–	–	±1	LSB
T_{amb}	operating ambient temperature	0	–	+70	°C

BLOCK DIAGRAM



(1) Alternatively Y or CVBS.
(2) Alternatively CHROMA or Cr.
(3) Alternatively CVBS or Yin.
(4) Alternatively CVBS or Cb.
(5) V1 devices only.

Fig.1 Block diagram; PLCC84.



(1) Alternatively Y or CVBS.
(2) Alternatively CHROMA or Cr.
(3) Alternatively CVBS or Yin.
(4) Alternatively CVBS or Cb.

Fig.2 Block diagram; TQFP64, V1 devices only.

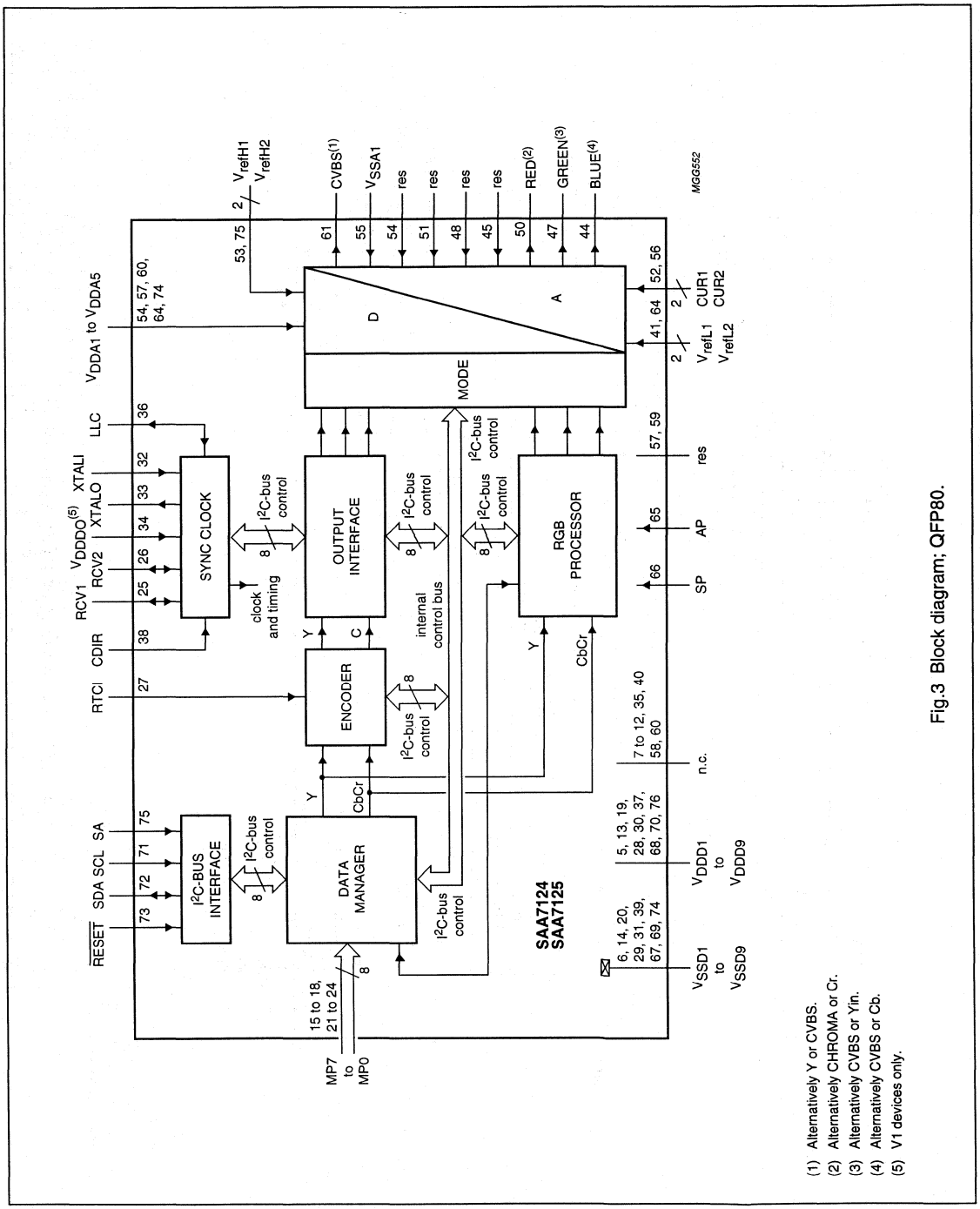


Fig.3 Block diagram; QFP80.

(1) Alternatively Y or CVBS.
(2) Alternatively CHROMA or Cr.
(3) Alternatively CVBS or Yin.
(4) Alternatively CVBS or Cb.
(5) V1 devices only.

PINNING

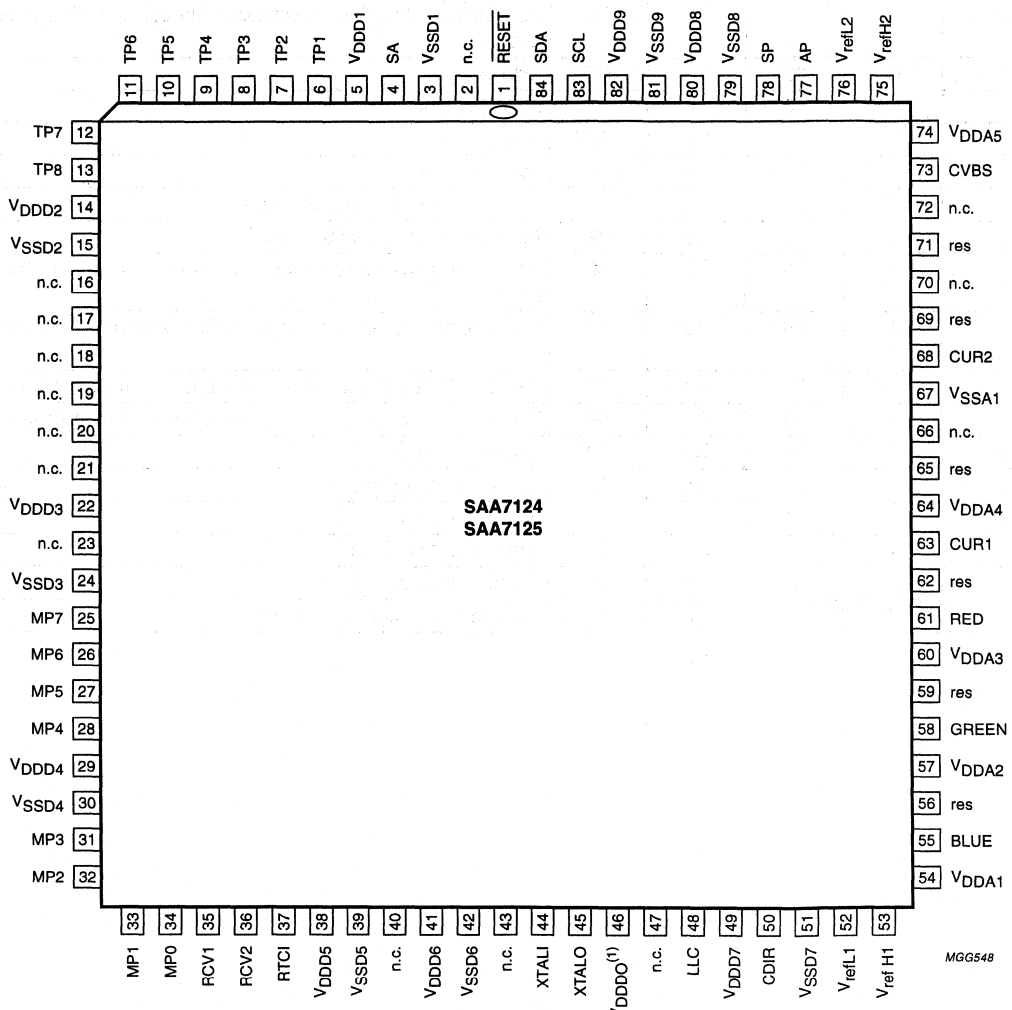
SYMBOL	TYPE	PIN			DESCRIPTION
		PLCC84	LQFP64	QFP80	
$\overline{RESET}$	I	1	57	73	Reset input, active LOW. After reset is applied, all digital I/Os are in input mode. The I²C-bus receiver waits for the START condition.
n.c.	–	2	–	–	not connected
V_{SSD1}	I	3	6	6	digital ground 1
SA	I	4	59	75	The I²C-bus slave address select input pin. LOW: slave address = 88H, HIGH = 8CH.
V_{DDD1}	I	5	5	5	digital supply voltage 1
TP1	O	6	61	77	Test pin outputs. Leave open for normal operation.
TP2	O	7	62	78	
TP3	O	8	63	79	
TP4	O	9	64	80	
TP5	O	10	1	1	
TP6	O	11	2	2	
TP7	O	12	3	3	
TP8	O	13	4	4	
V_{DDD2}	I	14	7	13	digital supply voltage 2
V_{SSD2}	I	15	8	14	digital ground 2
n.c.	–	16	–	7	not connected
n.c.	–	17	–	8	
n.c.	–	18	–	9	
n.c.	–	19	–	10	
n.c.	–	20	–	11	
n.c.	–	21	–	12	
V_{DDD3}	I	22	13	19	digital supply voltage 3
n.c.	–	23	–	–	not connected
V_{SSD3}	I	24	14	20	digital ground 3
MP7	I	25	9	15	Upper 4 bits of MPEG port. It is an input for *"CCIR 656"* style multiplexed Cb, Y, Cr data.
MP6	I	26	10	16	
MP5	I	27	11	17	
MP4	I	28	12	18	
V_{DDD4}	I	29	22	28	digital supply voltage 4
V_{SSD4}	I	30	23	29	digital ground 4
MP3	I	31	15	21	Lower 4 bits of MPEG port. It is an input for *"CCIR 656"* style multiplexed Cb, Y, Cr data.
MP2	I	32	16	22	
MP1	I	33	17	23	
MP0	I	34	18	24	
RCV1	I/O	35	19	25	Raster Control 1 for video port. This pin receives/provides a VS/FS/FSEQ signal.

SYMBOL	TYPE	PIN			DESCRIPTION
		PLCC84	LQFP64	QFP80	
RCV2	I/O	36	20	26	Raster Control 2 for video port. This pin provides an HS pulse of programmable length or receives an HS pulse.
RTCI	I	37	21	27	Real Time Control input. If the LLC clock is provided by an SAA7111 or SAA7151B, RTCI should be connected to the RTCO pin of the respective decoder to improve the signal quality.
V_{DDD5}	I	38	24	30	digital supply voltage 5
V_{SSD5}	I	39	25	31	digital ground 5
n.c.	–	40	–	35	not connected
V_{DDD6}	I	41	30	37	digital supply voltage 6
V_{SSD6}	I	42	51	39	digital ground 6
n.c.	–	43	–	40	not connected
XTALI	I	44	26	32	Crystal oscillator input (from crystal). If the oscillator is not used, this pin should be connected to ground.
XTALO	O	45	27	33	Crystal oscillator output (to crystal).
V_{DDDO}	I	46	28	34	digital supply voltage for the internal oscillator; note 1
n.c.	–	47	–	–	not connected
LLC	I/O	48	29	36	Line-Locked Clock. This is the 27 MHz master clock for the encoder. The I/O direction is set by the CDIR pin.
V_{DDD7}	I	49	52	68	digital supply voltage 7
CDIR	I	50	31	38	Clock direction. If CDIR input is HIGH, the circuit receives a clock signal, otherwise if CDIR is LOW, LLC is generated by the internal crystal oscillator.
V_{SSD7}	I	51	53	67	digital ground 7
V_{refL1}	I	52	32	41	Lower reference voltage 1 input for DACs; connect to analog ground.
V_{refH1}	I	53	33	42	Upper reference voltage 1 input for DACs; connect via 100 nF capacitor to analog ground.
V_{DDA1}	I	54	34	43	Analog supply voltage 1 for DACs.
BLUE	O	55	35	44	Analog output of the BLUE component.
res	I	56	–	45	reserved
V_{DDA2}	I	57	36	46	Analog supply voltage 2 for DACs.
GREEN	O	58	37	47	Analog output of GREEN component.
res	I	59	–	48	reserved
V_{DDA3}	I	60	38	49	Analog supply voltage 3 for DACs.
RED	O	61	39	50	Analog output of RED component.
res	I	62	–	51	reserved
CUR1	I	63	40	52	Current input 1 for RGB amplifiers; connect via 15 kΩ resistor to V_{DDA}.
V_{DDA4}	I	64	41	53	Analog supply voltage 4 for DACs.
res	I	65	–	54	reserved
n.c.	–	66	–	–	not connected

SYMBOL	TYPE	PIN			DESCRIPTION
		PLCC84	LQFP64	QFP80	
V_{SSA1}	I	67	42	55	Analog ground 1 for the DACs.
V_{SSA2}	I	–	43	–	Analog ground 2 for the DACs.
CUR2	I	68	44	56	Current input 2 for RGB amplifiers; connect via 15 kΩ resistor to V_{DDA}.
res	O	69	–	57	reserved
n.c.	–	70	–	58	not connected
res	O	71	–	59	reserved
n.c.	–	72	–	60	not connected
CVBS	O	73	45	61	Analog output of the CVBS signal.
V_{DDA5}	I	74	46	62	Analog supply voltage 5 for DACs.
V_{refH2}	I	75	47	63	Upper reference voltage 2 input for DACs; connect via 100 nF capacitor to analog ground.
V_{refL2}	I	76	48	64	Lower reference voltage 2 input for DACs; connect to analog ground.
AP	I	77	49	65	Test pin. Connected to digital ground for normal operation.
SP	I	78	50	66	Test pin. Connected to digital ground for normal operation.
V_{SSD8}	I	79	58	69	digital ground 8
V_{DDD8}	I	80	54	70	digital supply voltage 8
V_{SSD9}	I	81	–	74	digital ground 9
V_{DDD9}	I	82	60	76	digital supply voltage 9
SCL	I	83	55	71	I²C-bus serial clock input.
SDA	I/O	84	56	72	I²C-bus serial data input/output.

Note

1. V1 devices only.



(1) V1 devices only.

Fig.4 Pin configuration; PLCC84.

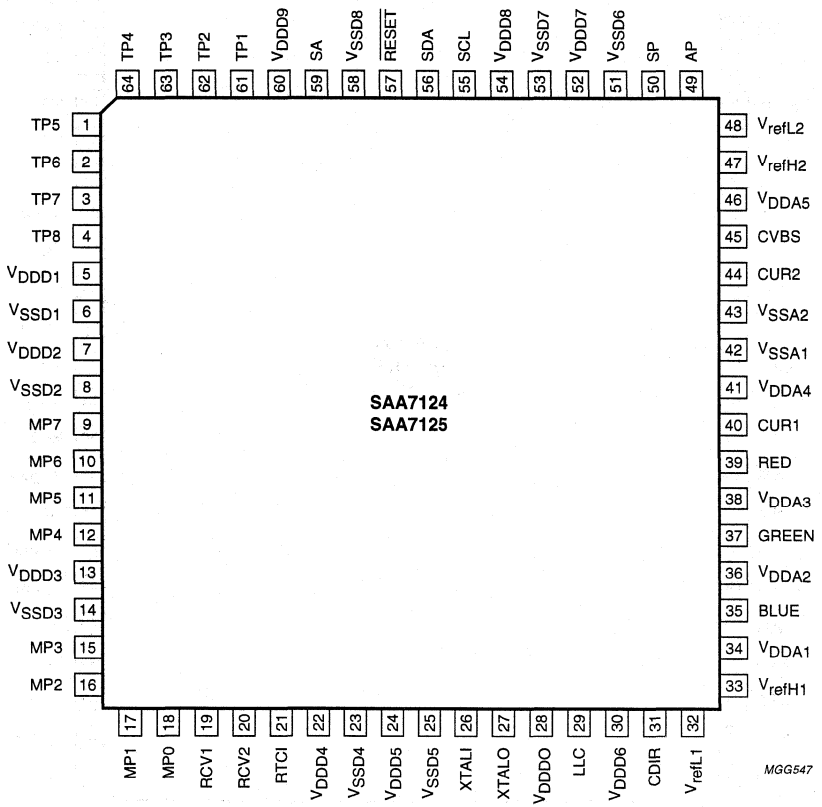
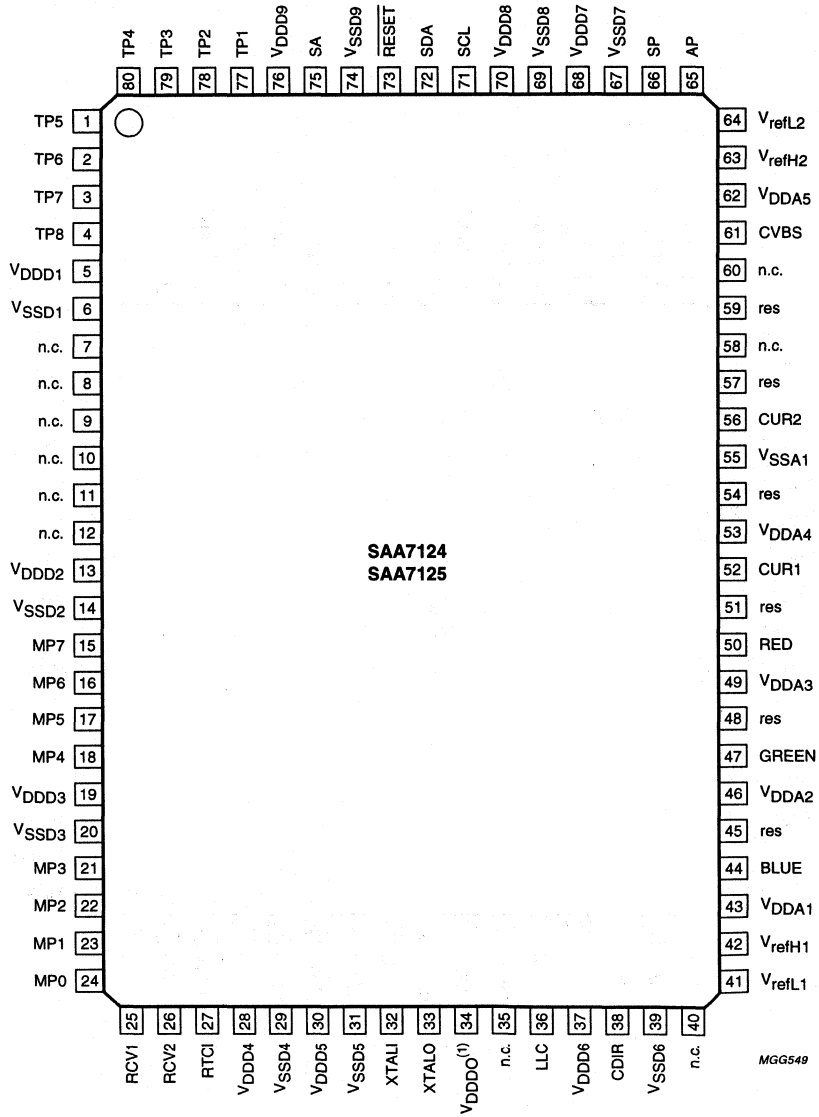


Fig.5 Pin configuration; LQFP64 (V1 devices only).



(1) V1 devices only.

Fig.6 Pin configuration; QFP80.

FUNCTIONAL DESCRIPTION

The digital video encoder (ECO-DENC) encodes digital luminance and colour difference signals into analog CVBS and simultaneously RGB signals. NTSC-M, PAL B/G standards and sub-standards are supported.

Both interlaced and non-interlaced operation is possible for all standards.

Optionally, the input Y, Cb and Cr data, digital-to-analog converted, is available at the analog RGB outputs.

For applications that do not require RGB output, the device can be configured in such a way that S-Video and twice CVBS is available (Y at CVBS-DAC, C at R-DAC, and CVBS at G-DAC and B-DAC).

The basic encoder function consists of subcarrier generation, colour modulation and insertion of synchronization signals. Luminance and chrominance signals are filtered in accordance with the standard requirements of *"RS-170-A"* and *"CCIR 624"*.

For ease of analog post filtering the signals are twice oversampled with respect to the pixel clock before digital-to-analog conversion.

For total filter transfer characteristics see Figs 7, 8, 9, 10, 11 and 12. The DACs for Y, C, and CVBS are realized with full 10-bit resolution, DACs for RGB with 9-bit resolution.

The MPEG port (MP) accepts 8 line multiplexed Cb, Y, Cr data.

The 8-bit multiplexed Cb-Y-Cr formats are *"CCIR 656"* (D1 format) compatible, but auxiliary codes such as SAV and EAV are decoded optionally for trigger purposes.

A crystal-stable master clock (LLC) of 27 MHz, which is twice the CCIR line-locked pixel clock of 13.5 MHz, needs to be supplied externally. Optionally, a crystal oscillator input/output pair of pins and an on-chip clock driver is provided.

It is also possible to connect a Philips Digital Video Decoder (SAA7111 or SAA7151B) in conjunction with a CREF clock qualifier to ECO-DENC. Via the RTCI pin, connected to RTCO of a decoder, information concerning actual subcarrier, PAL-ID, and if connected to SAA7111, definite subcarrier phase can be inserted.

The ECO-DENC synthesizes all necessary internal signals, colour subcarrier frequency, and synchronization signals, from that clock.

The encoder can be configured as slave with respect to RCV trigger inputs or auxiliary *"CCIR 656"* codes, or can be master to output horizontal and vertical trigger pulses.

The IC also contains Closed Caption and Extended Data Services Encoding (Line 21), and supports anti-taping signal generation in accordance with Macrovision.

A number of possibilities are provided for setting different video parameters such as:

- Black and blanking level control
- Colour subcarrier frequency
- Variable burst amplitude etc.

During reset ($\overline{\text{RESET}}$ = LOW) and after reset is released, all digital I/O stages are set to input mode. A reset forces the I²C-bus interface to abort any running bus transfer and sets register 3A to 03H, register 61 to 06H and registers 6BH and 6EH to 00H. All other control registers are not influenced by a reset.

Data manager

In the data manager, real time arbitration on the data stream to be encoded is performed.

Optionally, the device can operate as a 100/75 colour bar test pattern generator without need for an external data source.

Encoder

VIDEO PATH

The encoder generates out of Y, U and V baseband signals luminance and colour subcarrier output signals, suitable for use as CVBS or separate Y and C signals.

Luminance is modified in gain and in offset (latter programmable in a certain range to enable different black level set-ups). After having been inserted a fixed synchronization level, in accordance with standard composite synchronization schemes, and blanking level, programmable also in a certain range to allow for manipulations with Macrovision anti-taping, additional insertion of AGC super-white pulses, programmable in height, is supported.

In order to enable easy analog post filtering, luminance is interpolated from 13.5 MHz data rate to 27 MHz data rate, providing luminance in 10-bit resolution. This filter is also used to define smoothed transients for synchronization pulses and blanking period. For transfer characteristic of the luminance interpolation filter see Figs 9 and 10.

Chrominance is modified in gain (programmable separately for U and V), standard dependent burst is inserted, before baseband colour signals are interpolated from 6.75 MHz data rate to 27 MHz data rate. One of the interpolation stages can be bypassed, thus providing a higher colour bandwidth, which can be made use of for Y and C output. For transfer characteristics of the chrominance interpolation filter see Figs 7 and 8.

The amplitude of inserted burst is programmable in a certain range, suitable for standard signals and for special effects. Behind the succeeding quadrature modulator, colour in 10-bit resolution is provided on subcarrier.

The numeric ratio between Y and C outputs is in accordance with set standards.

CLOSED CAPTION ENCODER

Using this circuit, data in accordance with the specification of Closed Caption or Extended Data Service, delivered by the control interface, can be encoded (Line 21). Two dedicated pairs of bytes (two bytes per field), each pair preceded by run-in clocks and framing code, are possible.

The actual line number where data is to be encoded in, can be modified in a certain range.

Data clock frequency is in accordance with definition for NTSC-M standard 32 times horizontal line frequency.

Data LOW at the output of the DACs corresponds to 0 IRE, data HIGH at the output of the DACs corresponds to approximately 50 IRE.

It is also possible to encode Closed Caption Data for 50 Hz field frequencies at 32 times horizontal line frequency.

ANTI-TAPING (SAA7124 ONLY)

For more information contact your nearest Philips Semiconductors sales office.

RGB processor

This block contains a dematrix in order to produce RED, GREEN and BLUE signals to be fed to a SCART plug.

Before Y, Cb and Cr signals are de-matrixed, 2 times oversampling for luminance and 4 times oversampling for colour difference signals is performed. For transfer curves of luminance and colour difference components of RGB see Figs 11 and 12.

Output interface/DACs

In the output interface encoded both Y and C signals are converted from digital-to-analog in 10-bit resolution. Y and C signals are also combined to a 10-bit CVBS signal.

RED, GREEN and BLUE signals (optionally Cr, Y, Cb) are also converted from digital-to-analog, each providing a 9-bit resolution.

All output occurs with the same processing delay. Absolute amplitudes at the input of the DAC for CVBS is reduced by $^{15}/_{16}$ with respect to Y and C DACs to make maximum use of conversion ranges.

Depending on control bits YC_EN and DEMOFF, different signal combinations are available at DACs #1 to #4. YC_EN = DEMOFF = LOW is the default configuration after reset.

Table 1 Control of DAC signals

YC_EN	DEMOFF	DAC1	DAC2	DAC3	DAC4
0	0	CVBS	R	G	B
0	1	CVBS	Cr	Y	Cb
1	0	VBS	C	CVBS	CVBS
1	1	VBS	C	CVBS	CVBS

Outputs of the DACs can be set together in two groups (#1 and #2 by DOWNB, #3 and #4 by DOWNA) via software control to minimum output voltage for either purpose.

Synchronization

Synchronization of the ECO-DENC is able to operate in two modes; slave mode and master mode.

In the slave mode, the circuit accepts synchronization pulses at the bidirectional RCV1 port (or equivalently as frame synchronization from *"CCIR 656"* data stream). The timing and trigger behaviour related to RCV1 can be influenced by programming the polarity and on-chip delay of RCV1. Active slope of RCV1 defines the vertical phase and optionally the odd/even and colour frame phase to be initialized, it can be also used to set the horizontal phase.

If the horizontal phase is not to be influenced by RCV1, a horizontal pulse needs to be supplied at the RCV2 pin (or a horizontal synchronization from *"CCIR 656"* data stream). Timing and trigger behaviour can also be influenced for RCV2.

If there are missing pulses at RCV1 and/or RCV2, the time base of ECO-DENC runs free, thus an arbitrary number of synchronization slopes may miss, but no additional pulses (with the incorrect phase) must occur.

If the vertical and horizontal phase is derived from RCV1, RCV2 can be used for horizontal or composite blanking input or output.

Alternatively, the device can be triggered by auxiliary codes in a *"CCIR 656"* data stream at the MP port.

In the master mode, the time base of the circuit continuously runs free. On the RCV1 port, the IC can output:

- A Vertical Sync signal (VS) with 3 or 2.5 lines duration, or;
- An ODD/EVEN signal which is LOW in odd fields, or;
- A field sequence signal (FSEQ) which is HIGH in the first of 4, 8 fields respectively.

On the RCV2 port, the IC can provide a horizontal pulse with programmable start and stop phase; this pulse can be inhibited in the vertical blanking period to build up, for example, a composite blanking signal.

The polarity of both RCV1 and RCV2 is selectable by software control.

Field length is in accordance with to 50 Hz or 60 Hz standards, including non-interlaced options; start and end of its active part can be programmed. The active part of a field always starts at the beginning of a line, If the standard blanking option SBLBN is not set.

I²C-bus interface

The I²C-bus interface is a standard slave transceiver, supporting 7-bit slave addresses and 400 kbits/s guaranteed transfer rate. It uses 8-bit subaddressing with an auto-increment function. All registers are write only, except one readable status byte.

Two I²C-bus slave addresses are selected:

88H: LOW at pin SA

8CH: HIGH at pin SA.

Input levels and formats

ECO-DENC expects digital Y, Cb, Cr data with levels (digital codes) in accordance with *"CCIR 601"*.

For C and CVBS outputs, deviating amplitudes of the colour difference signals can be compensated by independent gain control setting, while gain for luminance is set to predefined values, distinguishable for 7.5 IRE set-up or without set-up.

For RGB (or Y, Cb and Cr) outputs fixed amplification in accordance with *"CCIR 601"* is provided.

Reference levels are measured with a colour bar, 100% white, 100% amplitude and 100% saturation.

TRANSFORMATION

$R = Y + 1.3707 \times (Cr - 128)$

$G = Y - 0.3365 \times (Cb - 128) - 0.6982 \times (Cr - 128)$

$B = Y + 1.7324 \times (Cb - 128)$.

Representation of R, G and B at the output is 9 bits at 27 MHz.

Table 2 8-bit multiplexed format (similar to *"CCIR 656"*)

TIME	BITS							
	0	1	2	2	4	5	6	7
Sample	Cb_0	Y_0	Cr_0	Y_1	Cb_2	Y_2	Cr_2	Y_3
Luminance pixel number	0		1		2		3	
Colour pixel number	0				2			

Bit allocation map

Table 3 Slave receiver (slave address 88H or 8CH)

REGISTER FUNCTION	SUB ADDRESS	DATA BYTE[1]							
		D7	D6	D5	D4	D3	D2	D1	D0
Null	00	0	0	0	0	0	0	0	0
		↓							
Null	39	0	0	0	0	0	0	0	0
I/O port control	3A	CBENB	0	YC_EN	SYMP	DEMOFF	0	Y2C	UV2C
Null	42	0	0	0	0	0	0	0	0
		↓							
Null	59	0	0	0	0	0	0	0	0
Chrominance phase	5A	CHPS7	CHPS6	CHPS5	CHPS4	CHPS3	CHPS2	CHPS1	CHPS0
Gain U	5B	GAINU7	GAINU6	GAINU5	GAINU4	GAINU3	GAINU2	GAINU1	GAINU0
Gain V	5C	GAINV7	GAINV6	GAINV5	GAINV4	GAINV3	GAINV2	GAINV1	GAINV0
Gain U MSB, black level	5D	GAINU8	0	BLCKL5	BLCKL4	BLCKL3	BLCKL2	BLCKL1	BLCKL0
Gain V MSB, blanking level, decoder type	5E	GAINV8	DECTYP	BLNNL5	BLNNL4	BLNNL3	BLNNL2	BLNNL1	BLNNL0
Blanking level VBI	5F	0	0	BLNVB5	BLNVB4	BLNVB3	BLNVB2	BLNVB1	BLNVB0
Null	60	0	0	0	0	0	0	0	0
Standard control	61	DOWNB	DOWNA	INPI	YGS	0	SCBW	PAL	FISE
RTC enable burst amplitude	62	RTCE	BSTA6	BSTA5	BSTA4	BSTA3	BSTA2	BSTA1	BSTA0
Subcarrier 0	63	FSC07	FSC06	FSC05	FSC04	FSC03	FSC02	FSC01	FSC00
Subcarrier 1	64	FSC15	FSC14	FSC13	FSC12	FSC11	FSC10	FSC09	FSC08
Subcarrier 2	65	FSC23	FSC22	FSC21	FSC20	FSC19	FSC18	FSC17	FSC16
Subcarrier 3	66	FSC31	FSC30	FSC29	FSC28	FSC27	FSC26	FSC25	FSC24
Line 21 odd 0	67	L21O07	L21O06	L21O05	L21O04	L21O03	L21O02	L21O01	L21O00
Line 21 odd 1	68	L21O17	L21O16	L21O15	L21O14	L21O13	L21O12	L21O11	L21O10
Line 21 even 0	69	L21E07	L21E06	L21E05	L21E04	L21E03	L21E02	L21E01	L21E00
Line 21 even 1	6A	L21E17	L21E16	L21E15	L21E14	L21E13	L21E12	L21E11	L21E10
RCV port control	6B	SRCV11	SRCV10	TRCV2	ORCV1	PRCV1	CBLF	ORCV2	PRCV2
Trigger control	6C	HTRIG7	HTRIG6	HTRIG5	HTRIG4	HTRIG3	HTRIG2	HTRIG1	HTRIG0
Trigger control	6D	HTRIG10	HTRIG9	HTRIG8	VTRIG4	VTRIG3	VTRIG2	VTRIG1	VTRIG0
Multi control	6E	SBLBN	0	PHRES1	PHRES0	0	0	FLC1	FLCO

REGISTER FUNCTION	SUB ADDRESS	DATA BYTE[1]							
		D7	D6	D5	D4	D3	D2	D1	D0
Closed caption	6F	CCEN1	CCEN0	0	SCCLN4	SCCLN3	SCCLN2	SCCLN1	SCCLN0
RCV2 output start	70	RCV2S7	RCV2S6	RCV2S5	RCV2S4	RCV2S3	RCV2S2	RCV2S1	RCV2S0
RCV2 output end	71	RCV2E7	RCV2E6	RCV2E5	RCV2E4	RCV2E3	RCV2E2	RCV2E1	RCV2E0
MSBs RCV2 output	72	0	RCV2E10	RCV2E9	RCV2E8	0	RCV2S10	RCV2S9	RCV2S8
Null	73	0	0	0	0	0	0	0	0
Null	74	0	0	0	0	0	0	0	0
Null	75	0	0	0	0	0	0	0	0
Null	76	0	0	0	0	0	0	0	0
Null	77	0	0	0	0	0	0	0	0
Null	78	0	0	0	0	0	0	0	0
Null	79	0	0	0	0	0	0	0	0
First active line	7A	FAL7	FAL6	FAL5	FAL4	FAL3	FAL2	FAL1	FAL0
Last active line	7B	LAL7	LAL6	LAL5	LAL4	LAL3	LAL2	LAL1	LAL0
MSBs vertical	7C	0	LAL8	0	FAL8	0	0	0	0
Null	7D	0	0	0	0	0	0	0	0
Null	7E	0	0	0	0	0	0	0	0
Null	7F	0	0	0	0	0	0	0	0

Note

1. All bits marked 0 must be programmed to zero.

I²C-bus format

Table 4 I²C-bus address; see Table 5

S	SLAVE ADDRESS	ACK	SUBADDRESS	ACK	DATA 0	ACK	--------	DATA n	ACK	P

Table 5 Explanation of Table 4

PART	DESCRIPTION
S	START condition
Slave address	1 0 0 0 1 0 0 X or 1 0 0 0 1 1 0 X (note 1)
ACK	acknowledge, generated by the slave
Subaddress (note 2)	subaddress byte
DATA	data byte
--------	continued data bytes and ACKs
P	STOP condition

Notes

1. X is the read/write control bit; X = logic 0 is order to write; X = logic 1 is order to read, no subaddressing with read.
2. If more than 1 byte DATA is transmitted, then auto-increment of the subaddress is performed.

Slave Receiver

Table 6 Subaddress 3A

DATA BYTE	LOGIC LEVEL	DESCRIPTION
UV2C	0	Cb, Cr data are two's complement.
	1	Cb, Cr data are straight binary. Default after reset.
Y2C	0	Y data is two's complement.
	1	Y data is straight binary. Default after reset.
DEMOFF	0	Y, Cb and Cr for RGB dematrix is active. Default after reset.
	1	Y, Cb and Cr for RGB dematrix is bypassed.
SYMP	0	Horizontal and vertical trigger is taken from RCV2 and RCV1 respectively. Default after reset.
	1	Horizontal and vertical trigger is decoded out of *"CCIR 656"* compatible data at MP port.
YC_EN	0	Output of CVBS and RGB signals. Default after reset.
	1	Output of Y, C, and CVBS, CVBS signals.
CBENB	0	Data from input ports is encoded. Default after reset.
	1	Colour bar with fixed colours is encoded. The LUTs are read in upward order from index 0 to index 7.

Table 7 Subaddress 5A

DATA BYTE	DESCRIPTION	VALUE	RESULT
CHPS	phase of encoded colour subcarrier (including burst) relative to horizontal sync. Can be adjusted in steps of 360/256 degrees	tbf	PAL-B/G and data from input ports
		tbf	PAL-B/G and data from look-up table
		tbf	NTSC-M and data from input ports
		tbf	NTSC-M and data from look-up table

Table 8 Subaddress 5B and 5D

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
GAINU	variable gain for Cb signal; input representation accordance with *"CCIR 601"*	white-to-black = 92.5 IRE[1]	
		GAINU = 0	output subcarrier of U contribution = 0
		GAINU = 118 (76H)	output subcarrier of U contribution = nominal
		white-to-black = 100 IRE[2]	
		GAINU = 0	output subcarrier of U contribution = 0
		GAINU = 125 (7DH)	output subcarrier of U contribution = nominal

Notes

1. GAINU = –2.17 × nominal to +2.16 × nominal.
2. GAINU = –2.05 × nominal to +2.04 × nominal.

Table 9 Subaddress 5C and 5E

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
GAINV	variable gain for Cr signal; input representation accordance with *"CCIR 601"*	white-to-black = 92.5 IRE[1]	
		GAINV = 0	output subcarrier of V contribution = 0
		GAINV = 165 (A5H)	output subcarrier of V contribution = nominal
		white-to-black = 100 IRE[2]	
		GAINV = 0	output subcarrier of V contribution = 0
		GAINV = 175 (AFH)	output subcarrier of V contribution = nominal

Notes

1. GAINV = –1.55 × nominal to +1.55 × nominal.
2. GAINV = –1.46 × nominal to +1.46 × nominal.

Table 10 Subaddress 5D

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
BLCKL	variable black level; input representation accordance with *"CCIR 601"*	white-to-sync = 140 IRE[1]	
		BLCKL = 0	output black level = 24 IRE
		BLCKL = 63 (3FH)	output black level = 49 IRE
		white-to-sync = 143 IRE[2]	
		BLCKL = 0	output black level = 24 IRE
		BLCKL = 63 (3FH)	output black level = 50 IRE

Notes

1. Output black level/IRE = BLCKL × 25/63 + 24; recommended value: BLCKL = 60 (3CH) normal.
2. Output black level/IRE = BLCKL × 26/63 + 24; recommended value: BLCKL = 45 (2DH) normal.

Table 11 Subaddress 5E

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
BLNNL	variable blanking level	white-to-sync = 140 IRE[1]	
		BLNNL = 0	output blanking level = 17 IRE
		BLNNL = 63 (3FH)	output blanking level = 42 IRE
		white-to-sync = 143 IRE[2]	
		BLNNL = 0	output blanking level = 17 IRE
		BLNNL = 63 (3FH)	output blanking level = 43 IRE
DECTYP	RTCI	logic 0	real time control input from SAA7151B
		logic 1	real time control input from SAA7111

Notes

1. Output black level/IRE = BLNNL × 25/63 + 17; recommended value: BLNNL = 58 (3AH) normal.
2. Output black level/IRE = BLNNL × 26/63 + 17; recommended value: BLNNL = 63 (3FH) normal.

Table 12 Subaddress 5F

DATA BYTE	DESCRIPTION
BLNVB	variable blanking level during vertical blanking interval is typically identical to value of BLNNL

Table 13 Subaddress 61

DATA BYTE	LOGIC LEVEL	DESCRIPTION
FISE	0	864 total pixel clocks per line; default after reset
	1	858 total pixel clocks per line
PAL	0	NTSC encoding (non-alternating V component)
	1	PAL encoding (alternating V component); default after reset
SCBW	0	enlarged bandwidth for chrominance encoding (for overall transfer characteristic of chrominance in baseband representation see Figs 7 and 8)
	1	standard bandwidth for chrominance encoding (for overall transfer characteristic of chrominance in baseband representation see Figs 7 and 8); default after reset
YGS	0	luminance gain for white – black 100 IRE; default after reset
	1	luminance gain for white – black 92.5 IRE including 7.5 IRE set-up of black
INPI	0	PAL switch phase is nominal; default after reset
	1	PAL switch phase is inverted compared to nominal
DOWNA	0	DACs for G and B (Y and Cb or CVBS and CVBS) in normal operational mode; default after reset
	1	DACs for G and B (Y and Cb or CVBS and CVBS) forced to lowest output voltage
DOWNB	0	DACs for CVBS and R (CVBS and Cr or VBS and C) in normal operational mode; default after reset
	1	DACs for CVBS and R (CVBS and Cr or VBS and C) forced to lowest output voltage

Table 14 Subaddress 62A

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
BSTA	amplitude of colour burst; input representation in accordance with *"CCIR 601"*	white-to-black = 92.5 IRE; burst = 40 IRE; NTSC encoding BSTA = 0 to 1.25 × nominal	recommended value: BSTA = 102 (66H
		white-to-black = 92.5 IRE; burst = 40 IRE; PAL encoding BSTA = 0 to 1.76 × nominal	recommended value: BSTA = 72 (48H)
		white-to-black = 100 IRE; burst = 43 IRE; NTSC encoding BSTA = 0 to 1.20 × nominal	recommended value: BSTA = 106 (6AH)
		white-to-black = 100 IRE; burst = 43 IRE; PAL encoding BSTA = 0 to 1.67 × nominal	recommended value: BSTA = 75 (4BH)

Table 15 Subaddress 62B

DATA BYTE	LOGIC LEVEL	DESCRIPTION
RTCE	0	no real time control of generated subcarrier frequency
	1	real time control of generated subcarrier frequency through SAA7151B or SAA7111 (timing see Fig.15)

Table 16 Subaddress 63 to 66 (four bytes to program subcarrier frequency)

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
FSC0 to FSC3	f_{fsc} = subcarrier frequency (in multiples of line frequency); f_{llc} = clock frequency (in multiples of line frequency)	$FSC = round\left(\frac{f_{fsc}}{f_{llc}} \times 2^{32}\right)$ see note 1	FSC3 = most significant byte FSC0 = least significant byte

Note

1. Examples:
   a) NTSC-M: f_{fsc} = 227.5, f_{llc} = 1716 → FSC = 569408543 (21F07C1FH).
   b) PAL-B/G: f_{fsc} = 283.7516, f_{llc} = 1728 → FSC = 705268427 (2A098ACBH).

Table 17 Subaddress 67 to 6A

DATA BYTE	DESCRIPTION	REMARK
L21O0	first byte of captioning data, odd field	LSB of the respective bytes are encoded immediately after run-in and framing code, the MSBs of the respective bytes have to carry the parity bit, in accordance with the definition of Line 21 encoding format
L21O1	second byte of captioning data, odd field	
L21E0	first byte of extended data, even field	
L21E1	second byte of extended data, even field	

Table 18 Subaddress 6B

DATA BYTE	LOGIC LEVEL	DESCRIPTION
PRCV2	0	polarity of RCV2 as output is active HIGH, rising edge is taken when input, respectively; default after reset
	1	polarity of RCV2 as output is active LOW, falling edge is taken when input, respectively
ORCV2	0	pin RCV2 is switched to input; default after reset
	1	pin RCV2 is switched to output
CBLF	0	if ORCV2 = HIGH, pin RCV2 provides an HREF signal (Horizontal Reference pulse that is defined by RCV2S and RCV2E, also during vertical blanking Interval); default after reset if ORCV2 = LOW and bit SYMP = LOW, signal input to RCV2 is used for horizontal synchronization only (if TRCV2 = HIGH); default after reset
	1	if ORCV2 = HIGH, pin RCV2 provides a 'Composite-Blanking-Not' signal, this is a reference pulse that is defined by RCV2S and RCV2E, excluding Vertical Blanking Interval, which is defined by FAL and LAL if ORCV2 = LOW and bit SYMP = LOW, signal input to RCV2 is used for horizontal synchronization (if TRCV2 = HIGH) and as an internal blanking signal
PRCV1	0	polarity of RCV1 as output is active HIGH, rising edge is taken when input; default after reset
	1	polarity of RCV1 as output is active LOW, falling edge is taken when input
ORCV1	0	pin RCV1 is switched to input; default after reset
	1	pin RCV1 is switched to output
TRCV2	0	horizontal synchronization is taken from RCV1 port (at bit SYMP = LOW) or from decoded frame sync of *"CCIR 656"* input (at bit SYMP = HIGH); default after reset
	1	horizontal synchronization is taken from RCV2 port (at bit SYMP = LOW)
SRCV1	–	defines signal type on pin RCV1; see Table 19

Table 19 Logic levels and function of SRCV1

DATA BYTE		AS OUTPUT	AS INPUT	FUNCTION
SRCV11	SRCV10			
0	0	VS	VS	vertical sync each field; default after reset
0	1	FS	FS	frame sync (odd/even)
1	0	FSEQ	FSEQ	field sequence, vertical sync every fourth field (PAL = 0) or eighth field (PAL = 1)
1	1	not applicable	not applicable	–

Table 20 Subaddress 6C and 6D

DATA BYTE	DESCRIPTION
HTRIG	sets the horizontal trigger phase related to signal on RCV1 or RCV2 input (or to decoded *"CCIR 656"* data) values above 1715 (FISE = 1) or 1727 (FISE = 0) are not allowed increasing HTRIG decreases delays of all internally generated timing signals reference mark: analog output horizontal sync (leading slope) coincides with active edge of RCV used for triggering at HTRIG = tbfH (tbfH)

Table 21 Subaddress 6D

DATA BYTE	DESCRIPTION
VTRIG	sets the vertical trigger phase related to signal on RCV1 input (or to decoded *"CCIR 656"* data) increasing VTRIG decreases delays of all internally generated timing signals, measured in half lines variation range of VTRIG = 0 to 31 (1FH)

Table 22 Subaddress 6E

DATA BYTE	LOGIC LEVEL	DESCRIPTION
SBLBN	0	vertical blanking is defined by programming of FAL and LAL; default after reset
	1	vertical blanking is forced in accordance with *"CCIR 624"* (50 Hz) or *"RS170A"* (60 Hz)
PHRES	–	selects the phase reset mode of the colour subcarrier generator; see Table 23
FLC	–	field length control; see Table 24

Table 23 Logic levels and function of PHRES

DATA BYTE		FUNCTION
PHRES1	PHRES0	
0	0	no reset or reset via RTCI from SAA7111 if bit RTCE = 1; default after reset
0	1	reset every two lines
1	0	reset every eight fields
1	1	reset every four fields

Table 24 Logic levels and function of FLC

DATA BYTE		FUNCTION
FLC1	FLC0	
0	0	interlaced 312.5 lines/field at 50 Hz, 262.5 lines/field at 60 Hz; default after reset
0	1	non-interlaced 312 lines/field at 50 Hz, 262 lines/field at 60 Hz
1	0	non-interlaced 313 lines/field at 50 Hz, 263 lines/field at 60 Hz
1	1	non-interlaced 313 lines/field at 50 Hz, 263 lines/field at 60 Hz

Table 25 Subaddress 6F

DATA BYTE	DESCRIPTION
CCEN	enables individual Line 21 encoding; see Table 26
SCCLN	selects the actual line, where closed caption or extended data are encoded line = (SCCLN + 4) for M-systems line = (SCCLN + 1) for other systems

Table 26 Logic levels and function of CCEN

DATA BYTE		FUNCTION
CCEN1	CCEN0	
0	0	line 21 encoding off
0	1	enables encoding in field 1 (odd)
1	0	enables encoding in field 2 (even)
1	1	enables encoding in both fields

Table 27 Subaddress 70 to 72

DATA BYTE	DESCRIPTION
RCV2S	start of output signal on RCV2 pin values above 1715 (FISE = 1) or 1727 (FISE = 0) are not allowed first active pixel at analog outputs (corresponding input pixel coinciding with RCV2) at RCV2S = tbfH (tbfH)
RCV2E	end of output signal on RCV2 pin values above 1715 (FISE = 1) or 1727 (FISE = 0) are not allowed last active pixel at analog outputs (corresponding input pixel coinciding with RCV2) at RCV2E = tbfH (tbfH)

Table 28 Subaddress 7A to 7C

DATA BYTE	DESCRIPTION
FAL	first active line = FAL + 4 for M-systems, = FAL + 1 for other systems, measured in lines FAL = 0 coincides with the first field synchronization pulse
LAL	last active line = LAL + 3 for M-systems, = LAL for other system, measured in lines LAL = 0 coincides with the first field synchronization pulse

SUBADDRESSES

In subaddresses 5B, 5C, 5D, 5E and 62 all IRE values are rounded up.

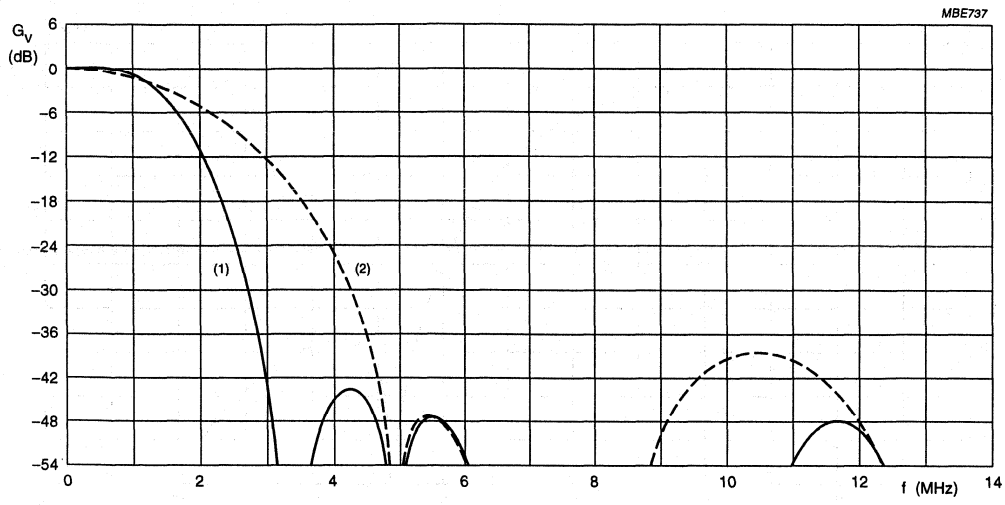
Slave Transmitter

Table 29 Slave transmitter (slave address 89H or 8DH)

REGISTER FUNCTION	SUBADDRESS	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
Status byte	–	VER2	VER1	VER0	CCRDO	CCRDE	0	FSEQ	O_E

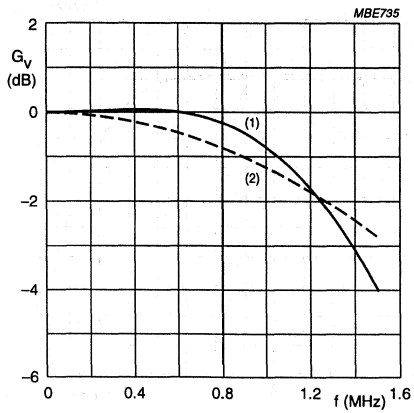
Table 30 No subaddress

DATA BYTE	LOGIC LEVEL	DESCRIPTION
VER	–	Version identification of the device. It will be changed with all versions of the IC that have different programming models. Current Version is 100 binary.
CCRDO	1	Closed caption bytes of the odd field have been encoded.
	0	The bit is reset after information has been written to the subaddresses 67 and 68. It is set immediately after the data has been encoded.
CCRDE	1	Closed caption bytes of the even field have been encoded.
	0	The bit is reset after information has been written to the subaddresses 69 and 6A. It is set immediately after the data has been encoded.
FSEQ	1	During first field of a sequence (repetition rate: NTSC = 4 fields, PAL = 8 fields.
	0	Not first field of a sequence.
O_E	1	During even field.
	0	During odd field.



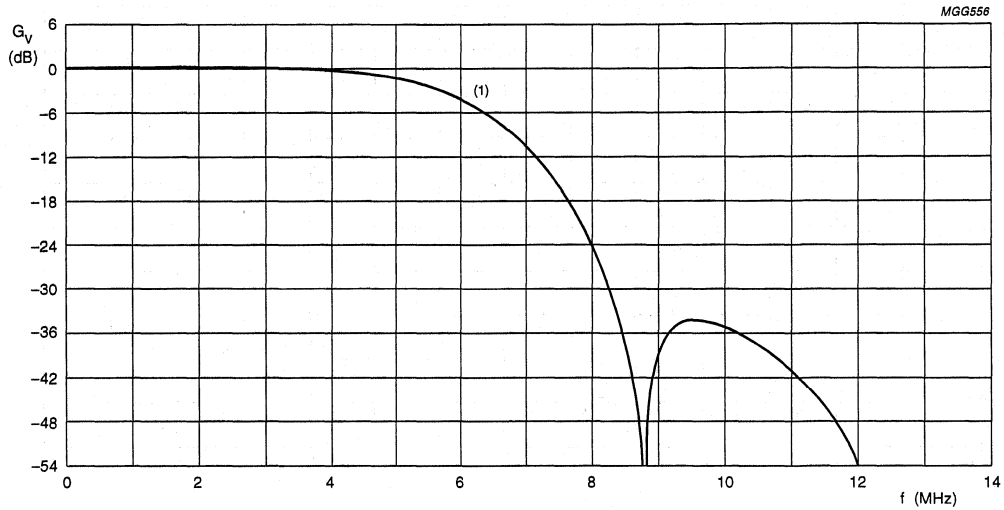
(1) SCBW = 1.
(2) SCBW = 0.

Fig.7 Chrominance transfer characteristic 1.



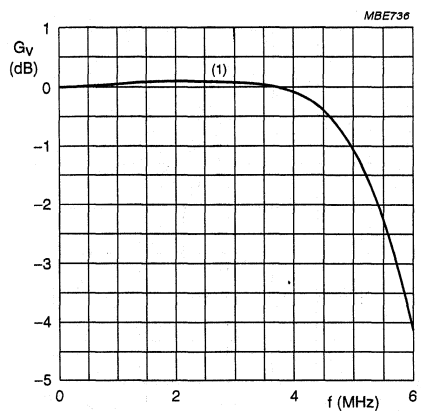
(1) SCBW = 1.
(2) SCBW = 0.

Fig.8 Chrominance transfer characteristic 2.



(1) Total luminance of Y and CVBS.

Fig.9 Luminance transfer characteristic 1.



(1) Detailed luminance of Y and CVBS.

Fig.10 Luminance transfer characteristic 2.

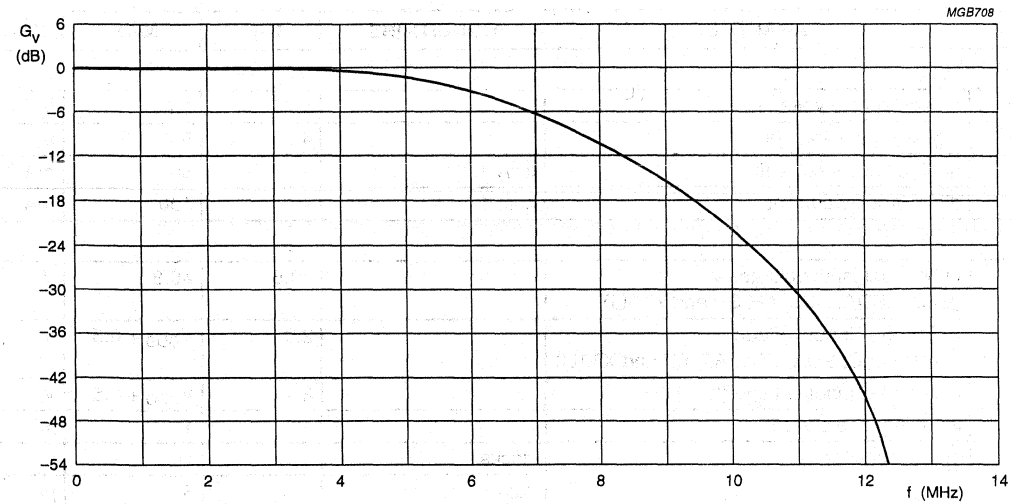


Fig.11 Luminance transfer characteristic in RGB.

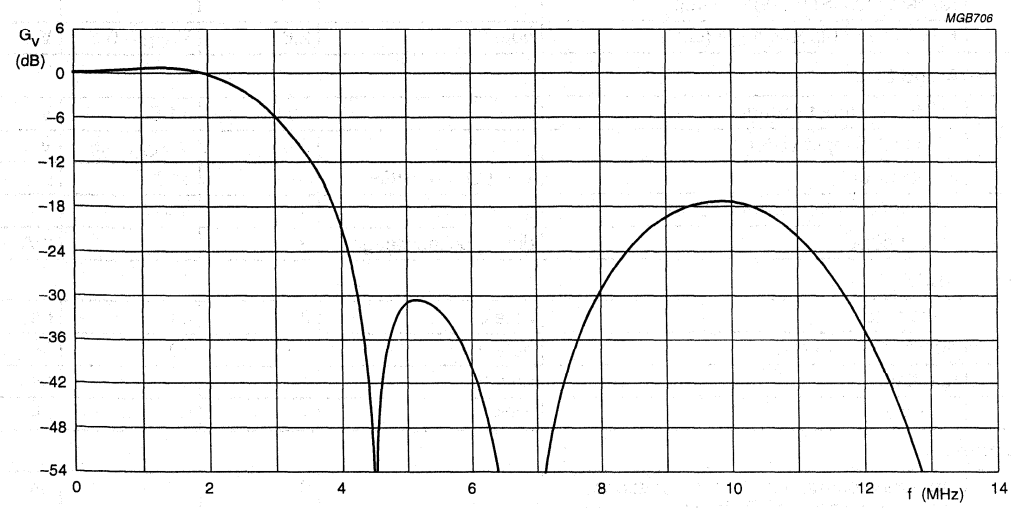


Fig.12 Colour difference transfer characteristic in RGB.

CHARACTERISTICS

V_{DDD} = 4.75 to 5.25 V; T_{amb} = 0 to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Supplies					
V_{DDA}	analog supply voltage		4.75	5.25	V
V_{DDD}	digital supply voltage		4.75	5.25	V
I_{DDA}	analog supply current	note 1	–	60	mA
I_{DDD}	digital supply current	note 1	–	100	mA
Inputs					
V_{IL}	LOW level input voltage (except SDA, SCL, AP, SP and XTALI)		−0.5	+0.8	V
V_{IH}	HIGH level input voltage (except LLC, SDA, SCL, AP, SP and XTALI)		2.0	V_{DDD} + 0.5	V
	HIGH level input voltage (LLC)		2.4	V_{DDD} + 0.5	V
I_{LI}	input leakage current		–	1	µA
C_i	input capacitance	clocks	–	10	pF
		data	–	8	pF
		I/Os at high impedance	–	8	pF
Outputs					
V_{OL}	LOW level output voltage (except SDA and XTALO)	note 2	0	0.6	V
V_{OH}	HIGH level output voltage (except LLC, SDA, and XTALO)	note 2	2.4	V_{DDD} + 0.5	V
	HIGH level output voltage (LLC)	note 2	2.6	V_{DDD} + 0.5	V
I²C-bus; SDA and SCL					
V_{IL}	LOW level input voltage		−0.5	+1.5	V
V_{IH}	HIGH level input voltage		3.0	V_{DDD} + 0.5	V
I_i	input current	V_i = LOW or HIGH	−10	+10	µA
V_{OL}	LOW level output voltage (SDA)	I_{OL} = 3 mA	–	0.4	V
I_o	output current	during acknowledge	3	–	mA
Clock timing (LLC)					
T_{LLC}	cycle time	note 3	34	41	ns
δ	duty factor t_{HIGH}/T_{LLC}	note 4	40	60	%
t_r	rise time	note 3	–	5	ns
t_f	fall time	note 3	–	6	ns
Input timing					
$t_{SU;DAT}$	input data set-up time (any other except CDIR, SCL, SDA, $\overline{\text{RESET}}$, AP and SP)		6	–	ns
$t_{HD;DAT}$	input data hold time (any other except CDIR, SCL, SDA, $\overline{\text{RESET}}$, AP and SP)		3	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Crystal oscillator					
f_n	nominal frequency (usually 27 MHz)	3rd harmonic	–	30	MHz
$\Delta f/f_n$	permissible deviation of nominal frequency	note 5	–50	+50	10^{-6}
CRYSTAL SPECIFICATION					
T_{amb}	operating ambient temperature		0	70	°C
C_L	load capacitance		8	–	pF
R_S	series resistance		–	80	Ω
C_1	motional capacitance (typical)		1.5 – 20%	1.5 + 20%	fF
C_0	parallel capacitance (typical)		3.5 – 20%	3.5 + 20%	pF
Data and reference signal output timing					
C_L	output load capacitance		7.5	40	pF
t_h	output hold time		4	–	ns
t_d	output delay time		–	25	ns
CHROMA, Y, CVBS and RGB outputs					
$V_{o(p-p)}$	output signal voltage (peak-to-peak value)	note 6	1.9	2.1	V
R_{int}	internal serial resistance		18	35	Ω
R_L	output load resistance		80	–	Ω
B	output signal bandwidth of DACs	–3 dB	10	–	MHz
ILE	LF integral linearity error of DACs		–	±4	LSB
DLE	LF differential linearity error of DACs		–	±1	LSB

Notes

1. At maximum supply voltage with highly active input signals.
2. The levels have to be measured with load circuits of 1.2 kΩ to 3.0 V (standard TTL load) and C_L = 25 pF.
3. The data is for both input and output direction.
4. With LLC in input mode. In output mode, with a crystal connected to XTALO/XTALI duty factor is typically 50%.
5. If an internal oscillator is used, crystal deviation of nominal frequency is directly proportional to the deviation of subcarrier frequency and line/field frequency.
6. For full digital range, without load, V_{DDA} = 5.0 V. The typical voltage swing is 2.0 V, the typical minimum output voltage (digital zero at DAC) is 0.2 V.

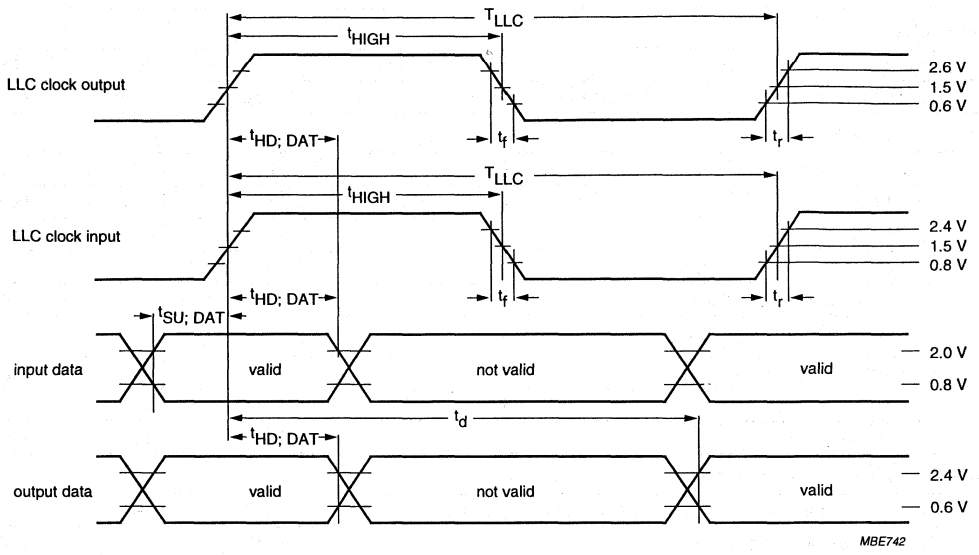
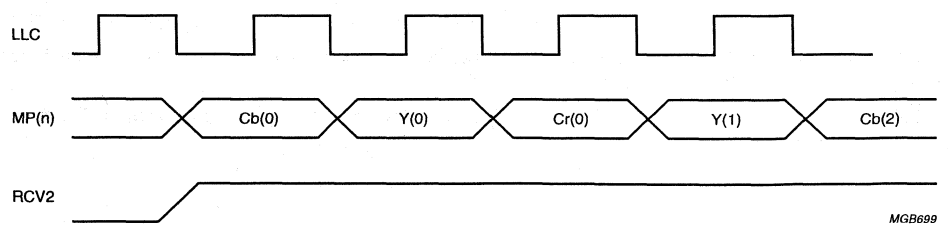
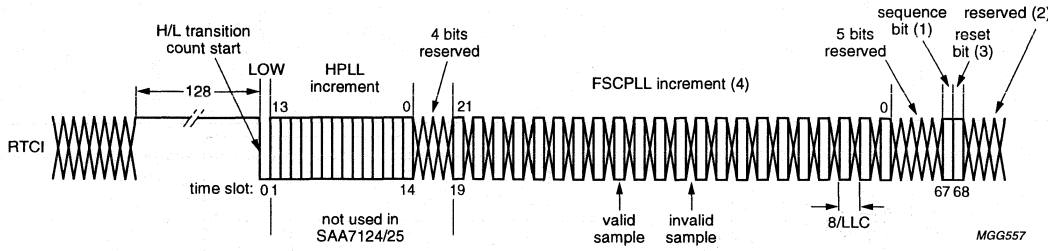


Fig.13 Clock data timing.



The data demultiplexing phase is coupled to the internal horizontal phase.
The phase of the RCV2 signal is programmed to 0F2H (110H for 50 Hz) in this example in output mode (RCV2S).

Fig.14 Functional timing.



(1) Sequence bit:
PAL = logic 0 then (R – Y) line normal; PAL = logic 1 then (R – Y) line inverted.
NTSC = logic 0 then no change.

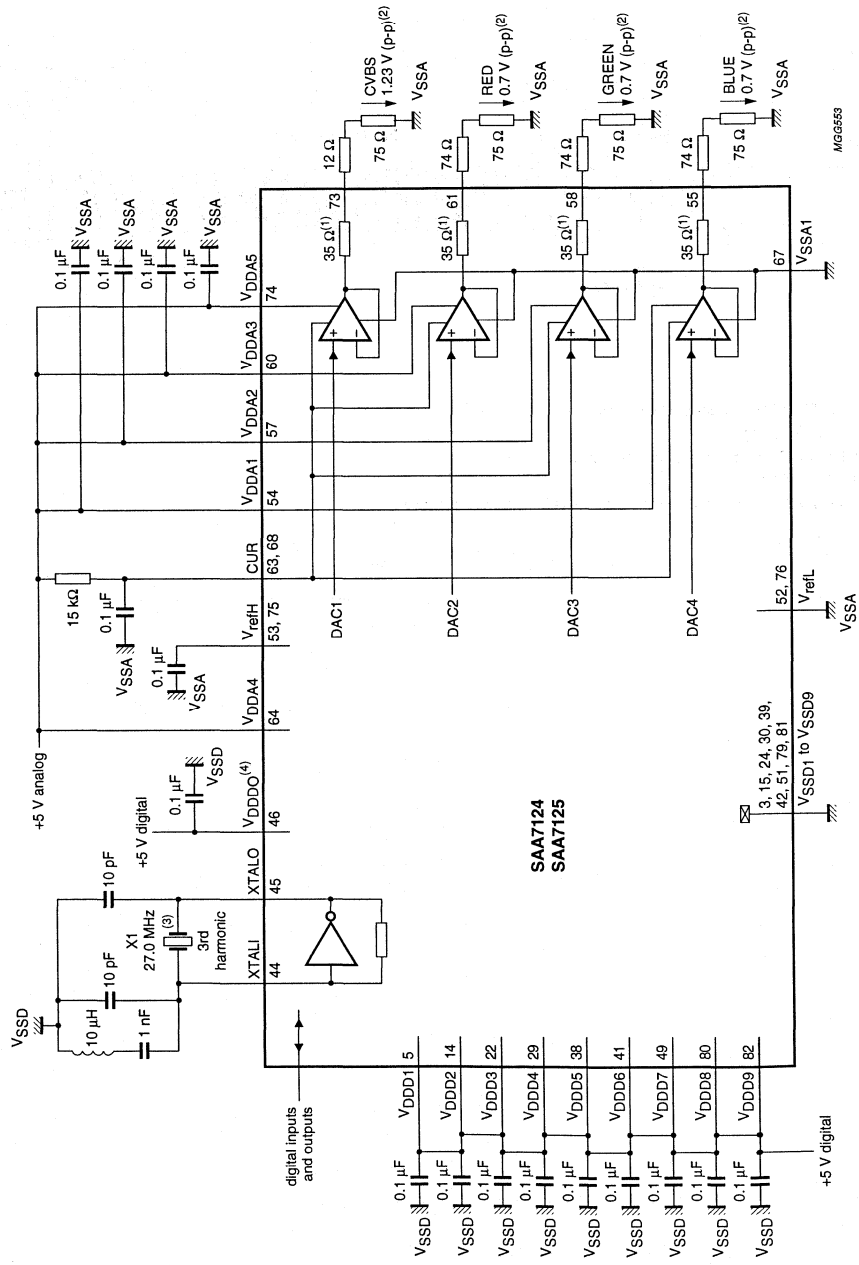
(2) Reserved bits: 235 with 50 Hz systems; 232 with 60 Hz systems.

(3) Only from SAA7111 decoder.

(4) SAAA7111 provides (22 : 0) bits, resulting in 3 reserved bits before sequence bit.

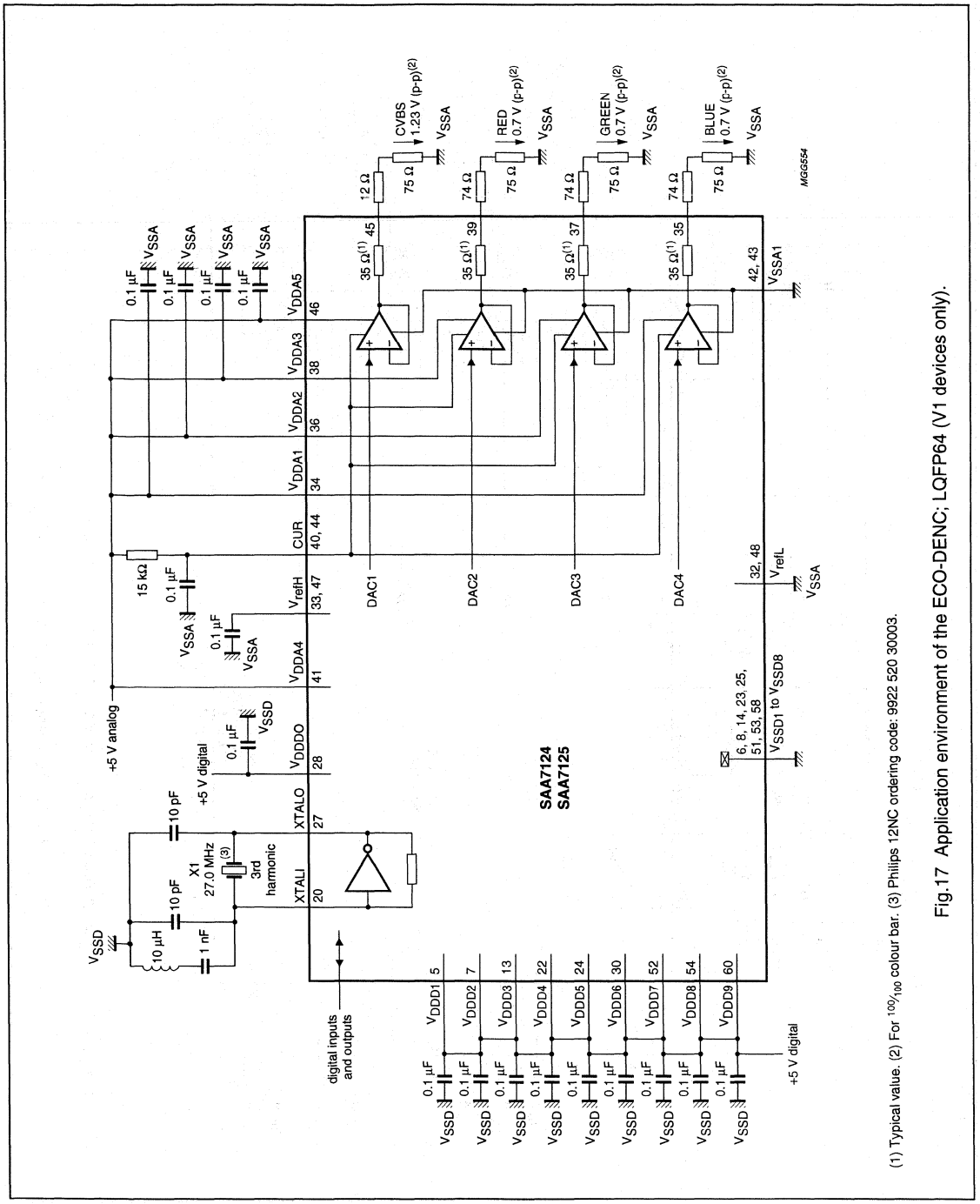
Fig.15 RTCI timing.

APPLICATION INFORMATION



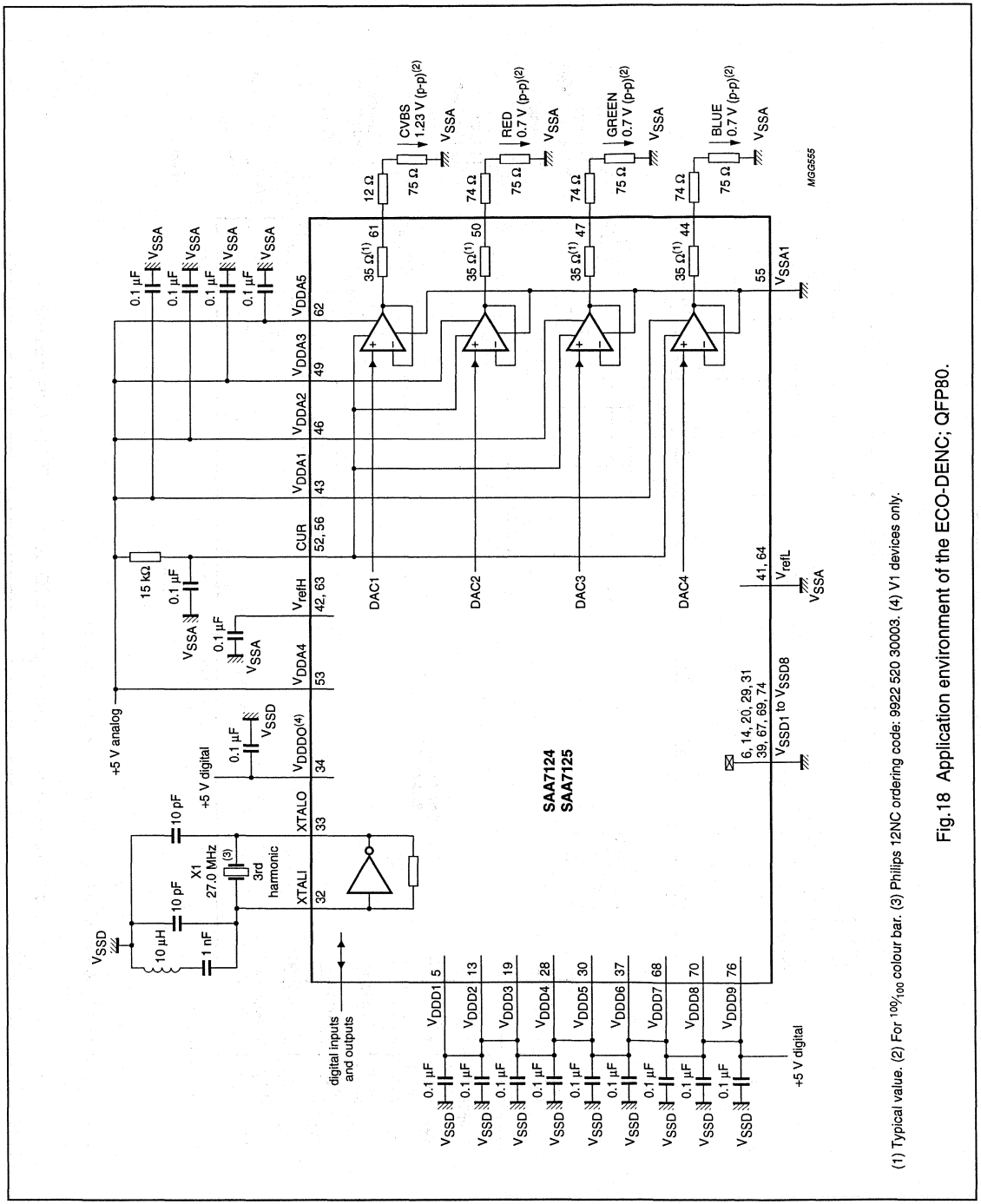
(1) Typical value. (2) For 100/100 colour bar. (3) Philips 12NC ordering code: 9922 520 30003. (4) V1 devices only.

Fig.16 Application environment of the ECO-DENC; PLCC84.



(1) Typical value. (2) For $^{100}/_{100}$ colour bar. (3) Philips 12NC ordering code: 9922 520 30003.

Fig.17 Application environment of the ECO-DENC; LQFP64 (V1 devices only).



(1) Typical value. (2) For $^{100}/_{100}$ colour bar. (3) Philips 12NC ordering code: 9922 520 30003. (4) V1 devices only.

Fig.18 Application environment of the ECO-DENC; QFP80.

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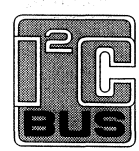


1 FEATURES

- Scaling of video pictures down to randomly sized windows
- Horizontal upscaling (zoom)
- Two dimensional phase-correct data processing for improved signal quality of scaled data, especially for compression applications
- Processing of a maximum of 2047 active samples per line (V-processing in bypass) and 2047 active lines per frame
- 16-bit YUV data input port
- Bidirectional expansion port with full duplex functionality (D1) or 16-bit YUV input/output
- Discontinuous data stream supported
- Field-wise switching between two data sources
- Two independent I²C-bus programming sets
- Brightness, contrast and saturation controls for scaled outputs
- Chroma key (α generation)
- YUV-to-RGB conversion including anti-gamma correction for RGB
- 16-word FIFO register for 32-bit output data
- Output configurable for 32, 24, 16 and 8-bit video data
- Scaled 16-bit 4 : 2 : 2 YUV output
- Scaled 15-bit RGB (5, 5, 5) + α with dither and 24-bit RGB (8, 8, 8) + α output
- Scaled 8-bit monochrome output
- Four independent user configurable general purpose I/O pins
- Low power consumption in I²C-bus controlled pseudo sleep mode
- **Support of 5 V (SAA7140A) and pure 3.3 V (SAA7140B) signalling environment.**

2 GENERAL DESCRIPTION

The SAA7140A and SAA7140B are CMOS High Performance Scaler (HPS) and is a highly integrated circuit designed for use in DeskTop Video (DTV) applications. The devices resample digital video signals using two dimensional phase-correct interpolation in order to display it in an arbitrarily sized window.

The SAA7140A fits perfectly into a 5 V signal environment and requires two different supply voltages (5 V and 3.3 V). The SAA7140B is a pure 3.3 V design and therefore has only 3.3 V supply pins. With respect to functions and programming, both devices are identical.

The devices incorporate additional functions such as control of brightness, saturation, contrast, chroma key generation, YUV-to-RGB conversion, compensation of gamma precorrection, dithering and choice of several output formats.

The SAA7140A and SAA7140B accepts data from 1 or 2 input signal sources, via it's 16-bit YUV input port and/or the bidirectional expansion port. They deliver scaled data on the 32-bit VRO output port and, if selected, also on the bidirectional expansion port. A synchronous (transparent) together with an asynchronous (burst) data transfer mode is supported at the 32-bit VRO port.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7140A	LQFP128	plastic low profile quad flat package; 128 leads; body 14 × 20 × 1.4 mm	SOT425-1
SAA7140B	LQFP128	plastic low profile quad flat package; 128 leads; body 14 × 20 × 1.4 mm	SOT425-1

4 BLOCK DIAGRAMS

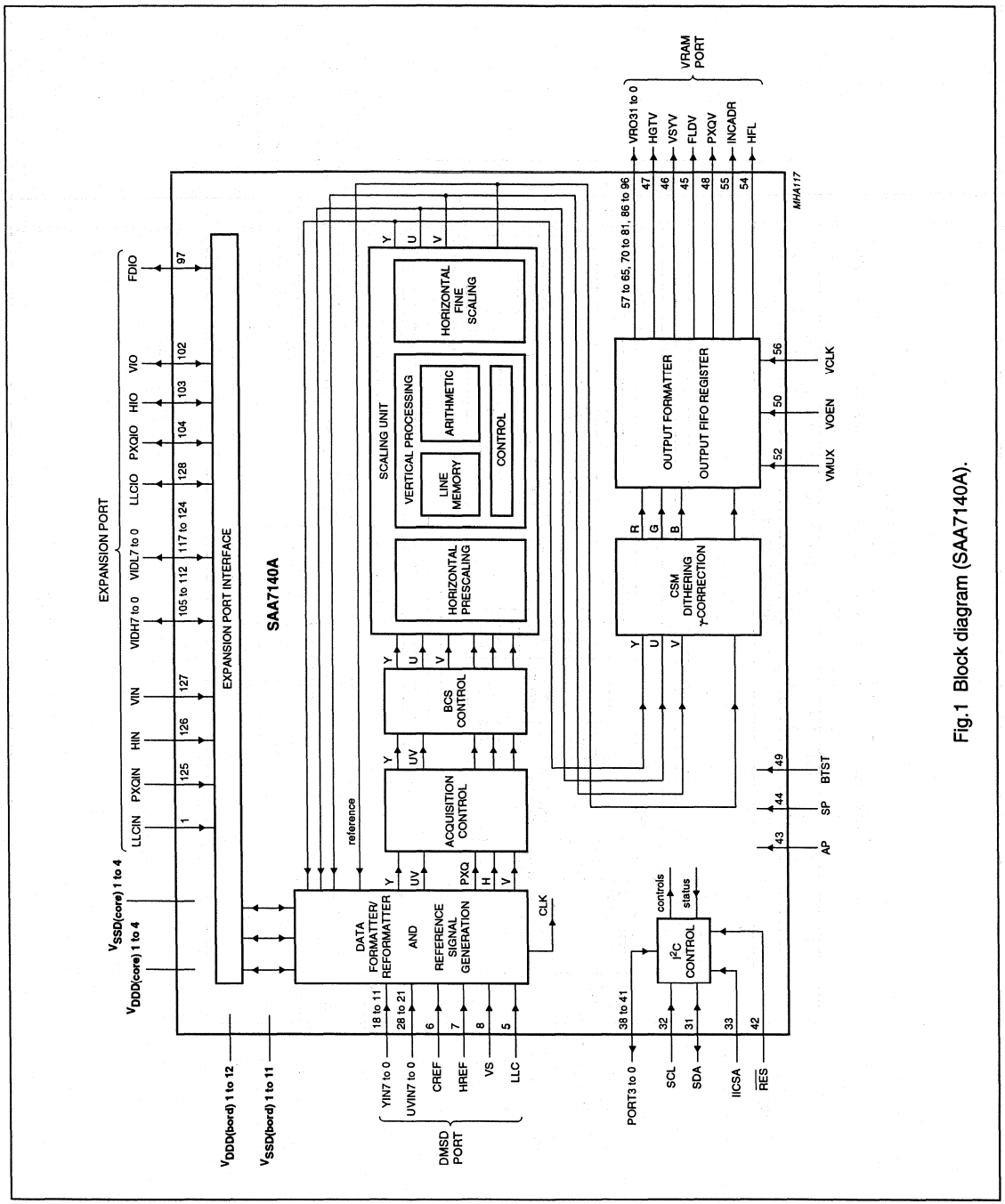


Fig.1 Block diagram (SAA7140A).

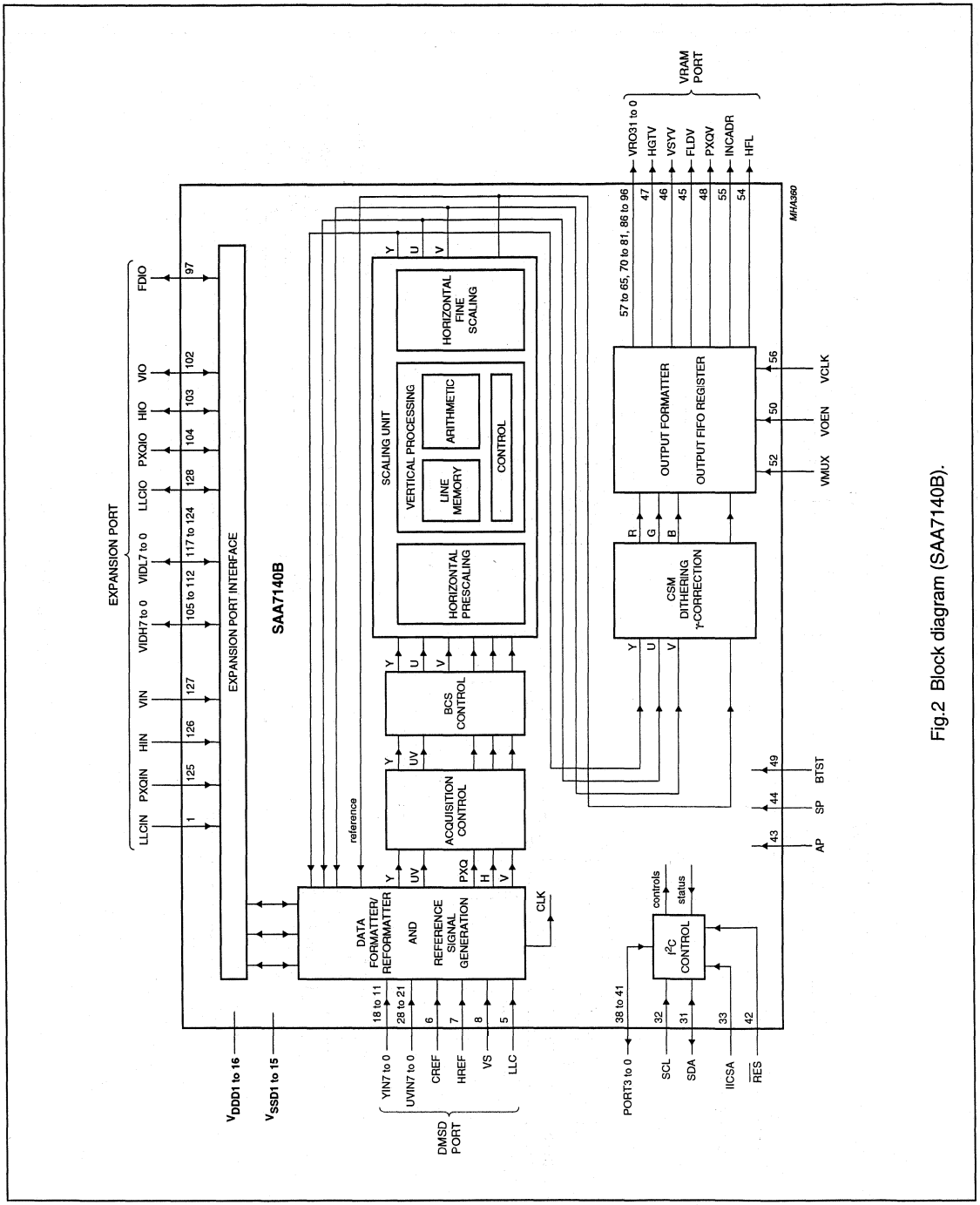


Fig.2 Block diagram (SAA7140B).

5 PINNING (SAA7140A)

SYMBOL	PIN	I/O	DESCRIPTION
LLCIN	1	I	line-locked system clock input; expansion port
$V_{DDD(bord)1}$	2	–	digital border supply voltage 1 (+5 V)
$V_{SSD(bord)1}$	3	–	digital border ground 1 (0 V)
$V_{DDD(bord)2}$	4	–	digital border supply voltage 2 (+5 V)
LLC	5	I	line-locked system clock input, maximum 32 MHz (2 × pixel rate); DMSD port
CREF	6	I	clock qualifier input (HIGH indicates valid input data YUV on DMSD port)
HREF	7	I	horizontal reference input signal; DMSD port
VS	8	I	vertical sync input signal; DMSD port
$V_{DDD(core)1}$	9	–	digital core supply voltage 1 (+3.3 V)
$V_{SSD(bord)2}$	10	–	digital border ground 2 (0 V)
YIN0	11	I	luminance input data (bit 0); DMSD port
YIN1	12	I	luminance input data (bit 1); DMSD port
YIN2	13	I	luminance input data (bit 2); DMSD port
YIN3	14	I	luminance input data (bit 3); DMSD port
YIN4	15	I	luminance input data (bit 4); DMSD port
YIN5	16	I	luminance input data (bit 5); DMSD port
YIN6	17	I	luminance input data (bit 6); DMSD port
YIN7	18	I	luminance input data (bit 7); DMSD port
$V_{DDD(bord)3}$	19	–	digital border supply voltage 3 (+5 V)
$V_{SSD(core)1}$	20	–	digital core ground 1 (0 V)
UVIN0	21	I	time-multiplexed colour-difference input data (bit 0); DMSD port
UVIN1	22	I	time-multiplexed colour-difference input data (bit 1); DMSD port
UVIN2	23	I	time-multiplexed colour-difference input data (bit 2); DMSD port
UVIN3	24	I	time-multiplexed colour-difference input data (bit 3); DMSD port
UVIN4	25	I	time-multiplexed colour-difference input data (bit 4); DMSD port
UVIN5	26	I	time-multiplexed colour-difference input data (bit 5); DMSD port
UVIN6	27	I	time-multiplexed colour-difference input data (bit 6); DMSD port
UVIN7	28	I	time-multiplexed colour-difference input data (bit 7); DMSD port
$V_{DDD(bord)4}$	29	–	digital border supply voltage 4 (+5 V)
$V_{SSD(bord)3}$	30	–	digital border ground 3 (0 V)
SDA	31	I/O	serial data input/output (I^2C-bus)
SCL	32	I	serial clock input (I^2C-bus)
IICSA	33	I	set address input (I^2C-bus)
$V_{DDD(bord)5}$	34	–	digital border supply voltage 5 (+5 V)
$V_{SSD(bord)4}$	35	–	digital border ground 4 (0 V)
$V_{DDD(bord)6}$	36	–	digital border supply voltage 6 (+5 V)
$V_{SSD(bord)5}$	37	–	digital border ground 5 (0 V)
PORT3	38	I/O	general purpose port 3 input/output (set via I^2C-bus)
PORT2	39	I/O	general purpose port 2 input/output (set via I^2C-bus)
PORT1	40	I/O	general purpose port 1 input/output (set via I^2C-bus)

SYMBOL	PIN	I/O	DESCRIPTION
PORT0	41	I/O	general purpose port 0 input/output (set via I^2C-bus)
$\overline{RES}$	42	I	reset input (active LOW for at least 30 clock cycles)
AP	43	I	connected to ground (action pin for testing)
SP	44	I	connected to ground (shift pin for testing)
FLDV	45	O	field identification output signal; VRAM port
VSYV	46	O	vertical sync output signal; VRAM port
HGTV	47	O	horizontal reference output signal; VRAM port
PXQV	48	O	pixel qualifier output signal to mark active pixels of a qualified line; VRAM port
BTST	49	I	connected to ground; BTST = HIGH sets all outputs to high-impedance state (testing)
VOEN	50	I	enable input signal for VRAM port
$V_{DDD(core)2}$	51	–	digital core supply voltage 2 (+3.3 V)
VMUX	52	I	VRAM output multiplexing, control input for the 32 to 16-bit multiplexer
$V_{SSD(core)2}$	53	–	digital core ground 2 (0 V)
HFL	54	O	FIFO half-full flag output signal
INCADR	55	O	line increment/vertical reset control output
VCLK	56	I/O	clock input/output signal for VRAM port
VRO31	57	O	32-bit digital VRAM port output (bit 31)
VRO30	58	O	32-bit digital VRAM port output (bit 30)
VRO29	59	O	32-bit digital VRAM port output (bit 29)
VRO28	60	O	32-bit digital VRAM port output (bit 28)
VRO27	61	O	32-bit digital VRAM port output (bit 27)
VRO26	62	O	32-bit digital VRAM port output (bit 26)
VRO25	63	O	32-bit digital VRAM port output (bit 25)
VRO24	64	O	32-bit digital VRAM port output (bit 24)
VRO23	65	O	32-bit digital VRAM port output (bit 23)
$V_{DDD(bord)7}$	66	–	digital border supply voltage 7 (+5 V)
$V_{SSD(bord)6}$	67	–	digital border ground 6 (0 V)
$V_{DDD(bord)8}$	68	–	digital border supply voltage 8 (+5 V)
$V_{SSD(bord)7}$	69	–	digital border ground 7 (0 V)
VRO22	70	O	32-bit VRAM port output (bit 22)
VRO21	71	O	32-bit VRAM port output (bit 21)
VRO20	72	O	32-bit VRAM port output (bit 20)
VRO19	73	O	32-bit VRAM port output (bit 19)
VRO18	74	O	32-bit VRAM port output (bit 18)
VRO17	75	O	32-bit VRAM port output (bit 17)
VRO16	76	O	32-bit VRAM port output (bit 16)
VRO15	77	O	32-bit VRAM port output (bit 15)
VRO14	78	O	32-bit VRAM port output (bit 14)
VRO13	79	O	32-bit VRAM port output (bit 13)
VRO12	80	O	32-bit VRAM port output (bit 12)

SYMBOL	PIN	I/O	DESCRIPTION
VRO11	81	O	32-bit VRAM port output (bit 11)
$V_{SSD(bord)8}$	82	–	digital border ground 8 (0 V)
$V_{DDD(bord)9}$	83	–	digital border supply voltage 9 (+5 V)
$V_{SSD(core)3}$	84	–	digital core ground 3 (0 V)
$V_{DDD(core)3}$	85	–	digital core supply voltage 3 (+3.3 V)
VRO10	86	O	32-bit VRAM port output (bit 10)
VRO9	87	O	32-bit VRAM port output (bit 9)
VRO8	88	O	32-bit VRAM port output (bit 8)
VRO7	89	O	32-bit VRAM port output (bit 7)
VRO6	90	O	32-bit VRAM port output (bit 6)
VRO5	91	O	32-bit VRAM port output (bit 5)
VRO4	92	O	32-bit VRAM port output (bit 4)
VRO3	93	O	32-bit VRAM port output (bit 3)
VRO2	94	O	32-bit VRAM port output (bit 2)
VRO1	95	O	32-bit VRAM port output (bit 1)
VRO0	96	O	32-bit VRAM port output (bit 0)
FDIO	97	I/O	field identification output signal; 7196 DIR input signal expansion port, I^2C-bus controlled
$V_{DDD(bord)10}$	98	–	digital border supply voltage 10 (+5 V)
$V_{SSD(bord)9}$	99	–	digital border ground 9 (0 V)
$V_{DDD(bord)11}$	100	–	digital border supply voltage 11 (+5 V)
$V_{SSD(bord)10}$	101	–	digital border ground 10 (0 V)
VIO	102	I/O	vertical sync input/output signal; expansion port
HIO	103	I/O	horizontal sync input/output signal; expansion port
PXQIO	104	I/O	pixel qualifier input/output signal to mark valid pixels; expansion port
VIDH7	105	I/O	bidirectional expansion port, high byte (bit 7) in 16-bit mode luminance component Y
VIDH6	106	I/O	bidirectional expansion port, high byte (bit 6) in 16-bit mode luminance component Y
VIDH5	107	I/O	bidirectional expansion port, high byte (bit 5) in 16-bit mode luminance component Y
VIDH4	108	I/O	bidirectional expansion port, high byte (bit 4) in 16-bit mode luminance component Y
VIDH3	109	I/O	bidirectional expansion port, high byte (bit 3) in 16-bit mode luminance component Y
VIDH2	110	I/O	bidirectional expansion port, high byte (bit 2) in 16-bit mode luminance component Y
VIDH1	111	I/O	bidirectional expansion port, high byte (bit 1) in 16-bit mode luminance component Y
VIDH0	112	I/O	bidirectional expansion port, high byte (bit 0) in 16-bit mode luminance component Y
$V_{DDD(bord)12}$	113	–	digital border supply voltage 12 (+5 V)

SYMBOL	PIN	I/O	DESCRIPTION
$V_{SSD(bord)11}$	114	–	digital border ground 11 (0 V)
$V_{DDD(core)4}$	115	–	digital core supply voltage 4 (+3.3 V)
$V_{SSD(core)4}$	116	–	digital core ground 4 (0 V)
VIDL7	117	I/O	bidirectional expansion port, low byte (bit 7) in 16-bit mode time-multiplexed colour-difference components U and V
VIDL6	118	I/O	bidirectional expansion port, low byte (bit 6) in 16-bit mode time-multiplexed colour-difference components U and V
VIDL5	119	I/O	bidirectional expansion port, low byte (bit 5) in 16-bit mode time-multiplexed colour-difference components U and V
VIDL4	120	I/O	bidirectional expansion port, low byte (bit 4) in 16-bit mode time-multiplexed colour-difference components U and V
VIDL3	121	I/O	bidirectional expansion port, low byte (bit 3) in 16-bit mode time-multiplexed colour-difference components U and V
VIDL2	122	I/O	bidirectional expansion port, low byte (bit 2) in 16-bit mode time-multiplexed colour-difference components U and V
VIDL1	123	I/O	bidirectional expansion port, low byte (bit 1) in 16-bit mode time-multiplexed colour-difference components U and V
VIDL0	124	I/O	bidirectional expansion port, low byte (bit 0) in 16-bit mode time-multiplexed colour-difference components U and V
PXQIN	125	I	pixel qualifier input signal to mark valid pixels; expansion port
HIN	126	I	horizontal sync input signal; expansion port
VIN	127	I	vertical sync input signal; expansion port
LLCIO	128	I/O	line-locked system clock input/output; expansion port

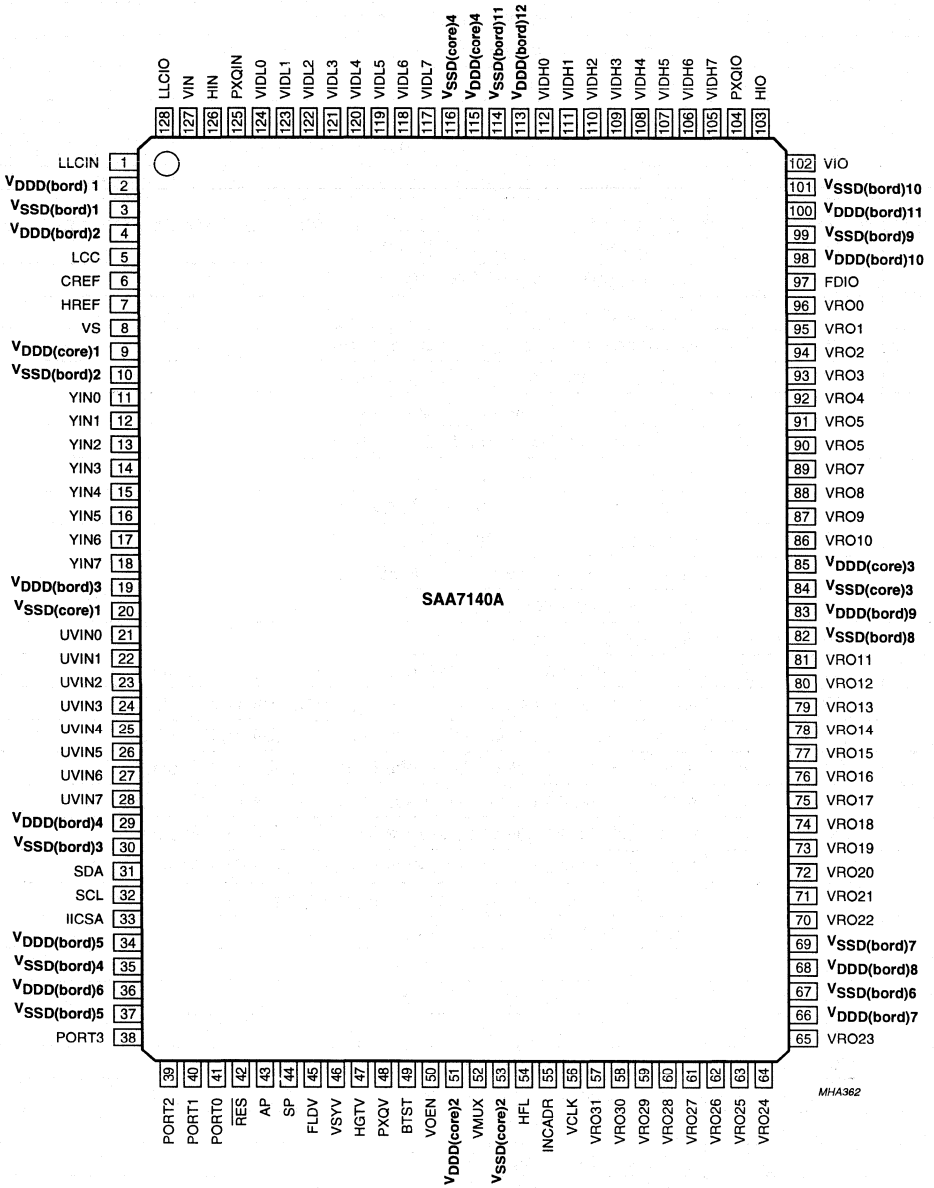


Fig.3 Pin configuration (SAA7140A).

6 PINNING (SAA7140B)

SYMBOL	PIN	I/O	DESCRIPTION
LLCIN	1	I	line-locked system clock input; expansion port
V_{DDD1}	2	–	digital supply voltage 1 (+3.3 V)
V_{SSD1}	3	–	digital ground 1 (0 V)
V_{DDD2}	4	–	digital supply voltage 2 (+3.3 V)
LLC	5	I	line-locked system clock input, maximum 32 MHz (2 × pixel rate); DMSD port
CREF	6	I	clock qualifier input (HIGH indicates valid input data YUV on DMSD port)
HREF	7	I	horizontal reference input signal; DMSD port
VS	8	I	vertical sync input signal; DMSD port
V_{DDD3}	9	–	digital supply voltage 3 (+3.3 V)
V_{SSD2}	10	–	digital ground 2 (0 V)
YIN0	11	I	luminance input data (bit 0); DMSD port
YIN1	12	I	luminance input data (bit 1); DMSD port
YIN2	13	I	luminance input data (bit 2); DMSD port
YIN3	14	I	luminance input data (bit 3); DMSD port
YIN4	15	I	luminance input data (bit 4); DMSD port
YIN5	16	I	luminance input data (bit 5); DMSD port
YIN6	17	I	luminance input data (bit 6); DMSD port
YIN7	18	I	luminance input data (bit 7); DMSD port
V_{DDD4}	19	–	digital supply voltage 4 (+3.3 V)
V_{SSD3}	20	–	digital ground 3 (0 V)
UVIN0	21	I	time-multiplexed colour-difference input data (bit 0); DMSD port
UVIN1	22	I	time-multiplexed colour-difference input data (bit 1); DMSD port
UVIN2	23	I	time-multiplexed colour-difference input data (bit 2); DMSD port
UVIN3	24	I	time-multiplexed colour-difference input data (bit 3); DMSD port
UVIN4	25	I	time-multiplexed colour-difference input data (bit 4); DMSD port
UVIN5	26	I	time-multiplexed colour-difference input data (bit 5); DMSD port
UVIN6	27	I	time-multiplexed colour-difference input data (bit 6); DMSD port
UVIN7	28	I	time-multiplexed colour-difference input data (bit 7); DMSD port
V_{DDD5}	29	–	digital supply voltage 5 (+3.3 V)
V_{SSD4}	30	–	digital ground 4 (0 V)
SDA	31	I/O	serial data input/output (I^2C-bus)
SCL	32	I	serial clock input (I^2C-bus)
IICSA	33	I	set address input (I^2C-bus)
V_{DDD6}	34	–	digital supply voltage 6 (+3.3 V)
V_{SSD5}	35	–	digital ground 5 (0 V)
V_{DDD7}	36	–	digital supply voltage 7 (+3.3 V)
V_{SSD6}	37	–	digital ground 6 (0 V)
PORT3	38	I/O	general purpose port 3 input/output (set via I^2C-bus)
PORT2	39	I/O	general purpose port 2 input/output (set via I^2C-bus)
PORT1	40	I/O	general purpose port 1 input/output (set via I^2C-bus)

SYMBOL	PIN	I/O	DESCRIPTION
PORT0	41	I/O	general purpose port 0 input/output (set via I²C-bus)
$\overline{RES}$	42	I	reset input (active LOW for at least 30 clock cycles)
AP	43	I	connected to ground (action pin for testing)
SP	44	I	connected to ground (shift pin for testing)
FLDV	45	O	field identification output signal; VRAM port
VSYV	46	O	vertical sync output signal; VRAM port
HGTV	47	O	horizontal reference output signal; VRAM port
PXQV	48	O	pixel qualifier output signal to mark active pixels of a qualified line; VRAM port
BTST	49	I	connected to ground; BTST = HIGH sets all outputs to high-impedance state (testing)
VOEN	50	I	enable input signal for VRAM port
V_{DDD8}	51	–	digital supply voltage 8 (+3.3 V)
VMUX	52	I	VRAM output multiplexing, control input for the 32 to 16-bit multiplexer
V_{SSD7}	53	–	digital ground 7 (0 V)
HFL	54	O	FIFO half-full flag output signal
INCADR	55	O	line increment/vertical reset control output
VCLK	56	I/O	clock input/output signal for VRAM port
VRO31	57	O	32-bit digital VRAM port output (bit 31)
VRO30	58	O	32-bit digital VRAM port output (bit 30)
VRO29	59	O	32-bit digital VRAM port output (bit 29)
VRO28	60	O	32-bit digital VRAM port output (bit 28)
VRO27	61	O	32-bit digital VRAM port output (bit 27)
VRO26	62	O	32-bit digital VRAM port output (bit 26)
VRO25	63	O	32-bit digital VRAM port output (bit 25)
VRO24	64	O	32-bit digital VRAM port output (bit 24)
VRO23	65	O	32-bit digital VRAM port output (bit 23)
V_{DDD9}	66	–	digital supply voltage 9 (+3.3 V)
V_{SSD8}	67	–	digital ground 8 (0 V)
V_{DDD10}	68	–	digital supply voltage 10 (+3.3 V)
V_{SSD9}	69	–	digital ground 9 (0 V)
VRO22	70	O	32-bit VRAM port output (bit 22)
VRO21	71	O	32-bit VRAM port output (bit 21)
VRO20	72	O	32-bit VRAM port output (bit 20)
VRO19	73	O	32-bit VRAM port output (bit 19)
VRO18	74	O	32-bit VRAM port output (bit 18)
VRO17	75	O	32-bit VRAM port output (bit 17)
VRO16	76	O	32-bit VRAM port output (bit 16)
VRO15	77	O	32-bit VRAM port output (bit 15)
VRO14	78	O	32-bit VRAM port output (bit 14)
VRO13	79	O	32-bit VRAM port output (bit 13)
VRO12	80	O	32-bit VRAM port output (bit 12)

SYMBOL	PIN	I/O	DESCRIPTION
VRO11	81	O	32-bit VRAM port output (bit 11)
V_{SSD10}	82	–	digital ground 10 (0 V)
V_{DDD11}	83	–	digital supply voltage 11 (+3.3 V)
V_{SSD11}	84	–	digital ground 11 (0 V)
V_{DDD12}	85	–	digital supply voltage 12 (+3.3 V)
VRO10	86	O	32-bit VRAM port output (bit 10)
VRO9	87	O	32-bit VRAM port output (bit 9)
VRO8	88	O	32-bit VRAM port output (bit 8)
VRO7	89	O	32-bit VRAM port output (bit 7)
VRO6	90	O	32-bit VRAM port output (bit 6)
VRO5	91	O	32-bit VRAM port output (bit 5)
VRO4	92	O	32-bit VRAM port output (bit 4)
VRO3	93	O	32-bit VRAM port output (bit 3)
VRO2	94	O	32-bit VRAM port output (bit 2)
VRO1	95	O	32-bit VRAM port output (bit 1)
VRO0	96	O	32-bit VRAM port output (bit 0)
FDIO	97	I/O	field identification output signal; 7196 DIR input signal expansion port, I^2C-bus controlled
V_{DDD13}	98	–	digital supply voltage 13 (+3.3 V)
V_{SSD12}	99	–	digital ground 12 (0 V)
V_{DDD14}	100	–	digital supply voltage 14 (+3.3 V)
V_{SSD13}	101	–	digital ground 13 (0 V)
VIO	102	I/O	vertical sync input/output signal; expansion port
HIO	103	I/O	horizontal sync input/output signal; expansion port
PXQIO	104	I/O	pixel qualifier input/output signal to mark valid pixels; expansion port
VIDH7	105	I/O	bidirectional expansion port, high byte (bit 7) in 16-bit mode luminance component Y
VIDH6	106	I/O	bidirectional expansion port, high byte (bit 6) in 16-bit mode luminance component Y
VIDH5	107	I/O	bidirectional expansion port, high byte (bit 5) in 16-bit mode luminance component Y
VIDH4	108	I/O	bidirectional expansion port, high byte (bit 4) in 16-bit mode luminance component Y
VIDH3	109	I/O	bidirectional expansion port, high byte (bit 3) in 16-bit mode luminance component Y
VIDH2	110	I/O	bidirectional expansion port, high byte (bit 2) in 16-bit mode luminance component Y
VIDH1	111	I/O	bidirectional expansion port, high byte (bit 1) in 16-bit mode luminance component Y
VIDH0	112	I/O	bidirectional expansion port, high byte (bit 0) in 16-bit mode luminance component Y
V_{DDD15}	113	–	digital supply voltage 15 (+3.3 V)

SYMBOL	PIN	I/O	DESCRIPTION
V_{SSD14}	114	–	digital ground 14 (0 V)
V_{DDD16}	115	–	digital supply voltage 16 (+3.3 V)
V_{SSD15}	116	–	digital ground 15 (0 V)
VIDL7	117	I/O	bidirectional expansion port, low byte (bit 7) in 16-bit mode time-multiplexed colour-difference components U and V
VIDL6	118	I/O	bidirectional expansion port, low byte (bit 6) in 16-bit mode time-multiplexed colour-difference components U and V
VIDL5	119	I/O	bidirectional expansion port, low byte (bit 5) in 16-bit mode time-multiplexed colour-difference components U and V
VIDL4	120	I/O	bidirectional expansion port, low byte (bit 4) in 16-bit mode time-multiplexed colour-difference components U and V
VIDL3	121	I/O	bidirectional expansion port, low byte (bit 3) in 16-bit mode time-multiplexed colour-difference components U and V
VIDL2	122	I/O	bidirectional expansion port, low byte (bit 2) in 16-bit mode time-multiplexed colour-difference components U and V
VIDL1	123	I/O	bidirectional expansion port, low byte (bit 1) in 16-bit mode time-multiplexed colour-difference components U and V
VIDL0	124	I/O	bidirectional expansion port, low byte (bit 0) in 16-bit mode time-multiplexed colour-difference components U and V
PXQIN	125	I	pixel qualifier input signal to mark valid pixels; expansion port
HIN	126	I	horizontal sync input signal; expansion port
VIN	127	I	vertical sync input signal; expansion port
LLCIO	128	I/O	line-locked system clock input/output; expansion port

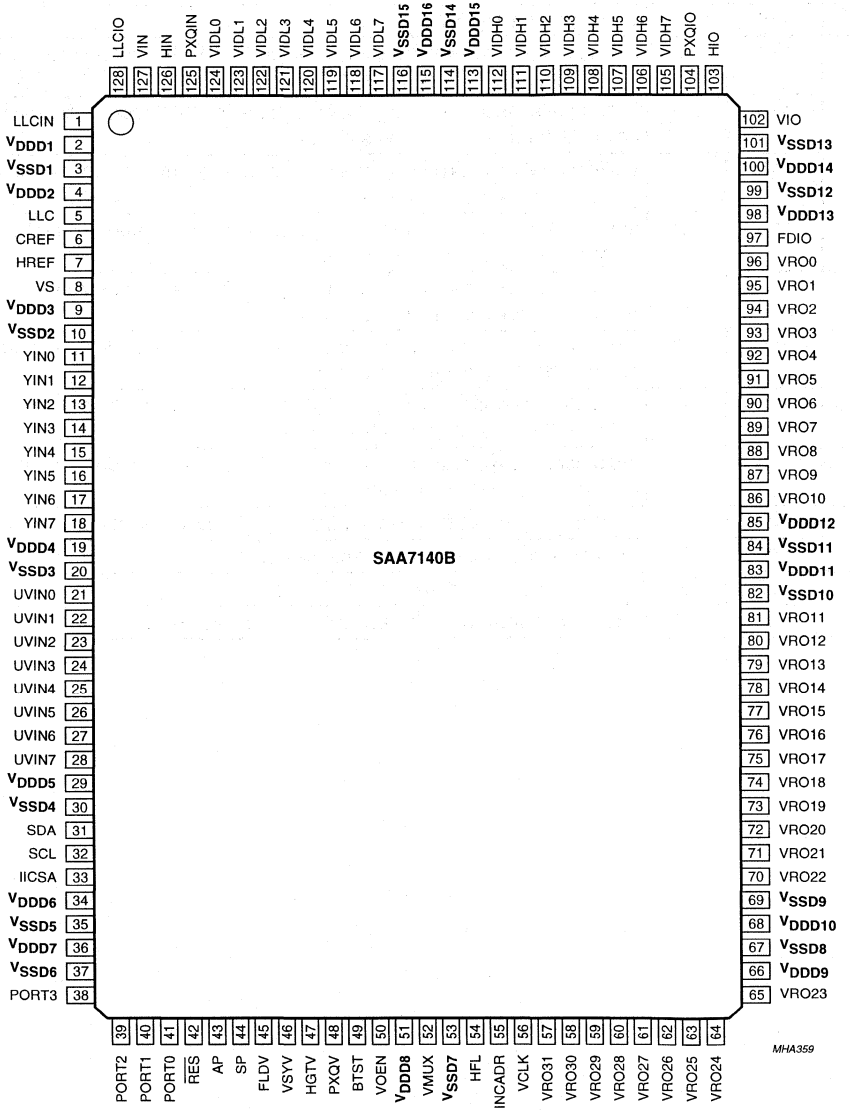


Fig.4 Pin configuration (SAA7140B).

7 FUNCTIONAL DESCRIPTION

The SAA7140A and SAA7140B accepts YUV data in a 16-bit wide parallel format at the DMSD port and accepts YUV input in a 16-bit wide parallel format and in an 8-bit byte-multiplexed Cb-Y-Cr-Y- format (CCIR-656 or D1 oriented) at the expansion port.

Depending on the selected port modes, the incoming data is formatted to the internal data representation, where reference signals or codes are detected in the Data Formatter/Reformatter (DFR). The horizontal and vertical timing reference can be defined under I²C-bus control. Based on that timing reference, the active processing window is defined in a versatile way via the programming. Two programming sets can be loaded simultaneously, and become valid for processing in a field alternating way. Before being processed in the central scaling unit, the incoming data passes through the BCS control unit where monitor control functions, for adjusting brightness, contrast (luminance) and saturation (chrominance) are implemented.

The scaling is performed in three steps:

1. Horizontal prescaling (bandwidth limitation for anti-aliasing, via FIR prefiltering and subsampling)
2. Vertical scaling (generating phase interpolated or vertically low-passed lines)
3. Horizontal variable phase scaling (phase-correct scaling to the new geometric relationships).

The scaled output data is fed back to the DFR unit and may be used as output signals from the bidirectional expansion port (if the mode is selected). They are converted in parallel from the YUV to the RGB domain in a digital matrix. Anti-gamma correction of gamma-corrected input signals can be performed in the RGB data path. The output formatter then formats the scaled data to one of the various output formats (e.g. monochrome, 16-bit YUV or 32-bit RGB (5, 5, 5).

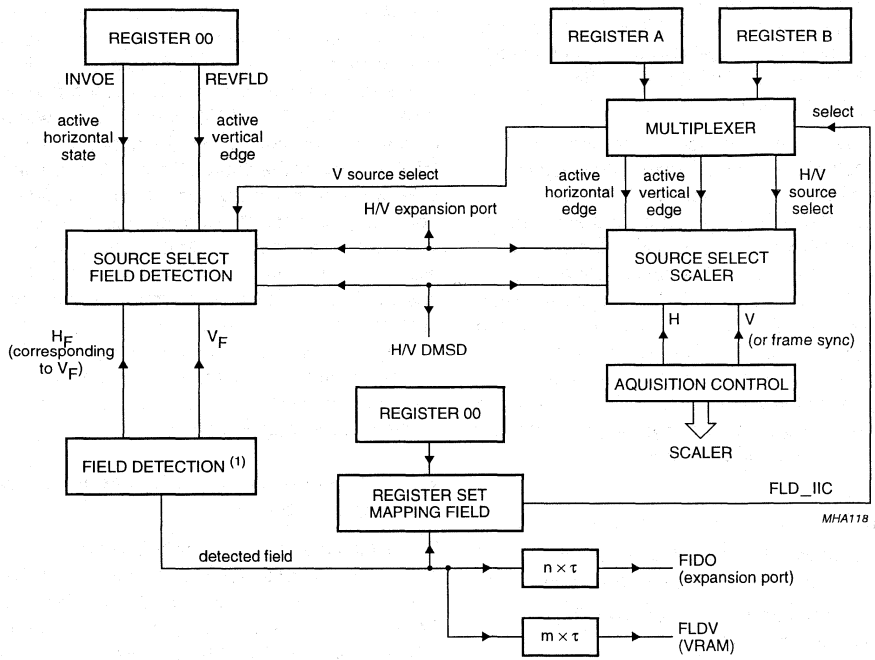
To ease frame buffer applications, the data can be transferred in a synchronous way (transparent mode), using separate reference and qualifier signals and a continuous output clock (VCLK). The data can also be transferred in an asynchronous way (burst mode) using the HFL and INCADR flags and a discontinuous input clock burst on VCLK.

In a typical application, the 16-bit wide YUV input receives clock, sync and data from a video decoder (SAA71xx) via the DMSD port. An MPEG compression/decompression circuit can be connected at the expansion port to receive the decoder data, scaled or unscaled, or to deliver data to the scaling processor. The scaling operation of the SAA7140A and SAA7140B can be performed on the data from a video decoder, or on the data from the MPEG-codec at the expansion port input. The source selection can be static or toggled on a field-by-field basis. For example, during the odd field the video decoder signal is scaled in accordance with the 'odd' parameter set for display in a window. The compression codec receives unscaled data. During the even field the decompressed data from the MPEG decoder gets sized for a second display window in accordance with the 'even' parameter set. The resulting output from the scaling operation is delivered via the 32-bit wide output (VRAM port) and to the expansion port output (optional).

7.1 Data format/reformatter and reference signal generation

The video data can be formatted/reformatted in accordance with the selected expansion port mode, from 16-bit (DMSD port) to serial 8-bit (expansion port output), from serial 8-bit (expansion port input) to internal parallel 16-bit format and from 24-bit (scaler output) to 16-bit/8-bit respectively (expansion port output). The definition of the timing references for the acquisition and field detection (polarity and edge selection) are based on the selected reference signal source. The field detector regenerates the field information from the selected incoming reference signals (see Fig.5).

The field sequence flag (FLD), detects the state of the H-sync signal at the reference edge of the V-sync signal. The detection is controlled by I²C-bus bits REVFLD and INVOE. The detection output can be seen on pins FLDV and FDIO (if FLDC = 0). Bits IREGS and SREGS control the mapping of the detected sequence to the I²C-bus register sets A and B (I²C-bus subaddress 02 to 1F and 22 to 3F).



FLD detection modes (I^2C-bus bits FICO1 and FICO0);

(1) In the normal mode: the FLD signal is detected from the incoming H and V signals.

In the improved mode: the FLD signal is resynchronized only after the H and V sequence runs stable for a certain period of time.

In the force toggle mode: the FLD signal toggles with every event on the V signal (H is independent).

Register set mapping modes (I^2C-bus bits IREGS and SREGS);

The FLD_IIC signal carries the detected FLD or the inverted FLD.

The signal is fixed to 0 (Register set A forced) or forced to 1 (Register set A forced).

Fig.5 Field detection/register set mapping.

7.1.1 Data formats and reference signals of the DMSD port

The 16-bit YUV colour difference and luminance signals (straight binary) are available in parallel on a 16-bit wide data stream. The code is in accordance with CCIR-601; black = 16, white = 235, no colour = 128, 100% colour saturation = 16 to 240 etc. Overshoots and undershoots are permitted and supported, i.e. processed as they are. The 16-bit wide YUV data format from the DMSD port (input only) is defined with Line-Locked Clock (LLC) with a double pixel clock frequency. Every second clock cycle is qualified with CREF, in pixel rate frequency.

The internal processing of the SAA7140A and SAA7140B relies on the presence of LLC, i.e. a clock of at least twice the sampling rate of the input data stream. The maximum LLC rate is 32 MHz.

The horizontal sync input (HREF) may be supplied as a H-pulse or horizontal gate signal. The positive or negative edge, (programmable by I^2C-bus bit REHAW), indicates the horizontal timing reference. The first valid pixels may occur not exactly at the start of the line but with a certain offset (counted in qualified pixels).

The vertical timing is indicated by the positive or negative edge (programmable by I²C-bus bit REVAW) of the sync input signal VS. The first valid line may occur not exactly at the start of the field but with a certain offset, counted in lines, with qualified pixels. Input signal VS defines, in relation to HREF, the odd/even field detection (see *SAA7191B*).

7.1.2 Data formats and reference signals of the expansion port

The expansion port (input/output) supports several modes; simultaneous (parallel) D1 input and D1 output (full duplex) with auxiliary sync and qualifying signals, or 16-bit wide YUV input or output (half duplex), selected via programming with clock, qualify and sync signal.
A discontinuous data stream is supported by accepting or generating a pixel/byte qualifying signal (PXQ), a generalization of the CREF definition at the DMSD port (PXQ = 1 qualified pixel, PXQ = 0 invalid data).

16-bit YUV (half duplex mode = field alternating data I/O): 16-bit YUV data stream (Y = VIDH7 to VIDH0, UV = VIDL7 to VIDL0). For the 16-bit YUV data input format, PXQ is inhibited from qualifying adjacent LLC clock cycles. There must be at least one empty clock cycle between two valid pixels.

8-bit Cb-Y-Cr-Y; CCIR 656 or D1 (full duplex mode): the colour difference signals and the luminance signal (straight binary) are byte-wise multiplexed onto the same 8-bit wide data stream, with sequence and timing in accordance with CCIR 656 recommendations (according to D1 for 60 Hz application respectively). The code is in accordance with CCIR 601 (black = 16, white = 235, no colour = 128, 100% colour saturation = 16 or 240, etc. Overshoots and undershoots are permitted and supported, i.e. processed as they are.

If the CCIR 656 output is selected, the video signal is clipped to 01H and FEH in order to leave the codes 00H and FFH for SAV and EAV encoding (SAV and EAV encoding not yet supported). The clock rate for this format is twice the pixel clock.

The horizontal sync input HIN is processed in an identical manner to HREF at the DMSD port. If the CCIR 656 data input format is selected, the horizontal timing reference is decoded from the input data stream (SAV, EAV and SHVS = 1) or taken from the selected H-reference signal HIN, HREF or HIO (SHVS = 0). The start condition to enable synchronization to the correct Cb-Y-Cr-Y-sequence is provided by the selected horizontal reference signal. The sequence only increments with qualified bytes.

Instead of a vertical sync signal, as described for the DMSD port, the expansion port also supports an odd/even signal applied to the input pin VIN or VIO (controlled by I²C-bus bit FSEL). The frame and the field timing is then indicated by a positive or negative edge of the V input. This may occur with a certain offset at the frame and field start, and is normally counted in lines.

If the CCIR 656 data input format is selected, the vertical timing reference is decoded from the input data stream by SAV and EAV (SHVS = 1) or taken from the selected V reference signal VIN, VS or VIO (SHVS = 0). The vertical synchronization pin can be programmed to carry either a vertical sync signal or an odd/even signal.

The horizontal and vertical sync outputs HIO and VIO are expansion port mode dependent and can be selected via the I²C-bus (VD1/VD0 and HD1/HD0):

Should the DMSD port be selected as the output source, HIO will carry a copy of HREF and VIO will carry a copy of VS.

If the expansion port carries data from the scaler output, then HIO is a gate signal enveloping the range of active video along a line and VIO is a positive sync pulse with a length of 4 lines

If HIN/VIN is selected as the output source, HIO carries a copy of HIN and VIO carries a copy of VIN (short cut).

If the CCIR 656 data output format is selected, the horizontal and vertical sync output signals are only supplied at pins HIO and VIO (SAV and EAV are not encoded as outputs).

Due to compatibility reasons to the expansion port definition of the SAA7194/SAA7196 circuits, the bidirectional pins HIO, VIO and PXQIO can also be configured as input pins (see Table 3).

The definition of the pin FDIO is I²C-bus selectable. Configured as an output pin, FDIO carries an odd/even signal generated in the FLD detection (see Fig.5). Configured as an input pin, FDIO controls the direction of the expansion port (compatibility to SAA7194/SAA7196, (see Table 3 and Chapter 8).

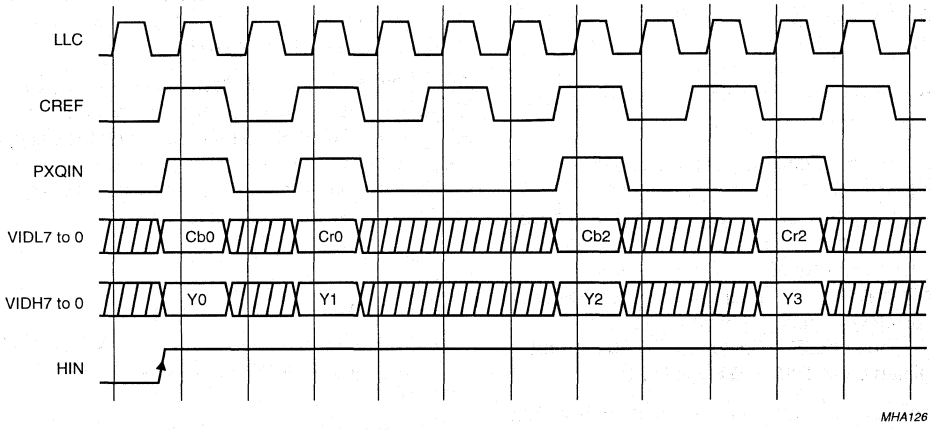


Fig.6 Timing of PXQIN for 16-bit data input from DMSD to expansion port.

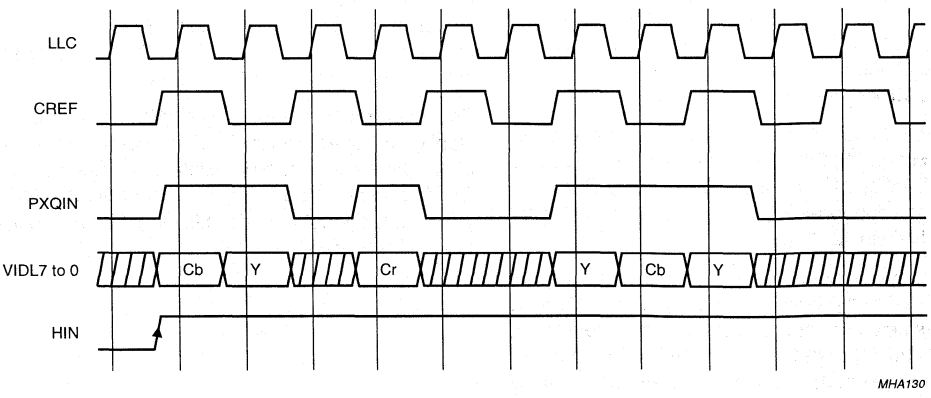


Fig.7 Timing of PXQIO for serial 8-bit data input at expansion port.

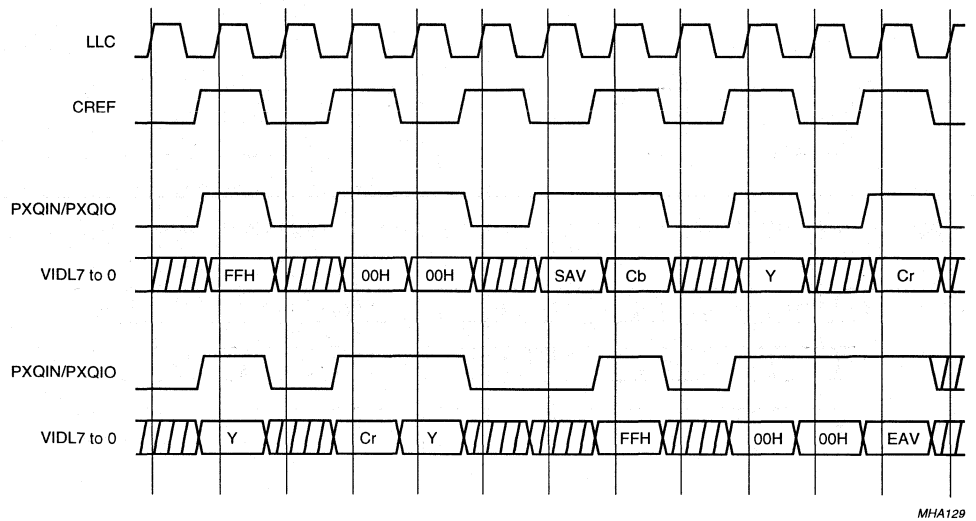


Fig.8 Timing of PXQIN/PXQIO for CCIR 656 data input at expansion port.

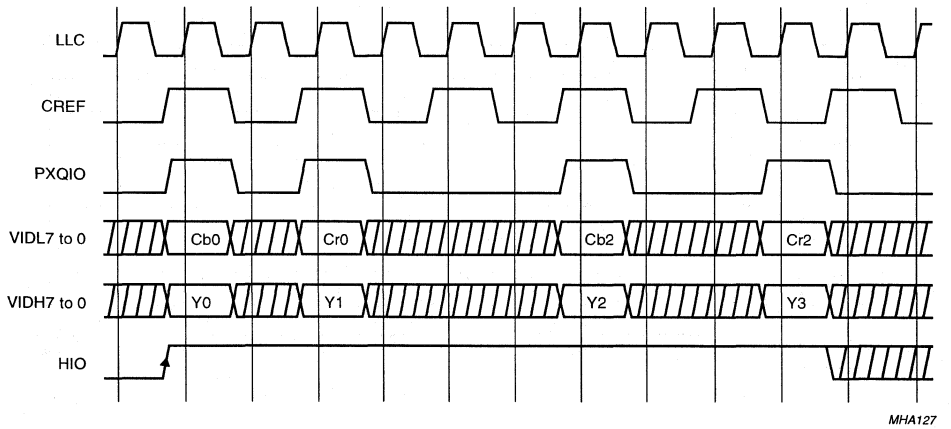


Fig.9 Timing of PXQIO for non-zoomed 16-bit data output at expansion port.

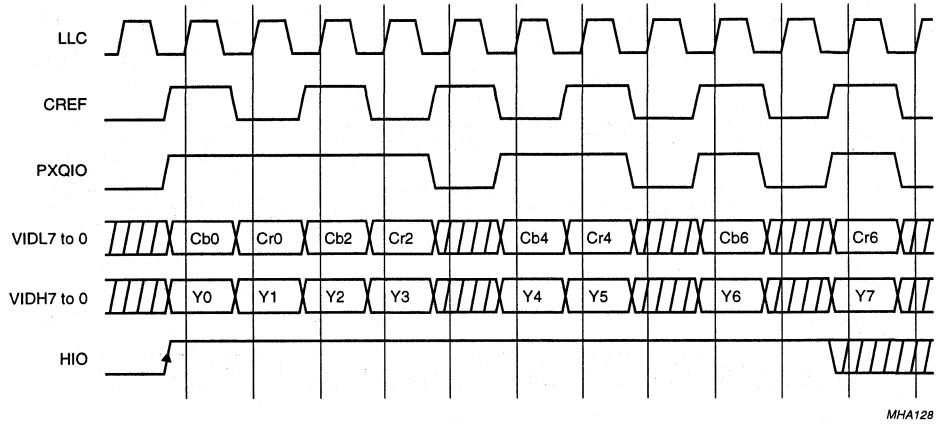


Fig.10 Timing of PXQIN for zoomed 16-bit data output at expansion port.

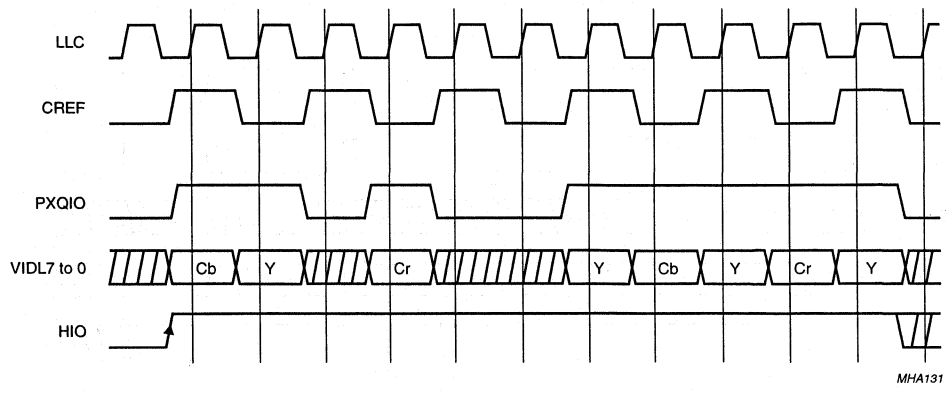
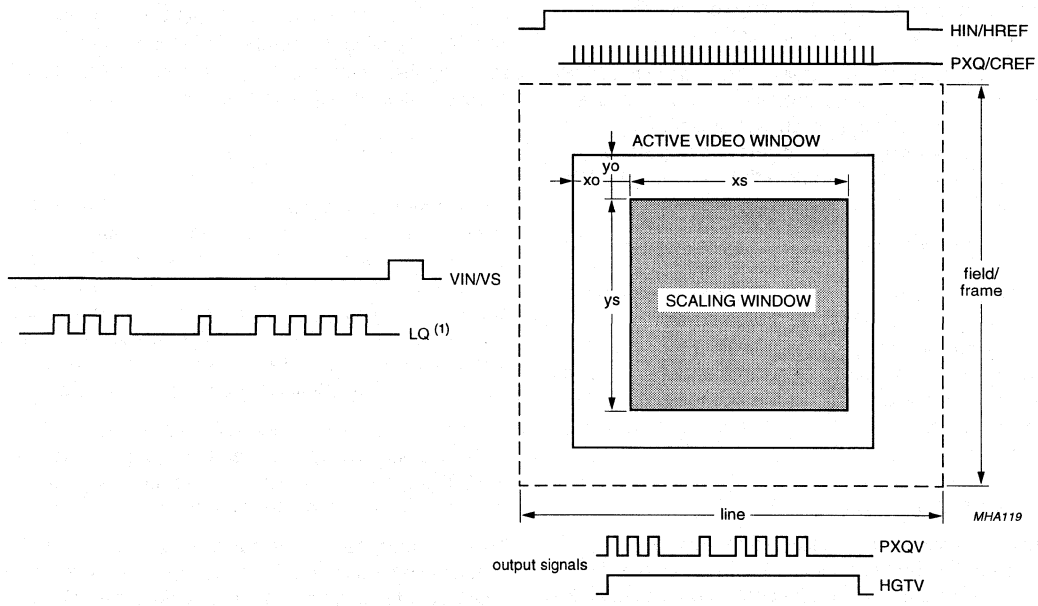


Fig.11 Timing of PXQIO for serial 8-bit data output at expansion port.

7.2 Acquisition control

The processing window for the scaling unit is defined in the acquisition control unit. An internal counter receives I²C-bus controlled values for offset (bits XO10 to XO0 and YO10 to YO0) and length (bits XS10 to XS0 and YS10 to YS0). The counter is reset by the corresponding sync reference input signal. The horizontal counter increments in qualified pixels and the vertical counter increments in qualified lines, i.e. lines containing at least one qualified pixel. Depending on the selected mode, the source for the horizontal reference may be HREF (DMSD port) or HIN (expansion port), or for the vertical reference, VS (DMSD port) or VIN (expansion port).

It should be noted that in order to avoid programming dependent line and field drop effects, all values must not exceed the number of qualified pixels per line or lines per field.



(1) LQ = qualified lines i.e. lines containing at least one qualified pixel.

Fig.12 Reference signals for scaling window.

7.3 BCS control

The parameters for Brightness, Contrast and Saturation (BSC) can be adjusted in the BSC control unit.

The luminance signal can be controlled via the I²C-bus using bits BRIG7 to BRIG0 and CONT6 to CONT0.

For the brightness control:

00H = minimum offset

80H = nominal level

FFH = maximum offset.

For the contrast control:

00H = luminance off

40H = nominal gain of 1.01

7FH = maximum gain of 1.9999.

The chrominance signal can be controlled via the I²C-bus using bits SAT6 to SAT0.

For the saturation control:

00H = colour off

40H = nominal gain of 1.0

7FH = maximum gain of 1.9999.

With respect to limiting, all values are limited to minimum (equals 0) and maximum (equals 255).

7.4 Scaling unit

Scaling to a randomly sized window is performed in three steps:

1. Horizontal prescaling (bandwidth limitation for anti-aliasing, via FIR prefiltering and subsampling)
2. Vertical scaling (generating phase interpolated or vertically low-passed lines)
3. Horizontal variable phase scaling (phase-correct scaling to the new geometric relations).

The scaling processor can obtain its clock from the DMSD port or the expansion port. Normally the two ports are synchronized to support program-set-swapping, asynchronous working results in restricted operation. The video signal source also provides the source for the scalers qualify signal PXQ.

The scaling process generates a new pixel/clock qualifier sequence. This results in PXQ being used at the VRAM port in the transparent mode, and for the expansion port output. There are restrictions in the combination of the input sample rate and up or down-scaling mode and scaling factor. The maximum resulting output sample rate at the VRAM port is LLC and at the expansion port the maximum pixel rate is ½LLC, due to the support of the CCIR 656 format.

7.4.1 Horizontal prescaling

The incoming pixels in the selected range are preprocessed in the horizontal prescaler, which is the first stage of the scaling unit. The prescaler consists of an FIR prefilter and a pixel collecting subsampler.

7.4.1.1 FIR prefilter

The video components Y, U and V are FIR prefiltered to reduce the signal bandwidth in accordance with the downscale for factors between 1 to ½, thus aliasing due to signal bandwidth expansion is reduced.

The prefilter consists of 3 filter stages. The transfer functions are given in Chapter 8.
The prefilter is controlled by the I²C-bus bits PFY3 to 0 and PFUV3 to 0 in I²C-bus subaddress 13 and 33.

Figures 13 and 14 illustrate some frequency responses and the corresponding I²C-bus settings.
The prefilter operates on 4 : 4 : 4 YUV data. As U and V are generated by simple chroma pixel doubling, the UV prefilter should also be used to generate the interpolated chroma values.

7.4.1.2 Subsampler

To improve the scaling performance for scales of less than ½ down to icon size, a FIR filtering subsampler is available. It performs a subsampling of the incoming data by a factor of 1/N (where N = XPSC + 1 = 1 to 64).
With N_{IP} equalling the number of input pixel/line and N_{OP} equalling the number of desired output pixels/line, the basic equation to calculate XPSC is as follows:

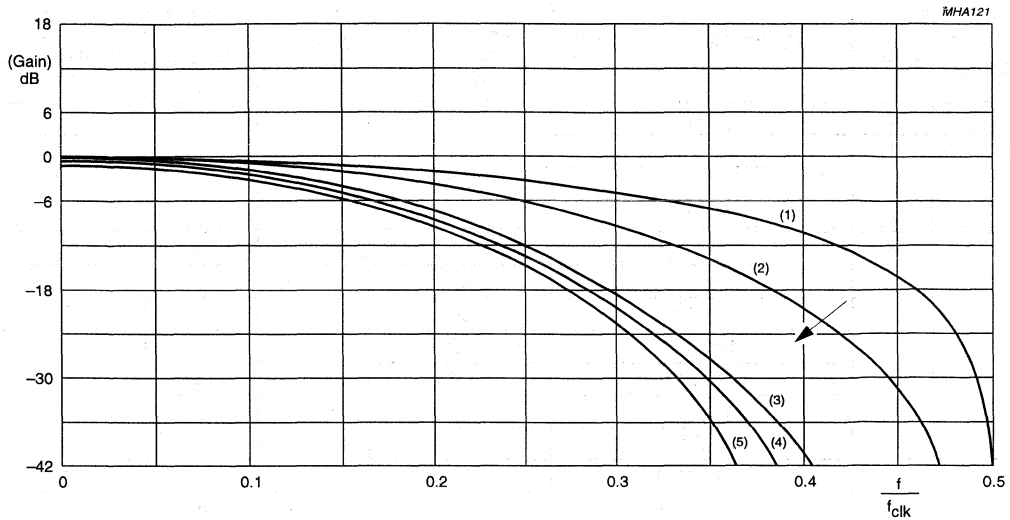
$$XPSC = TRUNC \times \left(\frac{N_{IP}}{N_{OP} - 1} \right)$$

The subsampler collects a number of [N + 1(–XACM)] pixels to calculate a new subsampled output pixel. Consequently, a downscale dependent FIR filter has been incorporated, with up to 65 taps, which reduces aliasing for small sizes. If XACM = 0 the collecting sequence overlaps, which means that the last pixel of sequence M is also the first pixel of sequence M + 1. To implement a real subsampler bypass XACM has to be set to logic 1.

It should be noted that because the phase-correct horizontal fine scaling is limited to a maximum downscale of ¼, this circuitry has to be used for downscales less than ¼ of the incoming pixel count.

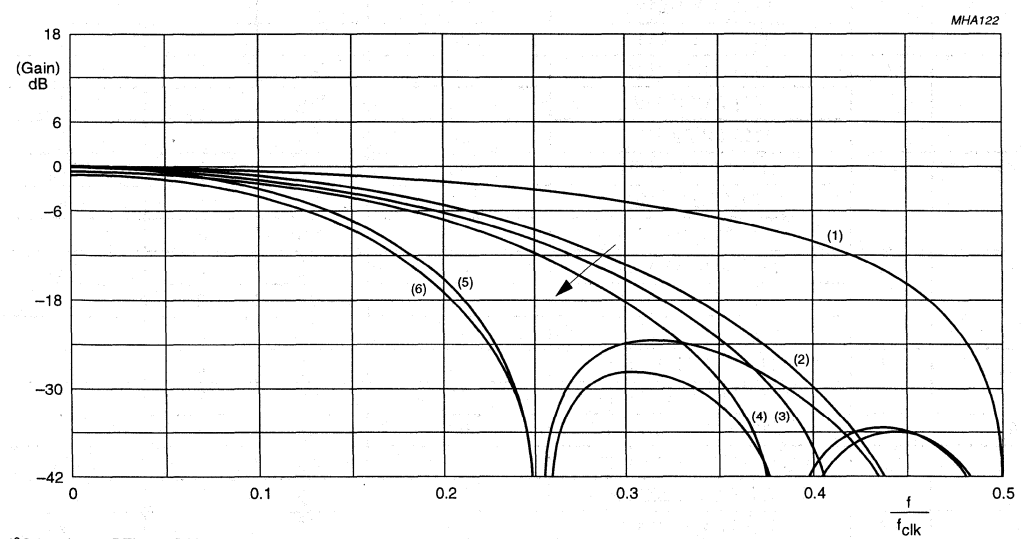
To obtain unity gain at the subsamplers output for all subsampling ratios, the I²C-bus parameters CXY, CXUV and DCGX have to be used. In addition, the I²C-bus parameters can be used to slightly modify the FIR characteristic of the subsampler.

Table 1 gives examples of I²C-bus register settings, depending on a given prescaler ratio. With reference to Table 1, it should be noted that an internal XPSC-dependent automatic prenormalization becomes valid for XPSC > 8, > 6 and >32, which reduces the input signal quantization. In addition, for XPSC ≥ 15 the LSB of the CXY and CXUV parameter become valid.



I²C-bus bytes PFY3 to PFY0.
(1) = 0001; (2) = 0010; (3) = 0011; (4) = 1011; (5) = 1111.

Fig.13 Luminance prefilter frequency response for miscellaneous I²C-bus settings.



I²C-bus bytes PFU3 to PFU0.
(1) = 0001; (2) = 0010; (3) = 1010; (4) = 1110; (5) = 0011; (6) = 1111.

Fig.14 Chrominance prefilter frequency response for miscellaneous I²C-bus settings.

Table 1 Horizontal prescaling and normalization

HORIZONTAL PRESCALING	XPSC	COEFFICIENT SEQUENCE (example)	CXY (luma)/ CXUV (chroma) (HEX)	WEIGHT SUM	DCGX	BSC (CONT/SAT) = x/y × 64
1	0	1-1	00	2	1	1
1/2	1	1-1-1	00	3	1	2/3
		1-2-1	02	4	2	1
1/3	2	1-1-1-1	00	4	2	1
1/4	3	1-1-1-1-1	00	5	2	4/5
		1-2-2-2-1	06	8	3	1
1/5	4	111 111	00	6	2	4/6
		121 121	02	8	3	1
		112 211	04	8	3	1
1/6	5	111 1 111	00	7	3	8/7
		111 2 111	08	8	3	1
1/7	6	1111 1111	00	8	3	1
1/8	7	1111 1 1111	00	9	3	8/9
		1222 2 2221	1E	16	7	1
1/9	8	1111 1 1 1111	00	10½	2	4/5
		1221 2 2 1221	16	16½	3	1
		1122 2 2 2211	1C	16½	3	1
1/10	9	1111 1 1 1 1111	00	11½	2	8/11
		1212 1 2 1 2121	2A	16½	3	1
		1112 2 2 2 2111	38	16½	3	1
1/11	10	1111 11 11 1111	00	12½	2	8/12
		1211 21 12 1121	12	16½	3	1
		1111 22 22 1111	30	16½	3	1
1/12	11	1111 11 1 11 1111	00	13½	2	8/13
		1121 11 2 11 1211	44	16½	3	1
		1111 12 2 21 1111	60	16½	3	1
1/13	12	1111 111 111 1111	00	14½	2	8/14
		1111 211 112 1111	10	16½	3	1
		1111 112 221 1111	40	16½	3	1
1/14	13	1111 111 1 111 1111	00	15½	2	8/15
		1111 111 2 111 1111	80	16½	3	1
1/15	14	1111 1111 1111 1111	00	16½	3	1
1/16	15	1111 1111 1 1111 1111		17½	3	16/17
		1222 2222 2 2222 2221	FF	32½	7	1
1/17	16	1111 1111 1 1 1111 1111	00	18¼	2	16/18
		1222 2222 1 1 2222 2221	FE	32¼	3	1
		1222 2122 22 2212 2221	DF	32¼	3	1

HORIZONTAL PRESCALING	XPSC	COEFFICIENT SEQUENCE (example)	CXY (luma)/ CXUV (chroma) (HEX)	WEIGHT SUM	DCGX	BSC (CONT/SAT) = x/y × 64
1/18	17	1111 1111 1 1 1 1111 1111	00	19/4	2	16/19
		1222 1222 1 2 1 2221 2221	EE	32/4	3	1
		1222 2112 2 2 2 2112 2221	9F	32/4	3	1
....	....	....	....	xx/4	....	....
1/33	32	1111 ... 1111	00	34/8	2	–
....	....	....	....	xx/8	....	....
1/63	62	....	....	....	....	....
1/64	63	....	....	....	....	....

7.4.2 VERTICAL SCALER

The vertical scaler performs the vertical downscaling of the input data stream to a random number of output lines. It can be used for input line lengths up to 768 pixels/line and has to be bypassed if the input line length exceeds the pixel count.

For vertical scaling there are two different modes implemented; the ACCU mode (vertical accumulation) for scales down to icon size and the Linear Phase Interpolation mode (LPI) for scales between 1 and ½.

7.4.2.1 ACCU mode (scaling factor range 1 to 1/1024; I²C-bus bit YACM = 1:

The ACCU mode can be used for vertical scaling down to icon size. In this mode, the I²C-bus parameter YSCI controls the scaling and parameter YACL controls the vertical anti-alias filtering.

The output lines are generated by a scale-dependent variable averaging (YACL + 2) input lines. In this way a vertical FIR filter can be created for anti-aliasing, with up to 65 taps (max.).

YSCI defines the output line qualifier pattern and YACL defines the sequence length for the line averaging. For accurate processing, the sequence has to fit into the qualifying pattern. In the event of mis-programming YACL unexpected line dropping occurs; where N_{OL} = number of output lines and N_{IL} = number of input lines. The I²C-bus bits YSCI (scaling increment), YACL (accumulation length; optimum: 1 line overlap) and YP (scaling start phase) have to be set according to the following equations (see Fig.15):

$$YACL = TRUNC \times \left(\frac{N_{IL}}{N_{OL} - 1} \right);$$

accumulation sequence length: i.e. the number of lines per sequence that are not part of overlay region of neighbouring sequences (optimum 1 line overlapped).

$$YSCI = INT\left[1024 \times \left(\frac{1 - N_{OL}}{N_{IL}} \right) \right]$$; scaling increment.

$$YP = INT\left(\frac{YSCI}{16} \right)$$; scaling start phase (fix; modified in LPI mode only).

In order to obtain unity amplitude gain for all sequence lengths and to improve the vertical scaling performance, the accumulated lines can be weighted and the amplitude of the scaled output signal has to be renormalized. In the given example (see Fig.15) using the optimum weighting, the gain of a sequence results in 1 + 2 + 2 + 1 = 6. Renormalization (factor 1/6) can be achieved;

By gain reduction using BCS control (brightness, contrast and saturation) down to 4/6 and a selecting factor of ¼ for DCGY2 to DCGY0 (see Section 8.3), which may result in a loss of signal quantization, or

By gain emphasizing using BCS control up to 8/6 and selecting a factor of ⅛ for DGY2 to DCGY0 which may result in a loss of signal detail, due to limiting in the BCS control.

Normally the weighting would be 2 + 2 + 2 + 2. In this situation the gain can be renormalized with DCGY2 to DCGY0 = 010 (factor ⅛).

Table 2 gives examples for I²C-bus register settings, depending on a given scale ratio.

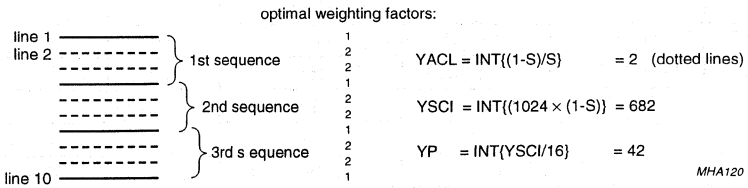


Fig.15 Example of vertical accumulation.

Table 2 Vertical scaling and normalization

VERTICAL SCALE RATIO (YSCI ≥)	YACL	COEFFICIENT SEQUENCE (example)	CYA (HEX)	CYB (HEX)	WEIGHT SUM	DCGY	BCS (CONT/SAT) = x/y × 64
1 to 1/2 (0)	0	1-1	01	00	2	0	1
1/2 to 1/3 (512)	1	1-1-1	03	00	3	0	2/3
		1-2-1	01	02	4	1	1
1/3 to 1/4 (683)	2	1-1-1-1	03	00	4	1	1
1/4 to 1/5 (768)	3	1-1-1-1-1	07	00	5	1	4/5
		1-2-2-2-1	01	06	8	2	1
1/5 to 1/6 (820)	4	111 111	07	00	6	1	4/6
		121 121	05	02	8	2	1
		112 211	03	04	8	2	1
1/6 to 1/7 (854)	5	111 1 111	0F	00	7	2	8/7
		111 2 111	07	08	8	2	1
1/7 to 1/8 (878)	6	1111 1111	0F	00	8	2	1
1/8 to 1/9 (896)	7	1111 1 1111	1F	00	9	2	8/9
		1222 2 2221	01	1E	16	3	1
1/9 to 1/10 (911)	8	1111 1 1 1111	1F	00	10	3	8/10
		2121 2 2 1212	09	15	16	3	1
		1122 2 2 2211	03	1C	16	3	1
1/10 to 1/11 (922)	9	1111 1 1 1 1111	3F	00	11	2	8/11
		1212 1 2 1 2121	15	2A	16	3	1
		1112 2 2 2 2111	07	38	16	3	1
1/11 to 1/12 (931)	10	1111 11 11 1111	3F	00	12	2	8/12
		1211 21 12 1121	2D	12	16	3	1
		1111 22 22 1111	0F	30	16	3	1

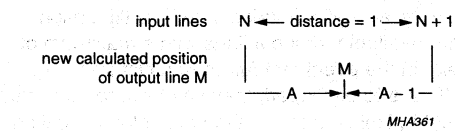
VERTICAL SCALE RATIO (YSCI ≥)	YACL	COEFFICIENT SEQUENCE (example)	CYA (HEX)	CYB (HEX)	WEIGHT SUM	DCGY	BCS (CONT/SAT) = x/y × 64
1/12 to 1/13 (939)	11	1111 11 1 11 1111	7F	00	13	2	8/13
		1111 21 2 12 1111	2F	50	16	3	1
		1121 11 2 11 1211	3B	44	16	3	1
1/13 to 1/14 (946)	12	1111 111 111 1111	7F	00	14	2	8/14
		1111 211 112 1111	6F	10	16	3	1
		1111 112 211 1111	3F	40	16	3	1
1/14 to 1/15 (951)	13	1111 111 1 111 1111	FF	00	15	2	8/15
		1111 111 2 111 1111	7F	80	16	3	1
1/15 to 1/16 (956)	14	1111 1111 1111 1111	FF	00	16	3	1
1/16 to 1/17 (960)	15	1111 1111 1 1111 1111	FF	00	17	3	16/17
		2122 2222 2 2222 2212	02	FD	32	4	1
1/17 to 1/18 (964)	16	1111 1111 1 1 1111 1111	FF	00	18	3	16/18
		2212 2212 2 2 2122 2122	44	BB	32	4	1
		1222 2222 1 1 2222 2221	01	FE	32	4	1
....	....	....	....	....	....	....	....
1/23 to 1/24 (980)	22	1111 2222 1111 1111 2222 1111	0F	F0	32	4	1
		1121 1212 1121 1211 2121 1211	AD	52	32	4	1

7.4.2.2 LPI mode (scaling factor range 1 to 1/2; IC-bus bit YACM = 0)

To preserve the signal quality for slight vertical downscales (scaling factors 1 to 1/2) linear phase interpolation between consecutive lines is implemented to generate geometrically correct vertical output lines.Therefore, the new geometric position between lines N and N + 1 can be calculated.

A new output line is calculated by weighting the samples 'p' (pixel) of lines N and N + 1 with the normalized distance to the new calculated position (see Fig.16);

When N_{OL} = number of output lines and N_{IL} = number of input lines the I²C-bus bits YSCI (scaling increment) and YP (scaling start phase) have to be set according to the following equations;



$$p(M) = A \times p(N+1) + (1-A) \times p(N)$$

where A = 0 to 63/64

Fig.16 New output line calculation.

$$YSCI = INT\left[1024 \times \left(\frac{N_{IL}}{N_{OL}} - 1\right)\right] \quad \text{; scaling increment}$$

$$YP = INT\left(\frac{YSCI}{16}\right) \quad \text{; scaling start phase}$$

(recommended value).

The vertical start phase offset is defined by $^{YP}/_{64}$ (YP = 0 to 64):

YP = 0: offset = 0 geometrical position of 1st line out = 1st line in.

YP = 64: offset = $^{64}/_{64}$ = 1 geometrical position of 1st line out = 2nd line in.

Finally 3 special modes must be emphasized:

1. By-pass (YSCI = 0, YP = 64) each line out is equivalent to corresponding line in.
2. Low-pass (YSCI = 0, YP < 64) e.g. YP = 32: average value of 2 lines ($1 + z^{-H}$ filter).
3. For processing of interlaced input signals the LPI mode **must** be used (the ACCU mode would cause 'line pairing' problems). The scaling start phase for odd and even field have to be set to:

   $$YP_{even} = YP_{odd} + \frac{YSCI}{32};$$

   where line 1 = odd.

In modes 1 and 2 the first input line is fed to the output (without processing) so that the number of output lines equals the number of input lines.

7.4.2.3 Flip option (FLIP = 1)

For both vertical scaling modes there is a flip option (mirroring) available for input lines with a maximum of 384 pixels. In the event that full screen pictures (e.g. 768 × 576) are to be flipped, they first have to be scaled down to 384 pixels per line in the horizontal prescaling unit. After vertical processing (flipping) they can be rezoomed to the original 768 pixels per line in the following VPD. It should be noted that when using the flip option, the last input line can not be displayed at the output.

7.4.3 Horizontal variable phase scaling

In the phase-correct horizontal variable phase scaling the pixels are calculated for the geometrical correct, orthogonal output pattern, down to ¼ of the prescaled pattern. In addition, a horizontal zooming feature is supported. The maximum zooming factor is at least 2, thus being even more dependent on input pattern and prescaling settings.

The phase scaling consists of a filter and arithmetic structure with 10 taps for the luminance and 4 taps for the chrominance processing. It is able to generate a phase-correct new pixel value, with virtually no phase or amplitude artefacts.

The new samples are calculated with a phase accuracy of $^1/_{64}$ of the pixel distance.

When using this circuit the up and down scaling is controlled by the I²C-bus parameters XSCI and XP. Because the variable phase scaling is restricted to downscale >¼ of the fine scalers input pixel count, XSCI is also a function of the prescaling parameter XPSC.

As N_{IP} = number of input pixels per line (at SAA7140A input) and N_{OP} = number of desired output pixels/line, XSCI is defined by the following equation:

$$XSCI = INT\left[\frac{N_{IP}}{N_{OP}} \times \frac{1024}{(XPSC + 1)}\right]$$

The maximum value of XSCI = 4095. Zooming is performed for XSCI values less than 1024. The number of disqualified clock cycles between consecutive pixel qualifiers (at the phase scalers input) defines the maximum possible zoom factor. This means that zooming may also be a function of XPSC. It should be noted that implementation is dependent on a zooming factor greater than 2. Some artefacts may occur at the end of the zoomed line.

Internal rounding effects, may result in a deviation of ±1 output pixels compared to the expected result. In this situation, the I²C-bus parameter XP can be used to shift the starting phase of the phase calculation and thereby force an additional cycle to be disqualified.

In addition, when XP ≥ 128 it will force the internal phase calculation to fixed values, especially when XP = 128 it will force the phase scaler into bypass.

The scaled output data is fed back to the data formatter/reformatter unit and may be used as output signals from the bidirectional expansion port (if the mode is selected).

7.5 Colour Space Matrix (CSM), dither and gamma correction

The scaled YUV output data can be converted after Interpolation into RGB data in accordance with CCIR 601 recommendations.

The matrix equations considering the digital quantization are as follows;

$R = Y + 1.375\ V$

$G = Y - 0.703125\ V - 0.34375\ U$

$B = Y + 1.734375\ U$

For error diffusion a dither algorithm of the 5-bit truncation error RGB (5, 5, 5) is implemented.

An anti-gamma characteristic ($\gamma = 1.4$) is implemented at the matrix output to provide anti-gamma correction of the RGB data. The curve can be used (bit RTB = 0) to compensate gamma correction for linear data representation of the RGB output data.

The chroma signal keyer generates an alpha signal to achieve an RGB (5, 5, 5) + α output signal. Therefore, the processed UV data amplitudes are compared with thresholds set via the I²C-bus. A logic 1 signal is generated if the amplitude is within the specified amplitude range, if the amplitude is outside the specified range a logic 0 is generated. Keying can be switched off by setting the lower limit higher than the upper limit.

For 16-bit YUV data formats or monochrome modes the CSM block is bypassed.

7.6 Output formatter and output FIFO register

In order to support various scaling applications, the output data at the VRAM port can be delivered in different formats and different transfer modes. Besides the 16-bit YUV format (see Section 7.1.1) the VRAM port also supports the data formats 24-bit RGB, 2 × 15-bit RGB + α or 8-bit grey scale.

Should the synchronous data transfer mode (transparent mode) be selected, the VRAM port will provide VCLK clock (clock rate of LLC) and PXQ (polarity via programming) on extra pins for use by the circuitry receiving the VRAM port data stream.

To ease frame buffer applications, an asynchronous transfer (burst or FIFO mode) can be selected. In this mode the VRAM ports VCLK has to be provided from an external source, with a maximum clock rate of 32 MHz. Only valid data is collected and transported.

7.6.1 Data formats and reference signals of the VRAM port

7.6.1.1 16-bit YUV (see Section 7.1.1)

The ordering of YUV bits and bytes at the VRAM port is identical to that of the SAA7196.

7.6.1.2 24-bit RGB:

The resampled YUV samples are converted into RGB (8 bits each). All three components have the same sample rate as luminance Y. Anti-gamma correction is available (programming). The alpha bit is generated as the chroma key in the UV domain.

Two RGB representations (code meanings) are supported:

1. The CCIR 601 orientated RGB representation defines code 16 for black and code 235 for full saturation.
2. The graphics display orientated RGB representation codes black with 00H and white with FFH.
   This representation can be achieved by corresponding programming of brightness (equals offset), contrast and saturation (equals gain) in the YUV domain.
   This format is used in the transparent mode and in the FIFO mode (one pixel at a time).

7.6.1.3 15-bit RGB (5, 5, 5) + α in 2 bytes

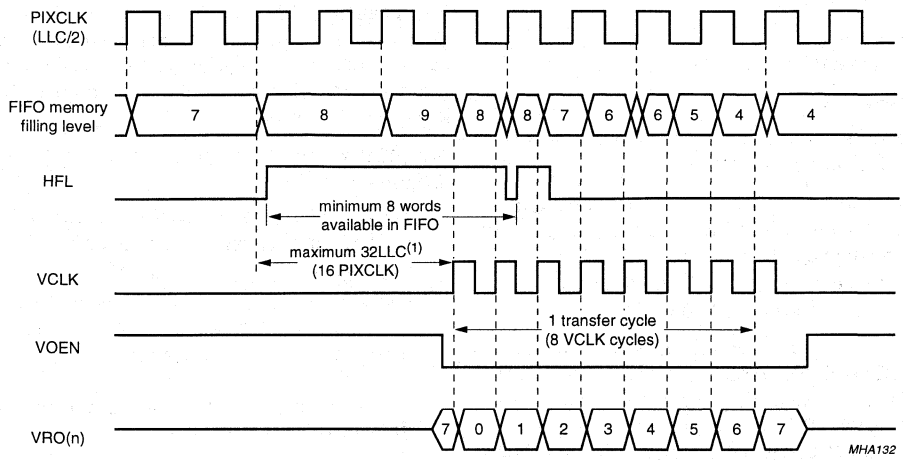
The resampled YUV samples are converted into 24-bit RGB. The following truncation to 5 bits is optionally (programming) performed with dithering effect (error diffusion). There are two representations (code meanings) supported; CCIR and graphics display orientated (see Section 7.6.1.2). The alpha bit is generated as chroma key in the YUV domain. This format is used in the transparent mode and in the FIFO mode (one pixel at a time, or two pixels at a time). The ordering of RGB bits and bytes at the VRAM port is identical to that of the SAA7196.

7.6.1.4 8-bit grey scale

This is simply a Y = luminance signal which can be selected to be coded as binary, or all bits inverted. This format is used in the transparent mode and in the FIFO mode (1, 2 or 4 pixels at a time).

The horizontal sync output HGTV marks (source independent) the range of the active video at the VRAM port.

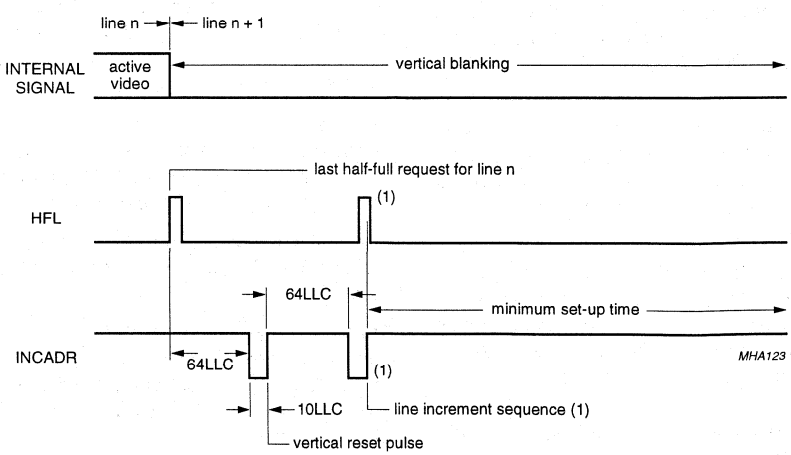
The vertical sync output VSYV (I²C-bus controlled polarity) carries the vertical sync information for the VRAM port output data (positive or negative pulse with a length of 4 lines). At the falling or rising edge of VSYV the FLDV output is stable.



If VCLK cycles occur at VOEN = HIGH the FIFO register is unchanged but the outputs VRO31 to VRO0 remain in the 3-state position.

(1) Only valid for non-zoomed data.

Fig.17 Output port transfer to VRAM at 32-bit data format without scaling.



(1) Only available for interfaced processing at the beginning of an odd field.

Fig.18 Vertical reset timing of the VRAM port.

7.7 Data transfer modes

7.7.1 EXPANSION PORT MODES

The expansion port is controlled by I²C-bus subaddresses 02 (22H) and 03 (23H).

The expansion port can be configured in a very flexible way. Table 3 gives examples of the I²C-bus programming for several expansion port configurations. SAA7196 compatible modes are marked as 'xx96' in the MODE column. After reset the expansion port reference signal inputs are set to the 'xxIO' pins.

After reset the expansion port reference signal inputs are set to the 'xxIO' pins.

Pin FDIO can be used in the same way as the DIR pin of the SAA7196 if the I²C-bus bit FLDC is set to logic 1.

More information concerning the control signals can be found in Chapter 8. For correct application the user should first decide about some global interface properties before referring to this chapter such as:

- Does the application require separate input and output reference signal lines, if yes then I²C-bus bit SRIO = 0
- Does the application need hardware controlled I/O switching, if yes then I²C-bus bit FLDC = 1 and use of pin FDIO or
- Does software controlled I/O switching (register set controlled) the same job, if yes then I²C-bus bit FLDC = 0
- Which signal path defines the clock system
- Which signal path is the synchronization master
- Is dynamic field-wise switching required or is the source switching quite static, if static then do not be confused about odd or even; use SREGS and IREGS before referring to the I²C-bus section.

Table 3 Expansion port programming examples

MODE	FDIO	DAVE OUTPUT CONTROL [SUBADDRESS 02 (22H)]									SCALER INPUT CONTROL [SUBADDRESS 03 (23H)]					I/O
		YUV8 04 to 24H	FLDC	VIDC	VD1	VD0	HD1	HD0	PXQD	LLCD	SRIO	VSI	HSI	VIPSI	LLCS	
0	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	note 1
1	X	0	0	1	0	0	0	0	0	0	0	0	0	1	0	note 2
2	X	0	0	1	X	1	x	1	0	1	0	1	1	1	1	note 3
3	X	0	0	1	X	1	X	1	0	0	0	1	1	1	0	note 4
4	X	0	0	0	1	0	1	0	1	0	0	0	0	0	0	note 5
5	X	1	0	0	1	0	1	0	1	0	0	0	0	1	0	note 6
6	X	1	0	0	0	0	0	0	0	0	0	1	1	1	1	note 7
7	X	1	0	0	1	0	1	0	1	1	0	1	1	1	1	note 8
8	X	0	0	1	0	0	0	0	0	0	0	0	1	1	0	note 9
9	X	1	0	1	X	X	X	X	X	X	1	1	1	1	1	note 10
0 '96	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	note 11
1 '96	1	0	1	0	0	0	0	0	0	0	1	0	0	0	0	note 12
2 '96	1	0	1	1	x	X	X	X	X	X	1	1	1	1	1	note 13
3 '96	x	0	1	1	x	X	X	1	0	0	1	1	1	0	0	note 14
4 '96	1	0	1	1	0	0	X	X	X	0	1	0	1	1	0	note 15
5 '96	0	0	1	0	0	0	X	X	X	0	1	0	0	1	1	note 16
6 '96	1	0	1	0	0	0	X	X	X	0	1	0	0	1	1	note 17
																note 18

Notes

1. Scaler input from LLC, Y/UVIN, CREF, HREF and VS; expansion port output clock, data, qualifier, horizontal and vertical reference derived from LLC, Y/UVIN, CREF, HREF and VS.
2. Scaler input from LLC, VIDHIL, PXQIN, HREF and VS; expansion port output clock, data, qualifier, horizontal and vertical reference derived from LLC, d.c., CREF, HREF and VS.
3. Scaler input from LLCIN, VIDHIL, PXQIN, HIN and VIN; expansion port output clock, data, qualifier, horizontal and vertical reference derived from LLCIN, d.c., CREF, HIN and VIN.
4. Scaler input from LLC, VIDHIL, PXQIN, HIN and VIN; expansion port output clock, data, qualifier, horizontal and vertical reference derived from LLC, d.c., CREF, HIN and VIN.

5. Scaler input from LLC, YIUVIN, CREF, HREF and VS; expansion port output clock, data, qualifier, horizontal and vertical reference derived from LLC, YUVsc, Psc, Hsc and Vsc.
6. Scaler input from LLC, VIDL, PXQIN, HREF and VS; expansion port output clock, data, qualifier, horizontal and vertical reference derived from LLC, YUVsc->VIDH, Psc, Hsc and Vsc.
7. Scaler input from LLCIN, VIDL, PXQIN, HIN and VIN; expansion port output clock, data, qualifier, horizontal and vertical reference derived from LLC, YIUVIN->VIDH, C+HREF and VS.
8. Scaler input from LLCIN, VIDL PXQIN, HIN and VIN; expansion port output clock, data, qualifier, horizontal and vertical reference derived from LLCIN, YUVsc->VIDH, Psc, Hsc and Vsc.
9. Scaler input from LLC, VIDHIL PXQIN, HIN and VS; expansion port output clock, data, qualifier, horizontal and vertical reference derived from LLC, d.c., CREF, HREF and VS.
10. Scaler input from LLCIO, VIDH, PXQIO, HIO and VIO; expansion port output clock, data, qualifier, horizontal and vertical reference derived from d.c., d.c., d.c., d.c. and d.c..
11. Scaler input from LLC, YIUVIN, CREF, HREF and VS; expansion port output clock, data, qualifier, horizontal and vertical reference derived from LLC, YIUVIN, CREF, HREF and VS.
12. Scaler input from LLC, VIDHIL, CREF, HREF and VS; expansion port output clock, data, qualifier, horizontal and vertical reference derived from LLC, d.c., CREF, HREF and VS.
13. Scaler input from LLCIO, VIDHIL, PXQIO, HIO and VIO; expansion port output clock, data, qualifier, horizontal and vertical reference derived from d.c., d.c., d.c., d.c. and d.c..
14. Scaler input from LLC, VIDHIL, CREF, HIO and VIO; expansion port output clock, data, qualifier, horizontal and vertical reference derived from LLC, d.c., CREF, d.c. and d.c.
15. Scaler input from LLC, VIDH/L, PXQIO, HIO and VS; expansion port output clock, data, qualifier, horizontal and vertical reference derived from LLC, d.c., d.c., d.c., HREF and VS.
16. Scaler input from LLC, Y/UVIN, CREF, HREF and VS; expansion port output clock, data, qualifier, horizontal and vertical reference derived from LLC, Y/UVIN, CREF, HREF and VS.
17. Scaler input from LLCIO, VIDH/L, PXQIO, HREF and VS; expansion port output clock, data, qualifier, horizontal and vertical reference derived from d.c., d.c., d.c., HREF and VS.
18. Fill in user specific configuration.

7.8 VRAM port modes

7.8.1 Data burst transfer mode (FIFO Mode)

Data transfer on the VRAM port is asynchronous (TTR = 0). This mode can be used for all output formats. Four signals for communication with the external memory are provided:

1. HFL flag: the half-full flag of the FIFO output register is raised when the FIFO contains at least 8 data words (HFL = HIGH). By setting HFL to logic 1, the SAA7140A and SAA7140B requests a data burst transfer, via the external memory controller, that has to start a transfer cycle within the next 32LLC cycles for 32-bit long word modes (16LLC cycles for 16 and 24-bit modes). If there are pixels in the FIFO at the end of the line, which are not transferred, the circuit fills up the FIFO register with 'fill pixels' until it is half-full and sets the HFL flag to request a data burst transfer. After the transfer is completed, HFL is used in combination with INCADR to indicate the line increments.
2. The INCADR output signal is used in combination with HFL to control horizontal and vertical address generation for a memory controller. The pulse sequence depends on field formats (interlace/non-interlace or odd/even fields) and control bits OF1 and OF0 (subaddress 01). This means that:
   a) HFL = 1 at the rising edge of INCADR: the END OF LINE is reached; request for line address increment
   b) HFL = 0 at the rising edge of INCADR: the END OF FIELD/FRAME is reached; request for line and pixel address reset
3. VCLK input signal to clock the FIFO register output data VRO(n). New data is placed on the VRO(n) port with the rising edge of VCLK (see Fig.17).
4. The VOEN input enables output data VRO(n). The outputs are in 3-state mode at VOEN = HIGH. VOEN changes only when VCLK is LOW. If VCLK pulses are applied when VOEN is HIGH, the outputs remain inactive but the FIFO register accepts the pulses.

7.8.2 Continuous data transfer mode (transparent mode)

Data transfer on the VRAM port can be achieved synchronously (TTR = 1), controlled by output reference signals at separate pins (except the α-signal) and a continuous clock output signal (clock rate of LLC) on the VCLK pin.

The SAA7140A and SAA7140B delivers a continuously processed data stream. Consequently, the extended formats of the VRAM port output are selected (bit FS2 = 1; see Tables 6 and 7).

The output reference signals have to be used to buffer qualified preprocessed RGB or YUV video data. The YUV data is only valid in qualified time slots. Control output signals (see Tables 6 and 7) are:

- α = keying signal of the chroma keyer (not on extra pin but in lower byte of VRO output)
- FLDV = odd/even field bit in accordance with the internal field processing
- VSYV = vertical sync signal, active polarity is defined by VSYP bit
- HGTV = horizontal gate signal, logic 1 marks the horizontal direction from XO to (XO + XS) lines
- PXQV = pixel qualifier signal, active polarity is defined by QPP bit.

Interlaced processing (OF bits, subaddress 01): to support correctly interlaced data storage, the scaler delivers two INCADR/HFL sequences in each qualified line and an additional INCADR/HFL sequence after the vertical reset sequence at the beginning of an odd field. Consequently, the scaled lines are automatically stored in the right sequence.

INCADR timing: the distance from the last half-full request (HFL) to the INCADR pulse may be longer than 64LLC. The state of HFL is defined for minimum 2LLC cycles afterwards.

Monochrome format (see Tables 6 and 7); If TTR = 1 and FS2 = 1 then Ya = Yb.

7.8.3 I²C-bus controlled pseudo sleep mode

To reduce the power consumption of the SAA7140A and SAA7140B during phases, where no scaling operations are requested in the application, it is possible to switch the SAA7140A and SAA7140B into a pseudo sleep mode.

This mode can be activated, if the clock input LLCIN is not used or if the hardware is able to pull the LLCIN input or the LLCIO pin (in input mode) down to logic 0.

In applications, which do not use LLCIN, then LLCIN should be connected to ground.

LLC has to be provided continuously.

To activate the 'Sleep Mode' the scalers processing has to be switched to one of the inactive clock inputs of the expansion port. For example, If LLCIO is used as input and output in the application then:

LLCIN grounded => 'Sleep Mode' is active, if I²C-bus bits FLDC = 0, SRIO = 0 and LLCS = 1.

and If LLCIN is used as input and LLCIO is used as output:

LLCIN pulled down => 'Sleep Mode' is active, if I²C-bus bits FLDC = 0, SRIO = 0 and LLCS = 1.

LLCIO pulled down => 'Sleep Mode' is active, if I²C-bus bits FLDC = 0, SRIO = 1 and LLCS = 1.

To activate the scaler again, switch back to an active input clock, via SRIO and/or LLCS.

In 'Sleep Mode' the power consumption of the SAA7140A and SAA7140B is reduced to approximately 15% of its normal operational value.

Table 4 VRAM port output data formats (VRO31 to VRO16) at FS2 bit = 0 and VOF bit = 1 (can be set via I²C-bus), burst mode only, Pixel order = n, n + 1, n + 2, etc.

PIXEL OUTPUT BITS	FS1 = 0; FS0 = 0 RGB (5, 5, 5) + α 32-BIT WORDS(1)(2)			FS1 = 0; FS0 = 1 YUV 4 : 2 : 2 32-BIT WORDS(2)(3)			FS1 = 1; FS0 = 0 YUV 4 : 2 : 2 16-BIT WORDS(2)(3)			FS1 = 1; FS0 = 1 8-BIT MONOCHROME 32-BIT WORDS(4)		
	n	n + 2	n + 4	n	n + 2	n + 4	n	n + 1	n + 2	n n + 1	n + 4 n + 5	n + 8 n + 9
VRO31	α	α	α	Y_{e7}	Y_{e7}	Y_{e7}	Y_{e7}	Y_{o7}	Y_{e7}	Y_{a7}	Y_{a7}	Y_{a7}
VRO30	R4	R4	R4	Y_{e6}	Y_{e6}	Y_{e6}	Y_{e6}	Y_{o6}	Y_{e6}	Y_{a6}	Y_{a6}	Y_{a6}
VRO29	R3	R3	R3	Y_{e5}	Y_{e5}	Y_{e5}	Y_{e5}	Y_{o5}	Y_{e5}	Y_{a5}	Y_{a5}	Y_{a5}
VRO28	R2	R2	R2	Y_{e4}	Y_{e4}	Y_{e4}	Y_{e4}	Y_{o4}	Y_{e4}	Y_{a4}	Y_{a4}	Y_{a4}
VRO27	R1	R1	R1	Y_{e3}	Y_{e3}	Y_{e3}	Y_{e3}	Y_{o3}	Y_{e3}	Y_{a3}	Y_{a3}	Y_{a3}
VRO26	R0	R0	R0	Y_{e2}	Y_{e2}	Y_{e2}	Y_{e2}	Y_{o2}	Y_{e2}	Y_{a2}	Y_{a2}	Y_{a2}
VRO25	G4	G4	G4	Y_{e1}	Y_{e1}	Y_{e1}	Y_{e1}	Y_{o1}	Y_{e1}	Y_{a1}	Y_{a1}	Y_{a1}
VRO24	G3	G3	G3	Y_{e0}	Y_{e0}	Y_{e0}	Y_{e0}	Y_{o0}	Y_{e0}	Y_{a0}	Y_{a0}	Y_{a0}
VRO23	G2	G2	G2	U_{e7}	U_{e7}	U_{e7}	U_{e7}	V_{e7}	U_{e7}	Y_{b7}	Y_{b7}	Y_{b7}
VRO22	G1	G1	G1	U_{e6}	U_{e6}	U_{e6}	U_{e6}	V_{e6}	U_{e6}	Y_{b6}	Y_{b6}	Y_{b6}
VRO21	G0	G0	G0	U_{e5}	U_{e5}	U_{e5}	U_{e5}	V_{e5}	U_{e5}	Y_{b5}	Y_{b5}	Y_{b5}
VRO20	B4	B4	B4	U_{e4}	U_{e4}	U_{e4}	U_{e4}	V_{e4}	U_{e4}	Y_{b4}	Y_{b4}	Y_{b4}
VRO19	B3	B3	B3	U_{e3}	U_{e3}	U_{e3}	U_{e3}	V_{e3}	U_{e3}	Y_{b3}	Y_{b3}	Y_{b3}
VRO18	B2	B2	B2	U_{e2}	U_{e2}	U_{e2}	U_{e2}	V_{e2}	U_{e2}	Y_{b2}	Y_{b2}	Y_{b2}
VRO17	B1	B1	B1	U_{e1}	U_{e1}	U_{e1}	U_{e1}	V_{e1}	U_{e1}	Y_{b1}	Y_{b1}	Y_{b1}
VRO16	B0	B0	B0	U_{e0}	U_{e0}	U_{e0}	U_{e0}	V_{e0}	U_{e0}	Y_{b0}	Y_{b0}	Y_{b0}

Notes

1. α = keying bit.
2. RGB and YUV = digital signals.
3. e = even pixel numbers.
4. a and b = consecutive pixels.

Table 5 VRAM port output data formats (VRO15 to VRO0) at FS2 bit = 0 and VOF bit = 1 (can be set via I²C-bus), burst mode only, Pixel order = n, 1n, 2n, etc.

PIXEL OUTPUT BITS	FS1 = 0; FS0 = 0 RGB (5, 5, 5) + α 32-BIT WORDS(1)(2)			FS1 = 0; FS0 = 1 YUV 4 : 2 : 2 32-BIT WORDS(2)(3)(4)			FS1 = 1; FS0 = 0 YUV 4 : 2 : 2 16-BIT WORDS(2)			FS1 = 1; FS0 = 1 8-BIT MONOCHROME 32-BIT WORDS(5)		
	n + 1	n + 3	n + 5	n + 1	n + 3	n + 5	OUTPUT NOT USED			n + 2 n + 3	n + 6 n + 7	n + 10 n + 11
VRO15	α	α	α	Y_{o7}	Y_{o7}	Y_{o7}	X	X	X	Y_{c7}	Y_{c7}	Y_{c7}
VRO14	R4	R4	R4	Y_{o6}	Y_{o6}	Y_{o6}	X	X	X	Y_{c6}	Y_{c6}	Y_{c6}
VRO13	R3	R3	R3	Y_{o5}	Y_{o5}	Y_{o5}	X	X	X	Y_{c5}	Y_{c5}	Y_{c5}
VRO12	R2	R2	R2	Y_{o4}	Y_{o4}	Y_{o4}	X	X	X	Y_{c4}	Y_{c4}	Y_{c4}
VRO11	R1	R1	R1	Y_{o3}	Y_{o3}	Y_{o3}	X	X	X	Y_{c3}	Y_{c3}	Y_{c3}
VRO10	R0	R0	R0	Y_{o2}	Y_{o2}	Y_{o2}	X	X	X	Y_{c2}	Y_{c2}	Y_{c2}
VRO9	G4	G4	G4	Y_{o1}	Y_{o1}	Y_{o1}	X	X	X	Y_{c1}	Y_{c1}	Y_{c1}
VRO8	G3	G3	G3	Y_{o0}	Y_{o0}	Y_{o0}	X	X	X	Y_{c0}	Y_{c0}	Y_{c0}
VRO7	G2	G2	G2	V_{e7}	V_{e7}	V_{e7}	X	X	X	Y_{d7}	Y_{d7}	Y_{d7}
VRO6	G1	G1	G1	V_{e6}	V_{e6}	V_{e6}	X	X	X	Y_{d6}	Y_{d6}	Y_{d6}
VRO5	G0	G0	G0	V_{e5}	V_{e5}	V_{e5}	X	X	X	Y_{d5}	Y_{d5}	Y_{d5}
VRO4	B4	B4	B4	V_{e4}	V_{e4}	V_{e4}	X	X	X	Y_{d4}	Y_{d4}	Y_{d4}
VRO3	B3	B3	B3	V_{e3}	V_{e3}	V_{e3}	X	X	X	Y_{d3}	Y_{d3}	Y_{d3}
VRO2	B2	B2	B2	V_{e2}	V_{e2}	V_{e2}	X	X	X	Y_{d2}	Y_{d2}	Y_{d2}
VRO1	B1	B1	B1	V_{e1}	V_{e1}	V_{e1}	X	X	X	Y_{d1}	Y_{d1}	Y_{d1}
VRO0	B0	B0	B0	V_{e0}	V_{e0}	V_{e0}	X	X	X	Y_{d0}	Y_{d0}	Y_{d0}

Notes

1. α = keying bit.
2. RGB and YUV = digital signals.
3. o = odd pixel numbers.
4. e = even pixel numbers.
5. c and d = consecutive pixels.

Table 6 VRAM port output data formats (VRO31 to VRO16) at FS2 bit = 1 and VOF bit = 1 (can be set via I²C-bus), burst and transparent mode, Pixel order = n, n + 1, n + 2, etc.

PIXEL OUTPUT BITS	FS1 = 0; FS0 = 0 RGB (5, 5, 5) + α 16-BIT WORDS[1][2]			FS1 = 0; FS0 = 1 YUV 4 : 2 : 2 16-BIT WORDS[2][3]			FS1 = 1; FS0 = 0 RGB (8, 8, 8) 24-BIT WORDS[2]			FS1 = 1; FS0 = 1 8-BIT MONOCHROME 16-BIT WORDS[4]		
	n	n + 1	n + 2	n	n + 1	n + 2	n	n + 1	n + 2	n n + 1	n + 2 n + 3	n + 4 n + 5
VRO31	α	α	α	Y_{e7}	Y_{e7}	Y_{e7}	R7	R7	R7	Y_{a7}	Y_{a7}	Y_{a7}
VRO30	R4	R4	R4	Y_{e6}	Y_{e6}	Y_{e6}	R6	R6	R6	Y_{a6}	Y_{a6}	Y_{a6}
VRO29	R3	R3	R3	Y_{e5}	Y_{e5}	Y_{e5}	R5	R5	R5	Y_{a5}	Y_{a5}	Y_{a5}
VRO28	R2	R2	R2	Y_{e4}	Y_{e4}	Y_{e4}	R4	R4	R4	Y_{a4}	Y_{a4}	Y_{a4}
VRO27	R1	R1	R1	Y_{e3}	Y_{e3}	Y_{e3}	R3	R3	R3	Y_{a3}	Y_{a3}	Y_{a3}
VRO26	R0	R0	R0	Y_{e2}	Y_{e2}	Y_{e2}	R2	R2	R2	Y_{a2}	Y_{a2}	Y_{a2}
VRO25	G4	G4	G4	Y_{e1}	Y_{e1}	Y_{e1}	R1	R1	R1	Y_{a1}	Y_{a1}	Y_{a1}
VRO24	G3	G3	G3	Y_{e0}	Y_{e0}	Y_{e0}	R0	R0	R0	Y_{a0}	Y_{a0}	Y_{a0}
VRO23	G2	G2	G2	U_{e7}	U_{e7}	U_{e7}	G7	G7	G7	Y_{b7}	Y_{b7}	Y_{b7}
VRO22	G1	G1	G1	U_{e6}	U_{e6}	U_{e6}	G6	G6	G6	Y_{b6}	Y_{b6}	Y_{b6}
VRO21	G0	G0	G0	U_{e5}	U_{e5}	U_{e5}	G5	G5	G5	Y_{b5}	Y_{b5}	Y_{b5}
VRO20	B4	B4	B4	U_{e4}	U_{e4}	U_{e4}	G4	G4	G4	Y_{b4}	Y_{b4}	Y_{b4}
VRO19	B3	B3	B3	U_{e3}	U_{e3}	U_{e3}	G3	G3	G3	Y_{b3}	Y_{b3}	Y_{b3}
VRO18	B2	B2	B2	U_{e2}	U_{e2}	U_{e2}	G2	G2	G2	Y_{b2}	Y_{b2}	Y_{b2}
VRO17	B1	B1	B1	U_{e1}	U_{e1}	U_{e1}	G1	G1	G1	Y_{b1}	Y_{b1}	Y_{b1}
VRO16	B0	B0	B0	U_{e0}	U_{e0}	U_{e0}	G0	G0	G0	Y_{b0}	Y_{b0}	Y_{b0}

Notes

1. α = keying bit.
2. RGB and YUV = digital signals.
3. e = even pixel numbers.
4. a and b = consecutive pixels.

Table 7 VRAM port output data formats (VRO15 to VRO0) at FS2 bit = 1 and VOF bit = 1 (can be set via I²C-bus), burst and transparent mode, Pixel order = n, n + 1, n + 2, etc.

PIXEL OUTPUT BITS	FS1 = 0; FS0 = 0 RGB (5, 5, 5) + α 16-BIT WORDS[1][2]			FS1 = 0; FS0 = 1 YUV 4 : 2 : 2 16-BIT WORDS[1][2]			FS1 = 1; FS0 = 0 RGB (8, 8, 8) 24-BIT WORDS[1][2]			FS1 = 1; FS0 = 1 8-BIT MONOCHROME 16-BIT WORDS[1]		
	n	n + 1	n + 2	n	n + 1	n + 2	n	n + 1	n + 2	n n + 1	n + 2 n + 3	n + 4 n + 5
VRO15	X	X	X	X	X	X	B7	B7	B7	X	X	X
VRO140	X	X	X	X	X	X	B6	B6	B6	X	X	X
VRO13	X	X	X	X	X	X	B5	B5	B5	X	X	X
VRO12	X	X	X	X	X	X	B4	B4	B4	X	X	X
VRO11	X	X	X	X	X	X	B3	B3	B3	X	X	X
VRO10	X	X	X	X	X	X	B2	B2	B2	X	X	X
VRO9	X	X	X	X	X	X	B1	B1	B1	X	X	X
VRO8	X	X	X	X	X	X	B0	B0	B0	X	X	X
VRO7	α	α	α	α	α	α	α	α	α	α	α	α
VRO6	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)
VRO5	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)
VRO4	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)
VRO3	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)
VRO2	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)
VRO1	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)
VRO0	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)	(α)

Notes

1. α = keying bit.
2. RGB = digital signals.

Table 8 Optional VRAM port output data formats (VRO31 to VRO16) at FS2 bit = 0 and VOF bit = 0 (can be set via I²C-bus), burst mode only; Pixel order = n, n + 1, n + 2, etc.; VMUX = 1 or 0

PIXEL OUTPUT BITS	FS1 = 0, FS0 = 0 RGB (5, 5, 5) + α 32-BIT LONG WORD[1][2][3]				FS1 = 0, FS0 = 1 YUV 4 : 2 : 2 32-BIT LONG WORD[2][4]				FS1 = 1, FS0 = 1 8-BIT MONOCHROME 32-BIT LONG WORD[5]			
	n		n + 2		n		n + 2		n n + 1		n + 4 n + 5	
	1	0	1	0	1	0	1	0	1	0	1	0
VRO31	α	Z	α	Z	Y_{e7}	Z	Y_{e7}	Z	Y_{a7}	Z	Y_{a7}	Z
VRO30	R4	Z	R4	Z	Y_{e6}	Z	Y_{e6}	Z	Y_{a6}	Z	Y_{a6}	Z
VRO29	R3	Z	R3	Z	Y_{e5}	Z	Y_{e5}	Z	Y_{a5}	Z	Y_{a5}	Z
VRO28	R2	Z	R2	Z	Y_{e4}	Z	Y_{e4}	Z	Y_{a4}	Z	Y_{a4}	Z
VRO27	R1	Z	R1	Z	Y_{e3}	Z	Y_{e3}	Z	Y_{a3}	Z	Y_{a3}	Z
VRO26	R0	Z	R0	Z	Y_{e2}	Z	Y_{e2}	Z	Y_{a2}	Z	Y_{a2}	Z
VRO25	G4	Z	G4	Z	Y_{e1}	Z	Y_{e1}	Z	Y_{a1}	Z	Y_{a1}	Z
VRO24	G3	Z	G3	Z	Y_{e0}	Z	Y_{e0}	Z	Y_{a0}	Z	Y_{a0}	Z
VRO23	G2	Z	G2	Z	U_{e7}	Z	U_{e7}	Z	Y_{b7}	Z	Y_{b7}	Z
VRO22	G1	Z	G1	Z	U_{e6}	Z	U_{e6}	Z	Y_{b6}	Z	Y_{b6}	Z
VRO21	G0	Z	G0	Z	U_{e5}	Z	U_{e5}	Z	Y_{b5}	Z	Y_{b5}	Z
VRO20	B4	Z	B4	Z	U_{e4}	Z	U_{e4}	Z	Y_{b4}	Z	Y_{b4}	Z
VRO19	B3	Z	B3	Z	U_{e3}	Z	U_{e3}	Z	Y_{b3}	Z	Y_{b3}	Z
VRO18	B2	Z	B2	Z	U_{e2}	Z	U_{e2}	Z	Y_{b2}	Z	Y_{b2}	Z
VRO17	B1	Z	B1	Z	U_{e1}	Z	U_{e1}	Z	Y_{b1}	Z	Y_{b1}	Z
VRO16	B0	Z	B0	Z	U_{e0}	Z	U_{e0}	Z	Y_{b0}	Z	Y_{b0}	Z

Notes

1. α = keying bit.
2. RGB and YUV = digital signals.
3. Z = high ohmic (3-state).
4. e = even pixel numbers.
5. a and b = consecutive pixels.

Table 9 Optional VRAM port output data formats (VRO15 to VRO0) at FS2 bit = 0 and VOF bit = 0 (can be set via I²C-bus), burst mode only; Pixel order = n, n + 1, n + 2, etc.; VMUX = 1 or 0

PIXEL OUTPUT BITS	FS1 = 0, FS0 = 0 RGB (5, 5, 5) + α 32-BIT LONG WORD[1][2][3]				FS1 = 0, FS0 = 1 YUV 4 : 2 : 2 32-BIT LONG WORD[2][3][4][5]				FS1 = 1, FS0 = 1 8-BIT MONOCHROME 32-BIT LONG WORD[3][6]			
		n + 1		n + 3		n + 1		n + 3		n + 2 n + 3		n + 6 n + 7
	1	0	1	0	1	0	1	0	1	0	1	0
VRO15	Z	α	Z	α	Z	Y_{o7}	Z	Y_{o7}	Z	Y_{c7}	Z	Y_{c7}
VRO14	Z	R4	Z	R4	Z	Y_{o6}	Z	Y_{o6}	Z	Y_{c6}	Z	Y_{c6}
VRO13	Z	R3	Z	R3	Z	Y_{o5}	Z	Y_{o5}	Z	Y_{c5}	Z	Y_{c5}
VRO12	Z	R2	Z	R2	Z	Y_{o4}	Z	Y_{o4}	Z	Y_{c4}	Z	Y_{c4}
VRO11	Z	R1	Z	R1	Z	Y_{o3}	Z	Y_{o3}	Z	Y_{c3}	Z	Y_{c3}
VRO10	Z	R0	Z	R0	Z	Y_{o2}	Z	Y_{o2}	Z	Y_{c2}	Z	Y_{c2}
VRO9	Z	G4	Z	G4	Z	Y_{o1}	Z	Y_{o1}	Z	Y_{c1}	Z	Y_{c1}
VRO8	Z	G3	Z	G3	Z	Y_{o0}	Z	Y_{o0}	Z	Y_{c0}	Z	Y_{c0}
VRO7	Z	G2	Z	G2	Z	V_{e7}	Z	V_{e7}	Z	Y_{d7}	Z	Y_{d7}
VRO6	Z	G1	Z	G1	Z	V_{e6}	Z	V_{e6}	Z	Y_{d6}	Z	Y_{d6}
VRO5	Z	G0	Z	G0	Z	V_{e5}	Z	V_{e5}	Z	Y_{d5}	Z	Y_{d5}
VRO4	Z	B4	Z	B4	Z	V_{e4}	Z	V_{e4}	Z	Y_{d4}	Z	Y_{d4}
VRO3	Z	B3	Z	B3	Z	V_{e3}	Z	V_{e3}	Z	Y_{d3}	Z	Y_{d3}
VRO2	Z	B2	Z	B2	Z	V_{e2}	Z	V_{e2}	Z	Y_{d2}	Z	Y_{d2}
VRO1	Z	B1	Z	B1	Z	V_{e1}	Z	V_{e1}	Z	Y_{d1}	Z	Y_{d1}
VRO0	Z	B0	Z	B0	Z	V_{e0}	Z	V_{e0}	Z	Y_{d0}	Z	Y_{d0}

Notes

1. α = keying bit.
2. RGB and YUV = digital signals.
3. Z = high ohmic (3-state).
4. o = odd pixel numbers.
5. e = even pixel number.
6. c and d = consecutive pixels.

8 I²C-BUS PROTOCOL

8.1 I²C-bus format

Table 10 I²C-bus format

S	SLAVE ADDRESS	ACK	SUBADDRESS	ACK	DATA0	ACK	X	DATAn	ACK	P

Table 11 Description of I²C-bus format

CODE	DESCRIPTION
S	START condition
Slave address	0111 00X = IICSA = LOW or 0111 001X = IICSA = HIGH
ACK	acknowledge generated by the slave
Subaddress	subaddress byte (if more than 1 data byte is transmitted then an auto-increment of the subaddress is performed)
Data	data byte
P	STOP condition
X	read/write control bit: X = 0, order to write (the circuit is slave receiver) X = 1, order to read (the circuit is slave transmitter)

Table 12 I²C-bus status byte (X in address byte = 1; 71H at IICSA = LOW or 73H at IICSA = HIGH)

FUNCTION	DATA BITS							
	D7	D6	D5	D4	D3	D2	D1	D0
Status byte (subaddress 20H)	ID3	ID2	ID1	ID0	X	X	X	X

Table 13 Function of status bits ID3 to ID0 (software model of SAA7140A and SAA7140B compatible)

ID3	ID2	ID1	ID0	VERSION
0	0	0	0	V0 (first version)

Remark: With the exception of subaddress 20H (read only) all I²C-bus registers are read/write registers.

8.2 I²C-bus bitmap

Table 14 I²C-bus decoder control; subaddress and data bytes for writing (X in address byte = 0; 70H at IICSA = LOW or 72H at IICSA = HIGH); programming set A: subaddress = 02H to 1FH

FUNCTION SUBADDRESS		DATA BITS								
		D7	D6	D5	D4	D3	D2	D1	D0	DF[1]
Initial settings expansion/DMSD	00	FSEL	RSEN[4]	SREGS	IREGS	INVOE	REVFLD	FICO1	FICO0	
Initial settings VRAM	01	VPE	TTR[4]	VOF	QPP	OF1	OF0	LW1	LW0	
Expansion port output control	02	FLDC	VIDC	VD1	VD0	HD1	HD0	PXQD	LLCD	
Expansion I/O control; scaler source control	03	VSYP[4]	SRIO[4]	REHAW	REVAW	VSI	HSI	VIPSI	LLCS	
Expansion/VRAM format control	04	SHVS	YUV8	MCT	RTB	DIT	FS2	FS1	FS0	
Luminance brightness	05	BRIG7	BRIG6	BRIG5	BRIG4	BRIG3	BRIG2	BRIG1	BRIG0	
Luminance contrast	06	X	CONT6	CONT5	CONT4	CONT3	CONT2	CONT1	CONT0	
Chroma saturation	07	X	SATN6	SATN5	SATN4	SATN3	SATN2	SATN1	SATN0	
Horizontal window start[2]	08	XO7	XO6	XO5	XO4	XO3	XO2	XO1	XO0	
Horizontal window length[2]	09	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	
(continue)	0A	X	XO10	XO9	XO8	X	XS10	XS9	XS8	
Horizontal phase offset	0B	XP7	XP6	XP5	XP4	XP3	XP2	XP1	XP0	
Vertical window start[3]	0C	YO7	YO6	YO5	YO4	YO3	YO2	YO1	YO0	
Vertical window length[3]	0D	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	
(continue)	0E	X	YO10	YO9	YO8	X	YS10	YS9	YS8	
Vertical phase offset	0F	X	YP6[4]	YP5	YP4	YP3	YP2	YP1	YP0	
Horizontal prescaling	10	X	XACM[4]	XPSC5	XPSC4	XPSC3	XPSC2	XPSC1	XPSC0	
Horizontal weighting control (select Y)	11	CXY7	CXY6	CXY5	CXY4	CXY3	CXY2	CXY1	CXY0	
Horizontal weighting control (select UV)	12	CXUV7	CXUV6	CXUV5	CXUV4	CXUV3	CXUV2	CXUV1	CXUV0	
Prefilter YUV	13	PFUV3	PFUV2	PFUV1	PFUV0	PFY3	PFY2	PFY1	PFY0	
Vertical interpolation control	14	FLIP	YACM	YACL5	YACL4	YACL3	YACL2	YACL1	YACL0	
Vertical weighting control 1	15	CYA7	CYA6	CYA5	CYA4	CYA3	CYA2	CYA1	CYA0	
Vertical weighting control 2	16	CYB7	CYB6	CYB5	CYB4	CYB3	CYB2	CYB1	CYB0	
DC gain normalization	17	X	DCGX2	DCGX1	DCGX0	X	DCGY2	DCGY1	DCGY0	
Horizontal scaling increment	18	XSCI7	XSCI6	XSCI5	XSCI4	XSCI3	XSCI2	XSCI1	XSCI0	
(continue)	19	X	X	X	X	XSCI11	XSCI10	XSCI9	XSCI8	
Vertical scaling increment	1A	YSCI7	YSCI6	YSCI5	YSCI4	YSCI3	YSCI2	YSCI1	YSCI0	
(continue)	1B	X	X	X	X	X	X	YSCI9	YSCI8	

FUNCTION SUBADDRESS		DATA BITS								
		D7	D6	D5	D4	D3	D2	D1	D0	DF[1]
Chroma keying upper limit for V	1C	VU7	VU6	VU5	VU4	VU3	VU2	VU1	VU0	
Chroma keying lower limit for V	1D	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0	
Chroma keying upper limit for U	1E	UU7	UU6	UU5	UU4	UU3	UU2	UU1	UU0	
Chroma keying lower limit for U	1F	UL7	UL6	UL5	UL4	UL3	UL2	UL1	UL0	
Programming set B; subaddress = 22H to 3FH										
Read only register	20	ID3	ID2	ID1	ID0	X	X	X	X	
I/O port enable	21	PEN3[4]	PEN2[4]	PEN1[4]	PEN0[4]	PORT3	PORT2	PORT1	PORT0	
Expansion port output control	22	FLDC	VIDC	VD1	VD0	HD1	HD0	PXQD	LLCD	
Expansion I/O control; scaler source control	23	VSYP[4]	SRIO[4]	REHAW	REVAW	VSI	HSI	VIPSI	LLCS	
Expansion/VRAM format control	24	SHVS	YUV8	MCT	RTB	DIT	FS2	FS1	FS0	
Luminance brightness	25	BRIG7	BRIG6	BRIG5	BRIG4	BRIG3	BRIG2	BRIG1	BRIG0	
Luminance contrast	26	X	CONT6	CONT5	CONT4	CONT3	CONT2	CONT1	CONT0	
Chroma saturation	27	X	SATN6	SATN5	SATN4	SATN3	SATN2	SATN1	SATN0	
Horizontal window start[5]	28	XO7	XO6	XO5	XO4	XO3	XO2	XO1	XO0	
Horizontal window length[5]	29	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	
(continue)	2A	X	XO10	XO9	XO8	X	XS10	XS9	XS8	
Horizontal phase offset	2B	XP7	XP6	XP5	XP4	XP3	XP2	XP1	XP0	
Vertical window start[6]	2C	YO7	YO6	YO5	YO4	YO3	YO2	YO1	YO0	
Vertical window length[6]	2D	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	
(continue)	2E	X	YO10	YO9	YO8	X	YS10	YS9	YS8	
Vertical phase offset	2F	YPF	YP6[4]	YP5	YP4	YP3	YP2	YP1	YP0	
Horizontal prescaling	30	X	XACM[4]	XPSC5	XPSC4	XPSC3	XPSC2	XPSC1	XPSC0	
Horizontal weighting control (select Y)	31	CXY7	CXY6	CXY5	CXY4	CXY3	CXY2	CXY1	CXY0	
Horizontal weighting control (select UV)	32	CXUV7	CXUV6	CXUV5	CXUV4	CXUV3	CXUV2	CXUV1	CXUV0	
Prefilter YUV	33	PFUV3	PFUV2	PFUV1	PFUV0	PFY3	PFY2	PFY1	PFY0	
Vertical interpolation control	34	FLIP	YACM	YACL5	YACL4	YACL3	YACL2	YACL1	YACL0	
Vertical weighting control 1	35	CYA7	CYA6	CYA5	CYA4	CYA3	CYA2	CYA1	CYA0	
Vertical weighting control 2	36	CYB7	CYB6	CYB5	CYB4	CYB3	CYB2	CYB1	CYB0	
DC gain normalization	37	X	DCGX2	DCGX1	DCGX0	X	DCGY2	DCGY1	DCGY0	
Horizontal scaling increment	38	XSCI7	XSCI6	XSCI5	XSCI4	XSCI3	XSCI2	XSCI1	XSCI0	

FUNCTION SUBADDRESS		DATA BITS								
		D7	D6	D5	D4	D3	D2	D1	D0	DF[1]
(continue)	39	X	X	X	X	XSCI11	XSCI10	XSCI9	XSCI8	
Vertical scaling increment	3A	YSCI7	YSCI6	YSCI5	YSCI4	YSCI3	YSCI2	YSCI1	YSCI0	
(continue)	3B	X	X	X	X	X	X	YSCI9	YSCI8	
Chroma keying upper limit for V	3C	VU7	VU6	VU5	VU4	VU3	VU2	VU1	VU0	
Chroma keying lower limit for V	3D	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0	
Chroma keying upper limit for U	3E	UU7	UU6	UU5	UU4	UU3	UU2	UU1	UU0	
Chroma keying lower limit for U	3F	UL7	UL6	UL5	UL4	UL3	UL2	UL1	UL0	

Notes

1. Default register contents to be filled in by hand.
2. Continued in 0A.
3. Continued in 0E.
4. Bits set to logic 1 after reset (all other bits set to logic 0 after reset).
5. Continued in 2A.
6. Continued in 2E.

8.3 Description of the I²C-bus bits

Tables 15 to 21 give the function of the register bits given in Table 14.

8.3.1 Initial settings for the expansion and DMSD port; subaddress 00H

Table 15 Field detection; data bits FICO1 to FICO0

FICO1	FICO0	DESCRIPTION
0	0	field sequence as detected from H and V sync signals
0	1	field sequence synchronized to H and V but noise limited
1	0	free running field sequence
1	1	reserved

Table 16 Reference edge selection for the V sync input of the field detection; data bit REVFLD

REVFLD	DESCRIPTION
0	rising edge is reference
1	falling edge is reference

Table 17 Polarity selection for the H sync input of the field detection (note 1); data bit INVOE

INVOE	DESCRIPTION
0	active LOW, e.g. for SAA71xx signals similar to HREF
1	active HIGH, e.g. for SAA71xx signals similar to HS

Note

1. INVOE may also be used for FDIO and FLDV output signal inversion

Table 18 Polarity of I²C-bus register set ID; data bit IREGS

IREGS	DESCRIPTION
0	register set ID as defined by SREGS
1	register set ID inverted

Table 19 Fix I²C-bus register set ID; data bit SREGS

SREGS	DESCRIPTION
0	register set ID toggles as detected and defined by FICO0 and FICO1
1	register set ID fixed to 1 (register set B selected)

Table 20 Enable of reference signals PXQIO, HIO, VIO, FDIO, LLCIO (expansion port) and PXQV, HGTV, VSYV, FLDV (VRAM port); data bit RSEN

RSEN	DESCRIPTION
0	reference signals enabled
1	reference signals disabled

Table 21 Field sync definition; data bit FSEL

FSEL	DESCRIPTION
0	V input for field detection to be handled as V sync signal
1	V input for field detection to be handled as frame sync signal

8.3.2 INITIAL SETTINGS FOR THE VRAM PORT; SUBADDRESS 01H

Table 22 First pixel position in VRO data for FS1 = 0; FS0 = 0 (RGB) and FS1 = 0; FS0 = 1 (YUV); data bits LW1 and LW0

LW1	LW0	BITS 31 to 24	BITS 23 to 16	BITS 15 to 8	BITS 7 to 0	REMARK
0	0	pixel 0	pixel 0	pixel 1	pixel 1	FS2 = 0; TTR = 0
0	1	pixel 0	pixel 0	pixel 1	pixel 1	
1	0	black	black	pixel 0	pixel 0	
1	1	black	black	pixel 0	pixel 0	

Table 23 First pixel position in VRO data for FS1 = 1; FS0 = 1 (monochrome)

LW1	LW0	BITS 31 to 24	BITS 23 to 16	BITS 15 to 8	BITS 7 to 0	REMARK
0	0	pixel 0	pixel 1	pixel 2	pixel 3	FS2 = 0; TTR = 0
0	1	black	pixel 0	pixel 1	pixel 2	
1	0	black	black	pixel 0	pixel 1	
1	1	black	black	black	pixel 0	
0	0	pixel 0	pixel 1	X	X	FS2 = 1; TTR = 0; LW only affects the grey scale format
0	1	black	pixel 0	X	X	
1	0	pixel 0	pixel 1	X	X	
1	1	black	pixel 0	X	X	

Table 24 Set output field mode; data bits OF1 to OF0

OF1	OF0	DESCRIPTION
0	0	both fields for interlaced storage
0	1	both fields for non-interlaced storage
1	0	odd fields only (even fields ignored) for non-interlaced storage
1	1	even fields only (odd fields ignored) for non-interlaced storage

Table 25 Pixel qualifier polarity flag; data bit QPP

QPP	DESCRIPTION
0	PXQV is active LOW (pin 41)
1	PXQV is active HIGH

Table 26 VRAM-port output format; data bit VOF

VOF	DESCRIPTION
0	enabling of 32 to 16-bit multiplexing via VMUX
1	disabling of 32 to 16-bit multiplexing via VMUX

Table 27 VRAM-port mode selection; data bit TTR

TTR	DESCRIPTION
0	FIFO mode (VRAM data burst transfer)
1	transparent mode

Table 28 VRAM-port outputs enable; data bit VPE

VPE	DESCRIPTION
0	HFL and INCADR inactive (HFL = LOW, INCADR = HIGH); VRO outputs in 3-state
1	HFL and INCADR enabled; VRO outputs dependent on VOEN

8.3.3 PORT I/O CONTROL; SUBADDRESS 21H

Table 29 Select direction of PORT3 to PORT0; data bits PEN3 to PEN0

PEN3 TO PEN0	DESCRIPTION
PENx = 0	PORTx set to output
PENx = 1	PORTx set to input

Table 30 Status of port I/O's, pins 32 (PORT3) to 35 (PORT0)

PORT3 to PORT0	DESCRIPTION
Write mode	set status of PORT3 to PORT0 registers (applied to pins 32 to 35 if PENx = 0)
Read mode	read status of PORT3 to PORT0; if PENx = 0 then status of PORTx register; if PENx = 1 then status of external driven data

8.3.4 REGISTER SET A (02H TO 1FH) AND B (22H TO 3FH)

Table 31 Source select for expansion port clock output LLCIO (note 1); data bit LLCD

LLCD	DESCRIPTION
0	source is clock from DMSD port
1	source is clock input from expansion port, as defined by SRIO

Note

1. The clock output on LLCIO may be disabled by I^2C-bus bits SRIO = 1 and LLCS = 1; see Table 37.

Table 32 Source select for expansion port pixel qualifier and data output at PXQIO and VIDH/VIDL[7 to 0] (note 1); data bit PXQD

PXQD	DESCRIPTION
0	sources are corresponding signals from DMSD port
1	sources are corresponding signals from scaler output

Note

1. The qualifier output on PXQIO may be disabled by I^2C-bus bits SRIO = 1 and VIPSI = 1; see Table 38.

Table 33 Source select for expansion port horizontal sync output HIO (note 1); data bits HD1 to HD0

HD1	HD0	DESCRIPTION
0	0	source is corresponding signal from DMSD port
0	1	source is HIN from expansion port (short-cut)
1	0	source is corresponding signal from scaler output
1	1	source is HIN from expansion port

Note

1. If SRIO and HSI = 1 then HIO output is disabled.

Table 34 Source select for expansion port vertical sync output VIO (note 1); data bits VD1 to VD0

VD1	VD0	DESCRIPTION
0	0	source is corresponding signal from DMSD port
0	1	source is VIN from expansion port (short-cut)
1	0	source is corresponding signal from scaler output
1	1	source is VIN from expansion port

Note

1. If SRIO and VSI = 1 then VIO output is disabled.

Table 35 I/O control for the expansion port data output VIDH7 to VIDH0 and VIDL7 to VIDL0 (dependent on YUV8 programming for FLDC = 0) (note 1); data bit VIDC

YUV8	VIDC	DESCRIPTION
0	0	VIDH = output, VIDL = output
0	1	VIDH = input, VIDL = input
1	0	VIDH = output, VIDL = input
1	1	VIDH = input, VIDL = output

Note

1. If FLDC and FDIO) = 1 the outputs VIDH/VIDL are disabled.

Table 36 FDIO I/O control and signal definition; data bit FLDC

FLDC	FDIO	DESCRIPTION
0	–	FDIO contains odd/even flag FLD and is switched to output
1	–	FDIO may be provided with a 7196 DIR like signal and is switched to input
–	0	LLCIO, PXQIO and VIDH/VIDL I/O definition as defined by the I^2C-bus parameters
–	1	selected outputs are forced to input mode and corresponding signals are used as scaler input

Table 37 Source select for scaler clock input; data bit LLCS (03H to 23H)

FLDC	FDIO	SRIO	LLCS	DESCRIPTION
X	X	X	0	source is LLC from DMSD port
X	X	0	1	source is LLCIN from expansion port
0	X	1	1	source is LLCIO input from expansion port, output is disabled
1	0	1	1	source is derived from LLCIO output; LLCD = 0 from LLC of decoder port, LLCD = 1 not allowed
1	1	1	1	source is LLCIO input from expansion port, output is disabled

Table 38 Source select for scaler data and pixel qualifier input; data bit VIPSI

FLDC	FDIO	SRIO	VIPSI	DESCRIPTION
0	X	X	0	source is data and CREF from DMSD port
0	X	–	1	source is data input VIDH/VIDL: when the pixel qualifier is PXQIN from expansion port FLDC = 0, FDIO = x, SRIO = 0 and VIPSI = 1; when the pixel qualifier is PXQIO from expansion port, output disabled FLDC = 0, FDIO = x, SRIO = 1 and VIPSI = 1;
1	0	–	X	source is derived from data output VIDH/VIDL, from decoder port for PXQD = 0, PXQD = 1 is not allowed: when the pixel qualifier is PXQIN from expansion port FLDC = 1, FDIO = 0, SRIO = 0 and VIPSI = x; when the pixel qualifier is CREF via the PXQIO output for PXQD = 0, PXQD = 1 is not allowed FLDC = 1, FDIO = 0, SRIO = 1 and VIPSI = x
1	1	–	X	source is data input VIDH/VIDL, output disabled, when the pixel qualifier is PXQIN from expansion port FLDC = 1, FDIO = 1, SRIO = 0 and VIPSI = x; when the pixel qualifier is PXQIO from expansion, port output disabled FLDC = 1, FDIO = 1, SRIO = 1 and VIPSI = x

Table 39 Source select for scaler horizontal sync input; data bit HSI

SRIO	HSI	DESCRIPTION
X	0	source is HREF from DMSD port
0	1	source is HIN from expansion port
1	1	source is HIO from expansion port, HIO output disabled

Table 40 Source select for scaler vertical sync input and field detection H/V; data bit VSI

SRIO	VSI	DESCRIPTION
X	0	source is VS from DMSD port; VS and HREF for field detection
0	1	source is VIN from expansion port; VIN and HIN for field detection
1	1	source is VIO from expansion port; VIO and HIO for field detection

Table 41 Reference edge selection for the V sync input of the acquisition window; data bit REVAW

REVAW	DESCRIPTION
0	rising edge is reference
1	falling edge is reference

Table 42 Reference edge selection for the H-sync input of the acquisition window; data bit REHAW

REHAW	DESCRIPTION
0	rising edge is reference
1	falling edge is reference

Table 43 Expansion-port clock and reference signal selection; data bit SRIO (see Tables 37 to 40)

SRIO	DESCRIPTION
0	clock and reference signals are taken from xxxIN pins
1	clock and reference signals are taken from xxxIO pin, xxxIN pins are ignored

Table 44 VSYV output signal polarity; data bit VSYP

VSYP	DESCRIPTION
0	VSYV contains 1 active V sync signals
1	VSYV contains 0 active V sync signals

Table 45 VRAM port output format select; data bits FS2 to FS0 (04H to 24H); see Tables 6 and 7

FS2	FS1	FS0	OUTPUT FORMAT
0	0	0	RGB (5, 5, 5) + α; 2 × 16-bit/pixel; 32-bit word length; RGB matrix on, VRAM output format
0	0	1	YUV 4 : 2 : 2; 2 × 16-bit/pixel; 32-bit word length; RGB matrix off, VRAM output format
0	1	0	YUV 4 : 2 : 2; 1 × 16-bit/pixel; 16-bit word length; RGB matrix off, optional output format
0	1	1	monochrome mode; 4 × 8-bit/pixel; 32-bit word length; RGB matrix off, VRAM output format
1	0	0	RGB (5, 5, 5) + α; 1 × 16-bit/pixel; 16-bit word length; RGB matrix on, VRAM output + transparent format
1	0	1	YUV 4 : 2 : 2 + α; 1 × 16-bit/pixel; 16-bit word length; RGB matrix off; VRAM output + transparent format
1	1	0	RGB (8, 8, 8) + α; 1 × 24-bit/pixel; 24-bit word length; RGB matrix on, VRAM output + transparent format
1	1	1	monochrome mode; 2 × 8-bit/pixel; 16-bit word length; RGB matrix off, VRAM output + transparent format

Table 46 Dithering (noise shaping) control (for VRAM port only); data bit DIT

DIT	DESCRIPTION
0	dithering on
1	dithering off

Table 47 ROM table for anti-gamma correction (for VRAM port only); data bit RTB

RTB	DESCRIPTION
0	ROM table switched on
1	ROM table switched off

Table 48 Monochrome and two's complement output data select; data bit MCT

MCT	DESCRIPTION
0	inverse grey scale luminance (if grey scale is selected by FS bits) or straight binary U, V data output
1	non-inverse monochrome luminance (if grey scale is selected by FS bits) or two's complement U, V data output

Table 49 Expansion port data path configuration; data bit YUV8; see Tables 8 and 9

YUV8	DESCRIPTION
0	expansion port set to 16-bit YUV
1	expansion port set to 8-bit YUV (VIDL7 to VIDL0)

Table 50 Select field sequence, H and V; data bit SHVS

SHVS	DESCRIPTION
0	use separate H and V input signals
1	use decoded information from the CCIR 656 data stream (only for YUV8 = 1)

Table 51 Luminance brightness control; data bits BRIG7 to BRIG0 (05H to 25H)

D7	D6	D5	D4	D3	D2	D1	D0	GAIN
1	1	1	1	1	1	1	1	255 (bright)
...	...	...	...	...	...	...	...	....
1	0	0	0	0	0	0	0	128 (CCIR level)
...	...	...	...	...	...	...	...	....
0	0	0	0	0	0	0	0	0 (dark)

Table 52 Luminance contrast control; data bits CONT6 to CONT0 (06H to 26H)

D7	D6	D5	D4	D3	D2	D1	D0	GAIN
0	1	1	1	1	1	1	1	1.999 (maximum contrast)
...	...	...	...	...	...	...	...	....
0	1	0	0	0	0	0	0	1 (CCIR level)
...	...	...	...	...	...	...	...	....
0	0	0	0	0	0	0	0	0 (luminance off)

Table 53 Chrominance saturation control; data bits SATN6 to SATN0 (07H to 27H)

D7	D6	D5	D4	D3	D2	D1	D0	GAIN
0	1	1	1	1	1	1	1	1.999 (maximum contrast)
...	...	...	...	...	...	...	...	....
0	1	0	0	0	0	0	0	1 (CCIR level)
...	...	...	...	...	...	...	...	....
0	0	0	0	0	0	0	0	0 (colour off)

Table 54 X (horizontal) offset definition, counted in input pixel qualifiers; data bits XO10 to XO0

XO10 to XO0	DESCRIPTION
08H to 28H and 0AH to 2AH	Defines the start position of the X processing window

Table 55 X (horizontal) source size definition, counted in input pixel qualifiers; data bits XS10 to XS0

XS10 to XS0	DESCRIPTION
09H to 29H and 0AH to 2AH	defines the length of the X processing window

Table 56 Start phase for horizontal variable phase scaling (defined by XSCI11 to XSCI0); data bits XP6 to XP0

XP6 to XP0	DESCRIPTION
0BH to 2BH	$XP_{START} = XP/128 \times T_{PXQ}$ (T_{PXQ} = distance between 2 pixels)

Table 57 X phase value fixed; data bit XP7

XP7	DESCRIPTION
0	sample phase is calculated for every qualified sample
1	sample phase is fixed to the value set by XP6 to XP0

Table 58 Y (vertical) offset definition, counted in input horizontal sync events; YO10 to YO0

YO10 to YO0	DESCRIPTION
0CH to 2CH and 0EH to 2EH	defines the start position of the Y processing window

Table 59 Y (vertical) source size definition, counted in input horizontal sync events; YS10 to YS0

YS10 to YS0	DESCRIPTION
0DH to 2DH and 0EH to 2EH	defines the length of the Y processing window

Table 60 Start phase for vertical scaling (defined by YSCI9 to YSCI0); data bits YP6 to YP0

YP6 to YP0	DESCRIPTION
0FH to 2FH	$YP_{START} = YP/128 \times T_{LINE}$ (T_{LINE} = distance between 2 lines)

Table 61 Prescaling factor of the X prescaler; data bits XPSC5 to XPSC0

XPSC5 to XPSC0	DESCRIPTION
10H to 30H	defines accumulation sequence length and subsampling factor of the input data stream where N_{OP} (XPSC) = TRUNC [N_{IN} / (XPSC + 1)] N_{OP} = number of prescaler output pixel and N_{IN} = number of qualified scaler input pixel

Table 62 X (horizontal) prescaler accumulation mode of accumulating FIR; data bit XACM

XACM	DESCRIPTION
0	accumulating operates overlapping
1	non overlapping accumulation (must be set to bypass the prescaler)

Table 63 Coefficient select for X prescaler (luminance component Y); data bits CXY7 to CXY0

CXY7 to CXY0	DESCRIPTION
11H to 31H	for DC gain compensation of prescaler the accumulated pixels can be weighted by 1 or 2. CXYi defines a sequence of 8 bits, which control the coefficients; when CXYi = 0 pixel weighted by 1 and when CXYi = 1 pixel weighted by 2

Table 64 Coefficient select for X prescaler (colour difference signals UV); data bits CXUV7 to CXUV0

CXUV7 to CXUV0	DESCRIPTION
12H to 32H	for DC gain compensation of prescaler the accumulated pixels can be weighted by 1 or 2. CXUVi defines a sequence of 8 bits, which control the coefficients; when CXUVi = 0 pixel weighted by 1 and when CXUVi = 1 pixel weighted by 2

Table 65 Prefilter selection for luminance component Y (note 1); data bits PFY3 to PFY0 (13H to 33H)

PFY1	PFY0 ≥	H1(z)	H2(z)	H3(z)
0	0	bypass	bypass	bypass
0	1	active	bypass	bypass
1	0	active	bypass	active
1	1	active	active	active

Note

1. $H(z) = H1(z) \times H2(z) \times H3(z)$ with H1 and $H3 = 1 + z^{-1}$; $H2 = 1 + A \times z^{-1} + z^{-2}$ and A = 2, $^{15}/_{16}$, $^{7}/_{8}$, $^{3}/_{4}$ for PFY3 and PFY2 = 00, 01, 10, 11.

Table 66 Prefilter selection for colour difference signals UV (note 1); data bits PFUV3 to PFUV0

PFUV1	PFUV0 ≥	H1(z)	H2(z)	H3(z)
0	0	bypass	bypass	bypass
0	1	active	bypass	bypass
1	0	active	active	bypass
1	1	active	active	active

Note

1. $H(z) = H1(z) \times H2(z) \times H3(z)$ with $H1 = 1 + z^{-1}$; $H2 = 1 + A \times z^{-1} + z^{-2}$; $H3 = 1 + z^{-2}$ and A = 2, $^{15}/_{16}$, $^{7}/_{8}$, $^{3}/_{4}$ for PFUV3 and PFUV2 = 00, 01, 10, 11.

Table 67 Accumulation sequence length of the Y (vertical) processing; data bits YACL5 to YACL0

YACL5 to YACL0	DESCRIPTION
14H to 34H	defines vertical accumulation sequence length of input lines. If accumulation FIR filter mode is selected (YACM), YACL has to fit to the vertical scaling factor (defined by YSCI9 to YSCI0)

Table 68 Y (vertical) scaler accumulation (respectively calculation) mode of vertical arithmetic; data bit YACM

YACM	DESCRIPTION
0	arithmetic operates as a linear phase interpolator (LPI)
1	arithmetic operates as accumulating FIR filter in vertical direction

Table 69 Horizontal flip 'mirroring'; maximum pixels after prescaling = 384; data bit FLIP

FLIP	DESCRIPTION
0	output lines correspond to input lines
1	output lines correspond flipped input lines (see Section 7.4.2)

Table 70 Coefficient select for Y (vertical) processing in accumulation mode (notes 1 and 2); data bits CYA7 to CYA0 and CYB7 to CYB0 (15H to 35H and 16H to 36H)

CYBi	CYAi	CYi	WEIGHTING FACTOR
0	0	0	0
0	1	1	1
1	0	2	2
1	1	3	4

Notes

1. For improvement of vertical filtering the accumulated lines can be weighted. Weighting factor = $2^{(2 \times CYBi + CYAi - 1)}$
2. The resulting factor as a function of a bit pattern CYAi, CYBi and the DC gain control DCGY, is given in Tables 71 and 72.

Table 71 DC gain control of vertical scaler (see Table 2) (notes 1, 2 and 3) ; data bits DCGY2 to DCGY0 (17H to 37H)

DCGY2	DCGY1	DCGY0	DCGY	GAIN FACTOR
0	0	0	0	2
0	0	1	1	4
...	....	....	....	....
...	....	....	....	....
1	1	1	7	256

Notes

1. Dependent on active coefficients and the sequence length, the amplitude gain has to be renormalized.
2. Gain factor = $2^{(DCGY + 1)}$.
3. The resulting factor is a function of CYi and DCGY; 0 for (CYAi = CYBi = 0) or (CYAi = CYBi = 1 and DCGY = 0) or (DGCY > 5). The weighting/gain factor is given in Table 72.

Table 72 Weighting factor as a function of gain factor

CYI	DCGY0	DCGY1	DCGY2	DCGY3	DCGY4	DCGY5	DCGY6	DCGY7
0	0	0	0	0	0	0	0	0
1	$\frac{1}{2}$	$\frac{1}{4}$	$\frac{1}{8}$	$\frac{1}{16}$	$\frac{1}{32}$	$\frac{1}{64}$	0	0
2	1	$\frac{1}{2}$	$\frac{1}{4}$	$\frac{1}{8}$	$\frac{1}{16}$	$\frac{1}{32}$	0	0
3	0	1	$\frac{1}{2}$	$\frac{1}{4}$	$\frac{1}{8}$	$\frac{1}{16}$	0	0

Table 73 DC gain control of horizontal prescaler (see Table 1; note 1); data bits DCGX2 to DCGX0

DCGX2	DCGX1	DCGX0	GAIN
0	0	0	× 1
0	0	1	× 1/2
0	1	0	× 1/4
0	1	1	× 1/8
1	0	0	× 1/2
1	0	1	× 1/4
1	1	0	× 1/8
1	1	1	× 1/16

Note

1. Dependent on the number of active coefficients '2' in the accumulation sequence and the sequence length, the output amplitude gain has to be renormalization via DCGX.

Table 74 X scaler increment for variable phase scaling in horizontal pixel phase arithmetic (note 1); data bits XSCI11 to XSCI0 (18H to 38H and 19H to 39H)

XSCI11 TO XSCI0	DESCRIPTION
18H to 38H and 19H to 39H	$XSCI = INT\left[\frac{N_{IP}}{N_{OP}} \times \frac{1024}{(XPSC+1)}\right]$

Note

1. Where N_{IP} = number of qualified scaler input pixel and N_{OP} = number of output pixel.

Table 75 Y scaler increment for vertical down scaling; data bits YSCI9 to YSCI0 (1Ah to 3Ah and 1BH to 3BH)

YSCI9 TO YSCI0	DESCRIPTION
1AH to 3AH	$YSCI = INT\left[1024 \times \left(\frac{N_{IL}}{N_{OL}} - 1\right)\right]$; for YACM = 0 = LPI mode
1BH to 3BH	$YSCI = INT\left[1024 \times \left(1 - \frac{N_{OL}}{N_{IL}}\right)\right]$; for YACM = 1 = accumulation mode

Table 76 Set upper limit V for colour keying (8-bit; two's complement); data bits VU7 to VU0 (1CH to 3CH)

VU7	VU6	VU5	VU4	VU3	VU2	VU1	VU0	DESCRIPTION
1	0	0	0	0	0	0	0	as maximum negative value = −128 signal level
0	0	0	0	0	0	0	0	limit = 0
0	1	1	1	1	1	1	1	as maximum positive value = +127 signal level

Table 77 Set lower limit V for colour keying (8-bit; two's complement); data bits VL7 to VL0 (1DH to 3DH)

VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0	DESCRIPTION
1	0	0	0	0	0	0	0	as maximum negative value = −128 signal level
0	0	0	0	0	0	0	0	limit = 0
0	1	1	1	1	1	1	1	as maximum positive value = +127 signal level

Table 78 Set upper limit U for colour keying (8-bit; two's complement); data bits UU7 to UU0 (1EH to 3EH)

UU7	UU6	UU5	UU4	UU3	UU2	UU1	UU0	DESCRIPTION
1	0	0	0	0	0	0	0	as maximum negative value = −128 signal level
0	0	0	0	0	0	0	0	limit = 0
0	1	1	1	1	1	1	1	as maximum positive value = +127 signal level

Table 79 Set lower limit U for colour keying (8-bit; two's complement); data bits UL7 to UL0 (1FH to 3FH)

UL7	UL6	UL5	UL4	UL3	UL2	UL1	UL0	DESCRIPTION
1	0	0	0	0	0	0	0	as maximum negative value = −128 signal level
0	0	0	0	0	0	0	0	limit = 0
0	1	1	1	1	1	1	1	as maximum positive value = +127 signal level

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DDD(bord)}$	digital supply voltage for I/O section	SAA7140A	−0.5	+6.5	V
$V_{DDD(core)}$	digital supply voltage for internal core	SAA7140A	−0.5	+6.0	V
V_{DDD}	digital supply voltage	SAA7140B	−0.5	+6.0	V
V_I	DC input voltage	SAA7140B	−0.5	V_{DDD} + 0.5	V
V_O	DC output voltage	SAA7140B	−0.5	V_{DDD} + 0.5	V
P_{tot}	total power dissipation	SAA7140A	−	750	mW
		SAA7140B	−	750	mW
T_{stg}	storage temperature		−65	+150	°C
T_{amb}	operating ambient temperature		0	70	°C
V_{esd}	electrostatic protection		2000[1]	−	V

Note

1. Pin 31 (SDA): 800 V.

10 HANDLING

Inputs and output are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

11 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	60	K/W

12 DC CHARACTERISTICS

$V_{DDD(bord)}$ = 4.5 to 5.5 V; $V_{DDD(core)}$ = 3.0 to 3.6 V; V_{DDD} = 3.0 to 3.6 V; T_{amb} = 0 to 70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies; SAA7140A						
$V_{DDD(bord)}$	digital supply voltage for I/O section		4.5	5.0	5.5	V
$V_{DDD(core)}$	digital supply voltage for internal core		3.0	3.3	3.6	V
$I_{DDD(bord)}$	digital supply current for I/O section	normal operation	–	30	–	mA
		sleep mode	–	10	–	mA
$I_{DDD(core)}$	digital supply current for internal core	normal operation	–	60	–	mA
		sleep mode	–	10	–	mA
$I_{DDD(tot)}$	total digital supply current		–	100	–	mA
Supplies; SAA7140B						
V_{DDD}	digital supply voltage		3.0	3.3	3.6	V
I_{DDD}	digital supply current	normal operation	–	90	–	mA
		sleep mode	–	10	–	mA
Data, clock and control inputs						
V_{IL}	LOW level input voltage	clocks	−0.5	–	0.6	V
V_{IH}	HIGH level input voltage	clocks	2.4	–	V_{DDD} + 0.5	V
V_{IL}	LOW level input voltage	other inputs; SAA7140A	−0.5	–	0.8	V
		other inputs; SAA7140B	−0.5	–	$0.2V_{DDD}$	V
V_{IH}	HIGH level input voltage	other inputs; SAA7140A	2.0	–	V_{DDD} + 0.5	V
		other inputs; SAA7140B	2.4	–	V_{DDD} + 0.5	V
I_{LI}	input leakage current	V_{IL} = 0 V	–	–	1	mA
C_I	input capacitance	data	–	–	8	pF
		clocks	–	–	8	pF
		3-state I/O; high-impedance state	–	–	8	pF
Data, clock and control outputs (note 1)						
V_{OL}	LOW level output voltage	all outputs; SAA7140A	0	–	0.6	V
		clocks; SAA7140B	0	–	0.4	V
V_{OH}	HIGH level output voltage	clocks; SAA7140A	2.6	–	V_{DDD}	V
		clocks; SAA7140B	$0.85V_{DDD}$	–	V_{DDD}	V
V_{OH}	HIGH level output voltage	other outputs; SAA7140A	2.4	–	V_{DDD}	V
		other outputs; SAA7140B	$0.85V_{DDD}$	–	V_{DDD}	V
V_{OL}	LOW level output voltage	other outputs; SAA7140B	0	–	0.4	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I²C-bus, SDA and SCL (pins 31 and 32)						
V_{IL}	LOW level input voltage					
	SAA7140A		−0.5	–	+1.5	V
	SAA7140B		−0.5	–	$0.3V_{DDD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DDD}$	–	V_{DDD} + 0.5	V
$I_{31, 32}$	input current		–	–	±10	μA
I_{ACK}	output current on pin 31	acknowledge	3	–	–	mA
V_o	output voltage at acknowledge	I_{31} = 3 mA	–	–	0.4	V

Note

1. Levels measured with load circuit; 1.2 kΩ at 3 V (TTL load); C_L = 40 pF.

13 AC CHARACTERISTICS

$V_{DDD(bord)}$ = 4.5 to 5.5 V; $V_{DDD(core)}$ = 3.0 to 3.6 V; V_{DDD} = 3.0 to 3.6 V; T_{amb} = 0 to 70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Clock input timing (LLC, LLCIN and LLCIO as input) (see Fig.20)						
t_{LLC}, t_{LLCIN}	cycle time		31	–	45	ns
δ	duty factor	t_{LLCH} or t_{LLC}	40	50	60	%
t_r	rise time		–	–	5	ns
t_f	fall time		–	–	6	ns
VCLK input timing (for 'Burst Mode' only, TTR = 0); note 1 (see Fig.19)						
t_{VCLK}	VRAM port clock cycle time	note 2	30	–	200	ns
t_{pL}	VCLK LOW time	note 3	12	–	–	ns
t_{pH}	VCLK HIGH time	note 3	12	–	–	ns
t_r	rise time	0.6 V to $0.85V_{DDD}$	–	–	5	ns
t_f	fall time	$0.85V_{DDD}$ to 0.6 V	–	–	6	ns
Data and control input timing, related to the corresponding input clock; (see Fig.20)						
t_{SU}	set-up time		11	–	–	ns
t_{HD}	hold time		3	–	–	ns
Data and control input timing at the expansion port, related to LLCIO output						
t_{SU}	set-up time		15	–	–	ns
t_{HD}	hold time		0	–	–	ns
Clock output timing (LLCIO and VCLK output); note 4 (see Fig.20)						
C_L	output load capacitance		15	–	40	pF
t_{LLCIO}	cycle time		31	–	45	ns
δ	duty factor	t_{LLCIOH} or t_{LLCIO}	38	49	59	%
t_r	rise time	0.6 V to $0.85V_{DDD}$	–	–	5	ns
t_f	fall time	$0.85V_{DDD}$ to 0.6 V	–	–	6	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data and control output timing at the expansion port, related to LLCIO output; (see Fig.20)						
C_L	load capacitance		15	–	40	pF
t_{OHD}	output hold time	C_L = 7.5 pF	1.5	–	–	ns
		C_L = 15 pF	–	–	–	ns
t_{PD}	propagation delay from positive edge of LLCIO output	C_L = 40 pF	–	–	15	ns
VRO and reference signal output timing, related to VCLK output; (see Fig.19)						
C_L	output load capacitance	VRO outputs	15	–	40	pF
		other outputs	7.5	–	25	pF
t_{OHD}	VRO data hold time	C_L = 10 pF; note 5	0	–	–	ns
t_{OHL}	related to LCC scaler (INCADR, HFL)	C_L = 10 pF; notes 6 and 1	0	–	–	ns
t_{OHV}	related to VCLK (HFL)	C_L = 10 pF; note 6	0	–	–	ns
t_{OD}	VRO data delay time in burst mode (TTR = 0)	C_L = 40 pF; note 5	–	–	25	ns
	VRO data delay time in transparent mode (TTR = 1)	C_L = 40 pF; note 5	–	–	15	ns
t_{ODL}	related to LCC_{Scaler} (INCADR,HFL)	C_L = 25 pF; notes 6 and 7	–	–	60	ns
t_{ODV}	related to VCLK (HFL)	C_L = 25 pF; note 6	–	–	60	ns
t_D	VRO disable time to 3-state	C_L = 40 pF; note 7	–	–	40	ns
		C_L = 25 pF; note 8	–	–	24	ns
t_E	VRO enable time from 3-state	C_L = 40 pF; note 7	–	–	40	ns
		C_L = 25 pF; note 8	–	–	25	ns
$t_{HFL\ VOE}$	HFL rising edge to VRAM port enable	no zooming	–	–	810	ns
$t_{HFL\ VCLK}$	HFL rising edge to VCLK burst	no zooming	–	–	840	ns

Notes

1. LLC_{Scaler} may be LLC from DMSD port or LLCIN from expansion-port, dependent on scaler source clock selection via I²C-bus bit LLCS.
2. Maximum T_{VCLK} = 200 ns for test mode only. The applicable maximum cycle time depends on data format, horizontal scaling and input data rate.
3. Measured at 1.5 V level; t_{pL} may be infinite.
4. $LLCIO_{out}$ timing also valid for VCLKout in transparent mode; (see Fig.20).
5. Timings of VRO refer to the rising edge of VCLK.
6. The timing of INCADR and the rising edge of HFL always refers to LLC_{Scaler}. During a VRAM transfer, the falling edge of HFL is generated by VCLK. During horizontal increment and vertical reset cycles, both edges of HFL always refer to LLC scaler.
7. Asynchronous signals. Its timing refers to the 1.5 V switching point of VOEN input signal (pin 53).
8. The timing refers to the 1.5 V switching point of VMUX signal (pin 46) in 32 to 16-bit multiplexing mode. Corresponding pairs of VRO outputs are together connected.

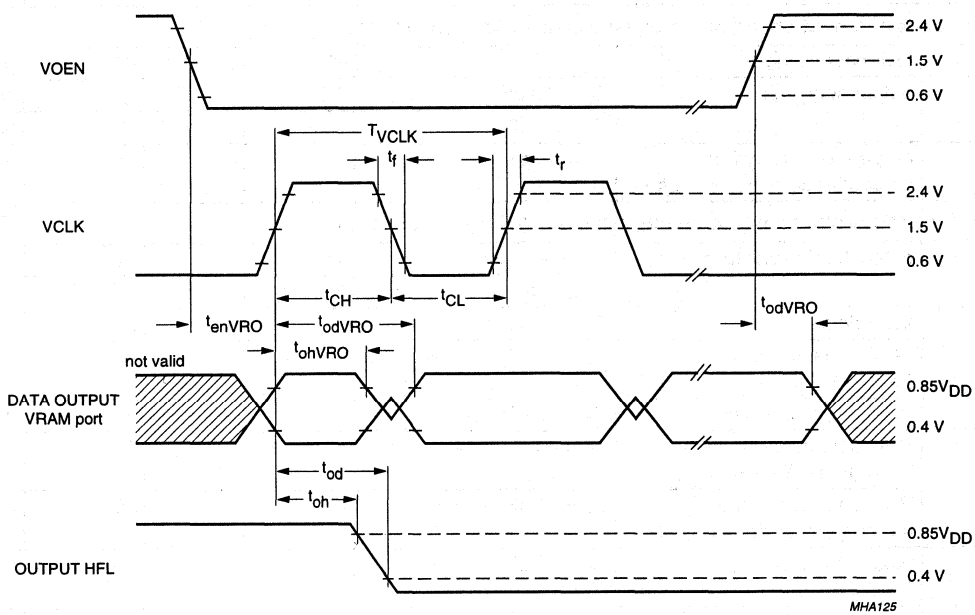


Fig.19 Data output timing (VRAM port).

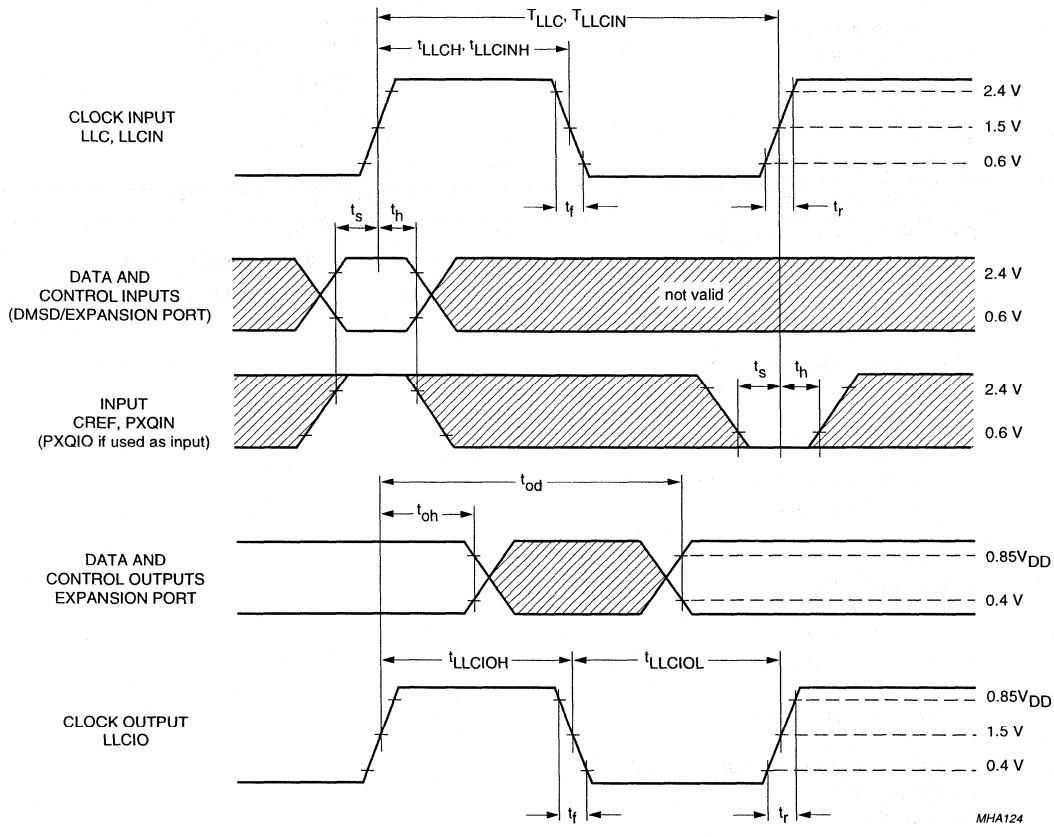


Fig.20 Data input/output timing (DMSD port and expansion port).

Multimedia bridge, high performance Scaler and PCI circuit (SPCI)

SAA7146

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Multimedia bridge, high performance Scaler and PCI circuit (SPCI)

SAA7146

1 FEATURES

1.1 Video processing

- Full size, full speed video delivery to and from the frame buffer or virtual system memory enables various processing possibilities for any external PCI device
- Full bandwidth PCI bus master write and read (up to 132 Mbytes/s)
- Virtual memory support (4 Mbytes per DMA channel)
- Processing of maximum 4095 active samples per line and maximum 4095 lines per frame
- Vanity picture (mirror) for video phone and video conferencing applications
- Video flip
- Colour space conversion with gamma correction for different kinds of displays
- Chroma Key generation and utilization
- Pixel dithering for low resolution video output formats
- Brightness, contrast and saturation control
- Video and Vertical Blanking Interval (VBI) synchronized programming of internal registers with Register Programming Sequencer (RPS), ability to control two asynchronous data streams simultaneously
- Memory Management Unit (MMU) supports virtual demand paging memory management (Windows, Unix, etc.)
- Rectangular clipping of frame buffer areas minimizes PCI bus load
- Random shape mask clipping protects selectable areas of frame buffer
- 3 × 128 Dword video FIFO with overflow detection and 'graceful' recovery.

1.2 Audio processing

- Video synchronous audio capture, e.g. for sound cards
- Various synchronization modes to support different audio and DSP data formats
- Audio input level monitoring enables peak control via software
- Programmable bit clock generation for master and slave applications.

1.3 Scaling

- Scaling of video pictures down to randomly sized windows
- High Performance Scaler (HPS) offers two-dimensional, phase correct data processing for improved signal quality of scaled video data, especially for compression applications
- Horizontal up-scaling (zoom) supports e.g. CCIR to square pixel conversion
- Additional Binary Ratio Scaler (BRS) supports CIF and QCIF formats, especially for video phone and video conferencing.

1.4 Interfacing

- Dual D1 (8-bit, CCIR 656) video I/O interface
- DMSD2 compatible (16-bit YUV) video input interface
- Supports various packed (pixel dithering) and planar video output formats
- Data Expansion Bus Interface (DEBI) for interfacing with MPEG- or JPEG decoders (ISA, 68000, Intel and Motorola format), capability for immediate and block mode (DMA) transfers
- 1 to 5 digital audio I/O ports
- Time Slot List (TSL) processing for flexible control of 2 asynchronous bidirectional digital audio interfaces simultaneously (4 DMA channels)
- 4 independent user configurable General Purpose I/O Ports (GPIO) for interrupt processing
- PCI interface (release 2.1)
- I^2C-bus interface (bus master).

1.5 General

- Subsystem (board) vendor ID support for board identification via software driver
- Internal arbitration control
- Diagnostic support and event analysis
- Programmable Vertical Blanking Interval (VBI) data region for e.g. to support INTERCAST
- 3.3 V core enables reduced power consumption, 5 V I/Os for PCI signalling environment
- CMOS, C100, 0.5 µm process.

2 GENERAL DESCRIPTION

The SAA7146, Multimedia PCI-Bridge, is a highly integrated circuit for DeskTop Video applications. The device provides a number of interface ports that enable a wide selection of video and audio ICs to be connected to the PCI-bus thus supporting a number of video applications in a PC. One example of the application capabilities is shown in Fig.1. Figure 2 shows the various interface ports and the main internal function blocks.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage I/O section	4.75	5.0	5.25	V
V_{DD3}	supply voltage core section	3.0	3.3	3.6	V
$I_{DD3V(tot)}$	3 V total supply current	–	400	–	mA
$I_{DD5V(tot)}$	5 V total supply current	–	60	–	mA
V_i; V_o	data input/output levels	TTL compatible			
f_{LLC}	LLC input clock frequency	–	–	32	MHz
f_{PCI}	PCI input clock frequency	–	–	33	MHz
f_{I^2S}	I^2S input clock frequency	–	–	12.5	MHz
T_{amb}	operating ambient temperature	0	–	70	°C

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7146H	SQFP208	plastic shrink quad flat package; 208 leads (lead length 1.95 mm); body 28 × 28 × 3.4 mm	SOT316-1

5 APPLICATION DIAGRAM

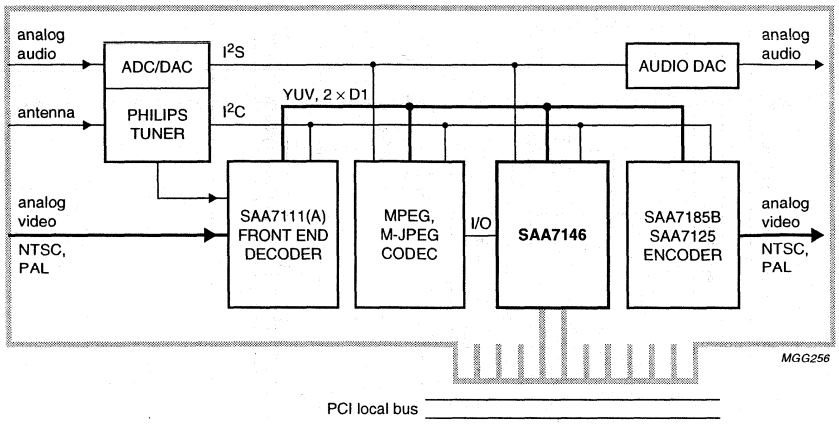


Fig.1 Application diagram.

6 BLOCK DIAGRAM

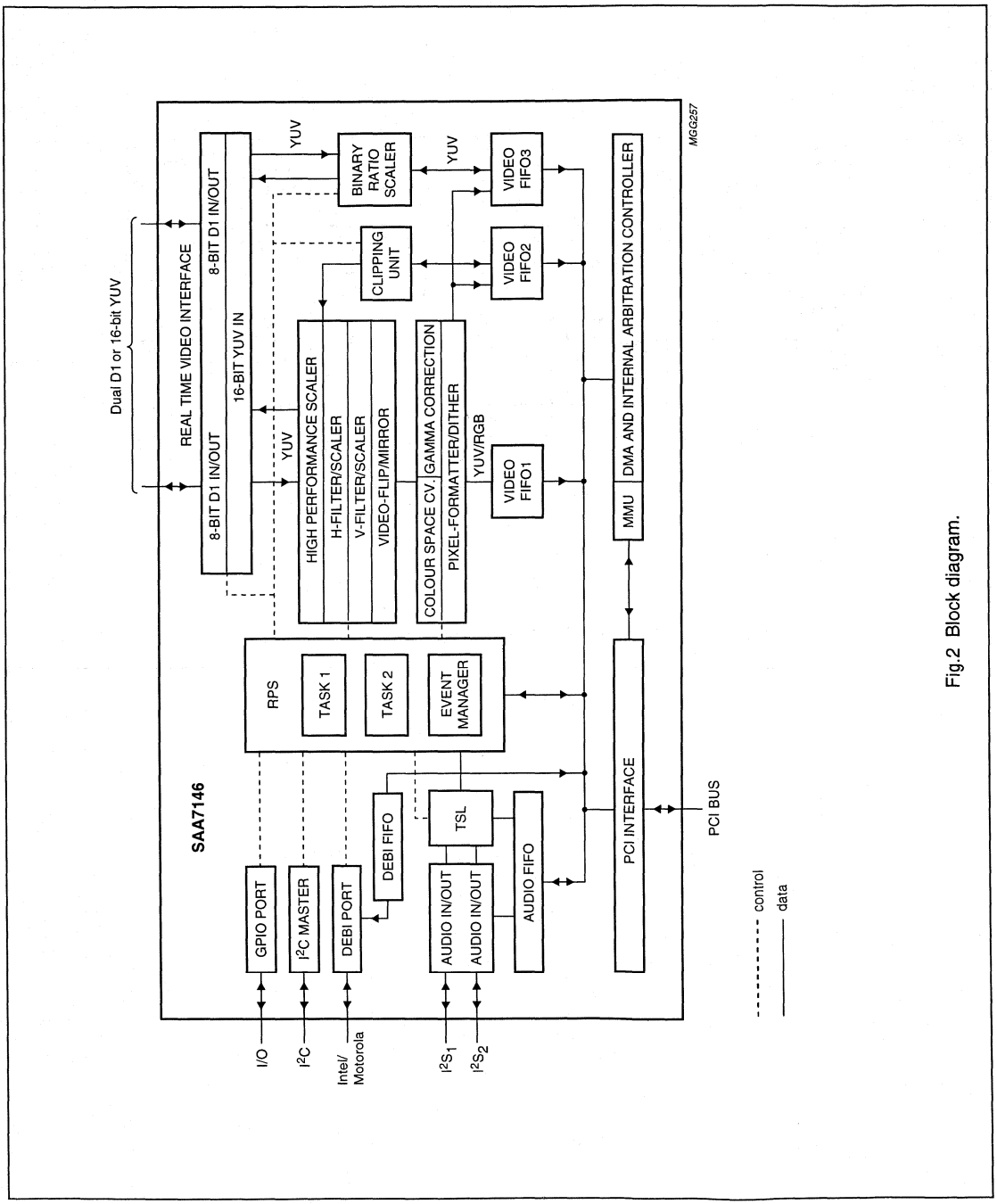


Fig.2 Block diagram.

7 PINNING

SYMBOL	PIN	STATUS	DESCRIPTION
V_{SS}	1	P	ground
D1_A0	2	I/O	digital CCIR 656 D1 port A (bit 0)
D1_A1	3	I/O	digital CCIR 656 D1 port A (bit 1)
D1_A2	4	I/O	digital CCIR 656 D1 port A (bit 2)
D1_A3	5	I/O	digital CCIR 656 D1 port A (bit 3)
V_{DD3}	6	P	+3.3 V core supply voltage; note 1
V_{DD}	7	P	+5 V I/O supply voltage; note 1
V_{SS}	8	P	ground
D1_A4	9	I/O	digital CCIR 656 D1 port A (bit 4)
D1_A5	10	I/O	digital CCIR 656 D1 port A (bit 5)
D1_A6	11	I/O	digital CCIR 656 D1 port A (bit 6)
D1_A7	12	I/O	digital CCIR 656 D1 port A (bit 7)
V_{DD3}	13	P	+3.3 V core supply voltage; note 1
V_{DD}	14	P	+5 V I/O supply voltage; note 1
V_{SS}	15	P	ground
VS_A	16	I/O	bidirectional vertical sync signal port A
HS_A	17	I/O	bidirectional horizontal sync signal port A
LLC_A	18	I/O	bidirectional line-locked system clock port A
PXQ_A	19	I/O	bidirectional pixel qualifier signal to mark valid pixels port A; note 2
n.c.	20	I/O	reserved pin; do not connect
V_{DD3}	21	P	+3.3 V core supply voltage; note 1
V_{DD}	22	P	+5 V I/O supply voltage; note 1
V_{SS}	23	P	ground
TRST#	24	I	test reset, JTAG pin must be set LOW for normal operation
TMS	25	I	test mode select, JTAG pin must be floating or set to HIGH during normal operation
TCLK	26	I	test clock, JTAG pin should be set LOW during normal operation
TDO	27	O	test data out, JTAG pin not active during normal operation
TDI	28	I	test data in, JTAG pin must be floating or set to HIGH during normal operation
V_{DD3}	29	P	+3.3 V core supply voltage; note 1
V_{DD}	30	P	+5 V I/O supply voltage; note 1
V_{SS}	31	P	ground
INTA#	32	O	PCI interrupt line
RST#	33	I	PCI global reset
CLK	34	I	PCI clock
GNT#	35	I	bus grant input signal, PCI arbitration signal
REQ#	36	O	bus request output signal, PCI arbitration signal

SYMBOL	PIN	STATUS	DESCRIPTION
V_{DD3}	37	P	+3.3 V core supply voltage; note 1
V_{DD}	38	P	+5 V I/O supply voltage; note 1
V_{SS}	39	P	ground
AD PCI31	40	I/O	PCI multiplexed address/data pin
AD PCI30	41	I/O	PCI multiplexed address/data pin
AD PCI29	42	I/O	PCI multiplexed address/data pin
AD PCI28	43	I/O	PCI multiplexed address/data pin
V_{DD3}	44	P	+3.3 V core supply voltage; note 1
V_{DD}	45	P	+5 V I/O supply voltage; note 1
V_{SS}	46	P	ground
AD PCI27	47	I/O	PCI multiplexed address/data pin
AD PCI26	48	I/O	PCI multiplexed address/data pin
AD PCI25	49	I/O	PCI multiplexed address/data pin
AD PCI24	50	I/O	PCI multiplexed address/data pin
V_{DD3}	51	P	+3.3 V core supply voltage; note 1
n.c.	52	I/O	reserved pin; do not connect
V_{DD}	53	P	+5 V I/O supply voltage; note 1
V_{SS}	54	P	ground
C/BE#[3]	55	I/O	PCI multiplexed bus command and Byte Enables
IDSEL	56	I	PCI initialization device select signal
AD PCI23	57	I/O	PCI multiplexed address/data pin
AD PCI22	58	I/O	PCI multiplexed address/data pin
AD PCI21	59	I/O	PCI multiplexed address/data pin
AD PCI20	60	I/O	PCI multiplexed address/data pin
n.c.	61	I/O	reserved pin; do not connect
V_{DD}	62	P	+5 V I/O supply voltage; note 1
V_{SS}	63	P	ground
AD PCI19	64	I/O	PCI multiplexed address/data pin
AD PCI18	65	I/O	PCI multiplexed address/data pin
AD PCI17	66	I/O	PCI multiplexed address/data pin
AD PCI16	67	I/O	PCI multiplexed address/data pin
V_{DD3}	68	P	+3.3 V core supply voltage; note 1
V_{DD}	69	P	+5 V I/O supply voltage; note 1
V_{SS}	70	P	ground
C/BE#[2]	71	I/O	PCI multiplexed bus command and Byte Enables
FRAME#	72	I/O	PCI cycle frame signal
IRDY#	73	I/O	PCI initiator ready signal
TRDY#	74	I/O	PCI target ready signal

SYMBOL	PIN	STATUS	DESCRIPTION
V_{DD3}	75	P	+3.3 V core supply voltage; note 1
V_{DD}	76	P	+5 V I/O supply voltage; note 1
V_{SS}	77	P	ground
DEVSEL#	78	I/O	PCI device select signal
STOP#	79	I/O	PCI stop signal
PERR#	80	O	PCI parity error signal
n.c.	81	O	reserved pin; do not connect
PAR	82	I/O	PCI parity signal
C/BE#[1]	83	I/O	PCI bus command/byte enables
V_{DD3}	84	P	+3.3 V core supply voltage; note 1
V_{DD}	85	P	+5 V I/O supply voltage; note 1
V_{SS}	86	P	ground
AD PCI15	87	I/O	PCI multiplexed address/data pin
AD PCI14	88	I/O	PCI multiplexed address/data pin
AD PCI13	89	I/O	PCI multiplexed address/data pin
AD PCI12	90	I/O	PCI multiplexed address/data pin
V_{DD3}	91	P	+3.3 V core supply voltage; note 1
V_{DD}	92	P	+5 V I/O supply voltage; note 1
V_{SS}	93	P	ground
AD PCI11	94	I/O	PCI multiplexed address/data pin
AD PCI10	95	I/O	PCI multiplexed address/data pin
AD PCI9	96	I/O	PCI multiplexed address/data pin
AD PCI8	97	I/O	PCI multiplexed address/data pin
n.c.	98	I/O	reserved pin; do not connect
V_{DD}	99	P	+5 V I/O supply voltage; note 1
V_{SS}	100	P	ground
C/BE#[0]	101	I/O	PCI multiplexed bus command and Byte Enables
AD PCI7	102	I/O	PCI multiplexed address/data pin
AD PCI6	103	I/O	PCI multiplexed address/data pin
V_{DD3}	104	P	+3.3 V core supply voltage; note 1
n.c.	105	I/O	reserved pin; do not connect
V_{DD}	106	P	+5 V I/O supply voltage; note 1
V_{SS}	107	P	ground
AD PCI5	108	I/O	PCI multiplexed address/data pin
AD PCI4	109	I/O	PCI multiplexed address/data pin
AD PCI3	110	I/O	PCI multiplexed address/data pin
AD PCI2	111	I/O	PCI multiplexed address/data pin

SYMBOL	PIN	STATUS	DESCRIPTION
V_{DD3}	112	P	+3.3 V core supply voltage; note 1
V_{DD}	113	P	+5 V I/O supply voltage; note 1
V_{SS}	114	P	ground
AD PCI1	115	I/O	PCI multiplexed address/data pin
AD PCI0	116	I/O	PCI multiplexed address/data pin
V_{DD3}	117	P	+3.3 V core supply voltage; note 1
V_{DD}	118	P	+5 V I/O supply voltage; note 1
V_{SS}	119	P	ground
AD15	120	I/O	DEBI multiplexed address data line
AD14	121	I/O	DEBI multiplexed address data line
AD13	122	I/O	DEBI multiplexed address data line
AD12	123	I/O	DEBI multiplexed address data line
V_{DD3}	124	P	+3.3 V core supply voltage; note 1
V_{DD}	125	P	+5 V I/O supply voltage; note 1
V_{SS}	126	P	ground
AD11	127	I/O	DEBI multiplexed address data line
AD10	128	I/O	DEBI multiplexed address data line
AD9	129	I/O	DEBI multiplexed address data line
AD8	130	I/O	DEBI multiplexed address data line
V_{DD3}	131	P	+3.3 V core supply voltage; note 1
V_{DD}	132	P	+5 V I/O supply voltage; note 1
V_{SS}	133	P	ground
RWN_SBHE	134	O	DEBI data transfer control signal (read write not/system byte high enable)
AS_ALE	135	O	DEBI address strobe and address latch enable
LDS_RDN	136	O	lower data strobe/read not
UDS_WRN	137	O	upper data strobe/write not
DTACK_RDY	138	I	DEBI data transfer acknowledge or ready
V_{DD3}	139	P	+3.3 V core supply voltage; note 1
V_{DD}	140	P	+5 V I/O supply voltage; note 1
V_{SS}	141	P	ground
AD0	142	I/O	DEBI multiplexed address data line
AD1	143	I/O	DEBI multiplexed address data line
AD2	144	I/O	DEBI multiplexed address data line
AD3	145	I/O	DEBI multiplexed address data line
V_{DD3}	146	P	+3.3 V core supply voltage; note 1
V_{DD}	147	P	+5 V I/O supply voltage; note 1
V_{SS}	148	P	ground

SYMBOL	PIN	STATUS	DESCRIPTION
AD4	149	I/O	DEBI multiplexed address data line
AD5	150	I/O	DEBI multiplexed address data line
AD6	151	I/O	DEMI multiplexed address data line
AD7	152	I/O	DEBI multiplexed address data line
n.c.	153	I/O	reserved pin; do not connect
n.c.	154	I/O	reserved pin; do not connect
V_{DD3}	155	P	+3.3 V core supply voltage; note 1
V_{DD}	156	P	+5 V I/O supply voltage; note 1
n.c.	157	I/O	reserved pin; do not connect
V_{SS}	158	P	ground
WS0	159	I/O	bidirectional word select signal for audio interface A1
SD0	160	I/O	bidirectional serial data for audio interface A1
BCLK1	161	I/O	bidirectional bit clock for audio interface A1
WS1	162	O	word select output signal for audio interface A1/A2
SD1	163	I/O	bidirectional serial data for audio interface A1/A2
WS2	164	O	word select output signal for audio interface A1/A2
SD2	165	I/O	bidirectional serial data for audio interface A1/A2
V_{DD3}	166	P	+3.3 V core supply voltage; note 1
V_{DD}	167	P	+5 V I/O supply voltage; note 1
V_{SS}	168	P	ground
WS3	169	O	word select output signal for audio interface A1/A2
SD3	170	I/O	bidirectional serial data for audio interface A1/A2
BCLK2	171	I/O	bidirectional bit clock for audio interface A2
WS4	172	I/O	bidirectional word select signal for audio interface A2
SD4	173	I/O	bidirectional serial data for audio interface A2
ACLK	174	I	audio reference clock input signal
SCL	175	I/O	I^2C-bus clock line
SDA	176	I/O	I^2C-bus data line
V_{DD3}	177	P	+3.3 V core supply voltage; note 1
V_{DD}	178	P	+5 V I/O supply voltage; note 1
V_{SS}	179	P	ground
GPIO3	180	I/O	general purpose I/O signal 3
GPIO2	181	I/O	general purpose I/O signal 2
GPIO1	182	I/O	general purpose I/O signal 1
GPIO0	183	I/O	general purpose I/O signal 0

SYMBOL	PIN	STATUS	DESCRIPTION
V_{DD3}	184	P	+3.3 V core supply voltage; note 1
V_{DD}	185	P	+5 V I/O supply voltage; note 1
V_{SS}	186	P	ground
D1_B0	187	I/O	digital CCIR 656 D1 port B (bit 0)
D1_B1	188	I/O	digital CCIR 656 D1 port B (bit 1)
D1_B2	189	I/O	digital CCIR 656 D1 port B (bit 2)
D1_B3	190	I/O	digital CCIR 656 D1 port B (bit 3)
V_{DD3}	191	P	+3.3 V core supply voltage; note 1
V_{DD}	192	P	+5 V I/O supply voltage; note 1
V_{SS}	193	P	ground
D1_B4	194	I/O	digital CCIR 656 D1 port B (bit 4)
D1_B5	195	I/O	digital CCIR 656 D1 port B (bit 5)
D1_B6	196	I/O	digital CCIR 656 D1 port B (bit 6)
D1_B7	197	I/O	digital CCIR 656 D1 port B (bit 7)
V_{DD3}	198	P	+3.3 V core supply voltage; note 1
V_{DD}	199	P	+5 V I/O supply voltage; note 1
V_{SS}	200	P	ground
LLC_B	201	I/O	bidirectional line-locked system clock port B
VS_B	202	I/O	bidirectional vertical sync signal port B
HS_B	203	I/O	bidirectional horizontal sync signal port B
PXQ_B	204	I/O	bidirectional pixel qualifier signal to mark valid pixels port B; note 3
n.c.	205	I/O	reserved pin; do not connect
V_{DD3}	206	P	+3.3 V core supply voltage; note 1
V_{DD}	207	P	+5 V I/O supply voltage; note 1
n.c.	208	I/O	reserved pin; do not connect

Notes

1. Operation of the SAA7146 requires two supply voltages, 3.3 V for the internal core and 5 V for the I/O pad section.
2. For continuous CCIR 656 format at the D1_A port this pin must be set HIGH.
3. For continuous CCIR 656 format at theD1_B port this pin must be set HIGH.

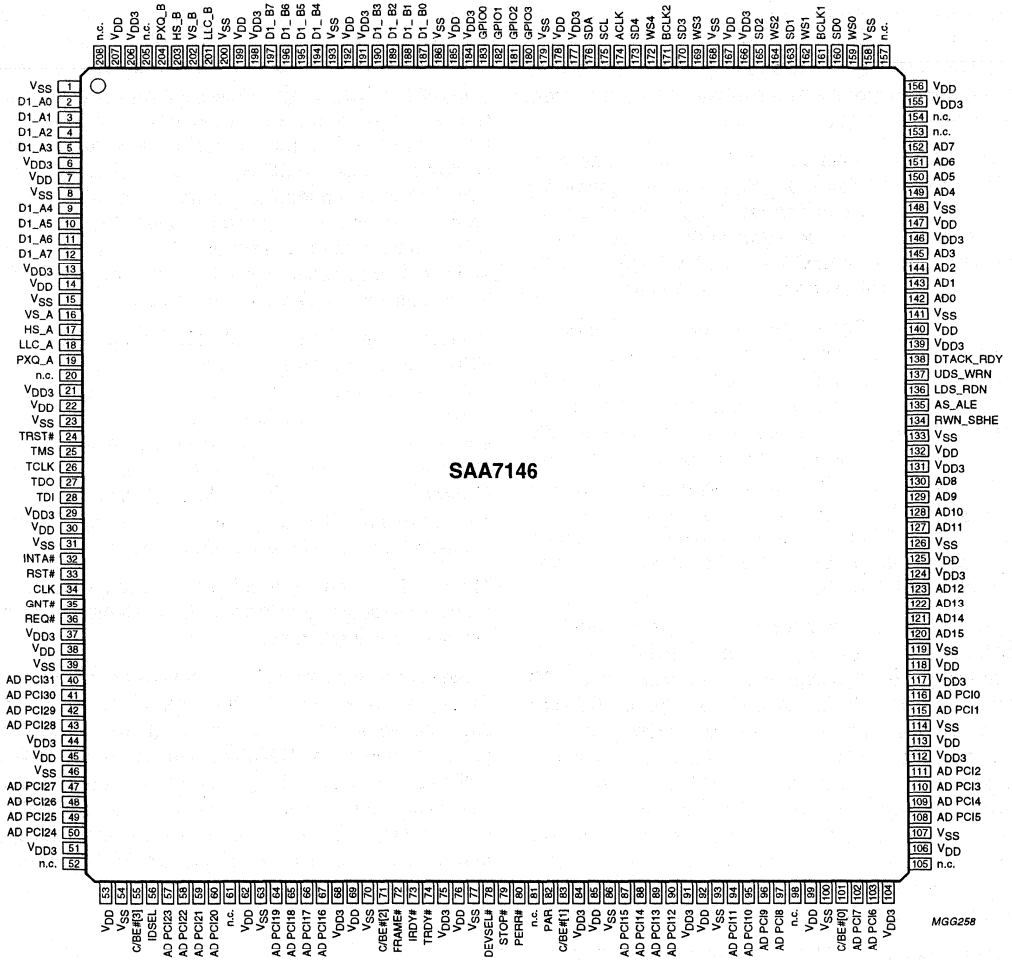


Fig.3 Pin configuration.

8 FUNCTIONAL DESCRIPTION

8.1 General

The Dual D1 (DD1) interface can be connected to digital Video Decoder ICs such as SAA7110/11, digital Video Encoder like SAA7185 video (de)-compression codec or to a D1 compatible connector, e.g. for an external digital camera. It supports bidirectional full duplex two channel full D1 (CCIR 656), optionally with separate sync wires H/V, pixel qualifier signal and double pixel clock I/O, up to 32 MHz. It also supports a 16-bit parallel 'YUV bus' used to interface the SAA7110.

The bidirectional digital audio serial interface is based on the I²S-bus standard also supporting flexible programming for various data and timing formats. Two independent interface circuits control audio data streaming of up to 8 stereo channels. Five devices like SAA7360/66 (ADC), and SAA7350/51 (DAC) can be connected directly.

The peripheral Data Port (Data Expansion Bus Interface DEBI) has parallel modes for system set-up and programming of peripheral multi-media devices (behind SAA7146), but is also capable and optimized to transport compressed MPEG/JPEG data to and from peripheral ICs to the PCI-system. DEBI supports ICs normally connected to the ISA bus, but has also a Motorola 68000 compatible mode of handshake signals. Besides the parallel port, there is also an I²C-bus port to control peripheral ICs such as single-chip decoders SAA7110/11 or encoders such as SAA7185/87, or audio ICs.

The PCI interface has master read and master write capability. The video signal flow to and from PCI is controlled by three video DMA channels, with a total FIFO capacity of 384 Dwords. The video DMA channel definition supports the typical video data structure (hierarchy) of pixels, lines, fields and frames. The audio signal flow is controlled by four audio DMA channels, each with 24 Dwords FIFO capacity. The DEBI is connected with to the PCI by single instruction direct access and via a data DMA channel for streaming data, with 32 Dwords FIFO capacity. To improve PCI efficiency, a local arbiter schedules the access to PCI for all local DMA channels.

The PCI interface of the SAA7146 supports virtual memory addressing for operating systems running virtual demand paging. The integrated Memory Management Unit (MMU) translates linear to physical addresses using a page table in system memory provided by the software driver. The MMU supports up to 4 Mbytes of virtual address space per DMA channel.

The main internal video processing function of the SAA7146 is its two-dimensional High Performance Scaler (HPS). Phase accurate re-sampling by interpolation supports independent horizontal up- and down scaling. In the horizontal direction the scaling processing is performed in two functional blocks: integer decimation by window averaging (n tap), and phase linear interpolation (10 tap filter for luminance, 6 tap filter for chrominance). The vertical processing for down scaling assumes the two algorithms: averaging over a window (n tap), or linear interpolation (2 tap). The scaling function can be used for random sized display windowing, or for horizontal upscaling (zoom), or for conversion between various sample schemes like CCIR or SQP. Incorporated in the HPS function is brightness, contrast and saturation control, and also colour key generation. The results of the HPS can be formatted in various RGB and YUV formats, and can be dithered for low bit rate formats. Packed formats as well as planar formats (YUV) are supported.

A second video channel (YUV 422 format) bypasses the HPS, and connects the real time video interface with the PCI interface through FIFO and DMA control. This video bypass channel, Binary Ratio Scaler (BRS), is bidirectional and has means to convert from full size video (50 or 60 Hz) to CIF, QCIF or QQCIF, and vice versa. (Binary ratio 1, 2, 4, 8, ½, ¼, ⅛ only). Multiple programmable VBI data and test signals regions can be bypassed without processing during each field.

The SAA7146 can perform functions such as video processing, audio handling and data extension bus. It has just one configuration space.

It can change it's programming sets using a Register Programming Sequencer (RPS) that works by itself on a user defined program controlled by internally supported real time events. The SAA7146 has two RPS machines to optimize flow control of e.g. an MPEG compressed data stream and real time video scaling control. The RPS programming is defined by an instruction list in the system main memory that consists of multiple RPS-Commands.

8.2 PCI Interface

This section describes the interface of the SAA7146 to the PCI bus. This includes the PCI modules, the DMA controls of the video, audio and data channels, the Memory Management Unit (MMU) and the Internal Arbitration Control (INTAC). The handling of the FIFOs and the corresponding errors are also described and a list of all DMA control registers given.

8.2.1 PCI MODULES AND CONFIGURATION SPACE

The SAA7146 provides a PCI bus interface having both slave and master capability. The master and the slave module fulfil the PCI local bus specification revision 2.1.

They decode the C_BE# lines to provide a byte-wise access and support 32-bit transfers up to a maximum clock rate of 33 MHz. To increase bus performance, they are able to handle fast back-to-back transfers.

During normal operation the SAA7146 checks for parity errors and reports them via the PERR# pin. If an address parity error is detected it will not respond.

Using the SAA7146 as a slave, access is obtained only to the programmable registers and the configuration space of it. Video, audio and other data the SAA7146 reads/writes autonomously via the master interface (see Fig.4). The use of the PCI master module, i.e. which DMA channel gets access to the PCI bus, is controlled by the INTAC; see Section 8.2.5).

The registers described in Table 1 are closely related to the PCI specification. It should be noted that Header type, Cache line size, BIST, Cardbus CIS pointer and expansion ROM Base Address Registers are not implemented. All registers, which are not implemented are treated as read only with a value of zero. Some values are loaded after PCI reset via I^2C-bus from EEPROM with device address 1010000 (binary). This loading will take approximately 1 ms. If any device tries to read or write data from or to the SAA7146 during the loading phase after reset, the SAA7146 will disconnect with retry.

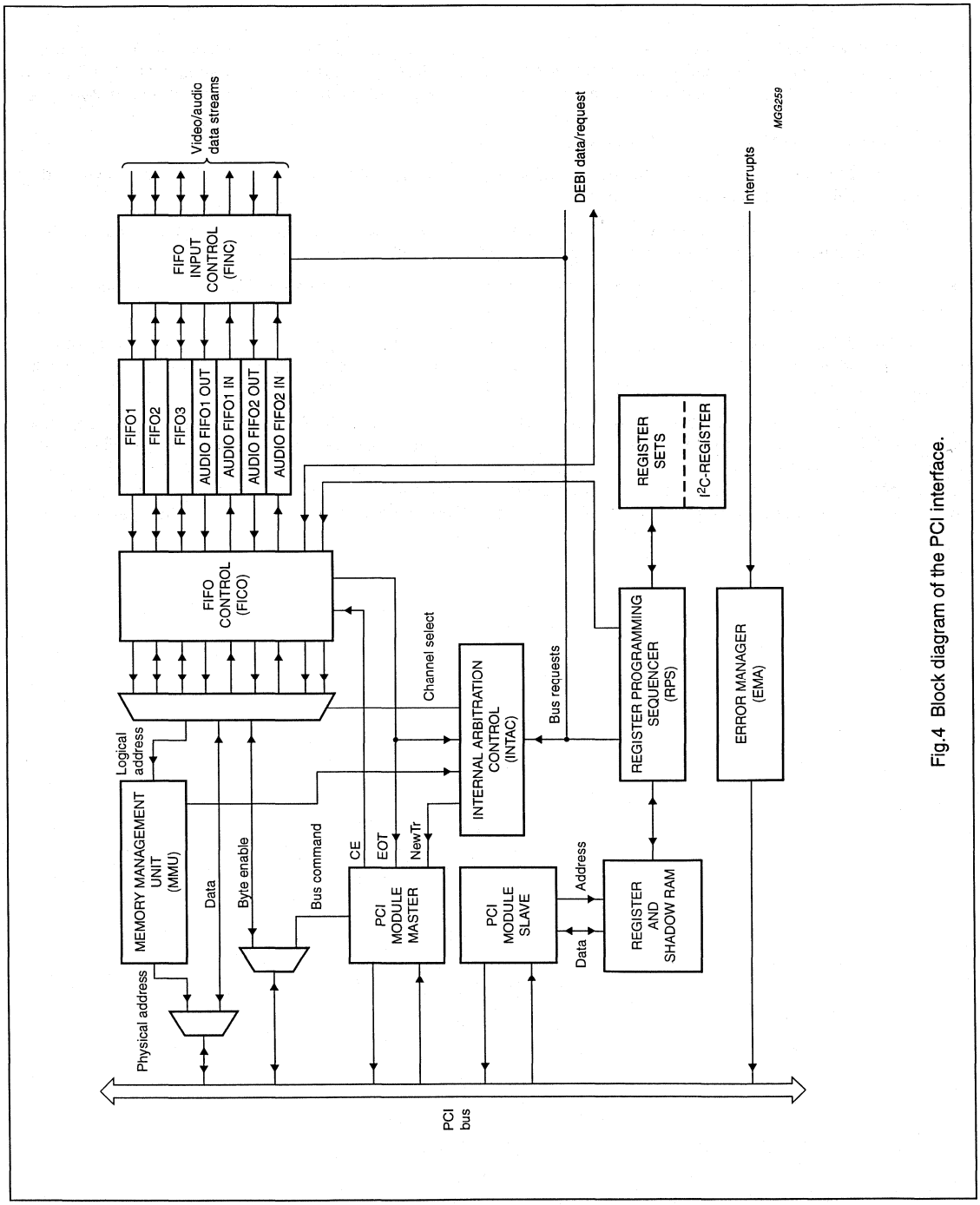


Fig.4 Block diagram of the PCI interface.

Table 1 Configuration Space Registers

ADDRESS (HEX)	NAME	BIT	TYPE	DESCRIPTION
00	Device ID	31 to 16	RO 7146H	SAA7146
	Vendor ID	15 to 0	RO 1131H	Philips
04	Status Register	31		Detected parity error
		29		Received master abort
		28		Received target abort
		26 and 25	RO 01	DEVSEL timing medium
		24		Data parity error detected
		23	RO 1	Fast back-to-back capable
	Command Register	9	RW	Fast back-to-back enable
		6	RW	Parity error response
		2	RW	Bus master enable
		1	RW	Memory space
08	Class Code	31 to 8	RO 048000H	Other multimedia device
	Revision ID	7 to 0	R	Reading these 8-bits returns 00H.
0C	Latency	15 to 8	RW	This register specifies, in units of PCI bus clocks, the value of the Latency Timer for this PCI bus master.
10	Base address Register	31 to 9	RW	This value must be added to the register offset to claim access to the programming registers. The lower 8 bits are forced to zero.
		8 to 0	RO	
2C	Subsystem ID	31 to 16	RO	This value will be loaded after PCI reset from external hardware using I^2C-bus. The default value is 0000H.
	Subsystem vendor ID	15 to 0	RO	This value will be loaded after PCI reset from external hardware using I^2C-bus. The default value is 0000H.
3C	Max_lat	31 to 24	RO	This value will be loaded after PCI reset from external hardware using I^2C-bus. The default value is 26H.
	Min_Gnt	23 to 16	RO	This value will be loaded after PCI reset from external hardware using I^2C-bus. The default value is 0FH.
	Interrupt Pin	15 to 8	R	The Interrupt Pin Register tells which interrupt pin the device uses. This device uses interrupt pin INTA#. When these bits are read they return 01H.
	Interrupt Line	7 to 0	RW	The Interrupt Line Register tells which input of the system interrupt controller the device's interrupt pin is connected to.

8.2.2 VIDEO DMA CONTROL

The SAA7146's DMA control is able to support up to three independent video targets or sources respectively. For this purpose it provides three video DMA channels. Each channel consists of a FIFO, a FIFO input control (FINC) placed on the scaler side of the FIFO, and a FIFO Control (FICO) placed on the PCI side of the FIFO. Channel 1 only supports the data stream direction into the PCI memory. It is not able to read data from system memory. However, this is possible using Channels 2 or 3. Table 2 surveys the possibilities and purposes of each video DMA channel.

Each FIFO, i.e. each DMA channel has its own programming set including base address (doubled for odd and even fields), pitch, protection address, page table base address, several handling mode control bits and a transfer enable bit (Tr_e).

In addition, each channel has a threshold and a burst length definition for internal arbitration (see Table 6, Section 8.2.5). To handle the reading modes FIFO2 and FIFO3 offer some additional registers: Number of Bytes per line (NumBytes), Number of Lines per field (NumLines) and the vertical scaling ratio (only FIFO3, see Table 66). The programming sets could be reloaded after previous job is done (EOW) to support several DMA targets per FIFO. The programming set currently used is loaded by the Register Programming Sequencer (RPS). If the RPS is not used, the registers could be rewritten each time, using the SAA7146 as a slave. But then the programmer must take care of the synchronization of these write accesses.

All registers needed for DMA control are described in Table 3, except the transfer enable bits, which are described in Table 10. The registers are accessed through PCI base address with appropriate offset.

Table 2 Size, direction and purpose of the video FIFOs and the associated DMA controls

FIFO	SIZE	DIRECTION	PURPOSE
FIFO 1	128 Dwords	Write to PCI	FIFO 1 buffers data from the HPS output and writes into PCI memory. In planar mode FIFO 1 gets the Y data.
FIFO 2	128 Dwords	RW	**Planar mode.** FIFO 2 buffers U data provided by the HPS. The associated DMA control 2 sends it into the PCI memory.
			Clip mode. DMA control 2 reads clipping information (clip bit mask or rectangular overlay data) from the PCI system memory and buffers it in FIFO 2.
FIFO 3	128 Dwords	RW	**Planar mode.** FIFO 3 buffers V data provided by the HPS and writes it into the PCI memory.
			Chroma keying mode. FIFO 3 buffers chroma keying information and writes it into PCI memory.
			BRS mode. FIFO 3 buffers data provided by the BRS. DMA control 3 sends it into the PCI memory.
			Read mode. DMA control 3 reads video data from the PCI system memory (the same data up to four times to offer a simple upscaling algorithm) and buffers it in FIFO 3.

Table 3 Video DMA Control Registers

OFFSET (HEX)	NAME	BIT	TYPE	DESCRIPTION
00	BaseOdd1	31 to 0	RW	PCI base address for odd fields of the upper (or lower if pitch is negative) left pixel of the transferred field.
04	BaseEven1	31 to 0	RW	PCI base address for even fields of the upper (or lower if pitch is negative) left pixel of the transferred field.
08	ProtAddr1	31 to 2	RW	Protection address
		1 and 0	R	Read only bits, a read operation returns '00'.
0C	Pitch1	31 to 0	RW	Distance between the start addresses of two consecutive lines of a single field.
10	Page1	31 to 12	RW	Base address of the page table (see Section 8.2.4).
	ME1	11	RW	Mapping enable. This bit enables the MMU.
		10 to 8		reserved
	Limit1	7 to 4	RW	Interrupt Limit. Defines the size of the memory range, that raise an interrupt, if its boundaries are passed.
	PV1	3	RW	Protection violation handling.
		2		reserved
	Swap1	1 and 0	RW	Endian swapping of all Dwords passing the FIFO: 00 = no swap 01 = two byte swap (3210 to 2301) 10 = four byte swap (3210 to 0123) 11 = reserved
14	NumLines1	27 to 16	RW	Number of lines per field. It defines the number of qualified lines to be processed by the HPS per field. This will cut off all the following input-lines at the HPS input.
	NumBytes1	11 to 0	RW	Number of pixels per line. It defines the number of qualified pixels to be processed by the HPS per line. This will cut off all the following pixels at the HPS input.
18	BaseOdd2	31 to 0	RW	PCI base address for odd fields of the upper (or lower if top-down flip is selected) left pixel of the transferred field.
1C	BaseEven2	31 to 0	RW	PCI base address for even fields of the upper (or lower if top-down flip is selected) left pixel of the transferred field.
20	ProtAddr2	31 to 2	RW	Protection address.
		1 and 0	R	Read only bits; a read operation returns '00'.
24	Pitch2	31 to 0	RW	Distance between the start addresses of two consecutive lines of a field.
28	Page2	31 to 12	RW	Base address of the page table (see Section 8.2.4).
	ME2	11	RW	Mapping enable. This bit enables the MMU.
		10 to 8		reserved
	Limit2	7 to 4	RW	Interrupt Limit. Defines the size of the memory range, that raise an interrupt, if its boundaries are passed.
	PV2	3	RW	Protection violation handling.

OFFSET (HEX)	NAME	BIT	TYPE	DESCRIPTION
28	RW2	2	RW	Specifies the data stream direction of FIFO 2. A logic 0 enables a write operation to the PCI memory. A logic 1 enables a read operation from the PCI memory.
	Swap2	1 and 0	RW	Endian swapping of all Dwords passing the FIFO: 00 = no swap 01 = two byte swap (3210 to 2301) 10 = four byte swap (3210 to 0123) 11 = reserved
2C	NumLines2	27 to 16	RW	Number of lines per field. In read mode NumLines defines the number of lines to be read from system memory. A logic 0 specifies one line. In write mode this register is not used.
	NumBytes2	11 to 0	RW	Number of bytes per line. In read mode this defines the number of bytes per line to be read from system memory. A logic 0 specifies one byte. In write mode this register is not used.
30	BaseOdd3	31 to 0	RW	PCI base address for odd fields of the upper (or lower if top-down flip is selected) left pixel of the transferred field.
34	BaseEven3	31 to 0	RW	PCI base address for even fields of the upper (or lower if top-down flip is selected) left pixel of the transferred field.
38	ProtAddr3	31 to 2	RW	Protection address.
		1 and 0	R	Read only bits; a read operation returns '00'.
3C	Pitch3	31 to 0	RW	Distance between the start addresses of two consecutive lines of a field.
40	Page3	31 to 12	RW	Base address of the page table (see Section 8.2.4).
	ME3	11	RW	Mapping enable. This bit enables the MMU.
		10 to 8		reserved
	Limit3	7 to 4	RW	Interrupt Limit. Defines the size of the memory range, that raise an interrupt, if its boundaries are passed.
	PV3	3	RW	Protection violation handling.
	RW3	2	RW	Specifies the data stream direction of FIFO 3. A logic 0 enables a write operation to the PCI memory. A logic 1 enables a read operation from the PCI memory.
	Swap3	1 and 0	RW	Endian swapping of all Dwords passing the FIFO: 00 = no swap 01 = two byte swap (3210 to 2301) 10 = four byte swap (3210 to 0123) 11 = reserved
44	NumLines3	27 to 16	RW	Number of lines per field. In read mode NumLines defines the number of lines to be read from system memory. A logic 0 specifies one line. In write mode it defines the number of qualified lines to be processed by the BRS per field. This will cut off all the following input-lines at the BRS input.
	NumBytes3	11 to 0	RW	Number of bytes per line. In read mode this defines the number of bytes per line to be read from system memory. A logic 0 specifies 1 byte. In write mode it defines the number of qualified bytes to be processed by the BRS per line. This will cut off all the following bytes at the BRS input.

The video sources provide 32 bits data and 4 bits byte enable, End Of Line (EOL), End Of Window (EOW), Begin Of Field (BOF), Line-Locked Clock (LLC), Odd/Even signal (OE) and a Valid Data (VD) signal. To start a transfer, e.g. with video DMA Channel 3, first this channel must be included in the internal arbitration scheme. This is achieved by setting the corresponding Tr_E bit (see Table 10). A FIFO is reset, if its Tr_E bit is not set.

In read mode, which is offered by Channels 2 and 3, the FICO requests a PCI transfer with the next BOF. Data is provided by the PCI master module. The FICO calculates the PCI address autonomously, starting with the base address of the corresponding field. Only the received data and byte enables will be filled into the FIFO. FIFO 3 offers the possibility to read video information from PCI memory, e.g. from the frame buffer. This could be done using the NumBytes and the NumLines Register, which defines the size of the source picture, so that the DMA control is able to synchronize itself to the source frame. FIFO 2 does the same if reading clip information from memory.

To support the Binary Ratio Scaler (BRS) included in the SAA7146, which only provides the possibility of horizontal upscaling, the DMA control 3 could do a line repetition by reading lines up to four times from PCI memory. This feature is controlled by the vertical scaling ratio in outbound mode (see Table 63). They specify the number of times each line should be read: 00 = only once, 01 = twice, and so on.

In the case of FIFO underflow, i.e. that the Binary Ratio Scaler or the clipping unit respectively tries to read data from the FIFO, even if the DMA control was not able to fill any data in until that moment, the reading unit tries to synchronize itself to the outgoing data stream as soon as possible. In this way the reading of unusable data is minimized. If the clipping unit receives no data, it will disable the associated pixels. The behaviour of the Binary Ratio Scaler depends on the selected read mode which is described in Section 8.10.

In the case of FIFO overflow, i.e. the scaler tries to transfer data although the FIFO is full, the FIFO input control locks the FIFO for the incoming data. While FIFO overflow the PCI address of the incoming data will be increased, overwriting itself each time. If the scaler transfers data, which has been clipped, the same mechanism is used to improve PCI performance.

Using the protection address system memory could be kept from prohibited write accesses. If the PCI pointer of the current transfer reaches or exceeds the protection address, the SAA7146 stops this transfer and an interrupt is set. No interrupt is set, if a protection violation occurs due to the programming done before the channel has been switched on. If the protection violation handling bit (PV) and the Limit Register are reset, the following data will be ignored until detection of the End of Window (EOW) signal. In read mode the DMA control also waits for this signal, to start the next transfer. If the PV bit is set, the input of the FIFO will be locked and the FIFO will be emptied. If the FIFO is empty the Tr_e bit is reset. This feature could be used for a single capture mode, if the protection address is the same address as the last pixel in this field. With that the SAA7146 will write one field into system memory and then stop. If the Limit Register has any other value than '0000' and the PV bit is zero, the DMA control continues writing data into system memory using the base address as new DMA address. The protection handling modes as selected by the PV bit and the contents of the Limit Register are shown in Table 4.

The SAA7146 is able to handle a negative pitch. With that, top-down-flip of the transmitted fields or frames is possible. A negative pitch (MSB = 1) leads to a different definition of the protection and the base address, as shown in Fig.5. If using negative pitch the first line starts at BaseAddr + pitch.

In 'none-RPS' mode the SAA7146 supports the displaying of interlaced video data by using the two different base addresses (BaseOdd, BaseEven) and vertical start phases (YPE6 to YPE0, YPO6 to YPO0) for odd and even fields.

If the Limit Register of any DMA channel (video, VBI data or audio) has a value other than '0000' the continuous write mode is chosen. If the actual PCI address hits the protection address and the PV bit is zero, the FINC stops the current transfer, sets an interrupt and resets the actual address to the base address. Consequently, the protection address could be used to define a memory space in which data is sent. The SAA7146 offers the possibility to monitor the filling grade of this memory space. The Limit Register defines an address limit, which generates an interrupt if passed by the actual PCI address pointer. '0001' means an interrupt will be generated if the lower 6 bits (64 bytes) of the PCI address are zero. '0010' defines a limit of 128 bytes, '0011' one of 256 bytes, and so on up to 1 Mbyte defined by '1111'. This interrupt range can be calculated as shown below.

Range = $2^{(5 + Limit)}$ bytes

Table 4 Protection violation handling modes

LIMIT	PV	DESCRIPTION
0000	0	Lock input of FIFO and empty FIFO (only in write mode). Unlock FIFO and start next transfer using the base address at the detection of EOW (End Of Window).
$\overline{0000}$	0	Restart immediately at base address.
XXXX[1]	1	Lock input of FIFO, empty FIFO and then reset Tr_e bit. The next transfer starts with Begin Of Field using the corresponding base address, if the Tr_e bit is set again. This setting is useful for single shot, that means transferring only one frame of a video stream. Therefore the protection address has to be the same as the address of the last pixel of the field.

Note

1. 'X' denotes don't care.

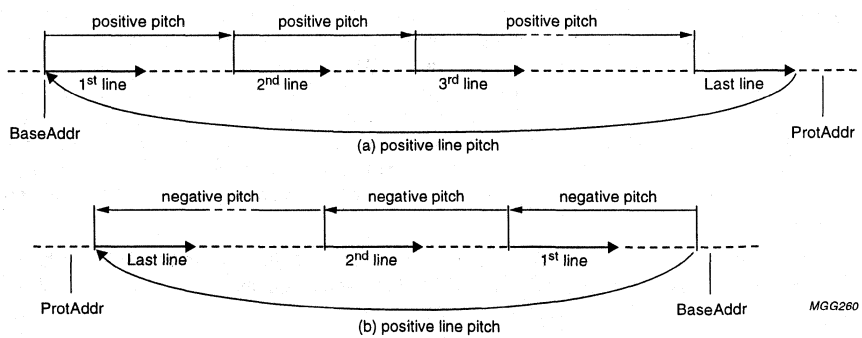


Fig.5 Handling of base and protection address using positive and negative line pitch.

8.2.3 AUDIO DMA CONTROL

The SAA7146 provides up to four audio DMA channels, each using a FIFO of 24 Dwords. Two channels are read only (A1_in and A2_in) and two channels are write only (A1_out and A2_out). Because audio presents a continuous data stream, which is not line or field dependent, the audio DMA control offers only one base address (BaseAxx) and no Pitch Register. For FIFO overflow and underflow the handling of these channels is the same as the video DMA channels (see Section 8.2.2).

The protection violation handling differs only if the Limit Register and the PV bit are programmed to zero. The audio DMA channel does not wait for the End of Field signal, like the video ones. It does not generate interrupts. The interrupt range specified by the Limit Register is defined in the same way as mentioned in Section 8.2.2. The audio DMA channels try immediately to transfer data after setting the transfer enable bits. All registers for audio DMA control, which are the base address, the protection address and the control bits are listed in Table 5, except the input control bits, which are listed in Table 6.

Table 5 Audio DMA Control Register

OFFSET (HEX)	NAME	BIT	TYPE	DESCRIPTION
94	BaseA1_in	31 to 0	RW	**Base address for audio input Channel 1.** This value specifies a byte address.
98	ProtA1_in	31 to 2	RW	**Protection address for audio input Channel 1.** This address could be used to specify a upper limit for audio access in memory space. Bits 0 and 1 are read only and return '00' when read.
		1 to 0	R	
9C	PageA1_in	31 to 12	RW	**Base address of the page table.** See Section 8.2.4.
	MEA1_in	11	RW	**Mapping enable.** This bit enables the MMU.
		10 to 8		reserved
	LimitA1_in	7 to 4	RW	**Interrupt Limit.** Defines the size of the memory range, that generates interrupt, if its boundaries are passed.
	PVA1_in	3	RW	**Protection violation handling.**
	–	2 to 0	–	reserved
A0	BaseA1_out	31 to 0	RW	**Base address for audio output Channel 1.** This value specifies a byte address. The lower two bits are forced to zero.
A4	ProtA1_out	31 to 2	RW	**Protection address for audio output Channel 1.** This address could be used to specify a upper limit for audio access in memory space. Bits 0 and 1 are read only and return '00' when read.
		1 and 0	R	
A8	PageA1_out	31 to 12	RW	**Base address of the page table.** See Section 8.2.4.
	MEA1_out	11	RW	**Mapping enable.** This bit enables the MMU.
	–	10 to 8	–	reserved
	LimitA1_out	7 to 4	RW	**Interrupt Limit.** Defines the size of the memory range, that generates an interrupt, if its boundaries are passed.
	PVA1_out	3	RW	**Protection violation handling.**
	–	2 to 0	–	reserved

OFFSET (HEX)	NAME	BIT	TYPE	DESCRIPTION
AC	BaseA2_in	31 to 0	RW	**Base address for audio input Channel 2.** This value specifies a byte address. The lower two bits are forced to zero.
B0	ProtA2_in	31 to 2	RW	**Protection address for audio input Channel 2.** This address could be used to specify a upper limit for audio access in memory space. Bits 0 and 1 are read only and return '00' when read.
		1 and 0	R	
B4	PageA2_in	31 to 12	RW	**Base address of the page table.** See Section 8.2.4.
	MEA2_in	11	RW	Mapping enable. This bit enables the MMU.
		10 to 8		reserved
	LimitA2_in	7 to 4	RW	**Interrupt Limit.** Defines the size of the memory range, that raise an interrupt, if its boundaries are passed.
	PVA2_in	3	RW	**Protection violation handling.**
	–	2 to 0	–	reserved
B8	BaseA2_out	31 to 0	RW	**Base address for audio output Channel 2.** This value specifies a byte address. The lower two bits are forced to zero.
BC	ProtA2_out	31 to 2	RW	**Protection address for audio output Channel 2.** This address could be used to specify a upper limit for audio access in memory space. Bits 0 and 1 are read only and return '00' when read.
		1 and 0	R	
C0	PageA2_out	31 to 12	RW	**Base address of the page table.** See Section 8.2.4.
	MEA2_out	11	RW	**Mapping enable.** This bit enables the MMU.
	–	10 to 8	–	reserved
	LimitA2_out	7 to 4	RW	**Interrupt Limit.** Defines the size of the memory range, that raise an interrupt, if its boundaries are passed.
	PVA2_out	3	RW	**Protection violation handling.**
	–	2 to 0	–	reserved

8.2.4 Memory Management Unit

8.2.4.1 Introduction

To perform DMA, physically continuous memory is needed. However, operating systems like Microsoft Windows are working with virtual demand paging, using a Memory Management Unit to translate linear to physical addresses. Memory allocation is done in the linear address space, resulting in fragmented memory in the physical address space. There is no way to allocate large buffers of physical, continuous memory, except reserving it during system start-up thus decreasing the system performance dramatically. To overcome this problem the SAA7146 contains a Memory Management Unit (MMU). This MMU can handle memory being fragmented to 4 kbyte pages, similar to the scheme used by the Intel 8086 processor family. The MMU can be bypassed to ease transfers to non-paged memory like the graphics adapter's frame buffer.

8.2.4.2 Memory allocation

The SAA7146s MMU requires a special scheme for memory allocation. The following steps need to be performed:

- Allocation of n pages, each page being 4 kbytes, aligned to a 4 kbyte boundary
- Allocation of one extra page, being used as page table
- Initialization of the page table.

Allocation of pages is done in physical address space. Operating systems implementing virtual memory provide services to allocate and free these pages.

The page table is stored in an extra page. This limits the linear address page to a size of 4 Mbytes and results in a 4 kbyte overhead. The page table is organized as an array of n Dwords, each entry giving the physical address of one of the n pages of allocated memory. As pages are aligned to 4 kbytes, the lower 12 bits of each entry are fixed to zero.

8.2.4.3 Implementation

The SAA7146 has up to 8 DMA channels (3 video, 4 audio and 1 DEBI channel) for which mapping is done. Each of them provides the linear address to/from which it wants to send/read data for the next transfer. Their register sets contain a page table base address (Pagexx) and a mapping enable bit (MExx). If MExx is set, mapping is enabled.

The MMU checks for each channel if its address has been already translated. If so, its request can pass to the Internal Arbitration Control (INTAC) managing the access to the PCI bus. If not, the MMU starts a bus transfer to the page table. The page table entry address could be calculated out of the channels PCI address and the page table base address, as shown in Fig.6. The upper 20-bits of the PCI address get replaced by the upper 20-bits of the according page address generating the mapped PCI address.

If the PCI address crosses a 4 kbyte boundary during a transfer, the MMU stops this transfer and suppresses its request to the INTAC until it has renewed the page address, which means replacing the upper 20-bits of the current address. To reduce latency the SAA7146 will do a prefetch, i.e. it will always try to have the next page address in advance.

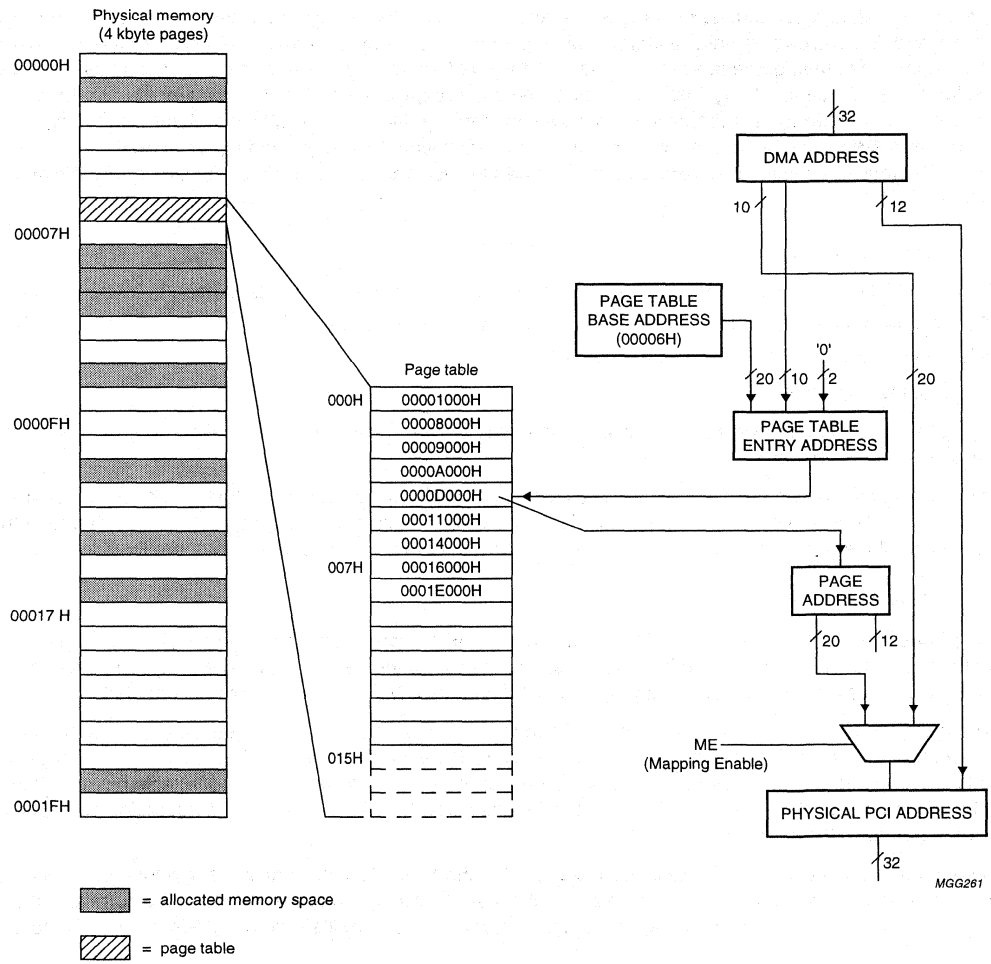


Fig.6 Memory Management Unit.

8.2.5 INTERNAL ARBITRATION CONTROL

The SAA7146 has up to three video DMA channels, four audio DMA channels and three other DMA channels, RPS, MMU and DEBI, each trying to get access to the PCI bus. To handle this, an Internal Arbitration Control (INTAC) is needed. INTAC controls the need for a PCI bus request and the order each DMA channel gets access to the bus.

The basic implementation of the internal arbitration control is a round-robin mechanism on the top, consisting of the RPS, the MMU and one of the eight data channels. Data channel arbitration is performed using a 'first come first serve' queue architecture, which may consist of up to eight entries.

Each data channel reaching a certain filling grade of its FIFO defined by the threshold, is allowed to make an entry into the arbitration queue. The threshold defines the number of Dwords needed to start a sensible PCI transfer and must be small enough to avoid a loss of data due to an overflow regarding the PCI latency time. After each job, End of Window (EOW) the video channels have to be emptied and are allowed to fill an entry into the queue, even if they have not yet reached their threshold.

Concurrent to the entry the channel sets a bit which prohibits further entries to this channel. In the worst case, each data channel can have only one entry in the queue.

If each channel wants to access the bus, which means the queue is full, an order like the one shown below will be given.

- MMU
- RPS.

First entry of the data channel queue:

- MMU
- RPS.

Second entry of the data channel queue:

- MMU
- . . . . and so on.

If INTAC detects at least one DMA channel in the queue or an MMU or RPS request, it signals the need for the bus setting the REQ# signal on the PCI bus. If the GNT# signal goes LOW, the SAA7146 is the owner of the bus and starts the PCI master module using the first channel selected. The master module tries to transfer the number of Dwords defined in the Burst Register. For RPS the burst length is hardwired to four and for the MMU it is hardwired to two Dwords. After that the master module stops this transfer and starts a transfer using the next channel.

If a DMA channel gets its transfer stopped due to a retry, the arbitration control sets the corresponding retry flag. INTAC tries to end a retried transfer, even if this transfer gets stopped via the Transfer Enable bit (Tr_E). For this reason the Transfer Enable bits are internally shadowed by INTAC. A transfer can only be stopped if it has no retry pending.

The Arbitration Control Registers are listed in Table 6.

Table 6 Arbitration Control Registers

OFFSET (HEX)	NAME	BIT	TYPE	DEFINITION
48	BurstDebi	28 to 26	RW	PCI burst length of the DEBI DMA channel; see Table 7.
	Burst3	20 to 18	RW	PCI burst length of video Channel 3; see Table 7.
	Thresh3	17 to 16	RW	Threshold of FIFO 3; see Table 8.
	Burst2	12 to 10	RW	PCI burst length of video Channel 2; see Table 7.
	Thresh2	9 to 8	RW	Threshold of FIFO 2; see Table 8.
	Burst1	4 to 2	RW	PCI burst length of video Channel 1; see Table 7.
	Thresh1	1 and 0	RW	Threshold of FIFO 1; see Table 8.
4C	BurstA1_in	28 to 26	RW	PCI burst length of audio input Channel 1 (see Table 7).
	ThreshA1_in	25 to 24	RW	Threshold of audio FIFOA1_in; see Table 8.
	BurstA1_out	20 to 18	RW	PCI burst length of audio output Channel 1; see Table 7.
	ThreshA1_out	17 and 16	RW	Threshold of audio FIFOA1_out; see Table 8.
	BurstA2_in	12 to 10	RW	PCI burst length of audio input Channel 2; see Table 7.
	ThreshA2_in	9 and 8	RW	Threshold of audio FIFOA2_in; see Table 8.
	BurstA2_out	4 to 2	RW	PCI burst length of audio output Channel 2; see Table 7.
	ThreshA2_out	1 and 0	RW	Threshold of audio FIFOA2_out; see Table 8.

Table 7 Burst length definition

VALUE	BURST LENGTH
000	1 Dword
001	2 Dwords
010	4 Dwords
011	8 Dwords
100	16 Dwords
101	32 Dwords
110	64 Dwords
111	128 Dwords

Table 8 Threshold definition

VALUE	WRITE MODE(1)		READ MODE(1)	
	VIDEO	AUDIO	VIDEO	AUDIO
00	4 Dwords of valid data	1 Dword of valid data	4 empty Dwords	1 empty Dword
01	8 Dwords of valid data	4 Dwords of valid data	8 empty Dwords	4 empty Dwords
10	16 Dwords of valid data	8 Dwords of valid data	16 empty Dwords	8 empty Dwords
11	32 Dwords of valid data	16 Dwords of valid data	32 empty Dwords	16 empty Dwords

Note

1. The threshold is reached, if the FIFO contains at least this number of Dwords.

8.2.6 STATUS INFORMATION OF THE PCI INTERFACE

Table 9 lists the status information the PCI interface makes available to the user in addition to the interrupt sources that are described later. This information is read only.

Table 9 Status bits of the DMA control

OFFSET (HEX)	NAME	BIT	TYPE	DESCRIPTION
120	VDP1	31 to 0	R	Logical video DMA pointer of FIFO 1
124	VDP2	31 to 0	R	Logical video DMA pointer of FIFO 2
128	VDP3	31 to 0	R	Logical video DMA pointer of FIFO 3
12C	ADP1	31 to 0	R	Logical audio DMA pointer of audio output FIFOA1_out
130	ADP2	31 to 0	R	Logical audio DMA pointer of audio input FIFOA1_in
134	ADP3	31 to 0	R	Logical audio DMA pointer of audio output FIFOA2_out
138	ADP4	31 to 0	R	Logical audio DMA pointer of audio input FIFOA2_in
13C	DDP	31 to 0	R	Logical DEBI DMA pointer

8.3 Main control

8.3.1 GENERAL

The SAA7146 has two Dwords of general control to support quick enable/disable switching of any activity of the SAA7146 via direct access by the CPU.

The main control Dwords are split in two parts. The upper parts have 16 bits of bit-mask to allow bit-selective write to the lower part which contains single bit enable/disable control of major interface functions of SAA7146. If a certain bit position is masked with a '1' in the mask word (upper 2 bytes) during a write access, then the corresponding bit in the control word (lower 2 bytes) is changed according to the contents of the transmitted data. By that the CPU can easily switch on or off certain selected interfaces of the SAA7146 without having to check the actual 'remaining' programming (enabling) of the other parts.

Table 10 Main Control Register 1

OFFSET	NAME	BIT	TYPE	DEFINITION
FCH	**Mask Word**			
	M15 to M00	31 to 16	RW	16-bit Mask Word for bit-selective writes to the Control Word.
	Control Word			
	MRST_N	15	RW	**Master Reset Not.** This is the Master Reset for the SAA7146. Writing a logic 0 to this bit will reset the SAA7146 to the same state as after a Power-on-reset. When read this bit always returns a logic 0.
	–	14	R	Reserved; read only bit.
	ERPS1	13	RW	**Enable Register Program Sequencer Task 1.** If ERPS1 = 1, then any RPS Task 1 action is enabled. If ERPS1 = 0, then RPS Task 1 action does not fetch any more commands.
	ERPS0	12	RW	**Enable Register Program Sequencer Task 0.** If ERPS0 = 1, then any RPS Task 1 action is enabled. If ERPS0 = 0, then RPS Task 1 action does not fetch any more commands.
	EDP	11	RW	**Enable DEBI Port Pins.** If EDP = 0, all pins of the DEBI port are 3-stated. If EDP = 1, then the function of all pins at the DEBI port is as programmed via the DEBI registers.
	EVP	10	RW	**Enable Real Time Video Ports Pins.** If EVP = 0, all 24 pins of the Real Time Video Interface (DD1 port) are 3-stated. If EVP = 1, then the function of all pins at the Real Time Video Interface (DD1 port) is as programmed by the Scaler Register; see Table 63.
	EAP	9	RW	**Enable Audio Port Pins.** If EAP = 0, all 14 pins of the Audio Interface Port are 3-stated. If EAP = 1, then the function of all pins at Audio Interface as programmed in Section 8.16.3.
	EI2C	8	RW	**Enable I^2C Port Pins.** If EI2C = 0, then both pins of the I^2C-bus Interface Port are 3-stated. If EI2C = 1, then the I^2C-bus interface is enabled and will function as programmed in Section 8.17.2.
	TR_E_DEBI	7	RW	Transfer enable bit of the DEBI.
	TR_E_1	6	RW	Transfer enable bit of video Channel 1. If set this channel is included in the internal arbitration scheme. If not set, this channel will be ignored and no transfer will start using this FIFO.
	TR_E_2	5	RW	Transfer enable bit of video Channel 2.
	TR_E_3	4	RW	Transfer enable bit of video Channel 3.
	TR_E_A2_OUT	3	RW	Transfer enable bit of audio Channel 2 out.
	TR_E_A2_IN	2	RW	Transfer enable bit of audio Channel 2 in.
	TR_E_A1_OUT	1	RW	Transfer enable bit of audio Channel 1 out.
	TR_E_A1_IN	0	RW	Transfer enable bit of audio Channel 1 in.

Table 11 Main Control Register 2

During initiation of an upload operation from the shadow RAM each of the UPLD bits [10 to 0] is assigned to a set of registers. If a logic 1 is written into a UPLD bit all dedicated shadow RAM registers containing changed data are uploaded into their working registers immediately. During a read cycle the UPLD bits give information on whether the shadow RAM contains changed data not yet uploaded into the working registers. The UPLD bits remain HIGH as long as the contents of the shadow RAM represents the current programming.

OFFSET (HEX)	NAME	BIT	TYPE	DEFINITION
100	**Mask Word**			
	M15 to M00	31 to 16	RW	16-bit Mask Word for bit-selective writes to the Control Word.
	Control Word			
	RPS_SIG4	15	RW	RPS Signal 4
	RPS_SIG3	14	RW	RPS Signal 3
	RPS_SIG2	13	RW	RPS Signal 2
	RPS_SIG1	12	RW	RPS Signal 1
	RPS_SIG0	11	RW	RPS Signal 0
	UPLD_D1_B	10	RW	Upload 'Video DATA stream handling at port D1_B (54H)'; see Table 65. To upload 'Initial setting of Dual D1 Interface (50H)', this bit and bit 9 must be set; see Table 63.
	UPLD_D1_A	9	RW	Upload 'Video DATA stream handling at port D1_A (54H)'; see Table 64. To upload 'Initial setting of Dual D1 Interface (50H)', this bit and bit 10 must be set; see Table 63.
	UPLD_BRS	8	RW	Upload 'BRS Control Register (58H)'; see Table 66.
	reserved	7	R	Read only.
	UPLD_HPS_H	6	RW	Upload 'HPS Horizontal-pre-scale (68H)'; see Table 75. Upload 'HPS Horizontal-fine-scale (6CH)'; see Table 77. Upload 'BCS control (70H)'; see Table 78.
	UPLD_HPS_V	5	RW	Upload 'HPS control (5CH)'; see Table 67. Upload 'HPS Vertical-scale (60H)'; see Table 68. Upload 'HPS Vertical-scale and gain (64H)'; see Table 69. Upload 'Chroma Key range (74H)'; see Table 82. Upload 'HPS Outputs and Formats (78H)'; see Table 83. Upload 'Clip control (78H)'; see Table 85.
	UPLD_DMA3	4	RW	Upload 'Video DMA3 registers'; (30H, 34H, 38H, 3CH, 40H, 44H and 48H [20 to 16]).
	UPLD_DMA2	3	RW	Upload 'Video DMA2 registers'; (18H, 1CH, 20H, 24H, 28H, 2CH and 48H [12 to 8]).
	UPLD_DMA1	2	RW	Upload 'Video DMA1 registers'; (00H, 04H, 08H, 0CH, 10H, 14H and 48H [4 to 0]).
	UPLD_DEBI	1	RW	Upload 'DEBI registers'; (88H, 7CH, 80H, 84H and 48H) [28 to 26]).
	UPLD_IIC	0	RW	Upload 'I^2C-bus registers'; (8CH and 90H).

8.4 Register Programming Sequencer (RPS)

The RPS is used as an additional method to program or read the registers of the SAA7146. Its main function is programming the registers on demand without delay via the interrupt handler of the host system.

Due to the fact that different applications of the SAA7146 can run independently of and asynchronously to each other the RPS is capable of running two parallel tasks. Both tasks are completely equal to each other and each has its own set of registers (RPS-Address, RPS-Page, HBI-Threshold and RPS-TimeOutValue). Each task can be separately enabled by setting its related ERPSx bit in the Main Control Register 1 (see Table 10). To allow communication between both tasks and the CPU there are five signals which can be set or reset from both tasks (see Table 11). The programming of a task is defined by an instruction list in the system main memory that consists of RPS-Commands. The operation of the RPS is initiated on command by setting the ERPS-bit of the desired task in the Main Control Register 1 (see Table 10).

The processing of RPS can be controlled by a sequence of wait commands on special events. Further the program flow can be controlled via conditional jumps related to the communication with the host setting semaphores or special interrupts.

8.4.1 RESET

During a reset the ERPS x (Enable RPS of Task x) bits in the Main Control Register 1(see Table 10) of the SAA7146 are cleared so that an RPS Task has to be explicitly started.

8.4.2 EVENT DESCRIPTION

Table 12 Description of events

EVENT	DESCRIPTION
IICD	**IIC Done.** Done flag of the I^2C.
DEBID	**DEBI Done.** Done flag of DEBI.
O_FID_A; O_FID_B	**Field Identification signal.** For an odd field dependent on sync-detection at Port A/Port B.
E_FID_A; E_FID_B	**Field Identification signal.** For an even field dependent on sync-detection at Port A/Port B.
HS	**HPS Source.** Wait for processing of source line before line addressed by SLCT is done.
HT	**HPS Target.** Wait for processing of target line before line addressed by TLCT is done.
VBI_A; VBI_B	**Vertical Blanking Indicator** at VS_A port/ VS_B port; for details on this signal see Table 86.
BRS_DONE	**Inactive BRS data path.** For details on this signal see Table 86.
HPS_DONE	**Inactive HPS data path between two windows.** For details on this signal see Table 86.
HPS_LINE_DONE	**Inactive HPS data path between two lines.** For details on this signal see Table 86.
VTD1; VTD2; VTD3	**Video Transfer Done.** Video DMA 1, Video DMA 2 or Video DMA 3 has transferred a complete window and is ready to be reprogrammed.
GPIO0	**General Purpose IO0.** This bit reflects the status of the GPIO Pin 0.
GPIO1	**General Purpose IO1.** This bit reflects the status of the GPIO Pin 1
GPIO2	**General Purpose IO2.** This bit reflects the status of the GPIO Pin 2.
GPIO3	**General Purpose IO3.** This bit reflects the status of the GPIO Pin 3.
SIGx	**General purpose signal x**. For intertask and RPS to CPU communication or program flow control. 'x' can take a value within the range 0 to 4.

8.4.3 COMMAND LIST

An instruction list of an RPS task is built in the system memory by the device driver. This list is made up of command sequences; each command being at least one Dword long. The first Dword of a command consists of the instruction code (4-bit) and a command specific part (28 bits). Commands longer than one Dword contain data in the additional Dwords.

Table 13 Command Dword

D31 to 28	D27 to 0
Instruction code	command specific

8.4.4 THE INSTRUCTION CODE

The instruction code identifies one of the following commands (see bits 31 to 28 of Tables 14 to 29).

8.4.4.1 PAUSE

The PAUSE command is a one Dword-command. This command contains in the command specific part the events to wait for; see Tables 14 and 15. The execution of the RPS task is delayed until the condition addressed via the events becomes true or a time out occurs.

To control the time a PAUSE command stays in the wait state it is possible to set a RPS-time out value. This value specifies after how many PCI-clocks and/or V_syncs a time out will be asserted. When it occurs the RPS_TO bit in the PSR is set and if enabled an interrupt will be generated. Anyway, the RPS will stop this task.

The OAN bit specifies if the condition in bits 25 to 0 is an AND (OAN set to '0') or if the condition is an OR (OAN set to '1'). If the INV bit is set this command will wait for the condition to become false.

8.4.4.2 UPLOAD

The UPLOAD command is a one Dword-command. This command contains in the command specific part the sections to be uploaded from the shadow RAM to the working registers. See Tables 16 and 17.

If the UPLOAD command finds a bit of a section set it uploads the corresponding registers from the shadow RAM to the working registers. This is done for registers with changed shadow RAM values only.

8.4.4.3 CHECK-LATE

The CHECK-LATE command is a one Dword-command. This command contains in the command specific part the events to check and if necessary to wait for, as shown in Tables 18 and 19. The execution of the RPS task is delayed until the condition addressed via the events becomes true, or a time out occurs and the upload is performed.

The OAN bit specifies if the condition in bits 25 to 0 is an AND (OAN set to '0') or if the condition is an OR (OAN set to '1'). If the INV bit is set this command will wait for the condition to become false.

If the CHECK_LATE command finds that the wait-condition is already true the RPS-LATE is set. Otherwise it waits for the condition as the PAUSE command. A time out behaviour such as described for the PAUSE command is supplied as well.

8.4.4.4 CLR_SIGNAL

The Clear Signal command clears selected signals. This will not effect the real status bit of the SAA7146. Only a copy of this bit related to the RPS will be cleared. It will be set again on the one hand via a SET_SIGNAL command or on the other hand when the real status will be set due to normal processing. The instruction code is $0. The CLR_SIGNAL format is shown in Tables 20 and 21.

8.4.4.5 NOP

The NOP command consists of one Dword and has the instruction code 0000. All bits of the command specific part have to be set to zero. This command is a special case of the CLR_SIGNAL command.

8.4.4.6 SET_SIGNAL

The Set Signal command sets the selected signals. If one of the SAA7146 status related signals is selected to be set, it will not effect the real status bit of the SAA7146. Only a copy of this bit related to the RPS, will be set. The SET_SIGNAL format is shown in Tables 22 and 23.

8.4.4.7 INTERRUPT

The Interrupt command will set the RPS_I bit of the task in the Interrupt Status Register if it is executed and the condition described by the event flags is true. The execution of RPS continues. The format of the Interrupt command is shown in Tables 24 and 25.

The OAN bit specifies if the condition in bits 25 to 0 is an AND (OAN set to '0') or if the condition is an OR (OAN set to '1'). If the INV bit is set this command will wait for the condition to become false.

8.4.4.8 STOP

The STOP command will terminate the RPS execution and reset the ERPS-bit. The command specific part of the STOP command is like the INTERRUPT command. If the addressed event is true the STOP will be executed otherwise the execution will continue with the next command. If no event is addressed the STOP will be executed unconditionally. The format of the STOP command is shown in Tables 26 and 27.

The OAN bit specifies if the condition in bits 25 to 0 is an AND (OAN set to '0') or if the condition is an OR (OAN set to '1'). If the INV bit is set this command will wait for the condition to become false.

8.4.4.9 JUMP

The JUMP command is a two Dword command. The second Dword contains the physical address at which the RPS will continue its execution. The address in the second Dword is directly transferred to the RPSAddr Register. The command specific part of the JUMP command is like the INTERRUPT command. If the addressed event is true the JUMP will be performed otherwise the execution will continue at the next command. If no event is addressed the JUMP will be unconditional. The format of the JUMP command is shown in Tables 28 and 29.

The OAN bit specifies if the condition in bits 25 to 0 is an AND (OAN set to '0') or if the condition is an OR (OAN set to '1'). If the INV bit is set this command will wait for the condition to become false

Table 14 PAUSE Command format

D31 TO D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
0010	OAN	INV	SIG4	SIG3	SIG2	SIG1	SIG0	GPIO3	GPIO2	GPIO1	GPIO0	HT

Table 15 PAUSE Command format (continued)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
HS	O_FID_B	E_FID_B	O_FID_A	E_FID_A	VBI_A	VBI_B	BRS_DONE	–	HPS_ LINE_ DONE	HPS_DONE	VTD3	VTD2	VTD1	DEBID	IICD

Table 16 Upload Command format

D31 TO D28	D25 TO D11	D10	D9	D8	D7	D6
0100	reserved	Video Data stream handling at Port DI_b (54H); see Table 65.	Video Data stream handling at Port DI_b (54H); see Table 64.	BRS Control Register (58H); see Table 66.	reserved	Horizontal-pre-scale (68H); see Table 75. Horizontal-fine-scale (6CH); see Table 77. BCS Control (70H); see Table 78.
		Initial setting of Dual D1 Interface (50H)				

Table 17 Upload Command format (continued)

D5	D4	D3	D2	D1	D0
HPS control (5CH); see Table 67. HPS Vertical scale (60H); see Table 68. HPS Vertical scale and gain (64H); see Table 69. Chroma key range (74H); see Table 82. HPS Output and Formats (78H); see Table 83. Clip control (78H); see Table 85.	Video DMA3 (30H, 34H, 38H, 3CH, 40H, 44H, 48H); [20 to 16]	Video DMA2 (18H, 1CH, 20H, 24H, 28H, 2CH, 48H); [12 to 8]	Video DMA1 (00H, 04H, 08H, 0CH, 10H, 14H, 48H); [4 to 0]	DEBI (88H, 7CH, 80H, 84H, 48H); [28 to 26]	IIC(8CH, 90H)

Table 18 CHECK_LATE Command DWORD format

D31 TO D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
0011	OAN	INV	SIG4	SIG3	SIG2	SIG1	SIG0	GPIO3	GPIO2	GPIO1	GPIO0	HT

Table 19 CHECK_LATE Command DWORD format (continued)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
HS	O_FID_B	E_FID_B	O_FID_A	E_FID_A	VBI_A	VBI_B	BRS_DONE	–	HPS_ LINE_ DONE	HPS_DONE	VTD3	VTD2	VTD1	DEBID	IICD

Table 20 CLR_SIGNAL Command format

D31 TO D28	D27 TO D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
0000	reserved	SIG4	SIG3	SIG2	SIG1	SIG0	GPIO3	GPIO2	GPIO1	GPIO0	HT

Table 21 CLR_SIGNAL Command format (continued)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
HS	O_FID_B	E_FID_B	O_FID_A	E_FID_A	VBI_A	VBI_B	BRS_DONE	–	HPS_ LINE_ DONE	HPS_DONE	VTD3	VTD2	VTD1	DEBID	IICD

Table 22 SET_SIGNAL Command format

D31 TO D28	D27 TO D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
0001	reserved	SIG4	SIG3	SIG2	SIG1	SIG0	GPIO3	GPIO2	GPIO1	GPIO0	HT

Table 23 SET_SIGNAL Command format (continued)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
HS	O_FID_B	E_FID_B	O_FID_A	E_FID_A	VBI_A	VBI_B	BRS_DONE	–	HPS_ LINE_ DONE	HPS_DONE	VTD3	VTD2	VTD1	DEBID	IICD

Table 24 INTERRUPT Command format

D31 TO D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
0110	OAN	INV	SIG4	SIG3	SIG2	SIG1	SIG0	GPIO3	GPIO2	GPIO1	GPIO0	HT

Table 25 INTERRUPT Command format (continued)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
HS	O_FID_B	E_FID_B	O_FID_A	E_FID_A	VBI_A	VBI_B	BRS_DONE	–	HPS_ LINE_ DONE	HPS_DONE	VTD3	VTD2	VTD1	DEBID	IICD

Table 26 STOP Command format

D31 TO D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
0101	OAN	INV	SIG4	SIG3	SIG2	SIG1	SIG0	GPIO3	GPIO2	GPIO1	GPIO0	HT

Table 27 STOP Command format (continued)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
HS	O_FID_B	E_FID_B	O_FID_A	E_FID_A	VBI_A	VBI_B	BRS_DONE	–	HPS_ LINE_ DONE	HPS_DONE	VTD3	VTD2	VTD1	DEBID	IICD

Table 28 JUMP Command format

D31 TO D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
1000	OAN	INV	SIG4	SIG3	SIG2	SIG1	SIG0	GPIO3	GPIO2	GPIO1	GPIO0	HT

Table 29 JUMP Command format (continued)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
HS	O_FID_B	E_FID_B	O_FID_A	E_FID_A	VBI_A	VBI_B	BRS_DONE	–	HPS_ LINE_ DONE	HPS_DONE	VTD3	VTD2	VTD1	DEBID	IICD

8.4.4.10 LDREG, STREG

The Load Register command has a variable Dword count specified by the Block_length. It is at least two Dwords long and at maximum, 256 Dwords. The Store Register command is a two DWORD command.

Table 30 LDREG Command format

D31 to 28	D27 to 16	D15 to 8	D7	D6 to 0
1001	Reserved	Block_length	Reserved	Register Address (Register offset divided-by-4)

Table 31 STREG Command format

D31 to 28	D27 to 16	D15 to 8	D7	D6 to 0
1010	Reserved	Block_length	Reserved	Register Address (Register offset divided-by-4)

The LDREG command interprets the following Dwords as data and writes it in the registers beginning at the specified register address (D6 to D0).

The STREG command is a two Dword command. It transfers the contents of the addressed (D6 to D0) SAA7146 register into PCI memory that is addressed by interpreting the contents of the next data Dword as the 32-bit target base address.

The Block_length entry defines the number of data Dwords to be processed by these commands. This enables the access to multiple registers on following addresses within a single RPS-command. The value specified must be at least one. If more than one Dword is accessed the register address is incremented each cycle by one. A value of zero is reserved and the command will be interpreted as a NOP.

The Register Address defines the target register address in Dwords. If this address points to a non-existent register the RPS_RE bit for the actual task will be set and if enabled an interrupt will be generated The command will be ignored and the execution of RPS continues.

All reserved bits should be written as '0's and should be ignored during read cycles.

8.4.4.11 MASKLOAD

The MASKLOAD command is a three Dword command. Its purpose is to modify only portions or selected bits of a SAA7146 register. The first Dword of the command contains the instruction code and specifies the register to be modified. The second Dword contains the mask and the third Dword contains the data to written to the register through this mask. The mask works as follows: if a bit in the mask is set the data from the third Dword at the corresponding bit position will be transferred to the register. If a bit in the mask is zero the corresponding bit in the register will stay unchanged.

Table 32 MASKLOAD Command first DWORD

D31 to 28	D27 to 7	D6 to 0
1100	Reserved	Register Address (Register offset divided-by-4)

8.4.5 Operation

The operation of the RPS is controlled by the enable bits in the Main Control Register 1 (see Table 10). If one of these bits is set the related RPS task starts its execution with the command addressed by the task related RPSAddr Register.

When a RPS task is switched on it immediately starts fetching its data via DMA beginning at the actual address pointer's location. Four Dwords are fetched at a time and loaded into an instruction queue. Operation continues to the end of the queue at the time the RPS DMA loads the next four Dwords in the RPS list.

To monitor the ongoing execution and the end of RPS there are status and interrupt bits for each task in the Primary Status Register and the Secondary Status Register (see Tables 38 and 39).

8.4.6 RPS-Address Register

The start address of the RPS list of each task is defined in the RPS Address Register of the task. The start address must be Dword aligned.

Table 33 RPS-Address Register

OFFSET (HEX)	NAME	BIT	TYPE	DESCRIPTION
104	RPS_ADDR0	31 to 2	RW	Default Value: 0
		1 and 0		00
108	RPS_ADDR1	31 to 2	RW	Default Value: 0
		1 and 0		00

During an RPS list execution this register works like a program counter. Since the RPS can write data into the main memory of the system a protection mechanism is implemented. There is a 4 kbyte page in the memory for each task in which the RPS tasks are allowed to write in. Every write access outside this page will cause an error and the RPS task will stop immediately. If the corresponding bit in the Interrupt Enable Register is set an interrupt will be generated. This protection mechanism can be disabled via the Enable RPS Page Register (ERPSP) bit. This bit is located at bit 0 of the RPS Page Register. A zero enables page errors. This bit is a logic 1 after a reset.

Table 34 RPS-Page Register

OFFSET (HEX)	NAME	BIT	TYPE	DESCRIPTION
C4	RPS_PAGE0	31 to 12	RW	Default value: 0
	reserved	11 to 1		0
	ERPSP0	0		Enable RPS Page Register 0
C8	RPS_PAGE1	31 to 12	RW	Default value: 0
	reserved	11 to 1		0
	ERPSP1	0		Enable RPS Page Register 1

8.4.7 Line Counter Thresholds

For the events related to the line counters of the source and the target, there are for each task two thresholds in the HBITRx. The purpose of this register is to set the HS or HT event flag when the corresponding line counter has reached the threshold. These thresholds must be written before waiting on the event. A value of zero as threshold turns the HS or HT event on, for every line.

Table 35 HBI Threshold Register

OFFSET (HEX)	NAME	BIT	TYPE	DESCRIPTION
CC	–	31 to 29	R	Reserved; read only.
	TLCS0	28	RW	**Target Line Counter Select for Task 0.** This bit defines if the TLCT0 refers to the HPS (a logic 0) or to the BRS (a logic 1).
	TLCT0	27 to 16	RW	**Target Counter Threshold for Task 0.** Specifies the threshold for the Target Line Counter.
	–	15 to 13	R	Reserved; read only.
	SLCS0	12	RW	**Source Line Counter Select for Task 0.** The bit defines if the SLCT0 refers to the HPS '0' or to the BRS '1'.
	SLCT0	11 to 0	RW	**Source Line Counter Threshold for Task 0.** Specifies the threshold for the Source Line Counter.
D0	–	31 to 29	R	Reserved; read only.
	TLCS1	28	RW	**Target Line Counter Select for Task 1.** This bit defines if the TLCT refers to the HPS '0' or to the BRS '1'.
	TLCT1	27 to 16	RW	**Target Line Counter Threshold for Task 1.** Specifies the threshold for the Target Line Counter.
	–	15 to 13	R	Reserved; read only.
	SLCS1	12	RW	**Source Line Counter Select for Task 1.** This bit defines if the SLCT1 refers to the HPS '0' or to the BRS '1'.
	SLCT1	11 to 0	RW	**Source Line Counter Threshold for Task 1.** Specifies the threshold for the Source Line Counter.

8.4.8 RPS Time Out Value

These registers contain the values for the time out conditions for the PAUSE and CHECK_LATE commands for each task. If the selected count value is zero the time out generation is disabled.

Table 36 RPS Time Out Value

OFFSET (HEX)	NAME	BIT	TYPE	DESCRIPTION
D4	V_TO0	31	RW	These two bits determine how the RPS_TO0 is generated; see Table 37.
	C_TO0	30	RW	
	V_ABN0	29	RW	This bit determines which port the V_sync for the time out check comes from. A logic 1 selects Port A; a logic 0 selects Port B.
	–	28	–	Reserved.
	Vsync_Cnt0	27 to 24	RW	This is a 4 bit value which sets the V_sync time out between 1 and 15 V_syncs.
	PCI_Cnt0	23 to 0	RW	This value specifies after how many PCI_Clocks a time out should be detected.
D8	V_TO1	31	RW	These two bits determine how the RPS_TO1 is generated; see Table 37.
	C_TO1	30	RW	
	V_ABN1	29	RW	This bit determines which port the V_sync for the time out check comes from. A logic 1 selects Port A; a logic 0 selects Port B.
	–	28	–	Reserved.
	Vsync_Cnt1	27 to 24	RW	This is a 4 bit value which sets the V_sync time out between 1 and 15 V_syncs
	PCI_Cnt1	23 to 0	RW	This value specifies after how many PCI_Clocks a time out should be detected.

Table 37 RPS_TOX generation

V_TOX	C_TOX	RPS_TOX GENERATED FORMAT
0	0	No time out check
0	1	PCI-Clock time out check
1	0	V_sync time out check
1	1	both time out checks

8.5 Status and Interrupts

8.5.1 General

To control the SAA7146 status information is collected and stored in two status registers: Primary Status Register (PSR) and Secondary Status Register (SSR). These two registers follow a hierarchical approach because the PSR contains summed up information from the SSR. Interrupts can only be generated from the PSR and are enabled via the Interrupt Enable Register (IER). If an interrupt condition occurs and the interrupt is enabled, the corresponding bit in the Interrupt Status Register (ISR) is set. These bits can be cleared by writing a logic 1 into them.

Both Status Registers are read only. Writing a logic 1 into any of the Primary Status Register bits causes the corresponding interrupt to be generated if enabled. Writing a logic 0 has no effect.

Table 38 Primary Status Register (PSR)

OFFSET (HEX)	NAME	BIT	TYPE	DESCRIPTION	RESET
110	PPEF	31	R	**PCI Parity Error.** This bit is set when a PCI Parity Error occurs during any transfer other than 'real time video data'. The bit in the ISR is set on the rising edge of this status bit.	ISR[31]
	PABO	30	R	**PCI Access Error.** This bit is set when the PCI interface starts an access, and has either a target or master abort. The bit in the ISR is set on the rising edge of this status bit.	ISR[30]
	PPED	29	R	**PCI Parity Errors on 'real time Data'.** This bit is set when a parity error has occurred since the last Vsync or under RPS since the last wait.	
	RPS_I1	28	R	**Interrupt issued by RPS command from Task 1.**	
	RPS_I0	27	R	**Interrupt issued by RPS command from Task 0.**	
	RPS_late1	26	R	**RPS Task 1 late.** RPS Task 1 late is set by the CHECK_LATE command. This bit is reset by starting a new RPS Task 1.	
	RPS_late0	25	R	**RPS Task 0 late.** RPS Task 0 late is set by the CHECK_LATE command. This bit is reset by starting a new RPS Task 0.	
	RPS_E1	24	R	**RPS_Error Task 1.** This bit reflects the status of the RPS error bits for Task 1 in the Secondary Status Register (see Table 39). This bit is reset by starting a new RPS Task 1.	
	RPS_E0	23	R	**RPS_Error Task 0.** This bit reflects the status of the RPS error bits for Task 0 in the Secondary Status Register (see Table 39). This bit is reset by starting a new RPS Task 0.	
	RPS_TO1	22	R	**RPS time out error in Task 1.** This bit is set when the RPS Task 1 stays longer than expected in the WAIT state. This bit is reset by starting a new RPS Task 1.	

OFFSET (HEX)	NAME	BIT	TYPE	DESCRIPTION	RESET
110	RPS_TO0	21	R	**RPS time out error in Task 0.** This bit is set when the RPS Task 0 stays longer than expected in the WAIT state. This bit is reset by starting a new RPS Task 0.	
	UPLD	20	R	**RPS in UPLOAD.** This bit is active while RPS uploads the working registers from the shadow RAM. The bit in the ISR is set on the falling edge of this status bit.	
	DEBI_S	19	R	**DEBI Status.** This bit stays set as long as DEBI is processing or halted by an error. The bit in the ISR is set on the falling edge of this status bit, which indicates a 'DEBI Done'.	
	DEBI_E	18	R	**DEBI Error/Event.** This bit is set when one of the two DEBI error/event flags (DEBI_EF or DEBI_TO) in the SSR is set. This bit is reset when a new DEBI command starts. The reset value of DEBI_TO is a logic 1.	
	IIC_S	17	R	**I^2C Status.** This bit stays set as long as I^2C-bus is transmitting data or halted by an error. The bit in the ISR is set on the falling edge of this status bit, which indicates a 'I^2C Done'.	
	IIC_E	16	R	**I^2C Error.** This bit gets set when one of the I^2C-bus status bits in the SSR is set. This bit is reset when a new I^2C-bus transfer starts.	
	A2_in	15	R	**Audio input DMA2 protection.** This bit is set when the Audio input DMA2 address generation exceeded an 'address boundary' or hit its 'limit' (protection address). It is reset with starting the DMA channel again.	
	A2_out	14	R	**Audio output DMA2 protection.** This bit is set when the Audio output DMA2 address generation exceeded an 'address boundary' or hit its 'limit' (protection address). It is reset with starting the DMA channel again.	
	A1_in	13	R	**Audio input DMA1 protection.** This bit is set when the Audio input DMA1 address generation exceeded an 'address boundary' or hit its 'limit' (protection address). It is reset with starting the DMA channel again.	
	A1_out	12	R	**Audio output DMA1 protection.** This bit is set when the Audio output DMA1 address generation exceeded an 'address boundary' or hit its 'limit' (protection address). It is reset with starting the DMA channel again.	
	AFOU	11	R	**Audio FIFO Overflow/Underflow.** This bit gets set when one of the four Audio FIFOs has an Underflow or Overflow.	
	V_PE	10	R	**Video address Protection Error.** This bit is set, when one of the Video DMAs 1 to 3 has an address protection error during an active transmission.	
	VFOU	9	R	**Video FIFO Overflow/Underflow.** This bit is set if any of the Video FIFOs1, 2 or 3 has an overflow or underflow.	

OFFSET (HEX)	NAME	BIT	TYPE	DESCRIPTION	RESET
110	FIDA	8	R	**Field ID Port A.** Via the FIDESA bits in the 'Initial setting of the Dual D1 Interface' (see Table 63), selected edge(s) of this signal will set the corresponding bit in the ISR when enabled.	
	FIDB	7	R	**Field ID Port B.** Via the FIDESB bits in the 'Initial setting of the Dual D1 Interface' (see Table 63), selected edge(s) of this signal will set the corresponding bit in the ISR when enabled.	
	PIN3	6	R	**GPIO Pin 3.** This bit reflects the state of the General Purpose Pin 3. Via the GPIO register, selected edge(s) of this signal will set the corresponding bit in the ISR when enabled.	
	PIN2	5	R	**GPIO Pin 2.** This bit reflects the state of the General Purpose Pin 2. Via the GPIO register, selected edge(s) of this signal will set the corresponding bit in the ISR when enabled.	
	PIN1	4	R	**GPIO Pin 1.** This bit reflects the state of the General Purpose Pin 1. Via the GPIO register selected edge(s) of this signal will set the corresponding bit in the ISR when enabled.	
	PIN0	3	R	**GPIO Pin 0.** This bit reflects the state of the General Purpose Pin 0. Via the GPIO register selected edge(s) of this signal will set the corresponding bit in the ISR when enabled.	
	ECS	2	R	**Event Counter Status.** This bit reflects the status of the four (SSR) Event Counter status bits EC5S, EC4S, EC2S and EC1S.	
	EC3S	1	R	**Event Counter 3 Status.** This bit is set when Event Counter 3 exceeds its threshold.	
	EC0S	0	R	**Event Counter 0 Status.** This bit is set when Event Counter 0 exceeds its threshold.	

Table 39 Secondary Status Register (SSR)

OFFSET (HEX)	NAME	BIT	TYPE	DESCRIPTION
114	PRQ	31	R	**PCI Request Pending.** This bit is set while the PCI has asserted its REQ-signal and has not received a GNT yet.
	PMA	30	R	**PCI master access.** This bit is active as long as the SAA7146 acts as a master on the PCI bus.
	RPS_RE1	29	R	**RPS Task 1 Register access Error.** This bit is set when the LDREG, STREG or MASKWRITE command tries to access a non-existing register. This bit is reset by writing a logic 1 to the RPS_E1 bit in the ISR or when a new RPS Task 1 is started.
	RPS_PE1	28	R	**RPS Task 1 Page Error.** This bit is set when the RPS Task 1 tries to write to an address outside the 4 Kbyte page. This bit is reset by writing a logic 1 to the RPS_E1 bit in the ISR or when a new RPS Task 1 is started.
	RPS_A1	27	R	**RPS Task 1 Active.** This bit is set whenever RPS Task 1 is executing and not staying in a wait condition or uploading the working registers.

OFFSET (HEX)	NAME	BIT	TYPE	DESCRIPTION
114	RPS_RE0	26	R	**RPS Task 0 Register access Error.** This bit is set when the LDREG, STREG or MASKWRITE command tries to access a non-existing register. This bit is reset by writing a logic 1 to the RPS_E0 bit in the ISR or when a new RPS Task 0 is started.
	RPS_PE0	25	R	**RPS Task 0 Page Error.** This bit is set when the RPS Task 0 tries to write-access an address outside the 4 kbyte page. This bit is reset by writing a logic 1 to the RPS_E0 bit in the ISR or when a new RPS Task 0 is started.
	RPS_A0	24	R	**RPS Task 0 Active.** This bit is set whenever RPS Task 0 is executing and not staying in a wait condition or uploading the working registers.
	DEBI_TO	23	R	**DEBI Time Out.** This bit is set, when the last DEBI command was terminated by a time out. This bit is reset by writing a logic 1 to the DEBI_E bit in the ISR. Reset value is a logic 1.
	DEBI_EF	22	R	**DEBI Format Error.** This bit indicates an illegal command to immediate transfer across a Dword boundary. This bit is reset by writing a logic 1 to the DEBI_E bit in the ISR.
	IIC_EA	21	R	**I²C Address Error.** This bit is set when there is no acknowledge after the device address. This bit is reset by writing a logic 1 to the I2C_E bit in the ISR or when a new I²C command starts.
	IIC_EW	20	R	**I²C Write data Error.** This bit is set when there is no acknowledge during the writing of the data byte(s). This bit is reset by writing a logic 1 to the I2C_E bit in the ISR or when a new I²C-bus command starts.
	IIC_ER	19	R	**I²C Read data Error.** This bit is set when there is no acknowledge during reading of the data byte(s). This bit is reset by writing a logic 1 to the I2C_E bit in the ISR or when a new I²C-bus command starts.
	IIC_EL	18	R	**I²C Loss arbitration Error.** This bit is set when the I²C-bus loses its arbitration. This bit is reset by writing a logic 1 to the I2C_E bit in the ISR or when a new I²C-bus command starts.
	IIC_EF	17	R	**I²C Frame Error.** This bit is set when there is an invalid start/stop condition since the last I²C-bus command. This bit is reset by writing a logic 1 to the I2C_E bit in the ISR or when a new I²C-bus command starts.
	V3P	16	R	**Video DMA 3 Protection error.** This bit is set when Video DMA3 generates an address during an active transmission beyond its protection address. This bit is reset by writing a logic 1 to the V_PE bit in the ISR or by re-loading the DMA base address.
	V2P	15	R	**Video DMA 2 Protection error.** This bit is set when Video DMA2 generates an address during an active transmission beyond its protection address. This bit is reset by writing a logic 1 to the V_PE bit in the ISR or by re-loading the DMA base address.
	V1P	14	R	**Video DMA 1 Protection error.** This bit is set when Video DMA1 generates an address during an active transmission beyond its protection address. This bit is reset by writing a logic 1 to the V_PE bit in the ISR or by re-loading the DMA base address.
	VF3	13	R	**Video FIFO 3 underflow/overflow.** This bit is set when the Video FIFO3 has an overflow/underflow. This bit is reset when reloading the DMA base address or by writing a logic 1 to the VFOU bit in the ISR.

OFFSET (HEX)	NAME	BIT	TYPE	DESCRIPTION
114	VF2	12	R	**Video FIFO 2 underflow/overflow.** This bit is set when the Video FIFO2 has an overflow/underflow. This bit is reset when reloading the DMA base address or by writing a logic 1 to the VFOU bit in the ISR.
	VF1	11	R	**Video FIFO 1 underflow/overflow.** This bit is set when the Video FIFO 1 has an overflow/underflow. This bit is reset when reloading the DMA base address or by writing a logic 1 to the VFOU bit in the ISR.
	AF2_in	10	R	**Audio input FIFO 2 underflow.** This bit is set when the Audio input FIFO 2 has an underflow. This bit is reset by restarting the DMA channel or by writing a logic 1 to the AFOU bit in the ISR.
	AF2_out	9	R	**Audio output FIFO 2 overflow.** This bit is set when the Audio output FIFO 2 has an overflow. This bit is reset by restarting the DMA channel or by writing a logic 1 to the AFOU bit in the ISR.
	AF1_in	8	R	**Audio input FIFO 1 underflow.** This bit is set when the Audio input FIFO 1 has an underflow. This bit is reset by restarting the DMA channel or by writing a logic 1 to the AFOU bit in the ISR.
	AF1_out	7	R	**Audio output FIFO 1 overflow.** This bit is set when the Audio output FIFO 1 has an overflow. This bit is reset by restarting the DMA channel or by writing a logic 1 to the AFOU bit in the ISR.
	reserved	6	R	Read only; returns a '0' when read.
	VGT	5	R	**Vertical Gate.** This bit reflects the vertical gate at the HPS output.
	LNQG	4	R	**Line qualifier gate.** This bit reflects the horizontal gate at the HPS output.
	EC5S	3	R	**Event Counter 5 Status.** This bit is set when the Event Counter 5 exceeds its threshold. This bit is reset by writing a logic 1 to the ECS bit in the ISR.
	EC4S	2	R	**Event Counter 4 Status.** This bit is set when Event Counter 4 exceeds its threshold. This bit is reset by writing a logic 1 to the ECS bit in the ISR.
	EC2S	1	R	**Event Counter 2 Status.** This bit is set when Event Counter 2 exceeds its threshold. This bit is reset by writing a logic 1 to the ECS bit in the ISR.
	EC1S	0	R	**Event Counter 1 Status.** This bit is set when Event Counter 1 exceeds its threshold. This bit is reset by writing a logic 1 to the ECS bit in the ISR.

Table 40 Interrupt Enable Register (IER)

OFFSET (HEX)	NAME	BIT	Type	DESCRIPTION
DC	PPEF	31	RW	PCI Parity Error interrupt enable
	PABO	30	RW	PCI Access Error interrupt enable
	PPED	29	RW	PCI Parity Errors on 'real time Data' interrupt enable
	RPS_I1	28	RW	Enables interrupts issued by RPS commands in Task 1
	RPS_I0	27	RW	Enables interrupts issued by RPS commands in Task 0
	RPS_late1	26	RW	RPS Task 1 late interrupt enable
	RPS_late0	25	RW	RPS Task 0 late interrupt enable
	RPS_E1	24	RW	RPS_Error1 interrupt enable
	RPS_E0	23	RW	RPS_Error0 interrupt enable
	RPS_TO1	22	RW	RPS time out Task 1 interrupt enable
	RPS_TO0	21	RO	RPS time out Task 0 interrupt enable
	UPLD	20	RW	RPS Upload interrupt enable
	DEBI_S	19	RW	DEBI Status interrupt enable
	DEBI_E	18	RW	DEBI Error interrupt enable
	IIC_S	17	RW	I^2C Status interrupt enable
	IIC_E	16	RW	I^2C Error interrupt enable
	A2_in	15	RW	Audio input DMA2 protection interrupt enable
	A2_out	14	RW	Audio output DMA2 protection interrupt enable
	A1_in	13	RW	Audio input DMA1 protection interrupt enable
	A1_out	12	RW	Audio output DMA1 protection interrupt enable
	AFOU	11	RW	Audio FIFO Overflow/Underflow interrupt enable
	V_PE	10	RW	Video address Protection Error interrupt enable
	VFOU	9	RW	Video FIFO Overflow/Underflow interrupt enable
	FIDA	8	RW	Field ID port A interrupt enable
	FIDB	7	RW	Field ID port B interrupt enable
	PIN3	6	RW	GPIO Pin 3 interrupt enable
	PIN2	5	RW	GPIO Pin 2 interrupt enable
	PIN1	4	RW	GPIO Pin 1 interrupt enable
	PIN0	3	RW	GPIO Pin 0 interrupt enable
	ECS	2	RW	Event Counter 1, 2, 4 and 5 Status interrupt enable
	EC3S	1	RW	Event Counter 3 Status interrupt enable
	EC0S	0	RW	Event Counter 0 Status interrupt enable

Table 41 Interrupt Status Register (ISR)

OFFSET (HEX)	NAME	BIT	TYPE	DESCRIPTION
10C	PPEF	31	RW	PCI Parity Error interrupt status
	PABO	30	RW	PCI Access Error interrupt status
	PPED	29	RW	PCI Parity Errors on 'real time Data' interrupt status
	RPS_I1	28	RW	Interrupt issued by RPS command from Task 1 interrupt status
	RPS_I0	27	RW	Interrupt issued by RPS command from Task 0 interrupt status
	RPS_late1	26	RW	RPS Task 1 is late interrupt status
	RPS_late0	25	RW	RPS Task 0 is late interrupt status
	RPS_E1	24	RW	RPS_Error from Task 1 interrupt status
	RPS_E0	23	RW	RPS_Error from Task 0 interrupt status
	RPS_TO1	22	RW	RPS time out Task 1 interrupt status
	RPS_TO0	21	RW	RPS time out Task 0 interrupt status
	UPLD	20	RW	RPS Upload interrupt status
	DEBI_S	19	RW	DEBI Status interrupt status
	DEBI_E	18	RW	DEBI Error interrupt status
	IIC_S	17	RW	I^2C Status interrupt status
	IIC_E	16	RW	I^2C Error interrupt status
	A2_in	15	RW	Audio input DMA2 protection interrupt status
	A2_out	14	RW	Audio output DMA2 protection interrupt status
	A1_in	13	RW	Audio input DMA1 protection interrupt status
	A1_out	12	RW	Audio output DMA1 protection interrupt status
	AFOU	11	RW	Audio FIFO Overflow/Underflow interrupt status
	V_PE	10	RW	Video address Protection Error interrupt status
	VFOU	9	RW	Video FIFO Overflow/Underflow interrupt status
	FIDA	8	RW	Field ID port A interrupt status
	FIDB	7	RW	Field ID port B interrupt status
	PIN3	6	RW	GPIO Pin 3 interrupt status
	PIN2	5	RW	GPIO Pin 2 interrupt status
	PIN1	4	RW	GPIO Pin 1 interrupt status
	PIN0	3	RW	GPIO Pin 0 interrupt status
	ECS	2	RW	Event Counter 1, 2, 4 and 5 interrupt status
	EC3S	1	RW	Event Counter 3 interrupt status
	EC0S	0	RW	Event Counter 0 interrupt status

8.6 GPIO

8.6.1 General

The SAA7146 has four general purpose I/O pins. The purpose of these four pins is to have the possibility to map some special functions to the outside. For example they could be used to signal to other devices a power-down mode or to map an internal status bit to it, e.g. to detect a sync lost from the VBLK pin of the SAA7110.

Table 42 GPIO Registers

OFFSET (HEX)	NAME	BIT	TYPE	DESCRIPTION
E0	GPIO3	31 to 24	RW	GPIO3 Control Register
	GPIO2	23 to 16	RW	GPIO2 Control Register
	GPIO1	15 to 8	RW	GPIO1 Control Register
	GPIO0	7 to 0	RW	GPIO0 Control Register

Table 43 GPIO Control Register

7	6	5	4	3	2	1	0	DESCRIPTION
0	0	0	0	X	X	X	X	input, no interrupt condition
0	0	0	1	X	X	X	X	input, rising edge is interrupt condition
0	0	1	0	X	X	X	X	input, falling edge is interrupt condition
0	0	1	1	X	X	X	X	input, both edges are interrupt condition
0	1	X	0	X	X	X	X	output, fixed constant LOW
0	1	X	1	X	X	X	X	output, fixed constant HIGH
1	0	X	X	X	X	X	X	reserved
1	1	s5	s4	s3	s2	s1	s0	output, monitoring the selected status bits of PSR or SSR; see Table 48

8.7 Event Counter

The event counters in the SAA7146 provide the possibility of obtaining a statistical look at the different interrupt sources. For this purpose there are six counters implemented in two registers (EC1R and EC2R). Each register contains one 12-bit counter and two 10-bit counters. To be flexible in the information collected in the counters it is possible to map each status bit to any counter. This is done via the Event Counter Source Select Register (ECSSR). The four 10-bit counters and the two 12-bit counters are able to select one of the 64 possible sources (see Table 47). In addition to the counting, it is possible to generate interrupts via threshold values for the counters. These thresholds are kept in the two Event Threshold Registers (ET1R and ET2R). If a counter exceeds its threshold it is reset to zero and the corresponding status bit is set.

Table 44 Event Counter set 1 Register (EC1R)

OFFSET (HEX)	NAME	BIT	TYPE	DESCRIPTION
read:118	EC2 [9:0]	31 to 22	R	**Event Counter Three.** This is the second 10-bit counter.
	EC1 [9:0]	21 to 12	R	**Event Counter Two.** This is the first 10-bit counter.
	EC0 [1:0]	11 to 0	R	**Event Counter One.** This is the first 12-bit counter.

Table 45 Event Counter set 2 Register (EC2R)

OFFSET (HEX)	NAME	BIT	TYPE	DESCRIPTION
11C	EC5 [9:0]	31 to 22	R	**Event Counter Six.** This is the fourth 10-bit counter.
	EC4 [9:0]	21 to 12	R	**Event Counter Five.** This is the third 10-bit counter.
	EC3 [11:0]	11 to 0	R	**Event Counter Four.** This is the second 12-bit counter.

Table 46 Event Counter set 1 Source Select Register 1(EC1SSR)

OFFSET (HEX)	NAME	BIT	TYPE	DESCRIPTION
E4	–	31 to 24	R	Reserved; read only.
	ECS2 [5:0]	23 to 18	RW	**Event Counter 2 Source.** This 6 bit value addresses one of the status bits.
	ECEN2	17	RW	**Event Counter 2 Enable.** If this bit is set, Event Counter 2 is enabled.
	ECCLR2	16	RW	**Event Counter 2 Clear.** Writing a logic 1 to this bit will clear Event Counter 2. This bit always reads a logic 0.
	ECS1 [5:0]	15 to 10	RW	**Event Counter 1 Source.** This 6 bit value addresses one of the status bits.
	ECEN1	9	RW	**Event Counter 1 Enable.** If this bit is set Event Counter 1 is enabled.
	ECCLR1	8	RW	**Event Counter 1 Clear.** Writing a logic 1 to this bit will clear Event Counter 1. This bit always reads a logic 0.
	ECS0[5:0]	7 to 2	RW	**Event Counter 0 Source.** This 6 bit value addresses one of the status bits.
	ECEN0	1	RW	**Event Counter 0 Enable.** If this bit is set Event Counter 0 is enabled.
	ECCLR0	0	RW	**Event Counter 0 Clear.** Writing a logic 1 to this bit will clear Event Counter 0. This bit always reads a logic 0.

Table 47 Event Counter set 2 Source Select Register (EC2SSR)

OFFSET (HEX)	NAME	BIT	TYPE	DESCRIPTION
E8	–	31 to 24	R	Reserved; read only.
	ECS5 [5:0]	23 to 18	R	**Event Counter 5 Source.** This 6 bit value addresses one of the status bits.
	ECEN5	17	RW	**Event Counter 5 Enable.** If this bit is set the Event Counter 5 is enabled.
	ECCLR5	16	RW	**Event Counter 5 Clear.** Writing a logic 1 to this bit will clear Event Counter 5. This bit always reads a logic 0.
	ECS4 [5:0]	15 to 10	RW	**Event Counter 4 Source.** This 6 bit value addresses one of the status bits.
	ECEN4	9	RW	**Event Counter 4 Enable.** If this bit is set Event Counter 4 is enabled.
	ECCLR4	8	RW	**Event Counter 4 Clear.** Writing a logic 1 to this bit will clear Event Counter 4. This bit always reads a logic 0.
	ECS3 [5:0]	7 to 2	RW	**Event Counter 3 Source.** This 6 bit value addresses one of the status bits.
	ECEN3	1	RW	**Event Counter 3 Enable.** If this bit is set Event Counter 3 is enabled.
	ECCLR3	0	RW	**Event Counter 3 Clear.** Writing a logic 1 to this bit will clear Event Counter 3. This bit always reads a logic 0.

Table 48 Status bit addresses

ADDRESS (HEX)	STATUS BIT	EVENTS TO BE COUNTED
00	PPEF	number of PCI Parity errors
01	PABO	number of PCI Access errors
02	PPED	every PCI clock cycle with 'data' parity error
03	RPS_I1	number of RPS interrupts Task 1
04	RPS_I0	number of RPS interrupts Task 0
05	RPS_LATE1	number of RPS late errors for Task 1
06	RPS_LATE0	number of RPS late errors for Task 0
07	RPS_E1	number of RPS errors for Task 1
08	RPS_E0	number of RPS errors for Task 0
09	RPS_TO1	number of time-outs for RPS Task 1
0A	RPS_TO0	number of time-outs for RPS Task 0
0B	UPLD	time for upload, in PCI clocks
0C	DEBI_S	time DEBI is busy, in PCI clocks
0D	DEBI_E	number of DEBI errors in total
0E	IIC_S	time I^2C is busy, in PCI clocks
0F	IIC_E	number of I^2C errors in total
10	A2_in	number of protection hits
11	A2_out	number of protection hits

ADDRESS (HEX)	STATUS BIT	EVENTS TO BE COUNTED
12	A1_in	number of protection hits
13	A1_out	number of protection hits
14	AFOU	number of audio FIFOs overflows/underflows in total
15	V_PE	number of video FIFO protection violations in total
16	VFOU	number of video FIFOs overflows/underflows in total
17	FIDA	number of odd/even fields on port A (defined via FIDESA)
18	FIDB	number of odd/ even fields on port B (defined via FIDESB)
19	PIN3	number of active edges as defined in the GPIO registers; see Table 43
1A	PIN2	number of active edges as defined in the GPIO registers; see Table 43
1B	PIN1	number of active edges as defined in the GPIO registers; see Table 43
1C	PIN0	number of active edges as defined in the GPIO registers; see Table 43
1D	ECS	number of threshold overflows from EC1, EC2, EC4 and EC5 in total
1E	EC3S	number of threshold overflows of EC3S
1F	EC0S	number of threshold overflows of EC0S
20	PRQ	time from REQ to GNT, in PCI clocks
21	PMA	time in active master mode, in PCI clocks
22	RPS_RE1	number of RPS register access errors for Task 1
23	RPS_PE1	number of page errors for RPS Task 1
24	RPS_A1	time of RPS Task 1 busy, in PCI clocks
25	RPS_RE0	number of RPS register access errors for Task 0
26	RPS_PE0	number of page errors for RPS Task 0
27	RPS_A0	time of RPS Task 0 busy, in PCI clocks
28	DEBI_TO	number of DEBI time out errors
29	DEBI_EF	number of format errors on DEBI port
2A	IIC_EA	number of address errors on the I^2C-bus
2B	IIC_EW	number of I^2C write data errors
2C	IIC_ER	number of I^2C read data errors
2D	IIC_EL	number of arbitration losses on the I^2C-bus
2E	IIC_EF	number of I^2C frame errors
2F	V3P	number of protection violations for video FIFO 3
30	V2P	number of protection violations for video FIFO 2
31	V1P	number of protection violations for video FIFO 1
32	VF3	number of missed Dwords
33	VF2	number of missed Dwords

ADDRESS (HEX)	STATUS BIT	EVENTS TO BE COUNTED
34	VF1	number of missed Dwords
35	AF2_in	number of missed Dwords
36	AF2_out	number of missed Dwords
37	AF1_in	number of missed Dwords
38	AF1_out	number of missed Dwords
39	–	reserved
3A	VGT	number of Vsyncs in acquisition of HPS
3B	LNQG	number of output lines
3C	EC5S	number of threshold overflows of EC5
3D	EC4S	number of threshold overflows of EC4
3E	EC2S	number of threshold overflows of EC2
3F	EC1S	number of threshold overflows of EC1

Table 49 Event Counter Threshold set 1 Register (ECT1R)

OFFSET (HEX)	NAME	BIT	TYPE	DESCRIPTION
EC	ECT2 [9:0]	31 to 22	RW	**Event Counter 2 Threshold.** This is the threshold for the second 10-bit counter; see note 1.
	ECT1 [9:0]	21 to 12	RW	**Event Counter 1 Threshold.** This is the threshold for the first 10-bit counter; see note 1.
	ECT0 [11:0]	11 to 0	RW	**Event Counter 0 Threshold.** This is the threshold for the first 12-bit counter; see note 1.

Note

1. Each of these threshold values shows the limit up to which the related counter will run before it sets it interrupt status bit.

Table 50 Event Counter Threshold set 2 Register (ECT2R)

OFFSET (HEX)	NAME	BIT	TYPE	DESCRIPTION
F0	ECT6 [9:0]	31 to 22	RW	**Event Counter 5 Threshold.** This is the threshold for the fourth 10-bit counter; see note 1.
	ECT5 [9:0]	21 to 12	RW	**Event Counter 4 Threshold.** This is the threshold for the third 10-bit counter; see note 1.
	ECT4 [11:0]	11 to 0	RW	**Event Counter 3 Threshold.** This is the threshold for the second 12-bit counter; see note 1.

Note

1. Each of these threshold values shows the limit up to which the related counter will run before it sets it interrupt status bit.

8.8 Video processing

8.8.1 The real time Video Interface

The real time Video Interface consists of two bidirectional 8-bit wide ports, transporting colour difference samples and luminance samples in byte sequential manner. Each of the two video ports has its own clock pin, pixel qualifier and horizontal and vertical sync signal pin. The sync signal can optionally be coded in SAV and EAV codes according to D1 standard (SMPTE125M or CCIR 656). The two 8-bit ports can be combined to form a single 16-bit wide YUV port, to be backwards compatible to the DMSD2 output format.

8.8.2 DD1: Dual D1 (CCIR 656, SMPTE125M), I/O

8.8.2.1 Cb-Y-Cr-Y 8-bit wide stream

In this mode two video ports with YUV 4 : 2 : 2 sampling scheme are available. Each D1 port is I/O capable and has a separate clock input and separate sync lines. In this format the pixel rate is equivalent to the clock rate LLC. The colour difference signal sample and luminance signal sample (straight binary) are byte-wise multiplexed into the same 8-bit wide data stream, with sequence and timing in accordance to CCIR 656 recommendation (respectively according to D1 for 60 Hz application). The incoming and scaled data are reformatted to 16-bit for the HPS data path and the corresponding reference signals are generated. A discontinuous data stream is supported by accepting or generating a pixel/byte qualifying signal (PXQ = 1: qualified pixel, PXQ = 0: invalid data). The start condition for synchronizing to the correct Cb-Y-Cr-Y-sequence is given by the selected horizontal reference signal. The sequence increments only with qualified bytes.

8.8.2.2 YUV 16-bit parallel (DMSD2) stream

In this mode only the HPS data path is available. The BRS data path supports only 8-bit wide data streams. Colour difference signal and luminance signal (straight binary) are available in parallel on a 16-bit wide data stream. In this mode both D1 ports are inputs. With this format the pixel rate is half the clock rate LLC. The start condition for synchronising the clock divider and/or the correct U-V-sequence is given by the CREF signal, which must connect to the same port as the colour difference signal is connected to.

8.8.3 Video Data Formats on DD1

D1 (SMPTE125M, CCIR 656) as well as YUV16 represent both the same 4 : 2 : 2 sample scheme. Both formats, D1 and YUV16, are assumed to conform to CCIR recommendation 601 coding:

Y = 16 = black, 0%

Y = 235 = white, 100% brightness

U,V = 128 = no colour, 0% saturation

U,V = 128 ±112 = full colour, 100% saturation.

Data path processing in HPS and BRS, does not limit to this range and allows overshoots and uses 'margins' for processing. The reference values can be manipulated by the BCS processing in the HPS data path.

SAV and EAV are only decoded, and removed from the signal stream (substituted with neighbouring first or last active video sample), if so chosen. But even then, 'single' codes of '00' and/or 'FF' in data stream, i.e. not as part of SAV or EAV, remain in the data stream, and they are processed as data.

In case of video output at DD1, the codes '00' and 'FF' are optionally suppressed as video data in all modes, i.e. if raster signals (syncs) are not encoded in SAV and EAV.

The sync signals are always presented at the extra pins, independent of encoding into SAV and EAV.

8.8.4 SYNCHRONIZATION SIGNALS

Horizontal, vertical and frame synchronization signals are carried on the extra sync pins of DD1 (one pair of sync pins per D1 Channel), and/or are encoded as SAV and EAV in the 8-bit wide video signal stream. For the 16-bit wide YUV stream, sync signals are always on extra pins. For D1 video inputs, the SAA7146 is programmed to determine where to recover the synchronization information, from the dedicated sync pins, or from the encoded SAV and EAV codes in the data stream.

For D1 video outputs, the SAA7146 can be programmed to deliver synchronization information in SAV and EAV codes, and/or on the dedicated sync pins. Non standard rastered video signals are supported by sync signals at the dedicated sync pins, as well as via SAV and EAV codes. The number of clocks and pixels per line, and lines per field can be non-standard, and can assume numbers up to 4095.

The signal at the HS pin can assume the following functions:

- HS: input only, the rising edge is selected to act as timing reference
- HREF: input only, gated with CREF, the rising edge is selected as timing reference
- HGT: I/O, HIGH during active video
- ACT input only: HIGH during active video, inactive during horizontal and vertical blanking
- HGT and ACT: envelope all active pixels (there is no active pixel outside HGT or ACT), but may also include clock cycles marked as not valid pixels by means of PXQ.

The vertical sync signal can assume the following functions:

- VS: input only positive or negative, one edge is selected as timing reference:
  - if selected edge of VS and selected edge of HS are in phase, then begin 1st (odd) field
  - if selected edges of VS and HS are out of phase, then begin 2nd (even) field.
- V-dmsd: input only, falling (trailing) edge is timing reference:
  - if falling edge of V-dmsd is in high phase of HREF, then begin 1st (odd) field
  - if falling edge of V-dmsd is in low phase of HREF, then begin 2nd (even) field.
- VGT: I/O, HIGH during active video, (no holes for horizontal blanking)
- FS: input only, positive or negative, frame sync, (odd-even), (313-312, 263-262 lines) HIGH in one field, LOW in the other, changes on full line boundaries only.

8.8.5 FIELD DETECTION

The fields are detected simultaneously at both D1 sync-inputs. The results are available in two status registers.

8.8.5.1 Field detection control

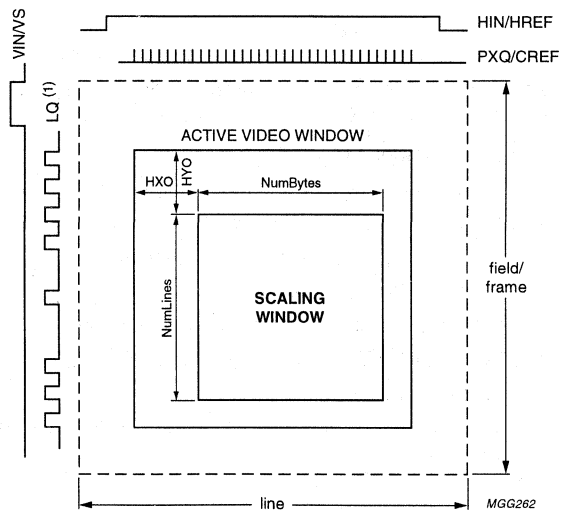
Field detection modes:

- Direct mode: FLD signal detected from incoming H/V signals
- Forced toggle: FLD signal regularly synchronized to source, but will never stay more than two fields with the same ID
- Free toggle: FLD signal toggles with every vertical reference signal, independent of source FID.

8.8.6 ACQUISITION CONTROL

The processing window for the scaling unit is defined in the acquisition control. An internal counter receives programmable values for offset (HXO11 to HXO0, HYO11 to HYO0 and BXO9 to BXO0, BYO9 to BYO0) and length (bits NumLines, NumBytes) and is reset by the corresponding sync reference input signal. The horizontal counter increments in qualified pixels for the HPS and qualified bytes for the BRS, the vertical counter increments in qualified lines, i.e. lines containing at least one qualified pixel. In order to avoid programming dependent line drop effects, the horizontal offset value must not exceed the number of pixels per line.

The acquisition provides the possibility to re-program the vertical offset after the previous job is done (End Of Window at the HPS and BRS is reached). So multiple windows during one field can be opened.



(1) LQ = qualified lines, i.e. lines containing at least one qualified pixel.

Fig.7 Reference signals for scaling window.

8.8.7 Comparison between CCIR 656 line and Source Line Counter

This Section describes how to choose the vertical offset and how to use the source line counter event for RPS programming, to capture the expected line.

The internal Source Line Counter (SLC) is reset by the selected edge of the vertical sync signal which is provided at port VS_X. The falling and rising edges of this signal are selected by the SYNC_X bits in the Initial settings DD1 Port Register (50H). Consequently, the behaviour of the Source Line Counter depends upon the connected vertical sync signal, so that different offsets must be selected to capture the expected line. The active video begins in the CCIR 656 line 23 of the video signal; Table 51 lists the different offsets which must be selected to capture the expected line. The subsequent diagrams and tables illustrate the relationship between the different vertical sync signals of the PAL and NTSC standards, the ODD and EVEN field and the internal Source Line Counter.

Table 51 Offsets to CCIR 656 line 23 depending on PAL or NTSC source, ODD and EVEN field and select mode (see note 1)

PAL				NTSC			
SLC SAV/EAV[2]	**SLC ext. FS**[3]	**SLC FALLING VS**[4]	**SLC RISING VS**[5]	**SLC SAV/EAV**	**SLC ext. FS**	**SLC FALLING VS**	**SLC RISING VS**
24 (25) 18H (19H)	15 (16) 0FH (10H)	16H (15) 0FH (10H)	21 (22) 15H (16H)	22 (22) 16H (16H)	12 (13)) 0CH (0DH)	12 (13) 0CH (0DH)	18 (19) 12H (13H)

Notes

1. Line numbers in brackets refer to EVEN field counting.
2. (SLC with SAV/EAV detection (50H, SYNC_X = 7).
3. SLC with external Field Identification Signal (50H, SYNC_X = 6).
4. SLC with detection on the falling edge of the vertical sync signal (50H, SYNC_X = 11, 3 or 5).
5. SLC with detection on the rising edge of the vertical sync signal. For Philips devices, the rising edge does not include field information, this information is only defined at the falling edge of the VS signal (50H, SYNC_X = 0, 2 or 4).

8.8.7.1 Video with PAL format

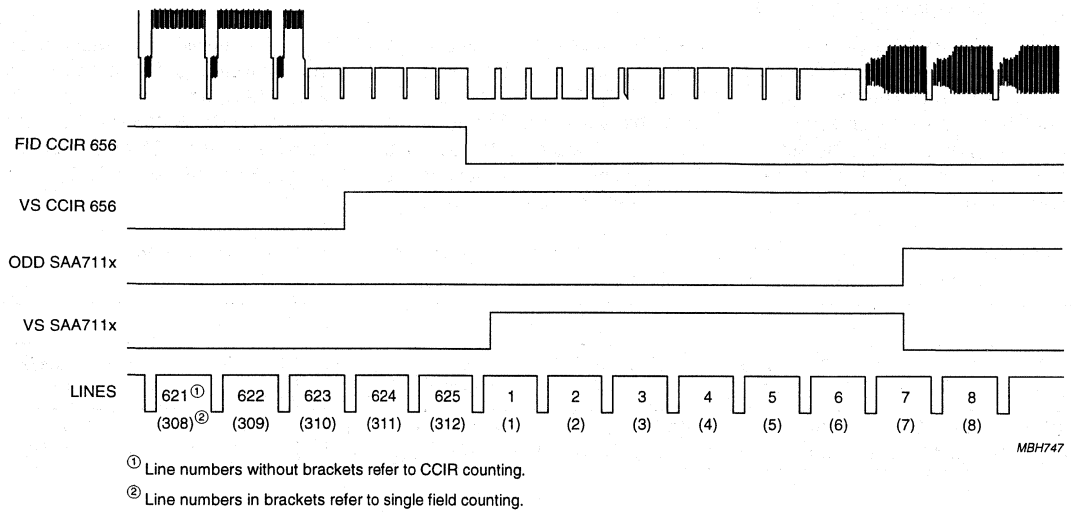


Fig.8 Output timing of SAA711x, 50 Hz, lines 621 to 8.

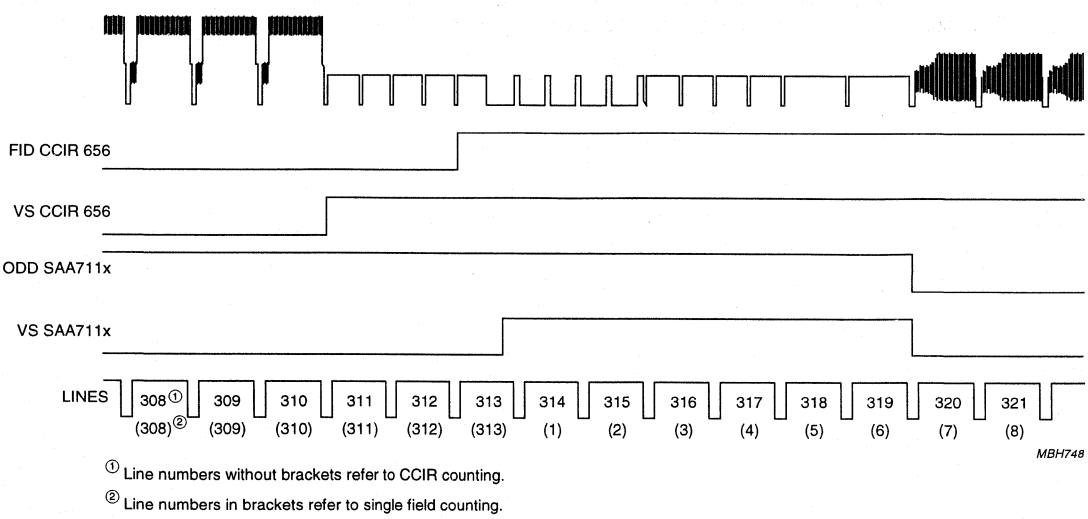


Fig.9 Output timing of SAA711x, 50 Hz, lines 308 to 321.

Table 52 Comparison between CCIR 656 lines and Source Line Counter (note 1)

CCIR 656 (D1) LINE[2]	612 (310)	622 (311)	624 (312)	625 (313)	1 (314)	2 (315)	3 (316)	4 (317)	5 (318)	6 (319)	7 (320)	8 (321)	9 (322)	10 (323)	11 (324)	12 (325)	13 (326)	14 (328)	15 (329)
SLC[3] SAV/EAV	311 (313)	312 (1)	1 (2)	2 (3)	3 (4)	4 (5)	5 (6)	6 (7)	7 (8)	8 (9)	9 (10)	10 (11)	11 (12)	12 (13)	13 (14)	14 (15)	15 (16)	16 (17)	17 (18)
SLC ext. FS[4]	302 (304)	303 (305)	304 (306)	305 (307)	306 (308)	307 (309)	308 (310)	309 (311)	310 (312)	311 (313)	312 (1)	1 (2)	2 (3)	3 (4)	4 (5)	5 (6)	6 (7)	7 (8)	8 (9)
SLC falling VS[5]	302 (304)	303 (305)	304 (306)	305 (307)	306 (308)	307 (309)	308 (310)	309 (311)	310 (312)	311 (313)	312 (1)	1 (2)	2 (3)	3 (4)	4 (5)	5 (6)	6 (7)	7 (8)	8 (9)
SLC rising VS[6]	308 (310)	309 (311)	310 (312)	311 (313)	312 (1)	1 (2)	2 (3)	3 (4)	4 (5)	5 (6)	6 (7)	7 (8)	8 (9)	9 (10)	10 (11)	11 (12)	12 (13)	13 (14)	14 (15)

Notes

1. Line numbers in brackets refer to EVEN field counting.
2. CCIR 656 (D1) line.
3. SLC with SAV/EAV detection (50H, SYNC_X = 7).
4. SLC with external Field Identification Signal (50H, SYNC_X = 6).
5. SLC with detection on the falling edge of the vertical sync signal (50H, SYNC_X = 11, 3 or 5).
6. SLC with detection on the rising edge of the vertical sync signal. For Philips devices, the rising edge does not include field information, this information is only defined at the falling edge of the VS signal (50H, SYNC_X = 0, 2 or 4).

8.8.7.2 Video with NTSC format

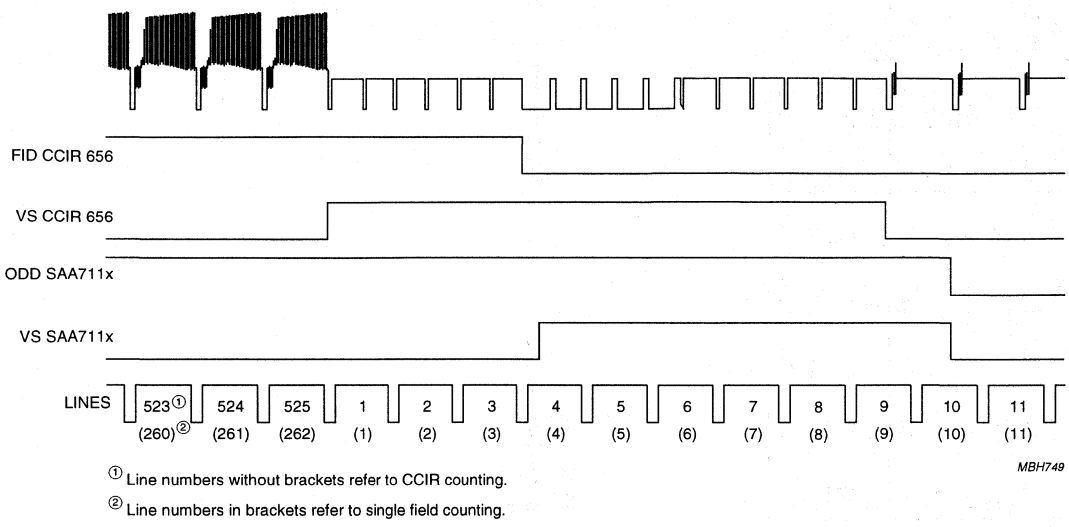


Fig.10 Output timing of SAA711x, 60 Hz, lines 523 to 11.

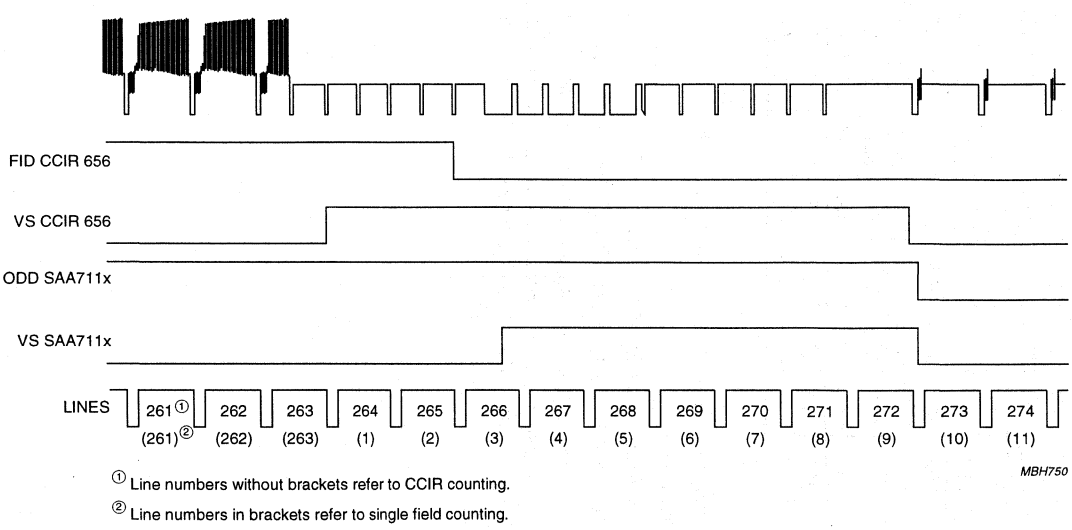


Fig.11 Output timing of SAA711x, 60 Hz, lines 261 to 274.

Table 53 Comparison between CCIR 656 lines and Source Line Counter (note 1)

CCIR 656 (D1) LINE[2]	525 (262)	1 (264)	2 (265)	3 (266)	4 (267)	5 (268)	6 (269)	7 (270)	8 (271)	9 (272)	10 (273)	11 (274)	12 (275)	13 (276)	14 (277)	15 (278)	16 (279)	17 (280)	18 (281)
SLC SAV/EAV[3]	262 (263)	1 (1)	2 (2)	3 (3)	4 (4)	5 (5)	6 (6)	7 (7)	8 (8)	9 (9)	10 (10)	11 (11)	12 (12)	13 (13)	14 (14)	15 (15)	16 (16)	17 (17)	18 (18)
SLC ext. FS[4]	252 (251)	253 (252)	254 (253)	255 (254)	256 (255)	257 (256)	258 (257)	259 (258)	260 (259)	261 (260)	262 (261)	1 (262)	2 (263)	3 (1)	4 (2)	5 (3)	6 (4)	7 (5)	8 (6)
SLC falling VS[5]	252 (251)	253 (252)	254 (253)	255 (254)	256 (255)	257 (256)	258 (257)	259 (258)	260 (259)	261 (260)	262 (261)	1 (262)	2 (263)	3 (1)	4 (2)	5 (3)	6 (4)	7 (5)	8 (6)
SLC rising VS[6]	258 (260)	259 (261)	260 (262)	261 (263)	262 (1)	1 (2)	2 (3)	3 (4)	4 (5)	5 (6)	6 (7)	7 (8)	8 (9)	9 (10)	10 (11)	11 (12)	12 (13)	13 (14)	14 (15)

Notes

1. Line numbers in brackets refer to EVEN field counting.
2. CCIR 656 (D1) line.
3. SLC with SAV/EAV detection (50H, SYNC_X = 7).
4. SLC with external Field Identification Signal (50H, SYNC_X = 6).
5. SLC with detection on the falling edge of the vertical sync signal (50H, SYNC_X = 11, 3 or 5).
6. SLC with detection on the rising edge of the vertical sync signal. For Philips devices, the rising edge does not include field information, this information is only defined at the falling edge of the VS signal (50H, SYNC_X = 0, 2 or 4).

8.9 High Performance Scaler (HPS)

Dependent upon the selected port modes, the incoming and scaled data are formatted/reformatted (8 or 16-bit) and the corresponding reference signals are generated. Based on these reference signals, the active processing window is defined in a versatile way, via programming. The Programming Register can be loaded during the processing of the previous field, frame or line by RPS. In this way each D1 port gets processed in a field or frame alternating manner. If the incoming signals are not locked, the acquisition is waiting for the new active video of the subsequent field. The corresponding fields are detected by a Field Detection. To support asynchronous video processing in the two video paths, each D1 port has its own Field Detection. The video signal source is also source for the qualify signal PXQ.

Before being processed in the central scaling unit, the incoming data passes to the BCS control unit, where monitor control functions for adjusting brightness and contrast (luminance) as well as saturation (chrominance) are implemented (BCS Control). The horizontal scaling is carried out in two steps, a prefiltering (bandwidth limitation for initialising) and a horizontal fine scaling. Between them the vertical processing is performed.

8.9.1 BCS Control

The parameters for brightness, contrast and saturation can be adjusted in the BCS control unit. The luminance signal can be controlled by the bits BRIG7 to BRIG0 and CONT6 to CONT0. The chrominance signal can be controlled by the bits SAT6 to SAT0.

Brightness control (BRIG7 to BRIG0):

- 00H; minimum offset
- 80H; CCIR level
- FFH; maximum offset.

Contrast control (CONT6 to CONT0):

- 00H; luminance off
- 40H; CCIR level
- 7FH; 1.9999 amplitude.

Saturation control (SAT6 to SAT0):

- 00H; colour off
- 40H; CCIR level
- 7FH; 1.9999 amplitude.

Limiting: All resulting output values are limited to minimum (equals 0) and maximum (equals 255).

8.9.2 Scaling Unit

The scaling to a randomly sized window is done in three steps:

- Horizontal Prescaling (bandwidth limitation for anti-aliasing, via FIR prefiltering and subsampling)
- Vertical Scaling (generating phase interpolated or vertically lowpassed lines)
- Horizontal Phasescaling (phase correct scaling to the new geometric relations).

The scaling process generates a new pixel/clock qualifier sequence. There are restrictions in the combination of input sample rate and up- or down scaling mode and scaling factor. The maximum resulting output sample rate at the DD1 port is ½LLC, due to support of CCIR 656 format.

8.9.2.1 *Horizontal prescaling*

The incoming pixels in the selected range are preprocessed in the Horizontal Prescaler, first stage of the scaling unit. It consists of a FIR Prefilter and a pixel collecting Subsampler.

8.9.2.2 *FIR Prefilter*

The video components Y, U and V are FIR prefiltered, to reduce the signal bandwidth in accordance to the downscale for factors between 1 and ½, so aliasing due to signal bandwidth expansion is reduced. The Prefilter consists of 3 filter stages, the transfer functions are listed in the Scaler Register section. The Prefilter is controlled by the Scaler Register bits PFY3 to PFY0 and PFUV3 to PFUV0 in the HPS Horizontal-pre-scale Register (see Table 75).

Figures 12 and 13 show frequency response and the corresponding Scaler Register settings. The prefilter operates on YUV 4 : 4 : 4 data. As U and V is generated by simple chroma pixel doubling, the UV prefilter should also be used to generate the interpolated chroma values.

8.9.2.3 *Subsampler*

To improve the scaling performance for scales less than ½ down to icon size, a FIR filtering subsampler is available. It performs a subsampling of the incoming data by a factor of 1/N, where N = 1 to 64. This operation is controlled by XPSC, with N = XPSC + 1. With NIP = number of input pixels/line and NOP = number of desired output pixels/line, the basic equation to calculate XPSC is:

XPSC = TRUNC [(NIP/NOP) – 1]

The subsampler collects a number of XPSC + (2 – XACM) pixels, to calculate a new subsampled output pixel. So a downscale dependent FIR filter is built, which reduces anti-aliasing for small sizes. If XACM = 0, the collecting sequence overlaps, which means that the last pixel of sequence M is also the first pixel of sequence M + 1. To implement a real subsampler bypass XACM has to be set to a logic 1.

As the phase correct horizontal fine scaling is limited to a maximum down scale of ¼, this circuitry has to be used for downscales less than ¼ of the incoming pixel count. To get unity gain at the subsamplers output for all subsampling ratios, the Scaler Register parameters CXY, CXUV and DCGX have to be used. In addition this can be used to modify the FIR characteristic of the subsampler slightly. Table 54 illustrates examples for Scaler Register settings, dependent on a given prescale ratio. Referring to Table 54, note that an internal XPSC dependent automatic prenormalization is valid for:

XPSC > 8, > 16, > 32, which reduces the input signal quantization. In addition note that for:
XPSC ≥ 5 the LSB of the CXY,CXUV parameter becomes valid.

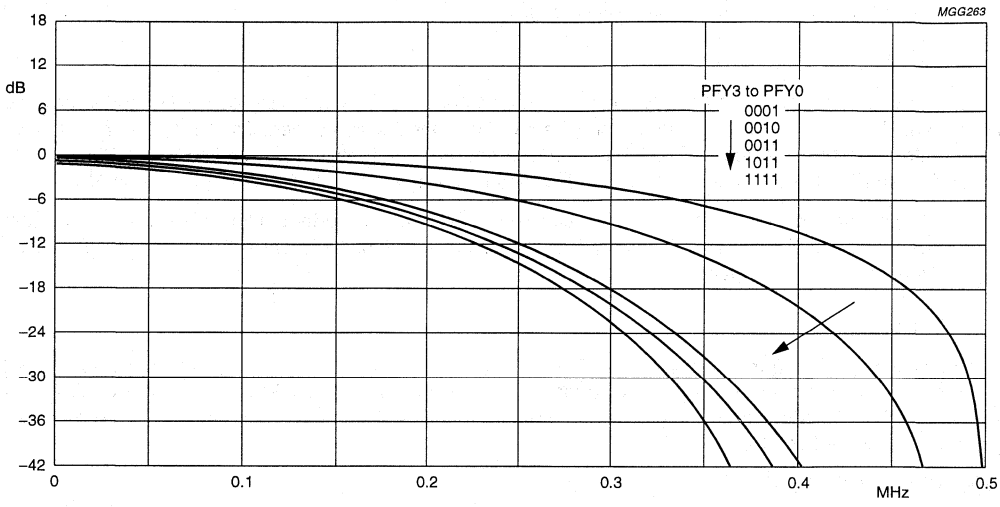


Fig.12 Luminance Prefilter: frequency response for miscellaneous register settings.

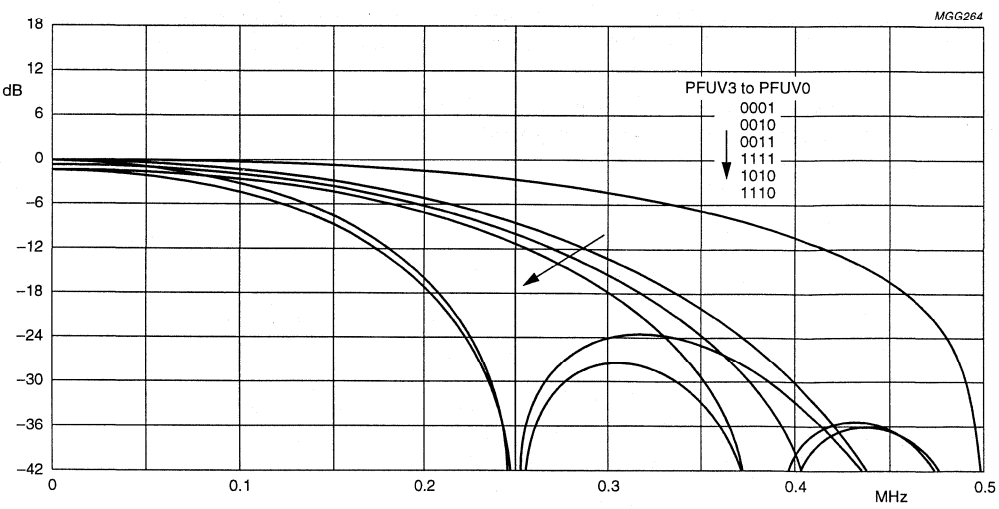


Fig.13 Chrominance Prefilter: frequency response for miscellaneous register settings.

Table 54 Horizontal prescaling and normalization

HORIZON. PRESCAL.	XPSC	COEFFICIENT SEQUENCE (EXAMPLE)	CXY (LUMINANCE CXUV (CHROMA)	WEIGHT SUM	DCGX	BCS (CONTR. I SAT.) = X/Y × 64
1	0	1-1	00	2	1	1
1/2	1	1-1-1	00	3	1	2/3
		1-2-1	02	4	2	1
1/3	2	1-1-1-1	00	4	2	1
1/4	3	1-1-1-1-1	00	5	2	4/5
		1-2-2-2-1	06	8	3	1
1/5	4	111 111	00	6	2	4/6
		121 121	02	8	3	1
		112 211	04	8	3	1
1/6	5	111 1 111	00	7	3	8/7
		111 2 111	08	8	3	1
1/7	6	1111 1111	00	8	3	1
1/8	7	1111 1 1111	00	9	3	8/9
		1222 2 2221	1E	16	7	1
1/9	8	11111 11111	00	10/2	2	4/5
		12212 21221	16	16/2	3	1
		11222 22211	1C	16/2	3	1
1/10	9	1111 1 1 1 1111	00	11/2	2	8/11
		1212 1 2 1 2121	2A	16/2	3	1
		1112 2 2 2 2111	38	16/2	3	1
1/11	10	1111 11 11 1111	00	12/2	2	8/12
		1211 21 12 1121	12	16/2	3	1
		1111 22 22 1111	30	16/2	3	1
1/15	14	1111 1111 1111 1111	00	16/2	3	1
1/16	15	1111 1111 1 1111 1111		17/2	3	16/17
		12222222222222221	FF	32/2	7	1
1/17	16	1111 1111	00	18/4	2	16/18
				xx/4		
1/33	32	1111 1111	00	34/8	2	
1/63	62					
1/64	63					

8.9.2.4 *Vertical Scaler*

The Vertical Scaler performs the vertical downscaling of the input data stream to a random number of output lines. It can be used for input line lengths up to 768 pixels/line. However, if the input line length exceeds this pixel count the Vertical Scaler must be bypassed. For the Vertical Scaling there are two different modes implemented: the ACCU mode (vertical accumulation) and LPI mode (Linear Phase Interpolation).

8.9.2.5 *ACCU mode (scaling factor range 1 to 1/1024; YACM = 1)*

The output lines are generated by a scale dependent variable averaging of maximum 64 input lines each. For a given scaling factor S, the YSCI (scaling increment), YACL (accumulation length; optimum: 1 line overlap), YPE (scaling start phase for EVEN fields) and YPO (scaling start phase for ODD fields) have to be set according to the equations below: (see Fig.14).

- YACL = INT{(1 - S)/S} accumulation sequence length; i.e. number of lines per sequence, that are not part of overlay region of neighbouring sequences (optimum: 1 line overlapped)
- YSCI = INT{1024 × (1 – S)} scaling increments.
- YP x = INT(YSCI/16) scaling start phase (fix; modified in LPI mode only).

In order to improve the vertical scaling performance, the accumulated lines can be weighted. Accordingly, the resulting amplitude gain of the scaled output signals has to be renormalized. In the given example (see Fig.14), using the optimal weighting, the gain of a sequence results in 1 + 2 + 2 + 1 = 6. Renormalization (factor $\frac{1}{6}$) can be achieved in two ways:

- Gain reduction using BCS control (brightness, contrast and saturation) down to $\frac{4}{6}$ and selecting factor $\frac{1}{4}$ for DCGY2 to DCGY0, which may result in less visible contrast
- Gain emphasizing using BCS control up to $\frac{8}{6}$ and selecting factor $\frac{1}{8}$ for DCGY2 to DCGY0.

Alternatively the gain can be renormalized only with DCGY2 to DCGY0 (factor $\frac{1}{8}$), if the weighting is changed to 2 + 2 + 2 + 2.

Table 55 illustrates examples for Scaler Register settings, dependent on a given scale ratio.

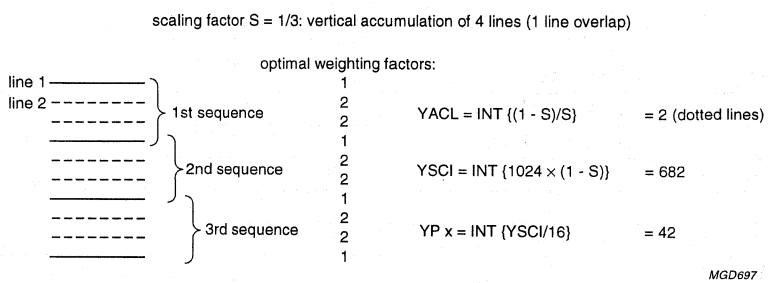


Fig.14 Example: Vertical Accumulation.

Table 55 Vertical scaling and normalization

VERTICAL SCALE RATIO	YACL	COEFFICIENT SEQUENCE (EXAMPLE)	CYA; CYB	WEIGHT SUM	DCGY	BCS (CONTR. I SAT.) = X/Y × 64
1 to 1/2	0	1-1	01, 00	2	0	1
1/2 to 1/3	1	1-1-1	03, 00	3	0	2/3
		1-2-1	01, 02	4	1	1
1/3 to 1/4	2	1-1-1-1	03, 00	4	1	1
1/4 to 1/5	3	1-1-1-1-1	07, 00	5	1	4/5
		1-2-2-2-1	01, 06	8	2	1
1/5 to 1/6	4	111 111	07, 00	6	1	4/6
		121 121	05, 02	8	2	1
		112 211	03, 04	8	2	1
1/6 to 1/7	5	111 1 111	0F, 00	7	2	8/7
		111 2 111	07, 08	8	2	1
1/7 to 1/8	6	1111 1111	0F, 00	8	2	1
1/8 to 1/9	7	1111 1 1111	1F, 00	9	2	8/9
		1222 2 2221	01, 1E	16	3	1
1/9 to 1/10	8	1111 1 1 1111	1F, 00	10	3	8/10
		2121 2 2 1212	09, 15	16	3	1
		1122 2 2 2211	03, 1C	16	3	1
1/10 to 1/11	9	1111 1 1 1 1111	3F, 00	11	2	8/11
		1212 1 2 1 2121	15, 2A	16	3	1
		1112 2 2 2 2111	07, 38	16	3	1
1/11 to 1/12	10	1111 11 11 1111	3F, 00	12	2	12/16
		1211 21 12 1121	2D, 12	16	3	1
		1111 22 22 1111	0F, 30	16	3	1
1/23 to 1/24	22	1111 2222 1111 1111 2222 1111	0F, F0	32	4	1
		1121 1212 1121 1211 2121 1211	B5, 4A	32	4	1

8.9.2.6 LPI mode (scaling factor range 1 to ½; I²C bit YACM = 0)

To preserve the signal quality for slight vertical downscales (scaling factors 1 to ½) Linear Phase Interpolation (LPI) between consecutive lines is implemented to generate geometrical correct vertical output lines. Therefore, the new geometric position between lines N and N + 1 is calculated.

A new output line is calculated by weighting the samples p of lines N and N + 1 with the normalized distance to the new calculated position:

N → Delta = 1 → N + 1

new line M

alpha → I ← (1 – alpha)

p(M) = alpha × p(N) + (1 – alpha) × p(N + 1).

For a given scaling factor S, the Scaler Register bits YSCI (scaling increment) and YP (scaling start phase) have to be set according to the equations below:

- YSCI = INT [1 024 × (NIL/NOL – 1)] scaling increment
- YPx = INT [$^{YSCI}/_{16}$] scaling start phase (recommended value).

The vertical start phase offset is defined by $^{YPx}/_{64}$ (YPx = 0 to 64):

- YPx = 0: offset = 0 geometrical position of 1st line out = 1st line in
- YPx = 64: offset = $^{64}/_{64}$ = 1 geometrical position of 1st line out = 2nd line in.

Finally 3 special modes are to be emphasized:

1. **Bypass** (YSCI = 0, YPx = 64); (each line out is equivalent to corresponding line in)
2. **Lowpass** (YSCI = 0, YPx < 64); [e.g. YPx = 32: average value of 2 lines (1 + z^{-h} Filter)]

   In both modes the first input line is fed to the output (without processing), so that the number of output lines = number of input lines.
3. For processing of **interlaced input** signals the LPI mode must be used (ACCU mode would cause 'line pairing' problems). The scaling start phase for odd and even field have to be set to:

   $YP_{even} = {}^{3}/_{2} \times YP_{odd}$ (line 1 = odd).

8.9.2.7 Flip option (Mirror = 1)

For both vertical scaling modes there is a flip option 'mirroring' available for input lines with a maximum of 384 pixels. In case full screen pictures (e.g. 768 × 576) are to be flipped, they have first to be downscaled to 384 pixel/line in the horizontal prescaling unit, and after vertical processing (flipping) may be rezoomed to the original 768 pixels/line in the following VPD.

It should be noted that when using the flip option, the last input line can not be displayed at the output.

8.9.3 Horizontal phase scaling

In the phase correct Horizontal phase scaling the pixels are calculated for the geometrical correct, orthogonal output pattern, down to $1/4$ of the prescaled pattern. In addition, a horizontal zooming feature is supported. The maximum zooming factor is at least 2, even more dependent on input pattern and prescaling settings.

The Phase Scaling consists of a filter and arithmetic structure which is able to generate a phase correct new pixel value, almost without phase or amplitude artefacts.

The required sample phase information is generated by a sample phase calculator, with an accuracy of $1/64$ of the pixel distance.

The up/down scaling with this circuitry is controlled by the Scaler Register parameters XSCI and XP. As the fine scaling is restricted to downscales $>1/4$ of the fine scalers input pixel count, XSCI is also a function of the prescaling parameter XPSC.

With NIP = number of input pixel/line (at DD1 input) and NOP = number of desired output pixels/line, XSCI is defined to:

$$XSCI = INT[(NIP/NOP) \times 1024/(XPSC + 1)]$$

The maximum value of XSCI = 4095. Zooming is performed for XSCI values less than 1024. The number of disqualified clock cycles between consecutive pixel qualifiers (at the fine scalers input) defines the maximum possible zoom factor. This means, zooming may also be a function of XPSC. It should be noted that if the zooming >factor 2, some artefacts may occur at the end of the zoomed line.

8.9.4 CSM (Colour Space Matrix), Dither, γ-Correction

The scaled YUV output data are converted after Interpolation into RGB data according to CCIR 601 recommendations. Data are bypassed in all YUV formats or monochrome modes.

The matrix equations considering the digital quantization are:

$R = Y + 1.375V$

$G = Y - 0.703125V - 0.34375U$

$B = Y + 1.734375U.$

For error diffusion a dither algorithm is implemented. ROM tables are implemented at the matrix output to provide anti-gamma correction of the RGB data. A curve for a gamma of 1.4 is implemented. The tables can be used to compensate gamma correction for linear data representation of RGB output data.

The chroma signal keyer generates an alpha signal used in several RGB formats. Therefore, the processed UV data amplitudes are compared with thresholds. A logic 1 is generated if the amplitude is inside the specified amplitude range, otherwise a logic 0 is generated. Keying can be switched off by setting the lower limit higher than the upper limit.

8.10 Binary Ratio Scaler (BRS)

8.10.1 General description

The BRS is a second scaler in the SAA7146. The BRS is assumed to support different encoder applications whilst the HPS is processing video data.The BRS does not support clipping.

The mainstream application for the BRS is to read data via PCI, e.g. a QCIF-formatted video data to proceed with horizontal and vertical up-scaling to CIF-format and place it at the encoder's disposal (normal playback mode).

To support CCIR encoder and square pixel encoder, an active video window as input for the BRS can be defined. It will prevent black pixels being displayed at the end of the line or at the bottom of the field.

The BRS supports only the YUV 4 : 2 : 2 video data format (see Section 8.11.2). The used DD1 I/O data format is 8-bit. The BRS uses video DMA Channel 3 (FIFO 3) which is only available, if the HPS is not in planar mode or writes back clip information.

Vertical up-scaling is supported by means of repeated reading of same line via PCI. Vertical down-scaling is done by line dropping.

Horizontal down-scaling is performed by an accumulating FIR filter. The down-scaling is available for the inbound mode and the up-scaling is available for the outbound mode.

- Vertical ratios: 4, 2, 1, $\frac{1}{2}$ and $\frac{1}{4}$; select with BRS_V
- Horizontal ratios: 8, 4, 2, 1, $\frac{1}{2}$, $\frac{1}{4}$ and $\frac{1}{8}$; select with BRS_H.

If the data is sent from DD1 to PCI, the processing window for the BRS scaling unit is defined in the acquisition control (see Section 8.8.6).

The PCI source data is defined by the base address (BaseODD3 and BaseEVEN3), the distance between the start addresses of two consecutive lines of a field (Pitch3), the Number of lines per field of the source frame (NumLines3) and the Number of Bytes per line of the source frame (NumByte3). The programmer must provide correct scaling settings to fulfil the target window requirements.

8.10.2 Playback mode

The SAA7146 offers three different modes to support the playback mode for various systems. The Binary Ratio Scaler (BRS) inputs data from FIFO 3, therefore the DMA3 is in master read operation. The scaling result is passed to the DD1 output.

8.10.2.1 Field Memory mode

In field memory mode the SAA7146 takes a vertical sync signal as timing reference signal. A reset signal for a field memory and a PXQ as write enable are generated within the circuit and sent to Port A or Port B. In this mode the pixel clock depends on the PCI-load. The pixels are provided to the DD1 port with maximum ½LLC (CCIR 656), the picture rate is restricted by the vertical timing reference. Since the transfer works without losing any data, the pixel clock can varied, so an external field memory is needed at the DD1-interface. The SAA7146 writes its data continuously to this memory. The video window depends on the selected window in the system memory, frame buffer (Numlines, Numbytes, pitch and base address) and the selected scaling ratio.

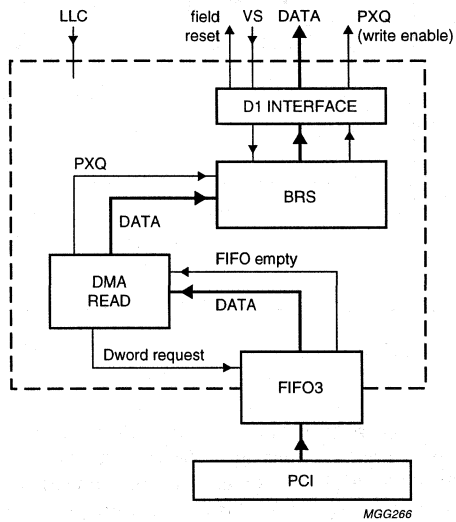


Fig.15 Sync- and data path for Field Memory mode.

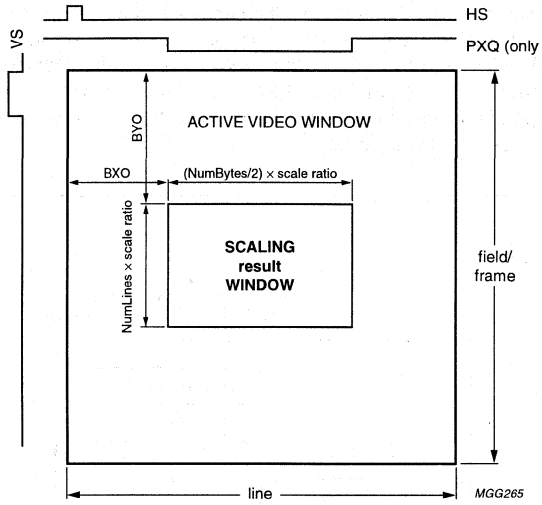


Fig.16 Reference signals for scaling window for Direct and Line Memory mode.

8.10.2.2 Direct mode

The timing reference signals (VS, HS, LLC and FID) are taken from Port A or Port B. The BRS has the duty to deliver pixel with pixel clock of ½LLC to the D1 port. To make sure, that there are no dropouts, a simple underflow handling is performed by the DMA read module. If the PCI load is great and a FIFO underflow occurs, the DMA read module use a grey value (10H for Luminance, 80H for chrominance) or the last pixel as a substitute. The FIFO control counts the failed requests and removes the late values from the FIFO hoping to catch up for lost time to the end of a line. At the end of a line given by an external source the DMA tries to read the data of the new line. This time is defined by the horizontal offset (BXO) of the input acquisition.

The PXQ can be used as KEY signal for the On Screen Display data to support panning, if the video window has no full screen format.

8.10.2.3 Line Memory mode

The timing reference signals (VS, HS, LLC and FID) are taken from Port A or Port B. The access time be extended by using a line memory at the D1 interface. If a FIFO underflow occurs during the active processing, the DMA read unit waits for the next valid data hoping to catch up for the lost time during the horizontal blanking interval. The timing is re-triggered by the H-sync and V-sync. Therefore it is possible, depending on the PCI load, that a line or a part of a line is multiple read from the line memory. The PXQ is used as a write enable signal.

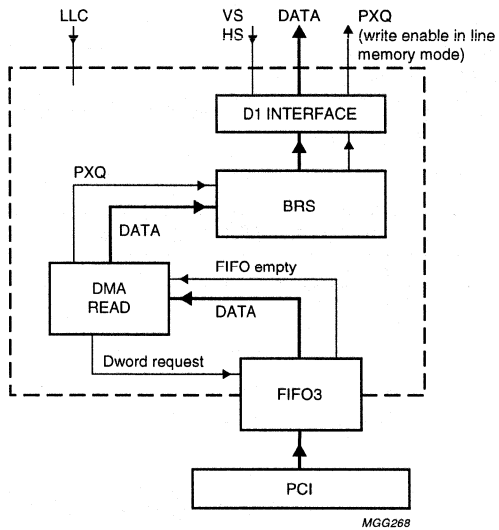


Fig.17 Sync- and data path for Direct and Line Memory mode.

8.10.3 VBI DATA INTERFACE

The SAA7146 transports VBI data (data during the Vertical Blanking Interval) or VBI test signals between real time world and the computer system. The data can assume YUV format, luminance Y only, undecoded digital CVBS on luminance channel, or a single bit stream of sliced data. 1MSB or 2MSB of Y is utilized to carry 'data bit', PXQ pixel qualifier is used as 'data clock'.

VBI data region must defined as 'data pass through' range of lines. VBI data lives in the same data path as the BRS without processing. The VBI data channel takes its data and sync signals from the same input as programmed for the BRS.

8.11 Video data formats on PCI bus

The endian-ness is supported in the way that Dword or word swapping is possible. The data formats using 32 bits per pixel require all bytes swapped in one Dword, whereas the data formats using 16 bits per pixel require all bytes swapped in both words of a Dword.

8.11.1 SCALER OUTPUT FORMATS (HPS)

8.11.1.1 RGB

RGB each defined as 'full range', all bits = 0 for black and all bits = 1 for white. All RGB formats are composed formats, and use video FIFO 1 and video DMA Channel 1.

- **αRGB-32:** αRGB each 1 byte, α can be the colour key bit in all 8 bits, or read via FIFO 2 (see 8-bit format alpha-8), uses one entire Dword per sample (see Table 56).

Table 56 αRGB-32 format

PACKING WITHIN 32-BIT Dword			
31 to 24	23 to 16	15 to 8	7 to 0
α/–	R	G	B
α/–	V	Y	U

- **RGB-24-packed:** RGB each 1 byte, packed cyclic into Dwords, uses 0.75 Dwords per sample, i.e. 3 Dwords per 4 samples, byte phase of first sample each line defined by 2 LSBs of DMA base (see Table 57).

Table 57 RGB-24-packed format

BUS CYCLE	PACKING WITHIN 32-BIT Dword			
	31 TO 24	23 TO 16	15 TO 8	7 TO 0
1	B_1	R_0	G_0	B_0
2	G_2	B_2	R_1	G_1
3	R_3	G_3	B_3	R_2

The following formats use two pixels per Dword and derive RGB from RGB-24 by truncation, or by error diffusion dither. The byte phase of the first sample each line is defined by LSB + 1 of DMA base. 'α' will be the colour key.

- RGB-16 (5-6-5): Red has 5 bits, Green has 6 bits, Blue has 5 bits
- RGB-15 (α-5-5-5): α-bit, Red has 5 bits, Green has 5 bits, Blue has 5 bits
- RGB-15 (5-5-α-5): Red has 5 bits, Green has 5 bits, α bit, Blue has 5 bits.

Table 58 RGB-16 formats Dword

PACKING WITHIN 32-BIT Dword	
31 to 16	15 to 0
$pixel_1$	$pixel_0$

8.11.1.2 YUV

All YUV formats based on CCIR coding:

Luminance Y in straight binary:

Black: Y = 16 of 256 linear coding

White: Y = 235 of 256 linear coding.

Colour difference signals UV in offset binary:

No colour: U = V = 128 of 256 steps

Full colour: U = V = 128 ±112 steps.

The following formats use video FIFO 1 and DMA Channel 1 and are packed formats.

- YUV 4 : 2 : 2: U and V sampled co-sided with first Y sample (of 2 samples in-line). Byte phase of the first sample each line is defined by LSB + 1 of DMA base (see Table 59).

Table 59 YUV 4 : 2 : 2 format

PACKING WITHIN 32-BIT Dword			
31 to 24	23 to 16	15 to 8	7 to 0
Y_1	V_0	Y_0	U_0

- YUV 4 : 1 : 1: U and V sampled co-sided with first Y sample, (of 4 samples in-line), 8 samples go in 3 Dwords (see Table 60).

Table 60 YUV 4 : 1 : 1 format

BUS CYCLE	PACKING WITHIN 32-BIT Dword			
	31 TO 24	23 TO 16	15 TO 8	7 TO 0
1	Y_1	V_0	Y_0	U_0
2	Y_3	V_4	Y_2	U_4
3	Y_7	V_6	Y_5	Y_4

The following formats are planar YUV formats and use the three video FIFOs 1, 2, and 3, and three video DMA Channels 1, 2 and 3. The byte phase of the first sample each line is defined by the 2 LSBs of every DMA base.

- YUV 4 : 4 : 4; U and V sampled with every Y sample
- YUV 4 : 2 : 2; U and V sampled co-sided with first Y sample (of 2 samples in-line)
- YUV 4 : 2 : 0; MPEG U and V sampled at upper left sample of 4 sample in square (2 × 2)
- YUV-9 video; U and V sampled at selected sample of 16 samples in-square (4 × 4)
- YUV1; YUYV, YUYV...
- YUV2; YYUU, YYVV...

8.11.1.3 8-bit formats

- Y8G; Only Y, or inverted Y.
- alpha-8; 8-bit alpha information, to be master-read through FIFO 2 and merged into RGB-24 with alpha.

There are two pseudo CLUT formats, which derives its bits from RGB-24 or YUV-24 by truncation, or by error diffusion dither. The byte phase of the first sample each field is defined by 2 LSBs of DMA base.

- RGB-8 (3 : 3 : 2); Red has 3 bits, Green has 3 bits, Blue has 2 bits.
- YUV8 (4 : 2 : 2); Y has 4 bits, U has 2 bits, V has 2 bits. Y = 0 doesn't exist, to handle 16-bit colour formats for pseudo CLUT. After dithering, $Y_{min} = 1$.

All 8-bit formats are packed formats, 4 samples go into one Dword. The byte phase of the first sample each line is defined by the 2 LSBs of the DMA base. All except alpha-8 use FIFO 1.

Table 61 8-bit formats

PACKING WITHIN 32-BIT Dword			
31 to 24	23 to 16	15 to 8	7 to 0
$pixel_3$	$pixel_2$	$pixel_1$	$pixel_0$

8.11.2 BINARY RATIO SCALER OUTPUT-FORMATS

All YUV formats based on CCIR coding:

Luminance Y in straight binary:

Black: Y = 16 of 256 linear coding

White: Y = 235 of 256 linear coding.

Colour difference signals UV in offset binary:

No colour: U = V = 128 of 256 steps

Full colour: U = V = 128 ±112 steps.

The following formats use video FIFO 1 and DMA Channel 1 and are packed formats.

- YUV 4 : 2 : 2 U and V sampled co-sided with first Y sample (of 2 samples in-line).

  Byte phase of the first sample each line is defined by LSB + 1 of DMA base.

Table 62 YUV 4 : 2 : 2 formats

PACKING WITHIN 32-BIT Dword			
31 to 24	23 to 16	15 to 8	7 to 0
Y_1	V_0	Y_0	U_0

8.11.2.1 VBI-data formats

- Y8; uses only the Y portion of the data stream and packs four bytes in one Dword
- YUV 4 : 2 : 2; packs two pixel into one Dword, the order is $Y_1V_0Y_0U_0$
- 1-bit format; the Y1 format is a 1-bit format which packs 32 times the most significant bit of luminance (Y) into one Dword, the first bit is bit 31 of the Dword
- 2-bit format; the Y2 format is a 2-bit format which packs 16 times the two most significant bits of luminance (Y) into one Dword, the first bit is bit 31 of the Dword.

8.12 Scaler Register

8.12.1 Initial setting of Dual D1 Interface

The initial settings of the Dual D1 interface contains all control bits of the Scaler part, which do not change during a cyclic processing of the video path. These control bits must be initialized at the beginning of the processing. The different upload conditions of the video path depends on these control bits. To change these bits during the active processing can be cause an unintentionally UPLOAD.

Table 63 Initial Setting of Dual D1 Interface

OFFSET (HEX)	NAME	BIT	TYPE	DESCRIPTION
50	LLC_a	31	RW	Line Locked Clock Control for D1_a: 0: LLC_a set to input 1: LLC_a set to output, taken from LLC_b
	SIO_a	30 to 29	RW	Synchronization port_a configuration: 00: HS_a and VS_a are input (i.e. 3-state). 01: HS_a is output, HGT of HPS; VS_a is output, VGT of HPS. 10: HS_a is output, RESET signal for a field memory VS_a is input, vertical sync signal for BRS this setting is needed for the field memory mode. 11: HS_a is output, HGT of BRS; VS_a is output, VGT of BRS.
	PVO_a	28	RW	Polarity of VS_a, if VS output: 0: direct from HPS or BRS, see SIO_a 1: inverted
	PHO_a	27	RW	Polarity of HS_a, if HS output is select by SIO_a: 0: direct from HPS or BRS, see SIO_a 1: inverted

OFFSET (HEX)	NAME	BIT	TYPE	DESCRIPTION
50	SYNC_a	26 to 24	RW	Sync edge selection and field detection mode internal sync signals SyncA(Ha, Va, Fa) if: HS, VS are input: Ha/Va/Fa derived from pins HS, VS are output: HS/VS as select by SIO_a. 000: Ha at rising edge of HS; Va at rising edge of VS; Fa = HS × VS-rising, directly 001: Ha at rising edge of HS; Va at falling edge of VS; Fa = Hs × VS-falling, directly 010: Ha at rising edge of HS; Va at rising edge of VS; Fa = HS × VS-falling, forced toggle 011: Ha at rising edge of HS; Va at falling edge of VS; Fa = HS × VS-falling, forced toggle 100: Ha at rising edge of HS; Va at rising edge of VS; Fa = free toggle 101: Ha at rising edge of HS; Va at falling edge of VS; Fa = free toggle 110: Ha at rising edge of HS; Va at rising and falling edge of Frame Sync at the VS pin; Fa = direct FS 111: Ha, Va, Fa; derived from SAV and EAV decoded from the data-stream at D1_a port. Not used if the MSB of HPSdatasel in Table 67 is set to 1.
	FIDESA	23 and 22	RW	Field identification port_A edge select (ODD is defined by FID = 1, EVEN is defined by FID = 0) 00: no interrupt condition 01: rising edge is interrupt condition 10: falling edge is interrupt condition 11: both edges are interrupt condition
	–	21 to 16	–	reserved
	LLC_b	15	RW	Line Locked Clock Control for D1_b: 0: LLC_b set to input 1: LLC_b set to output, taken from LLC_a
	SIO_b	14 and 13	RW	Synchronization port_b configuration: 00: HS_b and VS_b are input (i.e. 3-state) 01: HS_b is output, HGT of HPS; VS_b is output, VGT of HPS 10: HS_b is output, RESET signal for a field memory; VS_b is input, vertical sync signal for BRS this setting is needed for the field memory mode. 11: HS_b is output, HGT of BRS; VS_b is output, VGT of BRS

OFFSET (HEX)	NAME	BIT	TYPE	DESCRIPTION
50	PVO_b	12	RW	Polarity of VS_b, if VS output: 0: direct from HPS or BRS, see SIO_b 1: inverted
	PHO_b	11	RW	Polarity of HS_b, if HS output is select by SIO_b: 0: direct from HPS or BRS, see SIO_b 1: inverted
	SYNC_b	10 to 8	RW	Sync edge selection and field detection mode internal sync signals SyncA(Hb, Vb, Fb) if: HS, VS are input: Hb/Vb/Fb derived from pins HS, VS are output: HS/VS as select by SIO_b 000: Hb at rising edge of HS; Vb at rising edge of VS; Fb = HS × VS-rising, directly 001: Hb at rising edge of HS; Vb at falling edge of VS; Fb = Hs × VS-falling, directly 010: Hb at rising edge of HS; Vb at rising edge of VS; Fb = HS × VS-falling, forced toggle 011: Hb at rising edge of HS; Vb at falling edge of VS; Fb = HS × VS-falling, forced toggle 100: Hb at rising edge of HS; Vb at rising edge of VS 111: Hb, Vb, Fb derived from SAV and EAV decoded from the data-stream at D1_b port. Not used if the MSB of HPSdatasel in Table 67 is set to 1.
	FIDESB	7 and 6	RW	Field identification port_B edge select (ODD is defined by FID = 1, EVEN is defined by FID = 0) 00: no interrupt condition 01: rising edge is interrupt condition 10: falling edge is interrupt condition 11: both edges are interrupt condition
	–	5 to 0	–	reserved

8.12.2 VIDEO DATA STREAM HANDLING AT PORT D1_A

Table 64 Video data stream handling at port D1_a

OFFSET (HEX)	NAME	BIT	TYPE	DESCRIPTION
54	VID_a	31 and 30	RW	Video data port_a and PXQ_a select (PXQ goes always with data): 00: input, i.e. 3-state 01: reserved 10: output data stream is Y8C from BRS 11: output data stream is Y8C from HPS
	Y8C_a	29	RW	Y8C codes, if output Y8C only: 0: no SAV and EAV data in the Video data output-stream 1: with SAV and EAV
	–	28 and 27	–	reserved
	PFid_a	26	RW	Polarity change of the Field detection result at port_a: 0: as detected in the Field detection 1: inverted
	–	25 to 16	–	reserved

8.12.3 VIDEO DATA STREAM HANDLING AT PORT D1_B

Table 65 Video data stream handling at port D1_b

OFFSET (HEX)	NAME	BIT	TYPE	DESCRIPTION
54	VID_b	15 and 14	RW	Video data port_b and PXQ_b select (PXQ goes always with data): 00: input, i.e. 3-state 01: reserved 10: output data stream is Y8C from BRS 11: output data stream is Y8C from HPS
	Y8C_b	13	RW	Y8C codes: 0: no SAV and EAV data in the Video data output-stream: 1: with SAV and EAV
	–	12 and 11	–	reserved
	PFid_b	10	RW	Polarity change of the Field detection result at port_b: 0: as detected in the Field detection 1: inverted
	–	9 to 0	–	reserved

8.12.4 BRS Programming Register

The BRS programming has in principle three modes:

- **Inbound**, and **down** scaling:
  The Binary Ratio Scaler input multiplexer selects data from Dual D1 real time video interface, Port A or B, and 'normally' writes the result through FIFO 3 and via DMA3 to PCI, if DMA3 is enabled in master write mode, and not used for other purposes. Syncs including Field ID, are taken from Port A or B. (FID defines which base address is used in DMA3).
- **Outbound**, and **up** scaling in direct and line memory mode:
  The Binary Ratio Scaler inputs data from FIFO and DMA3 is in master read operation. The scaling result can be selected by the DD1 port output multiplexers. The timing reference signals (VS, HS, LLC, FID) are taken from port A or B.
- **Outbound**, and **up** scaling in **field memory** mode:
  The Binary Ratio Scaler input data from FIFO 3, therefore the DMA3 is in master read operation. The scaling result can be selected by the DD1 port output multiplexers. The vertical sync-signal is taken from the VS_a or VS_b port as timing reference signal. At the HS_a or HS_b port the SAA7146 generates a reset signal for each field. The PXQ is an output signal which is connected to the write enable port of the memory. The field detection must be set to 'free toggle' mode, in ground of the missing horizontal sync signal.

Table 66 BRS Control Register

OFFSET (HEX)	NAME	BIT	TYPE	DESCRIPTION	
				INBOUND	OUTBOUND
58	BRSdatasel and MODE	31 and 30	RW	Source select for BRS video data:	
				00: video data stream from A 01: video data stream from B 10: reserved	11: read from DMA_3/FIFO 3; in read mode the base address of DMA3 must be Dword
	BRSsyncsel	29	RW	Source select for BRS sync-signals:	
				0: take Ha, Va, Fa, LLC_a as select in the 'Initial Setting of DUAL D1 Interface'; see Table 63. 1: take Hb, Vb, Fb, LLC_b as select in the 'Initial Setting of DUAL D1 Interface'; see Table 63.	In direct and line memory mode the same setting as in the inbound mode is select. In field memory mode the horizontal sync-port must set to output to get the a field RESET signal for a field memory.
	BYO	28 to 19	RW	vertical offset, count in lines, after selected vertical sync-edge, until data is captured from DD1	BYO defines a vertical offset, count in lines, after selected vertical sync-edge, until data is read from the FIFO. For field memory mode BYO must be 000H. The video window is selected by 'NumLines', 'NumBytes', 'pitch' and 'base-address'.

<table>
<tr><th rowspan="2">OFFSET (HEX)</th><th rowspan="2">NAME</th><th rowspan="2">BIT</th><th rowspan="2">TYPE</th><th colspan="2">DESCRIPTION</th></tr>
<tr><th>INBOUND</th><th>OUTBOUND</th></tr>
<tr><td rowspan="3">58</td><td>BRS_V</td><td>18 and 17</td><td>RW</td><td>vertical down-scaling:
00: write every line to DMA3
01: write every 2nd line only
10: reserved
11: write every 4th line only</td><td>vertical up-scaling:
00: regular read
01: read every line twice
10: reserved
11: read every line 4 times</td></tr>
<tr><td>BXO</td><td>16 to 7</td><td>RW</td><td>horizontal offset, count in qualified LLC cycles, after selected horizontal sync-edge, till data is captured from DD1</td><td>BXO defines a horizontal offset, count in LLC cycles, after selected horizontal sync-edge, till data is read from the FIFO.
In field memory mode the following offsets depending on the horizontal scaling ratio must select to guarantee the correct outrun behaviour of the scaler.
<table><tr><td>Ratio:</td><td>Offset:</td></tr><tr><td>1</td><td>00H</td></tr><tr><td>2</td><td>0CH</td></tr><tr><td>4</td><td>16H</td></tr><tr><td>8</td><td>2EH</td></tr></table>The video window is select by ‘NumLines’, ‘NumBytes’, ‘pitch’ and ‘base-address’.</td></tr>
<tr><td>BRS_H</td><td>6 to 4</td><td>RW</td><td>horizontal down-scaling (see Section 8.10.1)
000: every pixel is captured
001: every 2nd pixel is captured
010: reserved
011: every 4th pixel is captured
100: reserved
101: reserved
110: reserved
111: every 8th pixel is captured</td><td>horizontal up-scaling:
000: provide every sample once
001: provide every sample twice
010: reserved
011: provide every sample 4 times
100: reserved
101: reserved
110: reserved
111: provide every sample 8 times</td></tr>
</table>

OFFSET (HEX)	NAME	BIT	TYPE	DESCRIPTION	
				INBOUND	OUTBOUND
58	Read mode	3 and 2	RW	reserved	00: line memory mode 01: field memory mode 10: direct mode with pixel repetition for not qualified bytes. 11: direct with grey pixel (10H for luminance and 80H for chrominance values) for not qualified bytes.
	PCI format	1 and 0	RW	output format, PCI-side: 00: YUV16, two bytes/pixel 01: Y8, only Luminance 10: Y2, 2MSBs of Y only 11: Y1, 1MSB of Y only	input format PCI-side: 00: YUV16, 4 : 2 : 2 01: reserved 10: reserved 11: reserved

8.12.5 HPS Programming register

Table 67 HPS control

OFFSET (HEX)	NAME	BIT	TYPE	DESCRIPTION
5C	HPSdatasel	31 and 30	RW	Source select for HPS video data: 00: input video stream for HPS is taken from port_a 01 input video stream for HPS is taken from port_b 10: Y-byte from port_b, C-byte from port_a (CREF must provide at Port A) 11: Y-byte from port_a, C-byte from port_b (CREF must provide at Port B)
	Mirror	29	RW	Left-Right Flip (mirroring), e.g. for vanity picture: 0: regular processing 1: Left-Right Flip, accessible only if XT (number of pixel after horizontal pre-scaling) is less than 384 pixels
	HPSsyncsel	28	RW	Source select for HPS sync-signals: 0: take Ha, Va, Fa, LLC_a as selected in Table 63 1: take Hb, Vb, Fb, LLC_b, as selected in Table 63
	–	27 to 24	RW	reserved
	HYO	23 to 12	RW	vertical offset (start line) of HPS operation, counted in horizontal source/input events, after selected vertical sync-edge
	–	11 to 0	RW	reserved

8.12.6 VERTICAL AND HORIZONTAL SCALING

Table 68 HPS, Vertical-scale

OFFSET (HEX)	NAME	BIT	TYPE	DESCRIPTION
60	YACM	31	RW	Y (vertical) scaler accumulation (calculation) mode of vertical arithmetic: 0: arithmetic operates as a linear phase interpolation (LPI) 1: arithmetic operates as accumulating FIR filter in vertical direction
	YSCI	30 to 21	RW	Y scaler Increment for vertical down scaling: YYSCI = INT[1 024 × (NIL/NIL – 1) for YACM = 0 → LPI YSCI = INT[1 024 × (1 – NOL/NIL)] for YACM = 1 → accumulation mode N_{IL} = number of qualified scaler input lines N_{OL} = number of output lines
	YACL	20 to 15	RW	Accumulation sequence Length of the Y (vertical) processing. Defines vertical accumulation sequence length of input lines. If accumulation FIR filter mode is selected YACM, YACL has to fit to the vertical scaling factor (defined by YSCI).
	YPO	14 to 8	RW	Vertical Start Phase for vertical scaling of the ODD field YPO = PHOL × 128 (PHOL represents a phase offset with values between '0' and '1', where the '1' represents a distance between two consecutive lines of the input pattern)
	YPE	7 to 1	RW	Vertical Start Phase for vertical scaling of the EVEN field YPE = PHOL × 128 (PHOL represents a phase offset with values between '0' and '1', where the '1' represents a distance between two consecutive lines of the input pattern)
	–	0	RW	reserved

Table 69 HPS, Vertical-scale and gain

OFFSET (HEX)	NAME	BIT	TYPE	DESCRIPTION
64	PFY	31 to 28	RW	Prefilter selection for luminance component Y: $H(z) = H1(z) \times H2(z) \times H3(z)$ $H1, H3 = 1 + z^{-1}$ $H2 = 1 + A \times z^{-1} + z^{-2}$ see Table 70.
	PFUV	27 to 24	RW	Prefilter selection for colour difference signals UV: $H(z) = H1(z) \times H2(z) \times H3(z)$ $H1 = 1 + z^{-1}$ $H2 = 1 + A \times z^{-1} + z^{-2}$ $H3 = 1 + z^{-2}$ see Table 71.
	–	23 to 19	–	reserved
	DCGY	18 to 16	RW	DC Gain control of Y scaler: Dependent on active coefficients and the sequence length, the amplitude gain has to be renormalized. Gain factor = $2^{(DCGY + 1)}$; see Table 72. The resulting factor is a function of CYi and DCGY. The resulting factor weight = 0 for (CYAi = CYBi = 0) or (CYAi = CYBi = 1) or (DCGY >5) otherwise weight = weighting factor/gain factor; see Table 73.
	CYA	15 to 8	RW	Coefficient select for Y (vertical) processing in Accumulation mode: For improvement of vertical filtering the accumulated lines can be weighted. Weighting factor = $2^{(2 \times CYBi + CYAi - 1)}$. See Table 74.
	CYB	7 to 0	RW	

Table 70 Prefilter selection for luminance component Y

PFY1	PFY0	PFY1	PFY0	H1	H2	H3	A
X	X	0	0	bypass	bypass	bypass	X
X	X	0	1	active	bypass	bypass	X
X	X	1	0	active	bypass	active	X
0	0	1	1	active	active	active	2
0	1	1	1	active	bypass	bypass	$^{15}/_{16}$
1	0	1	1	active	bypass	active	$^{7}/_{8}$
1	1	1	1	active	active	active	$^{3}/_{4}$

Table 71 Prefilter selection for colour difference signals UV

PFY1	PFY0	PFY1	PFY0	H1	H2	H3	A
X	X	0	0	bypass	bypass	bypass	X
X	X	0	1	active	bypass	bypass	X
X	X	1	0	active	bypass	active	X
0	0	1	1	active	active	active	2
0	1	1	1	active	bypass	bypass	$^{15}/_{16}$
1	0	1	1	active	bypass	active	$^{7}/_{8}$
1	1	1	1	active	active	active	$^{3}/_{4}$

Table 72 DC gain control of Y scaler

DCGY2	DCGY1	DCGY0	DCGY	GAIN FACTOR
0	0	0	0	2
0	0	1	1	4
0	1	0	2	8
0	1	1	3	16
1	0	0	4	32
1	0	1	5	64
1	1	0	6	128
1	1	1	7	256

Table 73 Weighting and gain factor as a function of CYi and DCGY

CYi	DCGY							
	0	1	2	3	4	5	6	7
0	0	0	0	0	0	0	0	0
1	$^{1}/_{2}$	$^{1}/_{4}$	$^{1}/_{8}$	$^{1}/_{16}$	$^{1}/_{32}$	$^{1}/_{64}$	0	0
2	1	$^{1}/_{2}$	$^{1}/_{4}$	$^{1}/_{8}$	$^{1}/_{16}$	$^{1}/_{32}$	0	0
3	0	1	$^{1}/_{2}$	$^{1}/_{4}$	$^{1}/_{8}$	$^{1}/_{16}$	0	0

Table 74 Coefficient select for Y (vertical) processing in Accumulation mode

CYBi	CYAi	CYi	WEIGHTING FACTOR
0	0	0	0
0	1	1	1
1	0	2	2
1	1	3	4

Table 75 HPS, Horizontal Prescaler

OFFSET (HEX)	NAME	BIT	TYP.	DESCRIPTION
68	–	31 and 30	–	reserved
	DCGX	29 to 27	RW	DC Gain control of X prescaler (see Table 54). Dependent on the number of active coefficients '2' in the accumulation sequence and the sequence length, the output amplitude gain has to be set to; see Table 76.
	–	26 to 24	–	reserved
	XPSC	23 to 18	RW	Prescaling factor of the X PreSCaler. Defines accumulation sequence length and subsampling factor of the input data stream: XPSC = TRUNC NIP/NOP – 1). NOP = number of prescaler output pixel NIP = number of qualified scaler input pixel
	XACM	17	RW	X (horizontal) prescaler Accumulation mode of accumulating FIR: 0: accumulating operates overlapping 1: non overlapping accumulation (must be set to bypass the prescaler)
		16		reserved
	CXY	15 to 8	RW	Coefficient select for X prescaler (luminance component Y). For DC gain compensation of prescaler the accumulated pixels can be weighted by '1' or '2'. CXYi defines a sequence of 8 bits, which control the coefficients: CXYi = 0: pixel weighted by '1' CXYi = 1: pixel weighted by '2'
	CXUV	7 to 0	RW	Coefficient select for X prescaler (colour difference signals UV). For DC gain compensation of prescaler the accumulated pixels can be weighted by '1' or' 2'. CXUVi defines a sequence of 8 bits, which control the coefficients: CXUVi = 0: pixel weighted by '1' CXUVi = 1: pixel weighted by '2'

Table 76 Selection of output gain

DCGX2	DCGX1	DCGX0	GAIN
0	0	0	1
0	0	1	$\frac{1}{2}$
0	1	0	$\frac{1}{4}$
0	1	1	$\frac{1}{8}$
1	0	0	$\frac{1}{2}$
1	0	1	$\frac{1}{4}$
1	1	0	$\frac{1}{8}$
1	1	1	$\frac{1}{16}$

Table 77 HPS, Horizontal-fine-scale

OFFSET (HEX)	NAME	BIT	TYP.	DESCRIPTION
6C	XIM	31	RW	Horizontal interpolation mode: 0: normal mode, sample phase is calculated for every qualified sample 1: fixed phase, sample phase is fixed to the value set by XP
	XP	30 to 24	RW	Start phase for horizontal fine scaling XP = $PHO_P \times 128$ (PHOP represents a phase offset with values between '0' and '1', where the '1' represents a distance between two consecutive pixels of the input pattern).
	XSCI	23 to 12	RW	XScaler Increment for fine (phase correct) scaling in horizontal pixel phase arithmetic: XSCI = INT[(NIP/NOP) × 1024/(SPSC + 1)] NOP = number of output pixels NIP = number of qualified scaler input pixels
	HXO	11 to 0	RW	Horizontal offset (horizontal start) of input source for HPS, counted in qualified pixels with PXQ, after selected horizontal sync-edge.

8.12.7 BCS

Table 78 BCS control

OFFSET (HEX)	NAME	BIT	TYPE	DESCRIPTION
70	BRIG	31 to 24	RW	Luminance brightness control; see Table 79.
	CONT	23 to 16	RW	Luminance contrast control; see Table 80.
	–	15 to 8	–	reserved
	SATN	7 to 0	RW	Chrominance saturation control; see Table 81.

Table 79 Luminance brightness control

D7	D6	D5	D4	D3	D2	D1	D0	GAIN
1	1	1	1	1	1	1	1	255 (bright)
1	0	0	0	0	0	0	0	128 (CCIR level)
0	0	0	0	0	0	0	0	0 (dark)

Table 80 Luminance contrast control

D7	D6	D5	D4	D3	D2	D1	D0	GAIN
0	1	1	1	1	1	1	1	1.999 (max. contrast)
0	1	0	0	0	0	0	0	1 (CCIR level)
0	0	0	0	0	0	0	0	0 (luminance off)

Table 81 Chrominance saturation control

D7	D6	D5	D4	D3	D2	D1	D0	GAIN
0	1	1	1	1	1	1	1	1.999 (max. saturation)
0	1	0	0	0	0	0	0	1 (CCIR level)
0	0	0	0	0	0	0	0	0 (colour off)

8.12.8 CHROMA KEY

Table 82 Chroma Key range

OFFSET (HEX)	NAME	BIT	TYPE	DESCRIPTION
74	VL	31 to 24	RW	Set lower limit V for chroma-keying (8-bit; two's complement): 1000 0000: as maximum negative value = −128 signal level 0000 0000: limit = 0 0111 1111: as maximum positive value = +127 signal level
	VU	23 to 16	RW	Set upper limit V for chroma-keying (8-bit; two's complement): 1000 0000: as maximum negative value = −128 signal level 0000 0000: limit = 0 0111 1111: as maximum positive value = +127 signal level
	UL	15 to 8	RW	Set lower limit U for chroma-keying (8-bit; two's complement): 1000 0000: as maximum negative value = −128 signal level 0000 0000: limit = 0 0111 1111: as maximum positive value = +127 signal level
	UU	7 to 0	RW	Set upper limit U for chroma-keying (8-bit; two's complement): 1000 0000: as maximum negative value = −128 signal level 0000 0000: limit = 0 0111 1111: as maximum positive value = +127 signal level

Table 83 HPS Output and Formats

OFFSET (HEX)	NAME	BIT	TYPE	DESCRIPTION
78	matrix	31 and 30	RW	YUV to RGB conversion, gamma compensation 00: no YUV to RGB conversion 01: reserved 10: YUV to RGB conversion linear 11: YUV to RGB conversion with compensation of gamma-pre-correction
	–	29 and 28	–	reserved
	outformat	27 to 24	RW	output format, depends on matrix programming; see Table 84
		23 and 22	RW	Chroma Line select for INDEO-9
		21 and 20	RW	Chroma Pixel select for INDEO-9
	SHIFT	17	RW	0: normal mode, all bytes stay MSB aligned 1: shift mode, 'shift right' of all bytes, fill MSB position with 0, this mode has meaning only for output formats defined in bytes, undefined result in non-byte modes.
	DITHER	16	RW	Dither applies only to formats with reduced bit resolution, (#) that derived from higher bit resolution formats: 0: dither is applied by 'linear' one-dimensional error diffusion 1: dither algorithm is not applied, just truncation

Table 84 Output formats

CODE (HEX)	OUTPUT FORMAT	
0	YUV4 : 2 : 2, (16 = 8 – 8), composed	RGB16(5-6-5), composed, #
1	YUV4 : 4 : 4, composed, 'packed'	RGB24, composed, 'packed'
2	reserved	αRGB32 (8-8-8-8), composed
3	YUV4 : 1 : 1, composed	αRGB15 (1-5-5-5), composed, #
4	YUV2	RGαB15 (5-5-1-5), composed, #
5	reserved	reserved
6	Y8, monochrome	reserved
7	YUV8 (4-2-2), pseudo CLUT, #	RGB8 (3-3-2), pseudo CLUT, #
8	YUV4 : 4 : 4, de-composed	reserved
9	YUV4 : 2 : 2, de-composed	reserved
A	YUV4 : 2 : 0 (22:1:1) MPEG, de-composed.	reserved
B	YUV16 : 2 : 0 (42:1:1) INDEO-9, de-composed.	reserved
C	reserved	reserved
D	Y1	reserved
E	Y2	reserved
F	YUV1	reserved

Table 85 Clip control

OFFSET	NAME	BIT	TYPE	DESCRIPTION
78H	–	15 to 10	–	reserved
	ClipCK	9 and 8	RW	Clipping by chroma key CK, (or MSB of α-8) OR-ed with other Clip-list or Clip-bit-mask, if ClipMode is enabled 00: chroma key CK is not used for clipping, CK → α 01: chroma key CK is not used for clipping, inverted CK → α 10: clipping, based on chroma key CK bit 11: clipping, based on chroma key CK bit inverted.
	–	7	–	reserved, read only
	ClipMode	6 to 4	RW	Clipping based on DMA2 read information OR-ed with chroma key CK, if ClipCK is enabled: 000: no clipping based on DMA2 read, DMA2 can be used to write de-composed format U 001: no clipping based on DMA2 read; DMA2 reads 8-bit-α to substitute CK in α-formats 010: reserved 011: reserved 100: clipping, based on pixel clip list, rectangular overlays 101: clipping, based on pixel clip list, rectangular overlays, inverted 110: clipping, based on pixel clip bit mask 1-bit/pixel 111: clipping, based on pixel clip bit mask 1-bit/pixel, inverted.
	RecInterl	3	RW	Select interlaced mode for rectangular overlays: 0: normal mode 1: interlaced mode, this bit must be set if only one clip-list for both fields is available. This function assumes that the ODD field is always above the EVEN field.
	–	2	–	reserved
	ClipOut	1 and 0	RW	Use of DMA3, to report (write) key of clip information back: 00: no clip output, DMA3 can be used to write de-composed format V, or to serve BRS, read or write. 01: DMA3 writes chroma key information CK; 1-bit/pixel 10: DMA3 writes back (clip mask-CK); 1-bit /pixel 11: DMA3 writes applied pixel clipping back; 1-bit/pixel.

8.13 Scaler event description

The RPS is controlled by the PAUSE command on special events. This section describes the video events. On account of this video events a defined time for an upload is given. Table 86 shows also with which event it is useful to change the corresponding registers. For special applications it can be also useful to select other combinations. For this the termination of the UPLOAD must guarantee that the UPLOAD is done, before the processing restarts, e.g. with a new line or a new field. To avoid conflicts, e.g. change vertical settings during vertical processing, the MASKWRITE command can be used to change single bits within a Dword. Each video event can force only one upload at a time. This means that the video event is cleared by the circuit as described below. if the corresponding upload has occurred.

Table 86 UPLOAD handling for the Scaler Registers

REGISTER	OFFSET (HEX)	VIDEO EVENT	DESCRIPTION
Initial Setting of Dual D1 Interface	50	no VIDEO Event	The Initial Settings of the Dual D1 interface contains all control bits of the Scaler part which do not change during a cyclic processing of the video path. These control bits must be initialized at the start of the processing. The different upload conditions of the video path depends on these control bits. To change these bits during the cyclic processing can cause internal pulse signals which generate video events. These events may not fit into the sequence for the cyclic processing.
Video DATA stream handling at port D1_a	54	VBI_A	Vertical Blanking Indicator (VBI) at VS_a port. The VBI is a V-pulse which depends on the selected edge of the vertical blanking interval. The edge is defined by the SYNC_a bits. The selected mode depends on the accepted sync-signals. This register can be uploaded with this V-pulse.
Video DATA stream handling at port D1_b	54	VBI_B	Vertical Blanking Indicator (VBI) at VS_b port. The VBI is a V-pulse which depends on the selected edge of the vertical blanking interval. The edge is defined by the SIO_b bits. The selected mode depends on the accepted sync-signals. This register can be uploaded with this V-pulse.
BRS Control Register	58	BRS_DONE	Inactive BRS data path. In write mode the BRS data path is inactive, from the falling edge of VGT at the output of the BRS, which means that target line and target byte are reached, to the start of the next field (V-pulse which triggered the BRS acquisition). For the read mode this register contains only initial settings which can not change during cyclic processing.
HPS control	5C	HPS_DONE	Inactive HPS data path between two fields. The HPS data path is inactive from the falling edge of the VGT at the output of the HPS, indicating that target line and target byte are reached, to the start of the next field processing. V-pulse at the HPS acquisition input.
HPS Vertical-scale	60		
HPS Vertical-scale and gain	64		
Chroma Key range	74		
HPS Output and Formats	78		
Clip control	78		
HPS, Horizontal-pre-scale	68	HPS_LINE_DONE	Inactive HPS data path between two lines The HPS data path is inactive from the falling edge of the HGT at the output of the HPS, indicating that target byte are reached, to the start of the next line processing. Rising edge of the HGT at the HPS acquisition output.
HPS, Horizontal-fine-scale	6C		
BCS control	70		

8.14 Clipping

The SAA7146 supports clipping in the HPS data path. Clipping can be done with the Chroma Key information or with clip data information coming via master read through FIFO 2. Both sources will be ORed and can be switched on/off or inverted individually. These settings are controlled by the registers ClipCK and ClipMode.

The information read via FIFO 2 can be used for clipping with rectangle overlays or for bit mask clipping. The overlay clipping supports up to 16 rectangle overlays using 64 Dwords. The bit mask clipping allows an arbitrary number of window clips of any size or shape. This mode needs one bit for every pixel.

Chroma or clip information can be written to system memory via FIFO 3. This is controlled by the ClipOut Register. It is possible to combine the clip information with the inversion of the applied (foreground) chroma key. The result is a mask leaving the (background) area free. This mask can be read back in the next field to clip a different video stream to be placed into the same window as background (blue boxing).

Note that planar output formats overrule the use of FIFO 2 and FIFO 3 for clipping. Only chroma clipping is available and no clip information can be written.

8.14.1 Bit mask clipping

The bit mask clipping will use one Dword as clip-data for 32 pixels. The first bit of clip data is the MSB.

8.14.2 Rectangle overlay clipping

The rectangle overlay clipping is responsible for occluding rectangle overlay windows lying over a video window.

The rectangle clipping algorithm needs two lists, one for pixels and one for lines. Every list element in both lists contains a coordinate and display information for every overlay window. The 64 Dword FIFO 2 allows up to 16 overlay windows, each having two pixel list entries and two line list entries.

The rectangle overlay clipping can be used in interlaced or non-interlaced mode. This is controlled by the RecInterl Register bit. The overlay window coordinates are defined for the target window, independent of whether the video will be written interlaced or non-interlaced into the target window.

Every overlay window is defined by its top/left and bottom + 1/right + 1 coordinates. The coordinates are relative to the top left (0, 0) reference of the video window. The overlay clipping combines the coordinates with display information which is a 'overlay/no_overlay' (1, 0) bit for each overlay window. A simple example, shown in Fig.18, illustrates the relationship between coordinates and display information.

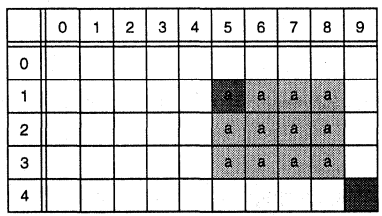
In this example one overlay window 'a' (5, 1; 8, 3) is defined. Relevant coordinates for the algorithm are the coordinates where display information changes. At the top/left coordinates (5,1) the display information will be set to 1 ('overlay'). Therefore, first list entries are (5, 1) for the pixel list and (1,1) for the line list. The overlay will end at the bottom/right coordinates plus one, e.g. at (9, 4) (8 + 1, 3 + 1). This will lead to the list entries (9, 0) for the pixel list and (4, 0) for the line list.

The central element of the rectangle overlay clipping combines the display information of lines and pixels held in the registers PIXEL_INFO and LINE_INFO. This unit will provide the 'no_display' information when both line and pixel display information are set to 'no_display'. In the example shown in Fig.18, this will happen for the pixels 5 to 8 and for the lines 1 to 3.

If there is more than one overlay window, the window display information of all windows will be combined into one display information. If any the display information of any window is saying 'no_display' the actual pixel will not be displayed. This ensures that overlapping overlay windows will be handled by the hardware, since the video information will only be displayed when no window is lying over it. Since the overlapping information is only implicitly in the lists, the overlapping information need not be taken into account during the creation of the lists.

The main part of the algorithm is responsible for loading the display information registers PIXEL_INFO and LINE_INFO. Both will be initialized to 'display'. LINE_INFO will be updated at the beginning of every line, when the line counter is equal to the LINE_NR in the line list. PIXEL_INFO will be updated when the pixel counter is equal to the PIXEL_NR in the pixel list. If there is no new information both registers will hold their old values.

Both line and pixel list have to be sorted from top to bottom or left to right coordinates and are not allowed to have two consecutive list elements with the same coordinate. In the example shown in Fig.19, the list entry with line coordinate 1 will hold the 'display' information of window 'a' and the 'no_display' information of window 'c', so two list elements with the same coordinate are merged into one. The last elements in the lists are characterized by the coordinate 0.



	0	1	2	3	4	5	6	7	8	9
0										
1						a	a	a	a	
2						a	a	a	a	
3						a	a	a	a	
4										

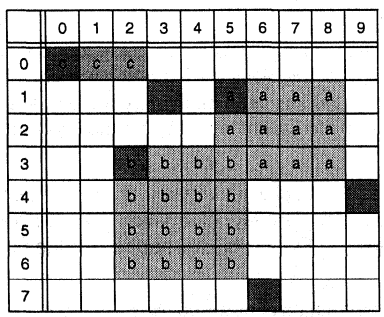
pixel	a
5	1
9	0

line	a
1	1
4	0

MGG267

Relevant coordinates shaded dark

Fig.18 Example 1 - Rectangle overlay clipping.



	0	1	2	3	4	5	6	7	8	9
0	c	c	c							
1				c		a	a	a	a	
2						a	a	a	a	
3			c	b	b	b	a	a	a	
4			b	b	b	b				c
5			b	b	b	b				
6			b	b	b	b				
7							c			

pixel	a	b	c
0	1	1	0
2	1	0	0
3	1	0	1
5	0	0	1
6	0	1	1
9	1	1	1
0	x	x	x

line	a	b	c
0	1	1	0
1	0	1	1
3	0	0	1
4	1	0	1
7	1	1	1
0	x	x	x

MGG269

Relevant coordinates shaded dark

Fig.19 Example 2 - Rectangle overlay clipping.

8.14.2.1 Memory organization for rectangle overlay windows.

Every overlay window is defined by two corners with four coordinates. One Dword holds one 11-bit coordinate and 16-bit with the display information for up to 16 overlay windows.

Table 87 Dword organization for rectangle overlay windows

UNUSED	COORDINATE	DISPLAY INFO
31 to 27 (5-bit)	26 to 16 (11-bit)	15 to 0 (16-bit)

The two lists, pixel list and line list, are interlocked in the 64 Dword memory. The pixel list is located at the even addresses, the line list at the odd addresses. This organization reduces the number of Dwords to be loaded, if there are less then 16 overlay windows. For example, 5 overlay windows need 20 Dwords for the coordinates and 2 Dwords as EOF marker.

8.14.2.2 Driver algorithm

Overlay window coordinates are relative to the video window and can range between 0, 0 and 2047. Relevant coordinates are top/left, bottom + 1/right + 1 of the overlay windows. If a overlay window has its bottom/right coordinates at the bottom/right of the video window its relevant coordinates bottom + 1/right + 1 would exceed the coordinate range and therefore don't have to be inserted into the lists.

Build lists:

Build sorted lists of lines and pixels containing top/left, bottom + 1/right + 1 coordinates of every overlay window, without having consecutive list entries with the same coordinate.
Every list will have an end of list entry with all coordinate bits set to zero. This EOL entry will follow the last entry.
If there are 16 overlay windows and no double coordinates the lists are full and there is no last entry.

Insert display information:

For every relevant coordinate in both lists and for every overlay window, if the coordinate in the line/pixel list is in between the top/bottom or left/right coordinates of the overlay window then set the display information bit to 1 ('display'). Otherwise, set the display information bit to 0 ('no_display').

8.15 Data Expansion Bus Interface (DEBI)

8.15.1 General description

The DEBI performs 16-bit parallel I/O in immediate (direct) transfer mode and block transfer mode. The immediate mode is used to transfer a byte, word or Dword to or from the target device. The block transfer mode offers the possibility to read or write up to 32 kbyte data blocks.

8.15.2 Features

- 8-bit and 16-bit slaves supported
- Byte, word and Dword transfers supported
- Slaves with or without handshake ability supported due to programmable cycle time
- Different endian types supported
- Interfacing to FIFO buffer for block transfer using DMA master transfer
- Optional address increment in block mode.

8.15.3 DEBI pins

There are 21 DEBI pins. Most of the control signals represent different functionality with respect to the selected interface mode (Intel/ISA or Motorola/68000).

Table 88 DEBI PIN list

PIN NAME	I/O	DESCRIPTION
AD15 to AD0	I/O	multiplexed Address and Data lines
AS_ALE	O	Address Strobe/Address Latch Enable
UDS_WRN	O	Upper Data Strobe/Write not
LDS_RDN	O	Lower Data Strobe/Read not
RWN_SBHE	O	Read/Write not/System Byte High Enable
DTACK_RDY	I	data acknowledge/Ready

8.15.4 FUNCTIONAL DESCRIPTION

32 bit transfers to 16 bit slave or 32 to 16 bit transfers to 8-bit slaves are done by generating multiple sub-cycles on the target bus. An immediate access cycle consist of one address phase and one data phase. A block transfer with address increment enabled consists of several consecutive address/data-phase couples. A block transfer with disabled address increment consists of one address phase followed by several data phases. The AS_ALE signal toggles only for a new address phase.The single bytes or words are assembled/disassembled to/from Dwords.This includes byte lane swapping since 8-bit devices use for data transfer AD7 to AD0 only. (AD15 to AD8 are also used in address phase since all 16 AD lines are used for addressing. Address generation is for 8-bit slaves the same as single byte transfers for 16-bit slaves).

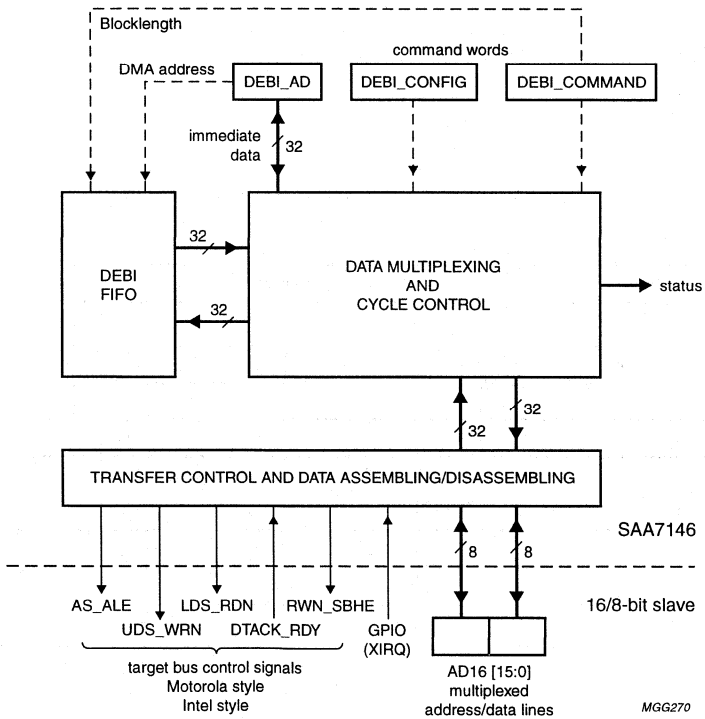


Fig.20 DEBI Interface.

8.15.4.1 Target bus cycle in Intel mode

A target transfer cycle starts by applying the target address to the multiplexed address/data lines. By setting ALE (Address Latch Enable) to LOW it is indicated that the address lines AD15 to AD0 and the SBHE (System Byte High Enable, indicating transfer on data lines 15 to 8) signal is valid. After asserting ALE the AD lines are multiplexed to data transfer. The indication of valid data in write mode or the request for data in read mode is done by transition of WRN or RDN to LOW. A 'normal' (no wait state) transfer does not use RDY LOW. If slaves use RDY LOW to extend the transfer time, they have to reset RDY to HIGH when they have placed valid data onto AD16 in read mode or when they have read their data in write mode. By using a programmable cycle timer, the transfer control gets into a 'wait for RDY HIGH' state for finishing the cycle when the TI (Timer overflow Interrupt) flag is set. The cycle will be ended when a time-out condition at RDY HIGH, or a rising edge of RDY after time-out is detected.

The enabling of the timer function is necessary for operating in the Intel mode. The cycle is ended by resetting ALE, SBHE, RDN/WRN to HIGH. A new cycle will not start before RDY HIGH is detected.

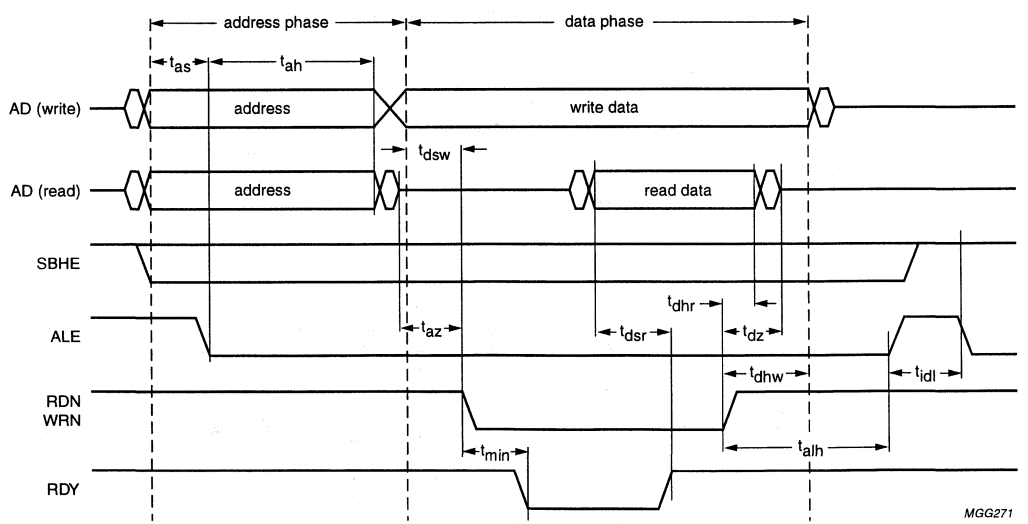


Fig.21 Intel style transfer.

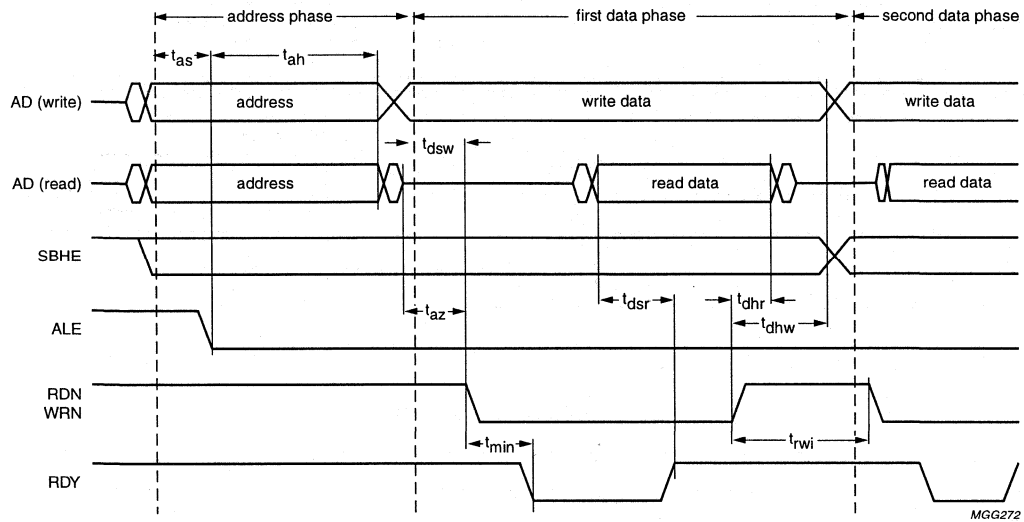


Fig.22 Intel style block transfer without address increment.

8.15.4.2 Target bus cycle in Motorola mode

The target transfer cycle starts with applying the target address onto the multiplexed address/data lines. By setting AS (Address Strobe) LOW it is indicated that the direction signal RWN (Read/Write Not) and the address is valid. The AS signal is usable as an Address Latch Enable signal, after asserting AS LOW the address/data lines will change to the data transfer state. The indication of valid data in write mode or the request for data in read mode is done by transition of UDS (Upper Data Strobe) and/or LDS (Lower Data Strobe) to LOW. Since the selection of the upper and lower bytes for transfer is done via LDS/UDS there is no need for address line A0. Only AD15 to AD1 are used for transmitting the (word-)address. Slaves with handshake ability must drive DTACK LOW when they have placed valid data onto AD16 in read mode or when they have read their data in write mode. The cycle is ended either with a time-out condition when DTACK is inactive, or when a positive DTACK edge is detected. Then AS, DS and RWN are reset HIGH. A new cycle will not start until DTACK HIGH is detected.

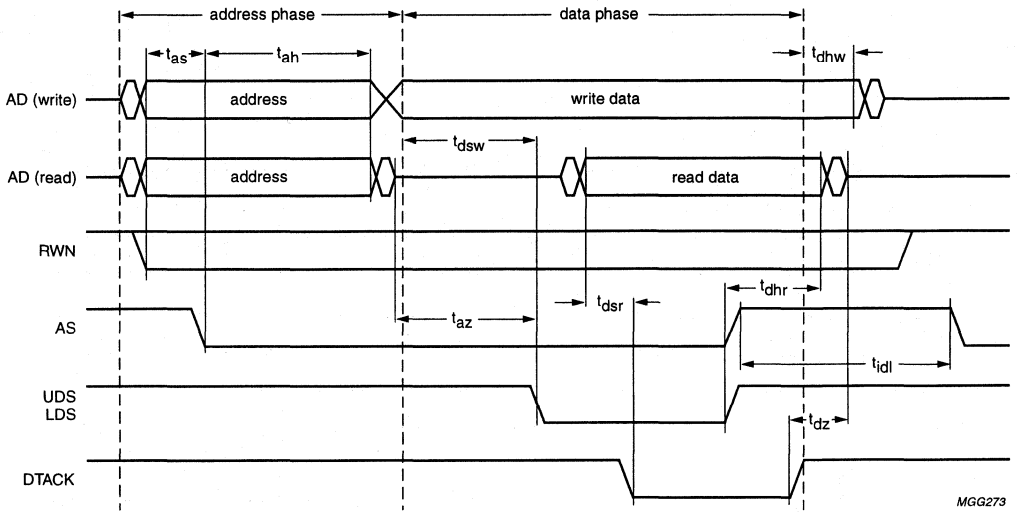


Fig.23 Motorola style transfer.

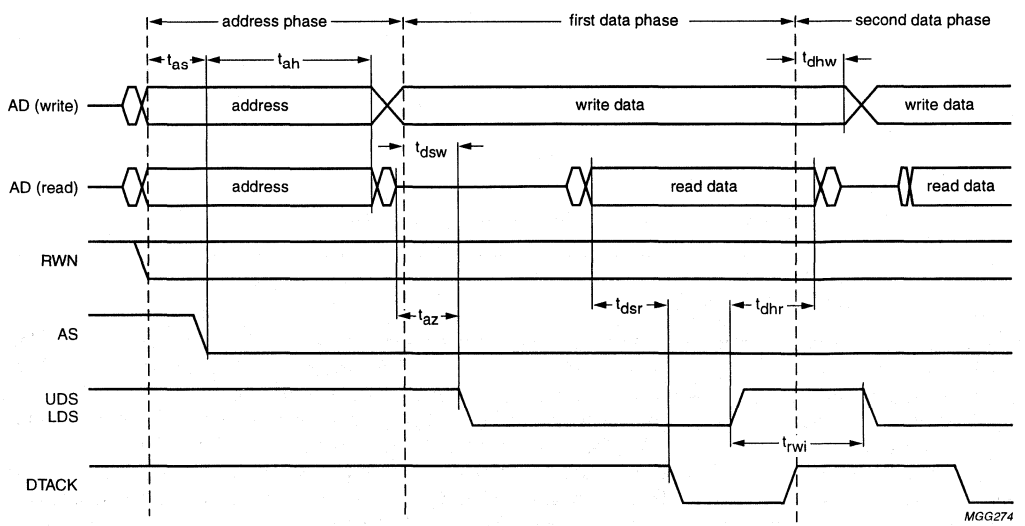


Fig.24 Motorola style block transfer without address increment.

Table 89 Timing parameters

SYMBOL	MIN.	MAX.	UNIT
t_{as}	15	–	ns
t_{ah}	20	–	ns
t_{az}	20	–	ns
t_{dhw}	0	–	ns
t_{dhr}	0	–	ns
t_{dsw}	15	–	ns
t_{dsr}	0	–	ns
t_{min}(1)	0	450	ns
t_{alh}	15	–	ns
t_{idl}	60	–	ns
t_{rwi}	30	–	ns
t_{dz}	0	120	ns

Note

1. Must be smaller than time-out adjustment.

8.15.4.3 Transfer configuration

The maximum cycle length is defined by using a programmable cycle timer. At time-out in Motorola mode the transfer control gets into a defined state by finishing the cycle when a slave is hanging or not able to handshake. In Intel mode the transfer control waits for RDY = 1 after time-out, i.e. the timer reflects the RDY reaction time of the target. In any time-out case the TI (Timer overflow Interrupt) flag is set. For initiating a transfer the target address (16-bit, pointing to the first byte to transfer), the transfer direction (WRITE_n) and the BLOCKLENGTH that indicates how many bytes have to be transferred must be specified. For block transfer a 32-bit DMA start address (PCI) has to be specified in the DEBI_AD Register. When the BLOCKLENGTH is 1 to 4 bytes the data is immediately transferred to/from the DEBI_AD Register. Immediate transfer crossing a Dword boundary is not allowed. Such illegal transfer attempts are reported by the FE (Format Error bit) in the Status Register. Immediate transfer starts with the least significant byte/word of the DEBI_AD Register. To support target devices of different endian type, the user must configure the Swap Register. External interrupts are supported by using GPIO pin events in RPS.

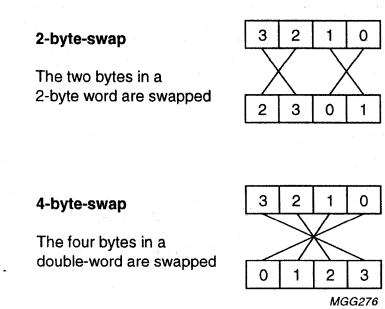


Fig.25 Transfer configuration.

8.15.4.4 Command word description

To configure and initiate a transfer there are 3 PCI memory mapped command words, writing to DEBI_COMMAND starts the transfer process.

Table 90 DEBI_AD

OFFSET (HEX)	NAME	BIT	TYPE	DESCRIPTION
88	DEBI_AD	31 to 0	RW	data input/output in immediate mode or DMA start address for block transfer (Dword aligned, [DEBI_AD1:0] must be 0)

Table 91 DEBI_CONFIG

OFFSET (HEX)	NAME	BIT	TYPE	DESCRIPTION
7C	TIMEOUT (3 to 0)	25 to 22	RW	finish cycle after <time-out> [PCI clock cycles] (if DTACK_RDY is inactive)
	SWAP	21 and 20	RW	endian swap type: 00: straight - don't swap 01: 2-byte swap 10: 4-byte swap 11: reserved
	SLAVE16	19	RW	indicates that slave is able to serve 16-bit cycles
	INCREMENT	18	RW	enables address increment for block transfer
	INTEL	17	RW	INTEL style bus handshake if HIGH, otherwise Motorola style
	TIEN	16	RW	Timer Enable (active LOW)

Table 92 DEBI_COMMAND

OFFSET (HEX)	NAME	BIT	TYPE	DESCRIPTION
80	BLOCK-LENGTH (14 to 0)	31 to 17	RW	BLOCKLENGTH > 4: block transfer length in bytes 4 ≥ BLOCKLENGTH > 0: immediate transfer 1 to 4 bytes BLOCKLENGTH = 0: reserved
	WRITE_N	16	RW	transfer direction (write if LOW)
	A16_IN	15 to 0	RW	slave target start address

Table 93 DEBI_PAGE

OFFSET (HEX)	NAME	BIT	TYPE	DESCRIPTION
84	DEBI_PAGE	31 to 12	RW	DEBI page table address (not used if PAGE_EN = 0)
	PAGE_EN	11	RW	enable address paging

8.16 Audio Interface

8.16.1 General description

The SAA7146 has two independent Audio Interface circuits A1 and A2 for serial input and output of digital audio data streams. The Audio Interface circuits are based on the I²S-bus standard, but can be configured to several data and timing formats (with respect to framing, bit clock and synchronisation). LSB first (Sony) formats are not supported. Up to 5 audio devices with separate serial data lines (state of the art) and dedicated word select lines can be connected directly. The interface also supports (future) devices that share one serial data line for multiple devices, to transmit data in different timeslots. A timeslot consists of one (serial) byte. Each interface circuit supports up to 5 serial data lines and related framing signals. A1 and A2 have the same internal structure. They share the audio interface pins, i.e. the pins can be accessed and utilized by one or the other audio interface circuit at a time.

In order to support systems with asynchronous or mixed audio sampling rates (e.g. 48 kHz and 44.1 kHz raster, or 48 kHz 2 × 16-bit stereo and 8 kHz 8-bit mono), the two audio interface circuits can run independently and even asynchronously regarding bit clock rate, sampling rate and framing (word select) signals. The two circuits can also be combined into one synchronous interface, sharing bit clock and framing and sampling frequencies. Each audio interface has two FIFOs, one for input, one for output, and two associated DMA control circuits, one for master-read, one for master-write, to exchange data with any PCI address, e.g. main memory. The data structure and signal flow control is timeslot oriented and also supports local feedback from input to output and from one timeslot to another timeslot. A set of timeslots can be looped into one 'audio super frame' containing up to 256 bits (32 timeslots). The signal flow is defined per timeslot and programmed by a timeslot list.

8.16.2 Basics of I²S-bus specification

The I²S-bus transports digital audio (sound) signals serially between ICs and consists of three signals:

- A continuous bit clock BCLK (or SCK), with (n × 8) - multiple of the audio sample frequency
- A serial data wire SD, transporting the data in serial bursts, with MSB first
- A framing signal WS (Word Select), defining (synchronizing) the start of a serial data burst.

WS and BCLK signals are provided by the master device. The SAA7146 audio interfaces are configurable as master or slave.

A data receiver must latch the data on SD with the rising edge of the bit clock BCLK. To satisfy the requirements regarding set-up and hold times more easily (and secure), it is recommended that the transmitter sends its data on the falling edge. Set-up and hold times are specified 'parameterized'; i.e. as a percentage of the actual bit clock. The serial data starts one clock cycle after an edge of WS or synchronous to the edge. The word (burst) length of transmitter and receiver may be different. Missing LSBs are filled with zeros, excess LSBs truncated. There are other formats for transmitting serial digital audio data between ICs, which are slightly different, but still very similar to I²S. The data set-up and hold time or even the definition of active clock edge may vary. The word select or framing signal can be 'in sync' with the MSB of the data burst instead of one clock cycle ahead. The Sony format is quite different, as it starts with LSB first.

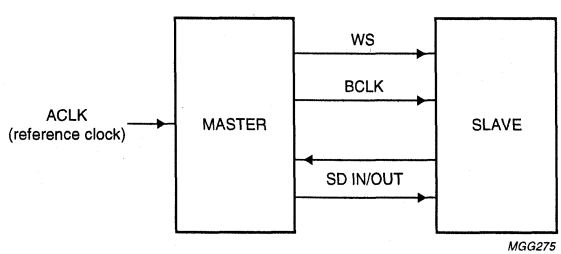


Fig.26 General application scheme.

8.16.3 Audio Interface pins

There are 14 Audio Interface pins. S01 is output only for A1 and input only for A2, SD4 is output only for A2 and input only for A1. The other pins can be used by either one of the two interface circuits but only one at a time.

Table 94 Audio pin list

PIN	I/O	FUNCTION
ACLK	I	audio reference clock; multiple of serial bit clock, multiple of audio sampling; maximum frequency 25 MHz; has to be provided even in slave mode
BCLK1	I/O	bit clock 1
BCLK2	I/O	bit clock 2
SD0	I/O	serial data output for audio interface A1 or input for A2
SD1	I/O	serial data I/O for audio interface A1 or A2
SD2	I/O	serial data I/O for audio interface A1 or A2
SD3	I/O	serial data I/O for audio interface A1 or A2
SD4	I/O	serial data input for audio interface A1 or output for A2
WS0	I/O	word select line 0, as input used as super frame sync (trigger)
WS1	O	word select output line 1
WS2	O	word select output line 2
WS3	O	word select output line 3
WS4	I/O	word select line 4, as input used as super frame sync (trigger)

8.16.4 Audio Interface circuit

Each of the two Audio Interface circuits of the SAA7146 consists of the following major functional parts:

- Output Dword (format) buffer (to load from FIFO)
- Output data Selector (byte mux 8 to 1)
- Parallel-to-Serial converter
- Output pin selector (destination mux)
- Serial Data Input selector (bit mux 4 to 1)
- Serial-to-Parallel converter (1 byte)
- Input Dword (format) buffer (to store into FIFO)
- Audio Input FIFO and Master Write DMA
- Feedback (Hand) buffer
- Master Read DMA and Audio Output FIFO
- Bit Clock selector or generator
- Timeslot counter and Word Select signal generator.

8.16.4.1 Audio clock selection

The clock divider circuit offers 16 different clock stages. To transform a reference clock of 24.576 MHz to a bit clock for an 8 kHz and 8-bit sampling (just 8-bit serial), a clock division of 384 has to be selected. To transform a reference clock of 24.576 MHz to a bit clock for an 48 kHz sampling and 64-bit framing, a division of 8 has to be selected.

The bit clock is divided-by-8, which defines a timeslot, corresponding to the time span of one byte in serial protocol. The timeslot counter gets a count pulse every timeslot. It can be running free, or can be triggered (reset) via an external word select signal (super-frame sync). Audio interface circuit A1 can be triggered by WS0, audio interface circuit A2 can be triggered by WS4. A timeslot list processor generates word select output signals, and the internal signals to control the signal flow per timeslot. A timeslot list contains up to 16 records, each 32-bits wide, supporting super frames with up to 32 timeslots.

WS0 (or WS4) trigger timeslot generator and timeslot counter directly 'in sync', or are one clock cycle ahead. The WS signals can be generated 'in sync' with the timeslot (i.e. MSB of serial data), or 1-bit clock cycle ahead. Each of the two audio interface circuits A1 and A2 has its own independent timing generator. Extra control bits define which of the two timing generators drive which of the word select pins WS0 to WS4.

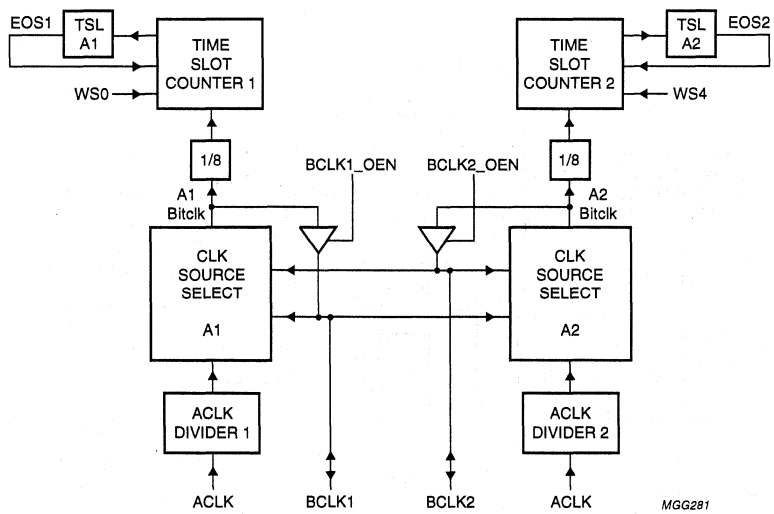


Fig.27 Audio clock control.

8.16.4.2 Audio data path

An input multiplexer selects serial data from one of four SD pins. A1 can select SD0 and the common serial data pins SD1, SD2 and SD3. A2 can select SD4 and the common serial data pins SD1, SD2 and SD3. A serial-to-parallel converter collects 8 bits to form a byte in a timeslot. At the end of the timeslot this byte can be stored into a Dword buffer, and/or into the feedback buffer or can be thrown away. The first byte that is latched, is placed into the first byte-place of the buffer, the second byte that is latched, is placed into the second byte-place, etc.

Big endian and Little endian stuffing is supported. If bytes are not latched into a certain buffer, the place pointer of the corresponding buffer is not incremented. The write (fill) pointer of the feedback buffer is reset to it's initial position with every start/restart of the super-frame. Up to four bytes of the input data stream can be placed in the intermediate feedback buffer. They can be selected from the buffer to provide data to the output.

The feedback buffer is also read and write accessible via the PCI bus. This allows reading of status information and writing of control information at specific positions in the audio frame. The write access to the feedback buffer is synchronized with the first byte position of the frame pointer (to avoid control data corruption in the current frame). The samples of the various real world audio signal streams are byte or word interleaved in system memory and PCI address space. It is the responsibility of system/board designer and of software/programmer to produce a reasonable sample ordering, e.g. have a 16-bit sample on a word boundary and not crossing a Dword boundary.

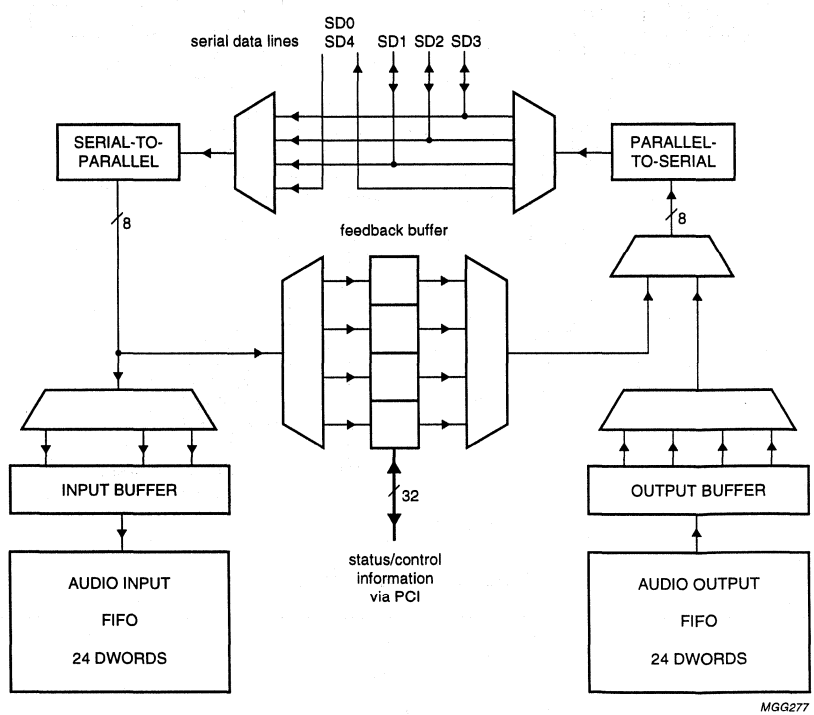


Fig.28 Audio data flow control in A1 and A2.

Table 95 Feed back buffers

OFFSET	NAME	BIT	TYPE	DESCRIPTION
144H	FB_BUFFER1	31 to 0	RW	feeds back audio data or stores status/control informations
148H	FB_BUFFER2	31 to 0	RW	feeds back audio data or stores status/control informations

Under control of the timeslot list, a collected Dword is then stored into the input FIFO. The FIFO size is determined to 24 Dwords.

An audio sampling frequency of f_s = 48 kHz, and n = 16 timeslots in a super-frame results in a maximum data load for PCI from an audio capture DMA channel of 768 kbytes/s. (The bit clock rate is 6144 kbit/s). That accounts for about 13 Dwords per regular video line time. To generate audio output signals, a master read DMA control fills the output FIFO. A Dword buffer is loaded from FIFO under control of the timeslot list. The parallel-to-serial converter takes a byte as programmed in the timeslot list from one of the 8 buffer places: 4 in the Dword buffer, 4 in the feedback buffer. The serial output is directed to one of the accessible SD pins. Positive as well as negative clock edge data transmission is supported by optional BCLK inversion.

Each record in the timeslot list describes, how the bytes appearing on the port, are mapped to the Dword wide DMA channels, respectively to the feedback or input buffers. A timeslot list record consists of 4 bytes. As up to 32 timeslots are supported, the timeslot list is comprised of 16 Dwords of programming for each audio interface circuit A1 or A2 which can be concatenated.

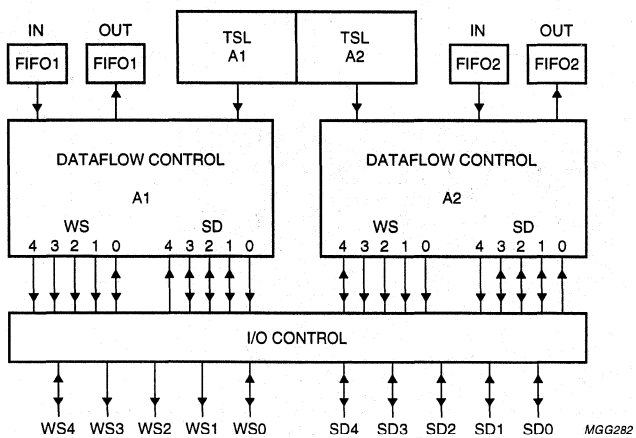


Fig.29 Audio data path components.

Table 96 Timeslot list structure

RECORD STRUCTURE		TSL1 16 DWORDS (OFFSET: 180 TO 1BCH)																TSL2 16 DWORDS (OFFSET: 1C0 TO 1FCH)															
BIT#	NAME	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
31	WS0																																
30	WS1																																
29	WS2																																
28	WS3																																
27	WS4																																
26	reserved																																
25	DIS_A1[1]																																
24	DIS_A1[0]																																
23	SDW_A1																																
22	SIB_A1																																
21	SF_A1																																
20	LF_A1																																
19	BSEL_A1[2]																																
18	BSEL_A1[1]																																
17	BSEL_A1[0]																																
16	DOD_A1[1]																																
15	DOD_A1[0]																																
14	LOW_A1																																
13	reserved																																
12	DIS_A2[1]																																
11	DIS_A2[0]																																
10	SDW_A2																																
9	SIB_A2																																
8	SF_A2																																
7	LF_A2																																
6	BSEL_A2[2]																																
5	BSEL_A2[1]																																
4	BSEL_A2[0]																																
3	DOD_A2[1]																																
2	DOD_A2[0]																																
1	LOW_A2																																
0	EOS																																

Each interface, A1 and A2, uses its own TSL when working independently of each other. The shaded areas are valid for combined processing of TSL1 and TSL2 only. In these modes, TSL1 or TSL2 are used interleaved or concatenated, to achieve one single TSL with up to 32 records. Both parts of the list control both interface circuits in parallel. All four DMA channels are available. The TSLs are write only.

Table 97 Timeslot list bit functions

NAME	FUNCTION
WS0	Defining pattern of word select signal output at WS0 pin. If WS0 pin is input and trigger, WS0 bit is meaningless.
WS1	Defining pattern of word select signal output at WS1 pin.
WS2	Defining pattern of word select signal output at WS2 pin.
WS3	Defining pattern of word select signal output at WS3 pin.
WS4	Defining pattern of word select signal output at WS4 pin. If WS4 pin is input and trigger, WS4 bit is meaningless.
DIS_Ax[1:0]	Select serial data input from: 00 : SD0 (for A2); SD4 (for A1) 01 : SD1 10 : SD2 11 : SD3.
SDW_Ax	0: do not load this byte into the Dword buffer 1: load this byte into the Dword buffer, place into the next available position
SIB_Ax	0: do not load this byte into the intermediate feedback buffer 1: load this byte into the intermediate feedback buffer, place into the next available position
SF_Ax	0: do nothing 1: store Dword buffer into input FIFO, at the next available position
LF_Ax	0: do nothing 1: load next Dword from output FIFO into output Dword buffer
BSEL_Ax[2:0]	Select byte for parallel-to-serial converter from output Dword buffer or from intermediate feedback buffer: 000: take byte 0 from output Dword buffer 001: take byte 1 from output Dword buffer 010: take byte 2 from output Dword buffer 011: take byte 3 from output Dword buffer 100: take byte 0 from intermediate feedback buffer 101: take byte 1 from intermediate feedback buffer 110: take byte 2 from intermediate feedback buffer 111: take byte 3 from intermediate feedback buffer.
DOD_Ax[1:0]	Define on which SD pin the serial output data will appear. If both circuits attempt to drive the same SD pin in the same timeslot, A1 gets preference. When a SD pin is not driven actively it is 3-stated. 00: at SD0 (for A1); at SD4 (for A2) 01: at SD1 10 at SD2 11: at SD3.
LOW_Ax	Drive the SD pin which was driven in the previous timeslot as output, for 7-bit clock cycles to active LOW and let then go to 3-state.
EOS	End Of Superframe: last record in timeslot list, next timeslot uses first record of the TSL (reset TSL pointer).

8.16.5 AUDIO CONFIGURATION

The configuration parameters are selected using two configuration registers: ACON1 and ACON2.

The ACON1 Register is locally buffered. The download from the Shadow Register into the working register is done when reaching a DMA protection address or immediately when both interfaces are not active (switched off, initial state).

Table 98 Audio Configuration Register 1 (ACON1)

OFFSET (HEX)	NAME	BIT	TYPE	DESCRIPTION
F4	AUDIO_MODE [2:0]	31 to 29	RW	defines interface activation and combination
	MAXLEVEL [6:0]	28 to 22	RW	defines the maximum allowed absolute value for the most significant byte of an audio sample
	A1_SWAP	21	RW	defines if input (captured) data is stuffed in little endian or big endian format for A1 (4 byte swap if set)
	A2_SWAP	20	RW	defines if input (captured) data is stuffed in little endian or big endian format for A2 (4 byte swap if set)
	WS0_CTRL [1:0]	19 and 18	RW	function control for WS0 line
	WS0_SYNC [1:0]	17 and 16	RW	pulse position and width control for WS0 line
	WS1_CTRL [1:0]	15 and 14	RW	function control for WS1 line
	WS1_SYNC [1:0]	13 and 12	RW	pulse position and width control for WS1 line
	WS2_CTRL [1:0]	11 and 10	RW	function control for WS2 line
	WS2_SYNC [1:0]	9 and 8	RW	pulse position and width control for WS2 line
	WS3_CTRL [1:0]	7 and 6	RW	function control for WS3 line
	WS3_SYNC [1:0]	5 and 4	RW	pulse position and width control for WS3 line
	WS4_CTRL [1:0]	3 and 2	RW	function control for WS4 line
	WS4_SYNC [1:0]	1 and 0	RW	pulse position and width control for WS4 line

Table 99 Audio Configuration Register 2 (ACON2)

OFFSET (HEX)	NAME	BIT	TYPE	DESCRIPTION
F8	A1_CLKSRC [4:0]	31 to 27	RW	defines the bit clock source for A1
	A2_CLKSRC [4:0]	26 to 22	RW	defines the bit clock source for A2
	INVERT_BCLK1	21	RW	use or output BCLK1 with inverted polarity
	INVERT_BCLK2	20	RW	use or output BCLK2 with inverted polarity
	BCLK1_OEN	19	RW	output enable BCLK1 (active LOW)
	BCLK2_OEN	18	RW	output enable BCLK2 (active LOW)

8.16.5.1 Audio mode control

There are 3 audio mode bits to select which TSL is active and how to synchronize and combine them. The first half of the following table supports asynchronous operation of A1 and A2, each following their own configuration bits and working independent to each other. In the second half of the table, the two interfaces work synchronous, according to the clock configuration setting of A1_CLKSRC. Some special cases are discussed below:

AUDIO_MODE [2:0] = 7:
The two TSLs are chained to each other thus enabling a longer TSL, with up to 32 timeslots to be built (SINGER format). There is only one common TSL pointer active, which is able to reach the whole address range. The pointer synchronisation is done according to A1 configuration. There is only one EOS bit needed.

AUDIO_MODE [2:0] = 5 ↔ 6:
Both interfaces working synchronous on the same TSL half and with the same record. Synchronous change from one TSL to the other TSL when reaching the protection address. By that the TSL can be changed, by switching to the other TSL, without disturbing real time flow of audio streams. There is no time gap necessary for reprogramming a TSL. Reprogramming is performed by using the other TSL as shadow. The two TSL pointers are locked, i.e. each one pointing to its own list area, but resetting and incrementing synchronous.

Table 100 Audio_mode control

AUDIO_MODE [2:0]	AUDIO INTERFACE A1	AUDIO INTERFACE A2
0	off	off
1	processing TSL1; synchronisation according to A1 configuration	off
2	off	processing TSL2; synchronisation according to A2 configuration
3	processing TSL1; synchronisation according to A1 configuration	processing TSL2; synchronisation according to A2 configuration
4	processing TSL1; synchronisation according to A1 configuration	processing TSL2; TSL2 pointer is in sync (locked) to TSL1 pointer; TSL2 pointer = TSL1 pointer + 16
5	processing TSL1; synchronisation according to A1 configuration	processing TSL1 in common with A1; TSL2 pointer = TSL1 pointer
6	processing TSL2 in common with A2; TSL1 pointer = TSL2 pointer	processing TSL2; synchronisation according to A1 configuration
7	processing TSL1 and TSL2 in common with A2, synchronization according to A1 configuration; TSL1 pointer range is up to 32 records	processing TSL1 and TSL2 in common with A1; TSL2 pointer = TSL1 pointer

8.16.5.2 Audio input level monitoring

The audio input level monitoring feature allows the control of audio input levels without additional external hardware, by comparing the absolute value of the most significant byte of an audio sample to a programmable reference maximum level. The MAXLEVEL is defined by 7 bits, since serial audio data is transmitted in two's complement and the sign of the compared byte is not relevant for audio level control. Therefore, MAXLEVEL is programmable from 0 up to 127. The two's complement value I–128I is not reachable, but also not functionally needed. The comparison results are stored in the 32-bit Level Report Register with one bit per timeslot of TSL1 and TSL2, reporting whether there was a level violation in that timeslot. The comparison runs all the time and the Level Report Register is reset when it is read by software.

Table 101 Level Report Register

OFFSET (HEX)	NAME	BIT	TYPE	DESCRIPTION
140	LEVEL_REPORT	31 to 0	R	Stores the violation of MAXLEVEL for all 32 TSL records. Reset to 0000H when read.

8.16.5.3 WS line controlling

The WSx_CTRL bits define which of the WS lines is output and controlled by which audio interface circuit (A1 or A2). WSx_SYNC defines the timing of WS signals.

Table 102 Static function control for word select lines

WSX_CTRL [1:0]	WS0 FUNCTION	WS1 FUNCTION	WS2 FUNCTION	WS3 FUNCTION	WS4 FUNCTION
00	3-state, input, rising edge resets TSL1 pointer	3-state	3-state	3-state	3-state, input, rising edge resets TSL2 pointer
01	output, controlled by TSL1	output, controlled by TSL1	output, controlled by TSL1	output, controlled by TSL1	output, controlled by TSL1
10	output, controlled by TSL2	output, controlled by TSL2	output, controlled by TSL2	output, controlled by TSL2	output, controlled by TSL2
11	output, active LOW	output, active LOW	output, active LOW	output, active LOW	output, active LOW

Table 103 Pulse width and position control

WSX_SYNC [1:0]	PULSE FUNCTION
00	I^2S style: WS goes active one bitclock cycle before MSB of timeslot and stays active until LSB, i.e. one bitclock before MSB of next timeslot.
01	WS goes active in sync with MSB and stays active until next MSB, i.e. active in sync with current timeslot.
10	WS goes active one bitclock before MSB and stays active for one bitclock cycle, i.e. negative edge is in sync with beginning of timeslot.
11	SINGER style: WS goes active in sync with MSB and stays active for one bitclock cycle and for two bitclock cycles in first timeslot of superframe.

8.16.5.4 Bit clock control

Specific to each audio interface, A1 or A2, is the programming of bit clock source.

Table 104 CLK source definition

AX_CLKSRC [4:0] (HEX)	A1 BITCLOCK	A2 BITCLOCK
1F to 13	reserved	reserved
12	ACLK divided-by-384	ACLK divided-by-384
11	ACLK divided-by-256	ACLK divided-by-256
10	ACLK divided-by-192	ACLK divided-by-192
0F	ACLK divided-by-128	ACLK divided-by-128
0E	ACLK divided-by-96	ACLK divided-by-96
0D	ACLK divided-by-64	ACLK divided-by-64
0C	ACLK divided-by-48	ACLK divided-by-48
0B	ACLK divided-by-32	ACLK divided-by-32
0A	ACLK divided-by-24	ACLK divided-by-24
09	ACLK divided-by-16	ACLK divided-by-16
08	ACLK divided-by-12	ACLK divided-by-12
07	ACLK divided-by-8	ACLK divided-by-8
06	ACLK divided-by-6	ACLK divided-by-6
05	ACLK divided-by-4	ACLK divided-by-4
04	ACLK divided-by-3	ACLK divided-by-3
03	ACLK divided-by-2	ACLK divided-by-2
02	ACLK	ACLK
01	BCLK2	BCLK1
00	BCLK1	BCLK2

8.16.6 SWITCHING AUDIO STREAMS

There are different levels of switching data streams on and off:

- DMA transfer enable; switching a DMA channel
- AUDIO_MODE; switching the two audio interfaces
- WSx_CTRL; switching a physical channel.

The AUDIO_MODE and WSx_CTRL programming is locally buffered and gets loaded when the corresponding DMA protection address is reached. When both interfaces are off, changes are loaded immediately.

If an audio interface is switched on, it will start working at TSL pointer reset. Disabling a DMA channel clears the corresponding FIFO and sets the DMA pointers to base address. This is the initial state. It is recommended to enable the output DMA channels before activating the interface, since the output FIFO has to be filled with valid output data.

It is responsibility of the software to configure data structures, TSL sequences and protection address in such way, that they match to each other.

8.17 I²C-bus Interface

8.17.1 General description

The I²C-bus is a simple 2-wire bus for efficient inter-IC data exchange. Only two bus lines are required: a serial clock line (SCL) and a serial data line (SDA). It's a true multi-master bus including collision detection and arbitration to prevent data corruption if two or more masters simultaneously initiate data transfers. Serial clock synchronization allows devices with different bit rates to communicate via the same serial bus. The block diagram is shown in Fig.30.

8.17.2 Functional description

The I²C-bus performs byte oriented data transfers. Clock generation and bus control arbitration are controlled by hardware. The Status Register (IICSTA) reflects the status of the interface and the I²C-bus (see Table 105). An Interrupt after execution may be enabled optionally. The Bus Clock Generator supports bit rates from 5 kHz up to 400 kHz.

The I²C-bus interface is programmed through the Transfer Control Register (IICTRF) which is shown in Table 107. A write to this register starts the transfer sequence where up to 3 bytes are transferred: BYTE2, BYTE1 and BYTE0. Any of these 3 bytes may be disabled or enabled for use (as data byte or 7-bit address plus RW# bit) in three I²C-bus protocol functions:

- START - start/restart and address device
- Cont. - transfer data and continue
- STOP - transfer data and stop.

All bus operations are done via these three functions. The functional usage of each single byte is defined by the byte specific attribute information; see Table 108.

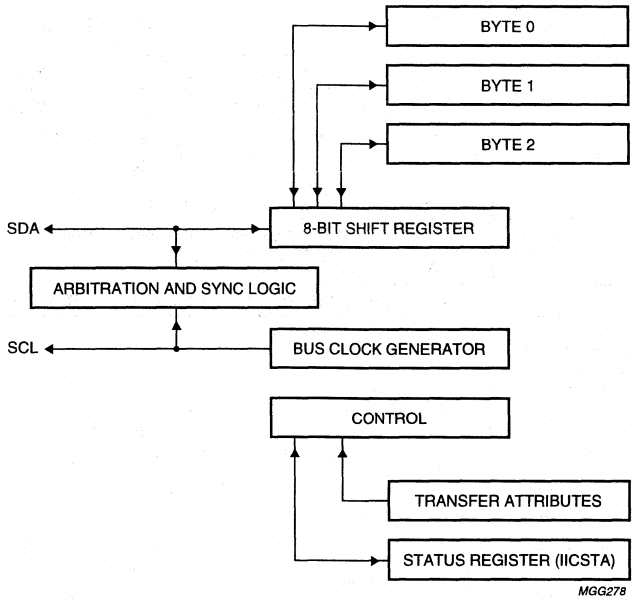


Fig.30 Block diagram of I²C-bus serial Interface.

Table 105 Status Register (IICSTA)

OFFSET (HEX)	NAME	BIT	TYPE	DESCRIPTION
90	IICCC[2:0]	10 to 8	RW	Clock bit rate selection; see Table 106
	ABORT	7	RW	ABORT OPERATION - clears busy bit (after an error)
	SPERR	6	RW	bus error due to invalid start/stop condition
	APERR	5	RW	NACK - error in address phase
	DTERR	4	RW	NACK - error in data transmission
	DRERR	3	RW	NACK - error when receiving data
	AL	2	RW	arbitration lost
	ERR	1	R	general error flag - has to be reset by clearing all error flags
	BUSY	0	R	operation ongoing

Table 106 Selection of I^2C-bus bit rate

IICCC2	IICCC1	IICCC0	BIT RATE[1]
1	0	1	PCI clock/6400
0	0	1	PCI clock/3200
1	0	0	PCI clock/480
1	1	0	PCI clock/320
1	1	1	PCI clock/240
0	0	0	PCI clock/120
0	1	0	PCI clock/80
0	1	1	PCI clock/60

Note

1. The selected bit rate is the maximum bit rate and could be 'stretched' (slowed down) by slaves. Refer to the document *"The I^2C-bus and how to use it"* for further details. This document may be ordered using the code 9398 393 40011.

Table 107 Transfer Control Register (IICTRF)

OFFSET (HEX)	NAME	BIT	TYPE	DESCRIPTION
8C	BYTE2	31 to 24	RW	Data/address Register 2
	BYTE1	23 to 16	RW	Data/address Register 1
	BYTE0	15 to 8	RW	Data/address Register 0
	ATTR2[1:0]	7 and 6	RW	attribute information for BYTE2
	ATTR1[1:0]	5 and 4	RW	attribute information for BYTE1
	ATTR0[1:0]	3 and 2	RW	attribute information for BYTE0
	ERR	1	RW	general error flag - has to be reset by clearing IICSTA
	BUSY	0	RW	operation ongoing

Table 108 ATTRx1 and ATTRx0 - Attribute information for BYTEx

ATTRX1	ATTRX0	SYMBOL	PROTOCOL FUNCTION				
1	1	start	start and address device, use BYTEx [7:1] as DA7 to D1 and BYTEx[0] as R/W bit				
			S	DA7 to DA1	R/W	A(1)	
1	0	cont.	transfer D and continue, use BYTEx [7:0] as D7 to D0				
				D7 to D0		A(1)	
0	1	stop	transfer D and stop, use BYTEx as D7 to D0				
				D7 to D0		A/NA(1)	P
0	0	nop	no operation, don't use this byte				

Note

1. The generation of NA or A is done by the controller hardware and is not user accessible.

8.17.2.1 Abbreviations used in Table 108

S - I²C START command

DA - 7-bit Device Address (BYTEx7 to BYTEx1)

R/W - Read/Write# bit (BYTEx0)

D - receive/transmit Data (BYTEx)

A - Acknowledge

NA - Negative Acknowledge (also used for identification of last master read data byte)

P - I²C STOP command.

8.17.2.2 Example

The protocol sequence for reading three bytes with sub-address access is illustrated in Fig.31. The procedure for this read operation is detailed below:

1. Address slave, write to IICTFR (see Fig.32):
   BYTE2 [7:1] = DA, BYTE2 [0] = 0 (write), ATTR2 = START
   BYTE1 = sub-address, ATTR1 = cont.
   BYTE0 [7:1] = DA, BYTE0 [0] = 1(read), ATTR0 = START
2. Wait until BUSY = 0
3. Check ERR bit, if it is inactive the slave target is successfully addressed
4. Transfer data, write attribute information to IICTFR (see Fig.33):
   BYTE2 = first received data byte, ATTR1 = cont.
   BYTE1 = second received data byte, ATT0 = STOP
5. Wait until BUSY = 0
6. Check ERR bit, if it is inactive IICTFR contains valid data.

Instead of checking ERR after each single three byte sequence, it is possible to check the general error flag ERR at the end of the whole protocol sequence. During a bus cycle, the BUSY bit is set HIGH. At the end of a bus cycle an interrupt request is generated if enabled and BUSY is cleared if no error occurs. Writes to the IICTRF should not be done while the BUSY bit is active, otherwise the ERR flag is set HIGH. If no transfer errors occur during the three transfer actions, the ERR bit will be set LOW. If an error occurs the ERR bit will be set HIGH and the BUSY bit stays HIGH. In this case the error and BUSY flags have to be cleared before starting a new operation.

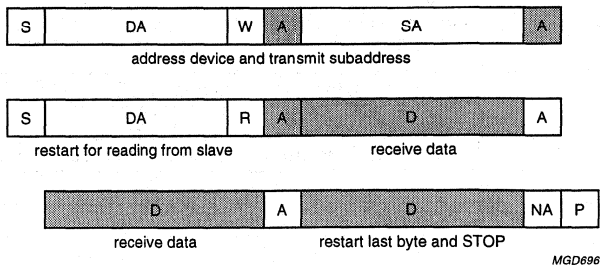


Fig.31 Protocol sequence for reading three bytes with sub-address access.

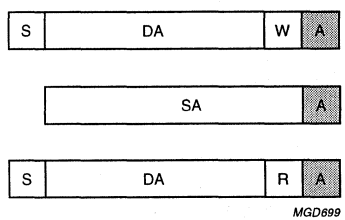


Fig.32 Address slave and write to IICTFR.

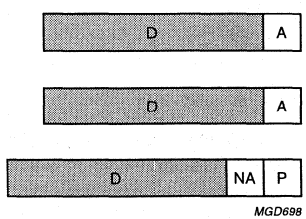


Fig.33 Transfer data and write attribute information to IICTFR.

8.18 SAA7146 Register Tables

Table 109 Registers and offsets sorted by functional groups

OFFSET (HEX)	NAME	TYPE	RAM	READ VALUE AFTER RESET	CORRESPONDING UPLOAD BIT
00	BaseOdd1	RW	yes	undefined	Video DMA1 upload
04	BaseEven1	RW	yes	undefined	
08	ProtAddr1	RW	yes	undefined	
0C	Pitch1	RW	yes	undefined	
10	BasePage1	RW	yes	undefined	
14	Num_Line_Byte1	RW	yes	undefined	
18	BaseOdd2	RW	yes	undefined	Video DMA2 upload
1C	BaseEven2	RW	yes	undefined	
20	ProtAddr2	RW	yes	undefined	
24	Pitch2	RW	yes	undefined	
28	BasePage2	RW	yes	undefined	
2C	Num_Line_Byte2	RW	yes	undefined	
30	BaseOdd3	RW	yes	undefined	Video DMA3 upload
34	BaseEven3	RW	yes	undefined	
38	ProtAddr3	RW	yes	undefined	
3C	Pitch3	RW	yes	undefined	
40	BasePage3	RW	yes	undefined	
44	Num_Line_Byte3	RW	yes	undefined	
94	BaseA1_in	RW	read	undefined	immediate write access
98	ProtA1_in	RW	read	undefined	
9C	PageA1_in	RW	read	undefined	
A0	BaseA1_out	RW	read	undefined	
A4	ProtA1_out	RW	read	undefined	
A8	PageA1_out	RW	read	undefined	
AC	BaseA2_in	RW	read	undefined	
B0	ProtA2_in	RW	read	undefined	
B4	PageA2_in	RW	read	undefined	
B8	BaseA2_out	RW	read	undefined	
BC	ProtA2_out	RW	read	undefined	
C0	PageA2_out	RW	read	undefined	
48	PCI_BT_V	RW	yes	undefined	Video DMA1, 2, or 3 upload

OFFSET (HEX)	NAME	TYPE	RAM	READ VALUE AFTER RESET	CORRESPONDING UPLOAD BIT
4C	PCI_BT_A	RW	read	undefined	immediate write access
120	PCI_VDP1	R	no	00000000	
124	PCI_VDP2	R	no	00000000	
128	PCI_VDP3	R	no	00000000	
12C	PCI_ADP1	R	no	00000000	
130	PCI_ADP2	R	no	00000000	
134	PCI_ADP3	R	no	00000000	
138	PCI_ADP4	R	no	00000000	
13C	PCI_DDP	R	no	00000000	
FC	MC1	RW	no	00008100	immediate access
100	MC2	RW	no	00000000	
104	RPS_ADDR0	RW	no	00000000	
108	RPS_ADDR1	RW	no	00000000	
C4	RPS_PAGE0	RW	read	undefined	immediate write access
C8	RPS_PAGE1	RW	read	undefined	
CC	RPS_THRESH0	RW	read	undefined	
D0	RPS_THRESH1	RW	read	undefined	
D4	RPS_TOV0	RW	read	undefined	
D8	RPS_TOV1	RW	read	undefined	
110	PSR	R	no	undefined	–
114	SSR	R	no	undefined	
DC	IER	RW	read	undefined	immediate write access
10C	ISR	RW	no	00000000	immediate access
E0	GPIO_CTRL	RW	read	undefined	immediate write access
118	EC1R	R	no	00000000	–
11C	EC2R	R	no	00000000	
E4	EC1SSR	RW	read	undefined	immediate write access
E8	EC2SSR	RW	read	undefined	
EC	ECT1R	RW	read	undefined	
F0	ECT2R	RW	read	undefined	
50	Initial settings DD1-Port	RW	yes	undefined	D1 Interface upload
54	Video DATA stream handling at port DD1	RW	yes	undefined	
58	BRS control #1 Register	RW	yes	undefined	BRS upload

OFFSET (HEX)	NAME	TYPE	RAM	READ VALUE AFTER RESET	CORRESPONDING UPLOAD BIT
5C	HPS control	RW	yes	undefined	HPS section 1 upload
60	HPS, Vertical-scale	RW	yes	undefined	HPS section 2 upload
64	HPS, Vertical-scale and gain	RW	yes	undefined	
68	HPS Horizontal-pre-scale	RW	yes	undefined	HPS section 1 upload
6C	HPS Horizontal-fine-scale	RW	yes	undefined	
70	BCS control	RW	yes	undefined	HPS section 2 upload
74	Chroma Key range	RW	yes	undefined	
78	HPS Output and Formats Clip control #1	RW	yes	undefined	
8C	IICTFR	RW	yes	XXXXXXX0	I^2C upload
90	IIC_STA	RW	yes	00000000	
88	DEBI_AD	RW	yes	00000000	DEBI upload
7C	DEBI_CONFIG	RW	yes	undefined	
80	DEBI_COMMAND	RW	yes	undefined	
84	DEBI_PAGE	RW	yes	undefined	
F4	ACON1	RW	read	undefined	immediate write access
F8	ACON2	RW	read	undefined	
144	FB_BUFFER1	RW	no	00000000	immediate access
148	FB_BUFFER2	RW	no	00000000	
140	LEVEL_REP	R	no	00000000	–
180-1BC	Audio Time Slot Registers1	W	no	no read back	immediate access
1C0-1FC	Audio Time Slot Registers2	W	no	no read back	

Table 110 Registers and offsets sorted by address-offset

OFFSET (HEX)	NAME	TYPE	RAM	READ VALUE AFTER RESET	CORRESPONDING UPLOAD BIT
00	BaseOdd1	RW	yes	undefined	Video DMA1 upload
04	BaseEven1	RW	yes	undefined	
08	ProtAddr1	RW	yes	undefined	
0C	Pitch1	RW	yes	undefined	
10	BasePage1	RW	yes	undefined	
14	Num_Line_Byte1	RW	yes	undefined	
18	BaseOdd2	RW	yes	undefined	Video DMA2 upload
1C	BaseEven2	RW	yes	undefined	
20	ProtAddr2	RW	yes	undefined	
24	Pitch2	RW	yes	undefined	
28	BasePage2	RW	yes	undefined	
2C	Num_Line_Byte2	RW	yes	undefined	
30	BaseOdd3	RW	yes	undefined	Video DMA3 upload
34	BaseEven3	RW	yes	undefined	
38	ProtAddr3	RW	yes	undefined	
3C	Pitch3	RW	yes	undefined	
40	BasePage3	RW	yes	undefined	
44	Num_Line_Byte3	RW	yes	undefined	
48	PCI_BT_V	RW	yes	undefined	Video DMA 1, 2, or 3 upload
4C	PCI_BT_A	RW	read	undefined	immediate write access
50	Initial settings DD1-Port	RW	yes	undefined	D1 Interface upload
54	Video DATA stream handling at port DD1	RW	yes	undefined	
58	BRS control #1 Register	RW	yes	undefined	BRS upload
5C	HPS control	RW	yes	undefined	HPS section 1 upload
60	HPS, Vertical-scale	RW	yes	undefined	HPS section 2 upload
64	HPS, Vertical-scale and gain	RW	yes	undefined	
68	HPS Horizontal-pre-scale	RW	yes	undefined	HPS section 1 upload
6C	HPS Horizontal-fine-scale	RW	yes	undefined	
70	BCS control	RW	yes	undefined	HPS section 2 upload
74	Chroma Key range	RW	yes	undefined	
78	HPS Output and Formats Clip control #1	RW	yes	undefined	

OFFSET (HEX)	NAME	TYPE	RAM	READ VALUE AFTER RESET	CORRESPONDING UPLOAD BIT
7C	DEBI_CONFIG	RW	yes	undefined	DEBI upload
80	DEBI_COMMAND	RW	yes	undefined	
84	DEBI_PAGE	RW	yes	undefined	
88	DEBI_AD	RW	yes	00000000	
8C	IICTFR	RW	yes	xxxxxxx0	I^2C upload
90	IIC_STA	RW	yes	00000000	
94	BaseA1_in	RW	read	undefined	immediate write access
98	ProtA1_in	RW	read	undefined	
9C	PageA1_in	RW	read	undefined	
A0	BaseA1_out	RW	read	undefined	
A4	ProtA1_out	RW	read	undefined	
A8	PageA1_out	RW	read	undefined	
AC	BaseA2_in	RW	read	undefined	
B0	ProtA2_in	RW	read	undefined	
B4	PageA2_in	RW	read	undefined	
B8	BaseA2_out	RW	read	undefined	
BC	ProtA2_out	RW	read	undefined	
C0	PageA2_out	RW	read	undefined	
C4	RPS_PAGE0	RW	read	undefined	
C8	RPS_PAGE1	RW	read	undefined	
CC	RPS_THRESH0	RW	read	undefined	
D0	RPS_THRESH1	RW	read	undefined	
D4	RPS_TOV0	RW	read	undefined	
D8	RPS_TOV1	RW	read	undefined	
DC	IER	RW	read	undefined	
E0	GPIO_CTRL	RW	read	undefined	
E4	EC1SSR	RW	read	undefined	
E8	EC2SSR	RW	read	undefined	
EC	ECT1R	RW	read	undefined	
F0	ECT2R	RW	read	undefined	immediate write access
F4	ACON1	RW	read	undefined	
F8	ACON2	RW	read	undefined	

OFFSET (HEX)	NAME	TYPE	RAM	READ VALUE AFTER RESET	CORRESPONDING UPLOAD BIT
FC	MC1	RW	no	00008100	immediate access
100	MC2	RW	no	00000000	
104	RPS_ADDR0	RW	no	00000000	
108	RPS_ADDR1	RW	no	00000000	
10C	ISR	RW	no	00000000	
110	PSR	R	no	undefined	–
114	SSR	R	no	undefined	
118	EC1R	R	no	00000000	
11C	EC2R	R	no	00000000	
120	PCI_VDP1	R	no	00000000	
124	PCI_VDP2	R	no	00000000	
128	PCI_VDP3	R	no	00000000	
12C	PCI_ADP1	R	no	00000000	
130	PCI_ADP2	R	no	00000000	
134	PCI_ADP3	R	no	00000000	
138	PCI_ADP4	R	no	00000000	
13C	PCI_DDP	R	no	00000000	
140	LEVEL_REP	R	no	00000000	
144	FB_BUFFER1	RW	no	00000000	immediate access
148	FB_BUFFER2	RW	no	00000000	
180-1BC	Audio Time Slot Registers 1	RW	no	no read back	
1C0-1FC	Audio Time Slot Registers 2	RW	no	no read back	

9 BOUNDARY-SCAN TEST

The SAA7146 has built in logic and 5 dedicated pins to support boundary-scan testing which allows board testing without special hardware (nails). The SAA7146 follows the *"IEEE Std. 1149.1 - Standard Test Access Port and Boundary-Scan Architecture"* set by the Joint Test Action Group (JTAG) chaired by Philips.

The 5 special pins are Test Mode Select (TMS), Test Clock (TCK), Test Reset (TRST), Test Data Input (TDI) and Test Data Output (TDO).

The BST functions BYPASS, EXTEST, SAMPLE, CLAMP and IDCODE are all supported (see Table 111). Details about the JTAG BST-TEST can be found in the specification *"EEE Std. 1149.1"*. A file ccontaining the detailed Boundary-Scan Description Language (BSDL) description of the SAA7146 is available on request.

Table 111 BST instructions supported by the SAA7146

INSTRUCTION	DESCRIPTION
BYPASS	This mandatory instruction provides a minimum length serial path (1 bit) between TDI and TDO when no test operation of the component is required.
EXTEST	This mandatory instruction allows testing of off-chip circuitry and board level interconnections.
SAMPLE	This mandatory instruction can be used to take a sample of the inputs during normal operation of the component. It can also be used to preload data values into the latched outputs of the Boundary-Scan Register.
CLAMP	This optional instruction is useful for testing when not all ICs have BST. This instruction addresses the Bypass Register while the Boundary-Scan Register is in external test mode.
IDCODE	This optional instruction will provide information on the components manufacturer, part number and version number.

9.1 Initialization of Boundary-Scan circuit

The TAP controller of an IC should be in the reset state (TEST_LOGIC_RESET) when the IC is in functional mode. This reset state also forces the Instruction Register into a functional instruction such as IDCODE or BTPASS.

To solve the power-up reset, the standard specifies that the TAP controller will be forced asychronously to the TEST_LOGIC_RESET state by setting the TRST pin LOW.

9.2 Device Identification Codes

A Device Identification Register is specified in *"IEEE Std. 1149.1-1990 - IEEE Standard Test Access Port and Boundary-Scan Architecture"*. It is a 32-bit register which contains fields for the specification of the IC manufacturer, the IC part number and the IC version number. Its biggest advantage is the possibilty to check for the correct ICs mounted after production and determination of the version number of ICs during field service.

When the IDCODE instruction is loaded into the BST Instruction Register, the Identification Register will be connected between TDI and TDO of the IC. The Identification Register will load a component specific code during the CAPTURE_DATA_REGISTER state of the TAP ccontroller and this code can subsequently be shifted out. At board level this code can be used to verify component manufacturer, type and version number. The Device Identification Register contains 32-bits, numbered 31 to 0, where bit 31 is the most significant bit (nearest to TDI) and bit 0 is the least significant bit (nearest to TDO); see Fig.34.

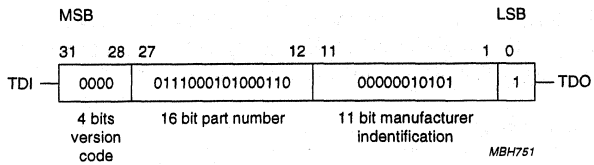


Fig.34 32 bits of identification code.

10 OPERATING CONDITIONS

10.1 Electrical conditions

- Operating time: The circuit is designed to be able to operate continuously
- Backup: No backup capability (standby) will be provided internally
- Handling: Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal handling precautions appropriate to handling MOS devices.

11 CHARACTERISTICS

Power supplies are 3.3 V for the internal core and 5 V for the I/O pad section. T_{amb} = 0 to 70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	digital supply voltage range for I/O section		4.75	5.0	5.25	V
V_{DD3}	digital supply voltage range for internal core		3.0	3.3	3.6	V
I_{DD3V}	3 V digital supply current	video overlay RGB mode	–	400	–	mA
I_{DD5V}	5 V digital supply current	video overlay RGB mode	–	60	–	mA
Data, clock and control inputs						
V_{IL}	LOW-level input voltage					
	clocks		–0.5	–	0.6	V
	other outputs		–0.5	–	0.8	V
V_{IH}	HIGH-level input voltage					
	clocks		2.4	–	V_{DD} + 0.25	V
	other inputs		2.0	–	V_{DD} + 0.25	V
I_{LI}	input leakage current	V_{IL} = 0 V	–	–	1	µA
C_i	input capacitance		–	–	10	pF
Data, clock and control outputs; note 1						
V_{OL}	LOW-level output voltage					
	clocks		0	–	0.6	V
	other outputs	note 2	0	–	0.6	V
V_{OH}	HIGH-level output voltage					
	clocks		2.6	–	V_{DD}	V
	other outputs	note 2	2.4	–	V_{DD}	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I²C-bus, SDA and SCL (pins 176,175)						
V_{IL}	LOW-level input voltage		−0.5	–	1.5	V
V_{IH}	HIGH-level input voltage		3	–	V_{DD} + 0.25	V
$I_{175,176}$	input current		–	–	±10	µA
I_{OL}	LOW-level output current pin 176		3	–	–	mA
V_{OL}	LOW-level output voltage	I_{176} = 3 mA	–	–	0.4	V
Clock input timing (LLC_A and LLC_B); note 3						
t_{LLC_A}, t_{LLC_B}	cycle time		31	–	45	ns
δ	duty factor	t_{LLCH}/t_{LLC}	40	50	60	%
t_r	rise time		–	–	5	ns
t_f	fall time		–	–	6	ns
Data and control input timing; note 3						
t_{SU}	set-up time		6	–	–	ns
t_{HD}	hold time		3	–	–	ns
Clock output timing (LLC_A, LLC_B); note 3						
C_L	output load capacitance		15	–	40	pF
t_{LLC_A}, t_{LLC_B}	cycle time		31	–	45	ns
δ	duty factor	t_{LLCH}/t_{LLC}	40	50	60	%
t_r	rise time	0.6 to 2.6 V	–	–	5	ns
t_f	fall time	2.6 to 0.6 V	–	–	5	ns
Data and control output timing; note 3						
C_L	load capacitance		15	–	40	pF
t_{OH}	output hold time	C_L = 15 pF	4	–	–	ns
t_{pd}	propagation delay from positive edge of LLC_A, LLC_B	C_L = 40 pF	–	–	25	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PCI I/O signals						
DC SPECIFICATION						
V_{IH}	HIGH-level input voltage		2.0	–	V_{DD} + 0.25	V
V_{IL}	LOW-level input voltage		−0.5	–	0.8	V
I_{LIH}	HIGH-level input leakage current HIGH	V_i = 2.7 V; note 1	–	–	70	μA
I_{LIL}	LOW-level input leakage	V_i = 0.5 V; note 1	–	–	−70	μA
V_{OH}	HIGH-level output voltage	I_o = −2 mA	2.4	–		V
V_{OL}	LOW-level output voltage	I_o = 3 mA and 6 mA; note 4	–	–	0.55	V
C_i	input pin capacitance		–	–	10	pF
C_{CLK}	CLK pin capacitance		5	–	12	pF
C_{IDSEL}	IDSEL pin capacitance	note 5	–	–	8	pF
AC SPECIFICATION						
$I_{OH(AC)}$	switching current HIGH	$0 < V_o \leq 1.4$; note 6	−44	–		mA
		$1.4 < V_o < 2.4$; note 6	$-44 + (V_o - 1.4)/0.024$	–		mA
		$3.1 < V_o < V_{CC}$; note 6	–	–	note 7	
	test point	V_o = 3.1 V; notes 7 and 8	–	–	−142	mA
$I_{OL(AC)}$	switching current LOW	$V_o > 2.2$ V; note 6	95	–		mA
		$2.2 > V_o > 0.55$; note 6	$V_o/0.023$	–		mA
		$0.71 > V_o > 0$; note 6	–	–	note 8	
	test point	V_o = 0.71 V; notes 7 and 8	–	–	206	mA
t_{slewr}	output rise slew rate	0.4 to 2.4 V; note 9	1	–	5	V/ns
t_{slewf}	output fall slew rate	2.4 to 0.4 V; note 9	1	–	5	V/ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing parameters						
t_{val}	CLK to signal valid delay - bussed signals	notes 10 and 11	2	–	11	ns
$t_{val(ptp)}$	CLK to signal valid delay - point-to-point	notes 10 and 11	2	–	12	ns
t_{on}	float to active delay	notes 11 and 12	2	–	–	ns
t_{off}	active to float delay	notes 11 and 12	–	–	28	ns
t_{su}	input set-up time to CLK - bussed signal	notes 10 and 11	7	–	–	ns
$t_{su(ptp)}$	input set-up time to CLK - point-to-point	notes 10 and 11	10, 12	–	–	ns
t_h	input hold time from CLK	note 11	0	–	–	ns
$t_{rst-CLK}$	reset active time after CLK stable	note 13	100	–	–	µs
$t_{rst-off}$	reset active to output float delay	notes 12, 13 and 14	–	–	40	ns

Notes to the characteristics

1. Input leakage currents include high-impedance output leakage for all bidirectional buffer with 3-state outputs.
2. Levels measured with load circuit: 1.2 kW at 3 V (TTL load) and C_L = 40 pF.
3. See clock and data timing in Fig.35.
4. FRAME#, TRDY#, IRDY#, DEVSEL# and STOP#.
5. Lower capacitance on this input only pin allows for non-resistive coupling to AD(xx).
6. Refer to the V/I curves in PCI specification. 'Switching current high' specifications are not relevant to INTA#, which are open-drain outputs.
7. $I_{OH(AC)} = 11.9 \times (V_o - 5.25) \times (V_o + 2.45)$ for $V_{DD} > V_o > 3.1$ V.
8. $I_{OL(AC)} = 78.5 \times V_o \times (4.4 - V_o)$ for $0 V < V_o < 0.71$ V.
9. This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range.
10. REQ# and GNT# are point-to-point signals, and have different output valid delay and input set-up times that do bussed signals. GNT# has a set-up of 10 ns. REQ# has a set-up of 12 ns. All other signals are bussed.
11. See input and output timing measurement conditions in Fig.36.
12. For purposes of active/float timing measurements the high-impedance or 'off' state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
13. RST# is asserted and deasserted asynchronously with respect to CLK.
14. All output drivers floated asynchronously when RST# is active.

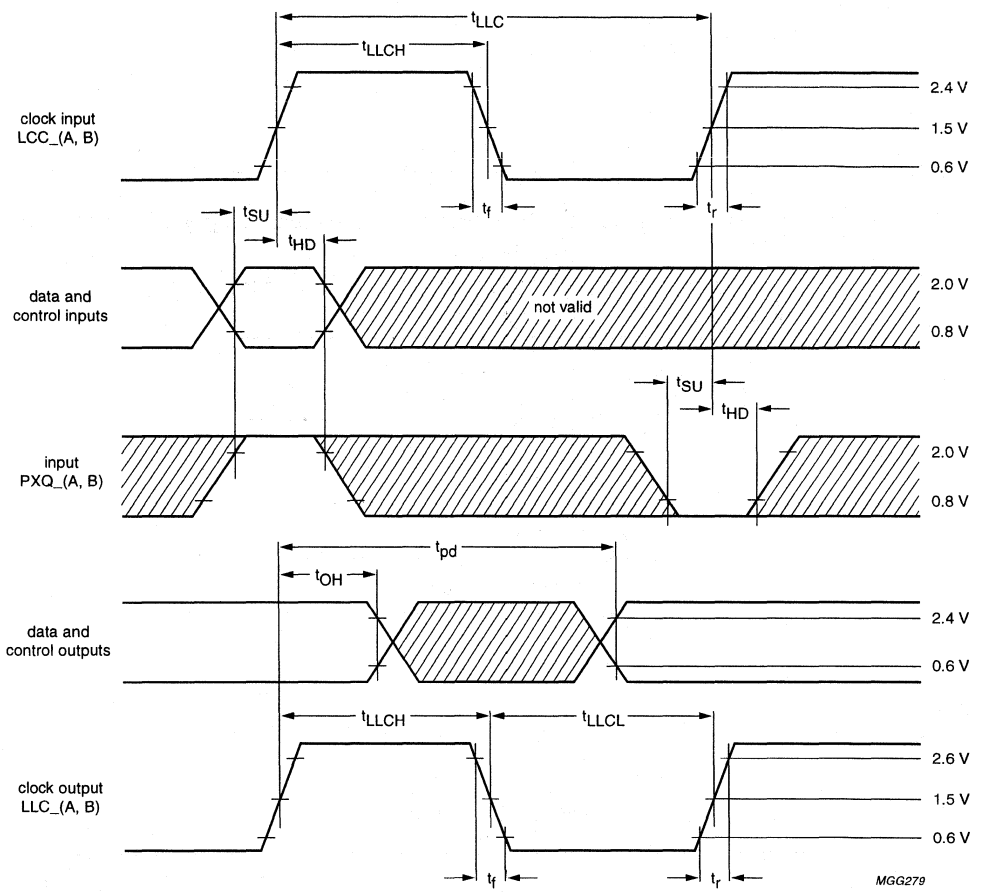


Fig.35 Clock/Data timing.

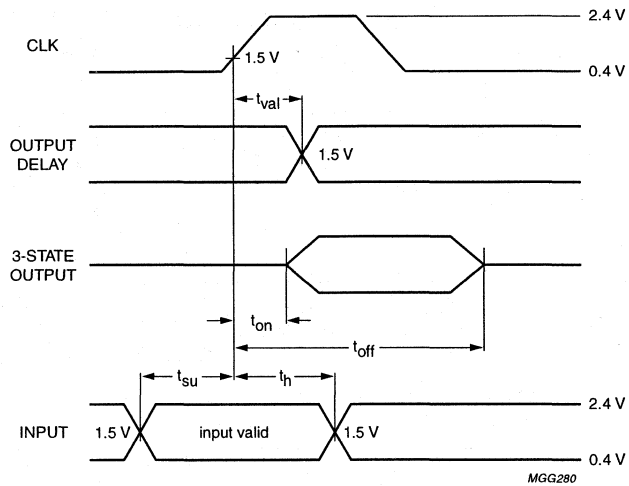
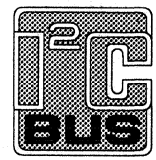


Fig.36 PCI I/O timing.

Digital Multistandard Colour Decoder with SCART interface (DMSD2-SCART)

SAA7151B



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Digital Multistandard Colour Decoder with SCART interface (DMSD2-SCART)

SAA7151B

1. FEATURES

- 8-bit performance on chip for luminance and chrominance signal processing for PAL, NTSC and SECAM standards
- Separate 8-bit luminance and 8-bit chrominance input signals from Y/C, CVBS, S-Video (S-VHS or Hi8) sources
- SCART signal insertion by means of RGB/YUV convertion; fast switch handling
- Horizontal and vertical sync detection for all standards
- Real time control output RTCO
- Fast sync recovery of vertical blanking for VCR signals (bottom flutter compensation)
- Controls via the I^2C-bus
- User programmable aperture correction (horizontal peaking)
- Cross-colour reduction by chrominance comb-filtering (NTSC) or by special cross-colour cancellation (SECAM)
- 8-bit quantization of output signals in 4:1:1 or 4:2:2 formats
- 720 active samples per line
- The YUV bus supports a data rate of 13.5 MHz (CCIR 601).
  - (864 x f_H) for 50 Hz
  - (858 x f_H) for 60 Hz
- Compatible with memory-based features (line-locked clock)
- One 24.576 MHz crystal oscillator for all standards

2. GENERAL DESCRIPTION

The SAA7151B is a digital multistandard colour-decoder having two 8-bit input channels, one for CVBS or Y, the other for chrominance or time-multiplexed colour-difference signals.

3. QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage (pins 5, 18, 28, 37 and 52)	4.5	5	5.5	V
I_{DD}	total supply current (pins 5, 18, 28, 37 and 52)	-	100	250	mA
V_I	input levels	TTL-compatible			
V_O	output levels	TTL-compatible			
T_{amb}	operating ambient temperature	0	-	70	°C

4. ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7151B	68	mini-pack PLCC	plastic	SOT188-2

5. BLOCK DIAGRAM

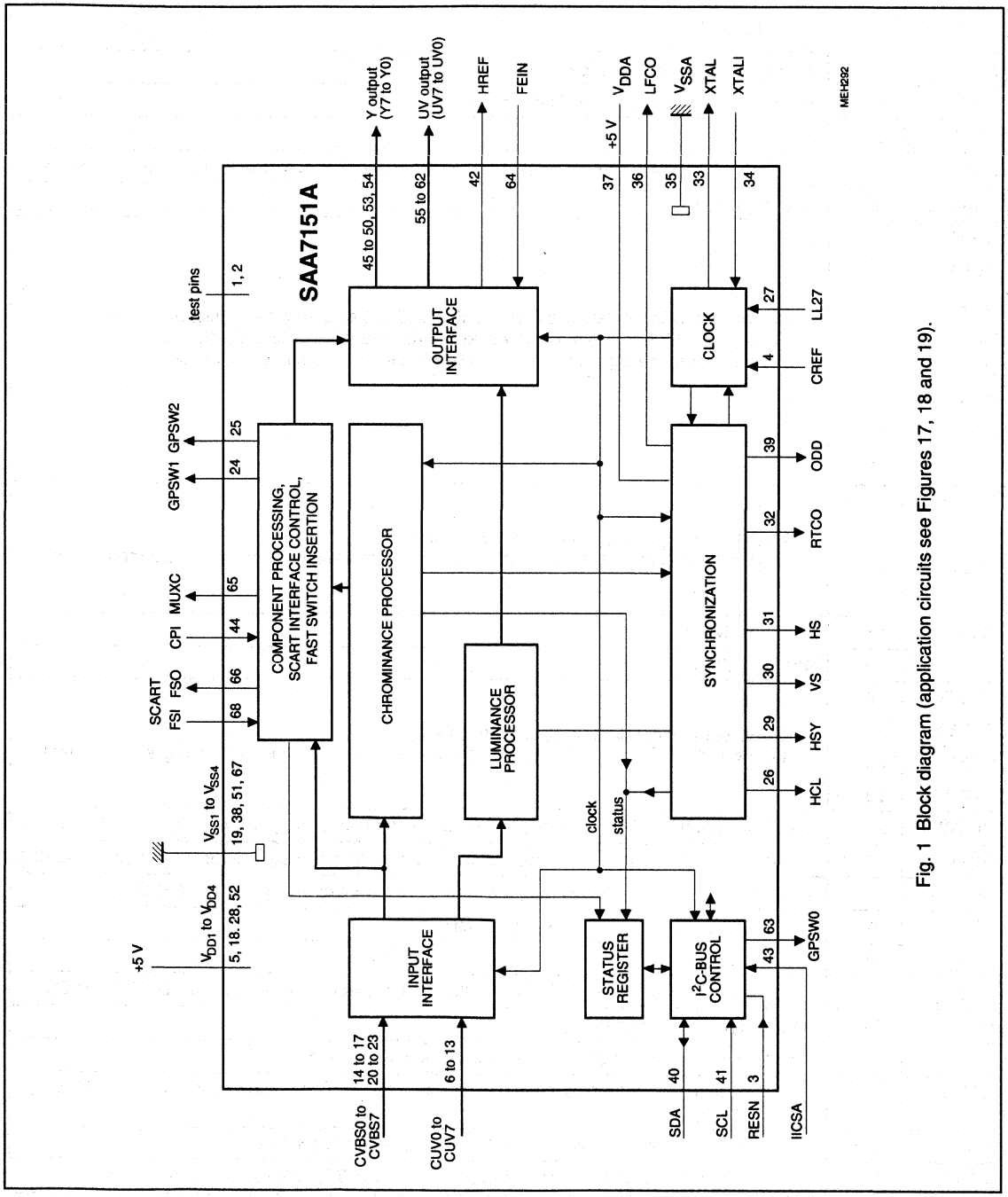


Fig. 1 Block diagram (application circuits see Figures 17, 18 and 19).

6. PINNING

SYMBOL	PIN	DESCRIPTION
SP	1	connected to ground (shift pin for testing)
AP	2	connected to ground (action pin for testing)
RESN	3	reset, active-LOW
CREF	4	clock reference, sync from external to ensure in-phase signals on the Y-, CUV- and YUV-bus
V_{DD1}	5	+5 V supply input 1
CUV0	6	chrominance input data bits CUV7 to CUV0 (digitized chrominance signals in two´s complement format from a S-Video source (S-VHS, Hi8) or time-multiplexed colour-difference signals from a YUV(RGB) source or both in combination)
CUV1	7	
CUV2	8	
CUV3	9	
CUV4	10	
CUV5	11	
CUV6	12	
CUV7	13	
CVBS0	14	CVBS lower input data bits CVBS3 to CVBS0 (CVBS with luminance, chrominance and all sync information in two´s complement format)
CVBS1	15	
CVBS2	16	
CVBS3	17	
V_{DD2}	18	+5 V supply input 2
V_{SS1}	19	ground 1 (0 V)
CVBS4	20	CVBS upper input data bits CVBS7 to CVBS4 (CVBS with luminance, chrominance and all sync information in two´s complement format)
CVBS5	21	
CVBS6	22	
CVBS7	23	
GPSW1	24	status bit output FSST0 or port 1 output for general purpose (programmable by subaddress 0C)
GPSW2	25	status bit output FSST1 or port 2 output for general purpose (programmable by subaddress 0C)
HCL	26	black level clamp pulse output (begin and stop programmable), e.g. for TDA8708A (ADC)
LL27	27	line-locked system clock input signal (27 MHz)
V_{DD3}	28	+5 V supply input 3
HSY	29	hor. sync pulse reference output (begin and stop programmable), e.g. for gain adj.TDA8708A (ADC)
VS	30	vertical sync output signal (Fig.10)
HS	31	horizontal sync output signal (Fig.14; start point programmable)
RTCO	32	real time control output; serial increments of HPLL and FSCPLL and status PAL or SECAM sequence (Fig.9)
XTAL	33	24.576 MHz clock output (open-circuit for use with external oscillator)
XTALI	34	24.576 MHz connection for crystal or external oscillator (TTL compatible squarewave)

SYMBOL	PIN	DESCRIPTION
V_{SSA}	35	analog ground
LFCO	36	line frequency control output signal, multiple of horizontal frequency (nominal 6.75 MHz)
V_{DDA}	37	+5 V supply input for analog part
V_{SS2}	38	ground 2 (0 V)
ODD	39	odd/even field identification output (odd = HIGH)
SDA	40	I^2C-bus data line
SCL	41	I^2C-bus clock line
HREF	42	horizontal reference for YUV data outputs (for active line 720Y samples long)
IICSA	43	set module address input of I^2C-bus (LOW = 1000 101X; HIGH = 1000 111X)
CPI	44	clamping pulse input (digital clamping of external UV signals)
Y7	45	Y signal output bits Y7 to Y2 (luminance), part of the digital YUV-bus
Y6	46	
Y5	47	
Y4	48	
Y3	49	
Y2	50	
V_{SS3}	51	ground 3 (0 V)
V_{DD4}	52	+5 V supply input 4
Y1	53	Y signal output bits Y1 to Y0 (luminance), part of the digital YUV-bus
Y0	54	
UV7	55	UV signal output bits UV7 to UV0, part of the digital YUV-bus
UV6	56	
UV5	57	
UV4	58	
UV3	59	
UV2	60	
UV1	61	
UV0	62	
GPSW0	63	port output for general purpose (programmable by subaddress 0D)
FEIN	64	fast enable input (active-LOW to control fast switching due to YUV data; HIGH = YUV high-Z
MUXC	65	multiplexer control output; source select signal for external ADC (UV signal multiplexing)
FSO	66	fast switch and sync insertion output; gated FS signal from FSI or sync insertion pulse in full screen RGB mode
V_{SS4}	67	ground 4 (0 V)
FSI	68	fast switch input signal fed from SCART/peri-TV connector (indicates fast insertion of RGB signals)

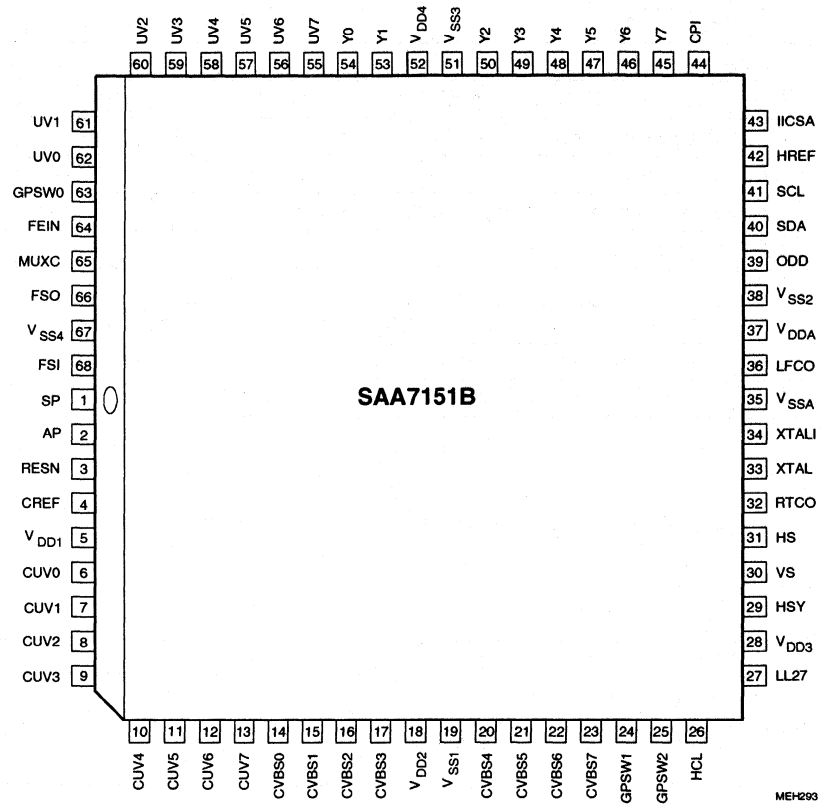


Fig.2 Pin configuration.

7. FUNCTIONAL DESCRIPTION

System configuration

The SAA7151B system processes digital TV signals with line-locked clock in PAL, SECAM and NTSC standards (CVBS or S-Video) as well as RGB signals coming from a SCART/peri-TV connector. The different source signals are switched, if necessary matrixed and converted (Fig.3 and Table 1).
8-bit CVBS data (digitized composite video) and 8-bit UV data (digitized chrominance and/or time-multiplexed colour-difference signals) are fed to the SAA7151B. The data rate is 27 MHz.

Chrominance processing

The 8-bit chrominance input signal (signal "C" out of CVBS or Y/C in Fig.4a) is fed via the input interface to a bandpass filter for eliminating the DC component, then to the quadrature demodulator. Subcarrier signals from the local oscillator (DTO1) with 90 degree phase shift are applied to its multiplier inputs. The frequency depends on set TV standard.

The multipliers operate as a quadrature demodulator for all PAL and NTSC signals; it operates as a frequency down-mixer for SECAM signals.
The two multiplier output signals are converted to a serial UV data stream and applied to two low-pass filter stages, then to a gain controlled amplifier. A final multiplexed low-pass filter achieves, together with the preceding stages, the required bandwidth performance.
The from PAL and NTSC originated signals are applied to a comb-filter. The signals, originated from SECAM, are fed through a cloche filter (0 Hz centre frequency), a phase demodulator and a differentiator to obtain frequency-demodulated colour-difference signals.

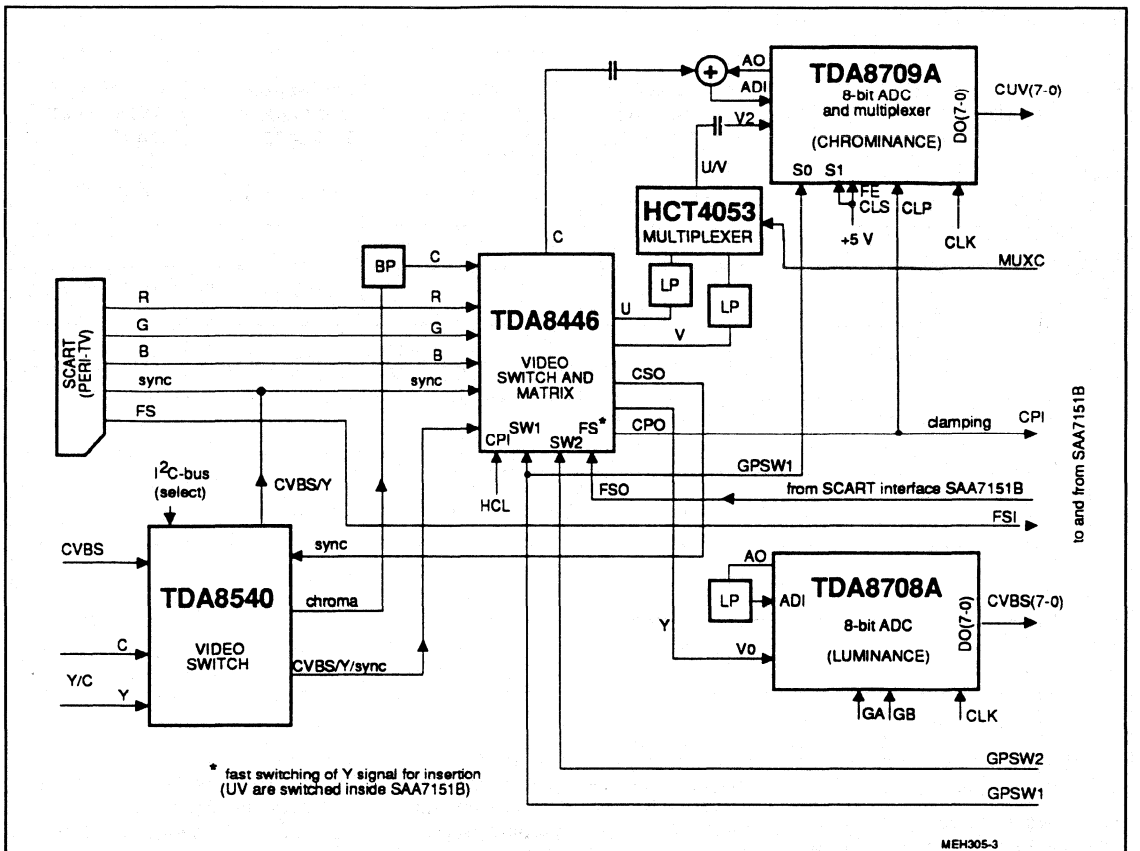


Fig.3 System configuration, RGB fast switch interface included (SCART).

The SECAM signals are fed after de-emphasis to a cross-over switch, to provide the both serial-transmitted colour-difference signals. These signals are finally fed via the fast switch to the output formatter stages and to the output interface. Chrominance signals are output in parallel (4:2:2) on the YUV-bus. The data rate of Y signal (pixel rate) is 13.5 MHz. UV signals have a data rate of 13.5 MHz/2 for the 4:2.2 format (Table 2) respectively 13.5 MHz/4 for the 4:1.1 format (Table 3)

Component processing and SCART interface control

The 8-bit multiplexed colour-difference input signal (signal CUV, Fig.1, out of matrixed RGB in Fig.3) is fed via the input interface to a chrominance stop filter (UV signal only can pass through; Figures 20 to 22). Here it is clamped and fed to the offset compensation which can be enabled or disabled via the I²C-bus.

For matrixed RGB signals – the full screen SCART mode and the fast insertion mode (blanking/switching) are selectable. The chrominance stop filter is automatically bypassed in full screen SCART mode.

Full screen RGB mode (SCART):

The CUV digital input signal (7-0) consists of time-multiplexed samples for U and V. An offset correction for both signals is applied to correct external clamping errors. An internal timing correction compensates for slight differences in timing during sampling. The U and V signals are delay-compensated and fed to the output formatter. The format 4:2:2 or 4:1:1 is generated by a switchable filter.

The control signals for the front end (Figures 3 and 18) MUXC, status bits FSST1, FSST0 (outputs GPSW2, GPSW1) and FSO are generated by the SAA7151B.

Table 1 SCART interface control (Fig.3)

MODE	CONNECTION FSO	GPSW 2	GPSW 1	MUXC	chroma output of TDA8446 to TDA8709A	TDA8709A selected input	CUV (7-0)	luminance fast switch TDA8446	input selector (via I²C-bus) TDA8540
RGB only	0	0	0	0	high-Z	VIN2	U/V	sync (RGB)	sync (RGB)
	0	0	0	1					
Y/C or CVBS only	0	0	1	0	C	VIN1	C	Y (Y/C) or CVBS	Y (Y/C) or CVBS
	0	0	1	1					
Fast switch	0	1	0	0	C	VIN2	0.5(C+U)/ 0.5(C+V)	Y (Y/C) or CVBS	Y (Y/C) or CVBS
	0	1	0	1					
	0	1	1	0	not used				
	0	1	1	1					
RGB only	1	0	0	0	high-Z	VIN2	U/V	Y (RGB)	sync (RGB)
	1	0	0	1					
	1	0	1	0	not used				
	1	0	1	1					
Fast switch	1	1	0	0	C	VIN2	0.5(C+U)/ 0.5(C+V)	Y (RGB)	Y (Y/C) or CVBS
	1	1	0	1					
	1	1	1	0	not used				
	1	1	1	1					

Fast insertion mode:

Fast insertion is applied by FSI pulse to ensure correct timing. The RGB source signal is matrixed into UV and inserted into the CVBS or Y/C source signal after two field periods if FSI pulses are received. The output FSO is set to HIGH during a determined insertion window (screen plain minus 6 % of horizontal and vertical deflection). Switch over depends on the phase of FSI in relation to the valid pixel sequence depending on the phase-different weighting factors. They are applied to the original and the inserted UV data (Figures 5 and 6)
The control signals for the front end (Table 1) MUXC, FSO, status bits FSST1 and FSST0 (outputs GPSW2 and GPSW1) are generated by the SAA7151B .

The amplitude of chrominance and colour-difference signals are scaled down by factor 2 to avoid overloading of the chrominance analog-to-digital converter. The amplitudes are reduced in the TDA8446 by signals on lines GPSW2 and GPSW1.

Luminance processing

The luminance input signal, a digital CVBS format or an 8-bit luminance format (S-Video), is fed through a sample rate converter to reduce the data rate to 13.5 MHz (Fig.4b).

Sample rate is converted by means of a switchable pre-filter. High frequency components are emphasized to compensate for loss in the following chrominance trap filter. This chrominance trap filter (f_0 = 4.43 MHz or f_0 = 3.58 MHz centre frequency selectable) eliminates the most of the colour carrier signal, therefore, it must be bypassed for S-Video signals.

The high frequency components of the luminance signal can be "peaked" in two bandpass filters with selectable transfer characteristic. A coring circuit (±1 LSB) can improve the signal , this signal is then added to the original signal. A switchable amplifier achieves a common DC amplification, because the DC gains are different in both chrominance trap modes. Additionally, a cut-off sync pulse is generated for the original signal in both modes.

Synchronization

The luminance output signal is fed to the synchronization stage. Its bandwidth is reduced to 1 MHz in a low-pass filter (sync pre-filter). The sync pulses are sliced and fed to the phase detectors to be compared with the sub-divided clock frequency. The resulting output signal is applied to the loop filter to

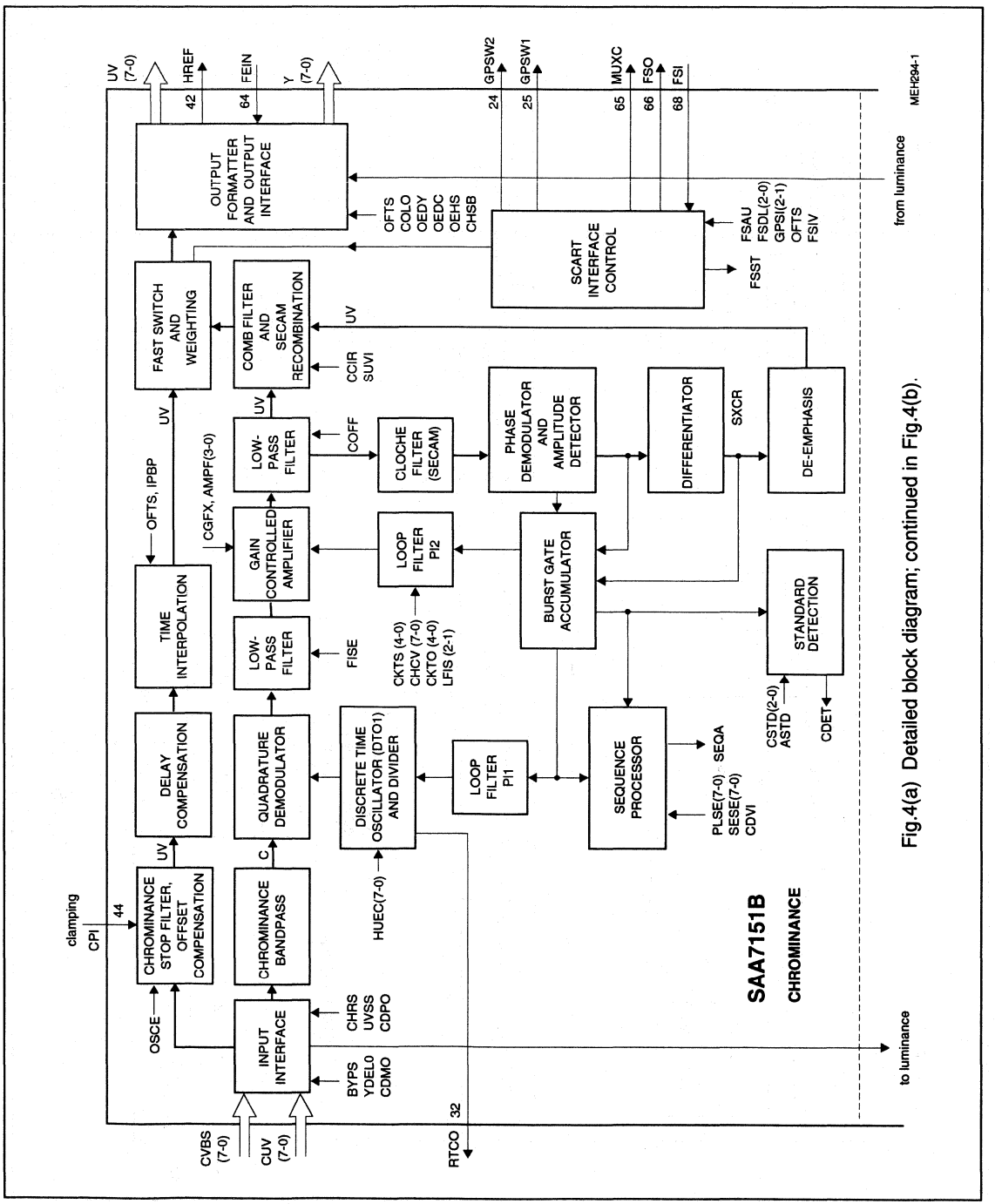


Fig.4(a) Detailed block diagram; continued in Fig.4(b).

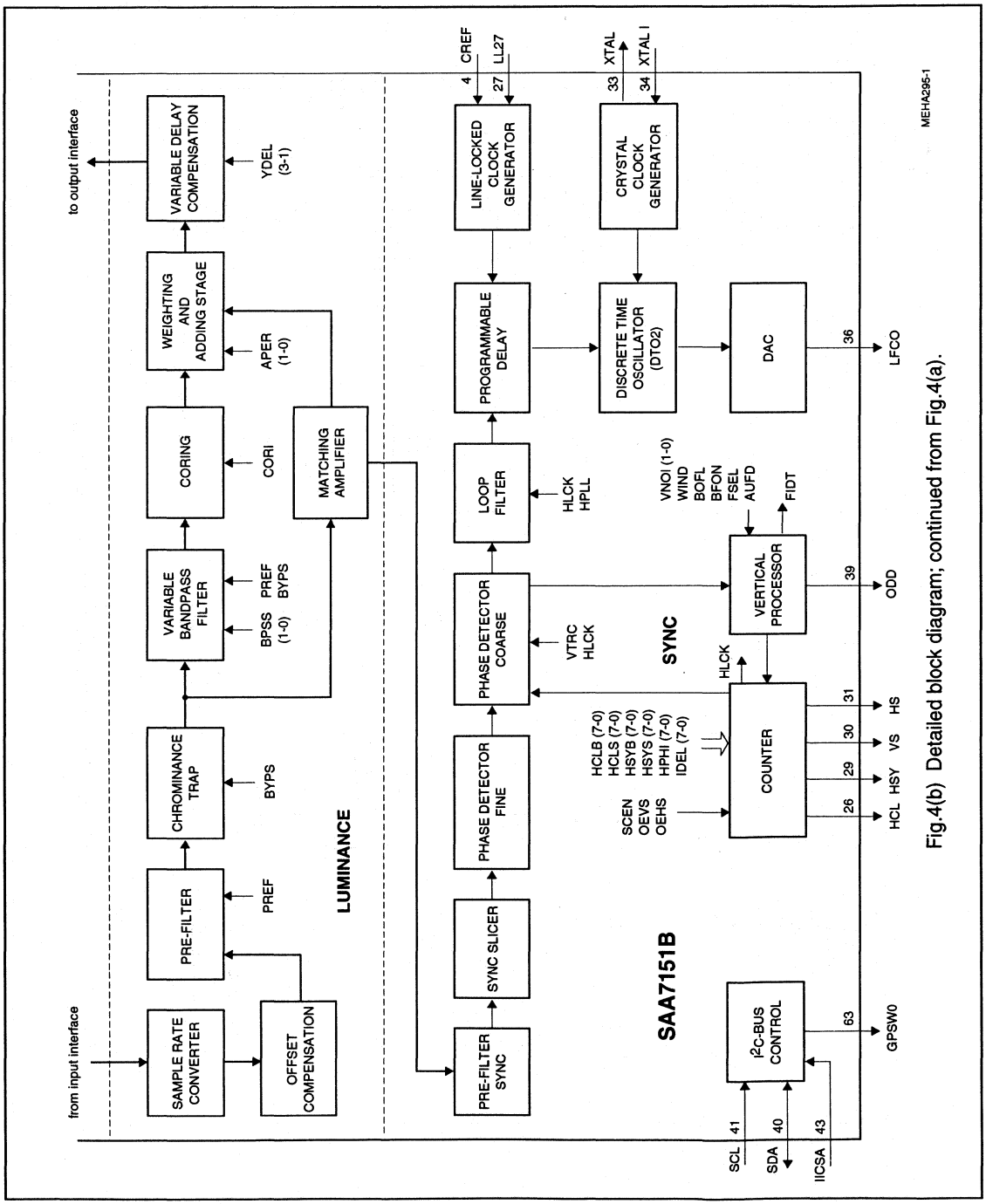


Fig.4(b) Detailed block diagram; continued from Fig.4(a).

accumulate all phase deviations. There are three groups of output timing signals:

a. signals related to data output signals (HREF)
b. signals related to the input signals (HSY, and HCL)
c. signals related to the internal sync phase

All horizontal timings are derived from the main counter, which represents the internal sync phase. The HREF signal only with its critical timing is phase-compensated in relationship to the data output signal. Future circuit improvements could slightly influence the processing delays of some internal stages to achieve a changed timing due to the timing groups b and c.
The HREF signal only controls the data multiplexer phase and the data output signals.

All timings of the following diagrams are measured with nominal input signals, for example coming from a pattern generator. Processing delay times are taken between input and data output, respectively between internal sync reference (main counter = 0) and the rising edge of HREF.

Line locked clock frequency

LFCO is required in an external PLL (SAA7157) to generate the line-locked clock frequency LL27 and CREF.

YUV-bus, digital outputs

The 16-bit YUV-bus transfers digital data from the output interfaces to a feature box, or to the digital-to-analog converter (DAC). Outputs are controlled via the I^2C-bus in normal selections, or they are controlled by output enable chain (FEIN, pin 64). The YUV-bus data rate 13.5 MHz. Timing is achieved by marking each second positive rising edge of the clock LL27 synchronized by CREF.

YUV-bus formats
4 : 2 : 2 and 4 : 1 : 1

The output signals Y7 to Y0 are the bits of the digital luminance signal. The output signals UV7 to UV0 are the bits of the digital colour-difference signal. The frames in the Tables 2 and 3 are the time to transfer a full set of samples. In case of 4 : 2 : 2 format two luminance samples are transmitted in comparision to one U and one V sample within one frame. The time frames are controlled by the HREF signal, which determines the correct UV data phase. The YUV data outputs can be enabled or set to 3-state position by means of the FEIN signal. FEIN = LOW enables the output; HIGH on this pin forces the Y and U/V outputs to a high-impedance state (Fig,5).

Table 2 for the 4 : 2 : 2 format (720 pixels per line). The quoted frequencies are valid on the YUV-bus. The time frames are controlled by the HREF signal.

OUTPUT	PIXEL BYTE SEQUENCE					
Y0 (LSB)	Y0	Y0	Y0	Y0	Y0	Y0
Y1	Y1	Y1	Y1	Y1	Y1	Y1
Y2	Y2	Y2	Y2	Y2	Y2	Y2
Y3	Y3	Y3	Y3	Y3	Y3	Y3
Y4	Y4	Y4	Y4	Y4	Y4	Y4
Y5	Y5	Y5	Y5	Y5	Y5	Y5
Y6	Y6	Y6	Y6	Y6	Y6	Y6
Y7 (MSB)	Y7	Y7	Y7	Y7	Y7	Y7
UV0 (LSB)	U0	V0	U0	V0	U0	V0
UV1	U1	V1	U1	V1	U1	V1
UV2	U2	V2	U2	V2	U2	V2
UV3	U3	V3	U3	V3	U3	V3
UV4	U4	V4	U4	V4	U4	V4
UV5	U5	V5	U5	V5	U5	V5
UV6	U6	V6	U6	V6	U6	V6
UV7(MSB)	U7	V7	U7	V7	U7	V7
Y frame	0	1	2	3	4	5
UV frame	0		2		4	

Table 3 for the 4 : 1 : 1 format (720 pixels per line). The quoted frequencies are valid on the YUV-bus. The time frames are controlled by the HREF signal.

OUTPUT	PIXEL BYTE SEQUENCE							
Y0 (LSB)	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0
Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1
Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2
Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3
Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4
Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5
Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6
Y7 (MSB)	Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7
UV0 (LSB)	0	0	0	0	0	0	0	0
UV1	0	0	0	0	0	0	0	0
UV2	0	0	0	0	0	0	0	0
UV3	0	0	0	0	0	0	0	0
UV4	V6	V4	V2	V0	V6	V4	V2	V0
UV5	V7	V5	V3	V1	V7	V5	V3	V1
UV6	U6	U4	U2	U0	U6	U4	U2	U0
UV7 (MSB)	U7	U5	U3	U1	U7	U5	U3	U1
Y frame	0	1	2	3	4	5	6	7
UV frame	0				4			

Signal levels (Figures 11 and 12)

The nominal input and output signal levels are defined by a colour bar signal with 75 % colour, 100 % saturation and 100 % luminance amplitude (EBU colour bar).

CUV-bus input format

The CUV-bus transfers the digital chrominance/colour-difference signals from the ADC to the SAA7151B (Fig.5; Table 1):

- normal mode for digital chrominance transmission.
- UV colour-difference mode for colour-difference signals UV (out of matrixed RGB signals)
- FS mode (fast switch mode; UV inserted into chrominance signal C with addition of the two signal spectra).

RTCO output

The RTCO output signal (Fig.9) contains serialized information about actual clock frequency, subcarrier frequency and PAL/SECAM sequence. This signal may preferably be used with the frequency-locked digital video encoder SAA7199B.

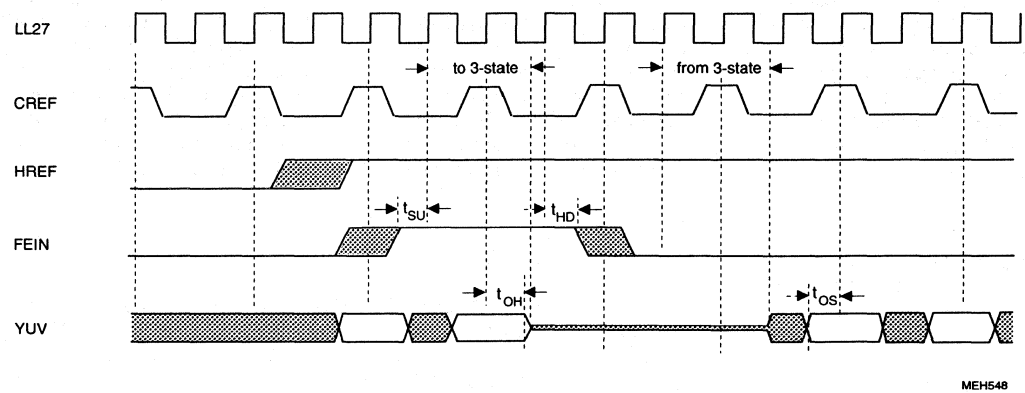


Fig.5 Timing example of fast enable input (FEIN).

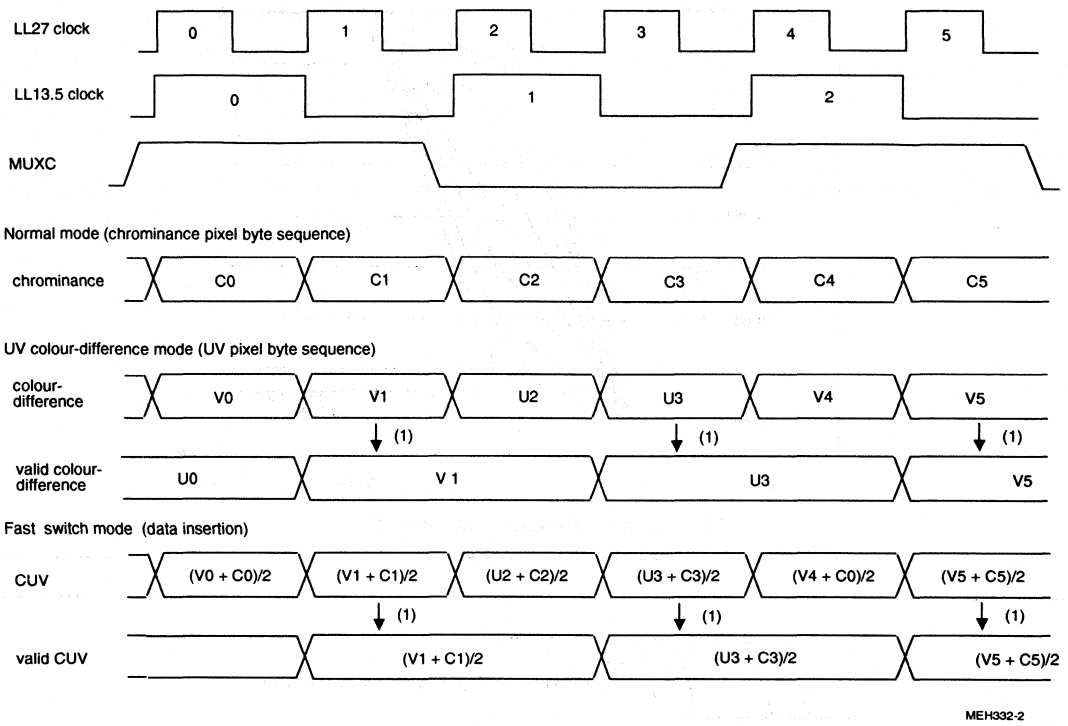


Fig.6 CUV input formats.
(1) each second sample only after a MUXC change is taken for down-sampling to 13.5 MHz to reduce cross-talk components between U and V signals.

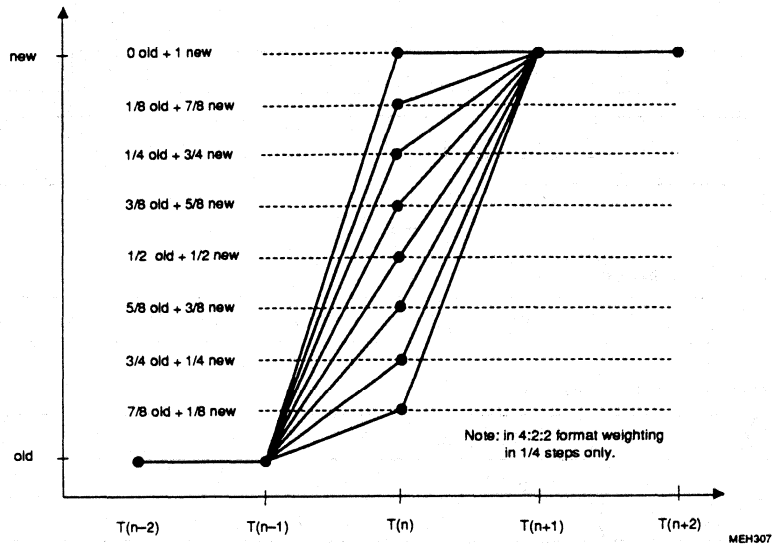


Fig.7 Addition of weighted components.

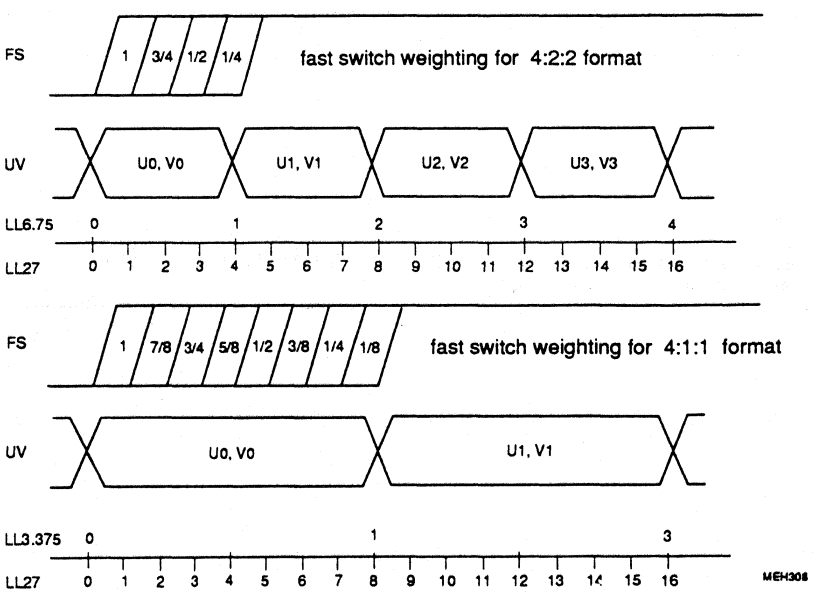


Fig.8 Weighting factors of fast switching for 4:2:2 and 4:1:1 formats.

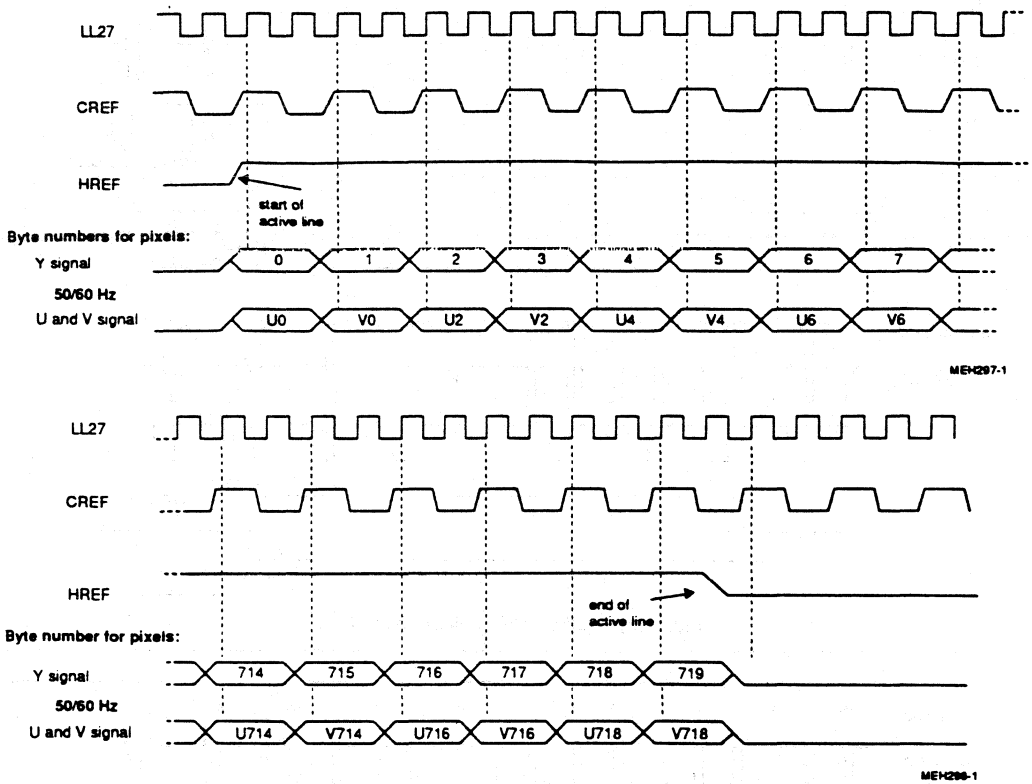
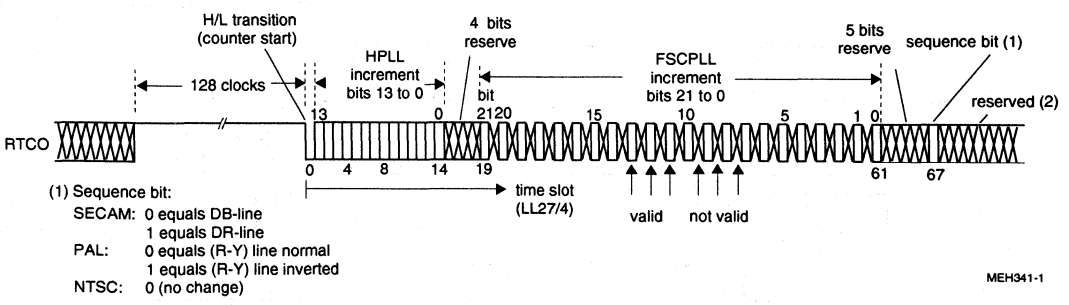


Fig.9 Line control by HREF in 4:2:2 format for 50 Hz and 60 Hz systems.



(1) Sequence bit:
SECAM: 0 equals DB-line
1 equals DR-line
PAL: 0 equals (R-Y) line normal
1 equals (R-Y) line inverted
NTSC: 0 (no change)

(2) Reserve bits: 236 for 50 Hz systems; 233 for 60 Hz systems.

Fig.10 RTCO timing.

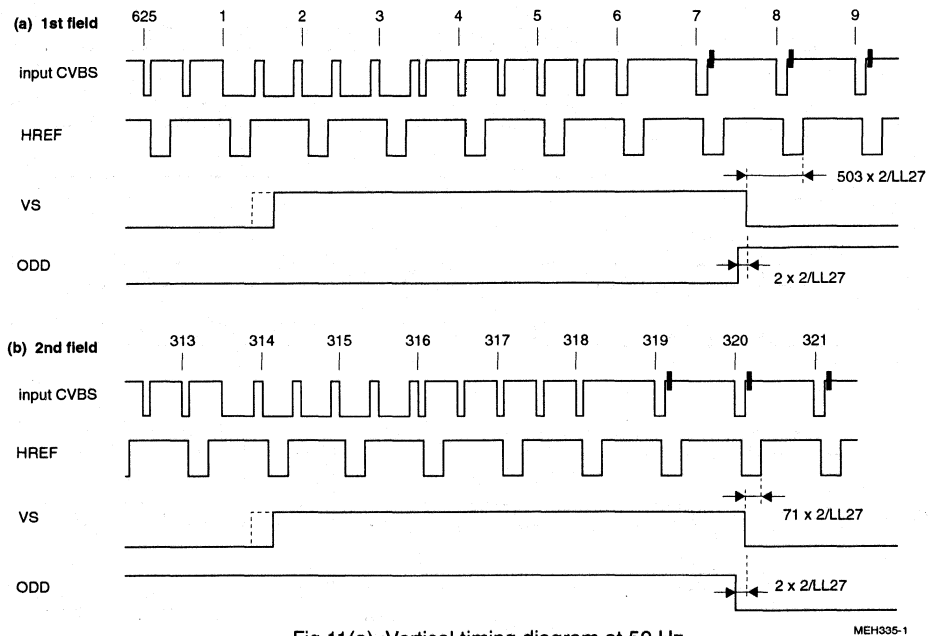


Fig.11(a) Vertical timing diagram at 50 Hz.

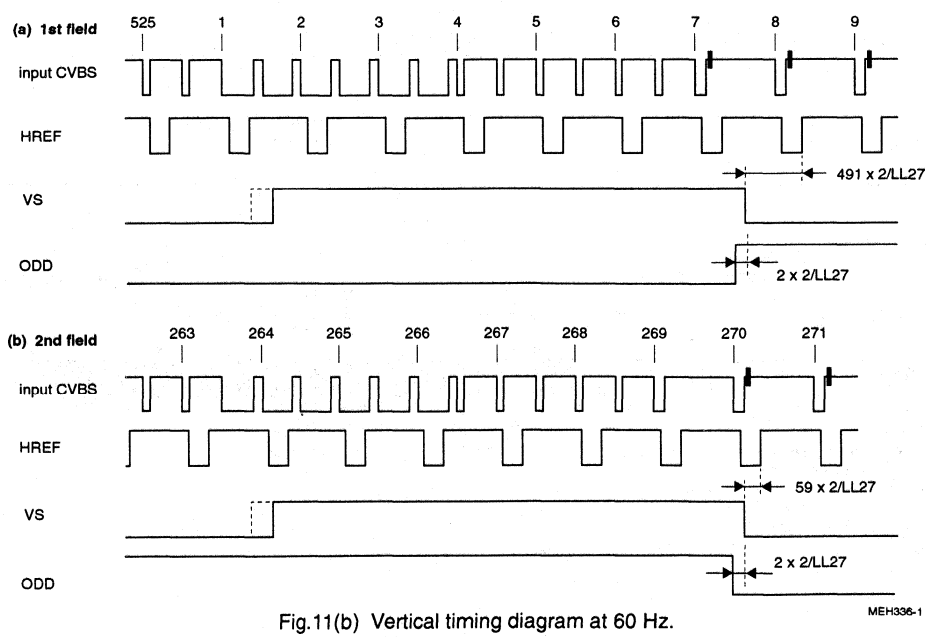
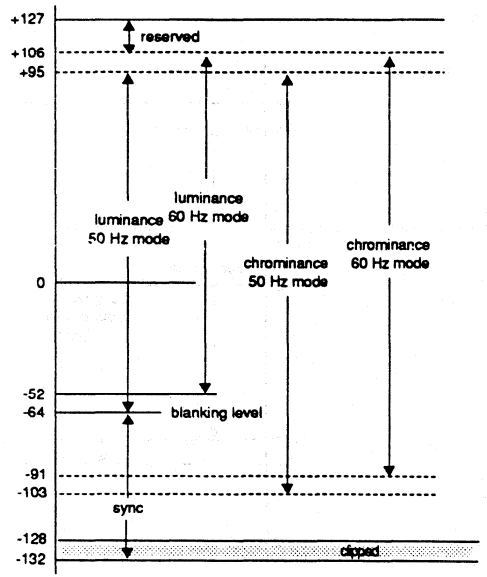
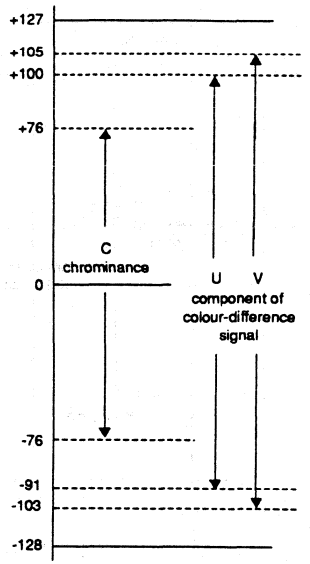


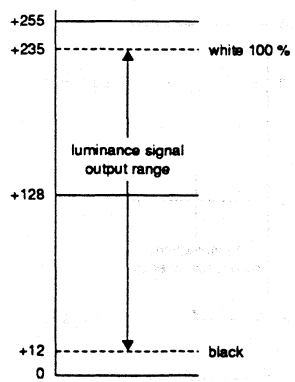
Fig.11(b) Vertical timing diagram at 60 Hz.



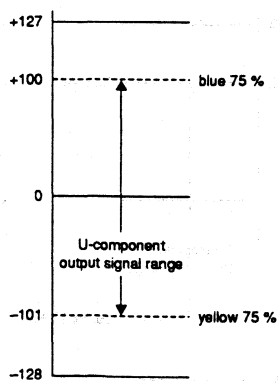
(a) CVBS input signal range.



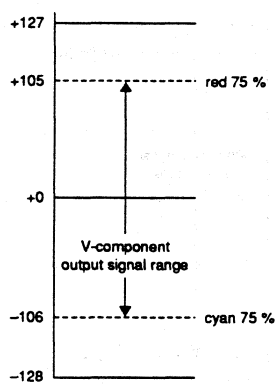
(b) CUV input signal range (U and V out of RGB; in FS mode ranges x 0.5).



(c) Y output signal range.



(d) U output signal range (B-Y).



(e) V output signal range (R-Y).

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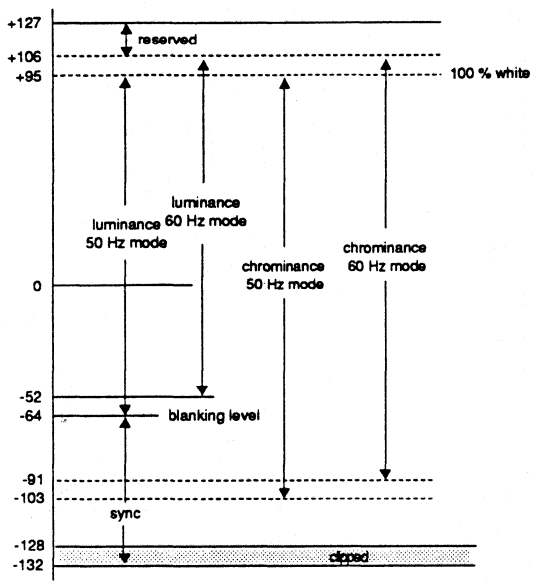
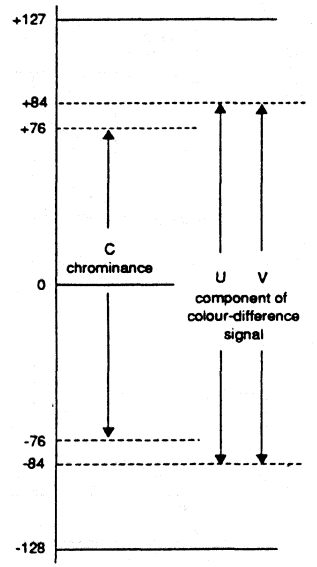
Notes: 1. All levels are related to EBU colour bar.
2. Values in decimal at 100 % luminance and 75 % chrominance amplitude.

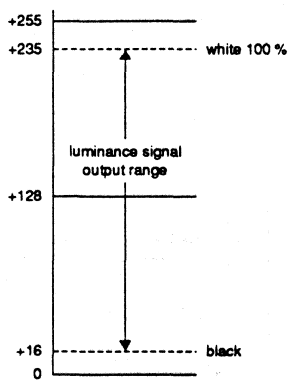
Fig.12 Input and output signal ranges in DTV mode (digital TV).



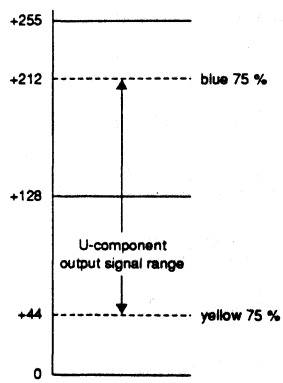
(a) CVBS input signal range.



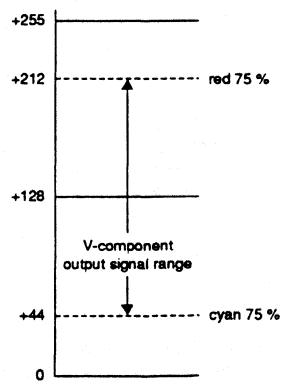
(b) CUV input signal range (U and V out of RGB; in FS mode ranges x 0.5).



(c) Y output signal range.



(d) U output signal range (B-Y).



(e) V output signal range (R-Y).

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Notes: 1. All levels are related to EBU colour bar.
2. Values in decimal at 100 % luminance and 75 % chrominance amplitude.
3. For SECAM input signals the CCIR levels will be exceeded.

Fig.13 Input and output signal ranges in CCIR mode.

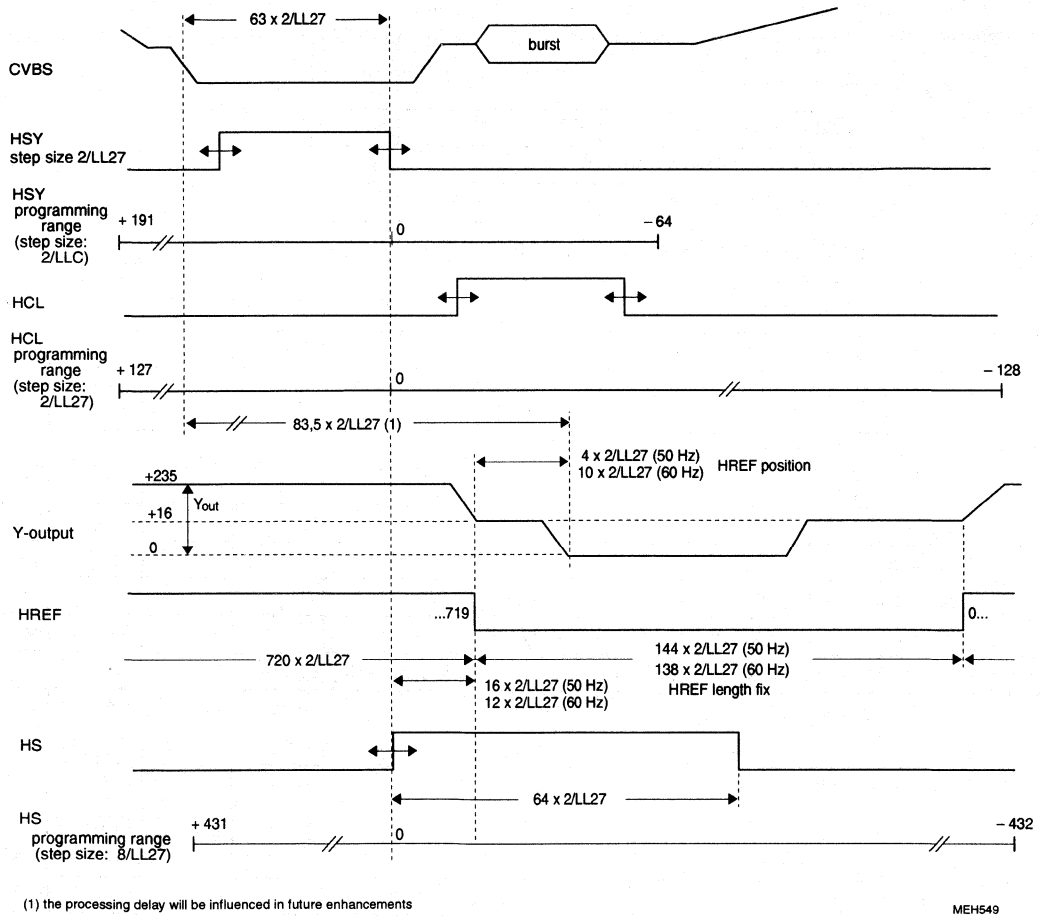


Fig.14 Horizontal sync and clamping timing for 50/60 Hz (signals HSY, HCL, HREF and HS).

8. LIMITING VALUES

In accordance with the Absolute Maximum Rating ystem (IEC 134); ground pins 19, 35, 38, 51 and 67 as well as supply pins 5, 18, 28, 37 and 52 connected together.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (pins 5, 18, 28, 37, 52)	−0.5	7.0	V
$V_{diff\ GND}$	difference voltage $V_{SS\ A} - V_{SS(1\ to\ 4)}$	-	±100	mV
V_I	voltage on all inputs	−0.5	V_{DD}+0.5	V
V_O	voltage on all outputs ($I_{O\ max}$ = 20 mA)	−0.5	V_{DD}+0.5	V
P_{tot}	total power dissipation	-	2.5	W
T_{stg}	storage temperature range	−65	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling* for all pins	-	±2000	V

9. CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; T_{amb} = 0 to 70 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage range (pins 5, 18, 28, 37, 52)		4.5	5	5.5	V
I_{DD}	total supply current (pins 5, 18, 28, 37, 52)	V_{DD} = 5 V; inputs LOW; outputs not connected	-	100	250	mA
I²C-bus, SDA and SCL (pins 40 and 41)						
$V_{I\ L}$	input voltage LOW		−0.5	-	1.5	V
$V_{I\ H}$	input voltage HIGH		3	-	V_{DD}+0.5	V
$I_{40,41}$	input current		-	-	±10	µA
I_{ACK}	output current on pin 40	acknowledge	3	-	-	mA
$V_{O\ L}$	output voltage at acknowledge	I_{40} = 3 mA	-	-	0.4	V
Data, clock and control inputs (pins 3, 4, 6 to 17, 20 to 23, 27, 34, 64 and 68); Figures 12 and 13						
$V_{I\ L}$	LL27 input voltage (pin 27)	LOW	−0.5	-	0.6	V
$V_{I\ H}$		HIGH	2.4	-	V_{DD}+0.5	V
$V_{I\ L}$	other input voltages	LOW	−0.5	-	0.8	V
$V_{I\ H}$		HIGH	2.0	-	V_{DD}+0.5	V
I_{leak}	input leakage current		-	-	10	µA
C_I	input capacitance	data inputs; note 1	-	-	8	pF
		I/O high-impedance	-	-	8	pF
		clock inputs	-	-	10	pF
$t_{SU.DAT}$	input data set-up time	Fig.15	11	-	-	ns
$t_{HD.DAT}$	input data hold time		3	-	-	ns

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.; inputs and outputs are protected against electrostatic discharge in normal handling. Normal precautions appropriate to handle MOS devices is recommended ("Handling MOS Devices").

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
YUV-bus, HREF and VS outputs (pins 30, 42, 45 to 50 and pins 53 to 62), Figures 9 and 12 to 13						
V_{OL}	output voltage LOW	notes 1 and 2	0	-	0.6	V
V_{OH}	output voltage HIGH		2.4	-	V_{DD}	V
C_L	load capacitor		15	-	50	pF
LFCO output (pin 36)						
V_o	output signal (peak-to-peak value)	note 2	1.4	-	2.6	V
V_{36}	output voltage range		1	-	V_{DD}	V
Control outputs (pins 24 to 26, 29, 31, 32, 33, 39, 63, 65 and 66); Fig.11, 14 and 15						
V_{OL}	output voltage LOW	notes 1 and 2	0	-	0.6	V
V_{OH}	output voltage HIGH		2.4	-	V_{DD}	V
C_L	load capacitor		7.5	-	25	pF
Timing of YUV-bus and control outputs		Figures 9 and 11				
t_{OH}	output signal hold time	YUV, HREF, VS at C_L = 15 pF;	13	-	-	ns
		controls at C_L = 7.5 pF	13	-	-	ns
t_{OS}	output set-up time	YUV, HREF, VS at C_L = 50 pF;	20	-	-	ns
		controls at C_L = 25 pF	20	-	-	ns
t_{SZ}	data output disable transition time	to 3-state condition	22	-	-	ns
t_{ZS}	data output enable transition time	from 3-state condition	20	-	-	ns
Chrominance PLL						
f_C	catching range		±400	-	-	Hz
Crystal oscillator		Figures 17 and 18; note 3				
f_n	nominal frequency	3rd harmonic	-	24.576	-	MHz
$\Delta f / f_n$	permissible deviation f_n		-	-	±50	10^{-6}
	temperature deviation from f_n		-	-	±20	10^{-6}
X1	crystal specification:					
	temperature range T_{amb}		0	-	70	°C
	load capacitance C_L		8	-	-	pF
	series resonance resistance R_S		-	40	80	Ω
	motional capacitance C_1		-	1.5±20%	-	fF
	parallel capacitance C_0		-	3.5±20%	-	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Line locked clock input LL27 (pin 27)		Fig.8 and 15				
t_{LL27}	cycle time	note 4	35	-	39	ns
t_p	duty factor	t_{LL27H}/t_{LL27}	40	50	60	%
t_r	rise time		-	-	5	ns
t_f	fall time		-	-	6	ns

Notes to the characteristics

1. Data output signals are Y7 to Y0 and UV7 to UV0. All other are control output signals.
2. Levels are measured with load circuit. YUV-bus, HREF and VS outputs with 1.2 kΩ in parallel to 50 pF at 3 V (TTL load); LFCO output with 10 kΩ in parallel to 15 pF and other outputs with 1.2 kΩ in parallel to 25 pF at 3 V (TTL load).
3. Recommended crystal: Philips 4322 143 05291.
4. t_{SU}, t_{HD}, t_{OH} and t_{OD} include t_r and t_f.

Table 4 High-impedance control for YUV-bus (Fig.15)

OEDY	OEDC	FEIN	Y(7:0)	UV(7:0)
0	0	0	Z	Z
0	1	0	Z	active
1	0	0	active	Z
1	1	0	Z	Z
X	X	1	Z	Z

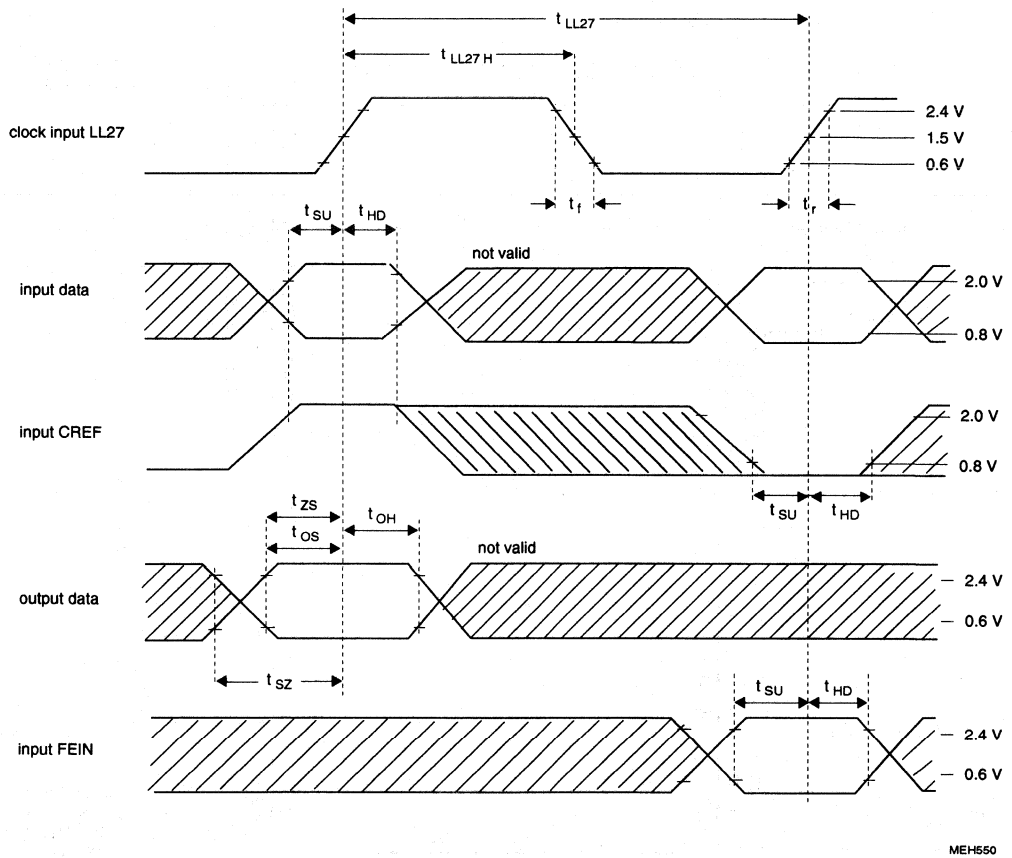


Fig.15 Data input and output timing diagram.

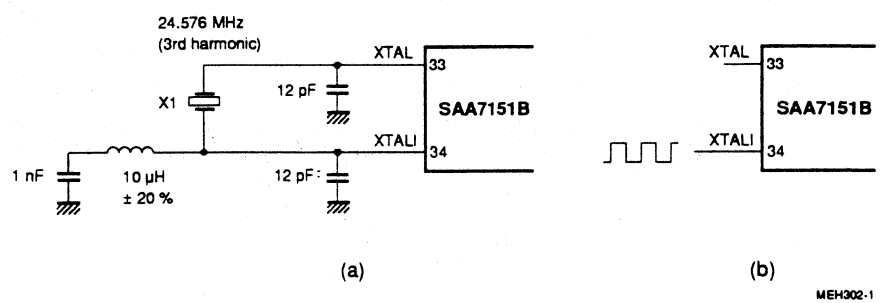


Fig.16 Oscillator application (a) and optional clock from external (b).

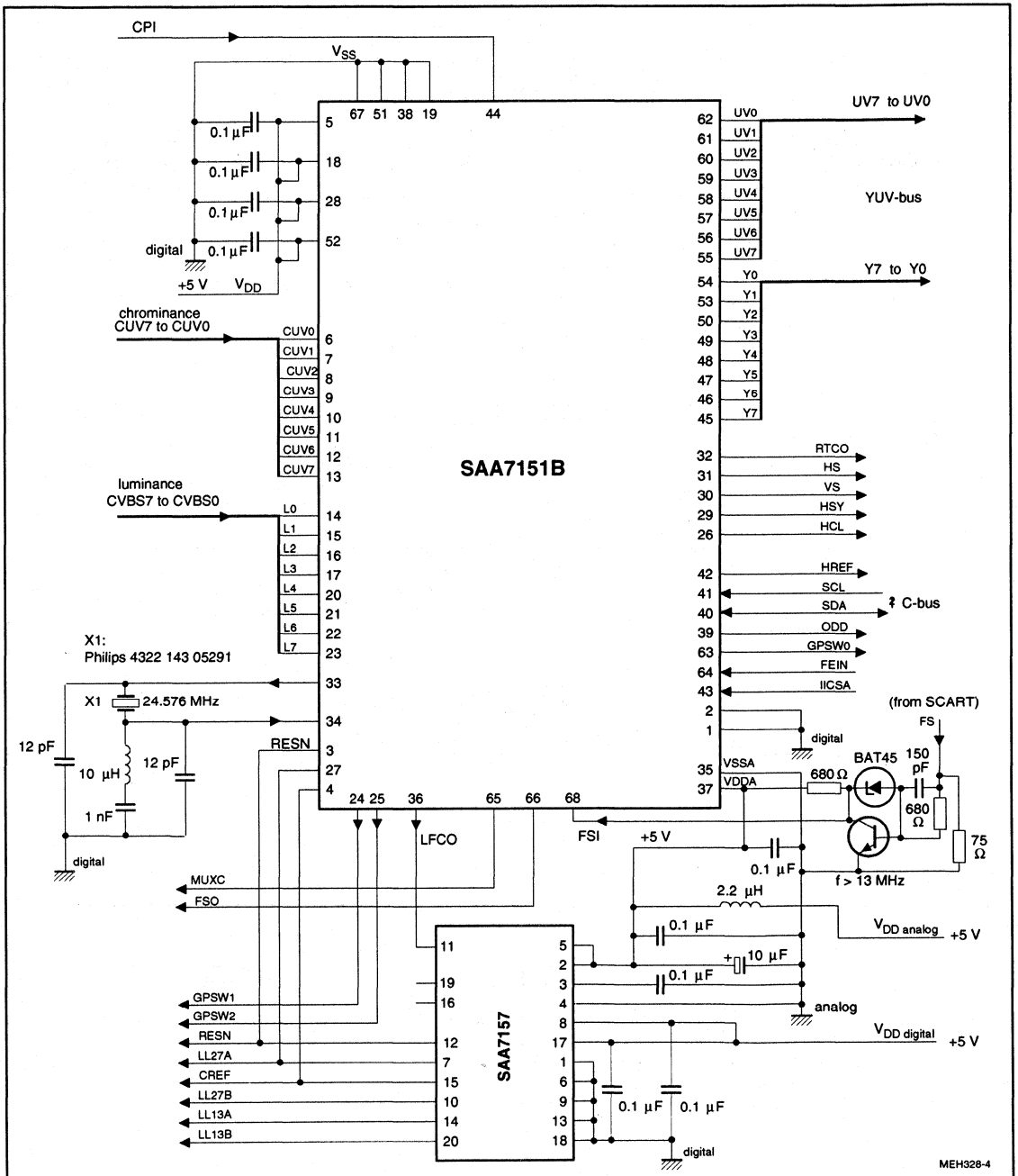


Fig.17 Application of SAA7151B.

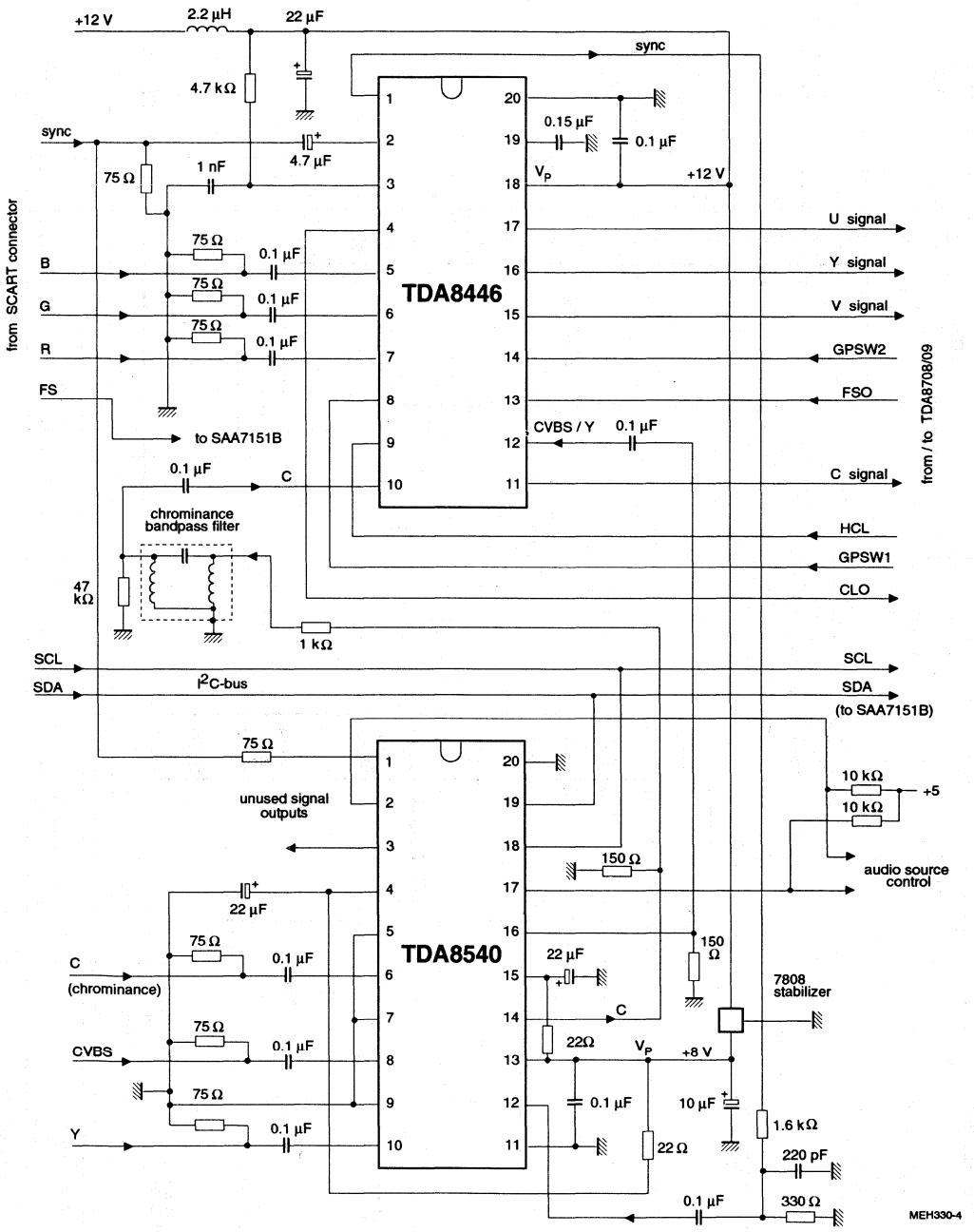


Fig.18 Application of input signal selecting (SCART interface).

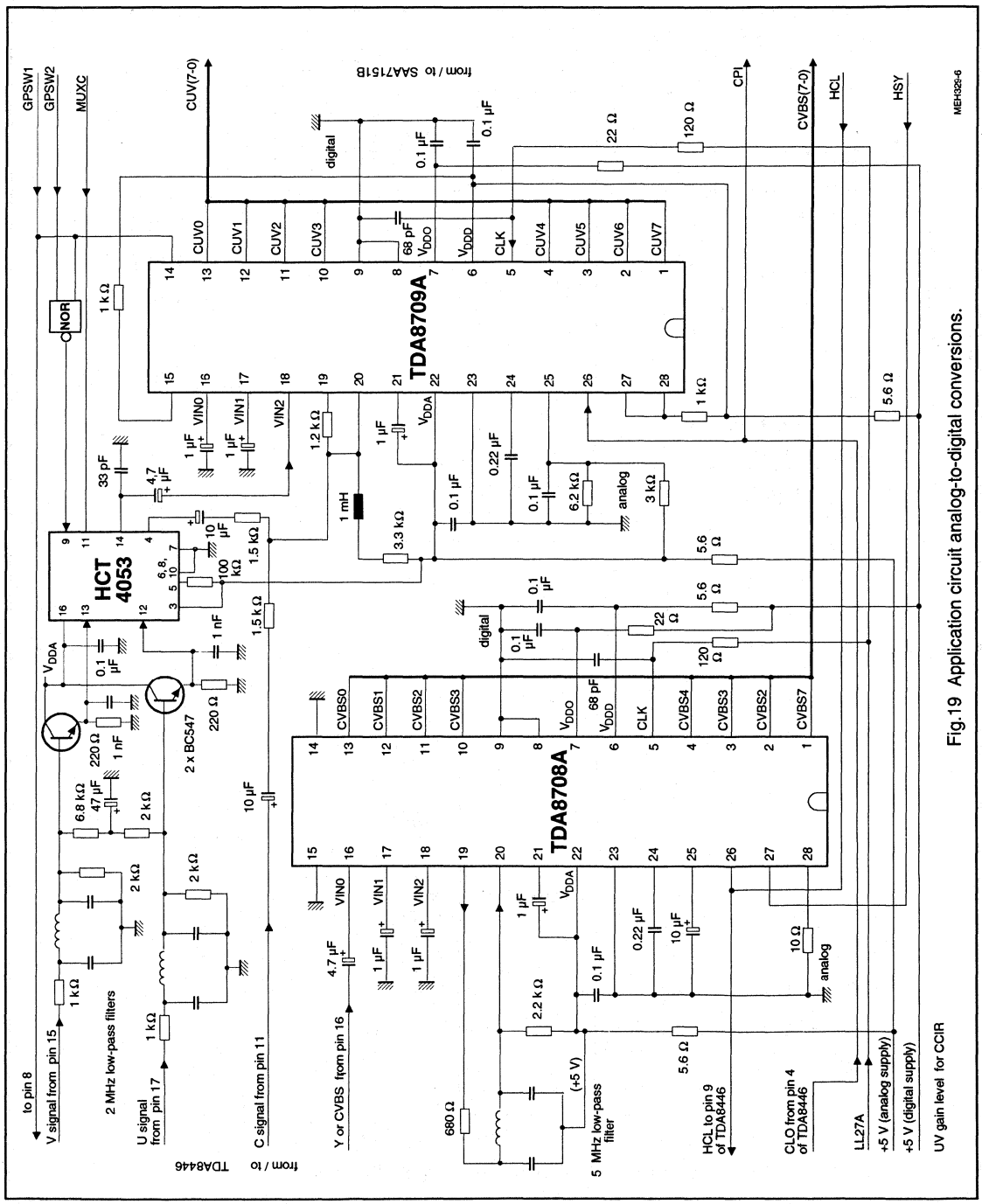


Fig.19 Application circuit analog-to-digital conversions.

10. I²C-BUS FORMAT

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA0	A		DATAn	A	P

S = start condition
SLAVE ADDRESS = **1000 101X** (IICSA = LOW) **or 1000 111X** (IICSA = HIGH)
A = acknowledge, generated by the slave
SUBADDRESS* = subaddress byte (Table 5)
DATA = data byte (Table 5)
P = stop condition

X = read/write control bit
X = 0, order to write (the circuit is slave receiver)
X = 1, order to read (the circuit is slave transmitter)

* If more than 1 byte DATA are transmitted, then auto-increment of the subaddress is performed.

Remarks:
- Prior to reset of the IC all outputs are undefined.
- After power-on reset, the control register 12 (hex) is set to 00 (hex).

Table 5 I²C-bus; DATA for status byte (X in address byte = 1; slave address 8B (hex) at IICSA = LOW or 8F (hex) at IICSA = HIGH)

FUNCTION		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
status byte		STTC	HLCK	FIDT	FSST1	FSST0	CDET2	CDET1	CDET0

Function of the bits:

STTC — Status time constant (to be used for gogical combfilter SAA7152): 0 = TV mode; 1 = VCR mode

HLCK — Horizontal PLL information: 0 = HPLL locked; 1 = HPLL unlocked

FIDT — Field information: 0 = 50 Hz system detected; 1 = 60 Hz system detected

FSST1 to FSST0 — Fast swiching output mode:

FSST1	FSST0	mode
0	0	RGB; FSI = HIGH (pin 68)
0	1	Y/C; FSI = LOW (pin 68)
1	0	fast switching (toggle)
1	1	not used

CDET2 to CDET0 — Identified colour standard

CDET2	CDET2	CDET2	standard
0	0	0	PAL-B/G, -H, -I; 50 Hz
0	0	1	PAL-N; 50 Hz
0	1	0	SECAM; 50 Hz
0	1	1	PAL-M; 60 Hz
1	0	0	PAL 4.43; 60 Hz
1	0	1	NTSC-M; 60 Hz
1	1	0	NTSC 4.43; 60 Hz
1	1	1	black/white

Table 6 I²C-bus; subaddress and data bytes for writing (X in address byte = 0; slave address 8A (hex) at IICSA = LOW or 8E at IICSA = HIGH)

function	subaddress byte	data byte D7	D6	D5	D4	D3	D2	D1	D0
increment delay	00	IDEL7	IDEL6	IDEL5	IDEL4	IDEL3	IDEL2	IDEL1	IDEL0
H-sync HSY begin	01	HSYB7	HSYB6	HSYB5	HSYB4	HSYB3	HSYB2	HSYB1	HSYB0
H-sync HSY stop	02	HSYS7	HSYS6	HSYS5	HSYS4	HSYS3	HSYS2	HSYS1	HSYS0
H-clamp HCL begin	03	HCLB7	HCLB6	HCLB5	HCLB4	HCLB3	HCLB2	HCLB1	HCLB0
H-clamp HCL stop	04	HCLS7	HCLS6	HCLS5	HCLS4	HCLS3	HCLS2	HCLS1	HCLS0
H-sync after PHI1	05	HPHI7	HPHI6	HPHI5	HPHI4	HPHI3	HPHI2	HPHI1	HPHI0
luminance control	06	BYPS	PREF	BPSS1	BPSS0	BFBY	CORI	APER1	APER0
hue control	07	HUEC7	HUEC6	HUEC5	HUEC4	HUEC3	HUEC2	HUEC1	HUEC0
miscellaneous controls #1	08	CSTD2	CSTD1	CSTD0	CKTQ4	CKTQ3	CKTQ2	CKTQ1	CKTQ0
miscellaneous controls #2	09	OSCE	LFIS1	LFIS0	CKTS4	CKTS3	CKTS2	CKTS1	CKTS0
PAL switch sensitivity	0A	PLSE7	PLSE6	PLSE5	PLSE4	PLSE3	PLSE2	PLSE1	PLSE0
SECAM switch sensitivity	0B	SESE7	SESE6	SESE5	SESE4	SESE3	SESE2	SESE1	SESE0
miscellaneous controls #3	0C	FSAU	GPSI2	GPSI1	CGFX	AMPF3	AMPF2	AMPF1	AMPF0
miscellaneous controls #4	0D	COLO	CHSB	GPSW0	SUVI	SXCR	FSDL2	FSDL1	FSDL0
miscellaneous controls #5	0E	CCIR	COFF	OEHS	OEVS	UVSS	CHRS	CDMO	CDPO
miscellaneous controls #6	0F	AUFD	FSEL	HPLL	SCEN	VTRC	MUIV	FSIV	WIND
miscellaneous controls #7	10	ASTD	OFTS	IPBP	CDVI	YDEL3	YDEL2	YDEL1	YDEL0
chroma gain reference	11	CHCV7	CHCV6	CHCV5	CHCV4	CHCV3	CHCV2	CHCV1	CHCV0
miscellaneous controls #8	12	OEDY	OEDC	VNOI1	VNOI0	BFON	BOFL2	BOFL1	BOFL0

Function of the bits of Table 6

IDEL7 to IDEL0 "00"

Increment delay time , step size = 4/LL27 = 148 ns*

D7	D6	D5	D4	D3	D2	D1	D0	decimal multiplier	note
1	1	1	1	1	1	1	1	−1 to −110	minimum −148 ns
1	0	0	1	0	0	1	0		−16.3 µs (outside available range)
1	0	0	1	0	0	0	1	−111 to −214	−16.44 µs
0	0	1	0	1	0	1	0		−31.7 µs (maximum value at FSEL = 1)
0	0	1	0	1	0	0	1	−215	−31.85 µs (outside central counter range at FSEL = 1 **)
0	0	1	0	1	0	0	0	−216	−32.0 µs (maximum value at FSEL = 0 **)
0	0	1	0	0	1	1	1	−217 to −256	−32.148 µs (outside central counter range at FSEL = 0 **)
0	0	0	0	0	0	0	0		−37.9 µs (outside central counter **)

* an internal sign-bit D8 set to HIGH indicates that all values are always negative

** H-PLL does not operate in this condition; the system clock frequency is set to a value fixed by the last update and is within ±7.1 % of the nominal frequency.

HSYB7 to HSYB0
HSYS7 to HSYS0
"01" and "02"

Horizontal sync begin, step size = 2/LL27 = 74 ns
Horizontal sync stop, step size = 2/LL27 = 74 ns

D7	D6	D5	D4	D3	D2	D1	D0	decimal multiplier	note
1	0	1	1	1	1	1	1	191 to 1	−14.2 µs (maximum negative value)
0	0	0	0	0	0	0	1		−74 ns
0	0	0	0	0	0	0	0	0	0 equals reference value
1	1	1	1	1	1	1	1	−1 to −64	+74 ns
1	1	0	0	0	0	0	0		+4.7 µs

HCLB7 to HCLB0
HCLS7 to HCLS0
"03" and "04"

Horizontal clamp begin, step size = 2/LL27 = 74 ns
Horizontal clamp stop, step size = 2/LL27 = 74 ns

D7	D6	D5	D4	D3	D2	D1	D0	decimal multiplier	note
0	1	1	1	1	1	1	1	127 to 1	−9.4 µs (maximum negative value)
0	0	0	0	0	0	0	1		−74 ns
0	0	0	0	0	0	0	0	0	0 equals reference value
1	1	1	1	1	1	1	1	−1 to −128	+74 ns
1	0	0	0	0	0	0	0		+9.5 µs (maximum positive value)

HPHI7 to HPHI0
"05"

Horizontal sync start, step size = 8/LL27 = 296 ns

D7	D6	D5	D4	D3	D2	D1	D0	decimal multiplier	note
0	1	1	1	1	1	1	1	+127 to +109	) forbidden (outside available central
0	1	1	0	1	1	0	1		) counter range)
0	1	1	0	1	1	0	0	+108 to +1	−32 µs (maximum negative value)
0	0	0	0	0	0	0	1		−0.296 ns
0	0	0	0	0	0	0	0	0	0 equals reference value
1	1	1	1	1	1	1	1	−1 to −107	+0.296 µs
1	0	0	1	0	1	0	1		+31.7 µs (maximum positive value)
1	0	0	1	0	1	0	0	−108 to −128	) forbidden (outside available central
1	0	0	0	0	0	0	0		) counter range)

BYPS
"06"

Input mode select bit: 0 = CVBS mode (chroma trap active)
1 = S-Video mode (chroma trap by-passed)

PREF

Use of pre-emphasis (to be used if chrominance trap is active):
0 = pre-filter bypassed; 1 = pre-filter on

BPSS1 to BPSS0

Aperture bandpass to select different centre frequencies (Figures 23 to 38):

BPSS1	BPSS0	centre frequency
0	0	4.1 MHz
0	1	3.8 MHz
1	0	2.6 MHz
1	1	2.9 MHz

"06" continued

BFBY: Bandfilter bypass switching: 0 = bandfilter active; 1 = bandfilter bypassed

CORI: Coring function: 0 = coring off; 1 = ±1 LSB coring

APER1 to APER0: Aperture factor (Figures 23 to 38):

APER1	APER0	factor
0	0	0
0	1	0.25
1	0	0.5
1	1	1

HUE7 to HUE0 "07": Hue control from +178.6° to −180.0°, equals data bytes 7F to 80 (hex); 0° equals 00.

CSTD2 to CSTD0 "08": Forced colour standard of input signal;

CSTD2	CSTD1	CSTD0	standard
0	0	0	PAL-B/G, -H, -I; 50 Hz
0	0	1	PAL-N; 50 Hz
0	1	0	SECAM; 50 Hz
0	1	1	PAL-M; 60 Hz
1	0	0	PAL 4.43; 60 Hz
1	0	1	NTSC-M; 60 Hz
1	1	0	NTSC 4.43; 60 Hz
1	1	1	black/white

CKTQ4 to CKTQ0: Colour killer threshold QAM (PAL/NTSC):

CKTQ4	CKTQ3	CKTQ2	CKTQ1	CKTQ0	
1	1	1	1	1	approximately −30 to −24 dB
1	0	0	0	0	−24 dB to −18 dB
0	0	0	0	0	

OSCE "09": External UV offset compensation: 0 = disabled; 1 = enabled

LFIS1 to LFIS0: Chrominance gain control (AGC filter):

LFIS1	LFIS0	control of loop filter time constant
0	0	slow
0	1	medium
1	0	fast
1	1	actual gain, stored (for test purposes only)

CKTS4 to CKTS0: Colour killer threshold SECAM as previously described under CKTQ subaddress"08"

PLSE7 to PLSE0 "0A"

PAL switch sensitivity from LOW to HIGH (HIGH means immediate sequence correction), equals FF to 00 (hex), MEDIUM equals 80.

SESE7 to SESE0 "0B"

SECAM switch sensitivity from LOW to HIGH (HIGH means immediate sequence correction), equals FF to 00 (hex), MEDIUM equals 80.

FSAU; GPSI2, and GPSI1 "0C"

Set port outputs (general purpose switching, internal)

FSAU	GPSI2	GPSI1	output GPSW2 (pin 25)	output GPSW1 (pin 24)
0	0	0	LOW	LOW
0	0	1	LOW	HIGH
0	1	0	HIGH	LOW
0	1	1	HIGH	HIGH
1	X	X	status bit FSST1 set	status bit FSST0 set

CGFX

Chrominance gain pre-determination: 0 = gain controlled via loop; 1 = gain set by AMPF-bits

AMPF3 to AMPF0

Chrominance amplification factor

AMPF3	AMPF2	AMPF1	AMPF0	gain
0	0	0	0	−6 dB
0	1	0	0	0 dB
0	1	0	1	+1.5 dB
.	.	.	.	+3 to +16.5 dB (approximately 1.5 dB steps)
1	1	1	1	+17 dB

COLO "0D"

Colour-on bit: 0 = colour-killer automatically enabled ; 1 = forced colour-on.

CHSB

Chrominance (UV) output code: 0 = two's complement; 1 = straightly binary

GPSW0

General purpose port output (pin 63): 0 = LOW; 1 = HIGH

SUVI

SECAM UV output signal polarity: 0 = U and V positive; 1 = U and V negative

SXCR

SECAM cross-colour reduction: 0 = off; 1 = on

FDSL2 to FDSL0

Fast switching delay adjustment in 37 ns steps:

FDSL2	FDSL1	FDSL0	delay
0	0	0	0
0	0	1	37 ns
0	1	0	74 ns
0	1	1	111 ns
1	0	0	−148 ns (negative delay)
1	0	1	−111 ns
1	1	0	−74 ns
1	1	1	−37 ns

CCIR "0E"	Set CCIR mode: 0 = digital TV mode (DTV); 1 = CCIR mode
COFF	Set colour off: 0 = colour on; 1 = colour off
OEHS	Enable horizontal sync outputs HS and HREF: 0 = output high-impedance; 1 = HS and HREF enabled
OEVS	Enable vertical sync output VS: 0 = output high-impedance; 1 = VS enabled
UVSS	Select UV pixel sample: 1 = first pixel after U/V signal has changed; 0 = second pixel (free of crosstalk signals)
CHRS	S-Video input mode: 0 = chrominance signal from CVBS or CUV input and controlled by BYPS (subaddress 06); 1 = S-Video mode; chrominance signal from CUV input
CDMO, CDPO	Chrominance delay: CDMO 0, CDPO 0 = no delay; CDMO 1, CDPO X = –37 ns (negative delay); CDMO 0, CDPO 1 = +37 ns
AUFD "0F"	Automatical field detection: 0 = field selection by FSEL-bit; 1 = automatical field detection
FSEL	Field select (AUFD-bit = 0): 0 = 50 Hz (625 lines); 1 = 60 Hz (525 lines)
HPLL	Horizontal PLL: 0 = PLL closed; 1 = PLL open, horizontal frequency fixed
SCEN	Sync and clamping pulse enable: 0 = HCL and HSY outputs HIGH (pins 26 and 29); 1 = HCL and HSY outputs active.
VTRC	VTR/TV mode select: 0 = TV mode (slow time constant); 1 = VTR mode (fast time constant).
MUIV	MUXC signal invertion: 0 = inverted; 1 = not inverted
FSIV	Fast switch input signal inversion: 0 = not inverted; 1 = inverted
WIND	Narrow fast switch window : 0 = off; 1 = on
ASTD "10"	Automatic standard switching: 0 = off; 1 = on
OFTS	Select output format: 0 = 4 : 1 : 1 format; 1 = 4 : 2 : 2 format.
IPBP	External UV signal interpolation filter: 0 = active; 1 = bypassed
CDVI	Chrominance PLL filter selection for: 0 = VTR or TV source; 1 = fast time constant for FSC-PLL (only for special applications)
YDEL3 to YDEL0	Luminance delay compensation in 37 ns steps: YDEL3 0, YDEL2 0, YDEL1 0, YDEL0 0 = 0 ns; YDEL3 0, YDEL2 0, YDEL1 0, YDEL0 1 = 37 ns; YDEL3 0, YDEL2 0, YDEL1 1, YDEL0 0 = 74 ns; YDEL3 0, YDEL2 0, YDEL1 1, YDEL0 1 = 111 ns; YDEL3 0, YDEL2 1, YDEL1 0, YDEL0 0 = 148 ns; YDEL3 0, YDEL2 1, YDEL1 0, YDEL0 1 = 185 ns; YDEL3 0, YDEL2 1, YDEL1 1, YDEL0 0 = 222 ns; YDEL3 0, YDEL2 1, YDEL1 1, YDEL0 1 = 259 ns; YDEL3 1, YDEL2 0, YDEL1 0, YDEL0 0 = –296 ns; YDEL3 1, YDEL2 0, YDEL1 0, YDEL0 1 = –259 ns; YDEL3 1, YDEL2 0, YDEL1 1, YDEL0 0 = –222 ns; YDEL3 1, YDEL2 0, YDEL1 1, YDEL0 1 = –185 ns; YDEL3 1, YDEL2 1, YDEL1 0, YDEL0 0 = –148 ns; YDEL3 1, YDEL2 1, YDEL1 0, YDEL0 1 = –111 ns; YDEL3 1, YDEL2 1, YDEL1 1, YDEL0 0 = –74 ns; YDEL3 1, YDEL2 1, YDEL1 1, YDEL0 1 = –37 ns

CHCV7 to CHCV0

"11"

Chroma gain reference value

D7	D6	D5	D4	D3	D2	D1	D0	gain	
1	1	1	1	1	1	1	1	maximum gain	
	:				:			to	)
1	0	1	1	0	0	1	1	DTV level	) default programmed values
	:				:			to	) dependend on application
0	0	1	1	1	1	0	1	CCIR level	)
	:				:			to	)
0	0	0	0	0	0	0	0	minimum gain	

OEDY
"12"
OEDC

Enable Y signals on YUV-bus: 0 = output high-impedance; 1 = output active (dependent on FEIN)

Enable UV signals on YUV-bus: 0 = output high-impedance; 1 = output active ((dependent on FEIN)

VNOI1, VNOI0

Vertical noise reduction mode:

VNOI1	VNOI0	mode
0	0	normal
0	1	searching
1	0	free-running
1	1	bypassed

BFON

Bottom flutter compensation switching: 0 = off; 1 = on (controlled by BOFL-bit)

BOFL2 to BOFL0

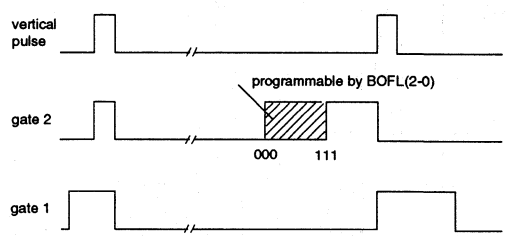
Bottom flutter compensation

BOFL2	BOFL1	BOFL0	start at line number
0	0	0	297 for PAL (247 for NTSC; active to end of field)
0	0	1	298 for PAL (248 for NTSC; active to end of field)
.	.	.	. .
1	1	0	303 for PAL (253 for NTSC; active to end of field)
1	1	1	304 for PAL (254 for NTSC; active to end of field)

The bottom flutter circuit is able to compensate for horizontal phase jump of up to ±16 µs.

Note: The bottom flutter gate is active at
- HPLL is locked
- HPLL in VTR mode
- the vertical noise limiter (VNL) is in the VTR mode
- gating is switched by BFON-bit = 1 (subaddress 12)

Gate 2	Gate 1	HPLL function
0	0	normal
1	0	disabled
0	1	double speed
1	1	unused



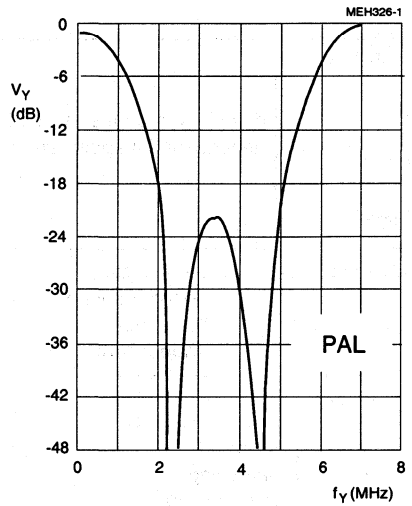


Fig.20 Frequency response of chroma stop filter in colour-difference mode for 50 Hz PAL. Filter is only active in fast switching mode, but bypassed in RGB mode. The selected filter is dependent on actual detected colour standard.

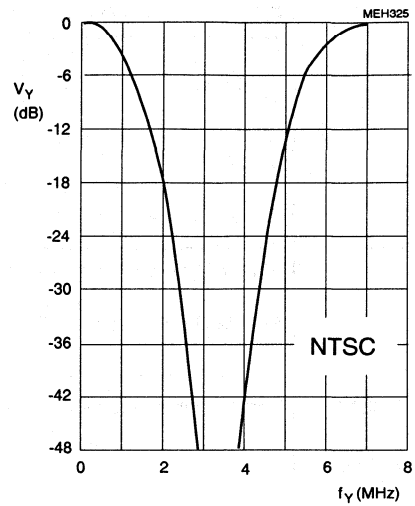


Fig.21 Frequency response of chroma stop filter in colour-difference mode for 60 Hz NTSC. Filter is only active in fast switching mode, but bypassed in RGB mode. The selected filter is dependent on actual detected colour standard.

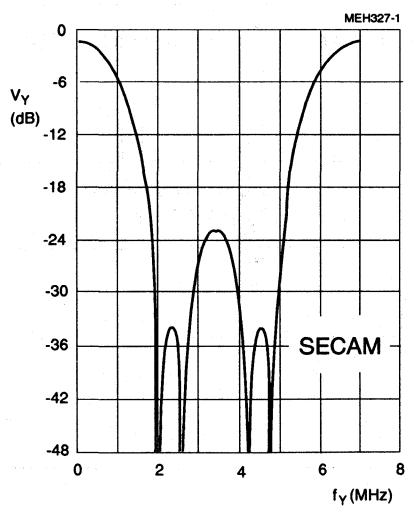


Fig.22 Frequency response of chroma stop filter in colour-difference mode for 50 Hz SECAM. Filter is only active in fast switching mode, but bypassed in RGB mode. The selected filter is dependent on actual detected colour standard.

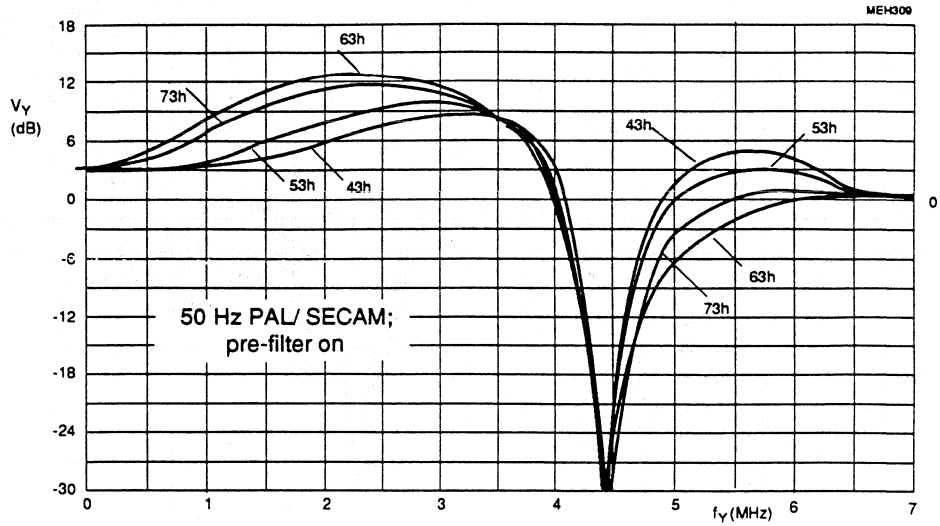


Fig.23 Maximum luminance peaking control as a function of four different aperture centre frequencies controllable by subaddress byte 06; aperture factor 1; coring off; chroma trap on; pre-filter on ; and bandfilter on.

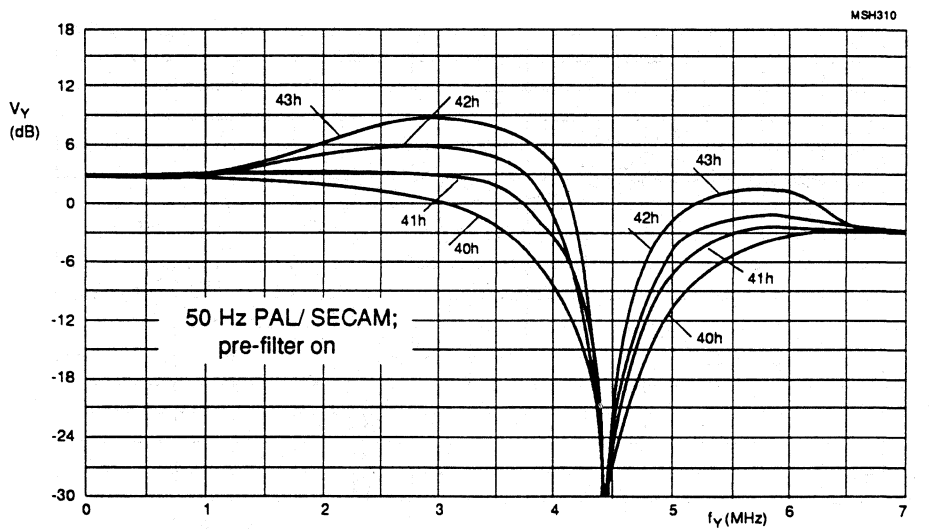


Fig.24 3.8 MHz luminance peaking control as a function of four different aperture factors controllable by subaddress byte 06; coring off; chroma trap on; pre-filter on and bandfilter on.

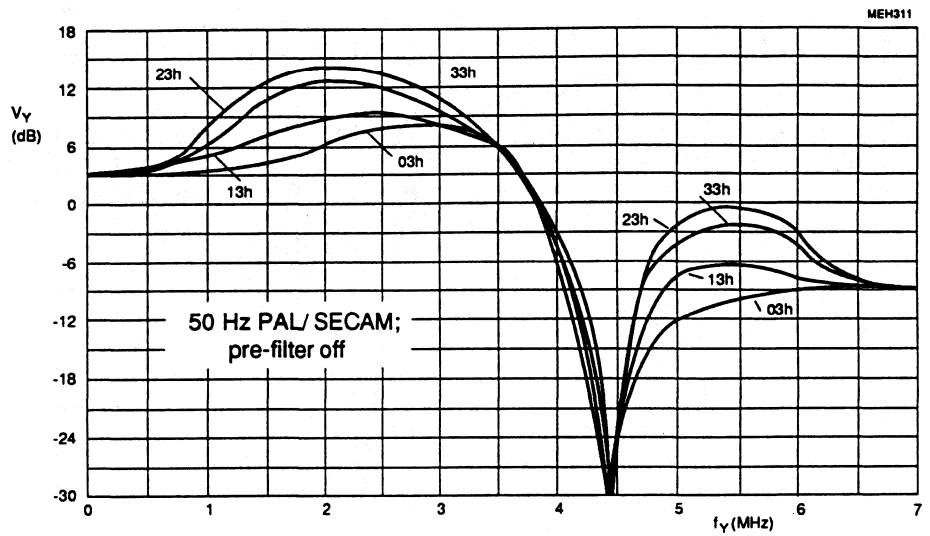


Fig.25 Maximum luminance peaking control as a function of four different aperture centre frequencies controllable by subaddress byte 06; aperture factor 1; coring off; chroma trap on; pre-filter off ; and bandfilter on.

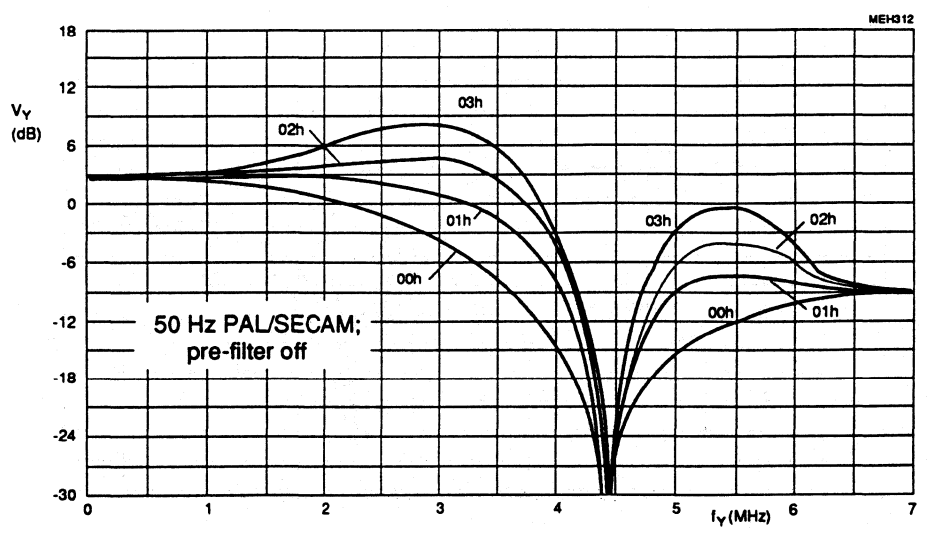


Fig.26 4.1 MHz luminance peaking control as a function of four different aperture factors controllable by subaddress byte 06; coring off; chroma trap on; pre-filter off and bandfilter on.

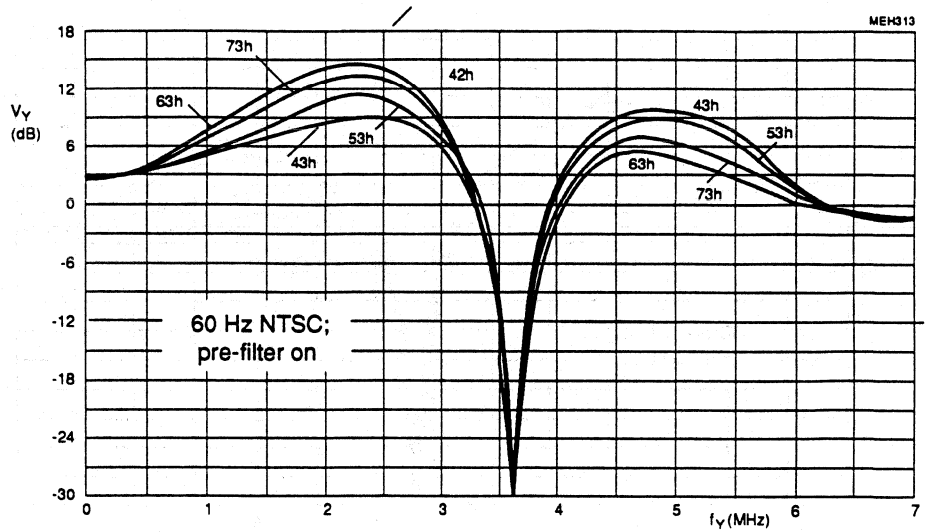


Fig.27 Maximum luminance peaking control as a function of four different aperture centre frequencies controllable by subaddress byte 06; aperture factor 1; coring off; chroma trap on; pre-filter on ; and bandfilter on.

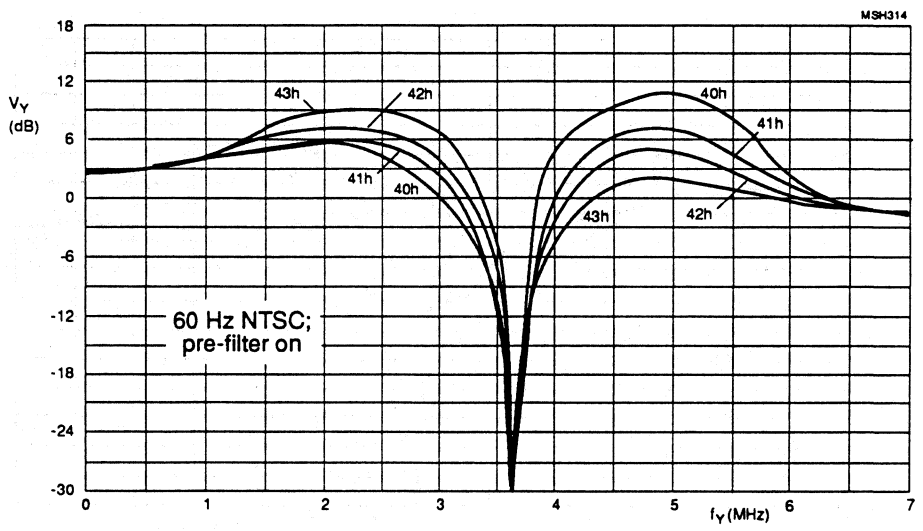


Fig.28 3.8 MHz luminance peaking control as a function of four different aperture factors controllable by subaddress byte 06; coring off; chroma trap on; pre-filter on and bandfilter on.

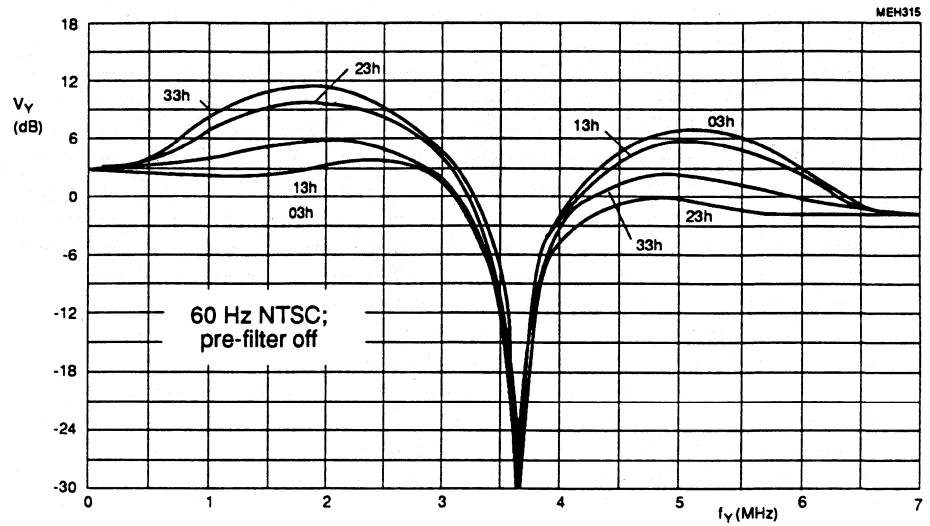


Fig.29 Maximum luminance peaking control as a function of four different aperture centre frequencies controllable by subaddress byte 06; aperture factor 1; coring off; chroma trap on; pre-filter off ; and bandfilter on.

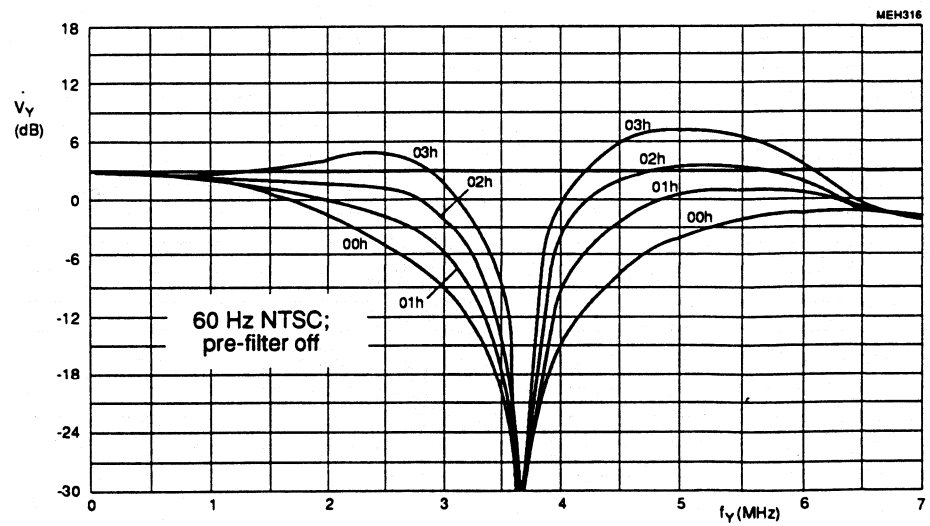


Fig.30 4.1 MHz luminance peaking control as a function of four different aperture factors controllable by subaddress byte 06; coring off; chroma trap on; pre-filter off and bandfilter on.

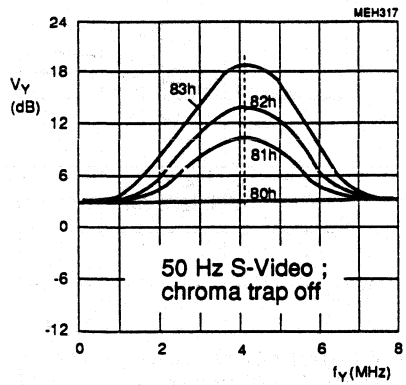


Fig.31 4.1 MHz luminance peaking control control as a function of four different aperture factors controllable by subaddress byte 06; pre-filter off; coring off and bandpass filter on.

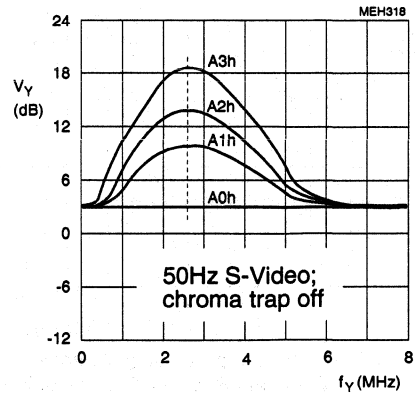


Fig.32 2.6 MHz luminance peaking control control as a function of four different aperture factors controllable by subaddress byte 06; pre-filter off; coring off and bandpass filter on.

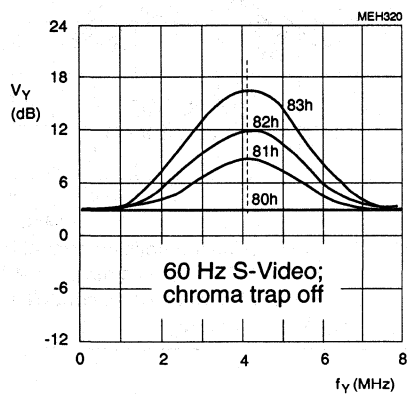


Fig.33 4.1 MHz luminance peaking control control as a function of four different aperture factors controllable by subaddress byte 06; pre-filter off; coring off and bandpass filter on.

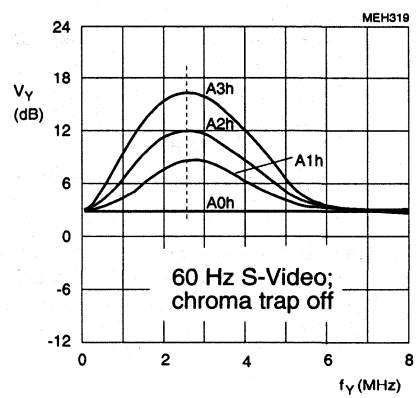


Fig.34 2.6 MHz luminance peaking control control as a function of four different aperture factors controllable by subaddress byte 06; pre-filter off; coring off and bandpass filter on.

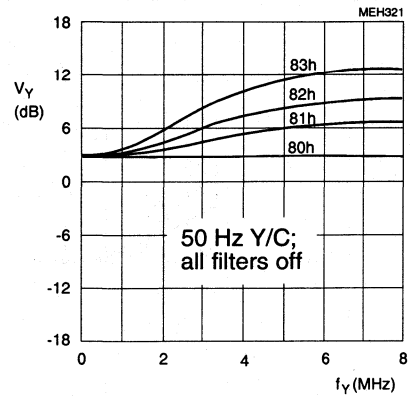


Fig.35 4.1 MHz luminance peaking control in 50 Hz / S-VHS mode as a function of four different aperture factors controllable by subaddress byte 06.

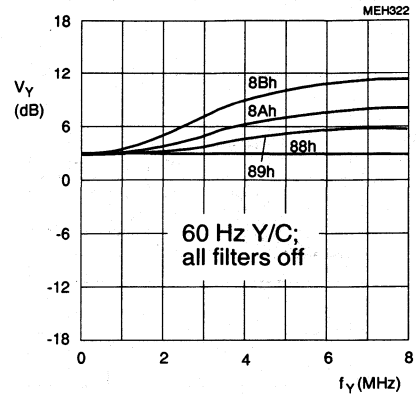


Fig.36 4.1 MHz luminance peaking control in 60 Hz / S-VHS mode as a function of four different aperture factors controllable by subaddress byte 06.

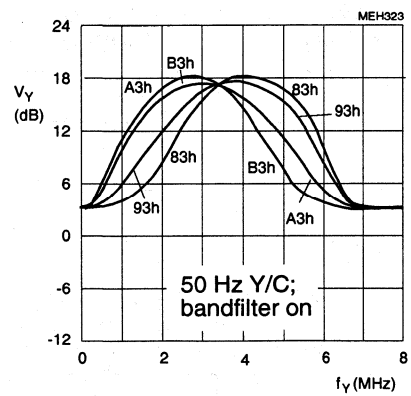


Fig.37 Maximum luminance peaking control in 50 Hz / S-VHS mode as a function of four aperture centre frequencies controllable by subaddress byte 06.

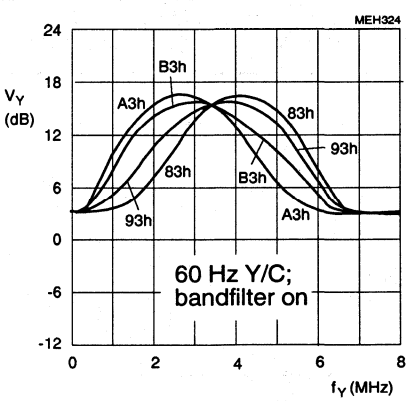
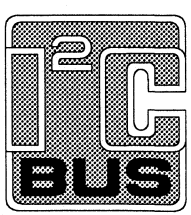


Fig.38 Maximum luminance peaking control in 60 Hz / S-VHS mode as a function of four aperture centre frequencies controllable by subaddress byte 06.



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

11. PROGRAMMING EXAMPLE

Coefficients to set operation for application circuits Figures 17, 18 and 19. Values recommended for PAL CVBS input signal and 4:2:2 CCIR output signal (all numbers of the Table 6 are hex values).

Table 7 Recommended default values (note 1)

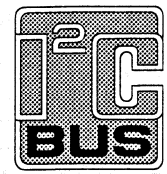
SUBADDRESS	BIT NAME	FUNCTION	VALUE (HEX)
00	IDEL(7-0)	increment delay	4D
01	HSYB(7-0)	horizontal sync HSY begin	3D
02	HSYS(7-0)	horizontal sync HSY stop	0D
03	HCLB(7-0)	horizontal clamping HCL begin	F3
04	HCLS(7-0)	horizontal clamping HCL stop	C6
05	HPHI(7-0)	horizontal sync after PHI1	FB
06	BYPS, PREF, BPSS(1-0) BFBY, CORI, APER(1-0)	luminance bandwidth control:	02 (note 2)
07	HUEC(7-0)	hue control (0 degree)	00
08	CSTD(2-0), CKTQ(4-0)	miscellanous controls #1	09
09	OSCE, LFIS(1-0),CKTS(4-0)	miscellanous controls #2	C0
0A	PLSE(7-0)	PAL switch sensitivity	4D
0B	SESE(7-0)	SECAM switch sensitivity	40
0C	FSAU, GPSI(2-1), CGFX, AMPF(3-0)	miscellanous controls #3	80
0D	COLO, CHSB, GPSW0, SUVI, SXCR, FSDL(2-0)	miscellanous controls #4	60
0E	CCIR, COEF, OEHS, OEVS UVSS, CHRS, CDMO, CDPO	miscellanous controls #5	B4
0F	AUFD, FSEL, HPLL, SCEN, VTRC, MUIV, FSIV, WIND	miscellanous controls #6	9F
10	ASTD, OFTS, IPBP, CDVI, YDEL(3-0)	miscellanous controls #7	C0
11	CHCV(7-0)	nominal chrominance gain	4F
12	OEDY, OEDC, VNOI(1-0), BFON, BOFL(2-0)	miscellanous controls #8	C2

Notes to Table 7

1 Slave address is 8A (hex) at IICSA = LOW or 8E (hex) at IICSA = HIGH.

2 Dependent on applications (Figures 23 to 38)

Digital Video Comb Filter (DCF) SAA7152



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Digital Video Comb Filter (DCF) SAA7152

1. FEATURES

- Comb filter circuit for luminance and chrominance separation
- Applicable for standards
  PAL B/G, M and N
  PAL 4.43 (525 lines; 60 Hz)
  NTSC M and N
  NTSC 4.43 (50 and 60 Hz)
- Luminance and chrominance bypasses with short delay in case of no filtering
- Line-locked system clock; CCIR-compatible
- I^2C-bus controlled

2. GENERAL DESCRIPTION

The CMOS digital comb filter circuit is located between video analog-to-digital converters and the video multistandard decoder SAA7151B (not applicable for SAA7191B). The two-dimensional filtering is only appropriate for standard signals from a source with constant phase relationship between subcarrier signal and horizontal frequency. The comb-filter has to be switched off for VTR signals and for separate VBS and and C signals. In VCR and S-Video operation the luminance low-pass and the chrominance bandpass parts can still be used for noise reduction purposes.

The processing delay is
21 x LL27 clocks in active mode or
3 x LL27 in short delay bypass mode (BYPS = 1).

3. QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage (pins 11, 34, 44)	4.5	5.0	5.5	V
I_P	total supply current	-	85	180	mA
V_i	input levels	TTL-compatible			
V_o	output levels	TTL-compatible			
LL27	typical system clock frequency	-	27	-	MHz
T_{amb}	operating ambient temperature range	0	-	70	°C

4. ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7152	44	PLCC	plastic	SOT187-2

5. BLOCK DIAGRAM

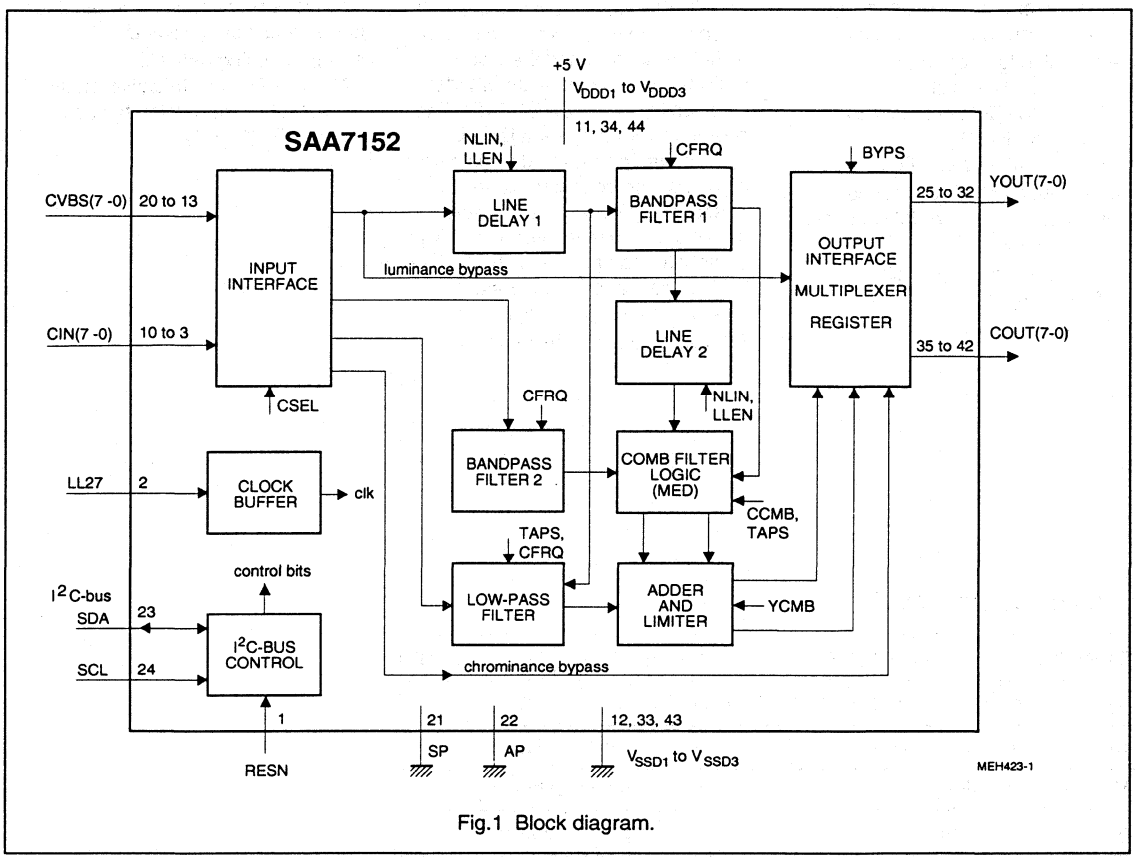

Fig.1 Block diagram.

6. PINNING

SYMBOL	PIN	DESCRIPTION
RESN	1	reset input; active-LOW
LL27	2	line-locked system clock input (27 MHz)
CIN0	3	chrominance input data bits CIN0 to CIN7
CIN1	4	
CIN2	5	
CIN3	6	
CIN4	7	
CIN5	8	
CIN6	9	
CIN7	10	

SYMBOL	PIN	DESCRIPTION
V_{DD1}	11	+5 V supply input 1
V_{SS1}	12	ground 1 (0 V)
CVBS0	13	CVBS input data bits o to 7
CVBS1	14	
CVBS2	15	
CVBS3	16	
CVBS4	17	
CVBS5	18	
CVBS6	19	
CVBS7	20	
SP	21	connected to ground (shift pin for testing)
AP	22	connected to ground (action pin for testing)
SDA	23	I^2C-bus data line
SCL	24	I^2C-bus clock line
YOUT7	25	luminance (Y) output data bits 7 to 0
YOUT6	26	
YOUT5	27	
YOUT4	28	
YOUT3	29	
YOUT2	30	
YOUT1	31	
YOUT0	32	
V_{SS2}	33	ground 2 (0 V)
V_{DD2}	34	+5 V supply input 2
COUT7	35	chrominance (C) output data bits 7 to 0
COUT6	36	
COUT5	37	
COUT4	38	
COUT3	39	
COUT2	40	
COUT1	41	
COUT0	42	
V_{SS3}	43	ground 3 (0 V)
V_{DD3}	44	+5 V supply input 3

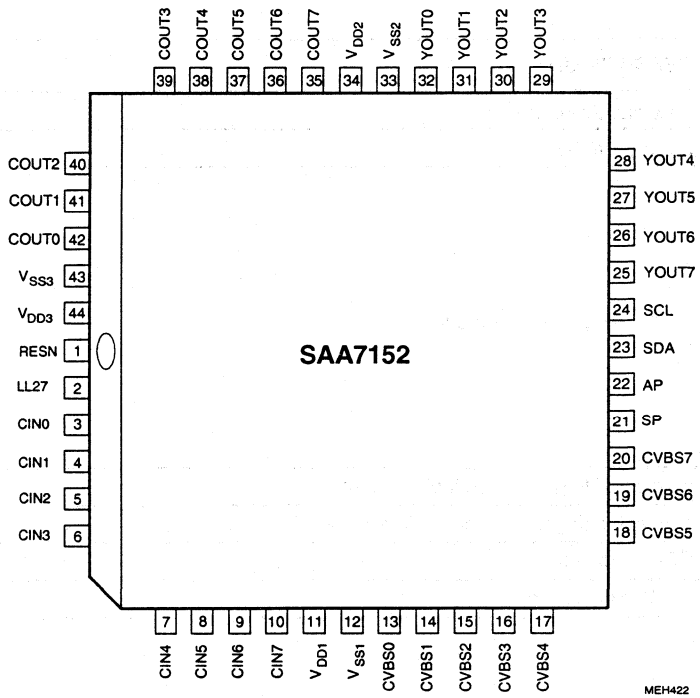

Fig.2 Pin configuration.

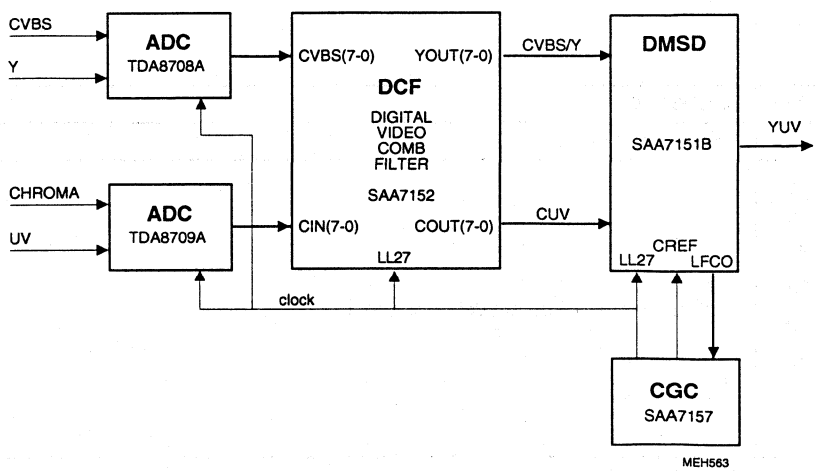

Fig.3 System environment.

7. I²C-BUS FORMAT

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA0	A		DATAn	A	P

S = start condition
SLAVE ADDRESS = 1011 0010 (B2 h)
A = acknowledge, generated by the slave
SUBADDRESS* = subadress byte (Table 1)
DATA = data byte (Table 1)
P = stop condition

X = read/write control bit
X = 0, order to write (the circuit is slave receiver)
X = 1, order to read (the circuit is slave transmitter)

* If more than 1 byte DATA are transmitted, then auto-increment of the subaddress is performed.

Table 1 I²C-bus; subaddress and data bytes for writing (after X = 0 in address byte)

FUNCTION	SUBADDRESS	DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Controls	00	BYPS	CSEL	CCMB	YCMB	TAPS	CFRQ	NLIN	LLEN

Function of the bits of Table 1:	
BYPS	Select bypass with a short delay; all other functions are disabled: 0 = no bypass; 1 = comb filter bypassed (delay is 3 LLC)
CSEL	Input mode select: 0 = CVBS selected; 1 = Y/C selected
CCMB	Select comb filtering: 0 = chrominance is bandpassed; 1 = chrominance is comb-filtered
YCMB	Enable chrominance substruction from CVBS signal: 0 = disabled, CVBS/Y signal is only low-passed 1 = enabled (chrominance trap or comb filtering)
TAPS	Selects tap for switching Y and C to adder: 0 = for bandpass/low-pass combination 1 = for comb filter active
CFRQ	Select centre frequency and matching factor of chrominance filter: 0 = 4.43 MHz; 1 = 3.58 MHz
NLIN	Select delay (number of lines): 0 = 4-line comb filter for standard PAL 1 = 2-line comb filter for standard NTSC
LLEN	Selects the number of clocks for each line delay: 0 = 1728 clocks (625 lines); 50 Hz) 1 = 1716 clocks (525 lines; 60 Hz)

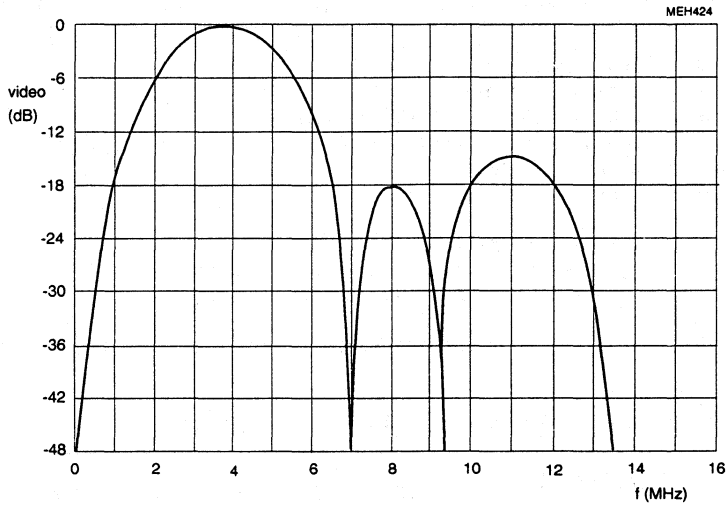

Fig.4 Frequency response of bandpass filters 1 and 2 with CFRQ-bit = 1.

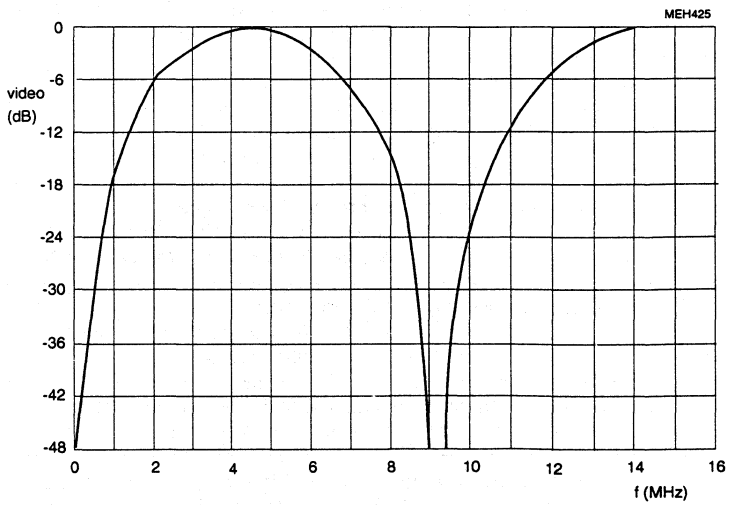

Fig.5 Frequency response of bandpass filters 1 and 2 with CFRQ-bit = 0.

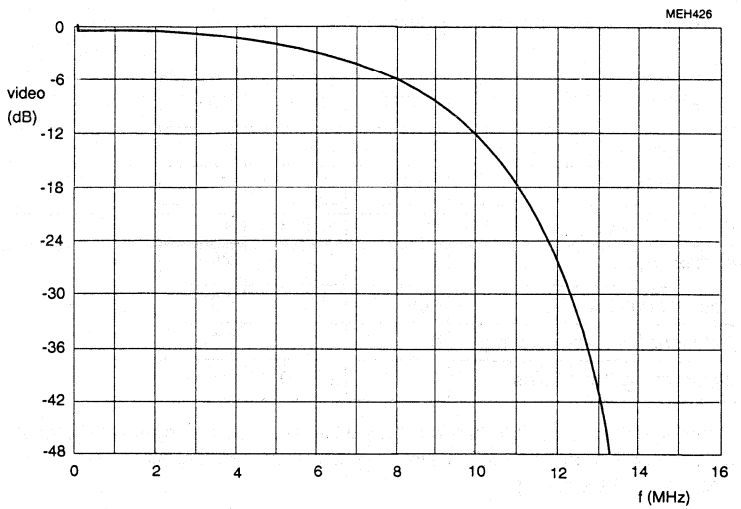

Fig.6 Frequency response of low-pass filter with CFRQ-bit = 1.

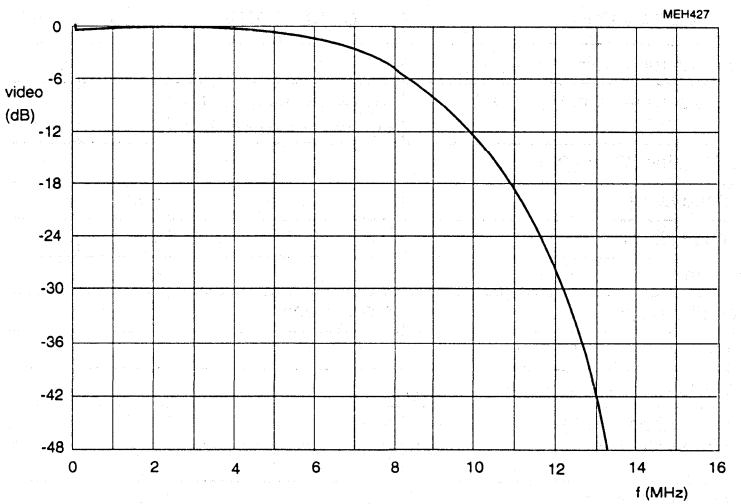

Fig.7 Frequency response of low-pass filter with CFRQ-bit = 0.

8. LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (pins 11, 34, 44)	−0.5	7.0	V
V_I	voltage on all inputs	−0.5	V_{DD}+0.5	V
V_O	voltage on all outputs ($I_{O\,max}$ = 20 mA)	−0.5	V_{DD}+0.5	V
P_{tot}	total power dissipation	-	1.0	W
T_{stg}	storage temperature range	−65	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling* for all pins	-	±2000	V

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.; inputs and outputs are protected against electrostatic discharge in normal handling. Normal precautions appropriate to handle MOS devices is recommended ("Handling MOS Devices").

9. CHARACTERISTICS

V_{DD1} to V_{DD3} = 5 V; T_{amb} = 0 to 70 °C and measurements taken in Fig.1 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage range (pins 11, 34, 44)		4.5	5	5.5	V
I_{DD}	total supply current (pins 11, 34, 44)	V_{DD} = 5 V; inputs LOW; outputs not connected	-	85	180	mA
I²C-bus, SDA and SCL (pins 23 and 24)						
$V_{I\,L}$	input voltage LOW		−0.5	-	1.5	V
$V_{I\,H}$	input voltage HIGH		3	-	V_{DD}+0.5	V
$I_{23,\,24}$	input current		-	-	±10	µA
I_{ACK}	output current on pin 23	acknowledge	3	-	-	mA
$V_{O\,L}$	output voltage at acknowledge	I_{23} = 3 mA	-	-	0.4	V
Data and clock inputs (pins 2 to 10 and pins 13 to 20)						
$V_{I\,L}$	LL27 input voltage (pin 2)	LOW	−0.5	-	0.6	V
$V_{I\,H}$		HIGH	2.4	-	V_{DD}+0.5	V
$V_{I\,L}$	other input voltages	LOW	−0.5	-	0.8	V
$V_{I\,H}$		HIGH	2.0	-	V_{DD}+0.5	V
I_{leak}	input leakage current		-	-	10	µA
C_I	input capacitance	data inputs	-	-	8	pF
		clock inputs	-	-	10	pF
$t_{SU.DAT}$	input data set-up time	Fig.8	11	-	-	ns
$t_{HD.DAT}$	input data hold time		3	-	-	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data outputs (pins 25 to 32 and pins 35 to 42)						
V_{OL}	output voltage LOW		0	-	0.6	V
V_{OH}	output voltage HIGH		2.4	-	V_{DD}	V
C_L	load capacitor		8	-	25	pF
Timing of data outputs		Fig.8				
t_{OH}	output signal hold time from positive edge of LL27	C_L = 8 pF	3	-	-	ns
t_{OD}	output delay from positive edge of LL27	C_L = 25 pF	-	-	32	ns
Line locked clock input LL27 (pin 2)		Fig.8				
t_{LL27}	cycle time	note 1	35	-	39	ns
t_p	duty factor	t_{LL27H}/t_{LL27}	40	50	60	%
t_r	rise time		-	-	5	ns
t_f	fall time		-	-	6	ns

Note to the characteristics

1. t_{SU}, t_{HD}, t_{OH} and t_{OD} include t_r and t_f.

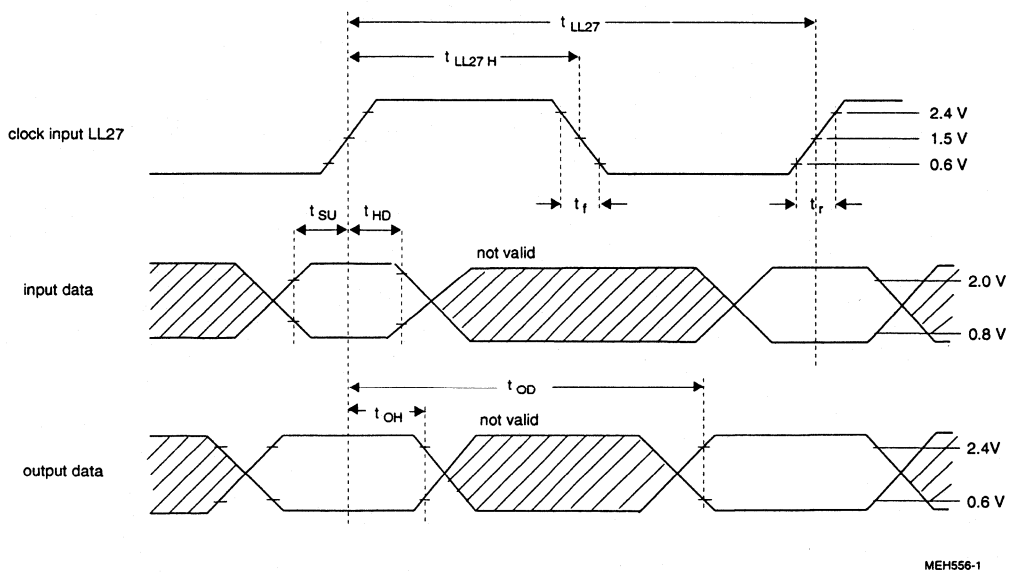

Fig.8 Data input and output timing.

Clock Generator Circuit for digital TV systems (CGC)

SAA7157

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Clock Generator Circuit for digital TV systems (CGC)

SAA7157

1. FEATURES

- Clock generation suitable for digital TV systems (line-locked)
- PLL frequency multiplier to generate 4 times of input frequency
- Dividers to generate clocks LL1.5A, LL1.5B, LL3A and LL3B (4th and 2nd multiples of input frequency)
- PLL mode or VCO mode selectable
- Reset control and power fail detection
- Suitable for applications with feature box and picture memory

2. GENERAL DESCRIPTION

The SAA7157 generates all clock signals required for a digital TV system suitable for the SAA715x family and the SAA7199B (DENC). The circuit operates in either the phase-locked loop mode (PLL) or voltage controlled oscillator mode (VCO).

3. QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage (pin 5)	4.5	5.0	5.5	V
V_{DDD}	digital supply voltage (pins 8, 17)	4.5	5.0	5.5	V
I_{DDA}	analog supply current	3	-	9	mA
I_{DDD}	digital supply current	10	-	60	mA
V_{LFCO}	LFCO input voltage (peak-to-peak value)	1	-	V_{DDA}	V
f_i	input frequency range	6.0	-	7.25	MHz
V_I	input voltage LOW input voltage HIGH	0 2.0	- -	0.8 V_{DDD}	V V
V_O	output voltage LOW output voltage HIGH	0 2.6	- -	0.6 V_{DDD}	V V
T_{amb}	operating ambient temperature range	0	-	70	°C

4. ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7157P	20	DIP	plastic	SOT146-1
SAA7157T	20	SO	plastic	SOT163-1

5. BLOCK DIAGRAM

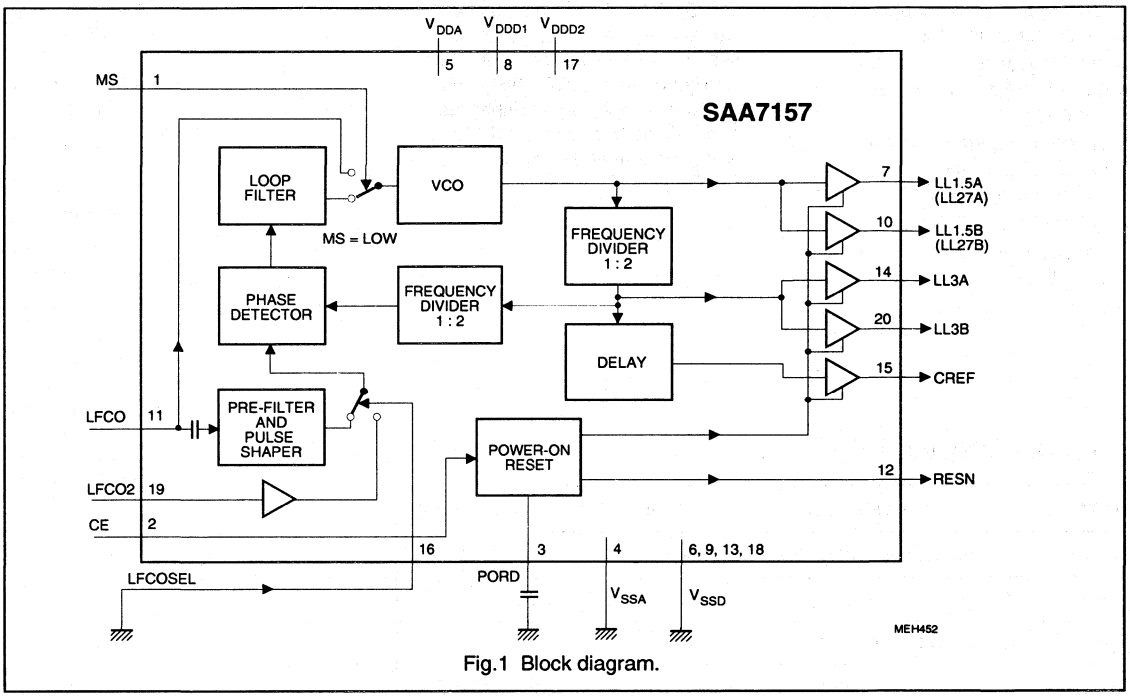


Fig.1 Block diagram.

6. FUNCTION DESCRIPTION

The SAA7157 generates all clock signals required for a digital TV system suitable for the SAA715x family consisting of an 8-bit analog-to-digital converter (ADC8), digital video multistandard decoder (DMSD2) and video enhancement and D/A processor circuit (VEDA). Optional extras (feature box, video memory etc.) can be driven via external buffers, advantageous for a digital TV system based on display standard conversion concepts.
The 6.75 MHz input signal LFCO (triangular waveform) coming from the DMSD or LFCO2 is multiplied to 27 MHz by the PLL (including phase detector, loop filter, VCO and frequency divider) and output on LL1.5A (pin7) and LL1.5B (pin 10). The 13.5 MHz frequencies are generated by dividers using ratio of 1:2 and are output on LL3A (pin 14) and LL3B (pin 20).

The rectangular output signals have 50 % duty factor. Outputs with equal frequency may be connected together externally. The clock outputs go HIGH during power-on reset (and chip enable) to ensure that no output clock signals are available before the PLL has locked-on.

Mode select MS
The LFCO input signal is directly connected to the VCO at MS = HIGH. The circuit operates as an oscillator and frequency divider. This function is not tested.

Source select LFCOSEL
Line frequency control signal (LFCO) is selected by LFCOSEL input.
LFCOSEL = LOW:
signal from LFCO (pin 11) is selected.
LFCOSEL = HIGH:
signal from LFCO2 (pin 19) is selected.
This function is not tested.

Chip enable CE
The buffer outputs are enabled and RESN is set to HIGH by CE = HIGH (Fig.4).
CE = LOW sets the clock outputs HIGH and RESN output LOW.

CREF output

TV2 digital clock reference output signal. Clock qualifier signal to TV system with 2 times of LFCO or LFCO2 frequency.

Power-on reset

Power-on reset is activated at power-on, when the supply voltage decreases below 3.5 V (Fig.4) or when chip enable is done. The indicator output RESN is LOW for a time determined by capacitor on pin 3. The RESN signal can be applied to reset other circuits of this digital TV system.
The LFCO or LFCO2 input signals have to be applied before RESN becomes HIGH.

7. PINNING

SYMBOL	PIN	DESCRIPTION
MS	1	mode select input (LOW = PLL mode)
CE	2	chip enable /reset (HIGH = outputs enabled)
PORD	3	power-on reset delay, dependent on external capacitor
V_{SSA}	4	analog ground (0 V)
V_{DDA}	5	analog supply voltage (+5 V)
V_{SSD1}	6	digital ground 1 (0 V)
LL1.5A	7	line-locked clock output signal 1.5A (4 times f_{LFCO})
V_{DDD1}	8	digital supply voltage 1 (+5 V)
V_{SSD2}	9	digital ground 2 (0 V)
LL1.5B	10	line-locked clock output signal 1.5B (4 times f_{LFCO})
LFCO	11	line-locked frequency control input signal 1
RESN	12	reset output (active-LOW, Fig.4)
V_{SSD3}	13	digital ground 3 (0 V)
LL3A	14	line-locked clock output signal 3A (2 times f_{LFCO})
CREF	15	clock reference output, qualifier signal (2 times f_{LFCO})
LFCOSEL	16	LFCO source select (LOW = LFCO selected)*
V_{DDD2}	17	digital supply voltage 2 (+5 V)
V_{SSD4}	18	digital ground 4 (0 V)
LFCO2	19	line-locked frequency control input signal 2*
LL3B	20	line-locked clock output signal 3B (2 times f_{LFCO})

PIN CONFIGURATION

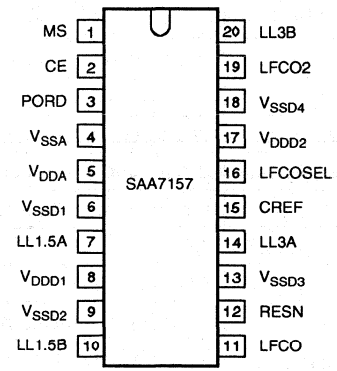


Fig.2 Pin configuration.

8. LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); ground pins as well as supply pins together connected.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage (pin 5)	−0.5	7.0	V
V_{DDD}	digital supply voltage (pins 8 and 17)	−0.5	7.0	V
$V_{diff\ GND}$	difference voltage $V_{DDA} - V_{DDD}$	-	±100	mV
V_O	output voltage (I_{OM} = 20 mA)	−0.5	V_{DDD}	V
P_{tot}	total power dissipation (DIL20)	0	1.1	W
T_{stg}	storage temperature range	−65	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling** for all pins	-	tbf	V

* MS and LFCO2 functions are not tested. LFCO2 is a multiple of horizontal frequency.

** Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is recommended to take normal handling precautions appropriate to "Handling MOS devices ".

9. CHARACTERISTICS

V_{DDA} = 4.5 to 5.5 V; V_{DDD} = 4.5 to 5.5 V; f_{LFCO} = 6.0 to 7.25 MHz and T_{amb} = 0 to 70 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage (pin 5)		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage (pins 8 and 17)		4.5	5.0	5.5	V
I_{DDA}	analog supply current (pin 5)		3	-	9	mA
I_{DDD}	digital supply current ($I_8 + I_{17}$)	note 1	10	-	60	mA
V_{reset}	power-on reset threshold voltage	Fig.4	-	3.5	-	V
Input LFCO (pin 11)						
V_{11}	DC input voltage		0	-	V_{DDA}	V
V_i	input signal (peak-to-peak value)		1	-	V_{DDA}	V
f_{LFCO}	input frequency range		6.0	-	7.25	MHz
C_{11}	input capacitance		-	-	10	pF
Inputs MS, CE, LFCOSEL and LFCO2 (pins 1, 2, 16 and 19); note 3						
V_{IL}	input voltage LOW		0	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{DDD}	V
f_{LFCO2}	input frequency range for LFCO2		6.0	-	7.25	MHz
I_{LI}	input leakage current	LFCOSEL	50	-	150	µA
		others	-	-	10	µA
C_I	input capacitance		-	-	5	pF
Output RESN (pin 12)						
V_{OL}	output voltage LOW	I_{OL} = 2 mA	0	-	0.4	V
V_{OH}	output voltage HIGH	I_{OH} = −0.5 mA	2.4	-	V_{DDD}	V
t_d	RESN delay time	C_3 = 0.1µF; Fig.4	20	-	200	ms
Output CREF (pin 15)						
V_{OL}	output voltage LOW	I_{OL} = 2 mA	0	-	0.6	V
V_{OH}	output voltage HIGH	I_{OH} = −0.5 mA	2.4	-	V_{DDD}	V
f_{CREF}	output frequency CREF	Fig.3	-	2 $f_{LFCO(2)}$		MHz
C_L	output load capacitance		15	-	40	pF
t_{SU}	set-up time	Fig.3; note 1	12	-	-	ns
t_{HD}	hold time	Fig.3; note 1	4	-	-	ns
Output signals LL1.5A, LL1.5B, LL3A and LL3B (pins 7, 10, 14, and 20); note 3						
V_{OL}	output voltage LOW	I_{OL} = 2 mA	0	-	0.6	V
V_{OH}	output voltage HIGH	I_{OH} = −0.5 mA	2.6	-	V_{DDD}	V
t_{comp}	composite rise time	Fig.3; notes 1 and 2	-	-	8	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{LL}	output frequency LL1.5A	Fig.3	-	4 $f_{LFCO(2)}$		MHz
	output frequency LL1.5B		-	4 $f_{LFCO(2)}$		MHz
	output frequency LL3A		-	2 $f_{LFCO(2)}$		MHz
	output frequency LL3B		-	2 $f_{LFCO(2)}$		MHz
t_r, t_f	rise and fall times	note 1; Fig.3	-	-	5	ns
t_{LL}	duty factor LL1.5A, LL1.5B, LL3A and LL3B (mean values)	note 1; Fig.3; at 1.5 V level	43	50	57	%

Notes to the characteristics

1. f_{LFCO} = 7.0 MHz and output load 40 pF (Fig.3). V_{SSA} and V_{SSD} short connected together.
2. t_{comp} is the rise time from LOW of all clocks to HIGH of all clocks (Fig.3) including rise time, skew and jitter components. Measurements taken between 0.6 V and 2.6 V. Skew between two LLx clocks will not deviate more than ±2 ns if output loads are matched within 20 %.
3. MS and LFCO2 functions not tested.

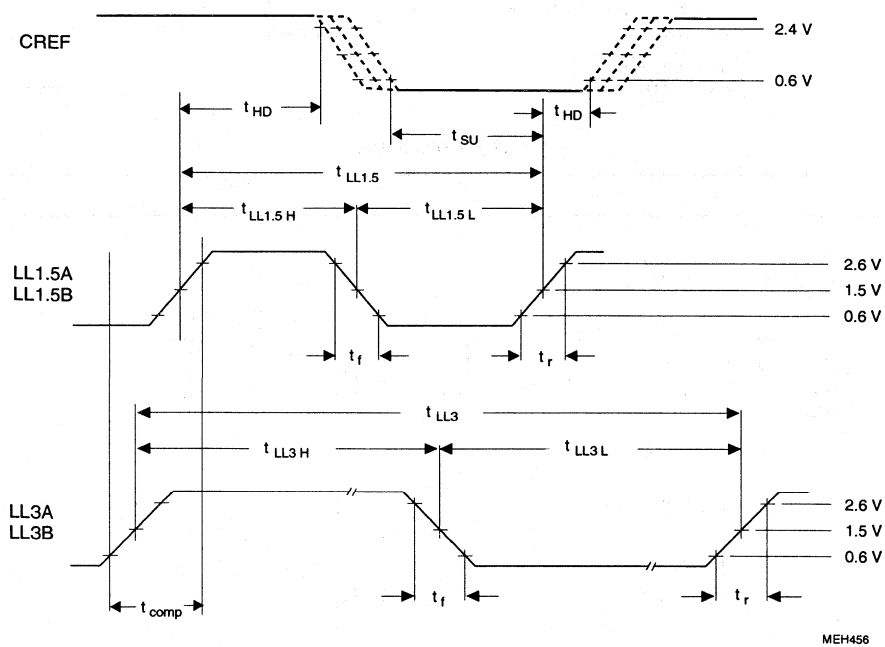


Fig.3 Output timing.

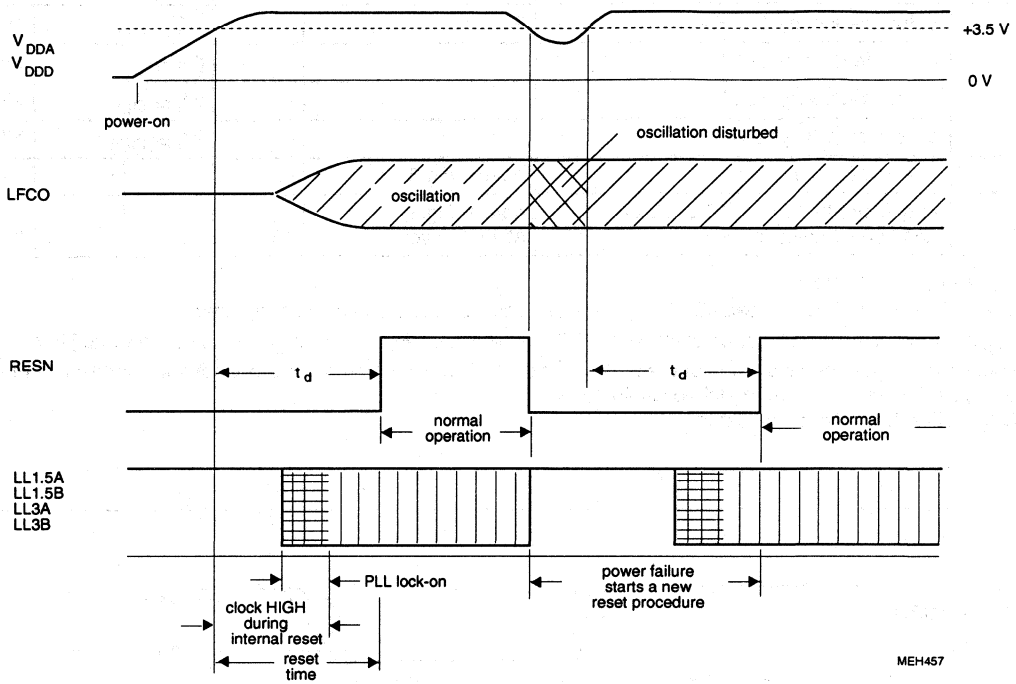


Fig.4 Reset procedure.

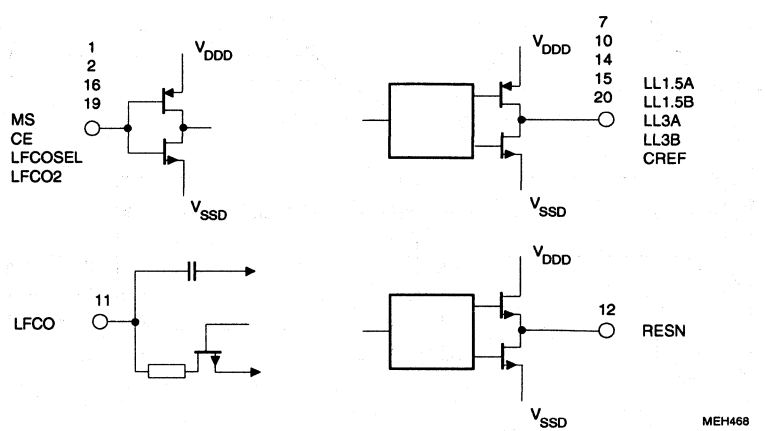
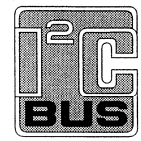


Fig.5 Internal circuit.

Video Enhancement and Digital-to-Analog processor (VEDA2)

SAA7165

FEATURES



- CMOS circuit to enhance video data and to convert luminance and colour-difference signals from digital-to-analog
- Digital Colour Transient Improvement block (DCTI) to increase the sharpness of colour transitions. The improved pin-compatible SAA7165 can supersede the SAA9065
- 16-bit parallel input for 4 : 1 : 1 and 4 : 2 : 2 YUV data
- Data clock input LLC (Line-Locked Clock) for a data rate up to 36 MHz
- 8-bit luminance and 8-bit multiplexed colour-difference formats (7-bit formats optional)
- MC input to support various clock and pixel rates
- Formatting YUV input data; 4 : 2 : 2 format, 4 : 1 : 1 format and filter characteristics selectable
- HREF input to determine the active line (number of pixels)
- Controllable peaking of luminance signal
- Coring stage with controllable threshold to eliminate noise in luminance signal
- Interpolation filter suitable for both formats to increase the data rate in chrominance path
- Polarity of colour-difference signals selectable
- All functions controlled via I^2C-bus
- Separate digital-to-analog converters (9-bit resolution for Y; 8-bit for colour-difference signals)
- 1 V (p-p)/75 Ω outputs realized by two resistors
- No external adjustments.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage	4.5	5	5.5	V
V_{DDA}	analog supply voltage	4.75	5	5.25	V
$I_{DD(tot)}$	total supply current	–	tbf	–	mA
V_{IL}	LOW-level input voltage on YUV-bus	−0.5	–	+0.8	V
V_{IH}	HIGH-level input voltage on YUV-bus	2	–	V_{DDD} + 0.5	V
f_{LLC}	input data rate	–	–	36	MHz
$V_{o(p-p)}$	output signals Y, (R – Y) and (B – Y) (peak-to-peak value)	–	2	–	V
R_L	output load resistance	125	–	–	Ω
ILE	DC integral linearity error in output signal (8-bit data)	–	–	1	LSB
DLE	DC differential error in output signal (8-bit data)	–	–	0.5	LSB
T_{amb}	operating ambient temperature range	0	–	70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7165WP	PLCC44	plastic leaded chip carrier; 44 leads	SOT187-2

BLOCK DIAGRAM

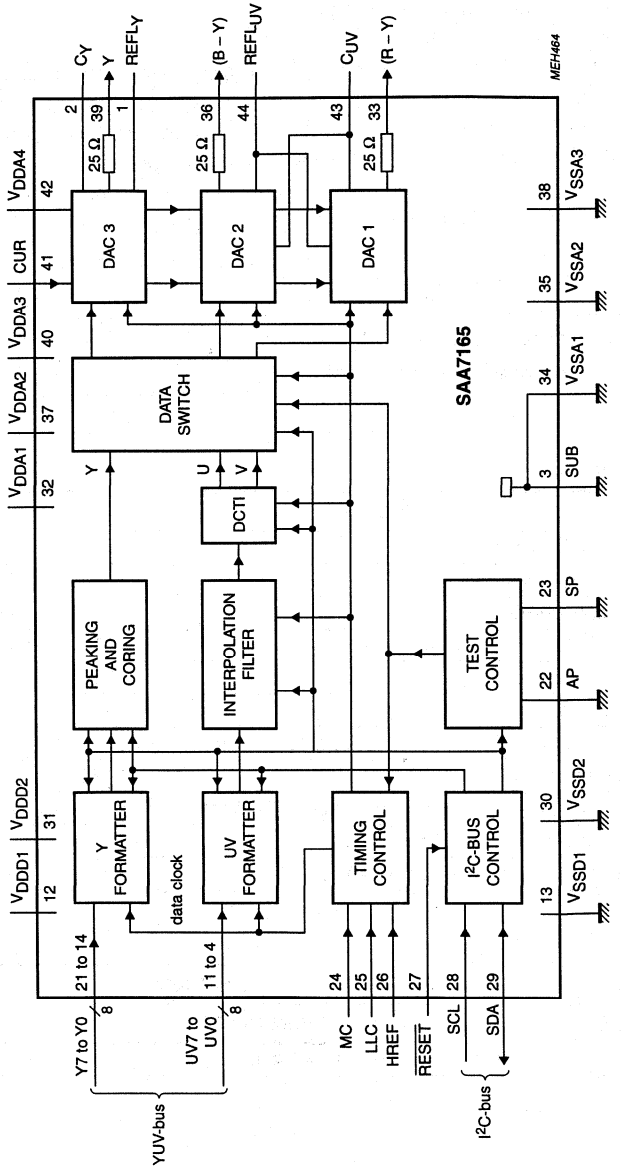


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$REFL_Y$	1	low reference of luminance DAC (connected to V_{SSA1})
C_Y	2	capacitor for luminance DAC (high reference)
SUB	3	substrate (connected to V_{SSA1})
UV0	4	UV signal input bit UV7 (digital colour-difference signal)
UV1	5	UV signal input bit UV6 (digital colour-difference signal)
UV2	6	UV signal input bit UV5 (digital colour-difference signal)
UV3	7	UV signal input bit UV4 (digital colour-difference signal)
UV4	8	UV signal input bit UV3 (digital colour-difference signal)
UV5	9	UV signal input bit UV2 (digital colour-difference signal)
UV6	10	UV signal input bit UV1 (digital colour-difference signal)
UV7	11	UV signal input bit UV0 (digital colour-difference signal)
V_{DDD1}	12	+5 V digital supply voltage 1
V_{SSD1}	13	digital ground 1 (0 V)
Y0	14	Y signal input bit Y7 (digital luminance signal)
Y1	15	Y signal input bit Y6 (digital luminance signal)
Y2	16	Y signal input bit Y5 (digital luminance signal)
Y3	17	Y signal input bit Y4 (digital luminance signal)
Y4	18	Y signal input bit Y3 (digital luminance signal)
Y5	19	Y signal input bit Y2 (digital luminance signal)
Y6	20	Y signal input bit Y1 (digital luminance signal)
Y7	21	Y signal input bit Y0 (digital luminance signal)
AP	22	connected to ground (action pin for testing)
SP	23	connected to ground (shift pin for testing)
MC	24	data clock CREF (e.g. 13.5 MHz); at MC = HIGH, the LLC divider-by-two is inactive
LLC	25	line-locked clock signal (LL27 = 27 MHz)
HREF	26	data clock for YUV data inputs (for active line 768Y or 640Y long)
$\overline{RESET}$	27	reset input (active LOW)
SCL	28	I^2C-bus clock line
SDA	29	I^2C-bus data line
V_{SSD2}	30	digital ground 2 (0 V)
V_{DDD2}	31	+5 V digital supply voltage 2
V_{DDA1}	32	+5 V analog supply voltage for buffer of DAC 1
(R – Y)	33	±(R – Y) output signal (analog signal)
V_{SSA1}	34	analog ground 1 (0 V)
V_{SSA2}	35	analog ground 2 (0 V)
(B – Y)	36	±(B – Y) output signal (analog colour-difference signal)
V_{DDA2}	37	+5 V analog supply voltage for buffer of DAC 2
V_{SSA3}	38	analog ground 3 (0 V)
Y	39	Y output signal (analog luminance signal)
V_{DDA3}	40	+5 V analog supply voltage for buffer of DAC 3

SYMBOL	PIN	DESCRIPTION
CUR	41	current input for analog output buffers
V_{DDA4}	42	supply and reference voltage for the three DACs
C_{UV}	43	capacitor for chrominance DACs (high reference)
$REFL_{UV}$	44	low reference of chrominance DACs (connected to V_{SSA1})

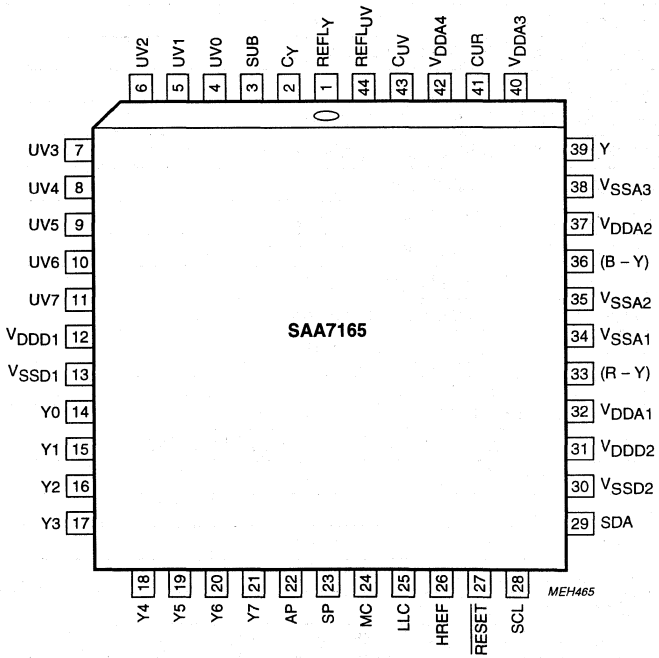


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The CMOS circuit SAA7165 processes digital YUV-bus data up to a data rate of 36 MHz. The data inputs Y7 to Y0 and UV7 to UV0 (see Fig.1) are provided with 8-bit data. The data of digital colour-difference signals U and V are in a multiplexed state (serial in 4 : 2 : 2 or 4 : 1 : 1 format; Tables 2 and 3).

Data is read with the rising edge of LLC (Line-Locked Clock) to achieve a data rate of LLC at MC = HIGH only. If MC is supplied with the frequency CREF (½LLC for example), data is read only at every second rising edge (see Fig.3).

The 7-bit YUV input data are also supported by means of bit R78 (R78 = 0). Additionally, the luminance data format is converted for internal use into a two´s complement format by inverting the MSB. The Y input byte (bits Y7 to Y0) represents luminance information; the UV input byte (bits UV7 to UV0) represents one of the two digital colour-difference signals in 4 : 2 : 2 format (Table 2).

The HREF input signal (HREF = HIGH) determines the start and the end of an active line (see Fig.3) and the number of pixels respectively. The analog output Y is blanked at HREF = LOW, the (B – Y) and (R – Y) outputs are in a colourless state. The blanking level can be set with bit BLV. The SAA7165 is controllable via the I²C-bus.

Formatting Y and UV

The input data formats are formatted into the internally used processing formats (separate for 4 : 2 : 2 and 4 : 1 : 1 formats). The IFF, IFC and IFL bits control the input data format and determine the right interpolation filter (see Figs 10 to 13).

Peaking and coring

Peaking is applied to the Y signal to compensate several bandwidth reductions of the external pre-processing. Y signals can be improved to obtain a better sharpness. There are the two switchable bandpass filters BF1 and BF2 controlled via the I²C-bus by the bits BP1, BP0 and BFB. Thus, a frequency response is achieved in combination with the peaking factor K (Figs 5 to 9; K is determined by the bits BFB, WG1 and WG0).

The coring stage with controllable threshold (4 states controlled by CO1 and CO0 bits) reduces noise disturbances (generated by the bandpass gain) by suppressing the amplitude of small high-frequent signal components. The remaining high-frequent peaking component is available for a weighted addition after coring.

Table 1 LLC and MC configuration modes in DMSD applications (note 1)

PIN	INPUT SIGNAL	DESCRIPTION
LLC	LLC (LL27)	The data rate on YUV-bus is half the clock rate on pin LLC, e.g. in SAA7151B, SAA7191 and SAA7191B single scan operation.
MC	CREF	
LLC	LLC (LL27)	The data rate on YUV-bus must be identical to the clock rate on pin LLC, e.g. in double scan applications.
MC	MC = HIGH	
LLC	LLC (LL27)	The data rate on YUV-bus must be identical to the clock rate on pin LLC, e.g. SAA9051 single scan operation.
MC	MC = HIGH	

Note

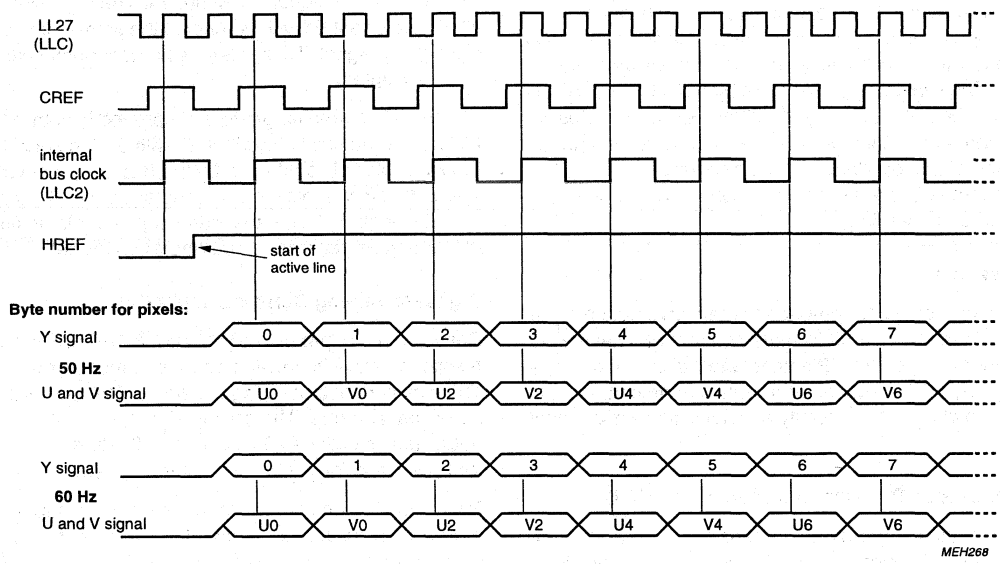
1. YUV data are only latched with the rising edge of LCC at MC = HIGH.

Table 2 Data format 4 : 2 : 2

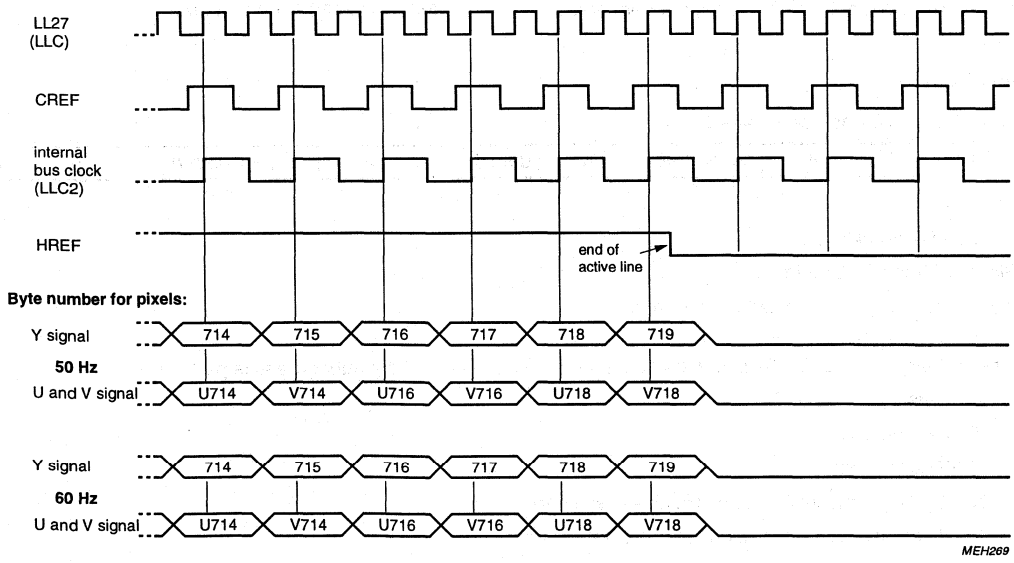
INPUT	PIXEL BYTE SEQUENCE (4 : 2 : 2 FORMAT)					
Y0 (LSB)	Y0	Y0	Y0	Y0	Y0	Y0
Y1	Y1	Y1	Y1	Y1	Y1	Y1
Y2	Y2	Y2	Y2	Y2	Y2	Y2
Y3	Y3	Y3	Y3	Y3	Y3	Y3
Y4	Y4	Y4	Y4	Y4	Y4	Y4
Y5	Y5	Y5	Y5	Y5	Y5	Y5
Y6	Y6	Y6	Y6	Y6	Y6	Y6
Y7 (MSB)	Y7	Y7	Y7	Y7	Y7	Y7
UV0 (LSB)	U0	V0	U0	V0	U0	V0
UV1	U1	V1	U1	V1	U1	V1
UV2	U2	V2	U2	V2	U2	V2
UV3	U3	V3	U3	V3	U3	V3
UV4	U4	V4	U4	V4	U4	V4
UV5	U5	V5	U5	V5	U5	V5
UV6	U6	V6	U6	V6	U6	V6
UV7 (MSB)	U7	V7	U7	V7	U7	V7
Y frame	0	1	2	3	4	5
UV frame	0		2		4	

Table 3 Data format 4 : 1 : 1

INPUT	PIXEL BYTE SEQUENCE (4 : 1 : 1 FORMAT)							
Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0
Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1
Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2
Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3
Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4
Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5
Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6
Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7
UV0	0	0	0	0	0	0	0	0
UV1	0	0	0	0	0	0	0	0
UV2	0	0	0	0	0	0	0	0
UV3	0	0	0	0	0	0	0	0
UV4	V6	V4	V2	V0	V6	V4	V2	V0
UV5	V7	V5	V3	V1	V7	V5	V3	V1
UV6	U6	U4	U2	U0	U6	U4	U2	U0
UV7	U7	U5	U3	U1	U7	U5	U3	U1
Y frame	0	1	2	3	4	5	6	7
UV frame	0				4			



a. Start of active line.



b. End of active line.

Fig.3 Line control by HREF for 4 : 2 : 2 format, CREF = 13.5 MHz; HREF = 720 pixel; 50 and 60 Hz field.

Interpolation

The chrominance interpolation filter consists of various filter stages, multiplexers and de-multiplexers to increase the data rate of the colour-difference signals by a factor of 2 or 4. The switching of the filters by the bits IFF, IFC and IFL is described previously. Additional signal samples with significant amplitudes between two consecutive signal samples of the low data rate are generated.
The time-multiplexed U and V samples are stored in parallel for converting.

Data switch

The digital signals are adapted to the conversation range. U and V data have 8-bit formats again; Y can have 9 bits dependent on peaking. Blanking and switching to colourless level is applied here. Bits can be inverted by INV-bit to change the polarity of colour-difference output signals.

Digital Colour Transient Improvement (DCTI)

The DCTI circuit improves the transition behaviour of the UV colour-difference signals. As the CVBS signal allows for a 4 : 1 : 1 bandwidth representation only, the DCTI improves the transients to the same performance as signals coming from a 4 : 2 : 2 source, or even more.

In order to obtain the point of inflection, the second derivative of the signal is calculated. The improved transition is centred with respect to the point of inflection of the original signal. Thus, there is no horizontal shift of the resulting signal.

The transition area length to be improved is controlled via I²C-bus by the bits LI1 and LI0 (Table 5); the sensitivity of the DCTI block is controlled by the bits GA1 and GA0. The CMO bit controls the colour detail sensitivity. It should be set to logic 1 (ON) if the video signal contains fine colour details (recommended operation mode).

Digital-to-Analog Converters (DACs)

Conversion is separate for Y, U and V. The converters use resistor chains with low-impedance output buffers.
The minimum output voltage is 200 mV to reduce integral non-linearity errors. The analog signal, without load on output pin, is between 0.2 and 2.2 V floating.
An application for 1 V/75 Ω on outputs is shown in Fig.14.

Each digital-to-analog converter has its own supply and ground pins suitable for decoupling. The reference voltage, supplying the resistor chain of all three DACs, is the supply voltage V_{DDA4}. The current into pin 41 is 0.3 mA; a larger current improves the bandwidth but increases the integral non-linearity.

I²C-bus format

Table 4 I²C-bus format; see notes 1 to 7

S	slave address	A	subaddress	A	data 0	A	...	data n	A	P

Notes

1. S = START condition.
2. Slave address = 1011 111X.
3. A = acknowledge; generated by the slave.
4. Subaddress = subaddress byte (Table 5);
   If more than 1 byte of DATA is transmitted, then auto-increment of the subaddress is performed.
5. Data = data byte (Table 5).
6. P = STOP condition.
7. X = R/$\overline{W}$ control bit:
   a) X = 0; order to write (the circuit is slave receiver).
   b) X = 1; order to read (the circuit is slave transmitter).

Table 5 I²C-bus transmission

SUBADDRESS	FUNCTION	DATA BITS							
		D7	D6	D5	D4	D3	D2	D1	D0
01	peaking and coring	AFB	CO1	CO0	BP1	BP0	BFB	WG1	WG0
02	input formats; interpolation	IFF	IFC	IFL	CMO	LI1	LI0	GA1	GA0
03	input/output setting	0	0	DC1	DC0	DRP	BLV	R78	INV

Table 6 Bit functions in data bytes

BIT	DESCRIPTION
CO1 and CO0	control of coring threshold; see Table 7
AFB, BP1, BP0, BFB	bandpass filter selection; see Table 8
BFB, WG1 and WG0	peaking factor K; see Table 9
IFF, IFC and IFL	input format and filter control at 13.5 MHz data rate; see Table 10
CMO	choice modification; 0 = modification off; 1 = modification on.
LI1 and LI0	DCTI timing range; see Table 11
GA1 and GA0	DCTI gain factor; see Table 12
DC1 and DC0	delay compensation of luminance signal; see Table 13
DRP	UV input data code; 0 = two's complement; 1 = offset binary
BLV	blanking level on Y output; 0 = 16 LSB; 1 = 0 LSB
R78	YUV input data solution; 0 = 7-bit data; 1 = 8-bit data
INV	polarity of colour-difference output signals: 0 = normal polarity equal to input signal 1 = inverted polarity

Table 7 Logic levels and function of CO1 and CO0

DATA BITS		FUNCTION
CO1	CO0	
0	0	coring off
0	1	small noise reduction
1	0	medium noise reduction
1	1	high noise reduction

Table 8 Logic levels and function of AFB, BP1, BP0 and BFB

DATA BITS				FUNCTION
AFB	BP1	BP0	BFB	
X	0	0	0	characteristic (see Fig.5)
X	0	1	0	characteristic (see Fig.6)
X	1	0	0	characteristic (see Fig.7)
X	1	1	0	characteristic (see Fig.8)
0	X	X	1	BF1 filter bypassed (see Fig.9a)
1	X	X	1	BF1 filter bypassed (see Fig.9b)

Table 9 Logic levels and function of BFB, WG1 and WG0

DATA BITS			FUNCTION
BFB	WG1	WG0	
0	0	0	K = 1/8; minimum peaking
0	0	1	K = 1/4
0	1	0	K = 1/2
0	1	1	K = 1; maximum peaking
1	0	0	K = 0; peaking off
1	0	1	K = 1/4; minimum peaking
1	1	0	K = 1/2
1	1	1	K = 1; maximum peaking

Table 10 Logic levels and function of IFF, IFC and IFL

DATA BITS			FUNCTION
IFF	IFC	IFL	
0	0	0	4 : 1 : 1 format; –3 dB attenuation at 1.6 MHz video frequency; (see Fig.10)
0	0	1	4 : 1 : 1 format; –3 dB attenuation at 600 kHz video frequency; (see Fig.11)
0	1	X	4 : 1 : 1 format; –3 dB attenuation at 1.2 MHz video frequency; (see Fig.12)
1	0	0	4 : 2 : 2 format; –3 dB attenuation at 1.6 MHz video frequency; (see Fig.10)
1	0	1	4 : 2 : 2 format; –3 dB attenuation at 600 kHz video frequency; (see Fig.11)
1	1	X	4 : 2 : 2 format; –3 dB attenuation at 2.5 MHz video frequency; (see Fig.13)

Table 11 Logic levels and function of LI1 and LI0

DATA BITS		RANGE
LI1	LI0	
0	0	+4 to –4
0	1	+6 to –6
1	0	+8 to –8
1	1	+12 to –12

Table 12 Logic levels and function of GA1 and GA0

DATA BITS		FACTOR
GA1	GA0	
0	0	off
0	1	1/4
1	0	1/2
1	1	1

Table 13 Logic levels and function of DC1 and DC0

DATA BITS		DELAYED CLOCK CYCLES
DC1	DC0	
0	0	0
0	1	+1
1	0	–2
1	1	–1

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDD1}	digital supply voltage 1 (pin 12)	−0.3	+7	V
V_{DDD2}	digital supply voltage 2 (pin 31)	−0.3	+7	V
V_{DDA1}	analog supply voltage 1 (pin 32)	−0.3	+7	V
V_{DDA2}	analog supply voltage 2 (pin 37)	−0.3	+7	V
V_{DDA3}	analog supply voltage 3 (pin 40)	−0.3	+7	V
V_{DDA4}	analog supply voltage 4 (pin 42)	−0.3	+7	V
V_{DDD}	digital supply voltage	−0.5	+7	V
ΔV_{GND}	difference voltage $V_{SSD} - V_{SSA}$	−	±100	mV
V_I	voltage on all input pins 4 to 11, 14 to 27 and 41	−0.3	V_{DDD}	V
V_O	voltage on analog output pins 33, 36 and 39	−0.3	V_{DDD}	V
V_{ESD}	electrostatic handling for all pins	±2000	−	V
P_{tot}	total power dissipation	0	tbf	mW
T_{stg}	storage temperature	−55	+150	°C
T_{amb}	operating ambient temperature	0	70	°C

Note

1. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	46	K/W

CHARACTERISTICS

V_{DDD} = 4.5 to 5.5 V; V_{DDA} = 4.75 to 5.25 V; LLC = LL27; MC = CREF = 13.5 MHz; T_{amb} = 0 to 70 °C; measurements taken in Fig.14; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDD1}	supply voltage range (pin 12)	for digital part	4.5	5	5.5	V
V_{DDD2}	supply voltage range (pin 31)	for digital part	4.5	5	5.5	V
V_{DDA1}	supply voltage range (pin 32)	for buffer of DAC 1	4.75	5	5.25	V
V_{DDA2}	supply voltage range (pin 37)	for buffer of DAC 2	4.75	5	5.25	V
V_{DDA3}	supply voltage range (pin 40)	for buffer of DAC 3	4.75	5	5.25	V
V_{DDA4}	supply voltage range (pin 42)	DAC reference voltage	4.75	5	5.25	V
I_{DDD}	supply current (I_{DDD1} + I_{DDD2})	for digital part	–	tbf	tbf	mA
I_{DDA}	supply current (I_{DDA1} + I_{DDA4})	for DACs and buffers	–	tbf	tbf	mA
YUV-bus inputs (pins 4 to 11 and 14 to 21) (see Figs 3 and 4)						
V_{IL}	LOW-level input voltage		−0.5	–	+0.8	V
V_{IH}	HIGH-level input voltage		2.0	–	V_{DDD} + 0.5	V
C_I	input capacitance	V_I = HIGH	–	–	10	pF
I_{LI}	input leakage current		–	–	4.5	µA
Inputs AP, SP, MC, LLC, HREF and $\overline{\text{RESET}}$ (pins 22 to 27)						
V_{IL}	LOW-level input voltage		−0.5	–	+0.8	V
V_{IH}	HIGH-level input voltage		2.0	–	V_{DDD} + 0.5	V
C_I	input capacitance	V_I = HIGH	–	–	10	pF
I_{LI}	input leakage current		–	–	4.5	µA
V_{24}	MC input voltage for LL27	27 MHz data rate	2.0	–	V_{DDD} + 0.5	V
	CREF signal on MC input	CREF data rate; note 1	–	–	–	V
I²C-bus SCL and SDA (pins 28 and 29)						
V_{IL}	LOW-level input voltage		−0.5	–	+1.5	V
V_{IH}	HIGH-level input voltage		3.0	–	V_{DDD} + 0.5	V
I_I	input current	V_I = LOW or HIGH	–	–	±10	µA
V_{ACK}	output voltage at acknowledge (pin 29)	I_{29} = 3 mA	–	–	0.4	V
I_{29}	output current	during acknowledge	3	–	–	mA
Digital-to-analog converters (pins 1, 2, 41, 42, 43 and 44)						
V_{DAC}	input reference voltage for internal resistor chains (pin 42)		4.75	5	5.25	V
I_{CUR}	input current (pin 41)	R_{41-42} = 15 kΩ	–	300	–	µA
$V_{1,44}$	reference voltage LOW	pin connected to V_{SSA1}	–	0	–	V
C_L	external blocking capacitor to V_{SSA1} for reference voltage HIGH (pins 2 and 43)		–	0.1	–	µF
f_{LLC}	data conversation rate (clock)	Fig.3	–	–	36	MHz

RES_{DAC}	resolution	luminance DAC	–	9	–	bits
		chrominance DACs	–	8	–	bits
ILE	DC integral linearity error	8-bit data	–	–	1.0	LSB
DLE	DC differential error	8-bit data	–	–	0.5	LSB
Y, (R – Y) and (B – Y) analog outputs (pins 33, 36 and 39)						
$V_{o(p-p)}$	output signal voltage (peak to peak value)	without load	–	2	–	V
$V_{33,36,39}$	output voltage range	without load; note 2	0.2	–	2.2	V
V_{39}	output blanking level	Y output; note 3	–	16	–	LSB
$V_{33,36}$	output no-colour level	±(R – Y), ±(B – Y); note 4	–	128	–	LSB
$R_{33,36,39}$	internal serial output resistance		–	25	–	Ω
$R_{L33,36,39}$	output load resistance	external load	125	–	–	Ω
B	output signal bandwidth	–3 dB	20	–	–	MHz
t_d	signal delay from input to Y output		–	tbf	–	ns
LCC timing (pin 25) (see Fig.3)						
T_{LLC}	cycle time		27.7	37	41	ns
$t_{p H}$	pulse width		40	50	60	%
t_r	rise time		–	–	5	ns
t_f	fall time		–	–	6	ns
YUV-bus timing (pins 4 to 11 and 14 to 21) (see Fig.5)						
$t_{SU;DAT}$	input data set-up time		10	–	–	ns
$t_{HD;DAT}$	input data hold time		3	–	–	ns
MC timing (pin 24) (see Fig.5)						
$t_{SU;DAT}$	input data set-up time		10	–	–	ns
$t_{HD;DAT}$	input data hold time		3	–	–	ns
$\overline{\text{RESET}}$ timing (pin 27)						
t_{SU}	set-up time after power-on or failure	active LOW; note 5	$4 \times t_{LLC}$	–	–	ns

Notes

1. YUV-bus data is read at MC = HIGH (pin 24) clocked with LLC (see Fig.5); data is read only with every second rising edge of LLC when CREF = ½LLC on pin 24.
2. 0.2 to 2.2 V output voltage range at 8-bit DAC input data; the data word can increase to 9-bit dependent on peaking factor.
3. The luminance signal is set to the digital black level: 16 LSB for BLV-bit = 0; 0 LSB for BLV-bit = 1.
4. The chrominance amplitudes are set to the digital colourless level of 128 LSB.
5. The circuit is prepared for a new data initialization.

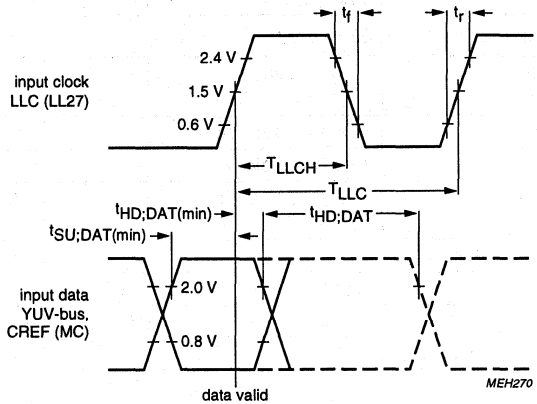
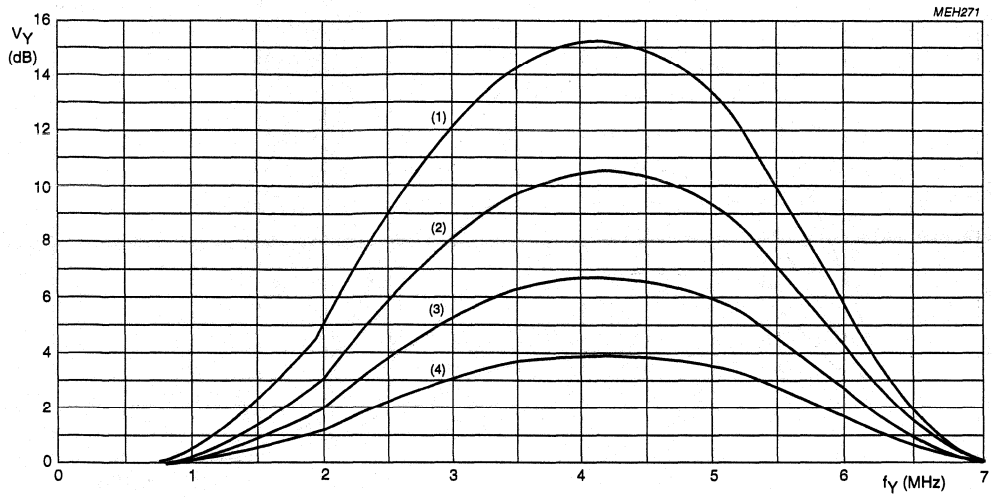


Fig.4 YUV-bus data and CREF timing.

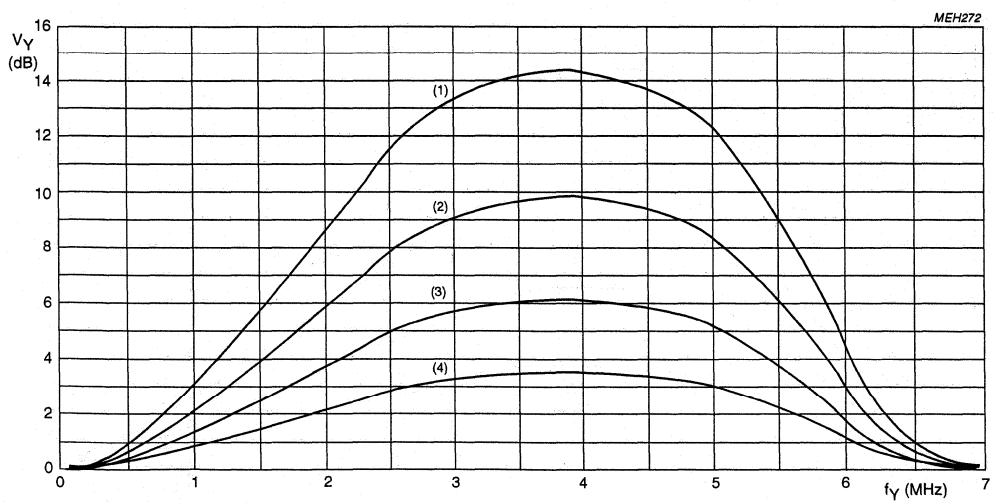
Table 14 YUV-bus data processing delay

PROCESSING DELAY	LLC CYCLES	REMARKS
YUV digital input	66	at MC = 1
YUV analog output	132	at MC = ½LLC



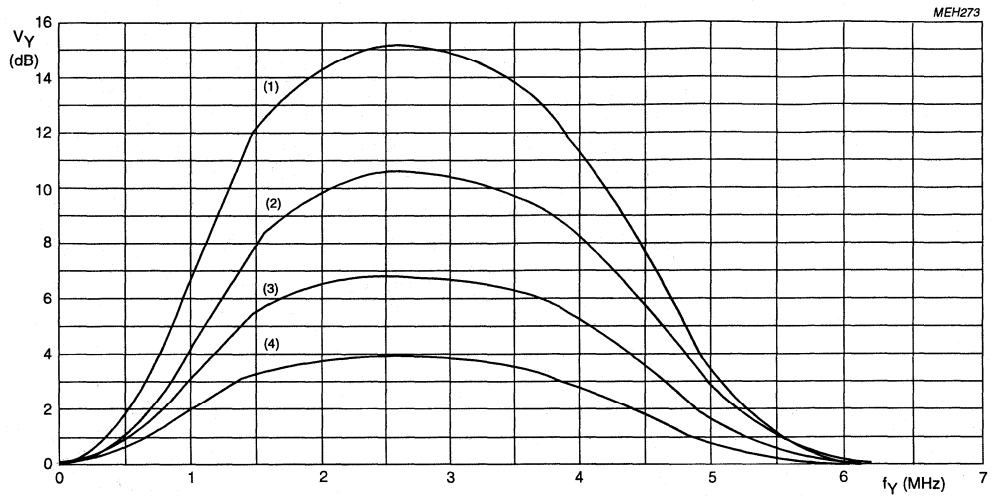
(1) K = 1
(2) K = ½
(3) K = ¼
(4) K = ⅛

Fig.5 Peaking frequency response with I²C-bus control bits BP1 = 0; BP0 = 0 and BFB = 0.



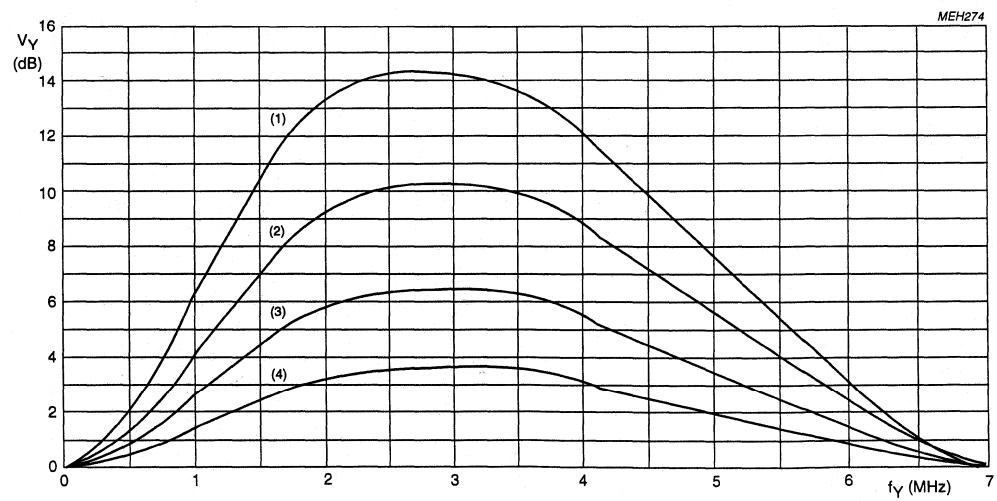
(1) K = 1
(2) K = ½
(3) K = ¼
(4) K = ⅛

Fig.6 Peaking frequency response with I²C-bus control bits BP1 = 0; BP0 = 1 and BFB = 0.



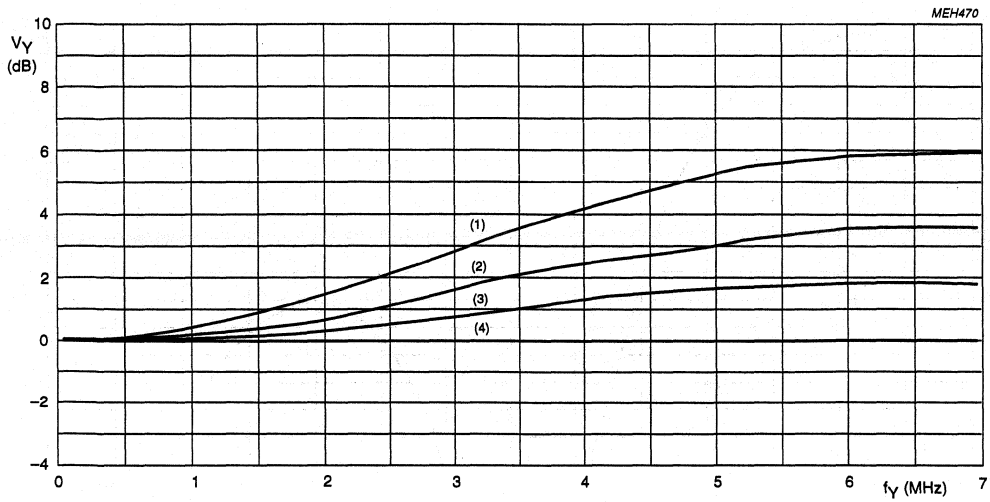
(1) K = 1
(2) K = ½
(3) K = ¼
(4) K = ⅛

Fig.7 Peaking frequency response with I²C-bus control bits BP1 = 1; BP0 = 0 and BFB = 0.

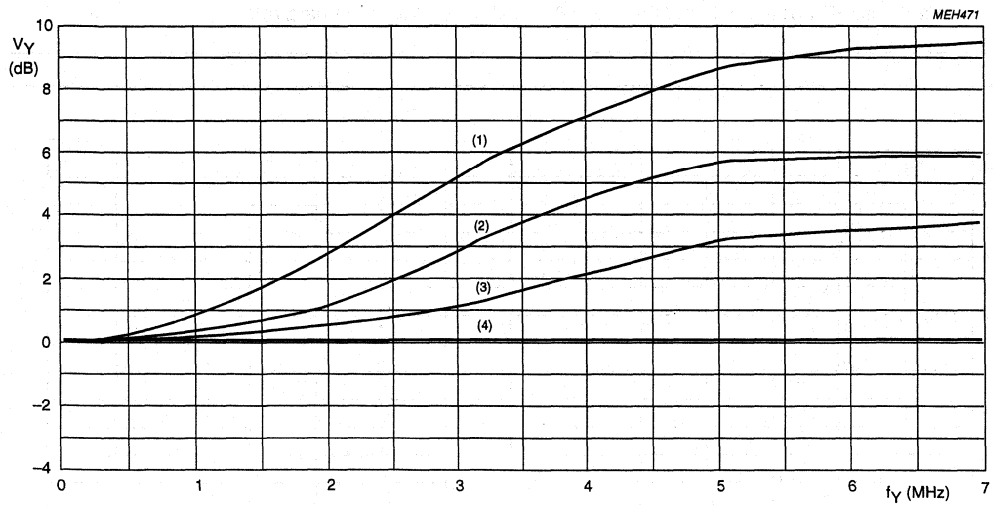


(1) K = 1
(2) K = ½
(3) K = ¼
(4) K = ⅛

Fig.8 Peaking frequency response with I²C-bus control bits BP1 = 1; BP0 = 1 and BFB = 0.



a. AFB = 0.



b. AFB = 1.

(1) K = 1
(2) K = ½
(3) K = ¼
(4) K = 0

Fig.9 Peaking frequency response with I²C-bus control bits BP1 = 0; BP0 = 0 and BFB = 1; bandpass filter BF1 bypassed and peaking off.

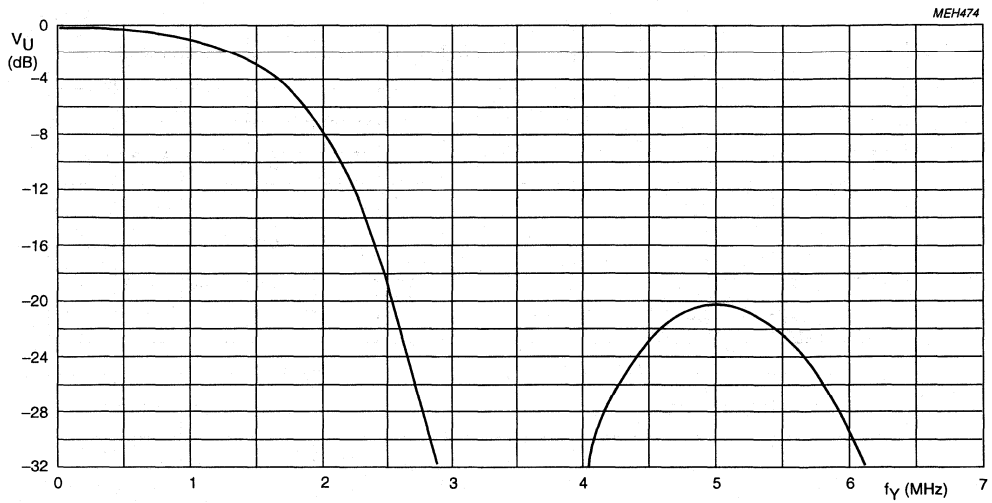


Fig.10 Interpolation filter at DCTI off with I²C-bus control bits IFF = 0; IFC = 0 and IFL = 0 in 4 : 1 : 1 format and control bits IFF = 1; IFC = 0 and IFL = 0 in 4 : 2 : 2 format; 13.5 MHz data rate.

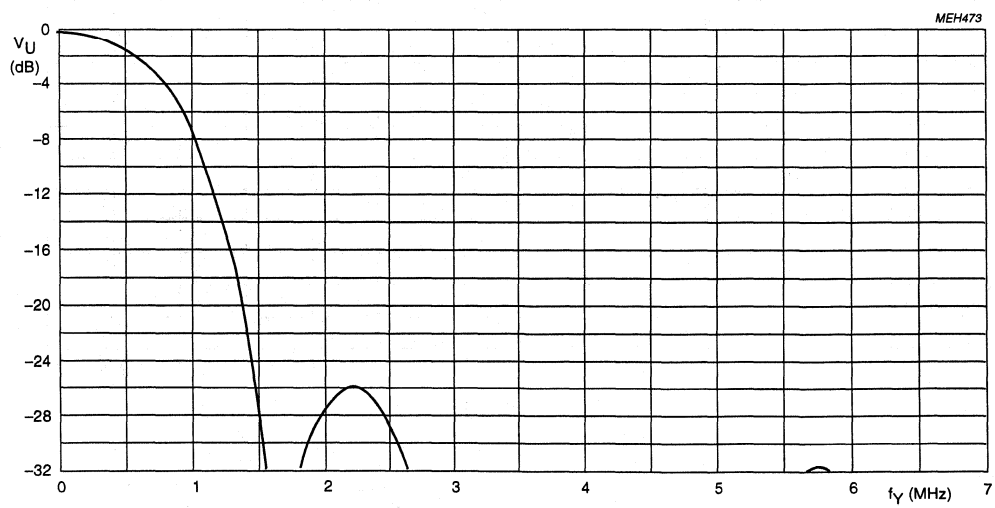


Fig.11 Interpolation filter at DCTI off with I²C-bus control bits IFF = 0; IFC = 0 and IFL = 1 in 4 : 1 : 1 format and control bits IFF = 1; IFC = 0 and IFL = 1 in 4 : 2 : 2 format; 13.5 MHz data rate.

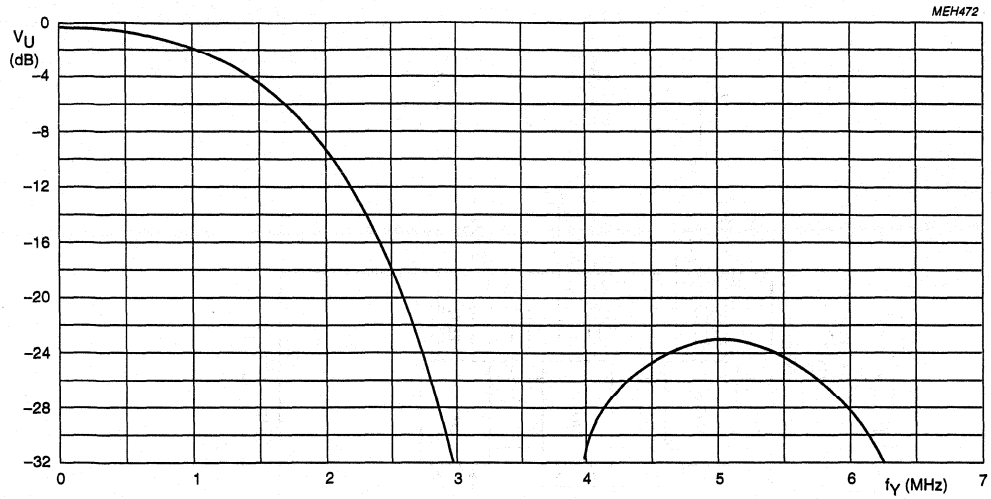


Fig.12 Interpolation filter at DCTI off with I²C-bus control bits IFF = 0; IFC = 1 and IFL = 0 in 4 : 1 : 1 format; 13.5 MHz data rate.

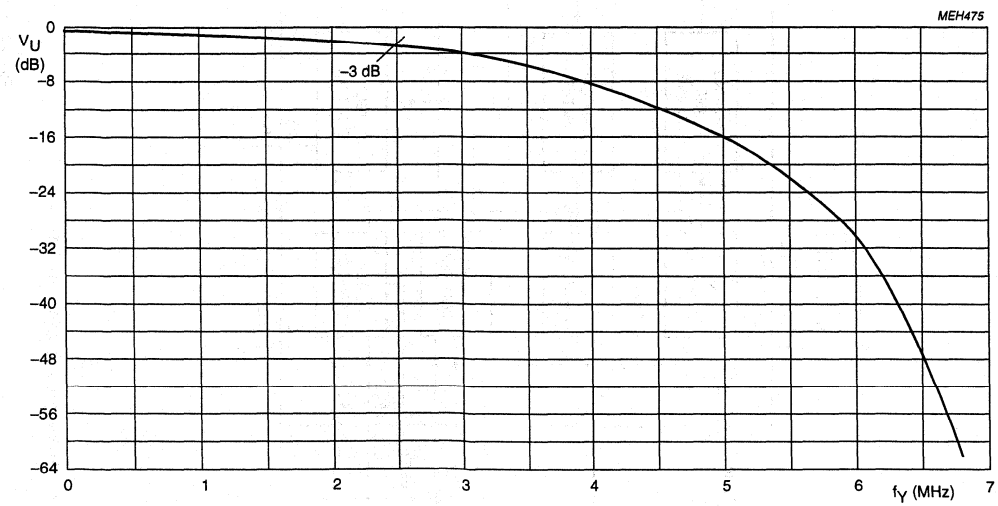


Fig.13 Interpolation filter with I²C-bus control bits IFF = 1; IFC = 1 and IFL = X in 4 : 2 : 2 format; 13.5 MHz data rate.

APPLICATION INFORMATION

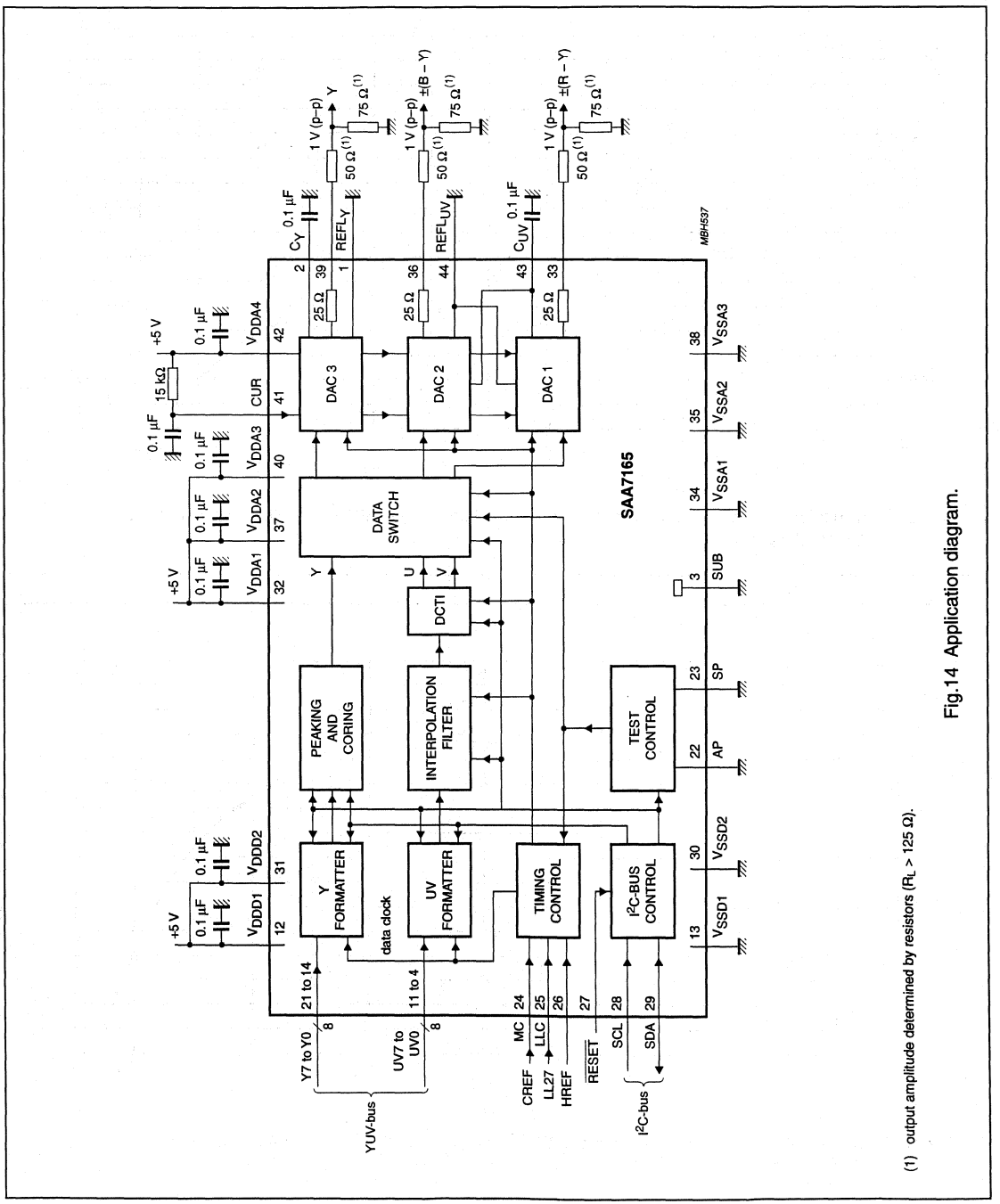


Fig.14 Application diagram.

(1) output amplitude determined by resistors (R_L > 125 Ω).

YUV-to-RGB Digital-to-Analog Converter DAC

SAA7167A

FEATURES

- On-chip mixing of digital video data and analog RGB signals
- Supports video input format of YUV 4 : 2 : 2, 4 : 1 : 1, 2 : 1 : 1 and RGB 5 : 6 : 5
- Video input rate up to 66 MHz
- Allows for both binary and two's complement video input data
- Triple 8-bit DACs for video output
- Built-in voltage output amplifier
- Provide keying control with external key and internal 8-bit, 2 × 8-bit and 3 × 8-bit pixel colour key
- Programmable via the I²C-bus
- 5 V CMOS device; LQFP48 package.

GENERAL DESCRIPTION

The SAA7167A is a mixed-mode designed IC containing a video data path, keying control block, analog mixer, and a voltage output amplifier, capable of converting digital video data to analog RGB video, and then mixing video and external analog RGB inputs.

The video data path contains a data re-formatter, YUV-to-RGB colour space matrix as well as triple DACs for video data processing. An analog mixer performs multiplexing between DAC outputs of the video path and external analog RGB inputs.

The final analog outputs are buffered with built-in voltage output amplifiers to provide the direct driving capability for a 150 Ω load. Figure 1 shows the overall block diagram.

The operation of SAA7167 is controlled via the I²C-bus.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDD}	digital supply voltage	4.75	5.25	V
V_{DDA}	analog supply voltage	4.75	5.25	V
T_{amb}	operating ambient temperature	0	70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7167A	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

BLOCK DIAGRAM

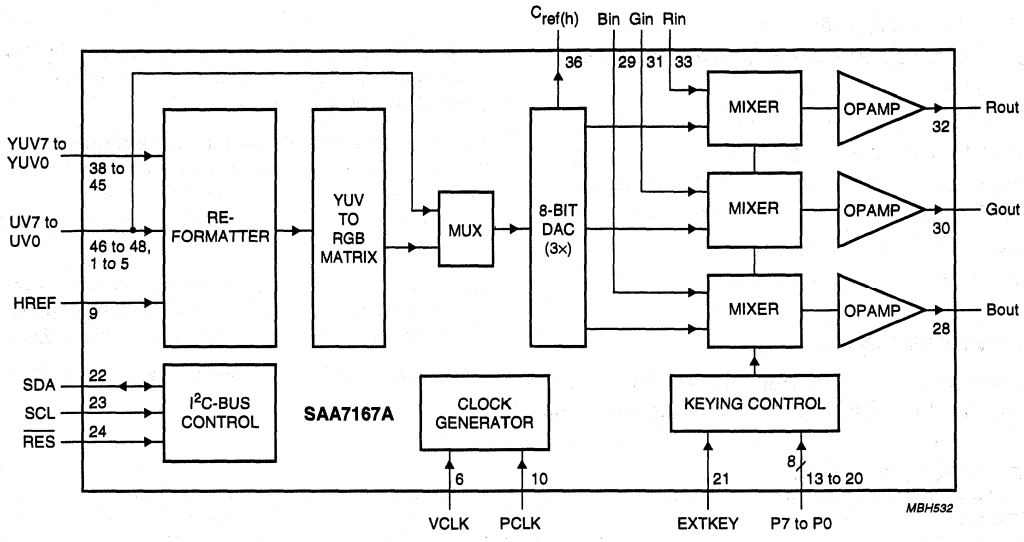


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION	I/O
UV4	1	digital video UV (of YUV format 4 : 1 : 1 and 4 : 2 : 2) input data, or digital G and R input data	I
UV3	2	digital video UV (of YUV format 4 : 1 : 1 and 4 : 2 : 2) input data, or digital G and R input data	I
UV2	3	digital video UV (of YUV format 4 : 1 : 1 and 4 : 2 : 2) input data, or digital G and R input data	I
UV1	4	digital video UV (of YUV format 4 : 1 : 1 and 4 : 2 : 2) input data, or digital G and R input data	I
UV0	5	digital video UV (of YUV format 4 : 1 : 1 and 4 : 2 : 2) input data, or digital G and R input data	I
VCLK	6	video clock input	I
V_{DDD}	7	digital supply voltage	I/O
V_{SSD}	8	digital ground	I/O
HREF	9	horizontal reference input signal	I
PCLK	10	pixel clock input	I
AP	11	test pins, normally connected to ground	I
SP	12	test pins, normally connected to ground	I
P7	13	pixel bus input 7 (for keying control)	I
P6	14	pixel bus input 6 (for keying control)	I
P5	15	pixel bus input 5 (for keying control)	I
P4	16	pixel bus input 4 (for keying control)	I
P3	17	pixel bus input 3 (for keying control)	I
P2	18	pixel bus input 2 (for keying control)	I
P1	19	pixel bus input 1 (for keying control)	I
P0	20	pixel bus input 0 (for keying control)	I
EXTKEY	21	external key signal input	I
SDA	22	I^2C-bus data line	I/O
SCL	23	I^2C-bus clock line	I
$\overline{RES}$	24	set to LOW to reset the I^2C-bus	I
n.c.	25	not connected	–
V_{SSA2}	26	analog ground 2	I/O
V_{DDA2}	27	analog supply voltage 2	I/O
Bout	28	analog Blue signal output	O
Bin	29	analog Blue signal input	I
Gout	30	analog Green signal output	O
Gin	31	analog Green signal input	I
Rout	32	analog Red signal output	O
Rin	33	analog Red signal input	I
V_{SSA1}	34	analog ground 1	I/O
V_{DDA1}	35	analog supply voltage 1	I/O
$C_{ref(h)}$	36	capacitor for reference high voltage output (2.25 V)	I/O

SYMBOL	PIN	DESCRIPTION	I/O
n.c.	37	not connected	–
YUV7	38	digital video Y or UV (of YUV format 2 : 1 : 1) input data, or digital G and B input data	I
YUV6	39	digital video Y or UV (of YUV format 2 : 1 : 1) input data, or digital G and B input data	I
YUV5	40	digital video Y or UV (of YUV format 2 : 1 : 1) input data, or digital G and B input data	I
YUV4	41	digital video Y or UV (of YUV format 2 : 1 : 1) input data, or digital G and B input data	I
YUV3	42	digital video Y or UV (of YUV format 2 : 1 : 1) input data, or digital G and B input data	I
YUV2	43	digital video Y or UV (of YUV format 2 : 1 : 1) input data, or digital G and B input data	I
YUV1	44	digital video Y or UV (of YUV format 2 : 1 : 1) input data, or digital G and B input data	I
YUV0	45	digital video Y or UV (of YUV format 2 : 1 : 1) input data, or digital G and B input data	I
UV7	46	digital video UV (of YUV format 4 : 1 : 1 and 4 : 2 : 2) input data, or digital G and R input data	I
UV6	47	digital video UV (of YUV format 4 : 1 : 1 and 4 : 2 : 2) input data, or digital G and R input data	I
UV5	48	digital video UV (of YUV format 4 : 1 : 1 and 4 : 2 : 2) input data, or digital G and R input data	I

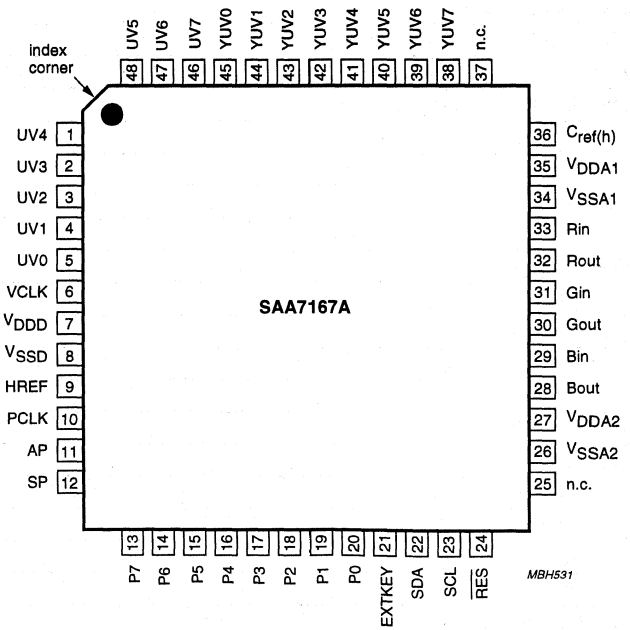


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The SAA7167A contains a video data path, 3 analog mixers and voltage output amplifiers for the RGB channels respectively, a keying control block as well as an I²C-bus control block.

Video data path

The video data path includes a video data re-formatter, a YUV-to-RGB colour space conversion matrix, and triple 8-bit DACs.

RE-FORMATTER

The re-formatter de-multiplexes the different video formats YUV 4 : 1 : 1, 4 : 2 : 2 or 2 : 1 : 1 to internal YUV 4 : 4 : 4, which can then be processed by the RGB matrix. The pixel byte sequences of those video input formats are shown in Tables 1 to 4.

Table 1 Pixel byte sequence of 4 : 2 : 2

INPUT	PIXEL BYTE SEQUENCE OF 4 : 2 : 2					
YUV0 (LSB)	Y0	Y0	Y0	Y0	Y0	Y0
YUV1	Y1	Y1	Y1	Y1	Y1	Y1
YUV2	Y2	Y2	Y2	Y2	Y2	Y2
YUV3	Y3	Y3	Y3	Y3	Y3	Y3
YUV4	Y4	Y4	Y4	Y4	Y4	Y4
YUV5	Y5	Y5	Y5	Y5	Y5	Y5
YUV6	Y6	Y6	Y6	Y6	Y6	Y6
YUV7 (MSB)	Y7	Y7	Y7	Y7	Y7	Y7
UV0 (LSB)	U0	V0	U0	V0	U0	V0
UV1	U1	V1	U1	V1	U1	V1
UV2	U2	V2	U2	V2	U2	V2
UV3	U3	V3	U3	V3	U3	V3
UV4	U4	V4	U4	V4	U4	V4
UV5	U5	V5	U5	V5	U5	V5
UV6	U6	V6	U6	V6	U6	V6
UV7 (MSB)	U7	V7	U7	V7	U7	V7
Y data	0	1	2	3	4	5
UV data	0		2		4	

Table 2 Pixel byte sequence of 4 : 1 : 1

INPUT	PIXEL BYTE SEQUENCE OF 4 : 1 : 1							
YUV0	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0
YUV1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1
YUV2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2
YUV3	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3
YUV4	Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4
YUV5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5
YUV6	Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6
YUV7	Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7
UV0	X	X	X	X	X	X	X	X
UV1	X	X	X	X	X	X	X	X
UV2	X	X	X	X	X	X	X	X
UV3	X	X	X	X	X	X	X	X
UV4	V6	V4	V2	V0	V6	V4	V2	V0
UV5	V7	V5	V3	V1	V7	V5	V3	V1
UV6	U6	U4	U2	U0	U6	U4	U2	U0
UV7	U7	U5	U3	U1	U7	U5	U3	U1
Y data	0	1	2	3	4	5	6	7
UV data	0				4			

Table 3 Pixel byte sequence of 2 : 1 : 1

INPUT	PIXEL BYTE SEQUENCE OF 2 : 1 : 1							
YUV0	U0	Y0	V0	Y0	U0	Y0	V0	Y0
YUV1	U1	Y1	V1	Y1	U1	Y1	V1	Y1
YUV2	U2	Y2	V2	Y2	U2	Y2	V2	Y2
YUV3	U3	Y3	V3	Y3	U3	Y3	V3	Y3
YUV4	U4	Y4	V4	Y4	U4	Y4	V4	Y4
YUV5	U5	Y5	V5	Y5	U5	Y5	V5	Y5
YUV6	U6	Y6	V6	Y6	U6	Y6	V6	Y6
YUV7	U7	Y7	V7	Y7	U7	Y7	V7	Y7
Y data	X	0	X	2	X	4	X	6
UV data	0	X	0	X	4	X	4	X

Table 4 Pixel byte sequence of 5 : 6 : 5

INPUT	PIXEL BYTE SEQUENCE OF RGB 5 : 6 : 5			
UV7	G0	G0	G0	G0
UV6	R4	R4	R4	R4
UV5	R3	R3	R3	R3
UV4	R2	R2	R2	R2
UV3	R1	R1	R1	R1
UV2	R0	R0	R0	R0
UV1	G5	G5	G5	G5
UV0	G4	G4	G4	G4
YUV7	G3	G3	G3	G3
YUV6	G2	G2	G2	G2
YUV5	G1	G1	G1	G1
YUV4	B4	B4	B4	B4
YUV3	B3	B3	B3	B3
YUV2	B2	B2	B2	B2
YUV1	B1	B1	B1	B1
YUV0	B0	B0	B0	B0
RGB data	0	1	2	3

For RGB 5 : 6 : 5 video inputs, the video data are just directly bypassed to triple DACs.

The input video data can be selected to either two's complement (I^2C-bus DRP-bit = 0) or binary offset (DRP-bit = 1). The video input format is selected by I^2C-bus bits FMTC1 and FMTC0.

The rising edge of HREF input defines the start of active video data. When HREF is inactive, the video output will be blanked.

YUV-TO-RGB MATRIX

The matrix converts YUV data, in accordance with CCIR-601, to RGB data with approximately 1.5 LSB deviation to the theoretical values for 8-bit resolution.

TRIPLE 8-BIT DACS

Three identical DACs for R, G and B video outputs are designed with voltage-drive architecture to provide high-speed operation of up to 66 MHz conversion data rate. A $C_{ref(h)}$ pin is provided to allow for one external de-coupling capacitor to be connected between the internal reference voltage source and ground.

Analog mixers and keying control

The analog mixers are controlled to switch between the outputs from the video DACs and analog RGB inputs by a keying signal. The analog RGB inputs need to interface with analog mixers in the way of DC-coupling, also these RGB inputs are limited to RGB signals without a sync level pedestal. The keying control can be enabled by setting I^2C bit KEN = 1. Two kinds of keying are possible to generate: one is external key (from EXTKEY pin when KMOD2 to KMOD0 are logic 0), and the other is the internal pixel colour key (when KMOD2 to KMOD0 are not logic 0) generated by comparing the input pixel data with the internal I^2C-bus register value KD7 to KD0. Controlled by KMOD2 to KMOD0 bits, there are 4 ways to compare the pixel data (see Table 5).

Table 5 KMOD2 to KMOD0

KMOD2 to KMOD0	PIXEL TYPE	REMARK
1 0 0	8-bit pixel	pseudo colour mode
1 0 1	2 × 8-bit pixel	high colour mode 1 with pixels given at both rising and falling edges of PCLK
1 1 0	2 × 8-bit pixel	high colour mode 2 with pixels given only at rising edges of PCLK
1 1 1	3 × 8-bit pixel	true colour mode

Since only one control register KD7 to KD0 provides the data value for pixel data comparison, when at 2 × 8-bit or 3 × 8-bit pixel input modes, it is presumed that all input bytes (lower, middle, or higher) of each pixel must be same as KD7 to KD0 in order to make graphics colour key active.

The polarity of EXTKEY can be selected with KINV. With KINV = 0, EXTKEY = HIGH switches analog mixers to select DAC outputs. Before the internal keying signal switches the analog multiplexers, it can be further delayed up to 7 PCLK cycles with the control bits KDLY2 to KDLY0.

Voltage output amplifiers

Before the analog input enters the analog mixers, it passes through voltage output amplifiers. Level shifters are used internally to provide an offset of 0.2 V and an amplifier gain of 2 for analog inputs to match with the output levels from DACs. After buffering with voltage output amplifiers, the final RGB outputs can drive a 150 Ω load directly (25 Ω internal resistor, 50 Ω external serial resistor, and 75 Ω load resistor at monitor side (see Fig.9).

The output voltage level of DAC ranges from the lowest level 0.2 V (zero code) to the highest level 1.82 V (all one code).

With the digital input YUV video data in accordance with CCIR-601, the RGB output of 8-bit DAC actually ranges from the 16th step (black) to the 235th step (white). Therefore, after the voltage divider with external serial resistor and monitor load resistor, the output voltage range to monitor is approximately 0.7 V (peak-to-peak).

I²C-bus control

Only one control byte is needed for the SAA7167A.
The I²C-bus format is shown in Table 6.

Table 6 I²C-bus format; see notes 1 to 7

S	slave address	A	subaddress	A	data	A	P

Notes

1. S = START condition.
2. Slave address = 1011 111X; this slave address is identical to the one for the SAA9065.
3. A = acknowledge; generated by the slave.
4. Subaddress = subaddress byte.
5. Data = data byte.
6. P = STOP condition.
7. X = R/$\overline{W}$ control bit:
   a) X = 0; order to write.
   b) X = 1; order to read (not used for SAA7167A).

Table 7 Control data byte

SUBADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
00	KMOD2	KMOD1	KMOD0	DRP	KEN	KINV	FMTC1	FMTC0
01	0	0	0	0	0	KDLY2	KDLY1	KDLY0
02	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0

Table 8 Bit functions in data byte; notes 1 and 2

BIT	DESCRIPTION
FMTC1 and FMTC0	video format control: 00; YUV 4 : 2 : 2 01; YUV 4 : 1 : 1 10; YUV 2 : 1 : 1/CCIR-656 11; RGB 5 : 6 : 5
KINV	key polarity: KINV = 0: EXTKEY = HIGH for analog mixer to select DAC outputs KINV = 1: EXTKEY = HIGH for analog mixer to select analog RGB inputs
KEN	key enable: 0 = disable 1 = enable
DRP	UV input data code: 0 = two's complement; 1 = binary offset
KMOD2 to KMOD0	keying mode: 000; external key 100; 8-bit pixel colour key 101; 2 × 8-bit pixel colour key (with two-edge clock latching for pixel input) 110; 2 × 8-bit pixel colour key (with one-edge clock latching for pixel input) 111; 3 × 8-bit pixel colour key (with one-edge clock latching for pixel input) all other combinations are reserved
KDLY2 to KDLY0	added keying delay cycles (from 0 to 7 PCLK)
KD7 to KD0	the data value compared for 8, 16 or 24-bit pixel colour key

Notes

1. All I²C-bus control bits are initialized to logic 0 after $\overline{RES}$ is activated.
2. PCLK should be active in any event to allow for correct operation of I²C-bus programming.

DC CHARACTERISTICS

T_{amb} = 0 to 70 °C.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage	4.75	5.0	5.25	V
V_{DDA}	analog supply voltage	4.75	5.0	5.25	V
I_{DDtot}	total supply current (f_{clk} = 66 MHz)	–	105	–	mA
V_{IH}	HIGH level input voltage (pin SDA)	3	–	V_{DDD} + 0.5	V
V_{IL}	LOW level input voltage (pin SDA)	−0.5	–	+1.5	V
V_{IH}	HIGH level digital input voltage	2	–	–	V
V_{IL}	LOW level digital input voltage	–	–	0.8	V
V_{in}	full-scale analog RGB inputs	–	0.7	–	V
V_{out}	full scale analog RGB outputs (for 150 Ω load)	–	1.4	–	V
DNL	differential non-linearity error of video output	–	–	1	LSB
INL	integral non-linearity error of video output	–	–	1	LSB

AC CHARACTERISTICS

T_{amb} = 0 to 70 °C.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VCLK					
f_{clk}	video clock rate	–	–	66	MHz
δ	duty factor of VCLK	40	50	60	%
PCLK					
f_{clk}	pixel clock rate				
	8-bit pixel colour key; see Fig.4	–	–	77.5	MHz
	2 × 8-bit pixel colour key; mode 1; see Fig.5	–	–	50	MHz
	2 × 8-bit pixel colour key; mode 2; see Fig.6	–	–	80	MHz
	3 × 8-bit pixel colour key; see Fig.7	–	–	77.5	MHz
δ	duty factor of PCLK	40	50	60	%
t_{su1}	digital input set-up time to VCLK rising edge	3	–	–	ns
t_{h1}	digital input hold time to VCLK rising edge	2	–	–	ns
t_{su2}	digital input set-up time to PCLK rising edge	0	–	–	ns
t_{h2}	digital input hold time to PCLK rising edge	4.2	–	–	ns
t_{su3}	digital input set-up time to PCLK falling edge	−1	–	–	ns
t_{h3}	digital input hold time to PCLK falling edge	6	–	–	ns
t_{sw}	switching time between video DAC/analog inputs; note 1	–	–	15	ns
T_{group}	overall group delay from digital video inputs to analog outputs (see Fig.8):				
	YUV video input mode	–	$20T_{VCLK} + t_{PD}$	–	ns
	RGB video input mode	–	$12T_{VCLK} + t_{PD}$	–	ns
t_r	DAC analog output rise time (see Fig.8); note 2	–	3.5	–	ns
t_f	DAC analog output fall time (see Fig.8); note 2	–	3.5	–	ns
t_s	DAC analog output settling time (see Fig.8); note 3	–	16.5	–	ns
t_{PD}	DAC analog output propagation delay (see Fig.8); note 4	–	20	–	ns
Analog outputs from analog inputs					
G_v	voltage gain	–	2.0	–	
B	bandwidth (−3 dB)	160	–	–	MHz
SR	slew rate	100	110	–	V/µs

Notes

1. Switching time measured from the 50% point of the EXTKEY transition edge to the 50% point of the selected analog output transition.
2. DAC output rise/fall time measured between the 10% and 90% points of full scale transition.
3. DAC settling time measured from the 50% point of full-scale transition to the output remaining within ±1 LSB.
4. DAC analog output propagation delay measured from the 50% point of the rising edge of VCLK to the 50% point of full-scale transition.

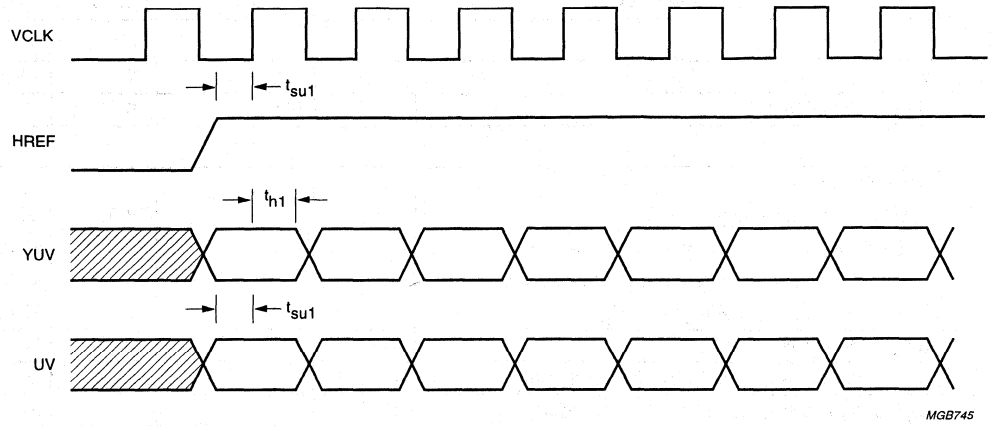


Fig.3 Video data input timing.

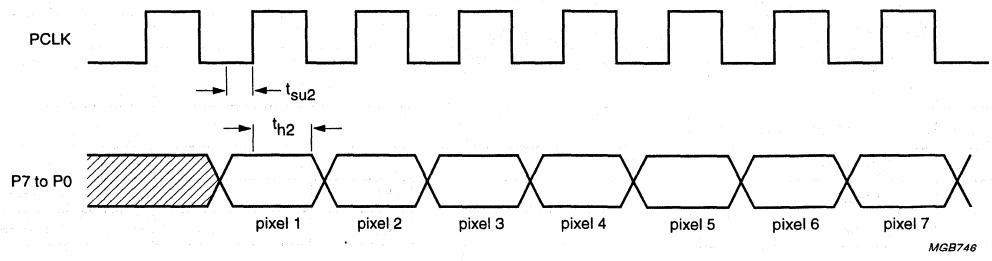


Fig.4 Pixel data timing; 8-bit pixel colour key.

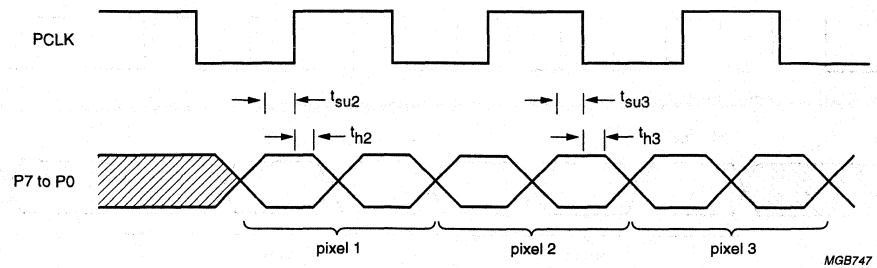


Fig.5 Pixel data input timing; 2 × 8-bit pixel colour key; mode 1.

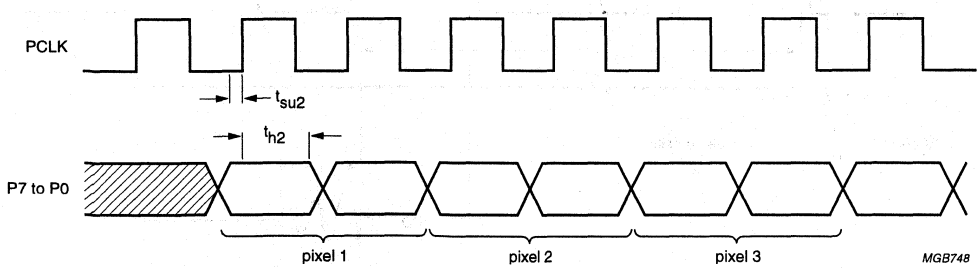


Fig.6 Pixel data input timing; 2 × 8-bit pixel colour key; mode 2.

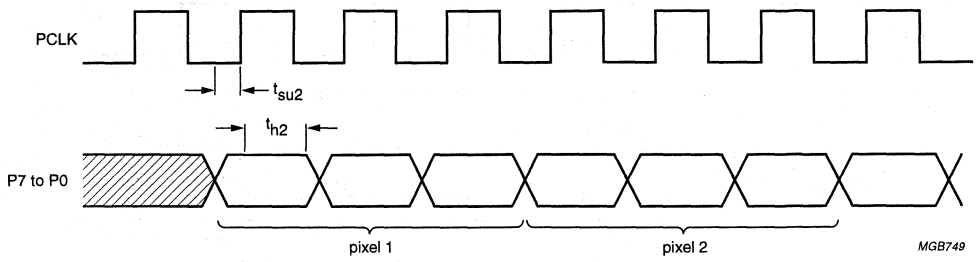


Fig.7 Pixel data input timing; 3 × 8-bit pixel colour key.

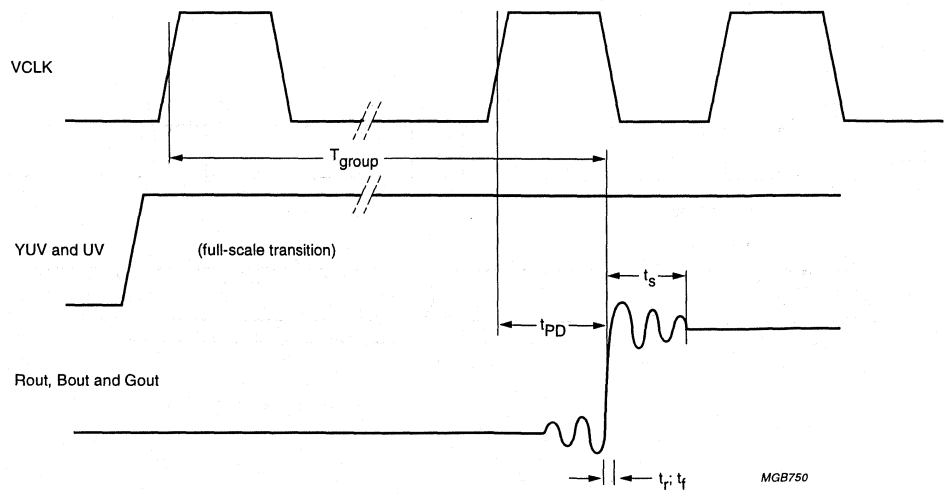


Fig.8 DAC output timing.

APPLICATION INFORMATION

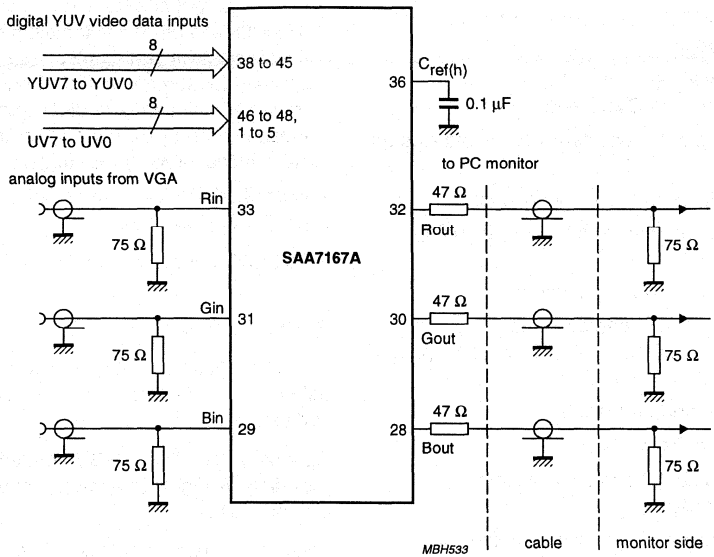


Fig.9 Typical application diagram for analog circuits.

Digital Video Encoder (EURO-DENC2) SAA7182A; SAA7183A

FEATURES

- Monolithic CMOS 3.3 V device with 5 V input stages
- Digital PAL/NTSC/SECAM encoder
- System pixel frequency 13.5 MHz
- Accepts MPEG decoded data on 8-bit wide input port. Input data format Cb, Y, Cr etc. "*(CCIR 656)*" or Y and Cb, Cr on 16 lines
- Three DACs for CVBS, Y and C operating at 27 MHz with 10 bit resolution
- Three DACs for RGB operating at 27 MHz with 9 bit resolution, RGB sync on CVBS and Y
- Analog multiplexing between internal RGB and external RGB on-chip
- CVBS, Y, C and RGB output simultaneously
- Closed captioning and teletext encoding including sequencer and filter
- Line 23 wide screen signalling encoding
- On-chip Cr, Y, Cb to RGB dematrix, including gain adjustment for Y and Cr, Cb, optionally to be by-passed for Cr, Y, Cb output on RGB DACs
- Fast I²C-bus control port (400 kHz)
- Encoder can be master or slave
- Programmable horizontal and vertical input synchronization phase
- Programmable horizontal sync output phase
- Internal Colour Bar Generator (CBG)
- Overlay with Look-Up Tables (LUTs) 8 × 3 bytes
- Macrovision Pay-per-View copy protection system as option, also used for RGB output.

This applies to SAA7183A only. The device is protected by USA patent numbers 4631603, 4577216 and 4819098 and other intellectual property rights. Use of the Macrovision anti-copy process in the device is licensed for non-commercial home use only. Reverse engineering or disassembly is prohibited. Please contact your nearest Philips Semiconductor sales office for more information

- Controlled rise/fall times of output syncs and blanking
- Down-mode of DACs
- PQFP80 or PLCC84 package.

GENERAL DESCRIPTION

The SAA7182A; SAA7183A encodes digital YUV video data to an NTSC, PAL, SECAM CVBS or S-Video signal and also RGB.

Optionally, the YUV to RGB dematrix can be by-passed providing the digital-to-analog converted Cb, Y, Cr signals instead of RGB.

The circuit accepts CCIR compatible YUV data with 720 active pixels per line in 4 : 2 : 2 multiplexed formats, for example MPEG decoded data. It includes a sync/clock generator and on-chip Digital-to-Analog Converters (DACs).

The circuit is compatible to the DIG-TV2 chip family.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7182AWP; SAA7183AWP	PLCC84	plastic leaded chip carrier; 84 leads	SOT189-2
	QFP80	plastic quad flat package; 80 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT318-2

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDA3}	3.3 V analog supply voltage	3.1	3.3	3.5	V
V_{DDD3}	3.3 V digital supply voltage	3.0	3.3	3.6	V
V_{DDD5}	5 V digital supply voltage	4.75	5.0	5.25	V
I_{DDA}	analog supply current	–	–	110	mA
I_{DDD3}	3.3 V digital supply current	–	–	80	mA
I_{DDD5}	5 V digital supply current	–	–	10	mA
V_i	input signal voltage levels	TTL compatible			
$V_{o(p-p)}$	analog output signal voltages Y, C, CVBS and RGB without load (peak-to-peak value)	–	1.4	–	V
R_L	load resistance	75	–	300	Ω
ILE	LF integral linearity error	–	–	±2	LSB
DLE	LF differential linearity error	–	–	±1	LSB
T_{amb}	operating ambient temperature	0	–	+70	°C

BLOCK DIAGRAM

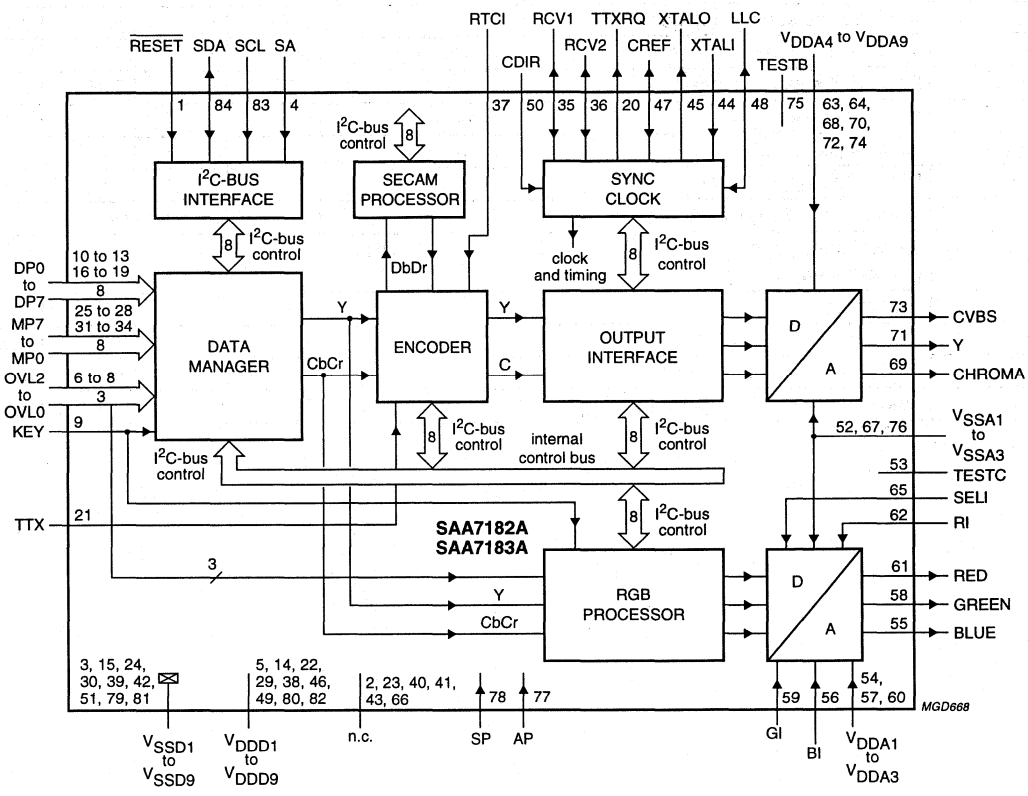


Fig.1 Block diagram; PLCC84.

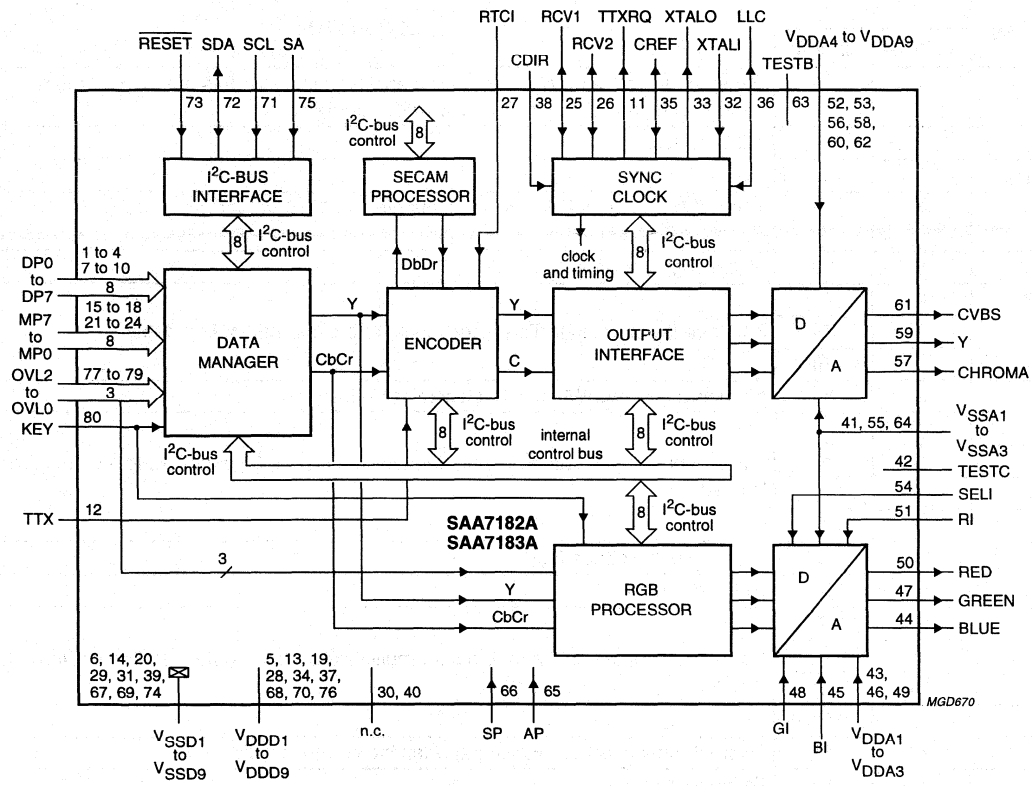


Fig.2 Block diagram; QFP80.

PINNING

SYMBOL	PIN		DESCRIPTION
	PLCC84	QFP80	
$\overline{RESET}$	1	73	Reset input, active LOW. After reset is applied, all digital I/Os are in input mode. The I²C-bus receiver waits for the START condition.
n.c.	2	–	not connected
V_{SSD1}	3	6	digital ground 1
SA	4	75	The I²C-bus slave address select input pin. LOW: slave address = 88H, HIGH = 8CH.
V_{DDD1}	5	13	digital supply voltage 1 (3.3 V)
OVL2	6	77	3-bit overlay data input. This is the index for the internal look-up table.
OVL1	7	78	
OVL0	8	79	
KEY	9	80	Key input for OVL. When HIGH it selects OVL input.
DP0	10	1	Lower 4 bits of the data port. Input for multiplexed Cb, Cr data if 16 line input mode is used.
DP1	11	2	
DP2	12	3	
DP3	13	4	
V_{DDD2}	14	5	digital supply voltage 2 (5 V)
V_{SSD2}	15	14	digital ground 2
DP4	16	7	Upper 4 bits of the data port. Input for multiplexed Cb, Cr data if 16 line input mode is used.
DP5	17	8	
DP6	18	9	
DP7	19	10	
TTXRQ	20	11	Teletext request output, indicating when bit stream is valid.
TTX	21	12	Teletext bit stream input.
V_{DDD3}	22	28	digital supply voltage 3 (3.3 V)
n.c.	23	–	not connected
V_{SSD3}	24	20	digital ground 1
MP7	25	15	Upper 4 bits of MPEG port. It is an input for "*CCIR 656*" style multiplexed Cb, Y, Cr data, or for Y data only, if 16 line input mode is used.
MP6	26	16	
MP5	27	17	
MP4	28	18	
V_{DDD4}	29	19	digital supply voltage 4 (5 V)
V_{SSD4}	30	29	digital ground 4
MP3	31	21	Lower 4 bits of MPEG port. It is an input for "*CCIR 656*" style multiplexed Cb, Y, Cr data, or for Y data only, if 16 line input mode is used.
MP2	32	22	
MP1	33	23	
MP0	34	24	
RCV1	35	25	Raster Control 1 for video port. This pin receives/provides a VS/FS/FSEQ signal.
RCV2	36	26	Raster Control 2 for video port. This pin provides an HS pulse of programmable length or receives an HS pulse.

SYMBOL	PIN		DESCRIPTION
	PLCC84	QFP80	
RTCI	37	27	Real Time Control input. If the LLC clock is provided by an SAA7111 or SAA7151B, RTCI should be connected to the RTCO pin of the respective decoder to improve the signal quality.
V_{DDD5}	38	68	digital supply voltage 5 (3.3 V)
V_{SSD5}	39	39	digital ground 5
n.c.	40	40	not connected
n.c.	41	–	not connected
V_{SSD6}	42	31	digital ground 6 for oscillator
n.c.	43	30	not connected
XTALI	44	32	Crystal oscillator input (from crystal). If the oscillator is not used, this pin should be connected to ground.
XTALO	45	33	Crystal oscillator output (to crystal).
V_{DDD6}	46	34	digital supply voltage 6 for oscillator (3.3 V)
CREF	47	35	Clock Reference signal. This is the clock qualifier for DIG-TV2 compatible signals.
LLC	48	36	Line-Locked Clock. This is the 27 MHz master clock for the encoder. The I/O direction is set by the CDIR pin.
V_{DDD7}	49	37	digital supply voltage 7 (5 V)
CDIR	50	38	Clock direction. If CDIR input is HIGH, the circuit receives a clock and optional CREF signal, otherwise if CDIR is LOW, CREF and LLC are generated by the internal crystal oscillator.
V_{SSD7}	51	67	digital ground 7
V_{SSA1}	52	41	Analog ground 1 for the DACs.
TESTC	53	42	Analog test pin. Leave open-circuit for normal operation.
V_{DDA1}	54	43	Analog supply voltage 1 for the RGB DACs (3.3 V).
BLUE	55	44	Analog output of the BLUE component.
BI	56	45	Analog input that can be switched to BLUE when SELI = HIGH.
V_{DDA2}	57	46	Analog supply voltage 2 for RGB DACs (3.3 V).
GREEN	58	47	Analog output of GREEN component.
GI	59	48	Analog input that can be switched to GREEN when SELI = HIGH.
V_{DDA3}	60	49	Analog supply voltage 3 for RGB DACs (3.3 V).
RED	61	50	Analog output of RED component.
RI	62	51	Analog input that can be switched to RED when SELI = HIGH.
V_{DDA4}	63	52	Analog supply voltage 4 for DACs (3.3 V).
V_{DDA5}	64	53	Analog supply voltage 5 for DACs (3.3 V).
SELI	65	54	Select analog input. Digital-to-analog converted RGB output when SELI = LOW; RI, GI and BI output when SELI = HIGH.
n.c.	66	–	not connected
V_{SSA2}	67	55	Analog ground 2 for the DACs.
V_{DDA6}	68	56	Analog supply voltage 6 for DACs (3.3 V).
CHROMA	69	57	Analog output of the chrominance signal.
V_{DDA7}	70	58	Analog supply voltage 7 for the Y/C/CVBS DACs (3.3 V).

SYMBOL	PIN		DESCRIPTION
	PLCC84	QFP80	
Y	71	59	Analog output of VBS signal.
V_{DDA8}	72	60	Analog supply voltage 8 for the Y/C/CVBS DACs.
CVBS	73	61	Analog output of the CVBS signal.
V_{DDA9}	74	62	Analog supply voltage 9 for the Y/C/CVBS DACs.
TESTB	75	63	Analog test pin. Leave open-circuit for normal operation.
V_{SSA3}	76	64	Analog ground 3 for the DACs.
AP	77	65	Test pin. Connected to digital ground for normal operation.
SP	78	66	Test pin. Connected to digital ground for normal operation.
V_{SSD8}	79	69	digital ground 8
V_{DDD8}	80	76	digital supply voltage 8 (3.3 V)
V_{SSD9}	81	74	digital ground 9
V_{DDD9}	82	70	digital supply voltage 9 (5 V)
SCL	83	71	I^2C-bus serial clock input.
SDA	84	72	I^2C-bus serial data input/output.

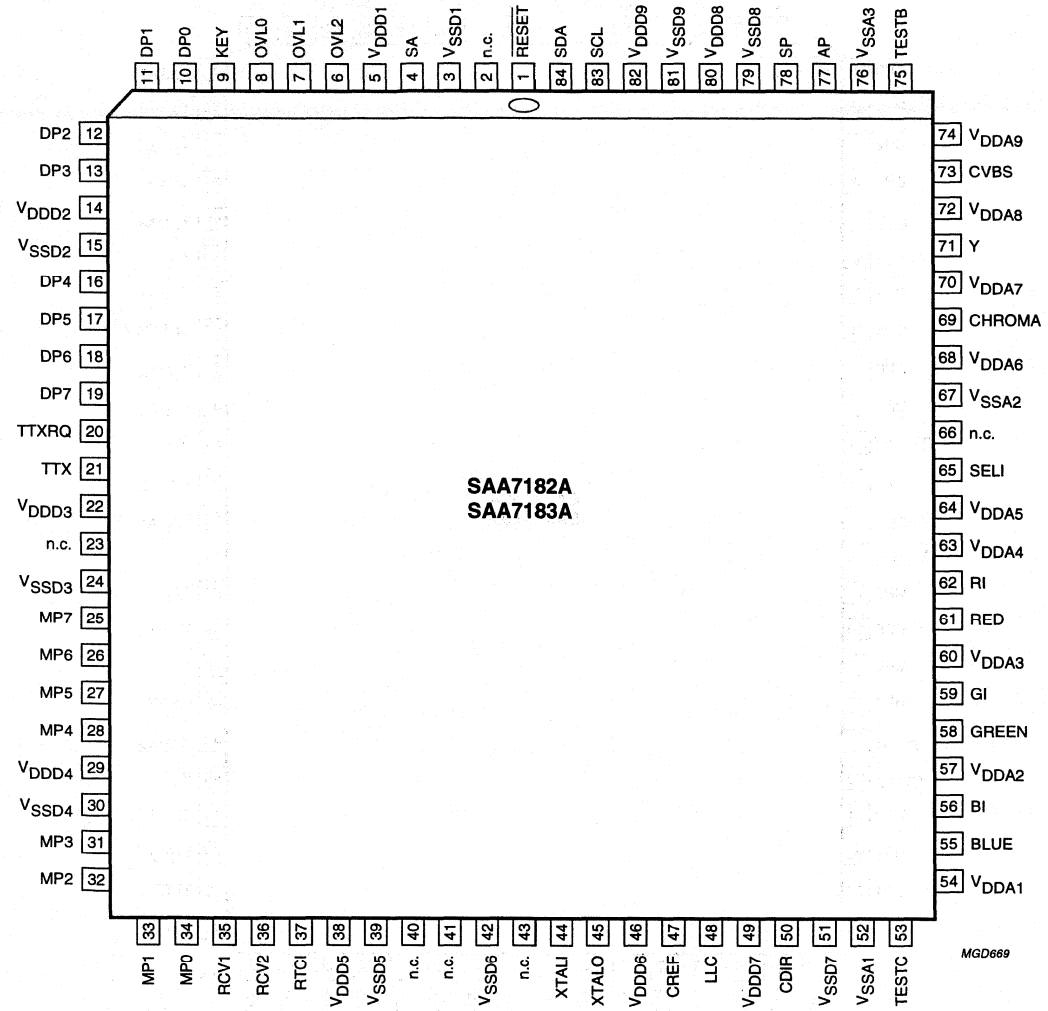


Fig.3 Pin configuration; PLCC84.

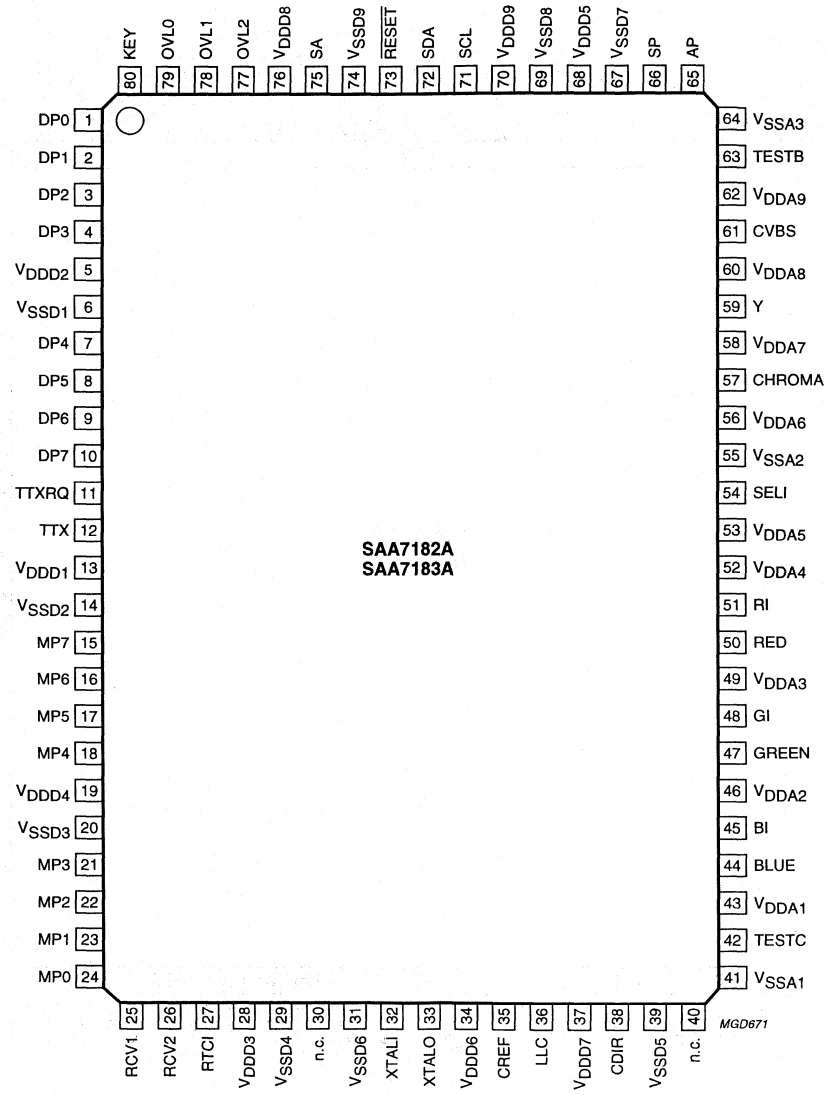


Fig.4 Pin configuration; QFP80.

FUNCTIONAL DESCRIPTION

The digital video encoder (EURO-DENC2) encodes digital luminance and colour difference signals into analog CVBS and simultaneously S-Video signals. NTSC-M, PAL B/G, SECAM standards and sub-standards are supported.

Both interlaced and non-interlaced operation is possible for all standards.

In addition, the de-matrixed Y, Cb, and Cr input is available on three separate analog outputs as RED, GREEN and BLUE. Under software control the dematrix can be by-passed to output digital-to-analog converted Cr, Y, and Cb signals on RGB outputs. Separate digital gain adjustment for luminance and colour difference signals is available.

Analog on-chip multiplexing between internal digital-to-analog converted RGB and external RI, GI and BI signals is also supported.

The basic encoder function consists of subcarrier generation, colour modulation and insertion of synchronization signals. Luminance and chrominance signals are filtered in accordance with the standard requirements of "*RS-170-A*" and "*CCIR 624*".

For ease of analog post filtering the signals are twice oversampled with respect to the pixel clock before digital-to-analog conversion.

For total filter transfer characteristics see Figs 5, 6, 7, 8, 9 and 10. The DACs for Y, C, and CVBS are realized with full 10-bit resolution, DACs for RGB are with 9-bit resolution.

The MPEG port (MP) accept 8 line multiplexed Cb, Y, Cr data.

The 8-bit multiplexed Cb-Y-Cr formats are "*CCIR 656*" (D1 format) compatible, but the SAV and EAV codes can be decoded optionally, when the device is to operate in slave mode.

Alternatively, 8-bits Y on MP port and 8-bit multiplexed Cb, Cr on DP port can be chosen as input.

A crystal-stable master clock (LLC) of 27 MHz, which is twice the CCIR line-locked pixel clock of 13.5 MHz, needs to be supplied externally. Optionally, a crystal oscillator input/output pair of pins and an on-chip clock driver is provided.

It is also possible to connect a Philips Digital Video Decoder (SAA7111 or SAA7151B) in conjunction with a CREF clock qualifier to EURO-DENC2. Via the RTCI pin, connected to RTCO of a decoder, information concerning actual subcarrier, PAL-ID, and if connected to SAA7111, definite subcarrier phase can be inserted.

The EURO-DENC2 synthesizes all necessary internal signals, colour subcarrier frequency, and synchronization signals, from that clock.

European teletext encoding is supported if an appropriate teletext bitstream is applied to the TTX pin.

Wide screen signalling data can be loaded via the I^2C-bus, and is inserted into line 23 for standards using 50 Hz field rate.

The IC also contains Closed Caption and Extended Data Services Encoding (Line 21), and supports anti-taping signal generation in accordance with Macrovision; it also supports overlay via KEY and three control bits by a 24 × 8 LUT.

A number of possibilities are provided for setting different video parameters such as:

Black and blanking level control

Colour subcarrier frequency

Variable burst amplitude etc.

During reset ($\overline{\text{RESET}}$ = LOW) and after reset is released, all digital I/O stages are set to input mode. A reset forces the I^2C-bus interface to abort any running bus transfer and sets register 3A to 03H, register 61 to 06H and registers 6BH and 6EH to 00H. All other control registers are not influenced by a reset.

Data manager

In the data manager, real time arbitration on the data stream to be encoded is performed.

Depending on the polarity of pin KEY, the MP input (or MP/DP input) or OVL input are selected to be encoded to CVBS and Y/C signals, and output as RGB.

KEY controls OVL entries of a programmable LUT for encoded signals and for RGB output. The common KEY switching signal can be disabled by software for the signals to be encoded (Y, C and CVBS), such that OVL will appear on RGB outputs, but not on Y, C and CVBS.

OVL input under control of KEY can be also used to insert decoded teletext information or other on-screen data.

Optionally, the OVL colour LUTs located in this block, can be read out in a pre-defined sequence (8 steps per active video line), achieving, for example, a colour bar test pattern generator without need for an external data source. The colour bar function is only under software control.

Encoder

VIDEO PATH

The encoder generates out of Y, U and V baseband signals luminance and colour subcarrier output signals, suitable for use as CVBS or separate Y and C signals.

Luminance is modified in gain and in offset (latter programmable in a certain range to enable different black level set-ups). After having been inserted a fixed synchronization level, in accordance with standard composite synchronization schemes, and blanking level, programmable also in a certain range to allow for manipulations with Macrovision anti-taping, additional insertion of AGC super-white pulses, programmable in height, is supported.

In order to enable easy analog post filtering, luminance is interpolated from 13.5 MHz data rate to 27 MHz data rate, providing luminance in 10-bit resolution. This filter is also used to define smoothed transients for synchronization pulses and blanking period. For transfer characteristic of the luminance interpolation filter see Figs 7 and 8.

Chrominance is modified in gain (programmable separately for U and V), standard dependent burst is inserted, before baseband colour signals are interpolated from 6.75 MHz data rate to 27 MHz data rate. One of the interpolation stages can be bypassed, thus providing a higher colour bandwidth, which can be made use of for Y and C output. For transfer characteristics of the chrominance interpolation filter see Figs 5 and 6.

The amplitude of inserted burst is programmable in a certain range, suitable for standard signals and for special effects. Behind the succeeding quadrature modulator, colour in 10-bit resolution is provided on subcarrier.

The numeric ratio between Y and C outputs is in accordance with set standards.

TELETEXT INSERTION AND ENCODING

Pin TTX receives a teletext bitstream sampled at the LLC clock, each teletext bit is carried by four or three LLC samples.

Phase variant interpolation is achieved on this bitstream in the internal teletext encoder, providing sufficient small phase jitter on the output text lines.

TTXRQ provides a fully programmable request signal to the teletext source, indicating the insertion period of bitstream at lines selectable independently for both fields. The internal insertion window for text is set to 360 teletext bits including clock run-in bits. For protocol and timing see Fig.19.

CLOSED CAPTION ENCODER

Using this circuit, data in accordance with the specification of Closed Caption or Extended Data Service, delivered by the control interface, can be encoded (Line 21). Two dedicated pairs of bytes (two bytes per field), each pair preceded by run-in clocks and framing code, are possible.

The actual line number where data is to be encoded in, can be modified in a certain range.

Data clock frequency is in accordance with definition for NTSC-M standard 32 times horizontal line frequency.

Data LOW at the output of the DACs corresponds to 0 IRE, data HIGH at the output of the DACs corresponds to approximately 50 IRE.

It is also possible to encode Closed Caption Data for 50 Hz field frequencies at 32 times horizontal line frequency.

ANTI-TAPING (SAA7183A ONLY)

For more information contact your nearest Philips Semiconductors sales office.

RGB processor

This block contains a dematrix in order to produce RED, GREEN and BLUE signals to be fed to a SCART plug.

Before Y, Cb and Cr signals are de-matrixed, individual gain adjustment for Y and colour difference signals and 2 times oversampling for luminance and 4 times oversampling for colour difference signals is performed. For transfer curves of luminance and colour difference components of RGB see Figs 9 and 10.

SECAM processor

SECAM specific pre-processing is achieved in this block by a pre-emphasis of colour difference signals (for gain and phase see Figs 11 and 12).

A baseband frequency modulator with a reference frequency shifted from 4.286 MHz to DC carries out SECAM modulation in accordance with appropriate standard or optionally wide clipping limits.

After the HF pre-emphasis, also applied on a DC reference carrier (anti-Cloche filter; see Figs 13 and 14), line-by-line sequential carriers with black reference of 4.25 MHz (Db) and 4.40625 MHz (Dr) are generated using specified values for FSC programming bytes.

Alternating phase reset in accordance with SECAM standard is carried out automatically. During vertical blanking the so-called bottle pulses are not provided.

Output interface/DACs

In the output interface encoded both Y and C signals are converted from digital-to-analog in 10-bit resolution. Y and C signals are also combined to a 10-bit CVBS signal.

The CVBS output occurs with the same processing delay as the Y and C outputs. Absolute amplitudes at the input of the DAC for CVBS is reduced by $^{15}/_{16}$ with respect to Y and C DACs to make maximum use of conversion ranges.

RED, GREEN and BLUE signals are also converted from digital-to-analog, each providing a 9-bit resolution. It is also possible to feed through three external analog RGB signals at pins RI, BI and GI when pin SELI = HIGH

Outputs of the DACs can be set together in two groups via software control to minimum output voltage for either purpose.

Synchronization

Synchronization of the EURO-DENC2 is able to operate in two modes; slave mode and master mode.

In the slave mode, the circuit accepts synchronization pulses at the bidirectional RCV1 port. The timing and trigger behaviour related to RCV1 can be influenced by programming the polarity and on-chip delay of RCV1. Active slope of RCV1 defines the vertical phase and optionally the odd/even and colour frame phase to be initialized, it can be also used to set the horizontal phase.

If the horizontal phase is not to be influenced by RCV1, a horizontal pulse needs to be supplied at the RCV2 pin. Timing and trigger behaviour can also be influenced for RCV2.

If there are missing pulses at RCV1 and/or RCV2, the time base of EURO-DENC2 runs free, thus an arbitrary number of synchronization slopes may miss, but no additional pulses (with the incorrect phase) must occur.

If the vertical and horizontal phase is derived from RCV1, RCV2 can be used for horizontal or composite blanking input or output.

Alternatively, the device can be triggered by auxiliary codes in a *CCIR 656* data stream at the MP port

In the master mode, the time base of the circuit continuously runs free. On the RCV1 port, the IC can output:

- A Vertical Sync signal (VS) with 3 or 2.5 lines duration, or;
- An ODD/EVEN signal which is LOW in odd fields, or;
- A field sequence signal (FSEQ) which is HIGH in the first of 4, 8, 12 fields respectively.

On the RCV2 port, the IC can provide a horizontal pulse with programmable start and stop phase; this pulse can be inhibited in the vertical blanking period to build up, for example, a composite blanking signal.

The polarity of both RCV1 and RCV2 is selectable by software control.

The length of a field and the start and end of its active part can be programmed. The active part of a field always starts at the beginning of a line.

I²C-bus interface

The I²C-bus interface is a standard slave transceiver, supporting 7-bit slave addresses and 400 kbits/s guaranteed transfer rate. It uses 8-bit subaddressing with an auto-increment function. All registers are write only, except one readable status byte.

Two I²C-bus slave addresses are selected:

88H: LOW at pin SA

8CH: HIGH at pin SA.

Input levels and formats

EURO-DENC2 expects digital Y, Cb, Cr data with levels (digital codes) in accordance with *"CCIR 601"*.

For C and CVBS outputs, deviating amplitudes of the colour difference signals can be compensated by independent gain control setting, while gain for luminance is set to predefined values, distinguishable for 7.5 IRE set-up or without set-up.

For RGB outputs variable amplification of the Y, Cb and Cr components is provided, enabling adjustment of contrast and colour saturation in certain range.

Reference levels are measured with a colour bar, 100% white, 100% amplitude and 100% saturation.

Table 1 *"CCIR 601"* signal component levels

COLOUR	SIGNALS[1]					
	Y	Cb	Cr	R[2]	G[2]	B[2]
White	235	128	128	235	235	235
Yellow	210	16	146	235	235	16
Cyan	170	166	16	16	235	235
Green	145	54	34	16	235	16
Magenta	106	202	222	235	16	235
Red	81	90	240	235	16	16
Blue	41	240	110	16	16	235
Black	16	128	128	16	16	16

Notes

1. Transformation:
   a) $R = Y + 1.3707 \times (Cr - 128)$
   b) $G = Y - 0.3365 \times (Cb - 128) - 0.6982 \times (Cr - 128)$
   c) $B = Y + 1.7324 \times (Cb - 128)$.
2. Representation of R, G and B (or Cr, Y and Cb) at the output is 9 bits at 27 MHz.

Table 2 8-bit multiplexed format (similar to *"CCIR 601"*)

TIME	BITS							
	0	1	2	2	4	5	6	7
Sample	Cb_0	Y_0	Cr_0	Y_1	Cb_2	Y_2	Cr_2	Y_3
Luminance pixel number	0		1		2		3	
Colour pixel number	0				2			

Table 3 16-bit multiplexed format (DTV2 format)

TIME	BITS							
	0	1	2	3	4	5	6	7
Sample Y line	Y_0		Y_1		Y_2		Y_3	
Sample UV line	Cb_0		Cr_0		Cb_2		Cr_2	
Luminance pixel number	0		1		2		3	
Colour pixel number	0				2			

Bit allocation map

Table 4 Slave receiver (slave address 88H or 8CH)

REGISTER FUNCTION	SUB ADDRESS	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
Null	00	0	0	0	0	0	0	0	0
				↓					
Null	25	0	0	0	0	0	0	0	0
Wide screen signal	26	WSS7	WSS6	WSS5	WSS4	WSS3	WSS2	WSS1	WSS0
Wide screen signal	27	WSSON	0	WSS13	WSS12	WSS11	WSS10	WSS9	WSS8
Null	28	0	0	0	0	0	0	0	0
				↓					
Null	37	0	0	0	0	0	0	0	0
Gain Y for RGB	38	0	0	0	GY4	GY3	GY2	GY1	GY0
Gain CD for RGB	39	0	0	0	GCD4	GCD3	GCD2	GCD1	GCD0
Input port control	3A	CBENB	DISKEY	PCREF	SYMP	DEMOFF	FMT16	Y2C	UV2C
OVL LUT Y0	42	OVLY07	OVLY06	OVLY05	OVLY04	OVLY03	OVLY02	OVLY01	OVLY00
OVL LUT U0	43	OVLU07	OVLU06	OVLU05	OVLU04	OVLU03	OVLU02	OVLU01	OVLU00
OVL LUT V0	44	OVLV07	OVLV06	OVLV05	OVLV04	OVLV03	OVLV02	OVLV01	OVLV00
				↓					
OVL LUT Y7	57	OVLY77	OVLY76	OVLY75	OVLY74	OVLY73	OVLY72	OVLY71	OVLY70
OVL LUT U7	58	OVLU77	OVLU76	OVLU75	OVLU74	OVLU73	OVLU72	OVLU71	OVLU70
OVL_LUT_V7	59	OVLV77	OVLV76	OVLV75	OVLV74	OVLV73	OVLV72	OVLV71	OVLV70
Chrominance phase	5A	CHPS7	CHPS6	CHPS5	CHPS4	CHPS3	CHPS2	CHPS1	CHPS0
Gain U	5B	GAINU7	GAINU6	GAINU5	GAINU4	GAINU3	GAINU2	GAINU1	GAINU0
Gain V	5C	GAINV7	GAINV6	GAINV5	GAINV4	GAINV3	GAINV2	GAINV1	GAINV0
Gain U MSB, black level	5D	GAINU8	0	BLCKL5	BLCKL4	BLCKL3	BLCKL2	BLCKL1	BLCKL0
Gain V MSB, blanking level, decoder type	5E	GAINV8	DECTYP	BLNNL5	BLNNL4	BLNNL3	BLNNL2	BLNNL1	BLNNL0
CCR, blanking level VBI	5F	CCRS1	CCRS0	BLNVB5	BLNVB4	BLNVB3	BLNVB2	BLNVB1	BLNVB0
Null	60	0	0	0	0	0	0	0	0
Standard control	61	DOWNB	DOWNA	INPI	YGS	SECAM	SCBW	PAL	FISE
Burst amplitude	62	RTCE	BSTA6	BSTA5	BSTA4	BSTA3	BSTA2	BSTA1	BSTA0
Subcarrier 0	63	FSC07	FSC06	FSC05	FSC04	FSC03	FSC02	FSC01	FSC00

REGISTER FUNCTION	SUB ADDRESS	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
Subcarrier 1	64	FSC15	FSC14	FSC13	FSC12	FSC11	FSC10	FSC09	FSC08
Subcarrier 2	65	FSC23	FSC22	FSC21	FSC20	FSC19	FSC18	FSC17	FSC16
Subcarrier 3	66	FSC31	FSC30	FSC29	FSC28	FSC27	FSC26	FSC25	FSC24
Line 21 odd 0	67	L21O07	L21O06	L21O05	L21O04	L21O03	L21O02	L21O01	L21O00
Line 21 odd 1	68	L21O17	L21O16	L21O15	L21O14	L21O13	L21O12	L21O11	L21O10
Line 21 even 0	69	L21E07	L21E06	L21E05	L21E04	L21E03	L21E02	L21E01	L21E00
Line 21 even 1	6A	L21E17	L21E16	L21E15	L21E14	L21E13	L21E12	L21E11	L21E10
RCV port control	6B	SRCV11	SRCV10	TRCV2	ORCV1	PRCV1	CBLF	ORCV2	PRCV2
Trigger control	6C	HTRIG7	HTRIG6	HTRIG5	HTRIG4	HTRIG3	HTRIG2	HTRIG1	HTRIG0
Trigger control	6D	HTRIG10	HTRIG9	HTRIG8	VTRIG4	VTRIG3	VTRIG2	VTRIG1	VTRIG0
Multi control	6E	SBLBN	0	PHRES1	PHRES0	0	0	FLC1	FLCO
Closed caption/teletext control	6F	CCEN1	CCEN0	TTXEN	CCLN4	CCLN3	CCLN2	CCLN1	CCLN0
RCV2 output start	70	RCV2S7	RCV2S6	RCV2S5	RCV2S4	RCV2S3	RCV2S2	RCV2S1	RCV2S0
RCV2 output end	71	RCV2E7	RCV2E6	RCV2E5	RCV2E4	RCV2E3	RCV2E2	RCV2E1	RCV2E0
MSBs RCV2 output	72	0	RCV2E10	RCV2E9	RCV2E8	0	RCV2S10	RCV2S9	RCV2S8
TTX request H start	73	TTXHS7	TTXHS6	TTXHS5	TTXHS4	TTXHS3	TTXHS2	TTXHS1	TTXHS0
TTX request H end	74	TTXHE7	TTXHE6	TTXHE5	TTXHE4	TTXHE3	TTXHE2	TTXHE1	TTXHE0
MSBs TTX request H	75	0	TTXHE10	TTXHE9	TTXHE8	0	TTXHS10	TTXHS9	TTXHS8
TTX odd request V S	76	TTXOVS7	TTXOVS6	TTXOVS5	TTXOVS4	TTXOVS3	TTXOVS2	TTXOVS1	TTXOVS0
TTX odd request V E	77	TTXOVE7	TTXOVE6	TTXOVE5	TTXOVE4	TTXOVE3	TTXOVE2	TTXOVE1	TTXOVE0
TTX even request V S	78	TTXEVS7	TTXEVS6	TTXEVS5	TTXEVS4	TTXEVS3	TTXEVS2	TTXEVS1	TTXEVS0
TTX even request V E	79	TTXEVE7	TTXEVE6	TTXEVE5	TTXEVE4	TTXEVE3	TTXEVE2	TTXEVE1	TTXEVE0
First active line	7A	FAL7	FAL6	FAL5	FAL4	FAL3	FAL2	FAL1	FAL0
Last active line	7B	LAL7	LAL6	LAL5	LAL4	LAL3	LAL2	LAL1	LAL0
MSB vertical	7C	0	LAL8	0	FAL8	TTXEVE8	TTXOVE8	TTXEVS8	TTXOVS8
Null	7D	0	0	0	0	0	0	0	0
Disable TTX line	7E	LINE15	LINE14	LINE13	LINE12	LINE11	LINE10	LINE9	LINE8
Disable TTX line	7F	LINE23	LINE22	LINE21	LINE20	LINE19	LINE18	LINE17	LINE16

I²C-bus format

Table 5 I²C-bus address; see Table 6

S	SLAVE ADDRESS	ACK	SUBADDRESS	ACK	DATA 0	ACK	--------	DATA n	ACK	P

Table 6 Explanation of Table 5

PART	DESCRIPTION
S	START condition
Slave address	1 0 0 0 1 0 0 X or 1 0 0 0 1 1 0 X (note 1)
ACK	acknowledge, generated by the slave
Subaddress (note 2)	subaddress byte
DATA	data byte
--------	continued data bytes and ACKs
P	STOP condition

Notes

1. X is the read/write control bit; X = logic 0 is order to write; X = logic 1 is order to read, no subaddressing with read.
2. If more than 1 byte DATA is transmitted, then auto-increment of the subaddress is performed.

Slave Receiver

Table 7 Subaddress 26 and 27

DATA BYTE	LOGIC LEVEL	DESCRIPTION
WSS0 to WSS13	–	Wide Screen Signalling bits 3 to 0 = aspect ratio 7 to 4 = enhanced services 10 to 8 = subtitles 13 to 11 = reserved
WSSON	0	wide screen signalling output is disabled
	1	wide screen signalling output is enabled

Table 8 Subaddress 38 and 39

DATA BYTE	DESCRIPTION
GY0 to GY4	Gain luminance of RGB (Cr, Y and Cb) output, ranging from $(1 - {}^{16}/_{32})$ to $(1 + {}^{15}/_{32})$. Suggested nominal value = –6 (11010b), depending on external application.
GCD0 to GCD4	Gain Colour Difference of RGB (Cr, Y and Cb) output, ranging from $(1 - {}^{16}/_{32})$ to $(1 + {}^{15}/_{32})$. Suggested nominal value = –6 (11010b), depending on external application.

Table 9 Subaddress 3A

DATA BYTE	LOGIC LEVEL	DESCRIPTION
UV2C	0	Cb, Cr data are two's complement.
	1	Cb, Cr data are straight binary. Default after reset.
Y2C	0	Y data is two's complement.
	1	Y data is straight binary. Default after reset.
FMT16	0	Selects Cb, Y, Cr and Y on 8 lines on MP port (*"CCIR 656"* compatible). Default after reset.
	1	Selects Cb and Cr on DP port and Y on MP port.
DEMOFF	0	Y, Cb and Cr for RGB dematrix is active. Default after reset.
	1	Y, Cb and Cr for RGB dematrix is bypassed.
SYMP	0	Horizontal and vertical trigger is taken from RCV2 and RCV1 respectively. Default after reset.
	1	Horizontal and vertical trigger is decoded out of *"CCIR 656"* compatible data at MP port.
PCREF	0	Normal polarity of CREF for DIG-TV2 compatible input signals.
	1	Inverted polarity of CREF for DIG-TV2 compatible input signals.
DISKEY	0	OVL keying enabled for Y, C and CVBS outputs. Default after reset.
	1	OVL keying disabled for Y, C and CVBS outputs.
CBENB	0	Data from input ports is encoded. Default after reset.
	1	Colour bar with programmable colours (entries of OVL_LUTs) is encoded. The LUTs are read in upward order from index 0 to index 7.

Table 10 Subaddress 42 to 59

COLOUR	DATA BYTE[1]			INDEX[2]
	OVLY	OVLU	OVLV	
White	107 (6BH)	0 (00H)	0 (00H)	0
	107 (6BH)	0 (00H)	0 (00H)	
Yellow	82 (52H)	144 (90H)	18 (12H)	1
	34 (22H)	172 (ACH)	14 (0EH)	
Cyan	42 (2AH)	38 (26H)	144 (90H)	2
	03 (03H)	29 (1DH)	172 (ACH)	
Green	17 (11H)	182 (B6H)	162 (A2H)	3
	240 (F0H)	200 (C8H)	185 (B9H)	
Magenta	234 (EAH)	74 (4AH)	94 (5EH)	4
	212 (D4H)	56 (38H)	71 (47H)	
Red	209 (D1H)	218 (DAH)	112 (70H)	5
	193 (C1H)	227 (E3H)	84 (54H)	
Blue	169 (A9H)	112 (70H)	238 (EEH)	6
	163 (A3H)	84 (54H)	242 (F2H)	
Black	144 (90H)	0 (00H)	0 (00H)	7
	144 (90H)	0 (00H)	0 (00H)	

Notes

1. Contents of OVL look-up tables. All 8 entries are 8-bits. Data representation is in accordance with *"CCIR 601"* (Y, Cb and Cr), but two's complement, e.g. for a $^{100}/_{100}$ (upper number) or $^{100}/_{75}$ (lower number) colour bar.
2. For normal colour bar with CBENB = logic 1.

Table 11 Subaddress 5A

DATA BYTE[1]	VALUE	RESULT
CHPS	tbf	PAL-B/G and data from input ports
	tbf	PAL-B/G and data from look-up table
	tbf	NTSC-M and data from input ports
	tbf	NTSC-M and data from look-up table

Note

1. Phase of encoded colour subcarrier (including burst) relative to horizontal sync. Can be adjusted in steps of 360/256 degrees.

Table 12 Subaddress 5B and 5D

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
GAINU	variable gain for Cb signal; input representation accordance with *"CCIR 601"*	white-to-black = 92.5 IRE[1]	
		GAINU = 0	output subcarrier of U contribution = 0
		GAINU = 118 (76H)	output subcarrier of U contribution = nominal
		white-to-black = 100 IRE[2]	
		GAINU = 0	output subcarrier of U contribution = 0
		GAINU = 125 (7DH)	output subcarrier of U contribution = nominal
	nominal GAINU for SECAM encoding	value = 106 (6AH)	

Notes

1. GAINU = –2.17 × nominal to +2.16 × nominal.
2. GAINU = –2.05 × nominal to +2.04 × nominal.

Table 13 Subaddress 5C and 5E

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
GAINV	variable gain for Cr signal; input representation accordance with *"CCIR 601"*	white-to-black = 92.5 IRE[1]	
		GAINV = 0	output subcarrier of V contribution = 0
		GAINV = 165 (A5H)	output subcarrier of V contribution = nominal
		white-to-black = 100 IRE[2]	
		GAINV = 0	output subcarrier of V contribution = 0
		GAINV = 175 (AFH)	output subcarrier of V contribution = nominal
	nominal GAINV for SECAM encoding	value = –129 (17FH)	

Notes

1. GAINV = –1.55 × nominal to +1.55 × nominal.
2. GAINV = –1.46 × nominal to +1.46 × nominal.

Table 14 Subaddress 5D

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
BLCKL	variable black level; input representation accordance with *"CCIR 601"*	white-to-sync = 140 IRE[1]	
		BLCKL = 0	output black level = 24 IRE
		BLCKL = 63 (3FH)	output black level = 49 IRE
		white-to-sync = 143 IRE[2]	
		BLCKL = 0	output black level = 24 IRE
		BLCKL = 63 (3FH)	output black level = 50 IRE

Notes

1. Output black level/IRE = BLCKL × 25/63 + 24; recommended value: BLCKL = 60 (3CH) normal.
2. Output black level/IRE = BLCKL × 26/63 + 24; recommended value: BLCKL = 45 (2DH) normal.

Table 15 Subaddress 5E

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
BLNNL	variable blanking level	white-to-sync = 140 IRE[1]	
		BLNNL = 0	output blanking level = 17 IRE
		BLNNL = 63 (3FH)	output blanking level = 42 IRE
		white-to-sync = 143 IRE[2]	
		BLNNL = 0	output blanking level = 17 IRE
		BLNNL = 63 (3FH)	output blanking level = 43 IRE
DECTYP	RTCI	logic 0	real time control input from SAA7151B
		logic 1	real time control input from SAA7111

Notes

1. Output black level/IRE = BLNNL × 25/63 + 17; recommended value: BLNNL = 58 (3AH) normal.
2. Output black level/IRE = BLNNL × 26/63 + 17; recommended value: BLNNL = 63 (3FH) normal.

Table 16 Subaddress 5F

DATA BYTE	DESCRIPTION
BLNVB	variable blanking level during vertical blanking interval is typically identical to value of BLNNL
CCRS	select cross colour reduction filter in luminance; see Table 17

Table 17 Logic levels and function of CCRS

CCRS1	CCRS0	FUNCTION
0	0	no cross colour reduction; for overall transfer characteristic of luminance see Fig.7
0	1	cross colour reduction #1 active; for overall transfer characteristic see Fig.7
1	0	cross colour reduction #2 active; for overall transfer characteristic see Fig.7
1	1	cross colour reduction #3 active; for overall transfer characteristic see Fig.7

Table 18 Subaddress 61:

DATA BYTE	LOGIC LEVEL	DESCRIPTION
FISE	0	864 total pixel clocks per line; default after reset
	1	858 total pixel clocks per line
PAL	0	NTSC encoding (non-alternating V component)
	1	PAL encoding (alternating V component); default after reset
SCBW	0	enlarged bandwidth for chrominance encoding (for overall transfer characteristic of chrominance in baseband representation see Figs 5 and 6); wide clipping for SECAM
	1	standard bandwidth for chrominance encoding (for overall transfer characteristic of chrominance in baseband representation see Figs 5 and 6); default after reset
SECAM	0	no SECAM encoding; default after reset
	1	SECAM encoding activated
YGS	0	luminance gain for white – black 100 IRE; default after reset
	1	luminance gain for white – black 92.5 IRE including 7.5 IRE set-up of black
INPI	0	PAL switch phase is nominal; default after reset
	1	PAL switch phase is inverted compared to nominal
DOWNA	0	DACs for CVBS, Y and C in normal operational mode; default after reset
	1	DACs for CVBS, Y and C forced to lowest output voltage
DOWNB	0	DACs for R, G and B in normal operational mode; default after reset
	1	DACs for R, G and B forced to lowest output voltage

Table 19 Subaddress 62A

DATA BYTE	LOGIC LEVEL	DESCRIPTION
RTCE	0	no real time control of generated subcarrier frequency
	1	real time control of generated subcarrier frequency through SAA7151B or SAA7111 (timing see Fig.18)

Table 20 Subaddress 62B

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
BSTA	amplitude of colour burst; input representation in accordance with *"CCIR 601"*	white-to-black = 92.5 IRE; burst = 40 IRE; NTSC encoding BSTA = 0 to 1.25 × nominal(1) white-to-black = 92.5 IRE; burst = 40 IRE; PAL encoding BSTA = 0 to 1.76 × nominal(2) white-to-black = 100 IRE; burst = 43 IRE; NTSC encoding BSTA = 0 to 1.20 × nominal(3) white-to-black = 100 IRE; burst = 43 IRE; PAL encoding BSTA = 0 to 1.67 × nominal(4)	
	fixed burst amplitude with SECAM encoding		

Notes

1. Recommended value: BSTA = 102 (66H).
2. Recommended value: BSTA = 72 (48H).
3. Recommended value: BSTA = 106 (6AH).
4. Recommended value: BSTA = 75 (4BH).

Table 21 Subaddress 63 to 66 (four bytes to program subcarrier frequency)

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
FSC0 to FSC3	f_{fsc} = subcarrier frequency (in multiples of line frequency); f_{llc} = clock frequency (in multiples of line frequency)	$FSC = \text{round}\left(\frac{f_{fsc}}{f_{llc}} \times 2^{32}\right)$ see note 1	FSC3 = most significant byte FSC0 = least significant byte

Note

1. Examples:
   a) NTSC-M: f_{fsc} = 227.5, f_{llc} = 1716 → FSC = 569408543 (21F07C1FH).
   b) PAL-B/G: f_{fsc} = 283.7516, f_{llc} = 1728 → FSC = 705268427 (2A098ACBH).
   c) SECAM: f_{fsc} = 274.304, f_{llc} = 1728 → FSC = 681786290 (28A33BB2H).

Table 22 Subaddress 67 to 6A

DATA BYTE[1]	DESCRIPTION
L21O0	first byte of captioning data, odd field
L21O1	second byte of captioning data, odd field
L21E0	first byte of extended data, even field
L21E1	second byte of extended data, even field

Note

1. LSBs of the respective bytes are encoded immediately after run-in and framing code, the MSBs of the respective bytes have to carry the parity bit, in accordance with the definition of Line 21 encoding format.

Table 23 Subaddress 6B

DATA BYTE	LOGIC LEVEL	DESCRIPTION
PRCV2	0	polarity of RCV2 as output is active HIGH, rising edge is taken when input, respectively; default after reset
	1	polarity of RCV2 as output is active LOW, falling edge is taken when input, respectively
ORCV2	0	pin RCV2 is switched to input; default after reset
	1	pin RCV2 is switched to output
CBLF	0	if ORCV2 = HIGH, pin RCV2 provides an HREF signal (Horizontal Reference pulse that is defined by RCV2S and RCV2E, also during vertical blanking Interval); default after reset if ORCV2 = LOW and bit SYMP = LOW, signal input to RCV2 is used for horizontal synchronization only (if TRCV2 = 1); default after reset
	1	if ORCV2 = HIGH, pin RCV2 provides a 'Composite-Blanking-Not' signal, this is a reference pulse that is defined by RCV2S and RCV2E, excluding Vertical Blanking Interval, which is defined by FAL and LAL if ORCV2 = LOW and bit SYMP = LOW, signal input to RCV2 is used for horizontal synchronization (if TRCV2 = 1) and as an internal blanking signal
PRCV1	0	polarity of RCV1 as output is active HIGH, rising edge is taken when input; default after reset
	1	polarity of RCV1 as output is active LOW, falling edge is taken when input
ORCV1	0	pin RCV1 is switched to input; default after reset
	1	pin RCV1 is switched to output
TRCV2	0	horizontal synchronization is taken from RCV1 port (at bit SYMP = LOW) or from decoded frame sync of *CCIR 656* input (at bit SYMP = HIGH); default after reset
	1	horizontal synchronization is taken from RCV2 port (at bit SYMP = LOW)
SRCV1	–	defines signal type on pin RCV1; see Table 24

Table 24 Logic levels and function of SRCV1

DATA BYTE		AS OUTPUT	AS INPUT	FUNCTION
SRCV11	SRCV10			
0	0	VS	VS	vertical sync each field; default after reset
0	1	FS	FS	frame sync (odd/even)
1	0	FSEQ	FSEQ	field sequence, vertical sync every fourth field (PAL = 0), eighth field (PAL = 1) or twelfth field (SECAM = 1)
1	1	not applicable	not applicable	–

Table 25 Subaddress 6C and 6D

DATA BYTE	DESCRIPTION
HTRIG	sets the horizontal trigger phase related to signal on RCV1 or RCV2 input values above 1715 (FISE = 1) or 1727 (FISE = 0) are not allowed increasing HTRIG decreases delays of all internally generated timing signals reference mark: analog output horizontal sync (leading slope) coincides with active edge of RCV used for triggering at HTRIG = tbf (tbf)

Table 26 Subaddress 6D

DATA BYTE	LOGIC LEVEL	DESCRIPTION
VTRIG	–	sets the vertical trigger phase related to signal on RCV1 input increasing VTRIG decreases delays of all internally generated timing signals, measured in half lines variation range of VTRIG = 0 to 31 (1FH)

Table 27 Subaddress 6E

DATA BYTE	LOGIC LEVEL	DESCRIPTION
SBLBN	0	vertical blanking is defined by programming of FAL and LAL; default after reset
	1	vertical blanking is forced in accordance with *"CCIR 624"* (50 Hz) or RS170A (60 Hz)
PHRES	–	selects the phase reset mode of the colour subcarrier generator; see Table 28
FLC	–	field length control; see Table 29

Table 28 Logic levels and function of PHRES

DATA BYTE		FUNCTION
PHRES1	PHRES0	
0	0	no reset or reset via RTCI from SAA7111 if bit RTCE = 1; default after reset
0	1	reset every two lines or SECAM-specific if bit SECAM = 1
1	0	reset every eight fields
1	1	reset every four fields

Table 29 Logic levels and function of FLC

DATA BYTE		FUNCTION
FLC1	FLC0	
0	0	interlaced 312.5 lines/field at 50 Hz, 262.5 lines/field at 60 Hz; default after reset
0	1	non-interlaced 312 lines/field at 50 Hz, 262 lines/field at 60 Hz
1	0	non-interlaced 313 lines/field at 50 Hz, 263 lines/field at 60 Hz
1	1	non-interlaced 313 lines/field at 50 Hz, 263 lines/field at 60 Hz

Table 30 Subaddress 6F

DATA BYTE	LOGIC LEVEL	DESCRIPTION
CCEN	–	enables individual Line 21 encoding; see Table 31
TTXEN	0	disables teletext insertion
	1	enables teletext insertion
SCCLN	–	selects the actual line, where closed caption or extended data are encoded line = (SCCLN + 4) for M-systems line = (SCCLN + 1) for other systems

Table 31 Logic levels and function of CCEN

DATA BYTE		FUNCTION
CCEN1	CCEN0	
0	0	Line 21 encoding off
0	1	enables encoding in field 1 (odd)
1	0	enables encoding in field 2 (even)
1	1	enables encoding in both fields

Table 32 Subaddress 70 to 72

DATA BYTE	DESCRIPTION
RCV2S	start of output signal on RCV2 pin values above 1715 (FISE = 1) or 1727 (FISE = 0) are not allowed first active pixel at analog outputs (corresponding input pixel coinciding with RCV2) at RCV2S = tbfH (tbfH)
RCV2E	end of output signal on RCV2 pin values above 1715 (FISE = 1) or 1727 (FISE = 0) are not allowed last active pixel at analog outputs (corresponding input pixel coinciding with RCV2) at RCV2E = tbfH (tbfH)

Table 33 Subaddress 73 to 75

DATA BYTE	DESCRIPTION
TTXHS	start of signal on pin TTXRQ (standard for 50 Hz field rate = tbf) values above 1715 (FISE = 1) or 1727 (FISE = 0) are not allowed
TTXHE	end of signal on pin TTXRQ (standard for 50 Hz field rate = TTXHS + 1402) values above 1715 (FISE = 1) or 1727 (FISE = 0) are not allowed

Table 34 Subaddress 76, 77 and 7C

DATA BYTE	DESCRIPTION
TTXOVS	first line of occurrence of signal on pin TTXRQ in odd field = TTXOVS + 1 (50 Hz field rate)
TTXOVE	last line of occurrence of signal on pin TTXRQ in odd field = TTXOVE (50 Hz field rate)

Table 35 Subaddress 78, 79 and 7C

DATA BYTE	DESCRIPTION
TTXEVS	first line of occurrence of signal on pin TTXRQ in even field = TTXEVS + 1 (50 Hz field rate)
TTXEVE	last line of occurrence of signal on pin TTXRQ in even field = TTXEVE (50 Hz field rate)

Table 36 Subaddress 7A to 7C

DATA BYTE	DESCRIPTION
FAL	first active line = FAL + 4 for M-systems, = FAL + 1 for other systems, measured in lines FAL = 0 coincides with the first field synchronization pulse
LAL	last active line = LAL + 3 for M-systems, = LAL for other system, measured in lines LAL = 0 coincides with the first field synchronization pulse

Table 37 Subaddress 7A to 7C

DATA BYTE	DESCRIPTION
LINE	individual lines in both fields (PAL counting) can be disabled for insertion of teletext by the respective bits, disabled line = LINExx (50 Hz field rate) this bit mask is effective only, if the lines are enabled by TTXOVS/TTXOVE and TTXEVS/TTXEVE

SUBADDRESSES

In subaddresses 5B, 5C, 5D, 5E and 62 all IRE values are rounded up.

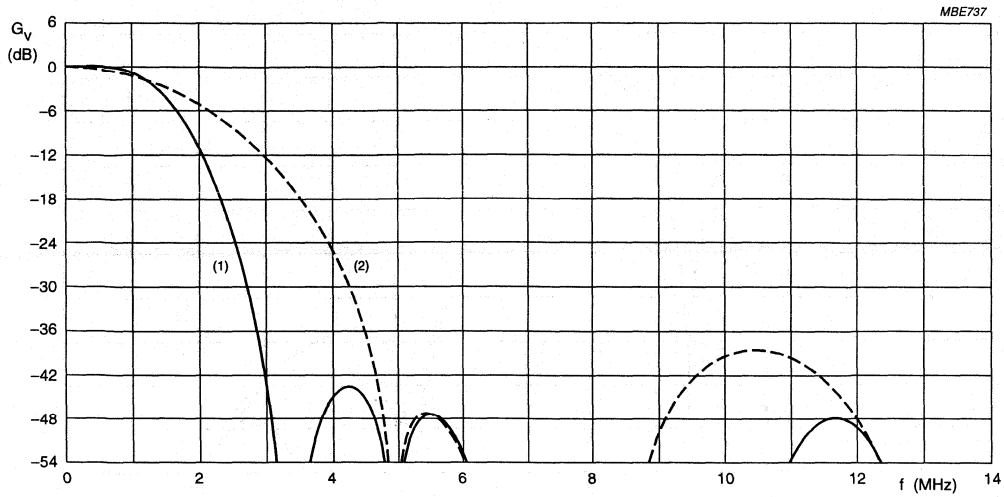
Slave Transmitter

Table 38 Slave transmitter (slave address 89H or 8DH)

REGISTER FUNCTION	SUBADDRESS	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
Status byte	–	VER2	VER1	VER0	CCRDO	CCRDE	0	FSEQ	O_E

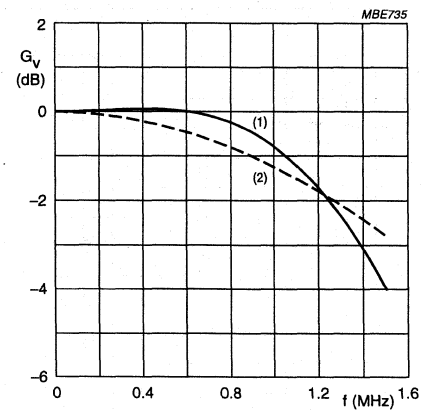
Table 39 No subaddress

DATA BYTE	LOGIC LEVEL	DESCRIPTION
VER	–	Version identification of the device. It will be changed with all versions of the IC that have different programming models. Current Version is 001 binary.
CCRDO	1	Closed caption bytes of the odd field have been encoded.
	0	The bit is reset after information has been written to the subaddresses 67 and 68. It is set immediately after the data has been encoded.
CCRDE	1	Closed caption bytes of the even field have been encoded.
	0	The bit is reset after information has been written to the subaddresses 69 and 6A. It is set immediately after the data has been encoded.
FSEQ	1	During first field of a sequence (repetition rate: NTSC = 4 fields, PAL = 8 fields, SECAM = 12 fields.
	0	Not first field of a sequence.
O_E	1	During even field.
	0	During odd field.



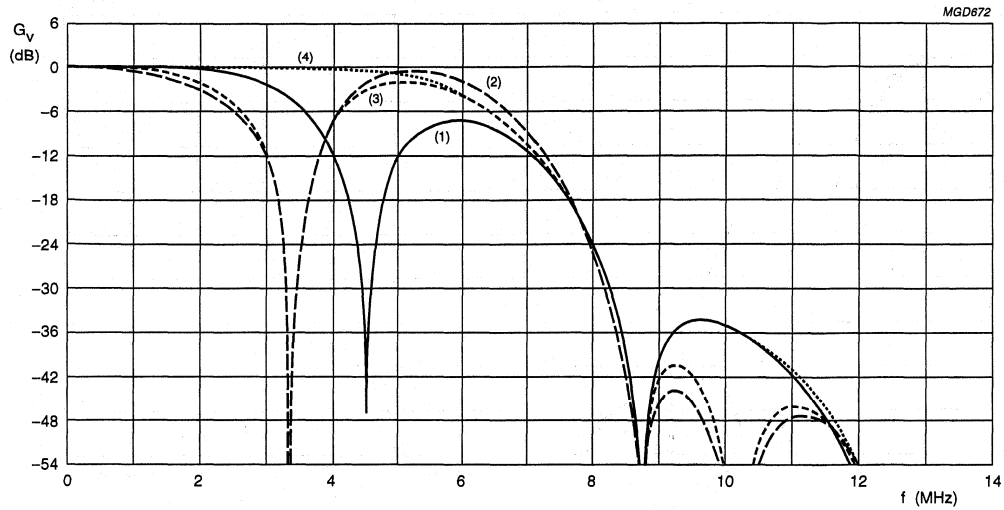
(1) SCBW = 1.
(2) SCBW = 0.

Fig.5 Chrominance transfer characteristic 1.



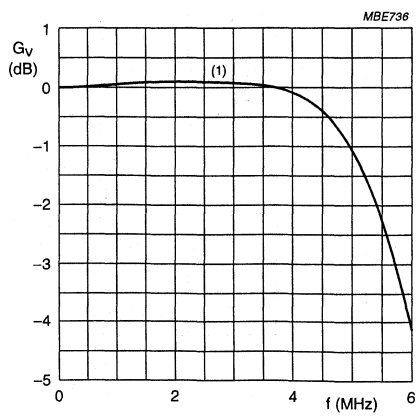
(1) SCBW = 1.
(2) SCBW = 0.

Fig.6 Chrominance transfer characteristic 2.



(1) CCRS1 = 0; CCRS0 = 1.
(2) CCRS1 = 1; CCRS0 = 0.
(3) CCRS1 = 1; CCRS0 = 1.
(4) CCRS1 = 0; CCRS0 = 0.

Fig.7 Luminance transfer characteristic 1.



(1) CCRS1 = 0; CCRS0 = 0.

Fig.8 Luminance transfer characteristic 2.

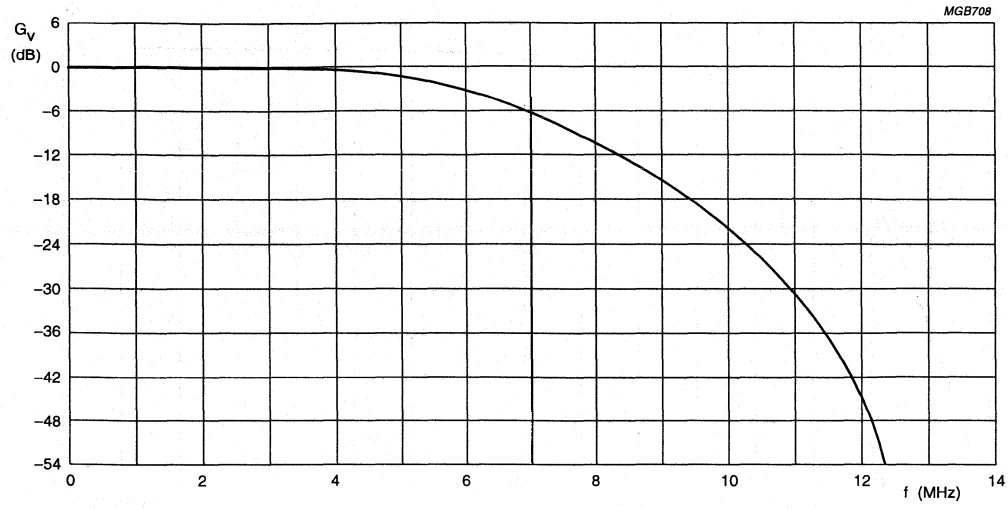


Fig.9 Luminance transfer characteristic in RGB.

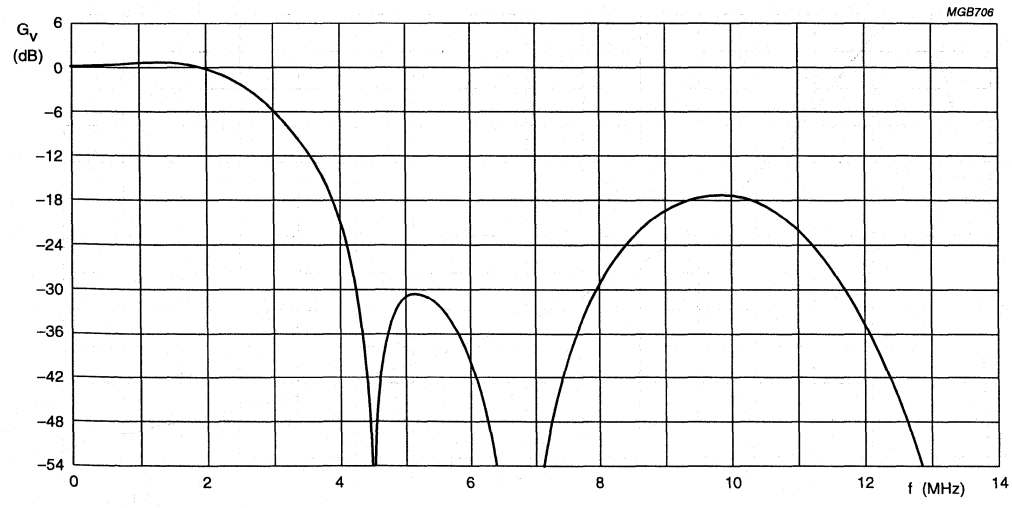


Fig.10 Colour difference transfer characteristic in RGB.

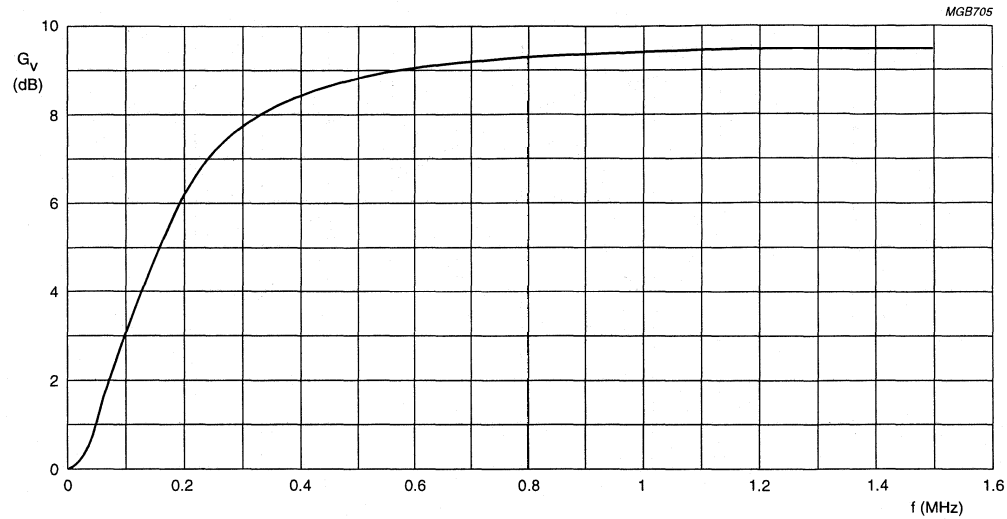


Fig.11 Gain of SECAM pre-emphasis.

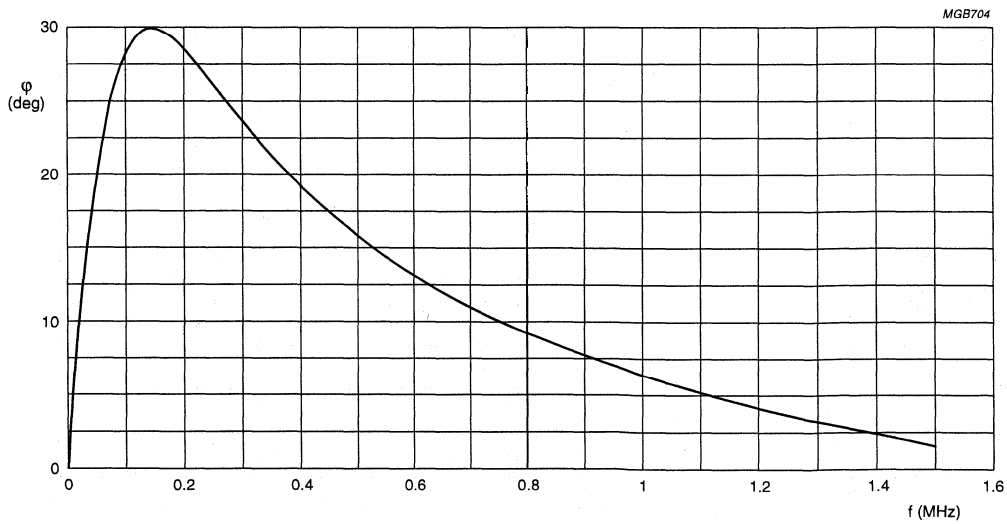


Fig.12 Phase of SECAM pre-emphasis.

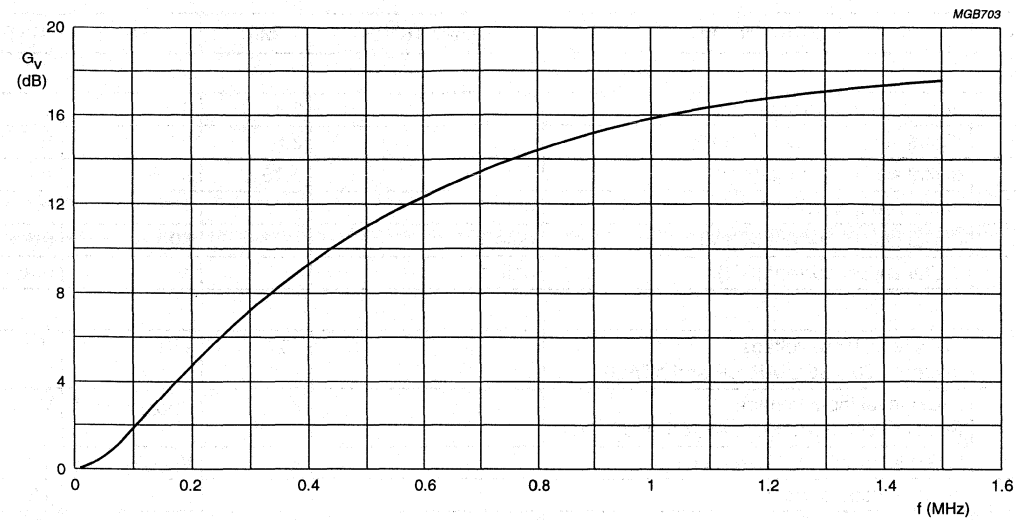


Fig.13 Gain of SECAM anti-Cloche.

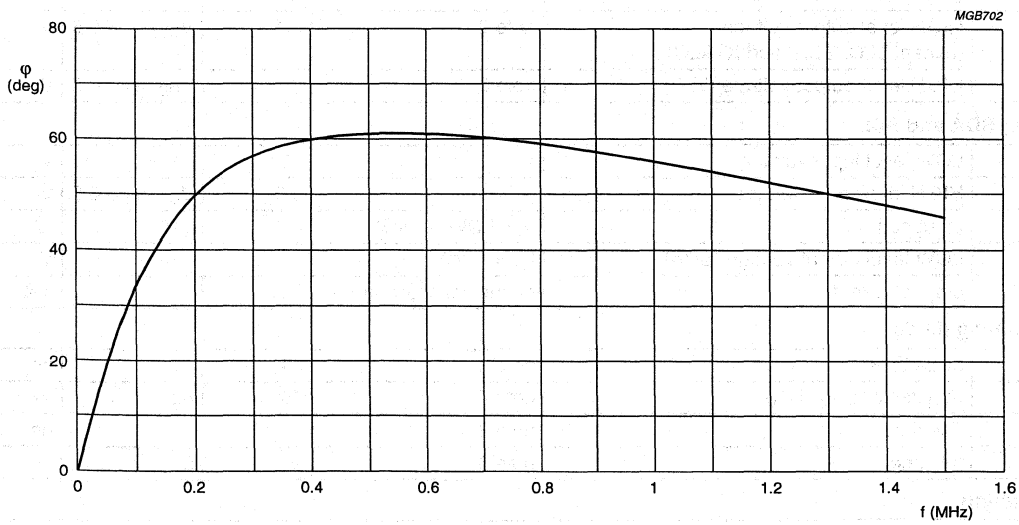


Fig.14 Phase of SECAM anti-Cloche.

CHARACTERISTICS

$V_{DDD(3)}$ = 3.0 to 3.6 V; $V_{DDD(5)}$ = 4.75 to 5.25 V; T_{amb} = 0 to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Supply					
$V_{DDA(3)}$	analog supply voltage (3.3 V)		3.1	3.5	V
$V_{DDD(3)}$	digital supply voltage (3.3 V)		3.0	3.6	V
$V_{DDD(5)}$	digital supply voltage (5 V)		4.75	5.25	V
I_{DDA}	analog supply current	note 1	–	110	mA
$I_{DDD(3)}$	digital supply current (3.3 V)	note 1	–	80	mA
$I_{DDD(5)}$	digital supply current (5 V)	note 1	–	10	mA
Inputs					
V_{IL}	LOW level input voltage (except SDA, SCL, AP, SP and XTALI)		−0.5	+0.8	V
V_{IH}	HIGH level input voltage (except LLC, SDA, SCL, AP, SP and XTALI)		2.0	$V_{DDD(5)}$ + 0.5	V
	HIGH level input voltage (LLC)		2.4	$V_{DDD(5)}$ + 0.5	V
I_{LI}	input leakage current		–	1	µA
C_i	input capacitance	clocks	–	10	pF
		data	–	8	pF
		I/Os at high impedance	–	8	pF
Outputs					
V_{OL}	LOW level output voltage (except SDA and XTALO)	note 2	0	0.6	V
V_{OH}	HIGH level output voltage (except LLC, SDA, and XTALO)	note 2	2.4	$V_{DDD(5)}$ + 0.5	V
	HIGH level output voltage (LLC)	note 2	2.6	$V_{DDD(5)}$ + 0.5	V
I²C-bus; SDA and SCL					
V_{IL}	LOW level input voltage		−0.5	+1.5	V
V_{IH}	HIGH level input voltage		3.0	$V_{DDD(5)}$ + 0.5	V
I_i	input current	V_i = LOW or HIGH	−10	+10	µA
V_{OL}	LOW level output voltage (SDA)	I_{OL} = 3 mA	–	0.4	V
I_o	output current	during acknowledge	3	–	mA
Clock timing (LLC)					
T_{LLC}	cycle time	note 3	34	41	ns
δ	duty factor t_{HIGH}/T_{LLC}	note 4	40	60	%
t_r	rise time	note 3	–	5	ns
t_f	fall time	note 3	–	6	ns
Input timing					
$t_{SU;DAT}$	input data set-up time (any other except CDIR, SCL, SDA, $\overline{\text{RESET}}$, AP and SP)		6	–	ns
$t_{HD;DAT}$	input data hold time (any other except CDIR, SCL, SDA, $\overline{\text{RESET}}$, AP and SP)		3	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Crystal oscillator					
f_n	nominal frequency (usually 27 MHz)	3rd harmonic	–	30	MHz
$\Delta f/f_n$	permissible deviation of nominal frequency	note 5	–50	+50	10^{-6}
CRYSTAL SPECIFICATION					
T_{amb}	operating ambient temperature		0	70	°C
C_L	load capacitance		8	–	pF
R_S	series resistance		–	80	Ω
C_1	motional capacitance (typical)		1.5 –20%	1.5 +20%	fF
C_0	parallel capacitance (typical)		3.5 –20%	3.5 +20%	pF
Data and reference signal output timing					
C_L	output load capacitance		7.5	40	pF
t_h	output hold time		4	–	ns
t_d	output delay time		–	25	ns
CHROMA, Y, CVBS and RGB outputs					
$V_{o(p-p)}$	output signal voltage (peak-to-peak value)	note 6	1.35	1.45	V
R_{int}	internal serial resistance		1	3	Ω
R_L	output load resistance		75	300	Ω
B	output signal bandwidth of DACs	–3 dB	10	–	MHz
ILE	LF integral linearity error of DACs		–	±2	LSB
DLE	LF differential linearity error of DACs		–	±1	LSB

Notes

1. At maximum supply voltage with highly active input signals.
2. The levels have to be measured with load circuits of 1.2 kΩ to 3.0 V (standard TTL load) and C_L = 25 pF.
3. The data is for both input and output direction.
4. With LLC in input mode. In output mode, with a crystal connected to XTALO/XTALI duty factor is typically 50%.
5. If an internal oscillator is used, crystal deviation of nominal frequency is directly proportional to the deviation of subcarrier frequency and line/field frequency.
6. For full digital range, without load, V_{DDA} = 3.3 V. The typical voltage swing is 1.4 V, the typical minimum output voltage (digital zero at DAC) is 0.2 V.

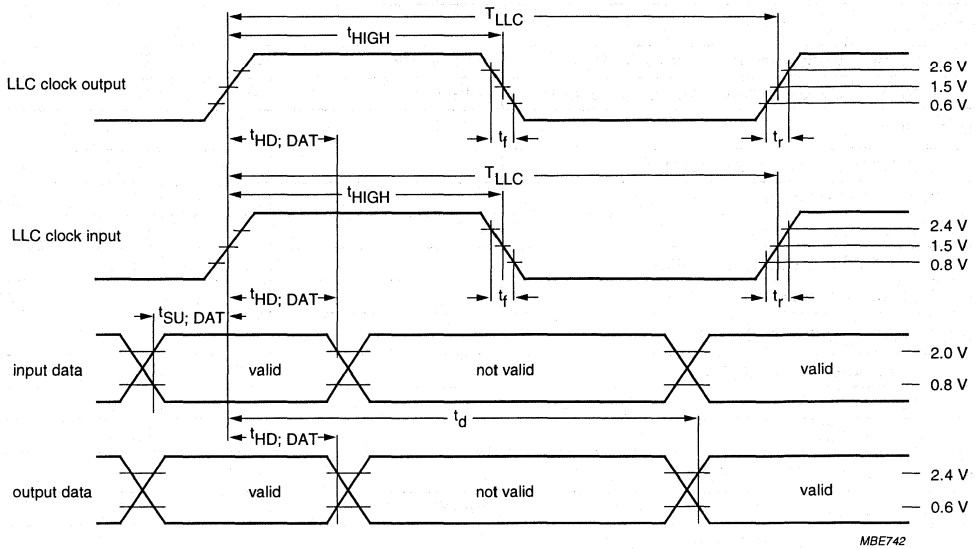
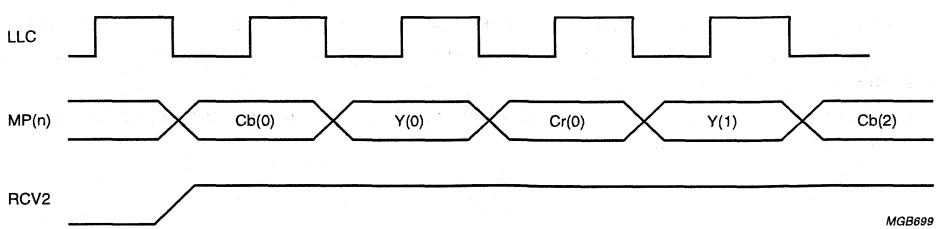
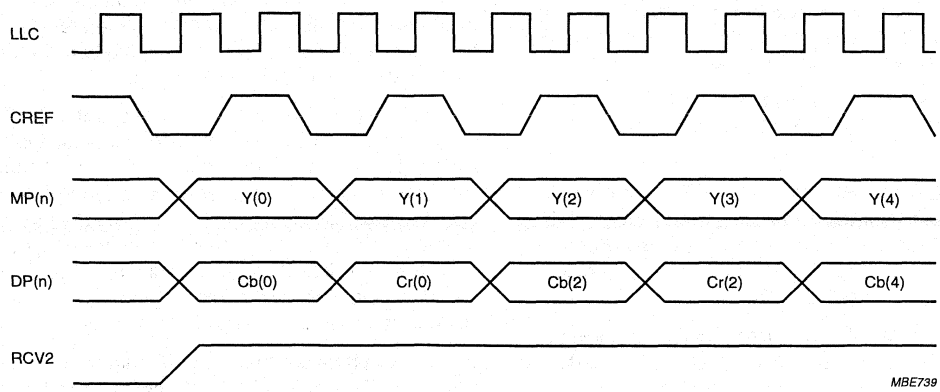


Fig.15 Clock data timing.



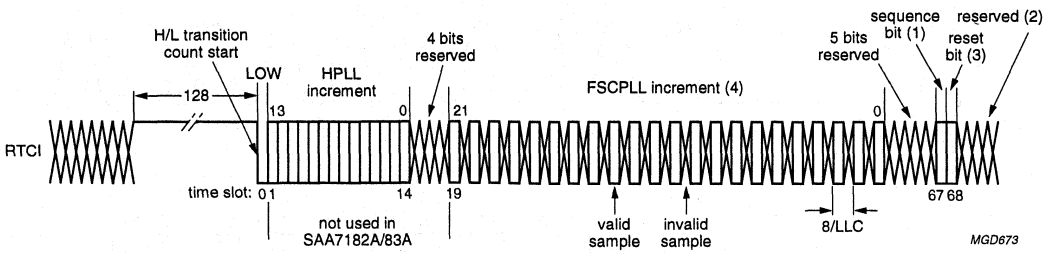
The data demultiplexing phase is coupled to the internal horizontal phase.
The phase of the RCV2 signal is programmed to tbf (tbf for 50 Hz) in this example in output mode (RCV2S).

Fig.16 Functional timing.



The data demultiplexing phase is coupled to the internal horizontal phase.
The CREF signal applies only for the 16 line digital TV format, because these signals are only valid in 13.5 MHz.
The phase of the RCV2 signal is programmed to tbf (tbf for 50 Hz) in this example in output mode (RCV2S).

Fig.17 Digital TV timing.



(1) Sequence bit:
PAL = logic 0 then (R – Y) line normal; PAL = logic 1 then (R – Y) line inverted.
NTSC = logic 0 then no change.
(2) Reserved bits: 235 with 50 Hz systems; 232 with 60 Hz systems.
(3) Only from SAA7111 decoder.
(4) SAAA7111 provides (22 : 0) bits, resulting in 3 reserved bits before sequence bit.

Fig.18 RTCI timing.

Teletext timing

Time t_{FD} is the time needed to interpolate input data TTX and inserting it into the CVBS and Y output signal, such that it appears at t_{TTX} = 10.2 µs after the leading edge of the horizontal synchronization pulse.

Time t_{PD} is the pipeline delay time introduced by the source that is gated by TTXRQ in order to deliver TTX data.

Since the pulse representing the TTXRQ signal is fully programmable in duration and rising/falling edges (TTXHS and TTXHE), the TTX data is always inserted at the correct position of 10.2 µs after the leading edge of outgoing horizontal synchronization pulse.

Time t_{TTXWin} is the internally used insertion window for TTX data; it has a constant length that allows insertion of 360 teletext bits (maximum) at a text data rate of 6.9375 Mbits/s. The insertion window is not opened if the control bit TTXEN is zero.

TELETEXT PROTOCOL

The frequency relationship between TTX bit clock and the system clock LLC for 50 Hz field rate is given by the relationship of line frequency multiples, which means 1728/444.

Thus 37 TTX bits correspond to 144 LLC clocks, each bit has a duration of nearly 4 LLC clocks. The chip-internal sequencer and variable phase interpolation filter minimizes the phase jitter, and thus generates a bandwidth limited signal, which is digital-to-analog converted for the CVBS and Y outputs.

At the TTX input, bit duration scheme repeats after 37 TTX bits or 144 LLC clocks. The protocol demands that TXX bits 10, 19, 28 and 37 are carried by three LLC samples, all others by four LLC samples. After a cycle of 37 TTX bits, the next bits with three LLC samples are bits 47, 56, 65 and 74; this scheme holds for all succeeding cycles of 37 TTX bits, until 360 TTX bits (including 16 run-in bits) are completed. For every additional line with TTX data, the bit duration scheme starts in the same way.

Using appropriate programming, all suitable lines of the odd field (TTXOVS and TTXOVE) plus all suitable lines of the even field (TTXEVS and TTXEVE) can be used for teletext insertion.

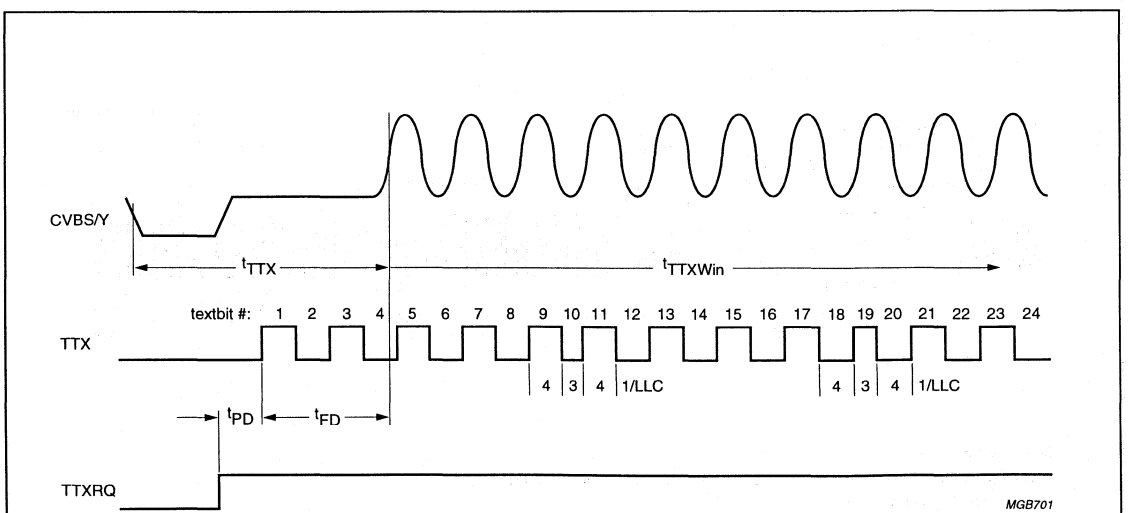
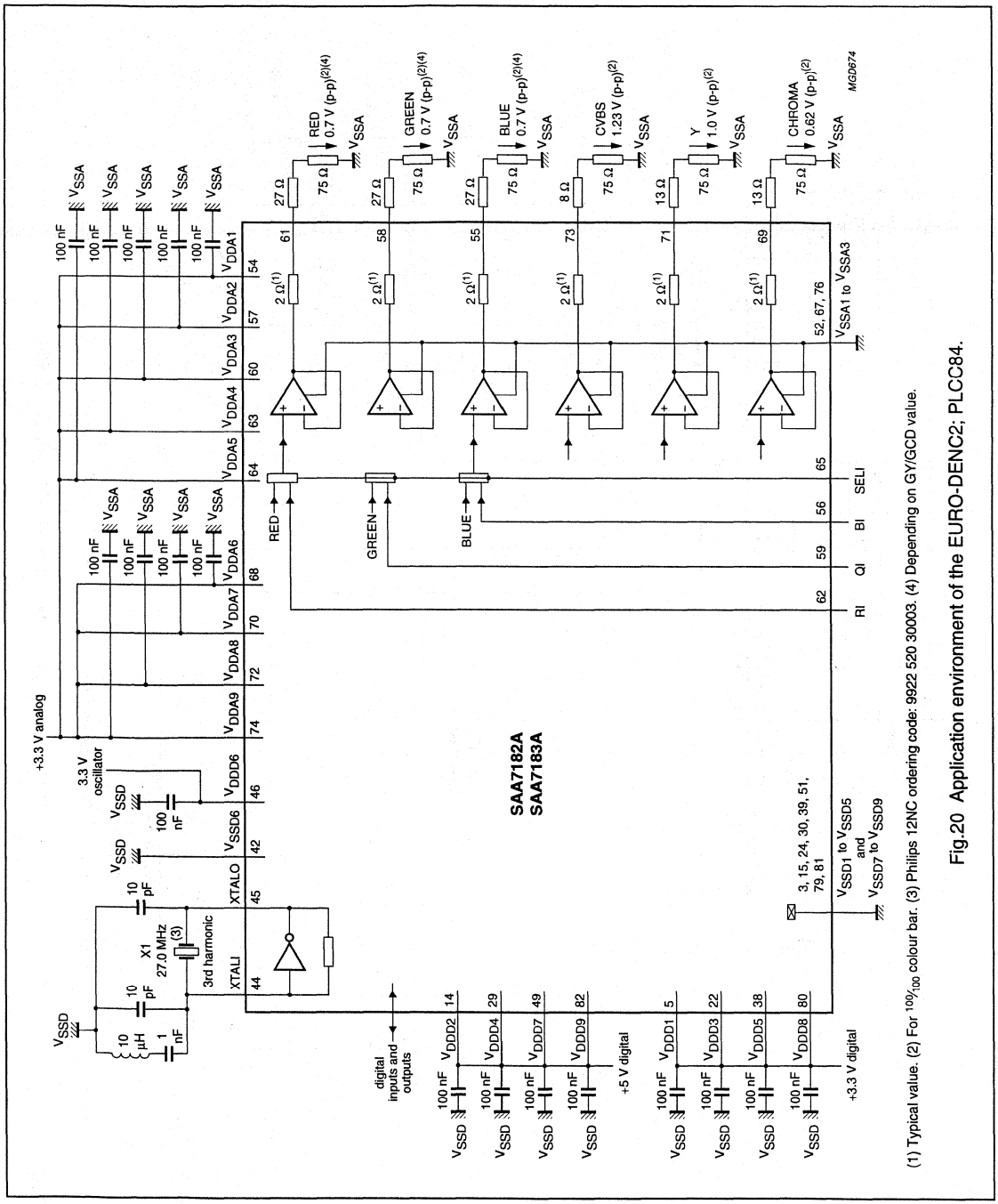


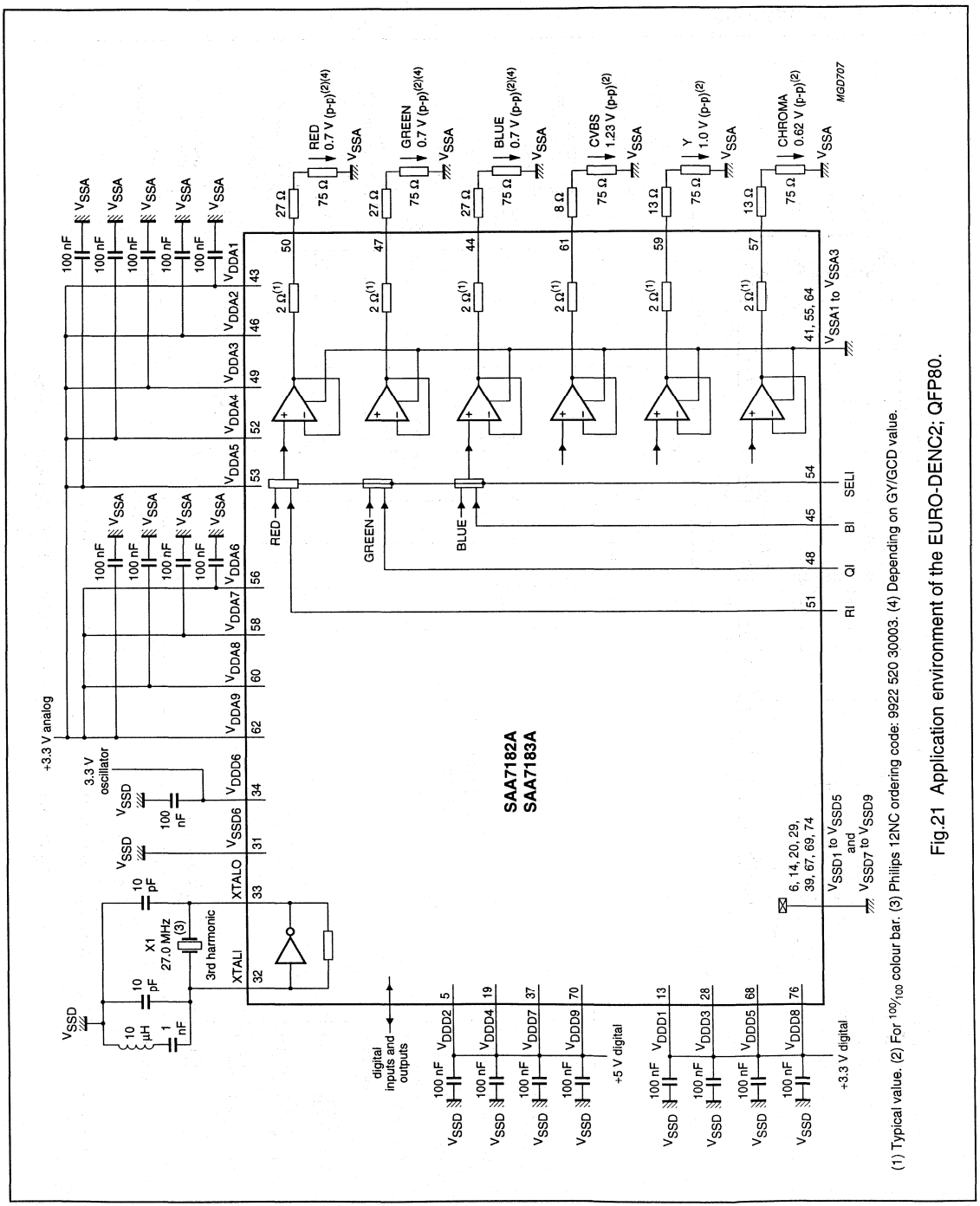
Fig.19 Teletext timing diagram.

APPLICATION INFORMATION



(1) Typical value. (2) For 100/100 colour bar. (3) Philips 12NC ordering code: 9922 520 30003. (4) Depending on GY/GCD value.

Fig.20 Application environment of the EURO-DENC2; PLCC84.



(1) Typical value. (2) For 100/100 colour bar. (3) Philips 12NC ordering code: 9922 520 30003. (4) Depending on GY/GCD value.

Fig.21 Application environment of the EURO-DENC2; QFP80.

Analog output voltages

The analog output voltages are dependent on the open loop voltage of the operational amplifiers for full-scale conversion (typical value 1.4 V), the internal series resistor (typical value 2 Ω), the external series resistor and the external load impedance.

The digital output signals in front of the DACs under nominal conditions occupy different conversion ranges, as indicated in Table 40 for a $^{100}/_{100}$ colour bar signal.

Values for the external series resistors result from a 75 Ω load (see Figs 20 and 21).

The analog inputs RI, GI, and BI are shifted first by an offset of 0.16 V (typical value), followed by an amplification of 1.72 (typical value). For an input voltage of 0 to 0.7 V an open loop output voltage of 0.28 to 1.48 V is achieved, resulting in V_o = 0.86 V (p-p) with an internal series resistor of 2 Ω, an external series resistor of 27 Ω at a 75 Ω load impedance.

Table 40 Digital output signals conversion range

CONVERSION RANGE (peak-to-peak		
CVBS, SYNC TIP-TO-PEAK CARRIER (digits)	**Y (VBS) SYNC TIP-TO-WHITE (digits)**	**RGB (Y) BLACK-TO-WHITE AT GDY = GDC = −6 (digits)**
1023	888	712

Digital Video Encoders (DENC2-M6) SAA7184; SAA7185B

FEATURES

- CMOS 5 V device
- Digital PAL/NTSC encoder
- System pixel frequency 13.5 MHz
- Accepts MPEG decoded data
- 8-bit wide MPEG port
- Input data format Cb, Y, Cr etc. (CCIR 656)
- 16-bit wide YUV input port
- I²C-bus control port or alternatively MPU parallel control port
- Encoder can be master or slave
- Programmable horizontal and vertical input synchronization phase
- Programmable horizontal sync output phase
- OVL overlay with Look-Up Tables (LUTs) 8 × 3 bytes
- Colour bar generator
- Line 21 closed caption encoder
- Cross-colour reduction
- Macrovision revision_6 Pay-per-View copy protection system as option (SAA7184 only). **Remark**: This device is protected by U.S. patent numbers 4631603 4577216 and 4819098 and other intellectual property rights. Use of the Macrovision anticopy process in the device is licensed for non-commercial home use only. Reverse engineering or disassembly is prohibited. Please contact your nearest Philips Semiconductors sales office for more information.
- DACs operating at 27 MHz with 10-bit resolution
- Controlled rise and fall times of output syncs and blanking
- Down-mode of DACs
- CVBS and S-Video output simultaneously
- PLCC68 package.

GENERAL DESCRIPTION

The SAA7184 and SAA7185B digital video encoders 2 (DENC2-M6) encode digital YUV video data to an NTSC or PAL CVBS or S-Video signal.

The circuit accepts CCIR compatible YUV data with 720 active pixels per line in 4 : 2 : 2 multiplexed formats, for example MPEG decoded data. The device includes a sync/clock generator and on-chip Digital-to-Analog Converters (DACs).

The circuit is compatible to the DIG-TV2 chip family.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7184WP	PLCC68	plastic leaded chip carrier; 68 leads	SOT188-2
SAA7185BWP			

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage	4.75	5.0	5.25	V
V_{DDD}	digital supply voltage	4.5	5.0	5.5	V
I_{DDA}	analog supply current	–	50	55	mA
I_{DDD}	digital supply current	–	130	170	mA
V_i	input signal voltage levels	TTL compatible			V
$V_{o(p-p)}$	analog output signal voltages Y, C and CVBS without load (peak-to-peak value)	–	2	–	V
R_L	load resistance	80	–	–	Ω
ILE	LF integral linearity error	–	–	±2	LSB
DLE	LF differential linearity error	–	–	±1	LSB
T_{amb}	operating ambient temperature	0	–	+70	°C

BLOCK DIAGRAM

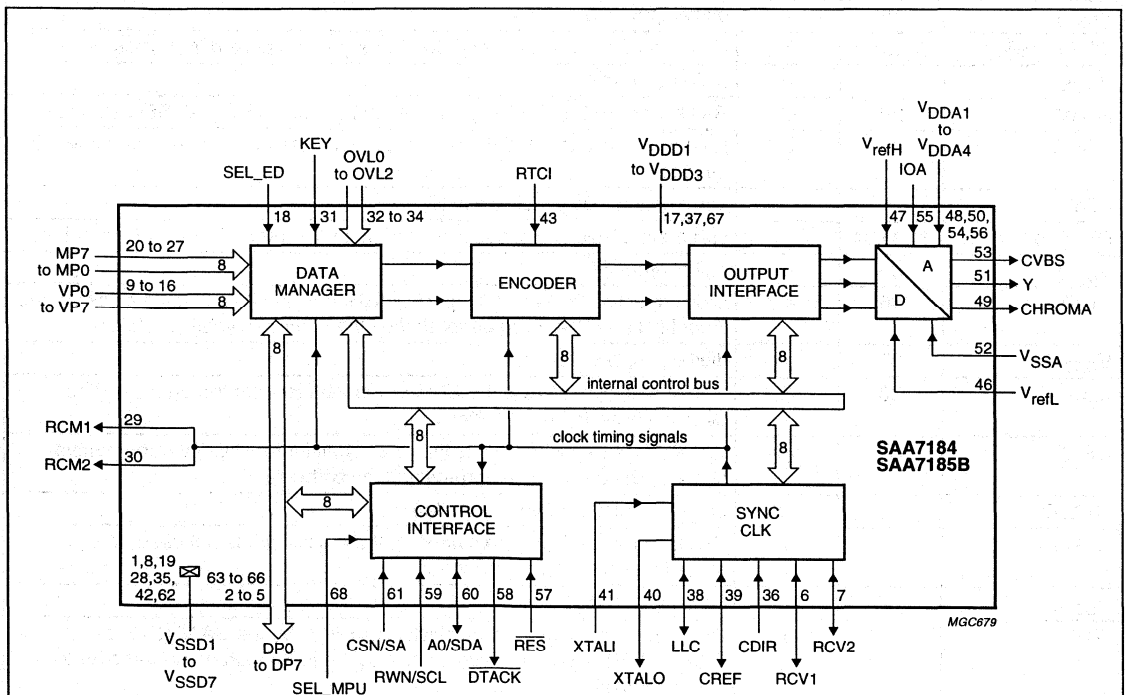


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	I/O	DESCRIPTION
V_{SSD1}	1	–	digital ground 1
DP4 to DP7	2 to 5	I/O	Upper 4 bits of the data port; if pin 68 (SEL_MPU) is HIGH, the data bus of the parallel MPU interface is used. If pin 68 is LOW, then the UV lines of the video port are used.
RCV1	6	I/O	Raster control 1 for video port; depending on the synchronization mode, this pin receives or provides a VS/FS/FSEQ signal.
RCV2	7	I/O	Raster control 2 for video port; depending on the synchronization mode, this pin receives or provides an HS/HREF/CBL signal.
V_{SSD2}	8	–	digital ground 2
VP0 to VP7	9 to 16	I	Video port; this is an input for CCIR 656 compatible multiplexed video data. If the 16-bit DIG-TV2 format is used, then Y data is input.
V_{DDD1}	17	I	digital supply voltage 1
SEL_ED	18	I	select encoder data; selects input data either from the MPEG port or from the video port
V_{SSD3}	19	–	digital ground 3
MP7 to MP0	20 to 27	I	MPEG port; it is an input for CCIR 656 style multiplexed YUV data.
V_{SSD4}	28	–	digital ground 4
RCM1	29	O	Raster control 1 for MPEG port; this pin provides a VS/FS/FSEQ signal.
RCM2	30	O	Raster control 2 for MPEG port; this pin provides an HS pulse for the MPEG decoder.
KEY	31	I	key signal for OVL (active HIGH)
OVL0 to OVL2	32 to 34	I	on-screen display data; this is the index for the internal OVL look-up tables
V_{SSD5}	35	–	digital ground 5
CDIR	36	I	Clock direction; if the CDIR input is HIGH, the circuit receives a clock signal, if not LLC and CREF are generated by the internal crystal oscillator.
V_{DDD2}	37	I	digital supply voltage 2
LLC	38	I/O	Line-locked clock; this is the 27 MHz master clock for the encoder. The direction is set by the CDIR pin.
CREF	39	I/O	Clock reference signal; this is the clock qualifier for DIG-TV2 compatible signals. The polarity is programmable by software.
XTALO	40	O	crystal oscillator output (to crystal)
XTALI	41	I	Crystal oscillator input (from crystal). If the oscillator is not used, this pin should be connected to ground.
V_{SSD6}	42	–	digital ground 6
RTCI	43	I	Real time control Input; if the clock is provided by the SAA7151B or SAA7111, RTCI should be connected to the RTCO pin of the decoder to improve the signal quality.
AP	44	–	test pin (should be connected to digital ground for normal operation)
SP	45	–	test pin (should be connected to digital ground for normal operation)
V_{refL}	46	I	lower reference voltage input for the DACs
V_{refH}	47	I	upper reference voltage input for the DACs
V_{DDA1}	48	I	analog positive supply voltage 1 for the DACs and output amplifiers

SYMBOL	PIN	I/O	DESCRIPTION
CHROMA	49	O	analog output of the chrominance signal
V_{DDA2}	50	I	analog supply voltage 2 for the DACs and output amplifiers
Y	51	O	analog output of the luminance signal
V_{SSA}	52	–	analog ground for the DACs and output amplifiers
CVBS	53	O	analog output of the CVBS signal
V_{DDA3}	54	I	analog supply voltage 3 for the DACs and output amplifiers
IOA	55	I	current input for the output amplifiers (connected via a 15 kΩ resistor to V_{DDA})
V_{DDA4}	56	I	analog supply voltage 4 for the DACs and output amplifiers
$\overline{RES}$	57	I	Reset input, active LOW. After reset is applied, all outputs are in 3-state input mode. The I²C-bus receiver waits for the start condition.
$\overline{DTACK}$	58	O	Data acknowledge output of the parallel MPU interface, active LOW, otherwise high impedance.
RWN/SCL	59	I	If pin 68 (SEL_MPU) is HIGH, this is the read/write signal of the parallel MPU interface. Otherwise it is the I²C-bus serial clock input.
A0/SDA	60	I/O	If pin 68 (SEL_MPU) is HIGH, this is the address signal of the parallel MPU interface. Otherwise it is the I²C-bus serial data input/output.
CSN/SA	61	I	If pin 68 (SEL_MPU) is HIGH, this is the chip select signal of the parallel MPU interface. Otherwise it is the I²C-bus slave address select pin. When LOW slave address = 88H, when HIGH slave address = 8CH.
V_{SSD7}	62	–	digital ground 7
DP0 to DP3	63 to 66	I/O	Lower 4 bits of the data port; if pin 68 (SEL_MPU) is HIGH, the data bus of the parallel MPU interface is used. If pin 68 is LOW, then the UV lines of the video port are used.
V_{DDD3}	67	I	digital supply voltage 3
SEL_MPU	68	I	Select MPU interface input; if it is HIGH, the parallel MPU interface is active, if not the I²C-bus interface will be used.

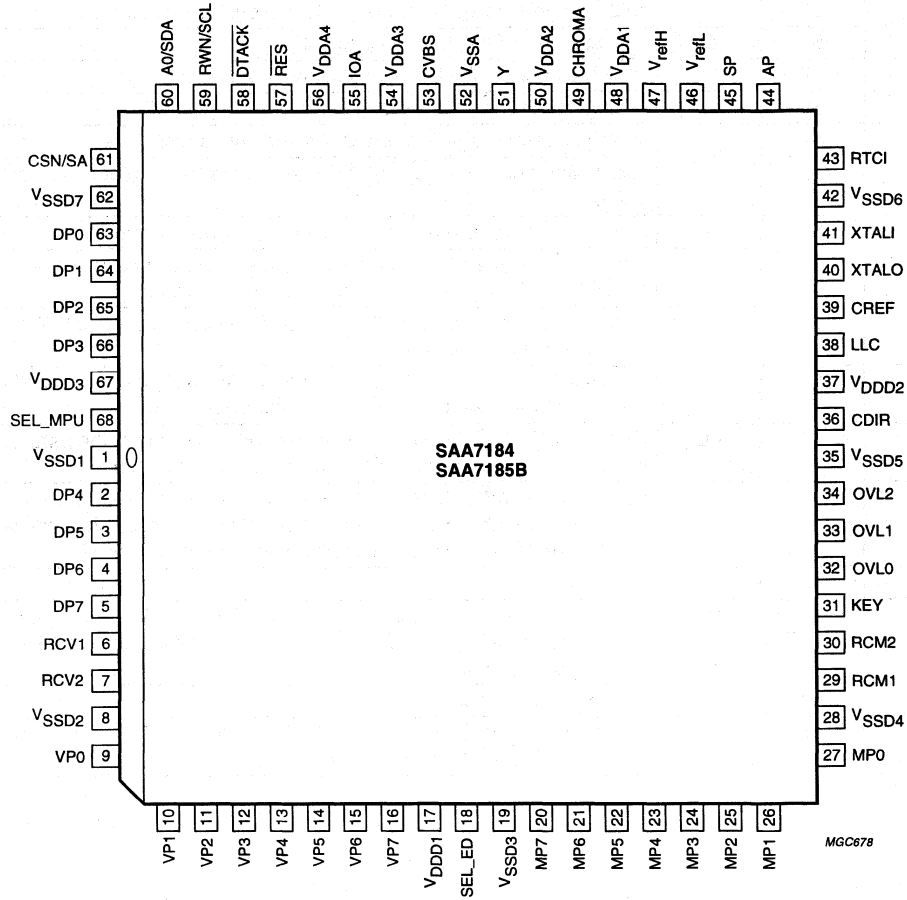


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The digital MPEG-compatible video encoder (DENC2-M6) encodes digital luminance and chrominance into analog CVBS and S-Video (Y/C) signals simultaneously. NTSC-M and PAL B/G standards and sub-standards are also supported.

The basic encoder function consists of subcarrier generation and colour modulation plus insertion of synchronization signals. Luminance and chrominance signals are filtered in accordance with the standard requirements of RS-170-A and CCIR 624.

For ease of analog post filtering the signals are twice oversampled, with respect to the pixel clock, before digital-to-analog conversion.

For total filter transfer characteristics see Figs 3, 4, 5 and 6. The DACs are realized with full 10-bit resolution. The encoder provides three 8-bit wide data ports that serve different applications.

The MPEG port and the video port accept 8 lines multiplexed Cb-Y-Cr data.

The video port is also able to accommodate DIG-TV2 family compatible 16-bit YUV signals. In this event, the data port is used for the U/V components.

Alternatively, the data port can accommodate the data of an 8-bit wide microprocessor interface.

The 8-bit multiplexed Cb-Y-Cr formats are CCIR 656 (D1 format) compatible, but the SAV, EAV etc. codes are not decoded.

A crystal-stable master clock (LLC) of 27 MHz, which is twice the CCIR line-locked pixel clock frequency of 13.5 MHz, needs to be supplied externally. A crystal oscillator input/output pair of pins and an on-chip clock driver are provided optionally. It is also possible to connect the Philips Digital Video Decoder (SAA7111 or SAA7151B) in conjunction with a CREF clock qualifier to the DENC2-M6 via the RETCI pin (connected to RTCO) of a decoder. Information concerning the actual subcarrier, PAL-ID and (with SAA7111) definite subcarrier phase can be inserted.

The DENC2-M6 synthesizes all necessary internal signals, colour subcarrier frequency and synchronization signals, from that clock. The DENC2-M6 is always the timing master for the MPEG port but can also be configured as master or slave for the video port.

The IC also contains closed caption and extended data services encoding (line 21), and supports anti-taping signal generation in accordance with Macrovision.
It also supports OVL via KEY and 3-bit overlay techniques using a 24 × 8 LUT.

The IC can be programmed via the I²C-bus or via the 8-bit MPU interface, but only one interface configuration can be active at a time. If the 16-bit video port mode (VP and DP) is being used, only the I²C-bus interface can be selected.

A number of possibilities are provided for setting the different video parameters such as:

- black and blanking level control
- colour subcarrier frequency
- black variable burst amplitude etc.

During reset ($\overline{RES}$ = LOW) and after reset is released, all digital I/O stages are set to the input mode. A reset forces the control interfaces to abort any running bus transfer and to set register 3AH to contents 1FH, register 61H to contents 06H, and registers 6CH and 7AH to contents 00H. All other control registers are not influenced by a reset.

Data manager

Real time arbitration on the data stream to be encoded is performed in the data manager.

Depending on the hardware conditions (signals on pins SEL_ED, KEY, OVL2 to OVL0, MP7 to MP0, VP7 to VP0 and DP7 to DP0) and different software programming, either data from the MP port, from the VP port or from the OVL port, is selected to be encoded to CVBS and Y/C signals.

Optionally, the OVL colour look-up tables located in this block can be read out in a pre-defined sequence (8 steps per active video line) thereby achieving, for example, a colour bar test pattern generator without the need for an external data source. The colour bar function is only under software control.

Encoder

VIDEO PATH

The encoder generates luminance and colour subcarrier output signals, suitable for use as CVBS or separate Y/C signals, from the Y, U and V baseband signals.

The luminance gain and offset are modified (offset being programmable within a certain range to enable different black level set-ups). After the signals have been inserted, a fixed synchronization level in accordance with standard composite synchronization schemes and blanking level, (also programmable in a certain range to allow for manipulations with Macrovision anti-tapping) additional insertion of AGC super white pulses (programmable in height) is supported.

In order to enable easy analog post filtering, luminance is interpolated from a 13.5 MHz data rate to a 27 MHz data rate, thereby providing luminance in a 10-bit resolution. This filter is also used to define smoothed transients for synchronization pulses and blanking period. The transfer characteristics of the luminance interpolation filter are illustrated in Figs 5 and 6.

The chrominance gain is modified (programmable separately for U and V), a standard dependent burst is inserted before baseband colour signals are interpolated from a 6.75 MHz data rate to a 27 MHz data rate. One of the interpolation stages can be bypassed, thereby providing a higher colour bandwidth, which can be used for the Y/C output. The transfer characteristics of the chrominance interpolation filter are illustrated in Figs 3 and 4.

The amplitude of the inserted burst is programmable within a certain range, suitable for standard signals and for special effects. Colour in a 10-bit resolution is provided on the subcarrier after the succeeding quadrature modulator.

The numeric ratio between Y and C outputs is in accordance with set standards.

CLOSED CAPTION ENCODER

Using the closed caption encoder circuit, data in accordance with the specification of closed caption or extended data service, delivered by the control interface, can be encoded (line 21). Two dedicated pairs of bytes (two bytes per field) are possible, each pair preceded by run-in clocks and framing code.

The actual line number where data is to be encoded, can be modified within a certain range.

The data clock frequency is in accordance with the definition for NTSC-M standard 32 times horizontal line frequency.

Data LOW at the output of the DACs corresponds to 0 IRE, data HIGH at the output of the DACs corresponds to approximately 50 IRE.

It is also possible to encode closed caption data for 50 Hz field frequencies at 32 times horizontal line frequency.

Output interface

In the output interface, encoded Y and C signals are converted from digital to analog in a 10-bit resolution and then combined into a 10-bit CVBS signal. Also, in front of the summation point, the luminance signal can be fed through a further filter stage (optional), thereby suppressing components in the subcarrier frequency range. Thus, a type of cross colour reduction is provided, which is useful in a standard TV set with CVBS input.

The slopes of the synchronization pulses are not affected with any active cross colour reduction.

Three different filter characteristics or bypass are available, see Fig.5.

The CVBS output occurs with the same processing delay as the Y and C outputs. Absolute amplitudes at the input of the DAC for CVBS is reduced by $^{15}/_{16}$ with respect to Y and C DACs to make maximum use of conversion ranges.

Outputs of all DACs can be set together, via software control, to minimum output voltage for either purpose.

Synchronization

The synchronization of the DENC2 is able to operate in two modes; slave mode and master mode.

In the slave mode, the circuit accepts synchronization pulses at the bidirectional RCV1 port. The timing and trigger behaviour, related to the video signal on VP (and DP, if used), can be influenced by programming the polarity and on-chip delay of RCV1. The active slope of RCV1 defines the vertical phase and, as an option, the odd/even and colour frame phase to be initialized. It can also be used to set the horizontal phase.

If the horizontal phase is not to be influenced by RCV1, a horizontal pulse needs to be applied at pin RCV2. Timing and trigger behaviour can also be influenced for RCV2.

If there are missing pulses at RCV1 and/or RCV2, the time base of the DENC2-M6 will become free-running, thus an arbitrary number of synchronization slopes may miss, but no additional pulses must occur (such as with wrong phase).

If the vertical and horizontal phase is derived from RCV1, RCV2 can be used for horizontal or composite blanking input or output.

In the master mode, the time base of the circuit is continuously free-running. At the RCV1 port, the IC can output:

- A vertical sync signal (VS) with 3 or 2.5 lines duration, or
- An odd/even signal which is LOW in odd fields, or
- A field sequence signal (FSEQ) which is HIGH in the first of 4 respectively 8 fields.

The IC can provide a horizontal pulse with programmable start and stop phase at the RCV2 port. This pulse can be inhibited in the vertical blanking period to build up, for example, a composite blanking signal.

The phase of the output pulses at RCV1 or RCV2 are referenced to the VP port, polarity of both signals is selectable.

The DENC2-M6 is **always** the timing master for the source at the MP input. The IC provides two signals for synchronizing this source:

1. At the RCM1 port the same signals as at RCV1 (as output) are available.
2. At RCM2 the IC provides a horizontal pulse with programmable start and stop phase.

The start and end of the active part can be programmed. The active part of a field always starts at the beginning of a line if the standard blanking option SBLBN is not set.

Control interface

DENC2-M6 contains two control interfaces, an I²C-bus slave transceiver and an 8-bit parallel microprocessor interface. The interfaces cannot be used simultaneously.

The I²C-bus interface is a standard slave transceiver, supporting 7-bit slave addresses and 400 kbits/s guaranteed transfer rate. It uses 8-bit subaddressing with an auto-increment function. All registers are write only, except one status byte which can be read.

Two I²C-bus slave addresses can be selected (pin SEL_MPU must be LOW):

88H: pin 61 = LOW

8CH: pin 61 = HIGH.

The parallel interface is defined by:

D7 to D0 data bus

$\overline{CS}$ active LOW chip select signal

R$\overline{W}$ read/write signal, LOW for a write cycle

$\overline{DTACK}$ 680xx style data acknowledge (handshake), active-LOW

A0 register select, LOW selects address, HIGH selects data.

The parallel interface uses two registers, one auto-incremental containing the current address of a control register (equals subaddress with I²C-bus control), and one containing actual data. The currently addressed register is mapped to the corresponding control register.

The status byte can be read (optionally) via a read access to the address register, no other read access is provided.

Input levels and formats

DENC2-M6 accepts digital YUV data with levels (digital codes) in accordance with CCIR 601.

Deviating amplitudes in the colour difference signals can be compensated for by independent gain control setting, while the gain for luminance is set to predefined values, distinguishable for 7.5 IRE set-up or without set-up.

The MPEG port accepts only 8-bit multiplexed CCIR 656 compatible data.

If the I²C-bus interface is used, the VP port can accommodate both formats, 8-bit multiplexed Cb-Y-Cr data on the VP lines, or the 16-bit DTV2 format with the Y signal on the VP lines and the UV signal on the DP port.

Reference levels are measured with a colour bar, 100% white, 100% amplitude and 100% saturation.

Table 1 CCIR signal component levels

SIGNAL	IRE	DIGITAL LEVEL	CODE
Y	0	16	straight binary
	50	126	
	100	235	
Cb	bottom peak	16	straight binary
	colourless	128	
	top peak	240	
Cr	bottom peak	16	straight binary
	colourless	128	
	top peak	240	

Table 2 8-bit multiplexed format (similar to CCIR 656)

TIME	0	1	2	2	4	5	6	7
Sample	Cb_0	Y_0	Cr_0	Y_1	Cb_2	Y_2	Cr_2	Y_3
Luminance pixel number	0		1		2		3	
Colour pixel number	0				2			

Table 3 16-bit multiplexed format (DTV2 format)

TIME	0	1	2	3	4	5	6	7
Sample Y line	Y_0		Y_1		Y_2		Y_3	
Sample UV line	Cb_0		Cr_0		Cb_2		Cr_2	
Luminance pixel number	0		1		2		3	
Colour pixel number	0				2			

Bit allocation map

Table 4 Slave receiver (slave address 88h or 8Ch)

REGISTER FUNCTION	SUB ADDRESS	DATA BYTE (note 1)							
		D7	D6	D5	D4	D3	D2	D1	D0
Null	00	0	0	0	0	0	0	0	0
	↓	↓							
Null	39	0	0	0	0	0	0	0	0
Input port control	3A	CBENB	0	0	V656	VY2C	VUV2C	MY2C	MUV2C
OVL LUT Y0	42	OVLY07	OVLY06	OVLY05	OVLY04	OVLY03	OVLY02	OVLY01	OVLY00
OVL LUT U0	43	OVLU07	OVLU06	OVLU05	OVLU04	OVLU03	OVLU02	OVLU01	OVLU00
OVL LUT V0	44	OVLV07	OVLV06	OVLV05	OVLV04	OVLV03	OVLV02	OVLV01	OVLV00
	↓	↓							
OVL LUT Y7	57	OVLY77	OVLY76	OVLY75	OVLY74	OVLY73	OVLY72	OVLY71	OVLY70
OVL LUT U7	58	OVLU77	OVLU76	OVLU75	OVLU74	OVLU73	OVLU72	OVLU71	OVLU70
OVL LUT V7	59	OVLV77	OVLV76	OVLV75	OVLV74	OVLV73	OVLV72	OVLV71	OVLV70
Chrominance phase	5A	CHPS7	CHPS6	CHPS5	CHPS4	CHPS3	CHPS2	CHPS1	CHPS0
Gain U	5B	GAINU7	GAINU6	GAINU5	GAINU4	GAINU3	GAINU2	GAINU1	GAINU0
Gain V	5C	GAINV7	GAINV6	GAINV5	GAINV4	GAINV3	GAINV2	GAINV1	GAINV0
Gain U MSB, black level	5D	GAINU8	0	BLCKL5	BLCKL4	BLCKL3	BLCKL2	BLCKL1	BLCKL0
Gain V MSB, blanking level	5E	GAINV8	0	BLNNL5	BLNNL4	BLNNL3	BLNNL2	BLNNL1	BLNNL0
Null	60	0	0	0	0	0	0	0	0
Standard control	61	0	DOWN	INPI1	YGS	RTCE	SCBW	PAL	FISE
Burst amplitude	62	DECTYP	BSTA6	BSTA5	BSTA4	BSTA3	BSTA2	BSTA1	BSTA0
Subcarrier 0	63	FSC07	FSC06	FSC05	FSC04	FSC03	FSC02	FSC01	FSC00
Subcarrier 1	64	FSC15	FSC14	FSC13	FSC12	FSC11	FSC10	FSC09	FSC08
Subcarrier 2	65	FSC23	FSC22	FSC21	FSC20	FSC19	FSC18	FSC17	FSC16
Subcarrier 3	66	FSC31	FSC30	FSC29	FSC28	FSC27	FSC26	FSC25	FSC24
Line 21 odd 0	67	L21O07	L21O06	L21O05	L21O04	L21O03	L21O02	L21O01	L21O00
Line 21 odd 1	68	L21O17	L21O16	L21O15	L21O14	L21O13	L21O12	L21O11	L21O10
Line 21 even 0	69	L21E07	L21E06	L21E05	L21E04	L21E03	L21E02	L21E01	L21E00
Line 21 even 1	6A	L21E17	L21E16	L21E15	L21E14	L21E13	L21E12	L21E11	L21E10
Encoder control, CC line	6B	MODIN1	MODIN0	PCREF	SCCLN4	SCCLN3	SCCLN2	SCCLN1	SCCLN0
RCV port control	6C	SRCV11	SRCV10	TRCV2	ORCV1	PRCV1	CBLF	ORCV2	PRCV2

REGISTER FUNCTION	SUB ADDRESS	DATA BYTE (note 1)							
		D7	D6	D5	D4	D3	D2	D1	D0
RCM, CC mode	6D	0	0	0	0	SRCM11	SRCM10	CCEN1	CCEN0
Horizontal trigger	6E	HTRIG7	HTRIG6	HTRIG5	HTRIG4	HTRIG3	HTRIG2	HTRIG1	HTRIG0
Horizontal trigger	6F	HTRIG8	HTRIG9	HTRIG10	0	0	0	0	0
f_{sc} reset mode, Vertical trigger	70	PHRES1	PHRES0	SBLBN	VTRIG4	VTRIG3	VTRIG2	VTRIG1	VTRIG0
Begin MP request	71	BMRQ7	BMRQ6	BMRQ5	BMRQ4	BMRQ3	BMRQ2	BMRQ1	BMRQ0
End MP request	72	EMRQ7	EMRQ6	EMRQ5	EMRQ4	EMRQ3	EMRQ2	EMRQ1	EMRQ0
MSBs MP request	73	0	EMRQ10	EMRQ09	EMRQ08	0	BMRQ10	BMRQ09	BMRQ08
Null	74	0	0	0	0	0	0	0	0
Null	75	0	0	0	0	0	0	0	0
Null	76	0	0	0	0	0	0	0	0
Begin RCV2 output	77	BRCV7	BRCV6	BRCV5	BRCV4	BRCV3	BRCV2	BRCV1	BRCV0
End RCV2 output	78	ERCV7	ERCV6	ERCV5	ERCV4	ERCV3	ERCV2	ERCV1	ERCV0
MSBs RCV2 output	79	0	ERCV10	ERCV09	ERCV08	0	BRCV10	BRCV09	BRCV08
Field length	7A	0	0	0	0	0	0	FLC1	FLC0
First active line	7B	FAL7	FAL6	FAL5	FAL4	FAL3	FAL2	FAL1	FAL0
Last active line	7C	LAL7	LAL6	LAL5	LAL4	LAL3	LAL2	LAL1	LAL0
MSBs field control	7D	0	0	LAL8	FAL8	0	0	0	0

Note

1. *All bits labelled '0' are reserved. They* ***must*** *be programmed with logic 0.*

I²C-bus format

Table 5 I²C-bus address; see Table 6

S	SLAVE ADDRESS	ACK	SUBADDRESS	ACK	DATA 0	ACK	--------	DATA n	ACK	P

Table 6 Explanation of Table 5

PART	DESCRIPTION
S	START condition
Slave address	1 0 0 0 1 0 0 X or 1 0 0 0 1 1 0 X (note 1)
ACK	acknowledge, generated by the slave
Subaddress (note 2)	subaddress byte
DATA	data byte
--------	continued data bytes and ACKs
P	STOP condition

Notes

1. X is the read/write control bit; X = logic 0 is order to write; X = logic 1 is order to read, no subaddressing with read.
2. If more than 1 byte DATA is transmitted, then auto-increment of the subaddress is performed.

Slave Receiver

Table 7 Subaddress 3A

DATA BYTE	LOGIC LEVEL	DESCRIPTION
MUV2C	0	Cb/Cr data at MP is two's complement.
	1	Cb/Cr data at MP is straight binary. Default after reset.
MY2C	0	Y data at MP is two's complement.
	1	Y data at MP is straight binary. Default after reset.
VUV2C	0	Cb/Cr data input to VP or DP is two's complement
	1	Cb/Cr data input to VP or DP is straight binary. Default after reset.
VY2C	0	Y data input to VP is two's complement
	1	Y data input to VP is straight binary. Default after reset.
V656	0	selects YUV 422 format on VP (8 lines Y) and DP (8 lines multiplexed Cb/Cr).
	1	selects CCIR 656 compatible format on VP (8 lines Cb, Y, Cr). Default after reset.
CBENB	0	data from input ports is encoded. Default after reset.
	1	colour bar with programmable colours (entries of OVL_LUTs) is encoded. The LUTs are read in upward order from index 0 to index 7.

Table 8 Subaddress 42 to 59

COLOUR	DATA BYTE[1]			INDEX[2]
	OVLY	OVLU	OVLV	
White	107 (6BH)	0 (00H)	0 (00H)	0
	107 (6BH)	0 (00H)	0 (00H)	
Yellow	82 (52H)	144 (90H)	18 (12H)	1
	34 (22H)	172 (ACH)	14 (0EH)	
Cyan	42 (2AH)	38 (26H)	144 (90H)	2
	03 (03H)	29 (1DH)	172 (ACH)	
Green	17 (11H)	182 (B6H)	162 (A2H)	3
	240 (F0H)	200 (C8H)	185 (B9H)	
Magenta	234 (EAH)	74 (4AH)	94 (5EH)	4
	212 (D4H)	56 (38H)	71 (47H)	
Red	209 (D1H)	218 (DAH)	112 (70H)	5
	193 (C1H)	227 (E3H)	84 (54H)	
Blue	169 (A9H)	112 (70H)	238 (EEH)	6
	163 (A3H)	84 (54h)	242 (F2H)	
Black	144 (90H)	0 (00H)	0 (00H)	7
	144 (90H)	0 (00H)	0 (00H)	

Notes

1. Contents of OVL look-up tables. All 8 entries are 8-bits. Data representation is in accordance with *CCIR 601* (Y, Cb, Cr), but two's complement, e.g. for a $^{100}/_{100}$ (upper number) or $^{100}/_{75}$ (lower number) colour bar.
2. For normal colour bar with CBENB = logic 1.

Table 9 Subaddress 5A

DATA BYTE	DESCRIPTION
CHPS	phase of encoded colour subcarrier (including burst) relative to horizontal sync. Can be adjusted in steps of 360/256 degrees.

Table 10 Subaddress 5B and 5D

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
GAINU	variable gain for Cb signal; input representation in accordance with *"CCIR 601"*	white-to-black = 92.5 IRE[1]	
		GAINU = 0	output subcarrier of U contribution = 0
		GAINU = 118 (76H)	output subcarrier of U contribution = nominal
		white-to-black = 100 IRE[2]	
		GAINU = 0	output subcarrier of U contribution = 0
		GAINU = 125 (7DH)	output subcarrier of U contribution = nominal

Notes

1. GAINU = –2.17 × nominal to +2.16 × nominal.
2. GAINU = –2.05 × nominal to +2.04 × nominal.

Table 11 Subaddress 5C and 5E

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
GAINV	variable gain for Cr signal; input representation in accordance with *"CCIR 601"*	white-to-black = 92.5 IRE[1]	
		GAINV = 0	output subcarrier of V contribution = 0
		GAINV = 165 (A5H)	output subcarrier of V contribution = nominal
		white-to-black = 100 IRE[2]	
		GAINV = 0	output subcarrier of V contribution = 0
		GAINV = 175 (AFH)	output subcarrier of V contribution = nominal

Notes

1. GAINV = −1.55 × nominal to + 0.55 × nominal.
2. GAINV = −1.46 × nominal to + 0.46 × nominal.

Table 12 Subaddress 5D

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
BLCKL	variable black level; input representation in accordance with *"CCIR 601"*	white-to-sync = 140 IRE[1]	
		BLCKL = 0	output black level = 24 IRE
		BLCKL = 63 (3FH)	output black level = 49 IRE
		white-to-sync = 143 IRE[2]	
		BLCKL = 0	output black level = 24 IRE
		BLCKL = 63 (3FH)	output black level = 50 IRE

Notes

1. Output black level/IRE = BLCKL × 25/63 + 24; recommended value: BLCKL = 60 (3CH) normal.
2. Output black level/IRE = BLCKL × 26/63 + 24; recommended value: BLCKL = 45 (2DH) normal.

Table 13 Subaddress 5E

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
BLNNL	variable blanking level	white-to-sync = 140 IRE[1]	
		BLNNL = 0	output blanking level = 17 IRE
		BLNNL = 63 (3FH)	output blanking level = 42 IRE
		white-to-sync = 143 IRE[2]	
		BLNNL = 0	output blanking level = 17 IRE
		BLNNL = 63 (3FH)	output blanking level = 43 IRE

Notes

1. Output black level/IRE = BLNNL × 25/63 + 17; recommended value: BLNNL = 58 (3AH) normal.
2. Output black level/IRE = BLNNL × 26/63 + 17; recommended value: BLNNL = 63 (3FH) normal.

Table 14 Subaddress 5F (CCRS and BLNVB; note 1)

DATA BYTE		FUNCTION
CCRS1	CCRS0	
0	0	no cross colour reduction (for overall transfer characteristic of luminance see Fig.5)
0	1	cross colour reduction #1 active (for overall transfer characteristic see Fig.5)
1	0	cross colour reduction #2 active (for overall transfer characteristic see Fig.5)
1	1	cross colour reduction #3 active (for overall transfer characteristic see Fig.5)

Note

1. BLNVB = vertical blanking level during vertical blanking interval and its value is typically identical to BLNNL.

Table 15 Subaddress 61

DATA BYTE	LOGIC LEVEL	DESCRIPTION
FISE	0	864 total pixel clocks per line. Default after reset.
	1	858 total pixel clocks per line
PAL	0	NTSC encoding (non-alternating V component)
	1	PAL encoding (alternating V component). Default after reset.
SCBW	0	enlarged bandwidth for chrominance encoding (for overall transfer characteristic of chrominance in baseband representation see Figs 3 and 4)
	1	standard bandwidth for chrominance encoding (for overall transfer characteristic of chrominance in baseband representation see Figs 3 and 4). Default after reset.
RTCE	0	no real time control of generated subcarrier frequency. Default after reset.
	1	real time control of generated subcarrier frequency through SAA7151B or SAA7111 (see Fig.9)
YGS	0	luminance gain for white – black 100 IRE. Default after reset.
	1	luminance gain for white – black 92.5 IRE including 7.5 IRE set-up of black
INPI	0	PAL switch phase is nominal. Default after reset.
	1	PAL switch phase is inverted compared to nominal
DOWN	0	DACs in normal operational mode. Default after reset.
	1	DACs forced to lowest output voltage

Table 16 Subaddress 62

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
BSTA	amplitude of colour burst; input representation in accordance with *CCIR 601*	white-to-black = 92.5 IRE; burst = 40 IRE; NTSC encoding BSTA = 0 to 1.25 × nominal(1) white-to-black = 92.5 IRE; burst = 40 IRE; PAL encoding BSTA = 0 to 1.76 × nominal(2) white-to-black = 100 IRE; burst = 43 IRE; NTSC encoding BSTA = 0 to 1.20 × nominal(3) white-to-black = 100 IRE; burst = 43 IRE; PAL encoding BSTA = 0 to 1.67 × nominal(4)	
DECTYP	real time control input (RTCI)	logic 0	control from SAA7151B digital colour decoder
		logic 1	control from SAA7111 video input processor (VIP)

Notes

1. Recommended value: BSTA = 102 (66H).
2. Recommended value: BSTA = 72 (48H).
3. Recommended value: BSTA = 106 (6AH).
4. Recommended value: BSTA = 75 (4BH).

Table 17 Subaddress 63 to 66 (four bytes to program subcarrier frequency)

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
FSC0 to FSC3	f_{fsc} = subcarrier frequency (in multiples of line frequency); f_{llc} = clock frequency (in multiples of line frequency)	$FSC = \text{round}\left(\frac{f_{fsc}}{f_{llc}} \times 2^{32}\right)$ see note 1	FSC3 = most significant byte FSC0 = least significant byte

Note

1. Examples:
   a) NTSC-M: f_{fsc} = 227.5, f_{llc} = 1716 → FSC = 569408543 (21F07C1FH).
   b) PAL-B/G: f_{fsc} = 283.7516, f_{llc} = 1728 → FSC = 705268427 (2A098ACBH).

Table 18 Subaddress 67 to 6A

DATA BYTE[1]	DESCRIPTION
L21O0	first byte of captioning data, odd field
L21O1	second byte of captioning data, odd field
L21E0	first byte of extended data, even field
L21E1	second byte of extended data, even field

Note

1. LSBs of the respective bytes are encoded immediately after run-in and framing code, the MSBs of the respective bytes have to carry the parity bit, in accordance with the definition of line 21 encoding format.

Table 19 Subaddress 6B

DATA BYTE	DESCRIPTION
SCCLN	selects the actual line, where closed caption or extended data is encoded; see note 1
MODIN	defines video data of MP port or VP (DP) port to be encoded; see Table 20
PCREF	0 = normal polarity of CREF for DIG TV2 compatible input signals; 1 = inverted

Note

1. Line = (SCCLN + 4) for M systems; line = (SCCLN + 1) for other systems.

Table 20 Logic levels and function of MODIN

DATA BYTE		FUNCTION
MODIN1	MODIN0	
0	0	unconditionally from MP port
0	1	from MP port, if pin SEL_ED = HIGH; otherwise from VP port
1	0	unconditionally from VP port
1	1	from VP port, if pin SEL_ED = HIGH; otherwise from MP port

Table 21 Subaddress 6C

DATA BYTE	LOGIC LEVEL	DESCRIPTION
PRCV2	0	polarity of RCV2 as output is active HIGH, rising edge is taken when input, respectively. Default after reset
	1	polarity of RCV2 as output is active LOW, falling edge is taken when input, respectively
ORCV2	0	pin RCV2 is switched to input. Default after reset
	1	pin RCV2 is switched to output
CBLF	0	if ORCV2 = HIGH, pin RCV2 provides an HREF signal (Horizontal Reference Pulse that is defined by RCV2S and RCV2E, also during vertical blanking Interval). Default after reset if ORCV2 = LOW, signal input to RCV2 is used for horizontal synchronization only (if TRCV2 = 1). Default after reset
	1	if ORCV2 = HIGH, pin RCV2 provides a 'composite blanking not' signal i.e. a reference pulse that is defined by RCV2S and RCV2E, excluding vertical blanking Interval, which is defined by FAL and LAL (PRCV2 must be LOW) if ORCV2 = LOW, signal input to RCV2 is used for horizontal synchronization (if TRCV2 = 1) and as an internal blanking signal
PRCV1	0	polarity of RCV1 as output is active HIGH, rising edge is taken when input, respectively. Default after reset
	1	polarity of RCV1 as output is active LOW, falling edge is taken when input, respectively
ORCV1	0	pin RCV1 is switched to input. Default after reset
	1	pin RCV1 is switched to output
TRCV2	0	horizontal synchronization is taken from RCV1 port. Default after reset
	1	horizontal synchronization is taken from RCV2 port
SRCV1	–	defines signal type on pin RCV1; see Table 22

Table 22 Logic levels and function of SRCV1

DATA BYTE		AS OUTPUT	AS INPUT	FUNCTION
SRCV11	SRCV10			
0	0	VS	VS	vertical sync each field. Default after reset
0	1	FS	FS	frame sync (odd/even)
1	0	FSEQ	FSEQ	field sequence, vertical sync every fourth field (PAL = 0) or eighth field (PAL = 1)
1	1	not applicable	not applicable	

Table 23 Subaddress 6D

DATA BYTE	DESCRIPTION
CCEN	enables individual line 21 encoding; see Table 24
SRCM	defines signal type on pin RCM1; see Table 25

Table 24 Logic levels and function of CCEN

DATA BYTE		FUNCTION
CCEN1	CCEN0	
0	0	line 21 encoding OFF
0	1	enables encoding in field 1 (odd)
1	0	enables encoding in field 2 (even)
1	1	enables encoding in both fields

Table 25 Logic levels and function of SRCM

DATA BYTE		AS OUTPUT	FUNCTION
SRCM1	SRCM0		
0	0	VS	vertical sync each field
0	1	FS	frame sync (odd/even)
1	0	FSEQ	field sequence, vertical sync every fourth field (FISE = 1) or eighth field (FISE = 0)
1	1	not applicable	

Table 26 Subaddress 6E to 6F

DATA BYTE	DESCRIPTION
HTRIG	sets the horizontal trigger phase related to signal on RCV1 or RCV2 input values above 1715 (FISE = 1) or 1727 (FISE = 0) are not allowed increasing HTRIG decreases delays of all internally generated timing signals reference mark: analog output horizontal sync (leading slope) coincides with active edge of RCV used for triggering at HTRIG = 037H

Table 27 Subaddress 70

DATA BYTE	LOGIC LEVEL	DESCRIPTION
VTRIG	–	sets the vertical trigger phase related to signal on RCV1 input increasing VTRIG decreases delays of all internally generated timing signals, measured in half lines variation range of VTRIG = 0 to 31 (1FH)
SBLBN	0	vertical blanking is defined by programming of FAL and LAL
	1	vertical blanking is forced in accordance with CCIR-624 (50 Hz) or RS170A (60 Hz); note 1
PHRES	–	selects the phase reset mode of the colour subcarrier generator; see Table 28

Note

1. If cross-colour reduction is programmed, it is active between FAL and LAL in both events.

Table 28 Logic levels and function of PHRES

DATA BYTE		FUNCTION
PHRES1	PHRES0	
0	0	no reset or reset via RTCI from SAA7111 if bit RTCE = 1
0	1	reset every two lines
1	0	reset every eight fields
1	1	reset every four fields

Table 29 Subaddress 71 to 73

DATA BYTE	DESCRIPTION
BMRQ	beginning of MP request signal (RCM2) values above 1715 (FISE = 1) or 1727 [FISE = 0] are not allowed first active pixel at analog outputs (corresponding input pixel coinciding with RCM2) at BMRQ = 0F9H [117H]
EMRQ	end of MP request signal (RCM2) values above 1715 (FISE = 1) or 1727 [FISE = 0] are not allowed last active pixel at analog outputs (corresponding input pixel coinciding with RCM2) at EMRQ = 683H [691H]

Table 30 Subaddress 77 to 79

DATA BYTE	DESCRIPTION
BRCV	beginning of output signal on RCV2 pin values above 1715 (FISE = 1) or 1727 [FISE = 0] are not allowed first active pixel at analog outputs (corresponding input pixel coinciding with RCV2) at BRCV = 0F9H [117H]
ERCV	end of output signal on RCV2 pin values above 1715 (FISE = 1) or 1727 (FISE = 0) are not allowed last active pixel at analog outputs (corresponding input pixel coinciding with RCV2) at ERCV = 683H [691H]

Table 31 Subaddress 7A

DATA BYTE		DESCRIPTION
FLC1	FLC0	
0	0	field length control interlaced 312.5 lines/fields at 50 Hz, 262.5 lines/fields at 60 Hz (reset default)
0	1	field length control non-interlaced 312 lines/fields at 50 Hz, 262 lines/fields at 60 Hz
1	0	field length control non-interlaced 313 lines/fields at 50 Hz, 262 lines/fields at 60 Hz
1	1	field length control non-interlaced 313 lines/fields at 50 Hz, 262 lines/fields at 60 Hz

Table 32 Subaddress 7B to 7D

DATA BYTE	DESCRIPTION
FAL	first active line = FAL + 4 for M systems; = FAL + 1 for other systems, measured in lines FAL = 0 coincides with the first field synchronization pulse
LAL	last active line = LAL + 3 for M systems; = LAL for other systems, measured in lines LAL = 0 coincides with the first field synchronization pulse

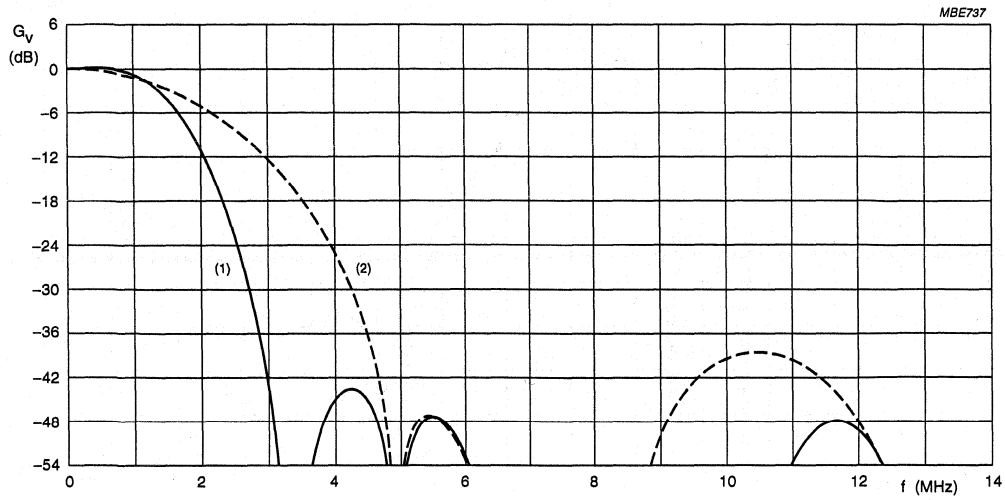
Slave Transmitter

Table 33 Slave Transmitter (slave address 89H or 8DH)

REGISTER FUNCTION	SUBADDRESS	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
Status byte	–	VER2	VER1	VER0	CCRDO	CCRDE	FSQ2	FSQ1	FSQ0

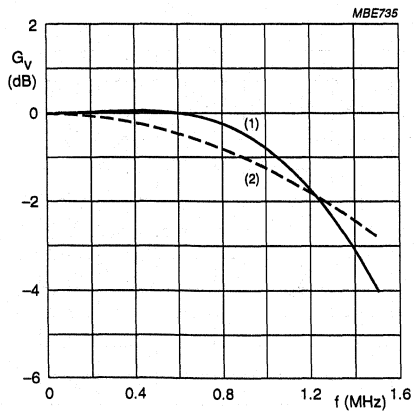
Table 34 No subaddress

DATA BYTE	DESCRIPTION
VER	Version identification of the device. It will be changed with all versions of the IC that have different programming models. Current version is 100 binary.
CCRDO	1 = closed caption bytes of the odd field have been encoded. 0 = the bit is reset after information has been written to the subaddresses 67 and 68. It is set immediately after the data have been encoded.
CCRDE	1 = closed caption bytes of the even field have been encoded. 0 = the bit is reset after information has been written to the subaddresses 69 and 6A. It is set immediately after the data have been encoded.
FSQ	State of the internal field sequence counter. Bit 0 (FSQ0) gives the odd/even information; odd = LOW, even = HIGH.



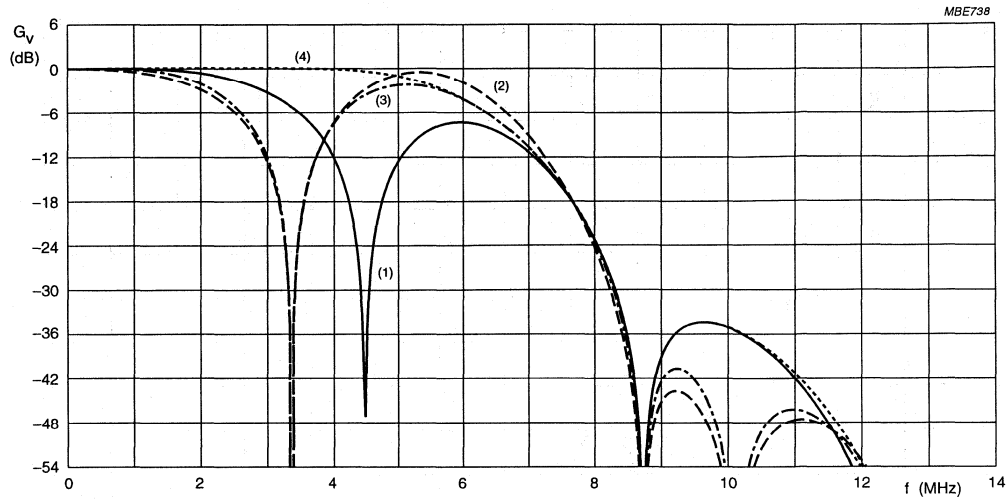
(1) SCBW = 1.
(2) SCBW = 0.

Fig.3 Chrominance transfer characteristic 1.



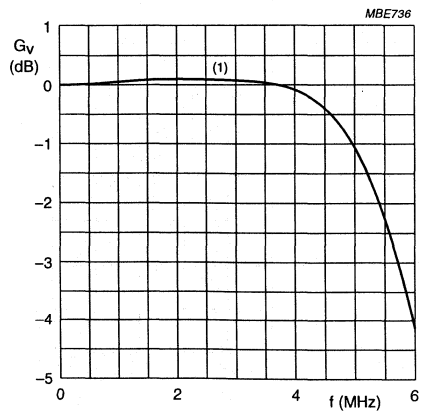
(1) SCBW = 1.
(2) SCBW = 0.

Fig.4 Chrominance transfer characteristic 2.



(1) CCRS1 = 0; CCRS0 = 1.
(2) CCRS1 = 1; CCRS0 = 0.
(3) CCRS1 = 1; CCRS0 = 1.
(4) CCRS1 = 0; CCRS0 = 0.

Fig.5 Luminance transfer characteristic 1.



CCRS1 = 0; CCRS0 = 0.

Fig.6 Luminance transfer characteristic 2.

CHARACTERISTICS

V_{DDD} = 4.5 to 5.5 V; T_{amb} = 0 to 70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Supply					
V_{DDD}	digital supply voltage		4.5	5.5	V
V_{DDA}	analog supply voltage		4.75	5.25	V
I_{DDD}	digital supply current	note 1	–	170	mA
I_{DDA}	analog supply current	note 1	–	55	mA
Inputs					
V_{IL}	LOW level input voltage (except SDA, SCL, AP, SP and XTALI)		−0.5	+0.8	V
V_{IH}	HIGH level input voltage (except LLC, SDA, SCL, AP, SP and XTALI)		2.0	V_{DDD} + 0.5	V
	HIGH level input voltage (LLC)		2.4	V_{DDD} + 0.5	V
I_{LI}	input leakage current		–	1	µA
C_I	input capacitance	clocks operating	–	10	pF
		data available	–	8	pF
		I/Os at high impedance	–	8	pF
Outputs					
V_{OL}	LOW level output voltage (except SDA and XTALO)	note 2	0	0.6	V
V_{OH}	HIGH level output voltage (except LLC, SDA, $\overline{DTACK}$ and XTALO)	note 2	2.4	V_{DDD} + 0.5	V
	HIGH level output voltage (LLC)	note 2	2.6	V_{DDD} + 0.5	V
I²C-bus; SDA and SCL					
V_{IL}	LOW level input voltage		−0.5	+1.5	V
V_{IH}	HIGH level input voltage		3.0	V_{DDD} + 0.5	V
I_I	input current	V_I = LOW or HIGH	−10	+10	µA
V_{OL}	LOW level output voltage (SDA)	I_{OL} = 3 mA	–	0.4	V
I_O	output current	during acknowledge	3	–	mA
Clock timing (LLC)					
T_{LLC}	cycle time	note 3	34	41	ns
δ	duty factor t_{HIGH}/T_{LLC}	note 4	40	60	%
t_r	rise time	note 3	–	5	ns
t_f	fall time	note 3	–	6	ns
Input timing					
t_{SU}	input data set-up time (any other except SEL_MPU, CDIR, $\overline{RW}$/SCL, A0/SDA, $\overline{CS}$/SA, $\overline{RES}$, AP and SP)		6	–	ns
t_{HD}	input data hold time (any other except SEL_MPU, CDIR, $\overline{RW}$/SCL, A0/SDA, $\overline{CS}$/SA, $\overline{RES}$, AP and SP)		3	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Crystal oscillator					
f_n	nominal frequency (usually 27 MHz)	3rd harmonic	–	30	MHz
$\Delta f/f_n$	permissible deviation of nominal frequency	note 5	–50	+50	10^{-6}
CRYSTAL SPECIFICATION					
T_{amb}	operating ambient temperature		0	70	°C
C_L	load capacitance		8	–	pF
R_S	series resistance		–	80	Ω
C_1	motional capacitance (typical)		1.5 –20%	1.5 +20%	fF
C_0	parallel capacitance (typical)		3.5 –20%	3.5 +20%	pF
MPU interface timing					
t_{AS}	address set-up time	note 6	9	–	ns
t_{AH}	address hold time		0	–	ns
$t_{R\overline{W}S}$	read/write set-up time	note 6	9	–	ns
$t_{R\overline{W}H}$	read/write hold time		0	–	ns
t_{DD}	data bus floating from $\overline{CS}$ (read)	notes 7, 8 and 9	75	142	ns
t_{DF}	data valid from $\overline{CS}$ (read)	notes 7 and 8	38	105	ns
t_{DS}	data bus set-up time (write)	note 6	9	–	ns
t_{DH}	data bus hold time (write)	note 6	9	–	ns
t_{ACS}	acknowledge delay from $\overline{CS}$	notes 7 and 8	112	180	ns
$t_{\overline{CS}D}$	$\overline{CS}$ HIGH from acknowledge		0	–	ns
t_{DAT}	$\overline{DTACK}$ floating from $\overline{CS}$ HIGH	notes 7 and 8; n = 7	75	142	ns
Data and reference signal output timing					
C_L	output load capacitance		7.5	40	pF
t_{OH}	output hold time		4	–	ns
t_{OD}	output delay time	CREF in output mode	–	25	ns
Chroma, Y and CVBS outputs					
$V_{o(p-p)}$	output signal voltage (peak-to-peak value)	note 10	1.9	2.1	V
R_I	internal series resistance		18	35	Ω
R_L	output load resistance		80	–	Ω
B	output signal bandwidth of DACs	–3 dB	10	–	MHz
ILE	LF integral linearity error of DACs		–	±2	LSB
DLE	LF differential linearity error of DACs		–	±1	LSB

Notes to the Characteristics

1. At maximum supply voltage with highly active input signals.
2. The levels have to be measured with load circuits of 1.2 kΩ to 3.0 V (standard TTL load) and C_L = 25 pF.
3. The data is for both input and output direction.
4. With LLC in input mode. In output mode, with a crystal connected to XTALO/XTALI duty factor is typically 50%.
5. If an internal oscillator is used, crystal deviation of nominal frequency is directly proportional to the deviation of subcarrier frequency and line/field frequency.
6. The value is calculated via equation $t = t_{SU} + t_{HD}$
7. The value depends on the clock frequency. The numbers given are calculated with f_{LLC} = 27 MHz.
8. The values given are calculated via equation $t_{dmax} = t_{OD} + n \times t_{LLC} + t_{LLC} + t_{SU}$ and $t_{dmin} = t_{OH} + n \times t_{LLC} + t_{LLC} - t_{HD}$
9. The falling edge of $\overline{DTACK}$ will always occur 1 × LLC after data is valid.
10. For full digital range, without load, V_{DDA} = 5.0 V. The typical voltage swing is 2.0 V, the typical minimum output voltage (digital zero at DAC) is 0.2 V.

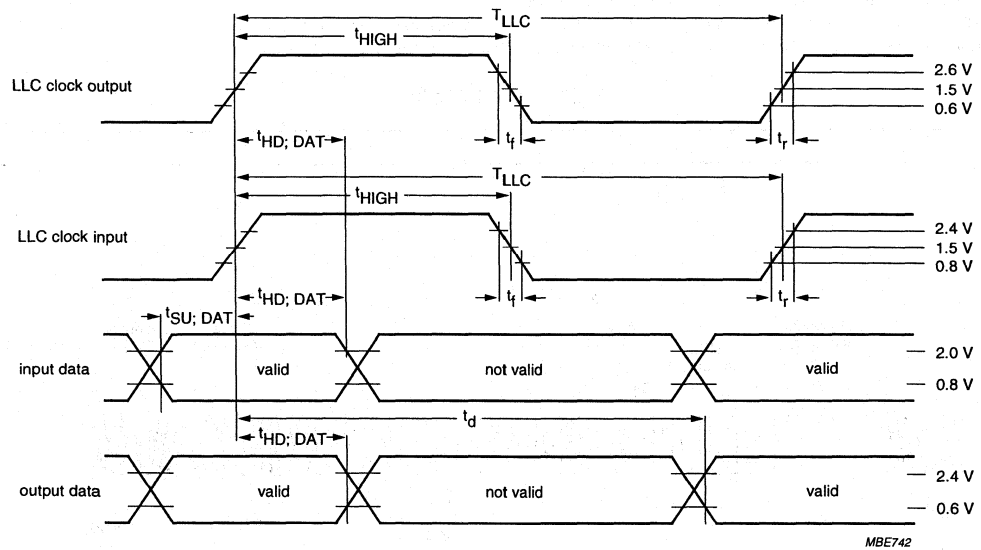
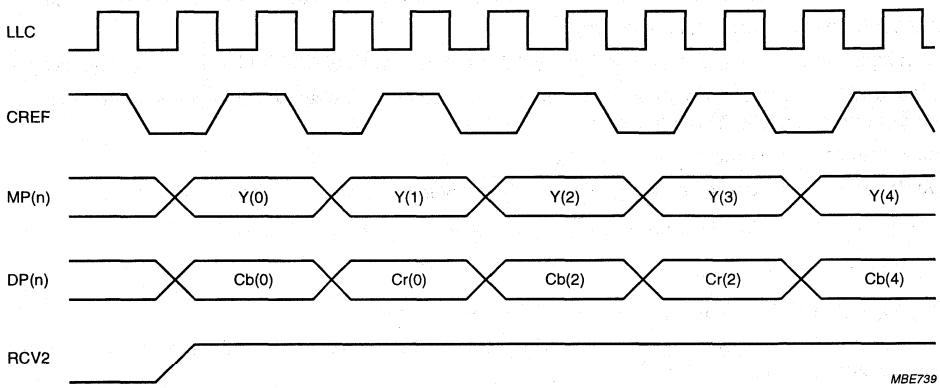
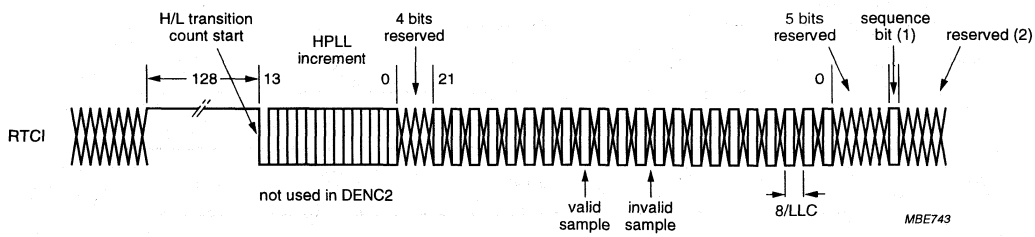


Fig.7 Clock data timing.



The data demultiplexing phase is coupled to the internal horizontal phase.
The CREF signal applies only for the 16 lines digital TV format, because these signals are only valid in 13.5 MHz.
The phase of the RCV2 signal is programmed to tbf (tbf for 50 Hz) in this example in output mode (BRCV2).

Fig.8 Digital TV timing.



(1) Sequence bit:
PAL = logic 0 then (R – Y) line normal; PAL = logic 1 then (R – Y) line inverted.
NTSC = logic 0 then no change.
(2) Reserved bits: 235 with 50 Hz systems; 232 with 60 Hz systems.
(3) Only from SAA7111 decoder.
(4) SAA7111 provides (22:0) bits, resulting in 3 reserved bits before sequence bit.

Fig.9 RTCI timing.

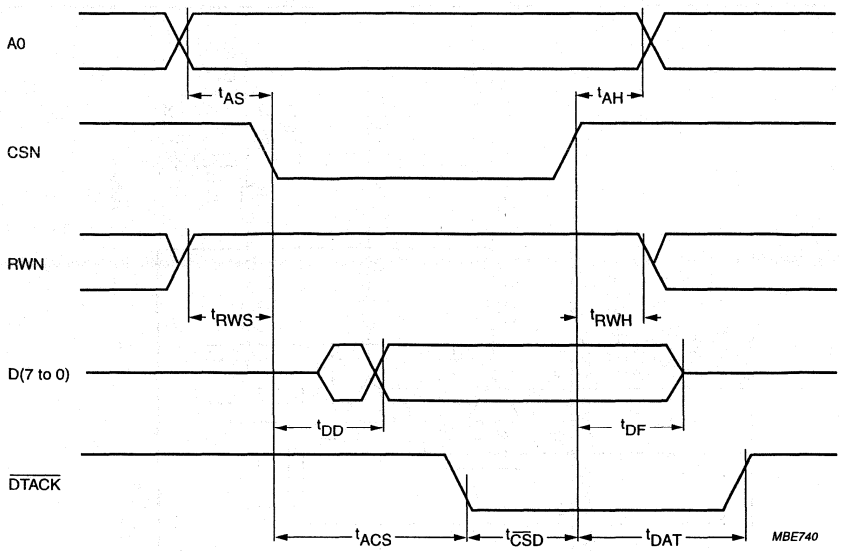


Fig.10 MPU interface timing (READ cycle).

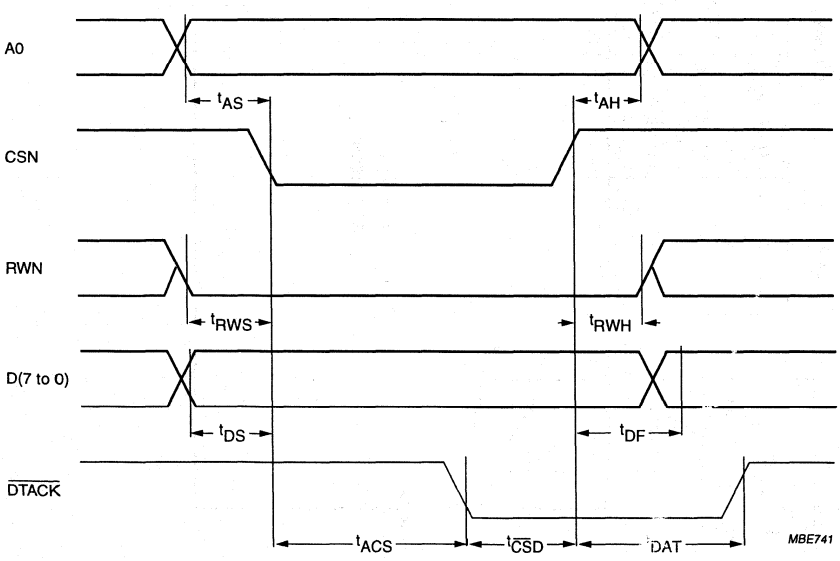


Fig.11 MPU interface timing (WRITE cycle).

APPLICATION INFORMATION

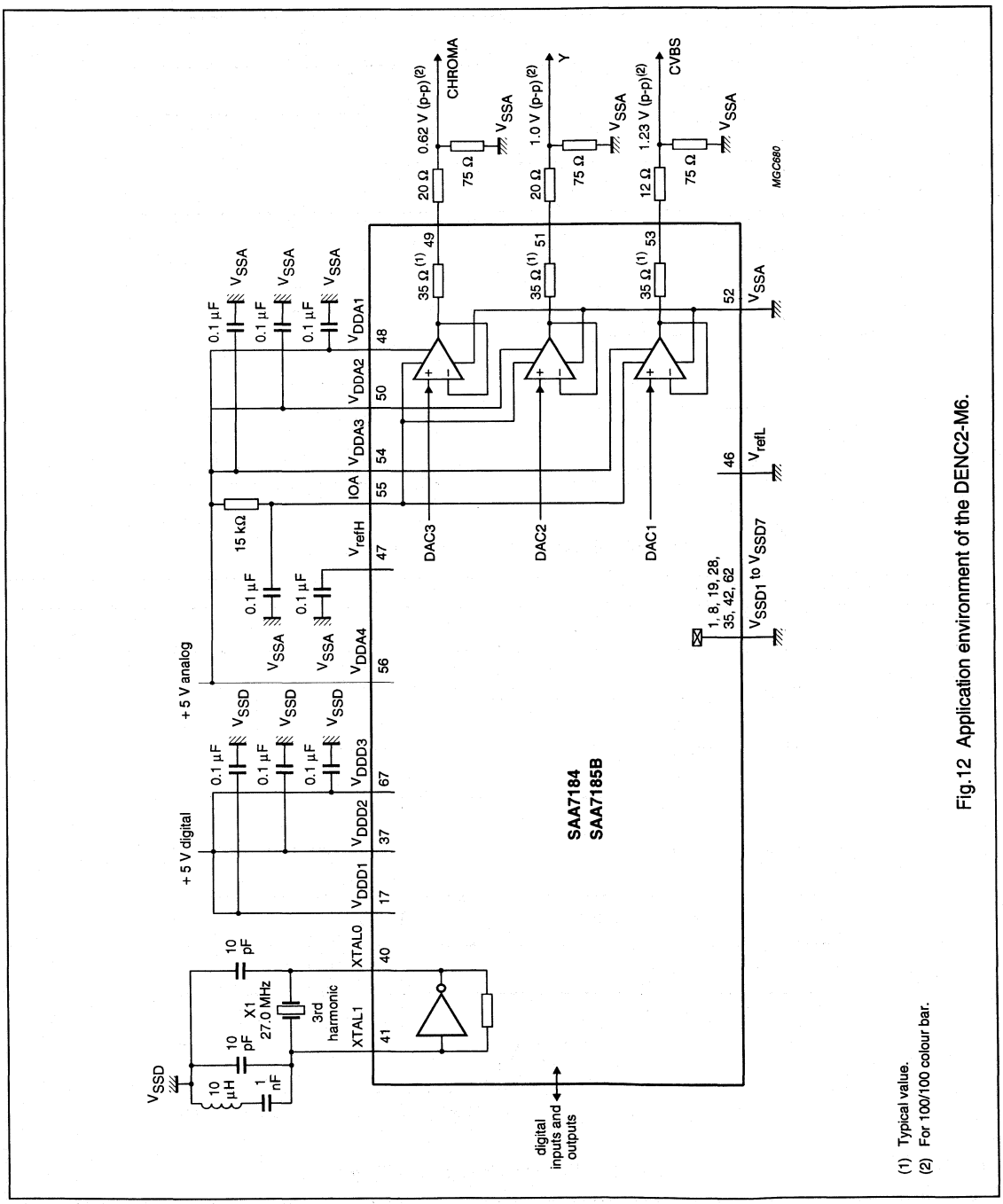


Fig.12 Application environment of the DENC2-M6.

(1) Typical value.
(2) For 100/100 colour bar.

Digital Video Encoder (DENC2) SAA7185

FEATURES

- CMOS 5 V device
- Digital PAL/NTSC encoder
- System pixel frequency 13.5 MHz
- Accepts MPEG decoded data
- 8-bit wide MPEG port
- Input data format Cb, Y, Cr etc. (CCIR 656)
- 16-bit wide YUV input port
- I²C-bus control or alternatively MPU parallel control port
- Encoder can be master or slave
- Programmable horizontal and vertical input synchronization phase
- Programmable horizontal sync output phase
- OSD overlay with Look-Up Tables (LUTs) 8 × 3 bytes
- Colour bar generator
- Line 21 Closed Caption encoder
- Cross-colour reduction
- DACs operating at 27 MHz with 10-bit resolution
- Controlled rise/fall times of output syncs and blanking
- Down-mode of DACs
- CVBS and S-Video output simultaneously
- PLCC68 package.

GENERAL DESCRIPTION

The SAA7185 encodes digital YUV video data to an NTSC, PAL CVBS or S-Video signal.

The circuit accepts CCIR compatible YUV data with 720 active pixels per line in 4 : 2 : 2 multiplexed formats, for example MPEG decoded data. It includes a sync/clock generator and on-chip Digital-to-Analog Converters (DACs).

The circuit is compatible to the DIG-TV2 chip family.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage	4.75	5.0	5.25	V
V_{DDD}	digital supply voltage	4.5	5.0	5.5	V
I_{DDA}	analog supply current	–	50	55	mA
I_{DDD}	digital supply current	–	140	170	mA
V_i	input signal voltage levels	TTL compatible			
$V_{o(p-p)}$	analog output signal voltages Y, C and CVBS without load (peak-to-peak value)	–	2	–	V
R_L	load resistance	80	–	–	Ω
ILE	LF integral linearity error	–	–	±2	LSB
DLE	LF differential linearity error	–	–	±1	LSB
T_{amb}	operating ambient temperature	0	–	+70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7185WP	PLCC68	plastic leaded chip carrier; 68 leads	SOT188-2

BLOCK DIAGRAM

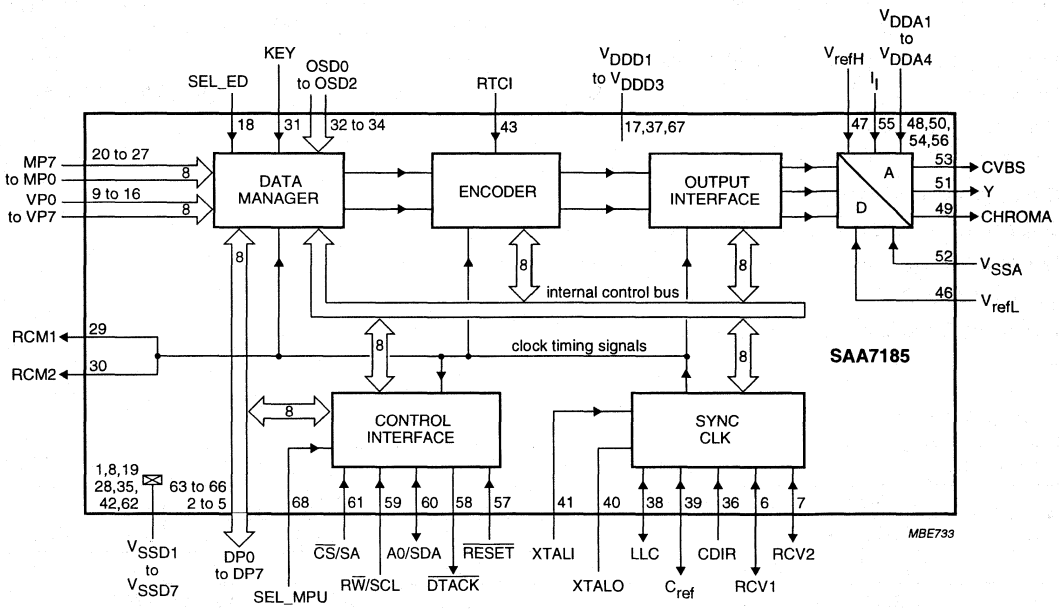


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{SSD1}	1	digital ground 1
DP4	2	Upper 4 bits of the Data Port. If pin 68 (SEL_MPU) is HIGH, this is the data bus of the parallel MPU interface. If it is LOW, they are the UV lines of the Video Port.
DP5	3	
DP6	4	
DP7	5	
RCV1	6	Raster Control 1 for Video port. Depending on the synchronization mode, this pin receives/provides a VS/FS/FSEQ signal.
RCV2	7	Raster Control 2 for Video port. Depending on the synchronization mode, this pin receives/provides an HS/HREF/CBL signal.
V_{SSD2}	8	digital ground 2
VP0	9	Video Port. This is an input for CCIR 656 compatible, multiplexed video data. If the 16-bit DIG-TV2 format is used, this is the Y data.
VP1	10	
VP2	11	
VP3	12	
VP4	13	
VP5	14	
VP6	15	
VP7	16	
V_{DDD1}	17	digital supply voltage 1
SEL_ED	18	Select Encoder Data. Selects data either from MPEG port or from video port as encoder input.
V_{SSD3}	19	digital ground 3
MP7	20	MPEG Port. It is an input for CCIR 656 style multiplexed YUV data.
MP6	21	
MP5	22	
MP4	23	
MP3	24	
MP2	25	
MP1	26	
MP0	27	
V_{SSD4}	28	digital ground 4
RCM1	29	Raster Control 1 for MPEG port. This pin provides a VS/FS/FSEQ signal.
RCM2	30	Raster Control 2 for MPEG port. This pin provides an HS pulse for the MPEG decoder.
KEY	31	Key signal for OSD. It is active HIGH.
OSD0	32	On-Screen Display data. This is the index for the internal OSD look-up table.
OSD1	33	
OSD2	34	
V_{SSD5}	35	digital ground 5
CDIR	36	Clock direction. If the CDIR input is HIGH, the circuit receives a clock signal, otherwise LLC and CREF are generated by the internal crystal oscillator.
V_{DDD2}	37	digital supply voltage 2

SYMBOL	PIN	DESCRIPTION
LLC	38	Line-Locked Clock. This is the 27 MHz master clock for the encoder. The direction is set by the CDIR pin.
C_{ref}	39	Clock Reference signal. This is the clock qualifier for DIG-TV2 compatible signals.
XTALO	40	Crystal oscillator output (to crystal).
XTALI	41	Crystal oscillator input (from crystal). If the oscillator is not used, this pin should br connected to ground.
V_{SSD6}	42	digital ground 6
RTCI	43	Real Time Control Input. If the clock is provided by an SAA7151B, RTCI should be connected to the RTCO pin of the decoder to improve the signal quality.
AP	44	Test pin. Connect to digital ground for normal operation.
SP	45	Test pin. Connect to digital ground for normal operation.
V_{refL}	46	Lower reference voltage input for the DACs.
V_{refH}	47	Upper reference voltage input for the DACs.
V_{DDA1}	48	Analog positive supply voltage 1 for the DACs and output amplifiers.
CHROMA	49	Analog output of the chrominance signal.
V_{DDA2}	50	Analog supply voltage 2 for the DACs and output amplifiers.
Y	51	Analog output of the luminance signal.
V_{SSA}	52	Analog ground for the DACs and output amplifiers.
CVBS	53	Analog output of the CVBS signal.
V_{DDA3}	54	Analog supply voltage 3 for the DACs and output amplifiers.
I_I	55	Current input for the output amplifiers, connect via a 15 kΩ resistor to V_{DDA}.
V_{DDA4}	56	Analog supply voltage 4 for the DACs and output amplifiers.
$\overline{RESET}$	57	Reset input, active LOW. After reset is applied, all outputs are in 3-state input mode. The I²C-bus receiver waits for the start condition.
$\overline{DTACK}$	58	Data acknowledge output of the parallel MPU interface, active LOW, otherwise high impedance.
$R\overline{W}$/SCL	59	If pin 68 (SEL_MPU) is HIGH, this is the read/write signal of the parallel MPU interface, otherwise it is the I²C-bus serial clock input.
A0/SDA	60	If pin 68 (SEL_MPU) is HIGH, this is the address signal of the parallel MPU interface, otherwise it is the I²C-bus serial data input/output.
$\overline{CS}$/SA	61	If pin 68 (SEL_MPU) is HIGH, this is the chip select signal of the parallel MPU interface, otherwise it is the I²C-bus slave address select pin. LOW: slave address = 88H, HIGH = 8CH.
V_{SSD7}	62	digital ground 7
DP0	63	Lower 4 bits of the Data Port. If pin 68 (SEL_MPU) is HIGH, this is the data bus of the parallel MPU interface. If it is LOW, they are the UV lines of the Video Port.
DP1	64	
DP2	65	
DP3	66	
V_{DDD3}	67	digital supply voltage 3
SEL_MPU	68	Select MPU interface input. If it is HIGH, the parallel MPU interface is active, otherwise the I²C-bus interface will be used.

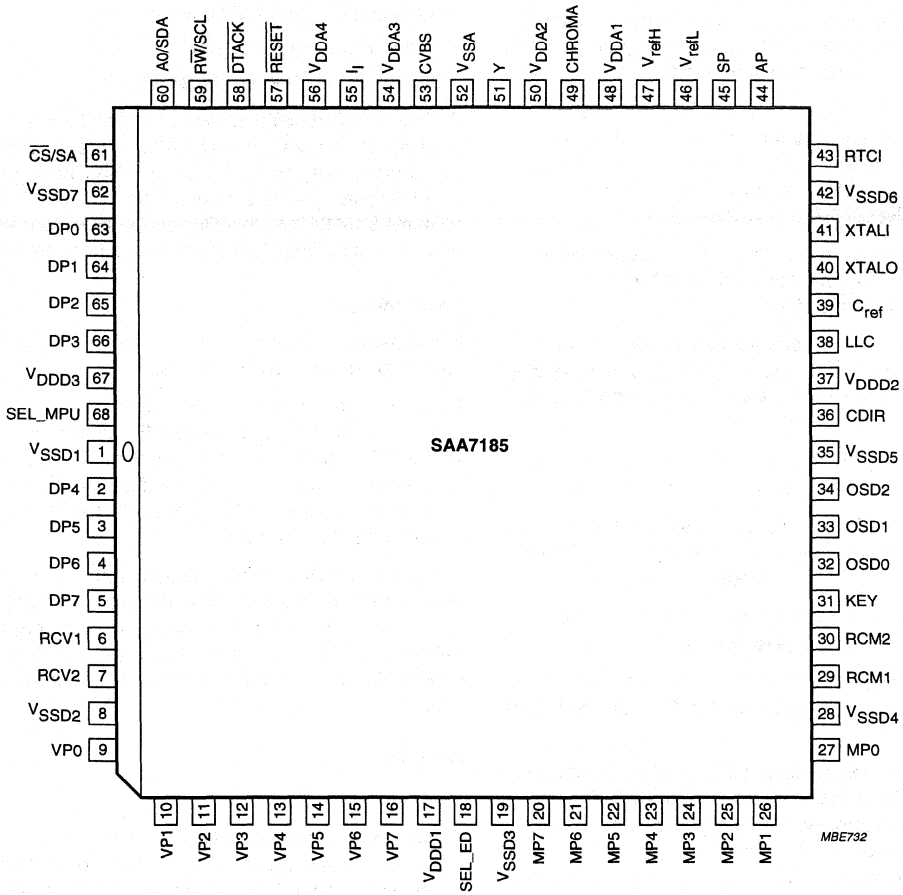


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The digital MPEG-compatible Video Encoder (DENC2) encodes digital luminance and chrominance into analog CVBS and simultaneously S-Video (Y/C) signals. NTSC-M and PAL B/G standards also sub-standards are supported.

The basic encoder function consists of subcarrier generation and colour modulation also insertion of synchronization signals. Luminance and chrominance signals are filtered in accordance with the standard requirements RS-170-A and CCIR 624.

For ease of analog post filtering the signals are twice oversampled with respect to pixel clock before digital-to-analog conversion.

For total filter transfer characteristics see Figs 3, 4, 5 and 6. The DACs are realized with full 10-bit resolution. The encoder provides three 8-bit wide data ports, that serve different applications.

The MPEG Port (MP) and the Video Port (VP) accept 8 lines multiplexed Cb-Y-Cr data.

The Video Port (VP) is also able to handle DIG-TV2 family compatible 16-bit YUV signals. In this event, the Data Port (DP) is used for the U/V components.

The Data Port can handle the data of an 8-bit wide microprocessor interface, alternatively.

The 8-bit multiplexed Cb-Y-Cr formats are CCIR 656 (D1 format) compatible, but the SAV, EAV etc. codes are not decoded.

A crystal-stable master clock (LLC) of 27 MHz, which is twice the CCIR line-locked pixel clock of 13.5 MHz, needs to be supplied externally. Optionally, a crystal oscillator input/output pair of pins and an on-chip clock driver is provided. Additionally, a DMSD2 compatible clock interface, using C_{ref} (input or output) and RTC (see *"data sheet SAA7151B"*) is available.

The DENC2 synthesizes all necessary internal signals, colour subcarrier frequency, and synchronization signals, from that clock. DENC2 is always timing master for the MPEG Port (MP), but it can additionally be configured as master or slave for the Video Port (VP).

The IC also contains Closed Caption and Extended Data Services Encoding (Line 21); it also supports OSD via KEY and three-bit overlay techniques by a 24 × 8 LUT.

The IC can be programmed via I²C-bus or 8-bit MPU interface, but only one interface configuration can be active at a time; if the 16-bit Video Port mode (VP and DP) is being used, only the I²C-bus interface can be selected.

A number of possibilities are provided for setting of different video parameters such as:

- black and blanking level control
- colour subcarrier frequency
- black variable burst amplitude etc.

During reset ($\overline{RESET}$ = LOW) and after reset is released, all digital I/O stages are set to input mode. A reset forces the control interfaces to abort any running bus transfer and to set Register 3AH to contents 13H, Register 61H to contents 0X010101b, and Register 6CH to contents 00H. All other control registers are not influenced by a reset.

Data manager

In the Data manager, real time arbitration on the data stream to be encoded is performed.

Depending on hardware conditions (signals on pins SEL_ED, KEY, OSD2 to OSD0, MP7 to to MP0, VP7 to VP0 and DP7 to DP0) and different software programming either data from the MP port, from the VP port, or from the OSD port are selected to be encoded to CVBS and Y/C signals.

Optionally, the OSD colour look-up tables located in this block, can be read out in a pre-defined sequence (8 steps per active video line), achieving e.g. a colour bar test pattern generator without need for an external data source. The colour bar function is only under software control.

Encoder

VIDEO PATH

The encoder generates out of Y, U and V baseband signals luminance and colour subcarrier output signals, suitable for use as CVBS or separate Y/C signals.

Luminance is modified in gain and in offset (latter programmable in a certain range to enable different black level set-ups). After having been inserted a fixed synchronization level, in accordance with standard composite synchronization schemes, a variable blanking level, programmable also in a certain range, is inserted.

In order to enable easy analog post filtering, luminance is interpolated from 13.5 MHz data rate to 27 MHz data rate, providing luminance in 10-bit resolution. This filter is also used to define smoothed transients for synchronization pulses and blanking period. For transfer characteristic of the luminance interpolation filter see Figs 5 and 6.

Chrominance is modified in gain (programmable separately for U and V), standard dependent burst is inserted, before baseband colour signals are interpolated from 6.75 MHz data rate to 27 MHz data rate. One of the interpolation stages can be bypassed, thus providing a higher colour bandwidth, which can be made use of for Y/C output. For transfer characteristics of the chrominance interpolation filter see Figs 3 and 4.

The amplitude of inserted burst is programmable in a certain range, suitable for standard signals and for special effects. Behind the succeeding quadrature modulator, colour in 10-bit resolution is provided on subcarrier.

The numeric ratio between Y and C outputs is in accordance with set standards.

Closed Caption Encoder

Using this circuit, data in accordance with the specification of Closed Caption or Extended Data Service, delivered by the control interface, can be encoded (Line 21). Two dedicated pairs of bytes (two bytes per field), each pair preceded by run-in clocks and framing code, are possible.

The actual line number where data is to be encoded in, can be modified in a certain range.

Data clock frequency is in accordance with definition for NTSC-M standard 32 times horizontal line frequency.

Data LOW at the output of the DACs corresponds to 0 IRE, data HIGH at the output of the DACs corresponds to approximately 50 Ω.

It is also possible to encode Closed Caption Data for 50 Hz field frequencies at 32 times horizontal line frequency.

Output Interface

In the output interface encoded Y and C signals are converted from digital-to-analog in 10-bit resolution both Y and C signals are combined to a 10-bit CVBS signal, also; in front of the summation point, the luminance signal can optionally be fed through a further filter stage, suppressing components in the range of subcarrier frequency. Thus, a type of Cross Colour reduction is provided, which is useful in a standard TV set with CVBS input.

Slopes of synchronization pulses are not affected with any Cross Colour reduction active.

Three different filter characteristics or bypass are available, see Fig.5.

The CVBS output occurs with the same processing delay as the Y and C outputs. Absolute amplitudes at the input of the DAC for CVBS is reduced by $^{15}/_{16}$ with respect to Y and C DACs to make maximum use of conversion ranges.

Outputs of all DACs can be set together via software control to minimum output voltage for either purpose.

Synchronization

The synchronization of the DENC2 is able to operate in two modes; slave mode and master mode.

In the slave mode, the circuit accepts synchronization pulses at the bidirectional RCV1 port. The timing and trigger behaviour related to the video signal on VP (and DP, if used) can be influenced by programming the polarity and on-chip delay of RCV1. Active slope of RCV1 defines the vertical phase and optionally the odd/even and colour frame phase to be initialized, it can be also used to set the horizontal phase.

If the horizontal phase is not be influenced by RCV1, a horizontal pulse needs to be supplied at the RCV2 pin. Timing and trigger behaviour can also be influenced for RCV2.

If there are missing pulses at RCV1 and/or RCV2, the time base of DENC2 runs free, thus an arbitrary number of synchronization slopes may miss, but no additional pulses (such with wrong phase) must occur.

If the vertical and horizontal phase is derived from RCV1, RCV2 can be used for horizontal or composite blanking input or output.

In the master mode, the time base of the circuit continuously runs free. On the RCV1 port, the IC can output:

- A Vertical Sync signal (VS) with 3 or 2.5 lines duration, or
- An ODD/EVEN signal which is LOW in odd fields, or
- A field sequence signal (FSEQ) which is HIGH in the first of 4 respectively 8 fields.

On the RCV2 port, the IC can provide a horizontal pulse with programmable start and stop phase; this pulse can be inhibited in the vertical blanking period to build up e.g. a composite blanking signal.

The phase of the pulses output on RCV1 or RCV2 are referenced to the VP port, polarity of both signals is selectable.

The DENC2 is **always** the timing master for the source at the MP input. The IC provides two signals for synchronizing this source:

On the RCM1 port the same signals as on RCV1 (as output) are available; on RCM2 the IC provides a horizontal pulse with programmable start and stop phase.

The length of a field also start and end of its active part can be programmed. The active part of a field always starts at the beginning of a line.

Control interface

DENC2 contains two control interfaces: an I²C-bus slave transceiver and 8-bit parallel microprocessor interface. The interfaces cannot be used simultaneously.

The I²C-bus interface is a standard slave transceiver, supporting 7-bit slave addresses and 100 kbits/s guaranteed transfer rate. It uses 8-bit subaddressing with an auto-increment function. All registers are write only, except one readable status byte.

Two I²C-bus slave addresses can be selected (pin SEL_MPU must be LOW):

88H: LOW at pin 61

8CH: HIGH at pin 61.

The parallel interface is defined by:

D7 to D0 data bus

$\overline{CS}$ active-LOW chip select signal

R$\overline{W}$ read/not write signal, LOW for a write cycle

$\overline{DTACK}$ 680xx style data acknowledge (handshake), active-LOW

A0 register select, LOW selects address, HIGH selects data.

The parallel interface uses two registers, one auto-incremental containing the current address of a control register (equals subaddress with I²C-bus control), one containing actual data. The currently addressed register is mapped to the corresponding control register.

The status byte can be read optionally via a read access to the address register, no other read access is provided.

Input levels and formats

DENC2 expects digital YUV data with levels (digital codes) in accordance with CCIR 601.

Deviating amplitudes of the colour difference signals can be compensated by independent gain control setting, while gain for luminance is set to predefined values, distinguishable for 7.5 IRE set-up or without set-up.

The MPEG port accepts only 8-bit multiplexed CCIR 656 compatible data.

If the I²C-bus interface is used, the VP port can handle both formats, 8-bit multiplexed Cb-Y-Cr data on the VP lines, or the 16-bit DTV2 format with the Y signal on the VP lines and the UV signal on the DP port.

Reference levels are measured with a colour bar, 100% white, 100% amplitude and 100% saturation.

Table 1 CCIR signal component levels

SIGNAL	IRE	DIGITAL LEVEL	CODE
Y	0	16	straight binary
	50	126	
	100	235	
Cb	bottom peak	16	straight binary
	colourless	128	
	top peak	240	
Cr	bottom peak	16	straight binary
	colourless	128	
	top peak	240	

Table 2 8-bit multiplexed format (similar to CCIR 656)

TIME	0	1	2	2	4	5	6	7
Sample	Cb_0	Y_0	Cr_0	Y_1	Cb_2	Y_2	Cr_2	Y_3
Luminance pixel number	0		1		2		3	
Colour pixel number	0				2			

Table 3 16-bit multiplexed format (DTV2 format)

TIME	0	1	2	3	4	5	6	7
Sample Y line	Y_0		Y_1		Y_2		Y_3	
Sample UV line	Cb_0		Cr_0		Cb_2		Cr_2	
Luminance pixel number	0		1		2		3	
Colour pixel number	0				2			

Bit allocation map

Table 4 Slave Receiver (Slave Address 88H or 8CH)

REGISTER FUNCTION	SUB ADDRESS	DATA BYTE (note 1)							
		D7	D6	D5	D4	D3	D2	D1	D0
Null	00	0	0	0	0	0	0	0	0
	↓	↓							
Null	39	0	0	0	0	0	0	0	0
Input port control	3A	CBENB	0	0	V656	VY2C	VUV2C	MY2C	MUV2C
OSD LUT Y0	42	OSDY07	OSDY06	OSDY05	OSDY04	OSDY03	OSDY02	OSDY01	OSDY00
OSD LUT U0	43	OSDU07	OSDU06	OSDU05	OSDU04	OSDU03	OSDU02	OSDU01	OSDU00
OSD LUT V0	44	OSDV07	OSDV06	OSDV05	OSDV04	OSDV03	OSDV02	OSDV01	OSDV00
	↓	↓							
OSD LUT Y7	57	OSDY77	OSDY76	OSDY75	OSDY74	OSDY73	OSDY72	OSDY71	OSDY70
OSD LUT U7	58	OSDU77	OSDU76	OSDU75	OSDU74	OSDU73	OSDU72	OSDU71	OSDU70
OSD LUT V7	59	OSDV77	OSDV76	OSDV75	OSDV74	OSDV73	OSDV72	OSDV71	OSDV70
Chrominance phase	5A	CHPS7	CHPS6	CHPS5	CHPS4	CHPS3	CHPS2	CHPS1	CHPS0
Gain U	5B	GAINU7	GAINU6	GAINU5	GAINU4	GAINU3	GAINU2	GAINU1	GAINU0
Gain V	5C	GAINV7	GAINV6	GAINV5	GAINV4	GAINV3	GAINV2	GAINV1	GAINV0
Gain U MSB, black level	5D	GAINU8	0	BLCKL5	BLCKL4	BLCKL3	BLCKL2	BLCKL1	BLCKL0
Gain V MSB, blanking level	5E	GAINV8	0	BLNNL5	BLNNL4	BLNNL3	BLNNL2	BLNNL1	BLNNL0
Null	5F	0	0	0	0	0	0	0	0
Cross-colour select	60	CCRS1	CCRS0	0	0	0	0	0	0
Standard control	61	0	DOWN	INPI1	YGS	RTCE	SCBW	PAL	FISE
Burst amplitude	62	SQP	BSTA6	BSTA5	BSTA4	BSTA3	BSTA2	BSTA1	BSTA0
Subcarrier 0	63	FSC07	FSC06	FSC05	FSC04	FSC03	FSC02	FSC01	FSC00
Subcarrier 1	64	FSC15	FSC14	FSC13	FSC12	FSC11	FSC10	FSC09	FSC08
Subcarrier 2	65	FSC23	FSC22	FSC21	FSC20	FSC19	FSC18	FSC17	FSC16
Subcarrier 3	66	FSC31	FSC30	FSC29	FSC28	FSC27	FSC26	FSC25	FSC24
Line 21 odd 0	67	L21O07	L21O06	L21O05	L21O04	L21O03	L21O02	L21O01	L21O00
Line 21 odd 1	68	L21O17	L21O16	L21O15	L21O14	L21O13	L21O12	L21O11	L21O10
Line 21 even 0	69	L21E07	L21E06	L21E05	L21E04	L21E03	L21E02	L21E01	L21E00
Line 21 even 1	6A	L21E17	L21E16	L21E15	L21E14	L21E13	L21E12	L21E11	L21E10
Encoder control, CC line	6B	MODIN1	MODIN0	0	SCCLN4	SCCLN3	SCCLN2	SCCLN1	SCCLN0

REGISTER FUNCTION	SUB ADDRESS	DATA BYTE (note 1)							
		D7	D6	D5	D4	D3	D2	D1	D0
RCV port control	6C	SRCV11	SRCV10	TRCV2	ORCV1	PRCV1	CBLF	ORCV2	PRCV2
RCM, CC mode	6D	0	0	0	0	SRCM11	SRCM10	CCEN1	CCEN0
Horizontal trigger	6E	HTRIG7	HTRIG6	HTRIG5	HTRIG4	HTRIG3	HTRIG2	HTRIG1	HTRIG0
Horizontal trigger	6F	0	0	0	0	0	HTRIG10	HTRIG09	HTRIG08
f_{sc} reset mode, Vertical trigger	70	PHRES1	PHRES0	SBLBN	VTRIG4	VTRIG3	VTRIG2	VTRIG1	VTRIG0
Begin MP request	71	BMRQ7	BMRQ6	BMRQ5	BMRQ4	BMRQ3	BMRQ2	BMRQ1	BMRQ0
End MP request	72	EMRQ7	EMRQ6	EMRQ5	EMRQ4	EMRQ3	EMRQ2	EMRQ1	EMRQ0
MSBs MP request	73	0	EMRQ10	EMRQ09	EMRQ08	0	BMRQ10	BMRQ09	BMRQ08
Null	74	0	0	0	0	0	0	0	0
Null	75	0	0	0	0	0	0	0	0
Null	76	0	0	0	0	0	0	0	0
Begin RCV2 output	77	BRCV7	BRCV6	BRCV5	BRCV4	BRCV3	BRCV2	BRCV1	BRCV0
End RCV2 output	78	ERCV7	ERCV6	ERCV5	ERCV4	ERCV3	ERCV2	ERCV1	ERCV0
MSBs RCV2 output	79	0	ERCV10	ERCV09	ERCV08	0	BRCV10	BRCV09	BRCV08
Field length	7A	FLEN7	FLEN6	FLEN5	FLEN4	FLEN3	FLEN2	FLEN1	FLEN0
First active line	7B	FAL7	FAL6	FAL5	FAL4	FAL3	FAL2	FAL1	FAL0
Last active line	7C	LAL7	LAL6	LAL5	LAL4	LAL3	LAL2	LAL1	LAL0
MSBs field control	7D	0	0	LAL8	FAL8	0	0	FLEN9	FLEN8

Note

1. All bits labelled '0' are reserved. They **must** be programmed with logic 0.

I²C-bus format

Table 5 I²C-bus address; see Table 6

S	SLAVE ADDRESS	ACK	SUBADDRESS	ACK	DATA 0	ACK	--------	DATA n	ACK	P

Table 6 Explanation of Table 5

PART	DESCRIPTION
S	START condition
Slave address	1 0 0 0 1 0 0 X or 1 0 0 0 1 1 0 X (note 1)
ACK	acknowledge, generated by the slave
Subaddress (note 2)	subaddress byte
DATA	data byte
--------	continued data bytes and ACKs
P	STOP condition

Notes

1. X is the read/write control bit; X = logic 0 is order to write; X = logic 1 is order to read, no subaddressing with read.
2. If more than 1 byte DATA is transmitted, then auto-increment of the subaddress is performed.

Slave Receiver

Table 7 Subaddress 3A

DATA BYTE	LOGIC LEVEL	DESCRIPTION
MUV2C	0	Cb/Cr data at MP are two's complement.
	1	Cb/Cr data at MP are straight binary. Default after reset.
MY2C	0	Y data at MP are two's complement.
	1	Y data at MP are straight binary. Default after reset.
VUV2C	0	Cb/Cr data input to VP or DP are two's complement. Default after reset.
	1	Cb/Cr data input to VP or DP are straight binary.
VY2C	0	Y data input to VP are two's complement. Default after reset.
	1	Y data input to VP are straight binary.
V656	0	Selects YUV 422 format on VP (8 lines Y) and DP (8 lines multiplexed Cb/Cr).
	1	Selects CCIR 656 compatible format on VP (8 lines Cb, Y, Cr). Default after reset.
CBENB	0	Data from input ports are encoded. Default after reset.
	1	Colour bar with programmable colours (entries of OSD_LUTs) is encoded. The LUTs are read in upward order from index 0 to index 7.

Table 8 Subaddress 42 to 59

COLOUR	DATA BYTE (note 1)			INDEX (note 2)
	OSDY	OSDU	OSDV	
White	107 (6BH)	0 (00H)	0 (00H)	0
	107 (6BH)	0 (00H)	0 (00H)	
Yellow	82 (52H)	144 (90H)	18 (12H)	1
	34 (22H)	172 (ACH)	14 (0Eh)	
Cyan	42 (2AH)	38 (26H)	144 (90H)	2
	03 (03H)	29 (1DH)	172 (ACH)	
Green	17 (11H)	182 (B6H)	162 (A2H)	3
	240 (F0H)	200 (C8H)	185 (B9H)	
Magenta	234 (EAH)	74 (4AH)	94 (5EH)	4
	212 (D4H)	56 (38H)	71 (47H)	
Red	209 (D1H)	218 (DAH)	112 (70H)	5
	193 (C1H)	227 (E3H)	84 (54H)	
Blue	169 (A9H)	112 (70H)	238 (EEH)	6
	163 (A3H)	84 (54H)	242 (F2H)	
Black	144 (90H)	0 (00H)	0 (00H)	7
	144 (90H)	0 (00H)	0 (00H)	

Notes

1. Contents of OSD Look-up tables. All 8 entries are 8-bits. Data representation is in accordance with CCIR 601 (Y, Cb, Cr), but two's complement, e.g. for a $^{100}/_{100}$ (upper number) or $^{100}/_{75}$ (lower number) colour bar.
2. For normal colour bar with CBENB = logic 1.

Table 9 Subaddress 5A

DATA BYTE	DESCRIPTION
CHPS	Phase of encoded colour subcarrier (including burst) relative to horizontal sync. Can be adjusted in steps of 360/256 degrees.

Table 10 Subaddress 5B and 5D

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
GAINU	variable gain for Cb signal; input representation accordance with CCIR 601	white-to-black = 92.5 IRE(1)	
		GAINU = 0	output subcarrier of U contribution = 0
		GAINU = 118 (76H)	output subcarrier of U contribution = nominal
		white-to-black = 100 IRE(2)	
		GAINU = 0	output subcarrier of U contribution = 0
		GAINU = 125 (7DH)	output subcarrier of U contribution = nominal

Notes

1. GAINU = −2.17 × nominal to +2.16 × nominal.
2. GAINU = −2.05 × nominal to +2.04 × nominal.

Table 11 Subaddress 5C and 5E

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
GAINV	variable gain for Cr signal; input representation accordance with CCIR 601	white-to-black = 92.5 IRE[1]	
		GAINV = 0	output subcarrier of V contribution = 0
		GAINV = 165 (A5H)	output subcarrier of V contribution = nominal
		white-to-black = 100 IRE[2]	
		GAINV = 0	output subcarrier of V contribution = 0
		GAINV = 175 (AFH)	output subcarrier of V contribution = nominal

Notes

1. GAINV = −1.55 × nominal to +1.55 × nominal.
2. GAINV = −1.46 × nominal to +1.46 × nominal.

Table 12 Subaddress 5D

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
BLCKL	variable black level; input representation accordance with CCIR 601	white-to-sync = 140 IRE[1]	
		BLCKL = 0	output black level = 24 IRE
		BLCKL = 63 (3FH)	output black level = 49 IRE
		white-to-sync = 143 IRE[2]	
		BLCKL = 0	output black level = 24 IRE
		BLCKL = 63 (3FH)	output black level = 50 IRE

Notes

1. Output black level/IRE = BLCKL × 25/63 + 24; recommended value: BLCKL = 60 (3CH) normal.
2. Output black level/IRE = BLCKL × 26/63 + 24; recommended value: BLCKL = 45 (2DH) normal.

Table 13 Subaddress 5E

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
BLNNL	variable blanking level	white-to-sync = 140 IRE[1]	
		BLNNL = 0	output blanking level = 17 IRE
		BLNNL = 63 (3FH)	output blanking level = 42 IRE
		white-to-sync = 143 IRE[2]	
		BLNNL = 0	output blanking level = 17 IRE
		BLNNL = 63 (3FH)	output blanking level = 43 IRE

Notes

1. Output black level/IRE = BLNNL × 25/63 + 17; recommended value: BLNNL = 58 (3AH) normal.
2. Output black level/IRE = BLNNL × 26/63 + 17; recommended value: BLNNL = 63 (3FH) normal.

Table 14 Subaddress 60 (CCRS; select cross colour reduction filter in luminance)

DATA BYTE		FUNCTION
CCRS1	CCRS0	
0	0	no cross colour reduction (for overall transfer characteristic of luminance see Fig.5)
0	1	cross colour reduction #1 active (for overall transfer characteristic see Fig.5)
1	0	cross colour reduction #2 active (for overall transfer characteristic see Fig.5)
1	1	cross colour reduction #3 active (for overall transfer characteristic see Fig.5)

Table 15 Subaddress 61

DATA BYTE	LOGIC LEVEL	DESCRIPTION
FISE	0	864 total pixel clocks per line
	1	858 total pixel clocks per line; default after reset
PAL	0	NTSC encoding (non-alternating V component); default after reset
	1	PAL encoding (alternating V component)
SCBW	0	enlarged bandwidth for chrominance encoding (for overall transfer characteristic of chrominance in baseband representation see Figs 3 and 4)
	1	standard bandwidth for chrominance encoding (for overall transfer characteristic of chrominance in baseband representation see Figs 3 and 4); default after reset
RTCE	0	no real time control of generated subcarrier frequency; default after reset
	1	real time control of generated subcarrier frequency through SAA7151B (timing see Fig.9)
YGS	0	luminance gain for white – black 100 IRE
	1	luminance gain for white – black 92.5 IRE including 7.5 IRE set-up of black; default after reset
INPI	0	PAL switch phase is nominal; default after reset
	1	PAL switch phase is inverted compared to nominal
DOWN	0	DACs in normal operational mode (not defined after reset, program after all zero-bits are set to zero)
	1	DACs forced to lowest output voltage (not defined after reset, program after all zero-bits are set to zero)

Table 16 Subaddress 62

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
BSTA	amplitude of colour burst; input representation accordance with CCIR 601	white-to-black = 92.5 IRE; burst = 40 IRE; NTSC encoding BSTA = 0 to 1.25 × nominal(1) white-to-black = 92.5 IRE; burst = 40 IRE; PAL encoding BSTA = 0 to 1.76 × nominal(2) white-to-black = 100 IRE; burst = 43 IRE; NTSC encoding BSTA = 0 to 1.20 × nominal(3) white-to-black = 100 IRE; burst = 43 IRE; PAL encoding BSTA = 0 to 1.67 × nominal(4)	
SQP	subcarrier real time	logic 0	control from SAA7151B digital colour decoder
		logic 1	not supported in current version, do not use

Notes

1. Recommended value: BSTA = 102 (66H).
2. Recommended value: BSTA = 72 (48H).
3. Recommended value: BSTA = 106 (6AH).
4. Recommended value: BSTA = 75 (4BH).

Table 17 Subaddress 63 to 66 (four bytes to program subcarrier frequency)

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
FSC0 to FSC3	f_{fsc} = subcarrier frequency (in multiples of line frequency); f_{llc} = clock frequency (in multiples of line frequency)	$FSC = round\left(\frac{f_{fsc}}{f_{llc}} \times 2^{32}\right)$ see note 1	FSC3 = most significant byte FSC0 = least significant byte

Notes

1. Examples:
   a) NTSC-M: f_{fsc} = 227.5 MHz, f_{llc} = 1716 MHz → FSC = 569408543 (21F07C1FH).
   b) PAL-B/G: f_{fsc} = 283.7516 MHz, f_{llc} = 1728 MHz → FSC = 705268427 (2A098ACBH).

Table 18 Subaddress 67 to 6A

DATA BYTE[1]	DESCRIPTION
L21O0	first byte of captioning data, odd field
L21O1	second byte of captioning data, odd field
L21E0	first byte of extended data, even field
L21E1	second byte of extended data, even field

Note

1. LSBs of the respective bytes are encoded immediately after run-in and framing code, the MSBs of the respective bytes have to carry the parity bit, in accordance with the definition of line 21 encoding format.

Table 19 Subaddress 6B

DATA BYTE	DESCRIPTION
SCCLN	selects the actual line, where closed caption or extended data are encoded; see note 1
MODIN	defines video data of MP port or VP(DP) port to be encoded; see Table 20

Note

1. Line = (SCCLN + 4) for M systems; line = (SCCLN + 1) for other systems.

Table 20 Logic levels and function of MODIN

DATA BYTE		FUNCTION
MODIN1	MODIN0	
0	0	unconditionally from MP port
0	1	from MP port, if pin SEL_ED = HIGH; otherwise from VP port
1	0	unconditionally from VP port
1	1	from VP port, if pin SEL_ED = HIGH; otherwise from MP port

Table 21 Subaddress 6C

DATA BYTE	LOGIC LEVEL	DESCRIPTION
PRCV2	0	polarity of RCV2 as output is active HIGH, rising edge is taken when input, respectively; default after reset
	1	polarity of RCV2 as output is active LOW, falling edge is taken when input, respectively
ORCV2	0	pin RCV2 is switched to input; default after reset
	1	pin RCV2 is switched to output
CBLF	0	if ORCV2 = HIGH, pin RCV2 provides an HREF signal (Horizontal Reference Pulse that is HIGH during active portion of line, also during vertical blanking Interval); default after reset
	1	if ORCV2 = LOW, signal input to RCV2 is used for horizontal synchronization only (if TRCV2 = 1); default after reset if ORCV2 = LOW, signal input to RCV2 is used for horizontal synchronization (if TRCV2 = 1) also as an internal blanking signal
PRCV1	0	polarity of RCV1 as output is active HIGH, rising edge is taken when input, respectively; default after reset
	1	polarity of RCV1 as output is active LOW, falling edge is taken when input, respectively
ORCV1	0	pin RCV1 is switched to input; default after reset
	1	pin RCV1 is switched to output
TRCV2	0	horizontal synchronization is taken from RCV1 port; default after reset
	1	horizontal synchronization is taken from RCV2 port
SRCV1	–	defines signal type on pin RCV1; see Table 22

Table 22 Logic levels and function of SRCV1

DATA BYTE		AS OUTPUT	AS INPUT	FUNCTION
SRCV11	SRCV10			
0	0	VS	VS	Vertical Sync each field; default after reset
0	1	FS	FS	Frame Sync (odd/even)
1	0	FSEQ	FSEQ	Field Sequence, vertical sync every fourth field (FISE = 1) or eighth field (FISE = 0)
1	1	–	–	not applicable

Table 23 Subaddress 6D

DATA BYTE	DESCRIPTION
CCEN	enables individual line 21 encoding; see Table 24
SRCM	defines signal type on pin RCM1; see Table 25

Table 24 Logic levels and function of CCEN

DATA BYTE		FUNCTION
CCEN1	CCEN0	
0	0	line 21 encoding OFF
0	1	enables encoding in field 1 (odd)
1	0	enables encoding in field 2 (even)
1	1	enables encoding in both fields

Table 25 Logic levels and function of SRCM

DATA BYTE		AS OUTPUT	FUNCTION
SRCM1	SRCM0		
0	0	VS	Vertical Sync each field
0	1	FS	Frame Sync (odd/even)
1	0	FSEQ	Field Sequence, vertical sync every fourth field (FISE = 1) or eighth field (FISE = 0)
1	1	–	not applicable

Table 26 Subaddress 6E to 6F

DATA BYTE	DESCRIPTION
HTRIG	sets the Horizontal Trigger phase related to signal on RCV1 or RCV2 input values above 1715 (FISE = 1) or 1727 (FISE = 0) are not allowed increasing HTRIG decreases delays of all internally generated timing signals reference mark: analog output horizontal sync (leading slope) coincides with active edge of RCV used for triggering at HTRIG = 032H

Table 27 Subaddress 70

DATA BYTE	LOGIC LEVEL	DESCRIPTION
VTRIG	–	sets the Vertical TRIGger phase related to signal on RCV1 input increasing VTRIG decreases delays of all internally generated timing signals, measured in half lines variation range of VTRIG = 0 to 31 (1FH)
SBLBN	0	vertical blanking is defined by programming of FAL and LAL
	1	vertical blanking is forced automatically at least during field synchronization and equalization pulses; note 1
PHRES	–	selects the phase reset mode of the colour subcarrier generator; see Table 28

Note

1. If cross-colour reduction is programmed, it is active between FAL and LAL in both events.

Table 28 Logic levels and function of PHRES

DATA BYTE		FUNCTION
PHRES1	PHRES0	
0	0	no reset
0	1	reset every two lines
1	0	reset every eight fields
1	1	reset every four fields

Table 29 Subaddress 71 to 73

DATA BYTE	DESCRIPTION
BMRQ	beginning of MP ReQuest signal (RCM2) values above 1715 (FISE = 1) or 1727 (FISE = 0) are not allowed first active pixel at analog outputs (corresponding input pixel coinciding with RCM2) at BMRQ = 0F9H (115H)
EMRQ	end of MP ReQuest signal (RCM2) values above 1715 (FISE = 1) or 1727 (FISE = 0) are not allowed last active pixel at analog outputs (corresponding input pixel coinciding with RCM2) at EMRQ = 686H (690H)

Table 30 Subaddress 77 to 79

DATA BYTE	DESCRIPTION
BRCV	beginning of output signal on RCV2 pin values above 1715 (FISE = 1) or 1727 (FISE = 0) are not allowed first active pixel at analog outputs (corresponding input pixel coinciding with RCV2) at BRCV = 0F9H (115H)
ERCV	end of output signal on RCV2 pin values above 1715 (FISE = 1) or 1727 (FISE = 0) are not allowed last active pixel at analog outputs (corresponding input pixel coinciding with RCV2) at ERCV = 686H (690H)

Table 31 Subaddress 7A to 7D

DATA BYTE	DESCRIPTION
FLEN	Length of a Field = FLEN + 1, measured in half lines valid range is limited to 524 to 1022 (FISE = 1) respectively 624 to 1022 (FISE = 0), FLEN should be even
FAL	First Active Line after vertical blanking interval = FAL + 1, measured in lines FAL = 0 coincides with the first field synchronization pulse
LAL	Last Active Line before vertical blanking interval = LAL + 1, measured in lines LAL = 0 coincides with the first field synchronization pulse

SUBADDRESSES

In subaddresses 5B, 5C, 5D, 5E and 62 all IRE values are rounded up.

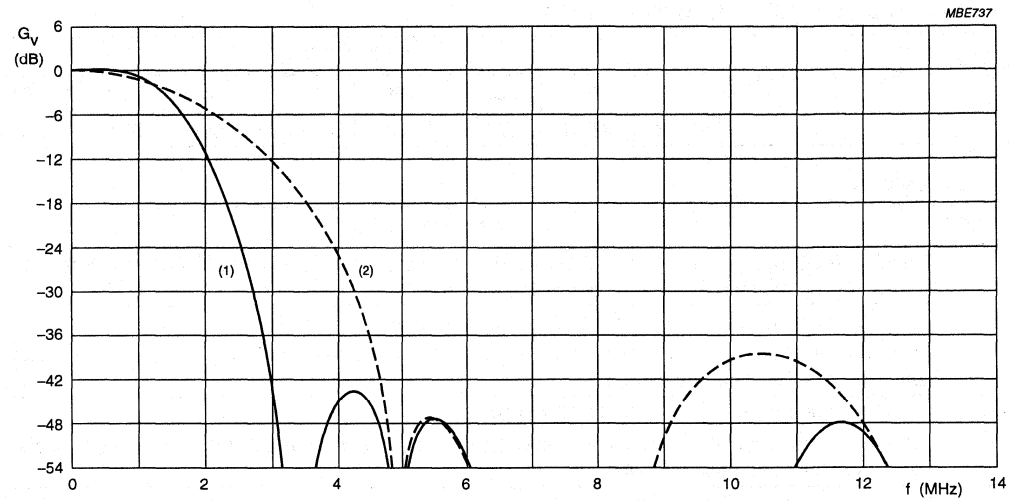
Slave Transmitter

Table 32 Slave Transmitter (slave address 89H or 8DH)

REGISTER FUNCTION	SUBADDRESS	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
Status byte	–	VER2	VER1	VER0	CCRDE	CCRDO	FSQ2	FSQ1	FSQ0

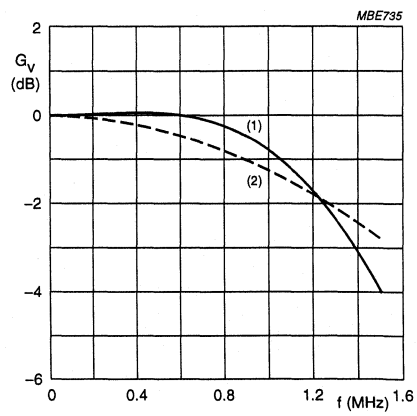
Table 33 No subaddress

DATA BYTE	DESCRIPTION
VER	Version identification of the device. It will be changed with all versions of the IC that have different programming models. Current Version is 000 binary.
CCRDE	Closed caption bytes of the even field have been encoded. The bit is reset after information has been written to the subaddresses 69 and 6A. It is set immediately after the data have been encoded.
CCRDO	Closed caption bytes of the odd field have been encoded. The bit is reset after information has been written to the subaddresses 67 and 68. It is set immediately after the data have been encoded.
FSQ	State of the internal field sequence counter. Bit 0 (FSQ0) gives the odd/even information; odd = LOW, even = HIGH.



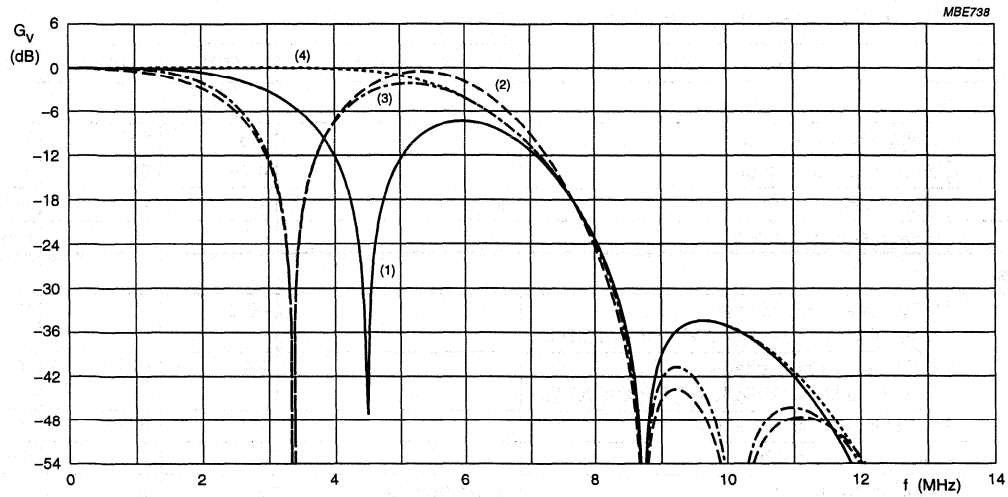
(1) SCBW = 1.
(2) SCBW = 0.

Fig.3 Chrominance transfer characteristic 1.



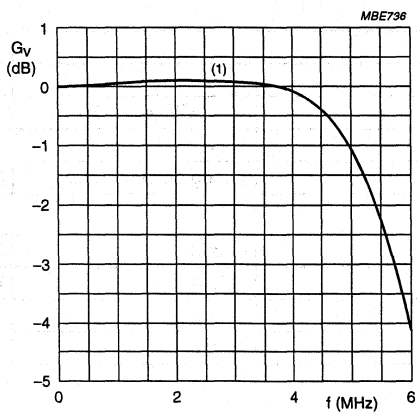
(1) SCBW = 1.
(2) SCBW = 0.

Fig.4 Chrominance transfer characteristic 2.



(1) CCRS1 = 0; CCRS0 = 1.
(2) CCRS1 = 1; CCRS0 = 0.
(3) CCRS1 = 1; CCRS0 = 1.
(4) CCRS1 = 0; CCRS0 = 0.

Fig.5 Luminance transfer characteristic 1.



CCRS1 = 0; CCRS0 = 0.

Fig.6 Luminance transfer characteristic 2

CHARACTERISTICS

V_{DDD} = 4.5 to 5.5 V; T_{amb} = 0 to 70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Supply					
V_{DDD}	digital supply voltage		4.5	5.5	V
V_{DDA}	analog supply voltage		4.75	5.25	V
I_{DDD}	digital supply current	note 1	–	170	mA
I_{DDA}	analog supply current	note 1	–	55	mA
Inputs					
V_{IL}	LOW level input voltage (except LLC, SDA, SCL, AP, SP and XTALI)		−0.5	+0.8	V
V_{IH}	HIGH level input voltage (except LLC, SDA, SCL, AP, SP and XTALI)		2.0	V_{DDD} + 0.5	V
	HIGH level input voltage (LLC)		2.4	V_{DDD} + 0.5	V
V_{LI}	input leakage current		–	1	µA
C_I	input capacitance	clocks operating	–	10	pF
		data available	–	8	pF
		I/Os at high impedance	–	8	pF
Outputs					
V_{OL}	LOW level output voltage (except SDA and XTALO)	note 2	0	0.6	V
V_{OH}	HIGH level output voltage (except LLC, SDA, $\overline{DTACK}$ and XTALO)	note 2	2.4	V_{DDD} + 0.5	V
	HIGH level output voltage (LLC)	note 2	2.6	V_{DDD} + 0.5	V
I^2C-bus; SDA and SCL					
V_{IL}	LOW level input voltage		−0.5	+1.5	V
V_{IH}	HIGH level input voltage		3.0	V_{DDD} + 0.5	V
I_I	input current	V_I = LOW or HIGH	−10	+10	µA
V_{OL}	LOW level output voltage (SDA)	I_{OL} = 3 mA	–	0.4	V
I_O	output current	during acknowledge	3	–	mA
Clock timing (LLC)					
T_{LLC}	cycle time	note 3	34	41	ns
δ	duty factor t_{HIGH}/T_{LLC}	note 4	40	60	%
t_r	rise time	note 3	–	5	ns
t_f	fall time	note 3	–	6	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Input timing					
$t_{SU;CREF}$	input data set-up time (C_{ref})		6	–	ns
$t_{HD;CREF}$	input data hold time (C_{ref})		3	–	ns
t_{SU}	input data set-up time (any other except SEL_MPU, CDIR, $\overline{RW}$/SCL, A0/SDA, $\overline{CS}$/SA, $\overline{RESET}$, AP and SP)		6	–	ns
t_{HD}	input data hold time (any other except SEL_MPU, CDIR, $\overline{RW}$/SCL, A0/SDA, $\overline{CS}$/SA, $\overline{RESET}$, AP and SP)		3	–	ns
Crystal oscillator					
f_n	nominal frequency (usually 27 MHz)	3rd harmonic	–	30	MHz
$\Delta f/f_n$	permissible deviation of nominal frequency	note 5	−50	+50	10^{-6}
CRYSTAL SPECIFICATION					
T_{amb}	operating ambient temperature		0	70	°C
C_L	load capacitance		8	–	pF
R_S	series resistance		–	80	Ω
C_1	motional capacitance (typical)		1.5 −20%	1.5 +20%	fF
C_0	parallel capacitance (typical)		3.5 −20%	3.5 +20%	pF
MPU interface timing					
t_{AS}	address set-up time	note 6	9	–	ns
t_{AH}	address hold time		0	–	ns
$t_{R\overline{W}S}$	read/write set-up time	note 6	9	–	ns
$t_{R\overline{W}H}$	read/write hold time		0	–	ns
t_{DD}	data bus floating from $\overline{CS}$ (read)	notes 7, 8 and 9; n = 9	–	400	ns
t_{DF}	data valid from $\overline{CS}$ (read)	notes 7 and 8; n = 5	–	255	ns
t_{DS}	data bus set-up time (write)	note 6	9	–	ns
t_{DH}	data bus hold time (write)	note 6	9	–	ns
t_{ACS}	acknowledge delay from $\overline{CS}$	notes 7 and 8; n = 11	–	475	ns
$t_{\overline{CS}D}$	$\overline{CS}$ HIGH from acknowledge		0	–	ns
t_{DAT}	$\overline{DTACK}$ floating from $\overline{CS}$ HIGH	notes 7 and 8; n = 7	–	330	ns
Data and reference signal output timing					
C_L	output load capacitance		7.5	40	pF
t_{OH}	output hold time		4	–	ns
t_{OD}	output delay time	C_{ref} in output mode	–	25	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
CHROMA, Y and CVBS outputs					
$V_{o(p-p)}$	output signal voltage (peak-to-peak value)	note 10	1.9	2.1	V
R_I	internal serial resistance		18	35	Ω
R_L	output load resistance		80	–	Ω
B	output signal bandwidth of DACs	–3 dB	10	–	MHz
ILE	LF integral linearity error of DACs		–	±2	LSB
DLE	LF differential linearity error of DACs		–	±1	LSB

Notes

1. At maximum supply voltage with highly active input signals.
2. The levels have to be measured with load circuits of 1.2 kΩ to 3.0 V (standard TTL load) and C_L = 25 pF.
3. The data is for both input and output direction.
4. With LLC in input mode. In output mode, with a crystal connected to XTALO/XTALI duty factor is typically 50%.
5. If an internal oscillator is used, crystal deviation of nominal frequency is directly proportional to the deviation of subcarrier frequency and line/field frequency.
6. The value is calculated via equation $t = t_{SU} + t_{HD}$
7. The value depends on the clock frequency. The numbers given are calculated with f_{LLC} = 27 MHz.
8. The values given are calculated via equation $t_{dmax} = t_{OD} + n \times t_{LLC} + t_{LLC} + t_{SU}$
9. The falling edge of $\overline{DTACK}$ will always occur1 × LLC after data is valid.
10. For full digital range, without load, V_{DDA} = 5.0 V. The typical voltage swing is 2.0 V, the typical minimum output voltage (digital zero at DAC) is 0.2 V.

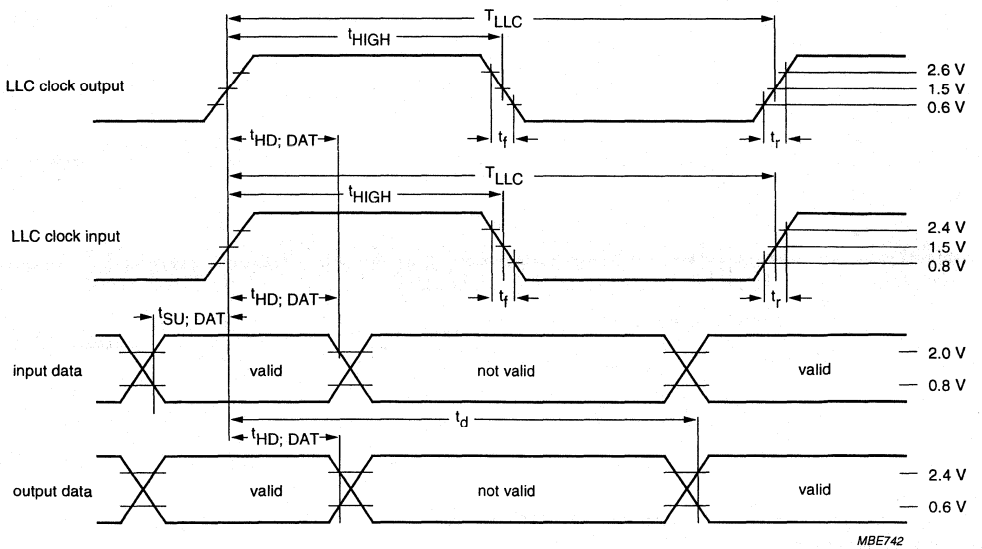
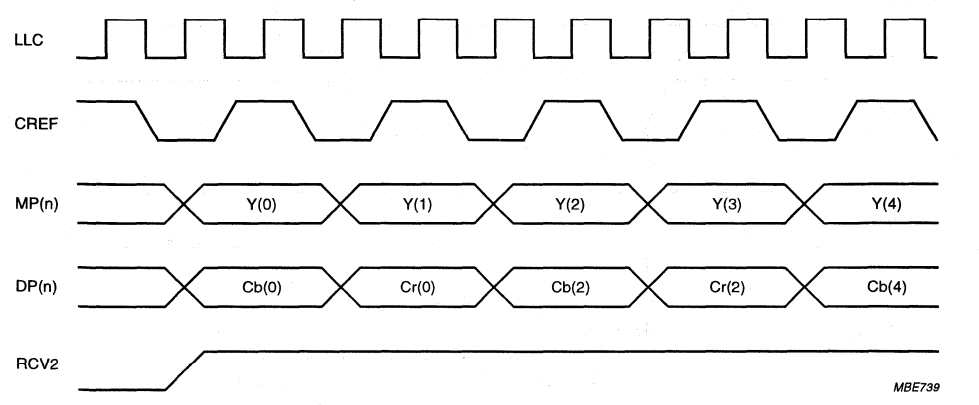
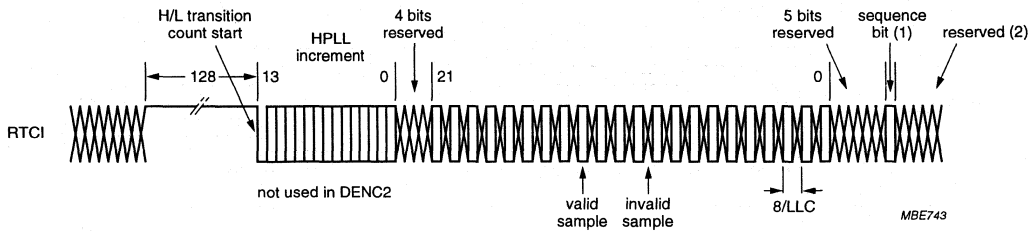


Fig.7 Clock data timing.



The data demultiplexing phase is coupled to the internal horizontal phase.
The C_{ref} signal applies only for the 16 lines digital TV format, because these signals are only valid in 13.5 MHz.
The phase of the RCV2 signal is programmed to 0F8h (115H for 50 Hz) in this example in output mode (BRCV2).

Fig.8 Digital TV timing.



(1) Sequence bit:
PAL = logic 0 then (R – Y) line normal; PAL = logic 1 then (R – Y) line inverted.
NTSC = logic 0 then no change.

(2) Reserved bits: 236 with 50 Hz systems; 233 with 60 Hz systems.

Fig.9 RTCI timing.

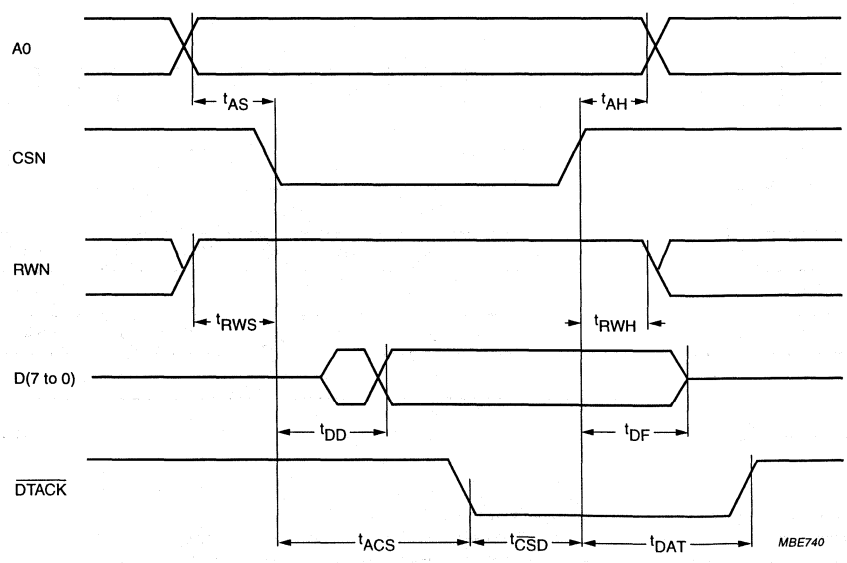


Fig.10 MPU interface timing (READ cycle).

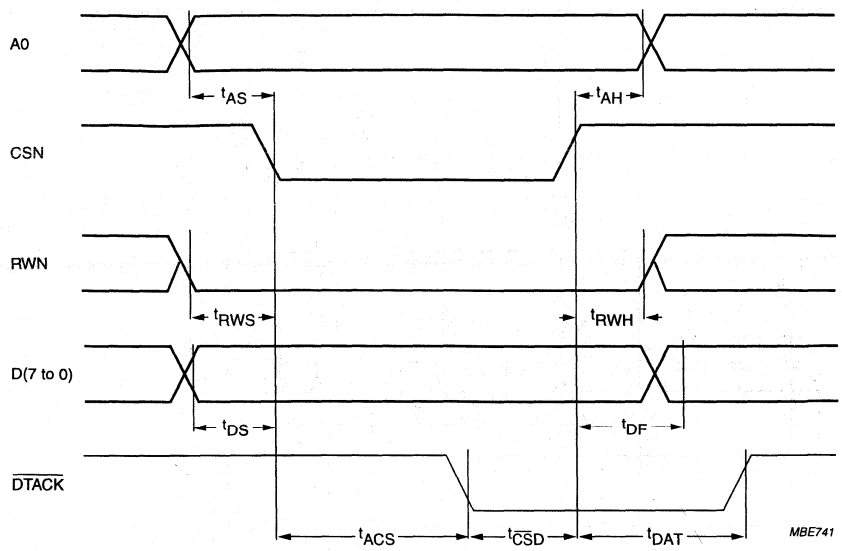


Fig.11 MPU interface timing (WRITE cycle).

APPLICATION INFORMATION

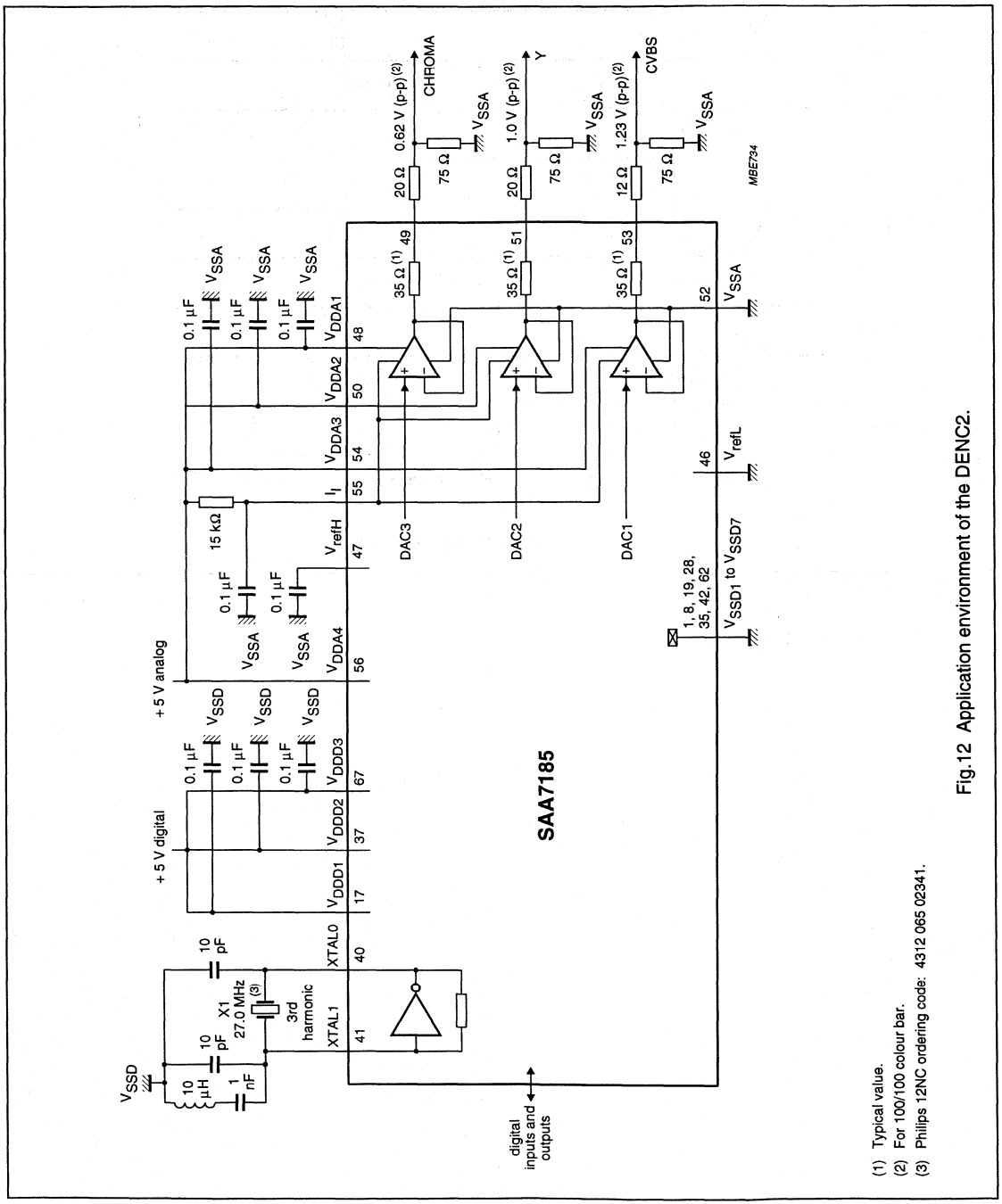
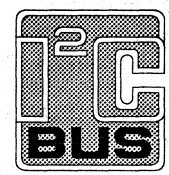


Fig.12 Application environment of the DENC2.

(1) Typical value.
(2) For 100/100 colour bar.
(3) Philips 12NC ordering code: 4312 065 02341.

Digital Video Scaler (DVS) SAA7186



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Digital Video Scaler (DVS) SAA7186

1. FEATURES

- Scaling of video picture windows down to randomly sized windows
- Processes maximum 1023 pixels per line and 1023 lines per field
- Two-dimensional data processing for improved signal quality of scaled video data and for compression of video data
- 16-bit YUV input data buffer
- Interlace/non-interlace video data processing and field control
- Line memories in Y path and UV path to store two lines, each with 2 x 768 x 8 bit capacity
- Vertical sync processing by scale control
- Non-scaled mode to get full picture or to gate videotext lines
- UV input and output data binary/two´s complement
- Switchable RGB matrix and anti-gamma ROMs
- 16-word FIFO register for 32-bit output data
- Output formats: 5-bit and 8-bit RGB, 8-bit YUV or 8-bit monochrome

2. GENERAL DESCRIPTION

The CMOS circuit SAA7186 scales and filters digital video data to randomly sized picture windows. YUV input data in 4:2:2 format are required (SAA7191B source).

3. QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	4.5	5	5.5	V
$I_{DD\ tot}$	total supply current (inputs LOW, without output load)	-	-	180	mA
V_I	data input level	TTL-compatible			
V_O	data output level	TTL-compatible			
LLC	input clock frequency	-	-	32	MHz
T_{amb}	operating ambient temperature range	0	-	70	°C

4. ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7186	100	QFP	plastic	SOT317-1

5. BLOCK DIAGRAM

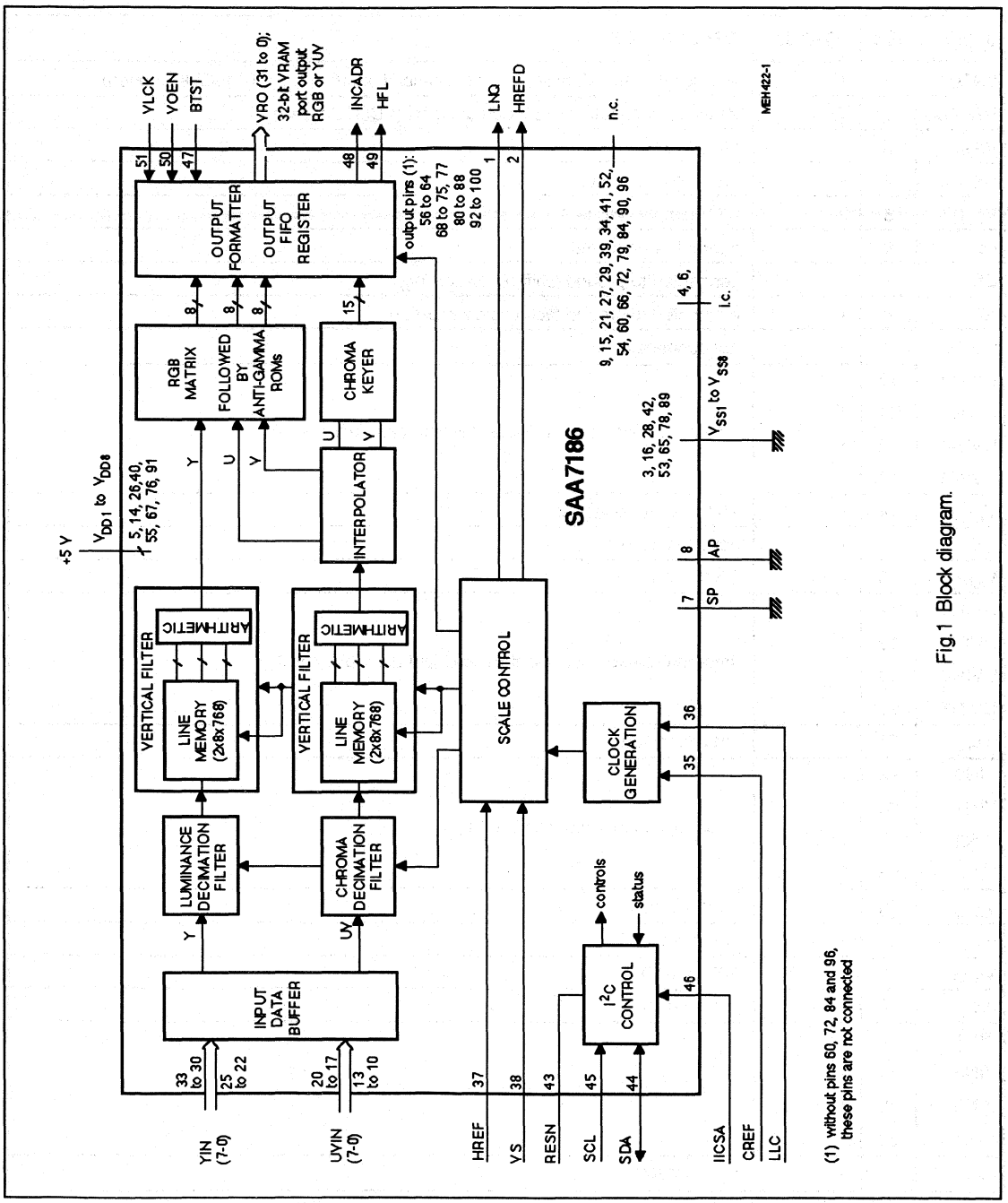


Fig.1 Block diagram.

6. PINNING

SYMBOL	PIN	STATUS	DESCRIPTION
LNQ	1	O	line qualifier signal; active polarity defined by QPL-bit in "10" (VCLK strobed)
HREFD	2	O	delay-compensated HREF output signal (VCLK strobed)
V_{SS1}	3	-	GND1 (0 V)
i.c.	4	-	internally connected
V_{DD1}	5	-	+5 V supply voltage 1
i.c.	6	-	internally connected
SP	7	I	connected to ground (shift pin for testing)
AP	8	I	connected to ground (action pin for testing)
n.c.	9	-	not connected
UVIN0	10	I	time-multiplexed colour-difference input data (bits 0 to 3)
UVIN1	11	I	
UVIN2	12	I	
UVIN3	13	I	
V_{DD2}	14	-	+5 V supply voltage 2
n.c.	15	-	not connected
V_{SS2}	16	-	GND2 (0 V)
UVIN4	17	I	time- multiplexed colour-difference input data (bits 4 to 7)
UVIN5	18	I	
UVIN6	19	I	
UVIN7	20	I	
n.c.	21	-	not connected
YIN0	22	I	luminance input data (bits 0 to 3)
YIN1	23	I	
YIN2	24	I	
YIN3	25	I	
V_{DD3}	26	-	+5 V supply voltage 3
n.c.	27	-	not connected
V_{SS3}	28	-	GND3 (0 V)
n.c.	29	-	not connected
YIN4	30	I	luminance input data (bits 4 to 7)
YIN5	31	I	
YIN6	32	I	
YIN7	33	I	
n.c.	34	-	not connected

SYMBOL	PIN	STATUS	DESCRIPTION
CREF	35	I	clock reference, external sync signal
LLC	36	I	line-locked system clock input signal (twice of pixel rate)
HREF	37	I	horizontal reference, pixel data clock signal (also present during vertical blanking)
VS	38	I	vertical sync input signal (approximately 6 lines long)
n.c.	39	-	not connected
V_{DD4}	40	-	+5 V supply voltage 4
n.c.	41	-	not connected
V_{SS4}	42	-	GND4 (0 V)
RESN	43	I	reset input (active-LOW for at least 30LLC periods)
SDA	44	I/O	IIC-bus data line
SCL	45	I	IIC-bus clock line
IICSA	46	I	set module address input of IIC-bus (LOW = B8, HIGH = BC)
BTST	47	I	output disable input; HIGH sets all data outputs to high-impedance state
INCADR	48	O	line increment / vertical reset control output line
HFL	49	O	FIFO register half-full flag output
VOEN	50	I	VRAM port output enable input (active-LOW)
VCLK	51	I	FIFO register clock input signal
n.c.	52	-	not connected
V_{SS5}	53	-	GND5 (0 V)
n.c.	54	-	not connected
V_{DD5}	55	-	+5 V supply voltage 5
VRO31	56	O	video output; 32-bit VRAM output port (bits 31 to 28)
VRO30	57	O	
VRO29	58	O	
VRO28	59	O	
n.c.	60	-	not connected
VRO27	61	O	video output; 32-bit VRAM output port (bits 27 to 24)
VRO26	62	O	
VRO25	63	O	
VRO24	64	O	
V_{SS6}	65	-	GND6 (0 V)
n.c.	66	-	not connected
V_{DD6}	67	-	+5 V supply voltage 6
VRO23	68	O	video output; 32-bit VRAM output port (bits 23 to 22)
VRO22	69	O	

SYMBOL	PIN	STATUS	DESCRIPTION
VRO21	70	O	video output; 32-bit VRAM output port (bits 21 to 20)
VRO20	71	O	
n.c.	72	-	not connected
VRO19	73	O	video output; 32-bit VRAM output port (bits 19 to 17)
VRO18	74	O	
VRO17	75	O	
V_{DD7}	76	-	+5 V supply voltage 7
VRO16	77	O	video output; 32-bit VRAM output port (bit16)
V_{SS7}	78	-	GND7 (0 V)
n.c.	79	-	not connected
VRO15	80	O	video output; 32-bit VRAM output port (bits 15 to 12)
VRO14	81	O	
VRO13	82	O	
VRO12	83	O	
n.c.	84	-	not connected
VRO11	85	O	video output; 32-bit VRAM output port (bits 11 to 8)
VRO10	86	O	
VRO9	87	O	
VRO8	88	O	
V_{SS8}	89	O	GND8 (0 V)
n.c.	90	-	not connected
V_{DD8}	91	-	+5 V supply voltage 8
VRO7	92	O	video output; 32-bit VRAM output port (bits 7 to 4)
VRO6	93	O	
VRO5	94	O	
VRO4	95	O	
n.c.	96	-	not connected
VRO3	97	O	video output; 32-bit VRAM output port (bits 3 to 0)
VRO2	98	O	
VRO1	99	O	
VRO0	100	O	

PIN CONFIGURATION

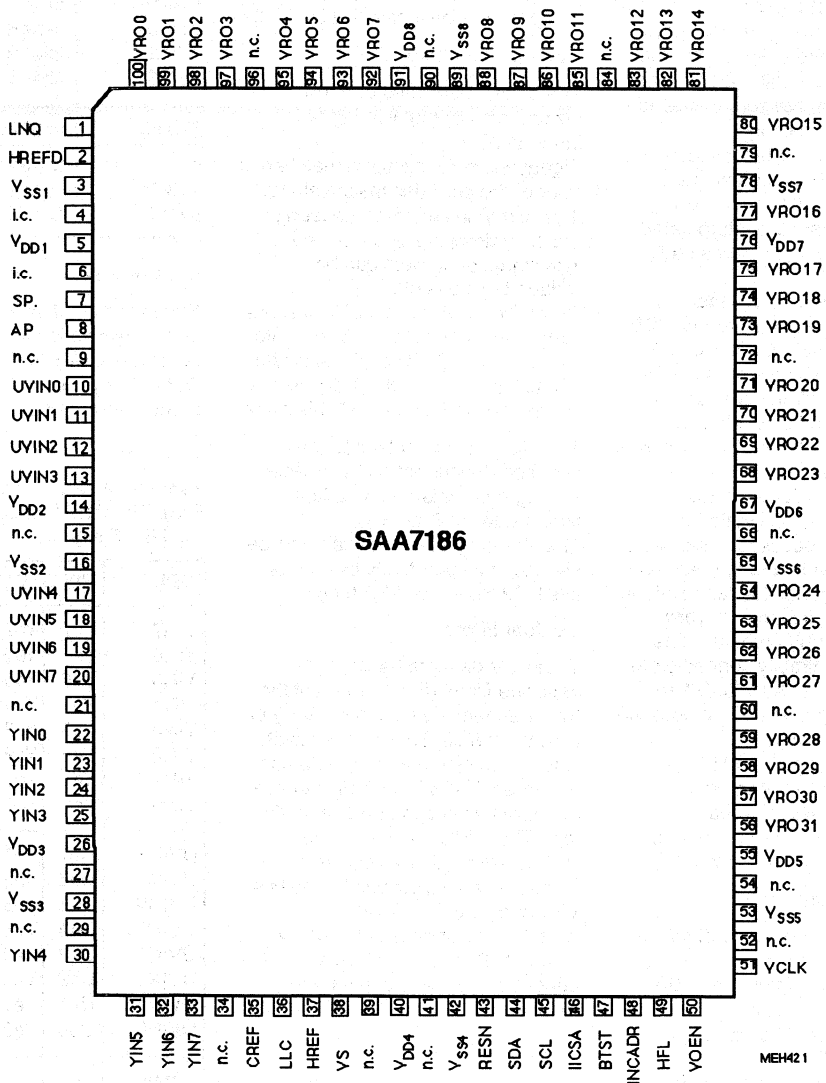


Fig.2 Pin configuration.

7. FUNCTIONAL DESCRIPTION

The input port is output of Philips digital video multistandard decoders (SAA7151B, SAA7191B) or other similar sources.
The SAA7186 input supports the 16-bit YUV 4:2:2 format.
The video data from the input port are converted into a unique internal two´s complement data stream and are processed in horizontal direction in two separate decimation filters.Then they are processed in vertical direction by the vertical processing unit (VPU).
Chrominance data are interpolated to a 4:4:4 format; a chroma keying bit is generated.
The 4:4:4 YUV data are then converted from the YUV to the RGB domain in a digital matrix. ROM tables in the RGB data path can be used for anti-gamma correction of gamma-corrected input signals. Uncorrected RGB and YUV signals can be bypassed.
A scale control unit generates reference and gate signals for scaling of the processed video data. After data formatting to the various VRAM port formats, the scaled video data are buffered in the 16 word x 32-bit output FIFO register. The FIFO output is directly connected to the VRAM output bus VRO(31-0). Specific reference signals support an easy memory interfacing.
All functions of the SAA7186 are controlled via I²C-bus using 17 subaddresses. The external microcontroller can get information by reading the status register.

Video input port

The 16-bit YUV input data in 4:2:2 format (Table 1) consist of 8-bit luminance data Y (pins YIN(7-0)) and 8-bit time-multiplexed colour-difference data UV (pins UVIN(7-0)).
The input data are clocked in by the signals LLC and CREF (Fig.3). HREF and VS inputs define the video scan pattern (window).

Sequential input data

- are limited to maximum 768 active pixels per line if the vertical filter is active
- UV can be processed in straight binary and two´s complement representation (controlled by TCC)

Decimation filters

The decimation filters perform accurate horizontal filtering of the input data stream.
Signal characteristics are matched in front of the pixel decimation stage, thus disturbing artifacts, caused by the pixel dropping, are reduced.
The signal bandwidth can be reduced in steps of:
2-tap filter = –6 dB at 0.325 pixel rate
3-tap filter = –6 dB at 0.25 pixel rate
4-tap filter = –6 dB at 0.21 pixel rate
5-tap filter = –6 dB at 0.125 pixel rate
9-tap filter = –6 dB at 0.075 pixel rate

The different characteristics are choosen dependent on the defined scaling parameters in an adaptive filter mode (AFS-bit = 1).
The filter characteristics can also be selected independently by control bits HF2 to HF0 at AFS-bit = 0.

Vertical filters

Y and UV data are handled in separate filters (Fig.1). Each of the two line memories has a capacity of 2 x 768 x 8-bit. Thus two complete video lines of 4:2:2 YUV data can be stored. The VPU is split into two memory banks and one arithmetic unit. The available processing modes, respectively transfer functions, are selectable by the bits VP1 and VP0 if AFS = 0.
An adaptive mode is selected by AFS = 1. Disturbing artifacts, generated by line dropping, are reduced.

Adaptive filter selection (AFS = 1):

scaling ratio	filter function (refer to I²C section)
XD/XS	horizontal
≤1	bypassed
≤14/15	filter 1
≤11/15	filter 6
≤7/15	filter 3
≤3/15	filter 4
YD/YS	vertical
≤1	bypassed
≤13/15	filter 1
≤4/15	filter 2

RGB matrix

Y data and UV data are converted after interpolation into RGB data according to CCIR601 recommendation. Data are bypassed in YUV or monochrome modes.

Table 1 4 : 2 : 2 format (pixels per line). The time frames are controlled by the HREF signal.

INPUT	PIXEL BYTE SEQUENCE				
YIN7	Ye7	Yo7	Ye7	Yo7	Ye7
YIN6	Ye6	Yo6	Ye6	Yo6	Ye6
YIN5	Ye5	Yo5	Ye5	Yo5	Ye5
YIN4	Ye4	Yo4	Ye4	Yo4	Ye4
YIN3	Ye3	Yo3	Ye3	Yo3	Ye3
YIN2	Ye2	Yo2	Ye2	Yo2	Ye2
YIN1	Ye1	Yo1	Ye1	Yo1	Ye1
YIN0	Ye0	Yo0	Ye0	Yo0	Ye0
UVIN7	Ue7	Ve7	Ue7	Ve7	Ue7
UVIN6	Ue6	Ve6	Ue6	Ve6	Ue6
UVIN5	Ue5	Ve5	Ue5	Ve5	Ue5
UVIN4	Ue4	Ve4	Ue4	Ve4	Ue4
UVIN3	Ue3	Ve3	Ue3	Ve3	Ue3
UVIN2	Ue2	Ve2	Ue2	Ve2	Ue2
UVIN1	Ue1	Ve1	Ue1	Ve1	Ue1
UVIN0	Ue0	Ve0	Ue0	Ve0	Ue0
Y frame	0	1	2	3	4
UV frame	0		2		4

e = even pixel; o = odd pixel

The matrix equations are these considering the digital quantization:

R = Y + 1.375 V
G = Y − 0.703125 V − 0.34375 U
B = Y + 1.734375 U.

Anti-gamma ROM tables:
ROM tables are implemented at the matrix output to provide anti-gamma correction of the RGB data. A curve for a gamma of 1.4 is implemented

The tables can be used (RTB-bit = 0) to compensate gamma correction for linear data representation of RGB output data.

Chrominance signal keyer

The keyer generates an alpha signal to achieve a 5-5-5 +α RGB alpha output signal. Therefore, the processed UV data amplitudes are compared with thresholds set via I²C-bus (subaddresses "0C to 0F"). A logical "1" signal is generated if the amplitude is inside the specified amplitude range, otherwise a logical "0" is generated.
Keying can be switched off by setting the lower limit higher than the upper limit ("0C or 0E" and "0D or 0F").

Scale control and vertical regions

The scale control block SC includes vertical address/sequence counters to define the current position in the input field and to address the internal VPU memories.
To perform scaling, XD of XS pixel selection in horizontal direction and YD of YS line selection in vertical direction are applied. The pixel and line dropping are controlled at the input of the FIFO register.
To control the decimation filter function and the vertical data processing in the adaptive mode

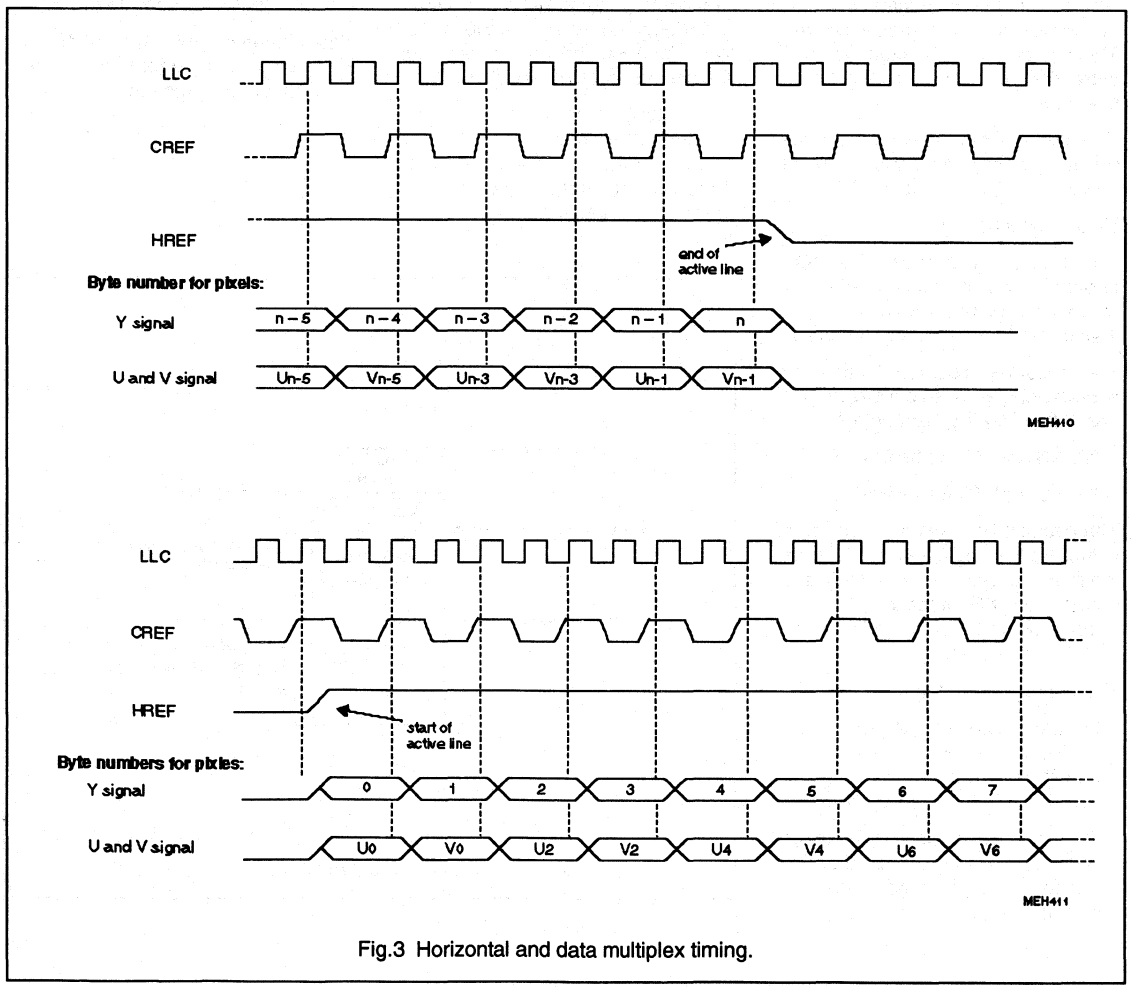


Fig.3 Horizontal and data multiplex timing.

(AFS = 1), the scaling ratio in horizontal and vertical direction is estimated in the SC block.

The input field can be divided into two vertical regions – the bypass region and the scaling region, which are defined via I²C-bus by the parameters VS, VC, YO and YS.

Vertical bypass region:

Data are not scaled and independent of I²C-bits FS1, FS0 the output format is always 8-bit grayscale (monochrome). The SAA7186 outputs all active pixels of a line, defined by the HREF input signal if the vertical bypass region is active. This can be used, for example, to store videotext information in the field memory.

The start line of the bypass region is defined by VS; the number of lines to be bypassed is defined by VC.

Vertical scaling region:

Data is scaled with start at line YO and the output format is selected when FS1, FS0 are valid.
This is the "normal operation" area.

The input/output screen dimensions in horizontal and vertical direction are defined by the parameters

XO, XS and XD for horizontal

YO, YS and YD for vertical.

The circuit processes XS samples of a line. Remaining pixels are ignored if a line is longer than XS. If a line is shorter than XS, processing is aborted when the falling edge of HREF is detected.

Vertical regions in Fig.4:

- the two regions can be programmed via I²C-bus, whereby regions should not overlap (active region overrides the bypass region).
- the start of a normal active picture depends on video standard and has to be programmed to the correct value.
- the offsets XO and YO have to be set according to the internal processing delays to ensure the complete number of destination pixels and lines (Table 6).
- the scaling parameters can be used to perform a panning function over the video frame/field.

Output data representation and levels

Output data representation of the YUV data can be modified by bits YLIM and MCT (subaddress 10). The DC gain is 1 for YUV input data. The corresponding RGB levels are defined by the matrix equations. With YLIM = 0, the luminance levels are limited according to CCIR 601

16 (239) = black
235 (20) = white
(..) = grayscale luminance levels

if the YUV or monochrome luminance output formats are selected.

With YLIM = 1, the luminance levels are not limited.

The signal levels of the RGB formats are limited in 8-bit to "0" or "255". For the 5-bit RGB formats a truncation from 8-bit to 5-bit is implemented.

Fill values are inserted dependent on longword position and destination size:

- "0" in RGB formats and for Y two´2 complement U, V
- "128" for U, V (straight binary)
- "255" in 8-bit grayscale format

The unused output values of the YUV and grayscale formats can be used for other purposes.

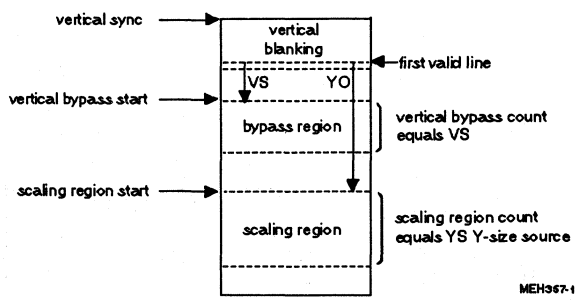


Fig.4 Vertical regions.

Table 2 VRAM port output data formats at EFE-bit = 0 dependend on FS1 and FS0 bits (set via I²C-bus)

PIXEL OUTPUT BITS	FS1 = 0; FS0 = 0 RGB 5-5-5 + 1 32-BIT WORDS			FS1 = 0; FS0 = 1 YUV 4:2:2 32-BIT WORDS			FS1 = 1; FS0 = 0 YUV 4:2:2 TEST 16-BIT WORDS			FS1 = 1; FS0 = 1 8-bit monochrome 32-BIT WORDS		
PIXEL ORDER	n	n+2	n+4	n	n+2	n+4	n	n+1	n+2	n n+1	n+4 n+5	n+8 n+9
VRO31	α	α	α	Ye7	Ye7	Ye7	Ye7	Yo7	Ye7	Ya7	Ya7	Ya7
VRO30	R4	R4	R4	Ye6	Ye6	Ye6	Ye6	Yo6	Ye6	Ya6	Ya6	Ya6
VRO29	R3	R3	R3	Ye5	Ye5	Ye5	Ye5	Yo5	Ye5	Ya5	Ya5	Ya5
VRO28	R2	R2	R2	Ye4	Ye4	Ye4	Ye4	Yo4	Ye4	Ya4	Ya4	Ya4
VRO27	R1	R1	R1	Ye3	Ye3	Ye3	Ye3	Yo3	Ye3	Ya3	Ya3	Ya3
VRO26	R0	R0	R0	Ye2	Ye2	Ye2	Ye2	Yo2	Ye2	Ya2	Ya2	Ya2
VRO25	G4	G4	G4	Ye1	Ye1	Ye1	Ye1	Yo1	Ye1	Ya1	Ya1	Ya1
VRO24	G3	G3	G3	Ye0	Ye0	Ye0	Ye0	Yo0	Ye0	Ya0	Ya0	Ya0
VRO23	G2	G2	G2	Ue7	Ue7	Ue7	Ue7	Ve7	Ue7	Yb7	Yb7	Yb7
VRO22	G1	G1	G1	Ue6	Ue6	Ue6	Ue6	Ve6	Ue6	Yb6	Yb6	Yb6
VRO21	G0	G0	G0	Ue5	Ue5	Ue5	Ue5	Ve5	Ue5	Yb5	Yb5	Yb5
VRO20	B4	B4	B4	Ue4	Ue4	Ue4	Ue4	Ve4	Ue4	Yb4	Yb4	Yb4
VRO19	B3	B3	B3	Ue3	Ue3	Ue3	Ue3	Ve3	Ue3	Yb3	Yb3	Yb3
VRO18	B2	B2	B2	Ue2	Ue2	Ue2	Ue2	Ve2	Ue2	Yb2	Yb2	Yb2
VRO17	B1	B1	B1	Ue1	Ue1	Ue1	Ue1	Ve1	Ue1	Yb1	Yb1	Yb1
VRO16	B0	B0	B0	Ue0	Ue0	Ue0	Ue0	Ve0	Ue0	Yb0	Yb0	Yb0
PIXEL ORDER	n+1	n+3	n+5	n+1	n+3	n+5	OUTPUTS NOT USED			n+2 n+3	n+6 n+7	n+10 n+11
VRO15	α	α	α	Yo7	Yo7	Yo7	X	X	X	Yc7	Yc7	Yc7
VRO14	R4	R4	R4	Yo6	Yo6	Yo6	X	X	X	Yc6	Yc6	Yc6
VRO13	R3	R3	R3	Yo5	Yo5	Yo5	X	X	X	Yc5	Yc5	Yc5
VRO12	R2	R2	R2	Yo4	Yo4	Yo4	X	X	X	Yc4	Yc4	Yc4
VRO11	R1	R1	R1	Yo3	Yo3	Yo3	X	X	X	Yc3	Yc3	Yc3
VRO10	R0	R0	R0	Yo2	Yo2	Yo2	X	X	X	Yc2	Yc2	Yc2
VRO9	G4	G4	G4	Yo1	Yo1	Yo1	X	X	X	Yc1	Yc1	Yc1
VRO8	G3	G3	G3	Yo0	Yo0	Yo0	X	X	X	Yc0	Yc0	Yc0
VRO7	G2	G2	G2	Ve7	Ve7	Ve7	X	X	X	Yd7	Yd7	Yd7
VRO6	G1	G1	G1	Ve6	Ve6	Ve6	X	X	X	Yd6	Yd6	Yd6
VRO5	G0	G0	G0	Ve5	Ve5	Ve5	X	X	X	Yd5	Yd5	Yd5
VRO4	B4	B4	B4	Ve4	Ve4	Ve4	X	X	X	Yd4	Yd4	Yd4
VRO3	B3	B3	B3	Ve3	Ve3	Ve3	X	X	X	Yd3	Yd3	Yd3
VRO2	B2	B2	B2	Ve2	Ve2	Ve2	X	X	X	Yd2	Yd2	Yd2
VRO1	B1	B1	B1	Ve1	Ve1	Ve1	X	X	X	Yd1	Yd1	Yd1
VRO0	B0	B0	B0	Ve0	Ve0	Ve0	X	X	X	Yd0	Yd0	Yd0

α = keying bit; R, G, B, Y. U and V = digital signals; e = even pixel number; o = odd pixel number; a b c d = consecutive pixels

Table 3 VRAM port output data formats at EFE-bit = 1 dependend on FS1 and FS0 bits (set via I²C-bus)

PIXEL OUTPUT BITS	FS1 = 0; FS0 = 0 RGB 5-5-5 + 1 16-BIT WORDS			FS1 = 0; FS0 = 1 YUV 4:2:2 16-BIT WORDS			FS1 = 1; FS0 = 0 RGB 8-8-8 24-BIT WORDS			FS1 = 1; FS0 = 1 8-bit monochrome 16-BIT WORDS		
PIXEL ORDER	**n**	**n+1**	**n+2**	**n**	**n+1**	**n+2**	**n**	**n+1**	**n+2**	**n n+1**	**n+2 n+3**	**n+4 n+5**
VRO31	α	α	α	Ye7	Yo7	Ye7	R7	R7	R7	Ya7	Ya7	Ya7
VRO30	R4	R4	R4	Ye6	Yo6	Ye6	R6	R6	R6	Ya6	Ya6	Ya6
VRO29	R3	R3	R3	Ye5	Yo5	Ye5	R5	R5	R5	Ya5	Ya5	Ya5
VRO28	R2	R2	R2	Ye4	Yo4	Ye4	R4	R4	R4	Ya4	Ya4	Ya4
VRO27	R1	R1	R1	Ye3	Yo3	Ye3	R3	R3	R3	Ya3	Ya3	Ya3
VRO26	R0	R0	R0	Ye2	Yo2	Ye2	R2	R2	R2	Ya2	Ya2	Ya2
VRO25	G4	G4	G4	Ye1	Yo1	Ye1	R1	R1	R1	Ya1	Ya1	Ya1
VRO24	G3	G3	G3	Ye0	Yo0	Ye0	R0	R0	R0	Ya0	Ya0	Ya0
VRO23	G2	G2	G2	Ue7	Ve7	Ue7	G7	G7	G7	Yb7	Yb7	Yb7
VRO22	G1	G1	G1	Ue6	Ve6	Ue6	G6	G6	G6	Yb6	Yb6	Yb6
VRO21	G0	G0	G0	Ue5	Ve5	Ue5	G5	G5	G5	Yb5	Yb5	Yb5
VRO20	B4	B4	B4	Ue4	Ve4	Ue4	G4	G4	G4	Yb4	Yb4	Yb4
VRO19	B3	B3	B3	Ue3	Ve3	Ue3	G3	G3	G3	Yb3	Yb3	Yb3
VRO18	B2	B2	B2	Ue2	Ve2	Ue2	G2	G2	G2	Yb2	Yb2	Yb2
VRO17	B1	B1	B1	Ue1	Ve1	Ue1	G1	G1	G1	Yb1	Yb1	Yb1
VRO16	B0	B0	B0	Ue0	Ve0	Ue0	G0	G0	G0	Yb0	Yb0	Yb0
PIXEL ORDER	**n**	**n+1**	**n+2**	**n**	**n+1**	**n+2**	**n**	**n+1**	**n+2**	**n n+1**	**n+2 n+3**	**n+4 n+5**
VRO15	X	X	X	X	X	X	B7	B7	B7	X	X	X
VRO14	X	X	X	X	X	X	B6	B6	B6	X	X	X
VRO13	X	X	X	X	X	X	B5	B5	B5	X	X	X
VRO12	X	X	X	X	X	X	B4	B4	B4	X	X	X
VRO11	X	X	X	X	X	X	B3	B3	B3	X	X	X
VRO10	X	X	X	X	X	X	B2	B2	B2	X	X	X
VRO9	X	X	X	X	X	X	B1	B1	B1	X	X	X
VRO8	X	X	X	X	X	X	B0	B0	B0	X	X	X
VRO7(1)(2)	α	α	α	α	X	α	α	α	α	α	α	α
VRO6 (2)	O/E	O/E	O/E	O/E	O/E	O/E	O/E	O/E	O/E	O/E	O/E	O/E
VRO5 (2)	VGT	VGT	VGT	VGT	VGT	VGT	VGT	VGT	VGT	VGT	VGT	VGT
VRO4 (2)	HGT	HGT	HGT	HGT	HGT	HGT	HGT	HGT	HGT	HGT	HGT	HGT
VRO3	X	X	X	X	X	X	X	X	X	X	X	X
VRO2 (2)	HRF	HRF	HRF	HRF	HRF	HRF	HRF	HRF	HRF	HRF	HRF	HRF
VRO1 (2)	LNQ	LNQ	LNQ	LNQ	LNQ	LNQ	LNQ	LNQ	LNQ	LNQ	LNQ	LNQ
VRO0 (2)	PXQ	PXQ	PXQ	PXQ	PXQ	PXQ	PXQ	PXQ	PXQ	PXQ	PXQ	PXQ

α = keying bit; R, G, B, Y. U and V = digital signals; e = even pixel number; o = odd pixel number; a b c d = consecutive pixels; O/E = odd/even flag

(1) YUV 16-bit format: the keying signal α is defined only for YU time steps. The corresponding YV sample has also to be keyed. The α signal in monochrome mode can be used only in the transparent mode (TTR = 1), in this case Ya = Yb.

(2) Data valid only when transparent mode active (TTR-bit = 1) and VCLK pin connected to LLC/2 clock rate.

Output FIFO register and VRAM output port

The output FIFO register is the buffer between the video data stream and the VRAM data input port. Resized video data are buffered and formatted. 32-, 24- and 16-bit video data modes are supported. The various formats are selected by the bits EFE, FS1 and FS0. VRAM port formats are shown in Tables 2 and 3. The FIFO register capacity is 16 word x 32 bit (for 32-, 24-, or 16-bit video data). The bits LW1 and LW0 can be used to define the position of the first pixel each line in the 32-bit longword formats or to shift the UV sequence to VU in the 16-bit YUV formats (LW1 = 1).

VRAM port inputs are:
VCLK to clock the FIFO register output data and VOEN to enable output data.

VRAM port outputs are:
the HFL flag (half-full flag), the signal INCADR (refer to section "data burst transfer") and the reference signals for pixel and line selection on outputs VRO(7-0) (only for 24- and 16-bit video data formats refer to "transparent data transfer").

VRAM port transfer procedures

Data transfer on the VRAM port can be done asynchroneously controlled by outputs HFL, INCADR and input VCLK (data burst transfer with bit TTR = 0).

Data transfer on the VRAM port can be done synchroneously controlled by output reference signals on outputs VRO(7-0) and a clock rate of LLC/2 on input VCLK (transparent data transfer with bit TTR = 1 and EFE = 1).
The scaling capability of the SAA7186 can be used in various applications.

Data burst transfer mode

Data transfer on the VRAM port is asynchroneously (TTR = 0). This mode can be used for all output formats. Four signals for communication with the external memory are provided.

- HFL flag, the half-full flag of the FIFO output register is raised when the FIFO contains at least 8 data words (HFL = HIGH).
  By setting HFL = 1, the SAA7186 requests a data burst transfer by the external memory controller, that has to start a transfer cycle within the next 32 LLC cycles for 32-bit longword modes (16 LLC cycles for 16- and 24-bit modes). If there are pixels in the FIFO at the end of a line, which are not transferred, the circuit fills up the FIFO register with "fill pixels" until it is half-full and sets the HFL flag to request a data burst transfer. After transfer is done, HFL is used in combination with INCADR to indicate the line increments (Figures 6 and 7).
- INCADR output signal is used in combination with HFL to control horizontal and vertical address generation for a memory controller. The pulse sequence depends on field formats (interlace/ non-interlace or odd/even fields, Figures 6 and 7) and control bits OF (subaddress 00).

  HFL = 1 at the rising edge of INCADR:
  the end of line is reached, request for line address increment
  HFL = 0 at the rising edge of INCADR:
  the end of field/frame is reached, request for line and pixel addresses reset
  (The distance from the last half-full request HFL to the INCADR pulse may be longer than 64 x LLC. The HFL state is defined for minimum 4 x LLC in front of the rising edge of INCADR and minimum 2 x LLC afterwards.)
- VCLK input signal to clock the FIFO register output data VRO(n). New data are placed on the VRO(n) port with the rising edge of VCLK (Fig.5).
- VOEN input enables output data VRO(n).The outputs are in 3-state mode at VOEN = HIGH.
  VOEN changes only when VCLK is LOW. If VCLK pulses are applied during VOEN = HIGH, the outputs remain inactive, but the FIFO register accepts the pulses.

Transparent data transfer mode

Data transfer on the VRAM port can be achieved synchroneously (TTR =1). With a contineous clock rate of LLC/2 on input VCLK, the SAA7186 delivers a contineously processed data stream. Therefore, the extended formats of the VRAM output port have to be selected (bit EFE = 1; Table 3). The reference and gate signals on outputs VRO(6-1) and the LNQ signal are delivered in each field (means scaled and ignored fields). The PXO signal (also VRO0) is only delivered in active fields.
The output signals VRO(7-0) can be used to buffer qualified pre-processed RGB or YUV video data (notice: the YUV data are only valid in qualified time slots). Control output signals in Table 3 are:

α	keying signal of the chroma keyer
O/E	odd/even field bit according to the internal field processing
VGT	vertical gate signal, "1" marks the scaling window in vertical direction from YO to (YO + YS) lines, cut by VS.
HGT	horizontal gate signal, "1" marks horizontal direction from XO to (XO + XS) lines, cut by HREF.
HRF	delay compensated horizontal reference signal.
LNQ	line qualifier signal, active polarity is defined by QPL bit.
PXQ	pixel qualifier signal, active polarity is defined by QPP bit.

Power-on reset

- the FIFO register contents are undefined
- outputs VRO are set to high-impedance state
- output INCADR = HIGH
- output HFL = LOW until the VPE bit is set to "1"
- subaddress "10" is set to 00h and VPE-bit in subaddress "00" is set to zero (Table 4).

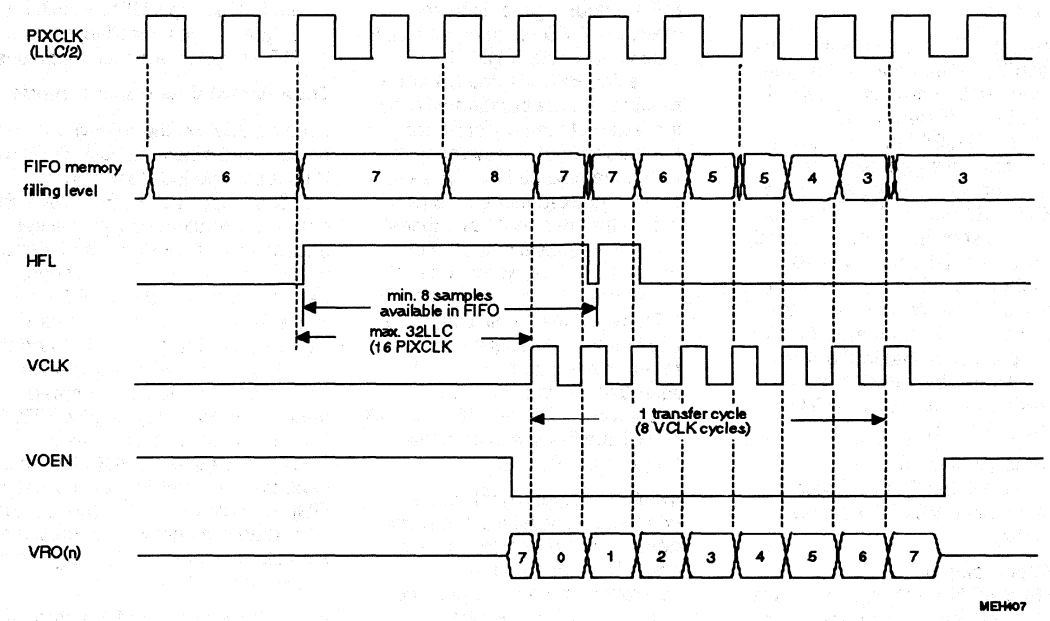


Fig.5 Output port transfer to VRAM at 32-bit data format without scaling. If VCLK cycles occur at VOEN = HIGH, the FIFO register is unchanged, but the outputs VRO(31-0) remain in 3-state position.

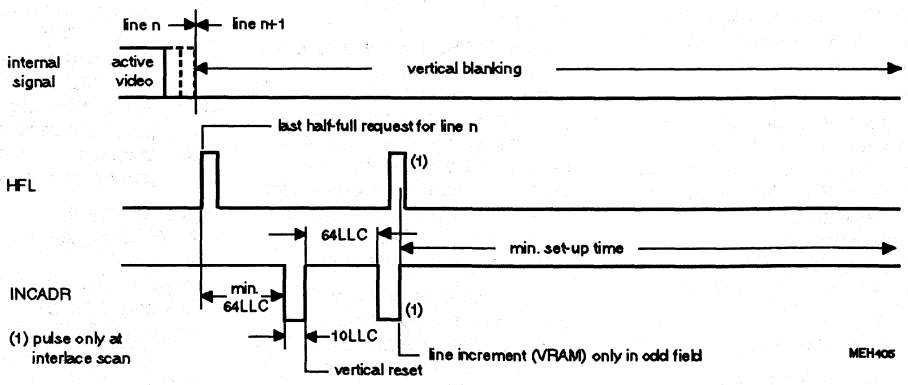


Fig.6 Vertical reset timing to the VRAM.

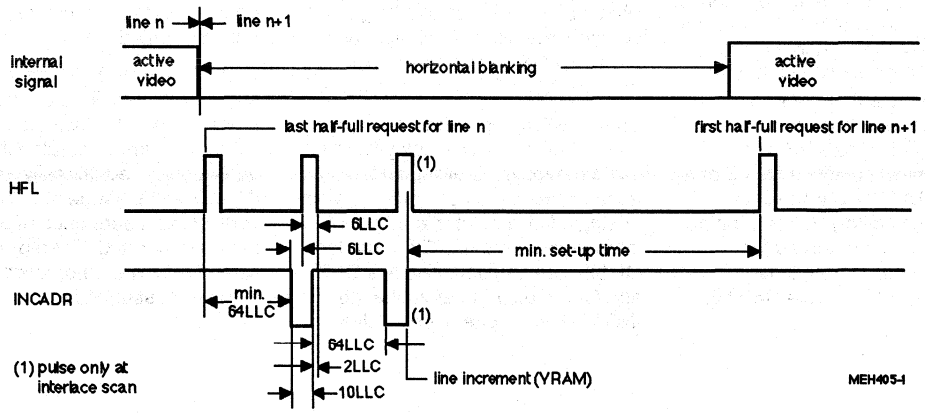


Fig.7 Horizontal increment timing to the VRAM.

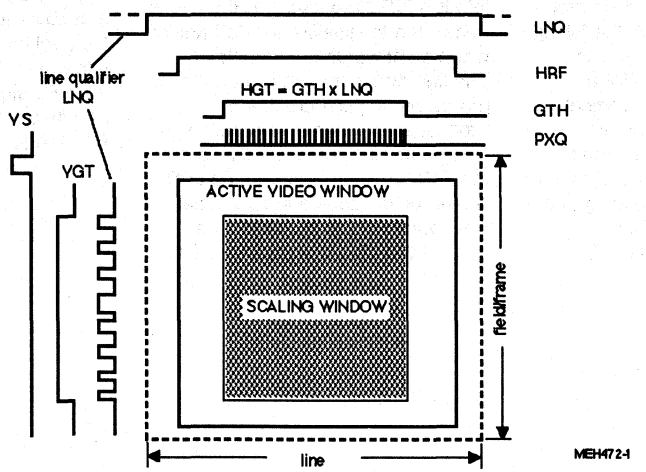


Fig.8 Reference signals for scaling window.

Field processing

The phase of the field sequence (odd/even dependent on inputs HREF and VS) is detected by means of the falling edge of VS. The current field phase is reported in the status byte by the OEF bit (Table 5). OEF bit can be stable 0 or 1 for non-interlaced input frames or non standard input signals VS and/or HREF (nominal condition for VS and HREF – SAA7191 B with active vertical noise limiter). A free-running odd/even flag is generated for internal field processing if the detection reports a stable OEF bit.

The POE bit (subaddress 0B) can be used to change the polarity of the internal flag (in case of non-standard VS and HREF signals) to control the phase of the free-running flag, and to compensate mis-detections. Thus, the SAA7186 can be used under various VS/HREF timing conditions.

The SAA7186 operates on fields. To support progressive displays and to avoid movement blurring and artifacts, the circuit can process both or single fields of interlaced or non-interlaced input data. Therefore the OF bits can be used. The bits OF1 and OF0 (Table 6) determine the INCADR/HFL generation in "data burst transfer mode". One of the fields (odd or even) is ignored when OF1 = 1; then no line increment sequence (INCADR/HFL) is generated, the vertical reset pulse is only generated.

With OF1 = OF0 = 0 the circuit supports correct interlaced data storage. Two INCADR/HFL sequences are generated in each qualified line; additionally an INCADR/HFL sequence after the vertical reset sequence of an odd field is generated. Thereby, the scaled lines are automatically stored in the right sequence.

8. OPERATION CYCLE

The operation is synchronized by the input field. The cycle is specified in the flow chart (Fig.9).
The circuit is inactive after power-on reset, VPO is 0 and the FIFO control is set "empty". The internal control registers are updated with the falling edge of VS signal. The circuit is switched active and waits for a transmission of VS and a vertical reset sequence to the memory controller. Afterwards, the circuit waits for the beginning of a scaling or bypass region. The processing of a current line is finished when a vertical sync pulse appears. The circuit performs a coefficient update and generates a new vertical reset (if it is still active).

Line processing starts when a line is decided to be active, the circuit starts to scale it. Active pixels are loaded into the FIFO register. An HFL flag is generated to initialize a data transfer when eight words are completed. The line end is reached when the programmed pixel number is processed or when a horizontal sync pulse occurs. If there are pixels in the FIFO register, it is filled up until it is half-full to cause a data transfer. Horizontal increment pulses are transmitted after this data transfer.

Remarks:
The SAA7186 will always wait for the HREF/VS pulse before the line increment/vertical reset sequence is performed.
After each line/field, the FIFO control is set to empty when INCADR/HFL sequence is transmitted.
No additional actions are necessary if the memory controller has ignored the HFL signal. There is no need to handle overflow/underflow of the FIFO register.

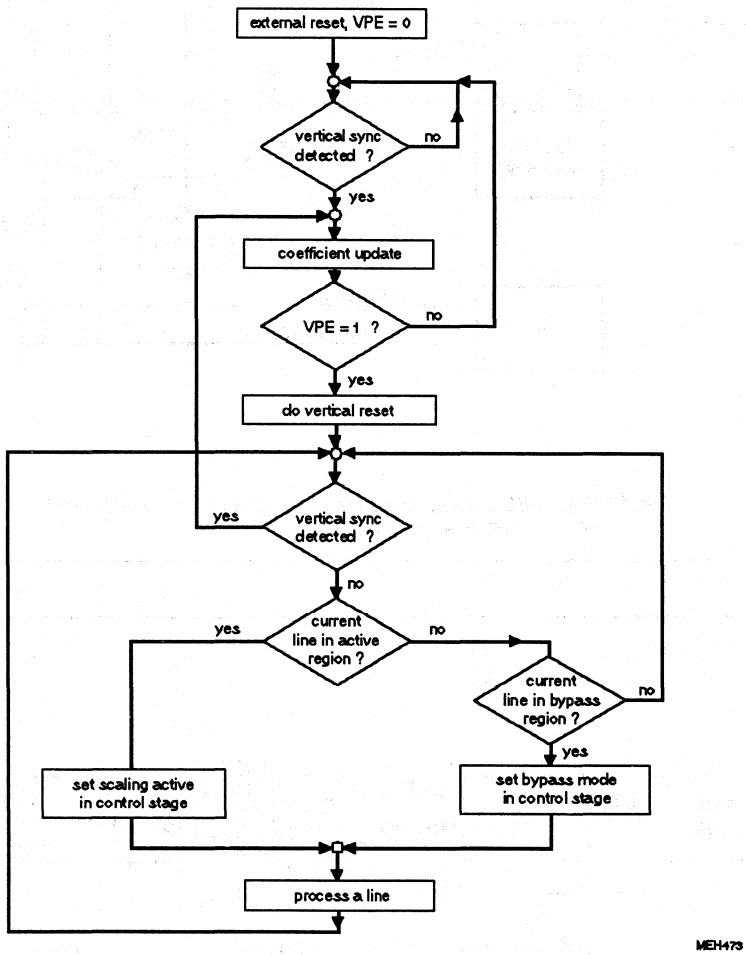


Fig.9 Operation cycle

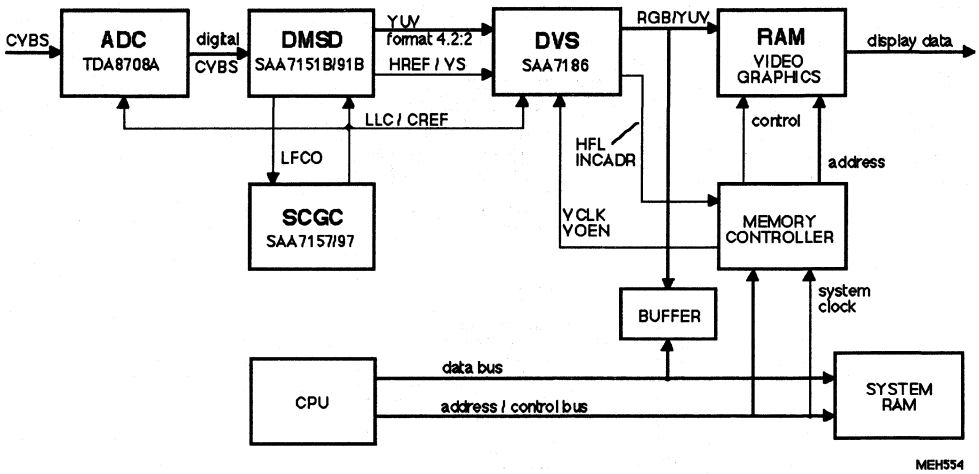


Fig.10 SAA7186 system configuration in Data Burst Transfer Mode (TTR = , VCLK = continuous).

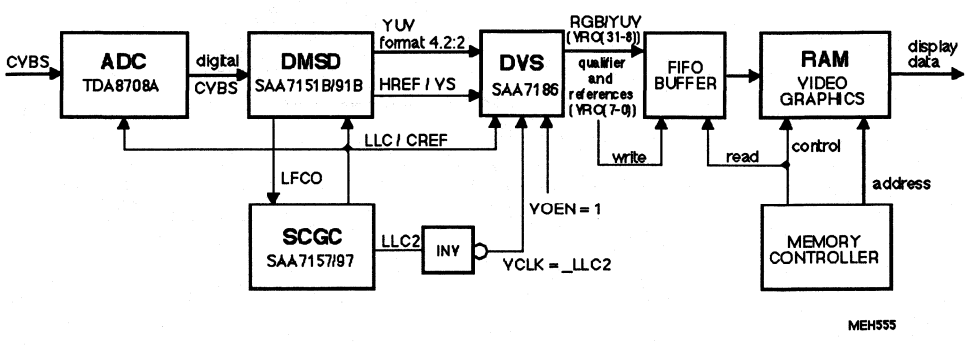


Fig.11 SAA7186 system configuration in Transparent Data Transfer Mode (TTR = 1, EFE = 1, VCLK = continuous (_LLC2)).

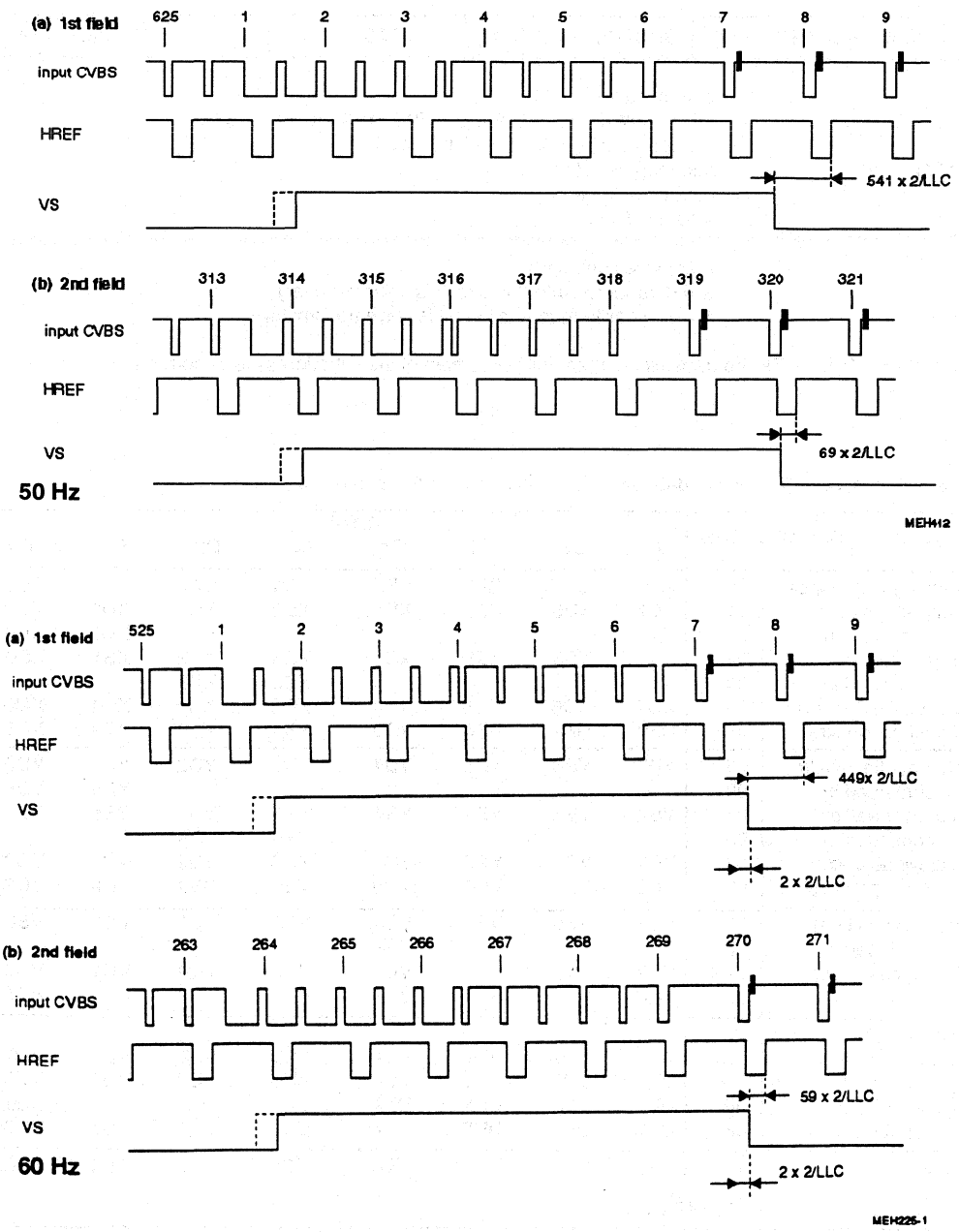


Fig.12 VS timing for video input source SAA7191B.

9. I²C-BUS FORMAT

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA0	A		DATAn	A	P

S = start condition
SLAVE ADDRESS = **1011 100X** (IICSA = LOW) **or 1011 110X** (IICSA = HIGH)
A = acknowledge, generated by the slave
SUBADDRESS* = subaddress byte (Table 4)
DATA = data byte (Table 4)
P = stop condition

X = read/write control bit
X = 0, order to write (the circuit is slave receiver)
X = 1, order to read (the circuit is slave transmitter)

* If more than 1 byte DATA are transmitted, then auto-increment of the subaddress is performed.

Table 4 I²C-bus; subaddress and data bytes for writing (X in address byte = 0).

FUNCTION	SUBADDRESS	DATA D7	D6	D5	D4	D3	D2	D1	D0	DF*
Formats and sequence	00	RTB	OF1	OF0	VPE	LW1	LW0	FS1	FS0	tbf
Output data pixel/line	01	XD7	XD6	XD5	XD4	XD3	XD2	XD1	XD0	
continued in	04							XD9	XD8	
Input data pixel/line	02	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	
continued in	04					XS9	XS8			
Horizontal window start	03	XO7	XO6	XO5	XO4	XO3	XO2	XO1	XO0	
Pixel decimation filter	04	HF2	HF1	HF0	XO8	XS9	XS8	XD9	XD8	
Output data lines/field	05	YD7	YD6	YD5	YD4	YD3	YD2	YD1	YD0	
continued in	09							YD9	YD8	
Input data lines/field	06	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	
continued in	09					YS9	YS8			
Vertical window start	07	YO7	YO6	YO5	YO4	YO3	YO2	YO1	YO0	
AFS/vertical processing	08	AFS	VP1	VP0	YO8	YS9	YS8	YD9	YD8	
Vertical bypass start	09	VS7	VS6	VS5	VS4	VS3	VS2	VS1	VS0	
continued in	0B				VS8					
Vertical bypass count	0A	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0	
continued in	0B	TCC	0	0	VS8	0	VC8	0	POE	
Chroma keying										
lower limit for V	0C	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0	
upper limit for V	0D	VU7	VU6	VU5	VU4	VU3	VU2	VU1	VU0	
lower limit for U	0E	UL7	UL6	UL5	UL4	UL3	UL2	UL1	UL0	
upper limit for U	0F	UU7	UU6	UU5	UU4	UU3	UU2	UU1	UU0	
Byte 10**	10	0	0	YLIM	MCT	QPL	QPP	TTR	EFE	
Unused	11 to 1F									

*) Default register contents fill in by hand
**) Byte 10 is set to 00h after power-on reset.

Table 5 I²C-bus status byte (X in address byte = 1)

FUNCTION		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
status byte		ID3	ID2	ID1	ID0	0	0	OEF	SVP

Function of status bits:

ID3 to ID0 Software version of SAA7186 compatible with

ID3	ID2	ID1	ID0	version
0	0	0	1	1

OEF Identification of field sequence dependent on inputs HREF and VS:
0 = even field detected; 1 = odd field detected

SVP State of VRAM port:
0 = inputs HFL and INCADR inactive;
1 = inputs HFL and INCADR active.

Table 6 Function of the register bits of Table 4

"00" RTB — ROM table bypass switch: 0 = anti-gamma ROM active; 1 = table is bypassed

OF1 to OF0 — Set output field mode:

OF1	OF0	field mode DVS process
0	0	both fields for interlaced storage
0	1	both fields for non-interlaced storage
1	0	odd fields only (even fields ignored) for non-interlaced storage
1	1	even fields only(odd fields ignored) for non-interlaced storage

VPE — VRAM port outputs enable: 0 = HFL and INCADR inactive; VRO outputs in 3-state position (HFL = LOW, INCADR = HIGH)
1 = HFL and INCADR enabled; VRO outputs dependent on VOEN

LW1 to LW0 — First pixel position in VRO data for FS1 = 0; FS0 = 0 (RGB) and FS1 = 0; FS0 = 1(YUV):

LW1	LW0	31 to 24	23 to 16	15 to 8	7 to 0	
0	0	pixel 0	pixel 0	pixel 1	pixel 1	)
0	1	pixel 0	pixel 0	pixel 1	pixel 1	)
1	0	black	black	pixel 0	pixel 0	) EFE = 0, TRR = 0
1	1	black	black	pixel 0	pixel 0	)

First pixel position in VRO data for FS1 = 1; FS0 = 1 (monochrome):

LW1	LW0	31 to 24	23 to 16	15 to 8	7 to 0	
0	0	pixel 0	pixel 1	pixel 2	pixel 3	)
0	1	black	pixel 0	pixel 1	pixel 2	)
1	0	black	black	pixel 0	pixel 1	) EFE = 0, TRR = 0
1	1	black	black	black	pixel 0	)
0	0	pixel 0	pixel 1	X	X	)
0	1	black	pixel 0	X	X	) EFE = 1, TRR = 0;
1	0	pixel 0	pixel 1	X	X	) LW only effects the
1	1	black	pixel 0	X	X	) greyscale formar

FS1 to FS0

FIFO output register format select (EFE- bit see "10"):

EFE	FS1	FS0	output format (Tables 2 and 3)
0	0	0	RGB 5-5-5 + alpa; 2x16-bit/pixel; 32-bit word length; RGB matrix on, VRAM output format
0	0	1	YUV 4:2:2; 2x16-bit/pixel; 32-bit word length; RGB matrix off, VRAM output format
0	1	0	YUV 4:2:2; video test mode; 1x16-bit/pixel;16-bit word length; RGB matrix off, optional output format
0	1	1	monochrome mode; 4x8-bit/pixel; 32-bit word length; RGB matrix off, VRAM output format
1	0	0	RGB 5-5-5 + alpa; 1x16-bit/pixel; 16-bit word length; RGB matrix on, VRAM output + transparent format
1	0	1	YUV 4:2:2 + alpa; 1x16-bit/pixel; 16-bit word length; RGB matrix off, VRAM output + transparent format
1	1	0	RGB 8-8-8 + alpa; 1x24-bit/pixel; 24-bit word length; RGB matrix on, VRAM output + transparent format
1	1	1	monochrome mode; 2x8-bit/pixel; 16-bit word length; RGB matrix off, VRAM output + transparent format

"01 and 04"
XD9 to XD0

Pixel number per line (straight binary) on output (VRO):
00 0000 0000 to 11 1111 1111 (number of XS pixels as a maximum)

"02 and 04"
XS9 to XS0

Pixel number per line (straight binary) on inputs (YIN and UVIN):
00 0000 0000 to 11 1111 1111 (number of input pixels per line as maximum)

"03 and 04"
XO8 to XO0

Horizontal start position (straight binary) of scaling window (take care of active pixel number per line).

start with 1st pixel after HREF rise = 0 0001 0000 to 1 1111 1111 (010 to 1FF)

window start and window end may be cut by internal delay compensated HREF = 0 phase. XO has to be matched to the internal processing delay to get full scaling range

"04"
HF2 to HF0

Horizontal decimation filter (Figures 13 and 14):

HF2	HF1	HF0	taps	filter
0	0	0	2	filter 1 $(1/2\ (1 + z^{-1}))$
0	0	1	3	filter 2 $(1/4\ (1 + 2z^{-1} + z^{-2}))$
0	1	0	5	filter 3 $(1/8\ (1 + 2z^{-1} + 2z^{-2} + 2z^{-3} + z^{-4}))$
0	1	1	9	filter 4 $(1/16\ (1 + 2z^{-1} + 2z^{-2} + 2z^{-3} + 2z^{-4} + 2z^{-5} + 2z^{-6} + 2z^{-7} + z^{-8}))$
1	0	0	1	filter bypassed
1	0	1	1	filter bypassed + delay in Y channel of 1T
1	1	0	8	filter 5 $(1/16\ (1 + 3z^{-1} + 3z^{-2} + z^{-3} + z^{-4} + 3z^{-5} + 3z^{-6} + z^{-7}))$
1	1	1	4	$(1/8\ (1 + 3z^{-1} + 3z^{-2} + z^{-3}))$

"05 and 08"
YD9 to YD0

Line number per output field (straight binary):
00 0000 0000 to 11 1111 1111 (number of YS lines as a maximum)

"06 and 08" YS9 to YS0	Line number per input field (straight binary): 00 0000 0000 0 line 11 1111 1111 1023 lines (maximum = number of lines/field – 3)
"07 and 08" YO8 to YO0	Vertical start of scaling window. "0" equals 3rd line after rising slope of VS input signal. Take care of active line number per field (straight binary). 0 0000 0000 start with 3rd line after the rising slope of VS 0 0000 0011 start with 1st line after the falling slope of nominal VS (SAA7151B/91B) 1 1111 1111 511 + 3 lines after the rising slope of VS (maximum value)
"08" AFS	Adaptive filter switch: 0 = off; use VP1, VP0 and HF2 to HF0 bits 1 = on; filter characteristics are selected by the scaler
VP1 to VP0	Vertical data processing VP1 VP0 | processing 0 0 | bypassed 0 1 | delay of one line $H(z) = z^{-H}$ 1 0 | vertical filter 1: $(H(z) = 1/2 (1 + z^{-H}))$ 1 1 | vertical filter 2: $(H(z) = 1/4 (1 + 2z^{-H} + z^{-2H}))$
"09 and 0B" VS8 to VS0	Vertical bypass start, sets begin of the bypass region (straight binary). Scaling region overrides bypass region (YO bits): 0 0000 0000 start with 3rd line after the rising slope of VS 0 0000 0011 start with 1st line after the falling slope of nominal VS (SAA7151B/91B) 1 1111 1111 511 + 3 lines after the rising slope of VS (maximum value)
"0A and 0B" VC8 to VC0	Vertical bypass count, sets length of bypass region (straight binary): 0 0000 0000 0 line length 1 1111 1111 511 lines length (maximum = number of lines/field – 3)
TCC	Two´s complement input data select (U, V): 0 = binary input data 1 = two`complement input data
POE	Polarity, internally detected odd/even flag O/E: 0 = flag unchanged; 1 = flag inverted
"0C" VL7 to VL0	Set lower limit for V colour-difference signal (8 bit; two´s complement): 1000 0000 as maximum negative value = –128 signal level 0000 0000 limit = 0 0111 1111 as maximum positive value = +127 signal level
"0D" VU7 to VU0	Set upper limit for V colour-difference signal (8 bit; two´s complement): 1000 0000 as maximum negative value = –128 signal level 0000 0000 limit = 0 0111 1111 as maximum positive value = +127 signal level

"0E" UL7 to UL0	Set lower limit for U colour-difference signal (8 bit; two´s complement): 1000 0000 as maximum negative value = –128 signal level 0000 0000 limit = 0 0111 1111 as maximum positive value = +127 signal level
"0F" UU7 to UU0	Set upper limit for U colour-difference signal (8 bit; two´s complement): 1000 0000 as maximum negative value = –128 signal level 0000 0000 limit = 0 0111 1111 as maximum positive value = +127 signal level
"10" YLIM	Y Limiter (YUV modes only) 0 = Y limited according to CCIR 601 1 = Y not limited
MCT	Monochrome and two´s complement output data select: 0 = inverse grayscale luminance (if grayscale is selected by FS bits) or straight binary U, V data output 1 = non-inverse monochrome luminance (if grayscale is selected by FS bits) or two`complement U, V data output
QPL	Line qualifier polarity flag : 0 = LNQ is active-LOW (pin 1 and on VRO1, pin 99); 1 = LNQ is active-HIGH
QPP	Pixel qualifier polarity flag : 0 = PXQ is active-LOW (VRO0, pin 100); 1 = PXQ is active-HIGH
TTR	Transparent data transfer: 0 = normal operation (VRAM protocol valid,) 1 = FIFO register transparent (output FIFO in shift register mode)
EFE	Extended formats enable, FS-bits in subaddress "00"

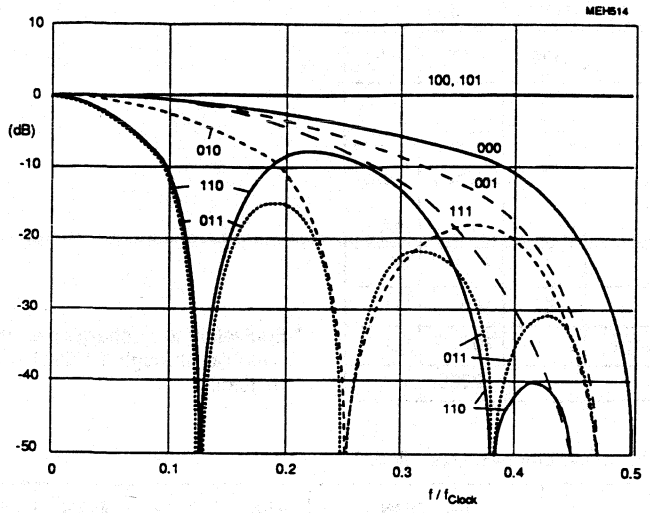


Fig.13 Horizontal frequency characteristic of luminance signal (Y) dependent on HF2 to HF0 bits (subaddress 04).

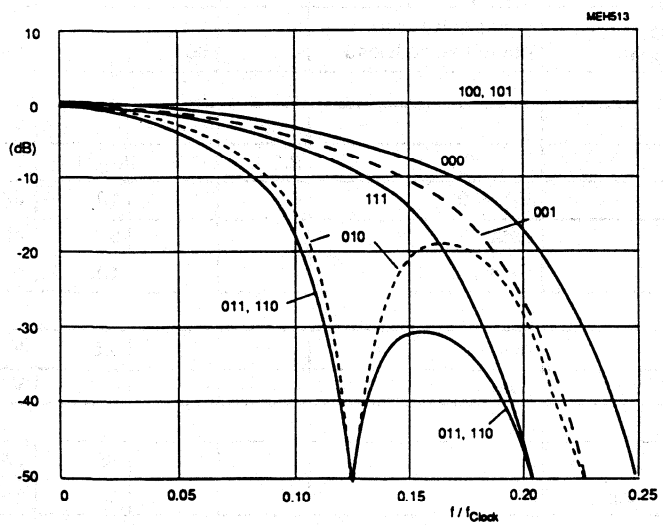


Fig.14 Horizontal frequency characteristic of chrominance signals (UV) without UV interpolation dependent on HF2 to HF0 bits (subaddress 04).

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

10. LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (pins 5, 14, 26, 40, 55, 67, 76 and 91)	–0.5	6.5	V
V_I	DC input voltage on all pins	–0.5	V_{DD}	V
I_{DD}	supply current (pins 5, 14, 26, 40, 55, 67, 76 and 91)	-	70	mA
P_{tot}	total power dissipation	0	1	W
T_{stg}	storage temperature range	–65	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling* for all pins	-	±2000	V

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

11. DC CHARACTERISTICS

V_{DD1} to V_{DD8} = 4.5 to 5.5 V; T_{amb} = 0 to 70 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage range (pins 5, 14, 26, 40, 55, 67, 76 and 91)		4.5	5	5.5	V
I_P	total supply current ($I_{DD1} + I_{DD2} + I_{DD3}$ $I_{DD4} + I_{DD5} + I_{DD6} + I_{DD7} + I_{DD8}$)	inputs LOW and outputs without load	-	80	-	mA
Data and control inputs						
V_{IL}	input voltage LOW		–0.5	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{DD}+0.5	V
I_{LI}	input leakage current	V_{IL} = 0	-	-	10	µA
C_I	input capacitance	data	-	-	8	pF
		clocks	-	-	10	pF
Data and control outputs						
V_{OL}	output voltage LOW	note 1	-	-	0.6	V
V_{OH}	outputt voltage HIGH	note 1	2.4	-	-	V
3-state outputs						
$I_{O\,off}$	high-impedance output current		-	-	±5	µA
C_O	high-impedance output capacitance		-	-	8	pF
I^2C-bus, SDA and SCL (pins 44 and 45)						
V_{IL}	input voltage LOW		–0.5	-	1.5	V
V_{IH}	input voltage HIGH		3	-	V_{DD}+0.5	V
$I_{44, 45}$	input current		-	-	±10	µA
I_{ACK}	output current on pin 44	acknowledge	3	-	-	mA
V_{OL}	output voltage at acknowledge	I_{44} = 3 mA	-	-	0.4	V

12. AC CHARACTERISTICS

V_{DD1} to V_{DD8} = 4.5 to 5.5 V; T_{amb} = 0 to 60 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
LLC timing (pin 36)		Fig.11				
t_{LLC}	cycle time		31	-	45	ns
t_p	pulse width (duty factor)	$t_{LLC\,H} / t_{LLC}$	40	50	60	%
t_r	rise time		-	-	5	ns
t_f	fall time		-	-	6	ns
Input data and CREF timing		Fig.15				
t_{SU}	setup time		11	-	-	ns
t_{HD}	hold time		3	-	-	ns
VCLK timing (pin 51)		Fig.16				
t_{VCLK}	VRAM port clock cycle time	note 2	50	-	200	ns
$t_{p\,L}$, $t_{p\,H}$	LOW and HIGH times	note 3	17	-	-	ns
t_r	rise time		-	-	5	ns
t_f	fall time		-	-	6	ns
Output data and reference signal timing		Figures 15 and 16				
C_L	load capacitance	VRO outputs	15	-	40	pF
		other outputs	7.5	-	25	pF
t_{OH}	VRO data hold time	C_L = 10 pF; note 4	0	-	-	ns
t_{OHL}	related to LLC (INCADR, HFL)	C_L = 10 pF; note 5	0		-	ns
t_{OHV}	related to VCLK (HFL)	C_L = 10 pF; note 5	0		-	ns
t_{OD}	VRO data delay time	C_L = 40 pF; note 4	-	-	25	ns
t_{ODL}	related to LLC (INCADR, HFL)	C_L = 25 pF; note 5	-	-	60	ns
t_{ODV}	related to VCLK (HFL)	C_L = 25 pF; note 5	-	-	60	ns
t_D	output disable time to 3-state	C_L = 40 pF; note 6	-	-	40	ns
t_E	output enable time from 3-state	C_L = 40 pF; note 6	-	-	40	ns
$t_{HFL\,VOE}$	HFL maximum response time	VRAM port enabled	-	-	810	ns
$t_{HFL\,VCLK}$	HFL maximum response time	HFL set at beginning of VCLK burst	-	-	840	ns

Notes to the caracteristics

1. Levels are measured with load circuit. VRO outputs with 1.2 kΩ in parallel to 25 pF at 3 V (TTL load).
2. Maximum t_{VCLK} = 200 ns for test mode only. The applicable maximum cycle time depends on data format, horizontal scaling and input data rate.
3. Measured at 1,5 V level; $t_{p\,L}$ may be unlimited.
4. Timings of VRO refer to the rising edge of VLCK.
5. The timing of INCADR refers to LLC; the rising edge of HFL always refers to LLC. During a VRAM transfer is the falling edge of HFL generated by VCLK. Both edges of HFL refer to LLC during horizontal increment and vertical reset cycles.
6. Asynchronous signals with timing refering to the 1.5 V switching point of VOEN input signal (pin 50).

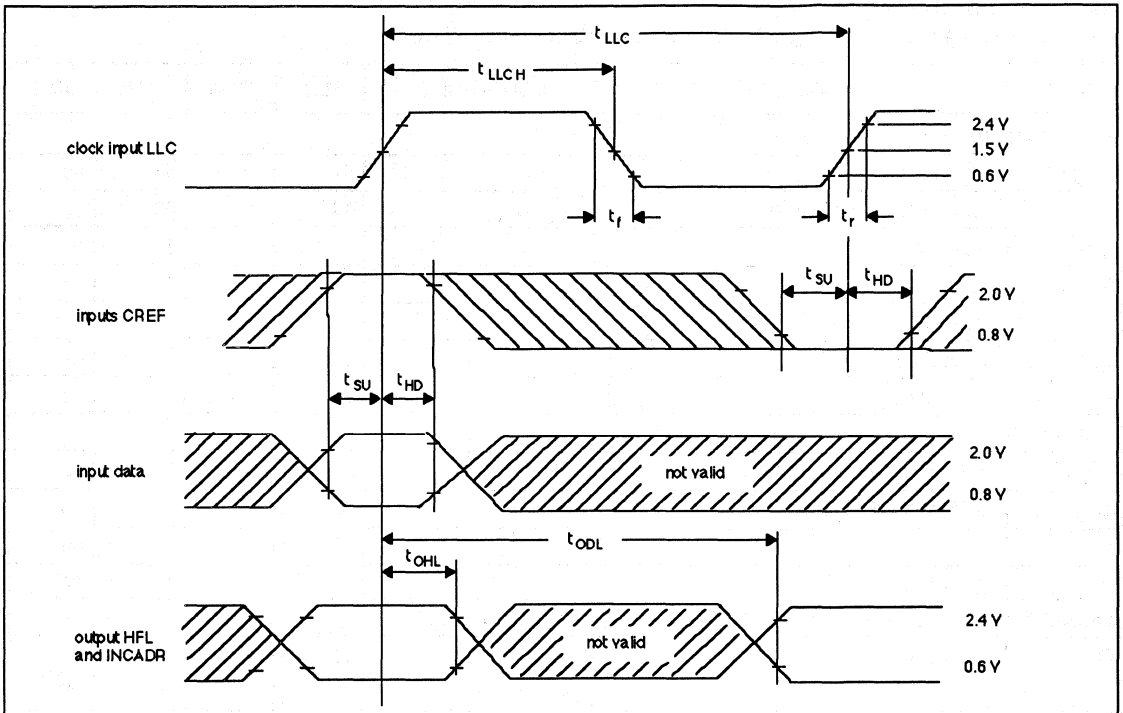


Fig.15 Data input timing (LLC).

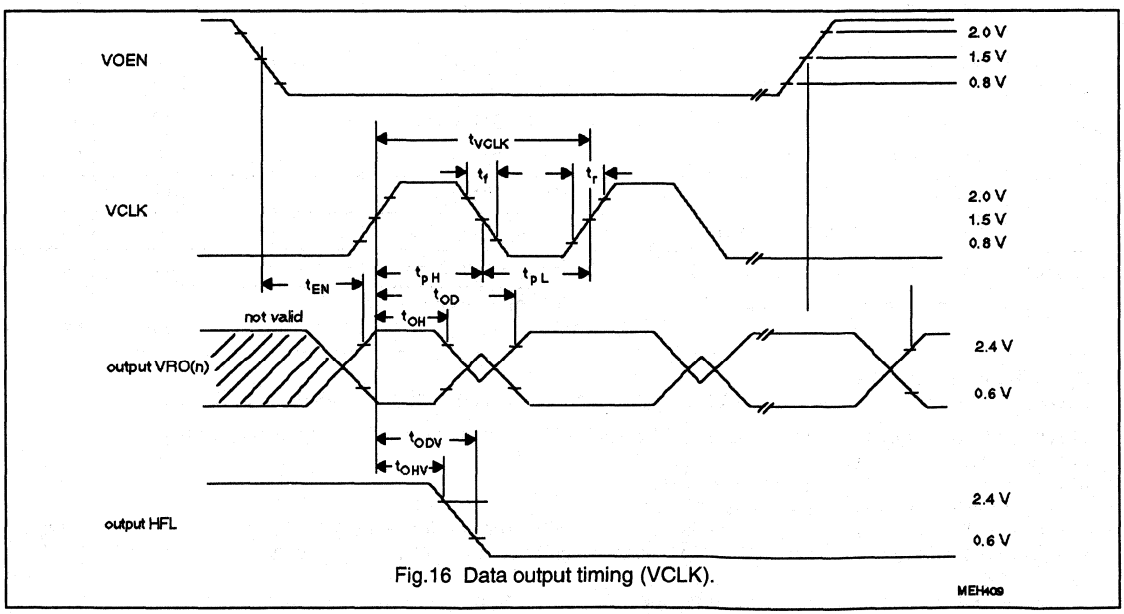


Fig.16 Data output timing (VCLK).

13. PROCESSING DELAYS

PORTS	DELAY IN LLC	REMARKS`
YIN to VRO	58	in transparent mode only
UVIN to VRO	58	in transparent mode only
HREF to VRO	58	in transparent mode only

14. PROGRAMMING EXAMPLE

Slave address byte is B8h at pin IICSA = 0 (or BCh at pin IICSA = +5 V).
This example shows the setting via I²C-bus for the processing of a picture segment at 1:1 horizontal and vertical scale.

Values in brackets [..]:
If no scaling or panning is wanted,
the parameters XD, XS, YD and YS should be set to the maximum value 3FFh.
the parameters XO and YO should be set to the minimum value 000h.
(in this case, HREF and VS from external define the SAA7186 processing window).

SUBADDR. (hex)	BITS	FUNCTION	VALUE (hex)	COMMENT
00	RTB, OF(1:0), VPE, LW(1:0), FS(1:0),	ROM table control and field sequence processing; VRAM port enable; output format select	11	(1)
01	XD(7:0)	LSB´s output pixel/line	80 [FF]	384 pixels out
02	XS(7:0)	LSB´s input pixel/line	80 [FF]	384 pixels in
03	XO(7:0)	LSB´s for horizontal window start	10 [00]	1st pixel after HREF = 1
04	HF(2:0), XO(8), XS(9, 8), XD(9, 8)	horizontal filter select and MSB´s of subaddresses 01, 02, 03	85 [8F]	horizontal filter bypassed
05	YD(7:0)	LSB´s output lines/field	90 [FF]	144 lines out
06	YS(7:0)	LSB´s input lines/field	90 [FF]	144 lines in
07	YO(7:0)	LSB´s vertical window start	03 [00]	1st line after VS = 0; (2)
08	AFS, VP(1:0), YO(8), YS(9, 8), YD(9, 8)	adaptive and vertical filter select; MSB´s of subaddresses 05, 06, 07	00 [FF]	no adaptive select vertical filter bypassed
09	VS(7:0)	LSB´s vertical bypass start position	00	not bypassed
0A	VC(7:0)	LSB´s vertical bypass lines/field	00	region
0B	VS(8), VC(8), TCC, POE	MSB´s of subaddresses 09, 0A; UV input data representation and odd/even polarity switch	00	defined; (3) (4)
0C	VL(7:0)	UV keyer: lower limit V (R-Y)	00	) keying is switched off
0D	VU(7:0)	UV keyer: upper limit V (R-Y)	FF	) by VU < VL
0E	UL(7:0)	UV keyer: lower limit U (B-Y)	00	-
0F	UU(7:0)	UV keyer: upper limit U (B-Y)	00	-
10	MCT, QPP, QPL, TTR, EFE	Y or UV output data representation, output data transfer mode, pixel/ line qualifier polarity.	00	(5)

Notes to the programming examples

(1) RTB = 0 ROM table is active (only for RGB formats)
OF = 00 SAA7186 processes the both fields for interlaced display
VPE = 1 VRAM port is enabled

LW = 00 longword position of first pixel in each output line = 0
FS = 01 16-bit 4:2:2 YUV output format is selected

(2) for nominal VS length of 6 x H-period (input SAA7191B respectively SAA7151B with active VNL)

(3) TTC = 0 straight binary UV input data expected

(4) odd/even polarity unchanged - can be used to change the field sequence if phase relations between HREF and VS are not according to SAA7191B respectively SAA7151B specification

(5) MCT = 0 when EFE, FS = 001h: UV output data are straight binary
QPP = 0 the pixel qualifier PXQ is "0"-active (if TTR, EFE = 1)

QPL = 0 line qualifier LNQ is "0"-active (if TTR, EFE = 1)
TTR = 0 VRAM port is set to data burst transfer
EFE = 0 32-bit longword formats selected.

Digital video encoder (DENC2-SQ) SAA7187

FEATURES

- CMOS 5 V device
- Digital PAL/NTSC encoder
- System pixel frequency selectable for 12.27 MHz (60 Hz fields) or 14.75 MHz (50 Hz fields)
- 24-bit wide YUV input port or
- 16-bit wide YUV input port or
- Input data format Cb, Y, Cr, etc. (CCIR 656)
- I²C-bus control port
- MPU parallel control port
- Encoder can be master or slave
- Programmable horizontal and vertical input synchronization phase
- Programmable horizontal sync output phase
- OSD overlay with Look-Up Tables (LUTs) 8 × 3 bytes
- Line 21 Closed Caption encoder
- Cross-colour reduction
- DACs operating at twice oversampling with 10-bit resolution
- Controlled rise/fall times of output syncs and blanking
- Down-mode of DACs
- CVBS and S-Video output simultaneously
- PLCC68 package.

GENERAL DESCRIPTION

The SAA7187 encodes digital YUV video data to an NTSC, PAL CVBS or S-Video signal.

The circuit accepts differently formatted YUV data with 640 or 768 active pixels per line. It includes a sync/clock generator and on-chip Digital-to-Analog Converters (DACs).

The circuit is compatible to the DIG-TV2 chip family (Square Pixel).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage	4.75	5.0	5.25	V
V_{DDD}	digital supply voltage	4.5	5.0	5.5	V
I_{DDA}	analog supply current	–	50	55	mA
I_{DDD}	digital supply current	–	175	210	mA
V_i	input signal voltage levels	TTL compatible			
$V_{o(p-p)}$	analog output signal voltages Y, C and CVBS without load (peak-to-peak value)	–	2	–	V
R_L	load resistance	80	–	–	Ω
ILE	LF integral linearity error	–	–	±2	LSB
DLE	LF differential linearity error	–	–	±1	LSB
T_{amb}	operating ambient temperature	0	–	+70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7187	PLCC68	plastic leaded chip carrier; 68 leads	SOT188-2

BLOCK DIAGRAM

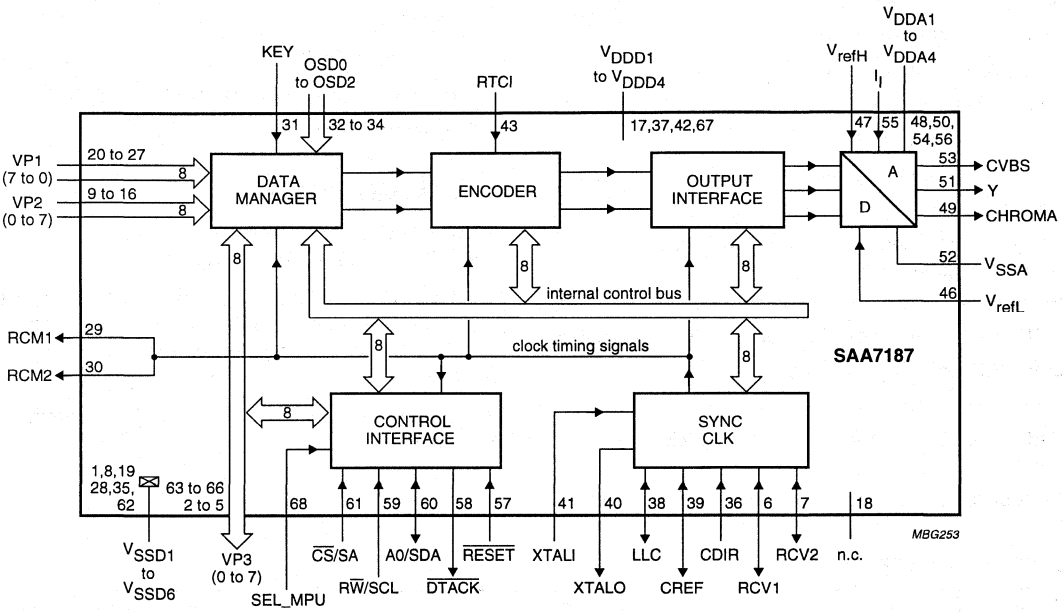


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{SSD1}	1	digital ground 1
VP3(4)	2	Upper 4 bits of the Video Port VP3. If pin 68 (SEL_MPU) is HIGH, this is the data bus of the parallel MPU interface. If it is LOW, there can be multiplexed UV lines (422) or the U signal (444) of the Video input.
VP3(5)	3	
VP3(6)	4	
VP3(7)	5	
RCV1	6	Raster Control 1 for Video port. Depending on the synchronization mode, this pin receives/provides a VS/FS/FSEQ signal.
RCV2	7	Raster Control 2 for Video port. Depending on the synchronization mode, this pin receives/provides an HS/HREF/CBL signal.
V_{SSD2}	8	digital ground 2
VP2(0)	9	Video Port VP2. In 444 input mode, this is input for the V-signal.
VP2(1)	10	
VP2(2)	11	
VP2(3)	12	
VP2(4)	13	
VP2(5)	14	
VP2(6)	15	
VP2(7)	16	
V_{DDD1}	17	digital supply voltage 1
n.c.	18	reserved, do not connect
V_{SSD3}	19	digital ground 3
VP1(7)	20	Video Port VP1. This is an input for CCIR 656 compatible, multiplexed video data, or during other input modes, this is the Y-signal.
VP1(6)	21	
VP1(5)	22	
VP1(4)	23	
VP1(3)	24	
VP1(2)	25	
VP1(1)	26	
VP1(0)	27	
V_{SSD4}	28	digital ground 4
RCM1	29	Raster Control Master 1. This pin provides a VS/FS/FSEQ signal.
RCM2	30	Raster Control Master 2. This pin provides a programmable HS pulse.
KEY	31	Key signal for OSD. It is active HIGH.
OSD0	32	On-Screen Display data. This is the index for the internal OSD look-up table.
OSD1	33	
OSD2	34	
V_{SSD5}	35	digital ground 5
CDIR	36	Clock direction. If the CDIR input is HIGH, the circuit receives a clock signal, otherwise LLC and CREF are generated by the internal crystal oscillator.
V_{DDD2}	37	digital supply voltage 2

SYMBOL	PIN	DESCRIPTION
LLC	38	Line-Locked Clock. This is the 24.54 MHz or 29.5 MHz master clock for the encoder. The direction is set by the CDIR pin.
CREF	39	Clock Reference signal. This is the clock qualifier for DIG-TV2 compatible signals.
XTALO	40	Crystal oscillator output (to crystal).
XTALI	41	Crystal oscillator input (from crystal). If the oscillator is not used, this pin should be connected to ground.
V_{DDD3}	42	digital supply voltage 3
RTCI	43	Real Time Control Input. If the clock is provided by an SAA7191B, RTCI should be connected to the RTCO pin of the decoder to improve the signal quality.
AP	44	Test pin. Connected to digital ground for normal operation.
SP	45	Test pin. Connected to digital ground for normal operation.
V_{refL}	46	Lower reference voltage input for the DACs.
V_{refH}	47	Upper reference voltage input for the DACs.
V_{DDA1}	48	Analog supply voltage 1 for the DACs and output amplifiers.
CHROMA	49	Analog output of the chrominance signal.
V_{DDA2}	50	Analog supply voltage 2 for the DACs and output amplifiers.
Y	51	Analog output of the luminance signal.
V_{SSA}	52	Analog ground for the DACs and output amplifiers.
CVBS	53	Analog output of the CVBS signal.
V_{DDA3}	54	Analog supply voltage 3 for the DACs and output amplifiers.
I_I	55	Current input for the output amplifiers, connect via a 15 kΩ resistor to V_{DDA}.
V_{DDA4}	56	Analog supply voltage 4 for the DACs and output amplifiers.
$\overline{RESET}$	57	Reset input, active LOW. After reset is applied, all outputs are in 3-state input mode. The I²C-bus receiver waits for the START condition.
$\overline{DTACK}$	58	Data acknowledge output of the parallel MPU interface, active LOW, otherwise high impedance.
R$\overline{W}$/SCL	59	If pin 68 (SEL_MPU) is HIGH, this is the read/write signal of the parallel MPU interface, otherwise it is the I²C-bus serial clock input.
A0/SDA	60	If pin 68 (SEL_MPU) is HIGH, this is the address signal of the parallel MPU interface, otherwise it is the I²C-bus serial data input/output.
$\overline{CS}$/SA	61	If pin 68 (SEL_MPU) is HIGH, this is the chip select signal of the parallel MPU interface, otherwise it is the I²C-bus slave address select pin. LOW: slave address = 88H, HIGH = 8CH.
V_{SSD6}	62	digital ground 6
VP3(0)	63	Lower 4 bits of the Video Port VP3. If pin 68 (SEL_MPU) is HIGH, this is the data bus of the parallel MPU interface. If it is LOW, there can be multiplexed UV lines (422) of the U-signal (444) of the Video input.
VP3(1)	64	
VP3(2)	65	
VP3(3)	66	
V_{DDD4}	67	digital supply voltage 4
SEL_MPU	68	Select MPU interface input. If it is HIGH, the parallel MPU interface is active, otherwise the I²C-bus interface will be used.

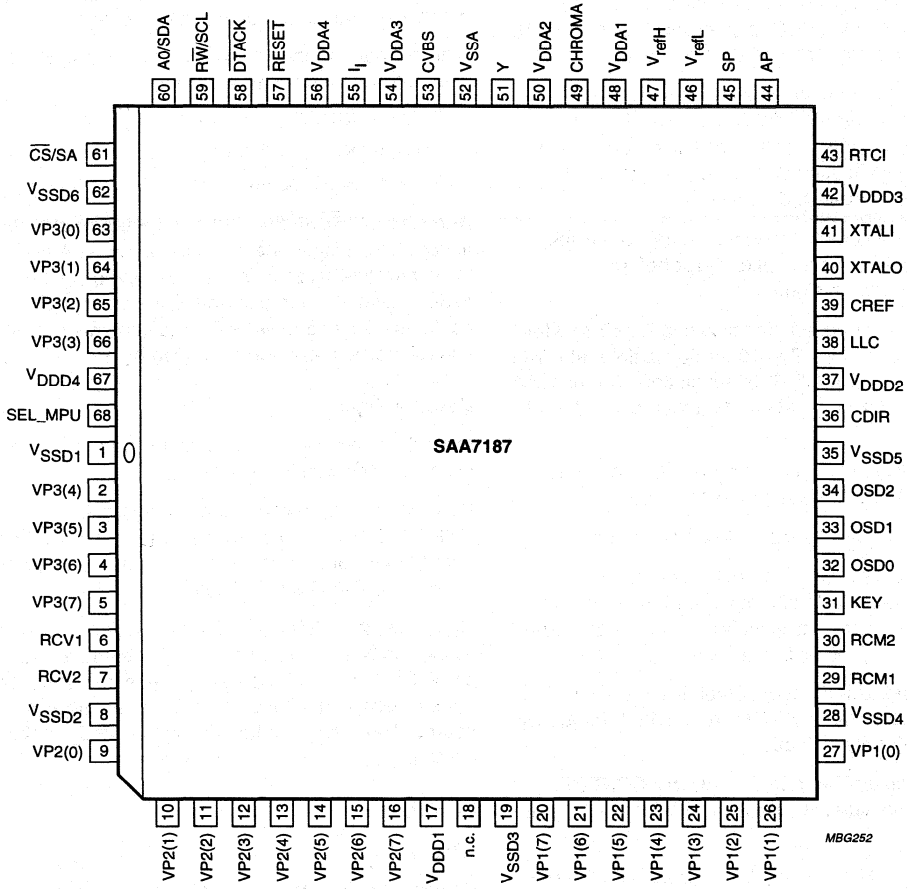


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The digital video encoder (DENC2-SQ) encodes digital luminance and chrominance into analog CVBS and simultaneously S-Video (Y/C) signals. NTSC-M and PAL B/G standards also sub-standards are supported.

The basic encoder function consists of subcarrier generation and colour modulation also insertion of synchronization signals. Luminance and chrominance signals are filtered in accordance with the standard requirements RS-170-A and CCIR 624.

For ease of analog post filtering the signals are twice oversampled with respect to pixel clock before digital-to-analog conversion.

For total filter transfer characteristics see Figs 3 to 6 for 60 Hz field rate, and Figs 7 to 10 for 50 Hz field rate. The DACs are realized with full 10-bit resolution. The encoder provides three 8-bit wide data ports, that serve different applications.

The VP1 port accepts 8 lines multiplexed Cb-Y-Cr data (CCIR 656 mode), or Y data only (444 mode).

The VP2 port accepts Cr data in 444 input mode.

The VP3 port accepts Cb data (444 input mode) or multiplexed Cb/Cr data (422 input mode). If not used for video input data, it can alternatively also handle the data of an 8-bit wide microprocessor interface.

Minimum suppression of output chrominance alias components approximately 1 MHz due to high frequency 444 input is better than 12 dB.

The 8-bit multiplexed Cb-Y-Cr formats are CCIR 656 (D1 format) compatible, but the SAV, EAV, etc. codes are not decoded.

A crystal-stable master clock (LLC) of 24.54 or 29.5 MHz, which is twice the line-locked pixel clock, needs to be supplied externally. Optionally, a crystal oscillator input/output pair of pins and an on-chip clock driver is provided. Additionally, a DMSD2 compatible clock interface, using CREF (input or output) and RTC (see *"data sheet SAA7191B"*) is available.

The DENC2-SQ synthesizes all necessary internal signals, colour subcarrier frequency, and synchronization signals, from that clock. DENC2-SQ can be timing master or slave.

The IC also contains Closed Caption and Extended Data Services Encoding (Line 21); it also supports OSD via KEY and three-bit overlay techniques by a 24 × 8 LUT.

The IC can be programmed via I²C-bus or 8-bit MPU interface, but only one interface configuration can be active at a time; if 422 or 444 input format is being used, only the I²C-bus interface can be selected.

A number of possibilities are provided for setting of different video parameters such as:

Black and blanking level control

Colour subcarrier frequency

Variable burst amplitude etc.

During reset ($\overline{\text{RESET}}$ = LOW) and after reset is released, all digital I/O stages are set to input mode. A reset forces the control interfaces to abort any running bus transfer and to set register 3AH to contents 00H, register 61H to contents 15H, and register 6CH to contents 00H. All other control registers are not influenced by a reset.

Data manager

In the data manager, the demultiplexing scheme is chosen in accordance with the input format.

Depending on hardware conditions (signals on pins KEY, OSD2 to OSD0), and software programming either data from the VP ports or from the OSD port are selected to be encoded to CVBS and Y/C signals.

Optionally, the OSD colour look-up tables located in this block, can be read out in a pre-defined sequence (8 steps per active video line), achieving e.g. a colour bar test pattern generator without need for an external data source. The colour bar function is only under software control.

Encoder

VIDEO PATH

The encoder generates out of Y, U and V baseband signals luminance and colour subcarrier output signals, suitable for use as CVBS or separate Y/C signals.

Luminance is modified in gain and in offset (latter programmable in a certain range to enable different black level set-ups). After having been inserted a fixed synchronization level, in accordance with standard composite synchronization schemes, a variable blanking level, programmable also in a certain range, is inserted.

Transients of both synchronization pulses and start/stop of blanking are reduced compared to overall luminance bandwidth.

In order to enable easy analog post filtering, luminance is interpolated from square pixel data rate to twice that rate (24.54 or 29.5 MHz respectively), providing luminance in 10-bit resolution. For transfer characteristic of the luminance interpolation filter see Figs 5 and 6 for 60 Hz field rate and Figs 9 and 10 for 50 Hz field rate.

Chrominance is modified in gain (programmable separately for U and V), standard dependent burst is inserted, before baseband colour signals are interpolated correctly to 24.54 or 29.5 MHz data rate. One of the interpolation stages can be bypassed, thus providing a higher colour bandwidth, which can be made use of for Y/C output. For transfer characteristics of the chrominance interpolation filter see Figs 3 and 4 for 60 Hz field rate and Figs 7 and 8 for 50 Hz field rate.

The amplitude of inserted burst is programmable in a certain range, suitable for standard signals and for special effects. Behind the succeeding quadrature modulator, colour in 10-bit resolution is provided on subcarrier.

The numeric ratio between Y and C outputs is in accordance with set standards.

Closed Caption Encoder

Using this circuit, data in accordance with the specification of Closed Caption or Extended Data Service, delivered by the control interface, can be encoded (Line 21). Two dedicated pairs of bytes (two bytes per field), each pair preceded by run-in clocks and framing code, are possible.

The actual line number where data is to be encoded in, can be modified in a certain range.

Data clock frequency is in accordance with definition for NTSC-M standard 32 times horizontal line frequency.

Data LOW at the output of the DACs corresponds to 0 IRE, data HIGH at the output of the DACs corresponds to approximately 50 IRE.

It is also possible to encode Closed Caption Data for 50 Hz field frequencies at 32 times horizontal line frequency.

Output interface

In the output interface encoded Y and C signals are converted from digital-to-analog in 10-bit resolution both Y and C signals are combined to a 10-bit CVBS signal, also; in front of the summation point, the luminance signal can optionally be fed through a further filter stage, suppressing components in the range of subcarrier frequency. Thus, a type of cross colour reduction is provided, which is useful in a standard TV set with CVBS input.

Slopes of synchronization pulses are not affected with any cross colour reduction active.

Three different filter characteristics or bypass are available, see Fig.5 for 60 Hz field rate and Fig.9 for 50 Hz field rate.

The CVBS output occurs with the same processing delay as the Y and C outputs. Absolute amplitudes at the input of the DAC for CVBS is reduced by $^{15}/_{16}$ with respect to Y and C DACs to make maximum use of conversion ranges.

Outputs of all DACs can be set together via software control to minimum output voltage for either purpose.

Synchronization

The synchronization of the DENC2-SQ is able to operate in two modes; slave mode and master mode.

In the slave mode, the circuit accepts synchronization pulses at the bidirectional RCV1 port. The timing and trigger behaviour related to the video signal on VP ports can be influenced by programming the polarity and on-chip delay of RCV1. Active slope of RCV1 defines the vertical phase and optionally the odd/even and colour frame phase to be initialized, it can be also used to set the horizontal phase.

If the horizontal phase is not be influenced by RCV1, a horizontal pulse needs to be supplied at the RCV2 pin. Timing and trigger behaviour can also be influenced for RCV2.

If there are missing pulses at RCV1 and/or RCV2, the time base of DENC2-SQ runs free, thus an arbitrary number of synchronization slopes may miss, but no additional pulses (such with wrong phase) must occur.

If the vertical and horizontal phase is derived from RCV1, RCV2 can be used for horizontal or composite blanking input or output.

In the master mode, the time base of the circuit continuously runs free. On the RCV1 port, the IC can output:

- A Vertical Sync signal (VS) with 3 or 2.5 lines duration, or
- An ODD/EVEN signal which is LOW in odd fields, or
- A field sequence signal (FSEQ) which is HIGH in the first of 4 respectively 8 fields.

On the RCV2 port, the IC can provide a horizontal pulse with programmable start and stop phase; this pulse can be inhibited in the vertical blanking period to build up e.g. a composite blanking signal.

The phase of the pulses output on RCV1 or RCV2 are referenced to the VP ports, polarity of both signals is selectable.

On the RCM1 port the same signals as on RCV1 (as output) are available; on RCM2 the IC provides a horizontal pulse with programmable start and stop phase.

The length of a field also start and end of its active part can be programmed. The active part of a field always starts at the beginning of a line.

Control interface

DENC2-SQ contains two control interfaces: an I²C-bus slave transceiver and 8-bit parallel microprocessor interface. The interfaces cannot be used simultaneously.

The I²C-bus interface is a standard slave transceiver, supporting 7-bit slave addresses and 100 kbits/s guaranteed transfer rate. It uses 8-bit subaddressing with an auto-increment function. All registers are write only, except one readable status byte.

Two I²C-bus slave addresses can be selected (pin SEL_MPU must be LOW):

88H: LOW at pin 61

8CH: HIGH at pin 61.

The parallel interface is defined by:

D7 to D0 data bus

$\overline{CS}$ active-LOW chip select signal

R$\overline{W}$ read/not write signal, LOW for a write cycle

$\overline{DTACK}$ 680xx style data acknowledge (handshake), active-LOW

A0 register select, LOW selects address, HIGH selects data.

The parallel interface uses two registers, one auto-incremental containing the current address of a control register (equals subaddress with I²C-bus control), one containing actual data. The currently addressed register is mapped to the corresponding control register.

The status byte can be read optionally via a read access to the address register, no other read access is provided.

Input levels and formats

DENC2-SQ expects digital YUV data with levels (digital codes) in accordance with CCIR 601.

Deviating amplitudes of the colour difference signals can be compensated by independent gain control setting, while gain for luminance is set to predefined values, distinguishable for 7.5 IRE set-up or without set-up.

Reference levels are measured with a colour bar, 100% white, 100% amplitude and 100% saturation.

When the IC is operating with input data in accordance with CCIR 656, programming can be carried out alternatively via the parallel interface using VP3 port for data transfer.

For other input modes, the I²C-bus interface has to be used for programming.

Table 1 CCIR signal component levels

SIGNAL	IRE	DIGITAL LEVEL	CODE
Y	0	16	straight binary
	50	126	
	100	235	
Cb	bottom peak	16	straight binary
	colourless	128	
	top peak	240	
Cr	bottom peak	16	straight binary
	colourless	128	
	top peak	240	

Table 2 8-bit multiplexed format (similar to CCIR 656)

TIME	FORMAT							
	0	1	2	3	4	5	6	7
Sample	Cb_0	Y_0	Cr_0	Y_1	Cb_2	Y_2	Cr_2	Y_3
Luminance pixel number	0		1		2		3	
Colour pixel number	0				2			

Table 3 16-bit multiplexed format (DTV2 format)

TIME	FORMAT							
	0	1	2	3	4	5	6	7
Sample Y line	Y_0		Y_1		Y_2		Y_3	
Sample UV line	Cb_0		Cr_0		Cb_2		Cr_2	
Luminance pixel number	0		1		2		3	
Colour pixel number	0				2			

Table 4 24-bit direct 444 format

TIME	FORMAT							
	0	1	2	3	4	5	6	7
Sample Y line	Y_0		Y_1		Y_2		Y_3	
Sample U line	Cb_0		Cb_1		Cb_2		Cb_3	
Sample V line	Cr_0		Cr_1		Cr_2		Cr_3	
Luminance pixel number	0		1		2		3	
Colour pixel number	0		1		2		3	

Bit allocation map

Table 5 Slave receiver (slave address 88H or 8CH)

REGISTER FUNCTION	SUB ADDRESS	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
Null	00	0	0	0	0	0	0	0	0
	01 to 38	↓							
Null	39	0	0	0	0	0	0	0	0
Input port control	3A	CBENB	0	0	0	VY2C	VUV2C	FMT1	FMT0
OSD LUT Y0	42	OSDY07	OSDY06	OSDY05	OSDY04	OSDY03	OSDY02	OSDY01	OSDY00
OSD LUT U0	43	OSDU07	OSDU06	OSDU05	OSDU04	OSDU03	OSDU02	OSDU01	OSDU00
OSD LUT V0	44	OSDV07	OSDV06	OSDV05	OSDV04	OSDV03	OSDV02	OSDV01	OSDV00
	45 to 56	↓							
OSD LUT Y7	57	OSDY77	OSDY76	OSDY75	OSDY74	OSDY73	OSDY72	OSDY71	OSDY70
OSD LUT U7	58	OSDU77	OSDU76	OSDU75	OSDU74	OSDU73	OSDU72	OSDU71	OSDU70
OSD LUT V7	59	OSDV77	OSDV76	OSDV75	OSDV74	OSDV73	OSDV72	OSDV71	OSDV70
Chrominance phase	5A	CHPS7	CHPS6	CHPS5	CHPS4	CHPS3	CHPS2	CHPS1	CHPS0
Gain U	5B	GAINU7	GAINU6	GAINU5	GAINU4	GAINU3	GAINU2	GAINU1	GAINU0
Gain V	5C	GAINV7	GAINV6	GAINV5	GAINV4	GAINV3	GAINV2	GAINV1	GAINV0
Gain U MSB, black level	5D	GAINU8	0	BLCKL5	BLCKL4	BLCKL3	BLCKL2	BLCKL1	BLCKL0
Gain V MSB, blanking level	5E	GAINV8	0	BLNNL5	BLNNL4	BLNNL3	BLNNL2	BLNNL1	BLNNL0
Null	5F	0	0	0	0	0	0	0	0
Cross-colour select	60	CCRS1	CCRS0	0	0	0	0	0	0
Standard control	61	0	DOWN	INPI1	YGS	RTCE	SCBW	PAL	FISE
Burst amplitude	62	SQP	BSTA6	BSTA5	BSTA4	BSTA3	BSTA2	BSTA1	BSTA0
Subcarrier 0	63	FSC07	FSC06	FSC05	FSC04	FSC03	FSC02	FSC01	FSC00
Subcarrier 1	64	FSC15	FSC14	FSC13	FSC12	FSC11	FSC10	FSC09	FSC08
Subcarrier 2	65	FSC23	FSC22	FSC21	FSC20	FSC19	FSC18	FSC17	FSC16
Subcarrier 3	66	FSC31	FSC30	FSC29	FSC28	FSC27	FSC26	FSC25	FSC24
Line 21 odd 0	67	L21O07	L21O06	L21O05	L21O04	L21O03	L21O02	L21O01	L21O00
Line 21 odd 1	68	L21O17	L21O16	L21O15	L21O14	L21O13	L21O12	L21O11	L21O10
Line 21 even 0	69	L21E07	L21E06	L21E05	L21E04	L21E03	L21E02	L21E01	L21E00
Line 21 even 1	6A	L21E17	L21E16	L21E15	L21E14	L21E13	L21E12	L21E11	L21E10
CC line	6B	0	0	0	SCCLN4	SCCLN3	SCCLN2	SCCLN1	SCCLN0

REGISTER FUNCTION	SUB ADDRESS	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
RCV port control	6C	SRCV11	SRCV10	TRCV2	ORCV1	PRCV1	CBLF	ORCV2	PRCV2
RCM, CC mode	6D	0	0	0	0	SRCM11	SRCM10	CCEN1	CCEN0
Horizontal trigger	6E	HTRIG7	HTRIG6	HTRIG5	HTRIG4	HTRIG3	HTRIG2	HTRIG1	HTRIG0
Horizontal trigger	6F	0	0	0	0	0	HTRIG10	HTRIG09	HTRIG08
f_{sc} reset mode, Vertical trigger	70	PHRES1	PHRES0	SBLBN	VTRIG4	VTRIG3	VTRIG2	VTRIG1	VTRIG0
Begin master request	71	BMRQ7	BMRQ6	BMRQ5	BMRQ4	BMRQ3	BMRQ2	BMRQ1	BMRQ0
End master request	72	EMRQ7	EMRQ6	EMRQ5	EMRQ4	EMRQ3	EMRQ2	EMRQ1	EMRQ0
MSBs master request	73	0	EMRQ10	EMRQ09	EMRQ08	0	BMRQ10	BMRQ09	BMRQ08
Null	74	0	0	0	0	0	0	0	0
Null	75	0	0	0	0	0	0	0	0
Null	76	0	0	0	0	0	0	0	0
Begin RCV2 output	77	BRCV7	BRCV6	BRCV5	BRCV4	BRCV3	BRCV2	BRCV1	BRCV0
End RCV2 output	78	ERCV7	ERCV6	ERCV5	ERCV4	ERCV3	ERCV2	ERCV1	ERCV0
MSBs RCV2 output	79	0	ERCV10	ERCV09	ERCV08	0	BRCV10	BRCV09	BRCV08
Field length	7A	FLEN7	FLEN6	FLEN5	FLEN4	FLEN3	FLEN2	FLEN1	FLEN0
First active line	7B	FAL7	FAL6	FAL5	FAL4	FAL3	FAL2	FAL1	FAL0
Last active line	7C	LAL7	LAL6	LAL5	LAL4	LAL3	LAL2	LAL1	LAL0
MSBs field control	7D	0	0	LAL8	FAL8	0	0	FLEN9	FLEN8

I²C-bus format

Table 6 I²C-bus address; see Table 7

S	SLAVE ADDRESS	ACK	SUBADDRESS	ACK	DATA 0	ACK	--------	DATA n	ACK	P

Table 7 Explanation of Table 6

PART	DESCRIPTION
S	START condition
Slave address	1 0 0 0 1 0 0 X or 1 0 0 0 1 1 0 X (note 1)
ACK	acknowledge, generated by the slave
Subaddress (note 2)	subaddress byte
DATA	data byte
--------	continued data bytes and ACKs
P	STOP condition

Notes

1. X is the read/write control bit; X = logic 0 is order to write; X = logic 1 is order to read, no subaddressing with read.
2. If more than 1 byte DATA is transmitted, then auto-increment of the subaddress is performed.

Slave receiver

Table 8 Subaddress 3A

DATA BYTE	LOGIC LEVEL	DESCRIPTION
FMT	see Table 9	Select input data format.
VUV2C	0	Cb/Cr data input to VP ports is two's complement. Default after reset.
	1	Cb/Cr data input to VP ports is straight binary.
VY2C	0	Y data input to VP1 port is two's complement. Default after reset.
	1	Y data input to VP1 port is straight binary.
CBENB	0	Data from input ports is encoded. Default after reset.
	1	Colour bar with programmable colours (entries of OSD_LUTs) is encoded. The LUTs are read in upward order from index 0 to index 7.

Table 9 Logic levels and function of FMT

DATA BYTE		FUNCTION
FMT1	FMT0	
0	0	Input data YUV 444, 24 lines, Y on VP1, Cr on VP2, Cb on VP3. Default after reset.
0	1	Input data YUV 422, 16 lines, Y on VP1, multiplexed CbCr on VP3.
1	0	Input data YUV 422, 8 lines, multiplexed in accordance with CCIR 656 on VP1.
1	1	Input data YUV 422, 8 lines, multiplexed in accordance with CCIR 656 on VP1.

Table 10 Subaddress 42 to 59

COLOUR	DATA BYTE (note 1)			INDEX (note 2)
	OSDY	OSDU	OSDV	
White	107 (6BH)	0 (00H)	0 (00H)	0
	107 (6BH)	0 (00H)	0 (00H)	
Yellow	82 (52H)	144 (90H)	18 (12H)	1
	34 (22hH	172 (ACH)	14 (0EH)	
Cyan	42 (2AH)	38 (26H)	144 (90H)	2
	03 (03H)	29 (1DH)	172 (ACH)	
Green	17 (11H)	182 (B6H)	162 (A2H)	3
	240 (F0H)	200 (C8H)	185 (B9H)	
Magenta	234 (EAH)	74 (4AH)	94 (5EH)	4
	212 (D4H)	56 (38H)	71 (47H)	
Red	209 (D1H)	218 (DAH)	112 (70H)	5
	193 (C1H)	227 (E3H)	84 (54H)	
Blue	169 (A9H)	112 (70H)	238 (EEH)	6
	163 (A3H)	84 (54H)	242 (F2H)	
Black	144 (90H)	0 (00H)	0 (00H)	7
	144 (90H)	0 (00H)	0 (00H)	

Notes

1. Contents of OSD Look-up tables. All 8 entries are 8-bits. Data representation is in accordance with CCIR 601 (Y, Cb, Cr), but two's complement, e.g. for a $^{100}/_{100}$ (upper number) or $^{100}/_{75}$ (lower number) colour bar.
2. For normal colour bar with CBENB = logic 1.

Table 11 Subaddress 5A

DATA BYTE	DESCRIPTION
CHPS	Phase of encoded colour subcarrier (including burst) relative to horizontal sync. Can be adjusted in steps of 360 or 256 degrees.

Table 12 Subaddress 5B and 5D

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
GAINU	variable gain for Cb signal; input representation accordance with CCIR 601	white-to-black = 92.5 IRE(1)	
		GAINU = 0	output subcarrier of U contribution = 0
		GAINU = 118 (76H)	output subcarrier of U contribution = nominal
		white-to-black = 100 IRE(2)	
		GAINU = 0	output subcarrier of U contribution = 0
		GAINU = 125 (7DH)	output subcarrier of U contribution = nominal

Notes

1. GAINU = −2.17 × nominal to +2.16 × nominal.
2. GAINU = −2.05 × nominal to +2.04 × nominal.

Table 13 Subaddress 5C and 5E

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
GAINV	variable gain for Cr signal; input representation accordance with CCIR 601	white-to-black = 92.5 IRE[1]	
		GAINV = 0	output subcarrier of V contribution = 0
		GAINV = 165 (A5H)	output subcarrier of V contribution = nominal
		white-to-black = 100 IRE[2]	
		GAINV = 0	output subcarrier of V contribution = 0
		GAINV = 175 (AFH)	output subcarrier of V contribution = nominal

Notes

1. GAINV = −1.55 × nominal to +1.55 × nominal.
2. GAINV = −1.46 × nominal to +1.46 × nominal.

Table 14 Subaddress 5D

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
BLCKL	variable black level; input representation accordance with CCIR 601	white-to-sync = 140 IRE[1]	
		BLCKL = 0	output black level = 24 IRE
		BLCKL = 63 (3FH)	output black level = 49 IRE
		white-to-sync = 143 IRE[2]	
		BLCKL = 0	output black level = 24 IRE
		BLCKL = 63 (3FH)	output black level = 50 IRE

Notes

1. Output black level/IRE = BLCKL × 25/63 + 24; recommended value: BLCKL = 60 (3CH) normal.
2. Output black level/IRE = BLCKL × 26/63 + 24; recommended value: BLCKL = 45 (2DH) normal.

Table 15 Subaddress 5E

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
BLNNL	variable blanking level	white-to-sync = 140 IRE[1]	
		BLNNL = 0	output blanking level = 17 IRE
		BLNNL = 63 (3FH)	output blanking level = 42 IRE
		white-to-sync = 143 IRE[2]	
		BLNNL = 0	output blanking level = 17 IRE
		BLNNL = 63 (3FH)	output blanking level = 43 IRE

Notes

1. Output black level/IRE = BLNNL × 25/63 + 17; recommended value: BLNNL = 58 (3AH) normal.
2. Output black level/IRE = BLNNL × 26/63 + 17; recommended value: BLNNL = 63 (3FH) normal.

Table 16 Subaddress 60 (CCRS; select cross colour reduction filter in luminance)

DATA BYTE		FUNCTION
CCRS1	CCRS0	
0	0	no cross colour reduction (for transfer characteristic of luminance see Figs 5 and 9)
0	1	cross colour reduction #1 active (for transfer characteristic see Figs 5 and 9)
1	0	cross colour reduction #2 active (for transfer characteristic see Figs 5 and 9)
1	1	cross colour reduction #3 active (for transfer characteristic see Figs 5 and 9)

Table 17 Subaddress 61

DATA BYTE	LOGIC LEVEL	DESCRIPTION
FISE	0	944 total pixel clocks per line
	1	780 total pixel clocks per line; default after reset
PAL	0	NTSC encoding (non-alternating V component); default after reset
	1	PAL encoding (alternating V component)
SCBW	0	enlarged bandwidth for chrominance encoding (for overall transfer characteristic of chrominance in baseband representation see Figs 3, 4, 7 and 8)
	1	standard bandwidth for chrominance encoding (for overall transfer characteristic of chrominance in baseband representation see Figs 3, 4, 7 and 8); default after reset
RTCE	0	no real time control of generated subcarrier frequency; default after reset
	1	real time control of generated subcarrier frequency through SAA7191B (timing see Fig.13)
YGS	0	luminance gain for white-to-black 100 IRE
	1	luminance gain for white-to-black 92.5 IRE including 7.5 IRE set-up of black; default after reset
INPI	0	PAL switch phase is nominal; default after reset
	1	PAL switch phase is inverted compared to nominal
DOWN	0	DACs in normal operational mode; default after reset
	1	DACs forced to lowest output voltage

Table 18 Subaddress 62

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
BSTA	amplitude of colour burst; input representation accordance with CCIR 601	white-to-black = 92.5 IRE; burst = 40 IRE; NTSC encoding BSTA = 0 to 1.25 × nominal(1) white-to-black = 92.5 IRE; burst = 40 IRE; PAL encoding BSTA = 0 to 1.76 × nominal(2) white-to-black = 100 IRE; burst = 43 IRE; NTSC encoding BSTA = 0 to 1.20 × nominal(3) white-to-black = 100 IRE; burst = 43 IRE; PAL encoding BSTA = 0 to 1.67 × nominal(4)	
SQP	subcarrier real time	logic 0	not supported in current version, do not use
		logic 1	control from SAA7191B digital colour decoder

Notes

1. Recommended value: BSTA = 102 (66H).
2. Recommended value: BSTA = 72 (48H).
3. Recommended value: BSTA = 106 (6AH).
4. Recommended value: BSTA = 75 (4BH).

Table 19 Subaddress 63 to 66 (four bytes to program subcarrier frequency)

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
FSC0 to FSC3	f_{sc} = subcarrier frequency (in multiples of line frequency); f_{LLC} = clock frequency (in multiples of line frequency)	$FSC = \text{round}\left(\frac{f_{sc}}{f_{LLC}} \times 2^{32}\right)$ see note 1	FSC3 = most significant byte FSC0 = least significant byte

Note

1. Examples:
   a) NTSC-M: f_{sc} = 227.5, f_{LLC} = 1560 → FSC = 626349397 (25555555H).
   b) PAL-B/G: f_{sc} = 283.7516, f_{LLC} = 1888 → FSC = 645499916 (26798C0CH).

Table 20 Subaddress 67 to 6A

DATA BYTE[1]	DESCRIPTION
L21O0	first byte of captioning data, odd field
L21O1	second byte of captioning data, odd field
L21E0	first byte of extended data, even field
L21E1	second byte of extended data, even field

Note

1. LSBs of the respective bytes are encoded immediately after run-in and framing code, the MSBs of the respective bytes have to carry the parity bit, in accordance with the definition of line 21 encoding format.

Table 21 Subaddress 6B

DATA BYTE	DESCRIPTION
SCCLN	selects the actual line, where closed caption or extended data are encoded; see note 1

Note

1. Line = (SCCLN + 4) for M systems; line = (SCCLN + 1) for other systems.

Table 22 Subaddress 6C

DATA BYTE	LOGIC LEVEL	DESCRIPTION
PRCV2	0	polarity of RCV2 as output is active HIGH, rising edge is taken when input, respectively; default after reset
	1	polarity of RCV2 as output is active LOW, falling edge is taken when input, respectively
ORCV2	0	pin RCV2 is switched to input; default after reset
	1	pin RCV2 is switched to output
CBLF	0	if ORCV2 = HIGH, pin RCV2 provides an HREF signal (Horizontal Reference Pulse that is HIGH during active portion of line, also during vertical blanking Interval); default after reset
	1	if ORCV2 = LOW, signal input to RCV2 is used for horizontal synchronization only (if TRCV2 = 1); default after reset if ORCV2 = LOW, signal input to RCV2 is used for horizontal synchronization (if TRCV2 = 1) also as an internal blanking signal
PRCV1	0	polarity of RCV1 as output is active HIGH, rising edge is taken when input, respectively; default after reset
	1	polarity of RCV1 as output is active LOW, falling edge is taken when input, respectively
ORCV1	0	pin RCV1 is switched to input; default after reset
	1	pin RCV1 is switched to output
TRCV2	0	horizontal synchronization is taken from RCV1 port; default after reset
	1	horizontal synchronization is taken from RCV2 port
SRCV1	–	defines signal type on pin RCV1; see Table 23

Table 23 Logic levels and function of SRCV1

DATA BYTE		AS OUTPUT	AS INPUT	FUNCTION
SRCV11	SRCV10			
0	0	VS	VS	Vertical Sync each field; default after reset
0	1	FS	FS	Frame Sync (odd/even)
1	0	FSEQ	FSEQ	Field Sequence, vertical sync every fourth field (FISE = 1) or eighth field (FISE = 0)
1	1	–	–	not applicable

Table 24 Subaddress 6D

DATA BYTE	DESCRIPTION
CCEN	enables individual line 21 encoding; see Table 25
SRCM	defines signal type on pin RCM1; see Table 26

Table 25 Logic levels and function of CCEN

DATA BYTE		FUNCTION
CCEN1	CCEN0	
0	0	line 21 encoding off
0	1	enables encoding in field 1 (odd)
1	0	enables encoding in field 2 (even)
1	1	enables encoding in both fields

Table 26 Logic levels and function of SRCM

DATA BYTE		AS OUTPUT	FUNCTION
SRCM1	SRCM0		
0	0	VS	Vertical Sync each field
0	1	FS	Frame Sync (odd/even)
1	0	FSEQ	Field Sequence, vertical sync every fourth field (FISE = 1) or eighth field (FISE = 0)
1	1	–	not applicable

Table 27 Subaddress 6E to 6F

DATA BYTE	DESCRIPTION
HTRIG	sets the Horizontal Trigger phase related to signal on RCV1 or RCV2 input values above 1559 (FISE = 1) or 1887 (FISE = 0) are not allowed increasing HTRIG decreases delays of all internally generated timing signals reference mark: analog output horizontal sync (leading slope) coincides with active edge of RCV used for triggering at HTRIG = 031H (033H)

Table 28 Subaddress 70

DATA BYTE	LOGIC LEVEL	DESCRIPTION
VTRIG	–	sets the Vertical Trigger phase related to signal on RCV1 input increasing VTRIG decreases delays of all internally generated timing signals, measured in half lines variation range of VTRIG = 0 to 31 (1FH)
SBLBN	0	vertical blanking is defined by programming of FAL and LAL
	1	vertical blanking is forced automatically at least during field synchronization and equalization pulses; note 1
PHRES	–	selects the phase reset mode of the colour subcarrier generator; see Table 29

Note

1. If cross-colour reduction is programmed, it is active between FAL and LAL in both events.

Table 29 Logic levels and function of PHRES

DATA BYTE		FUNCTION
PHRES1	PHRES0	
0	0	no reset
0	1	reset every two lines
1	0	reset every eight fields
1	1	reset every four fields

Table 30 Subaddress 71 to 73

DATA BYTE	DESCRIPTION
BMRQ	beginning of master request signal (RCM2) values above 1559 (FISE = 1) or 1887 (FISE = 0) are not allowed first active pixel at analog outputs (corresponding input pixel coinciding with RCM2) at BMRQ = 0E1H (130H)
EMRQ	end of master request signal (RCM2) values above 1559 (FISE = 1) or 1887 (FISE = 0) are not allowed last active pixel at analog outputs (corresponding input pixel coinciding with RCM2) at EMRQ = 5E9H (72AH)

Table 31 Subaddress 77 to 79

DATA BYTE	DESCRIPTION
BRCV	beginning of output signal on RCV2 pin values above 1559 (FISE = 1) or 1887 (FISE = 0) are not allowed first active pixel at analog outputs (corresponding input pixel coinciding with RCV2) at BRCV = 0E1H (130H)
ERCV	end of output signal on RCV2 pin values above 1559 (FISE = 1) or 1887 (FISE = 0) are not allowed last active pixel at analog outputs (corresponding input pixel coinciding with RCV2) at ERCV = 5E9H (72AH)

Table 32 Subaddress 7A to 7D

DATA BYTE	DESCRIPTION
FLEN	Length of a Field = FLEN + 1, measured in half lines valid range is limited to 524 to 1022 (FISE = 1) respectively 624 to 1022 (FISE = 0), FLEN should be even
FAL	First Active Line, measured in lines FAL = 0 coincides with the first field synchronization pulse
LAL	Last Active Line, measured in lines LAL = 0 coincides with the first field synchronization pulse

SUBADDRESSES

In subaddresses 5B, 5C, 5D, 5E and 62 all IRE values are rounded up.

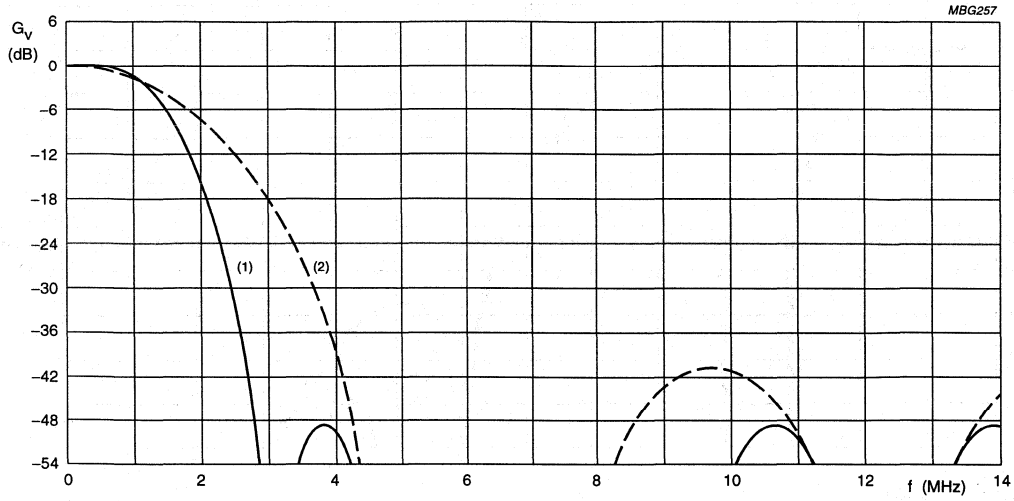
Slave transmitter

Table 33 Slave transmitter (slave address 89H or 8DH)

REGISTER FUNCTION	SUBADDRESS	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
Status byte	–	VER2	VER1	VER0	CCRDO	CCRDE	FSQ2	FSQ1	FSQ0

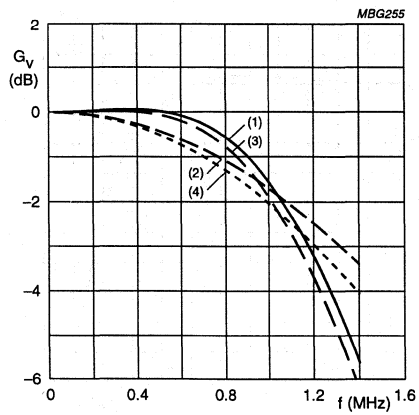
Table 34 No subaddress

DATA BYTE	DESCRIPTION
VER	Version identification of the device. It will be changed with all versions of the IC that have different programming models. Current Version is 000 binary.
CCRDE	Closed caption bytes of the even field have been encoded. The bit is reset after information has been written to the subaddresses 69 and 6A. It is set immediately after the data have been encoded.
CCRDO	Closed caption bytes of the odd field have been encoded. The bit is reset after information has been written to the subaddresses 67 and 68. It is set immediately after the data have been encoded.
FSQ	State of the internal field sequence counter. Bit 0 (FSQ0) gives the odd/even information; odd = LOW, even = HIGH.



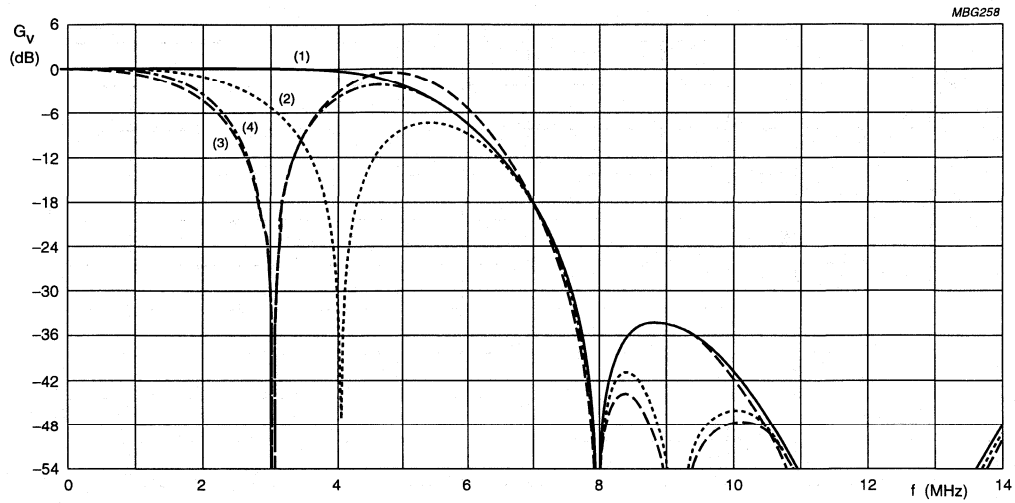
(1) SCBW = 1; 444 input.
(2) SCBW = 0; 444 input.

Fig.3 Chrominance transfer characteristic 1 (60 Hz).



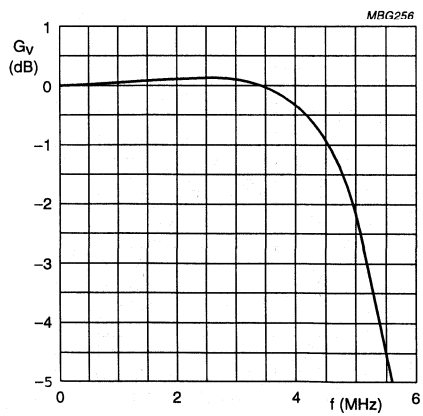
(1) SCBW = 1.
(2) SCBW = 0.
(3) SCBW = 1; 444 input.
(4) SCBW = 0; 444 input.

Fig.4 Chrominance transfer characteristic 2 (60 Hz).



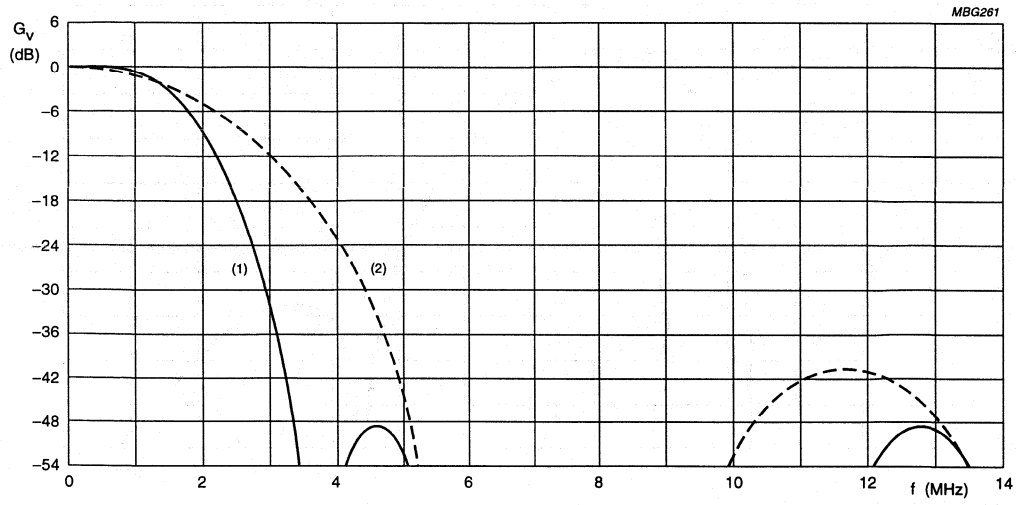
(1) CCRS1 = 0; CCRS0 = 0.
(2) CCRS1 = 0; CCRS0 = 1.
(3) CCRS1 = 1; CCRS0 = 0.
(4) CCRS1 = 1; CCRS0 = 1.

Fig.5 Luminance transfer characteristic 1 (60 Hz).



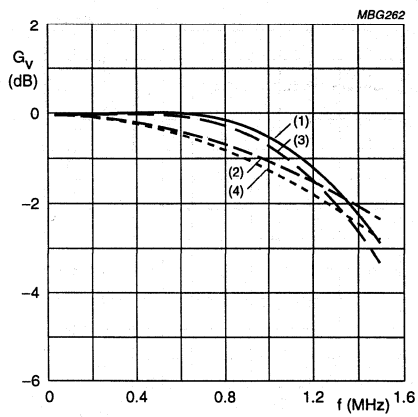
CCRS1 = 0; CCRS0 = 0.

Fig.6 Luminance transfer characteristic 2 (60 Hz).



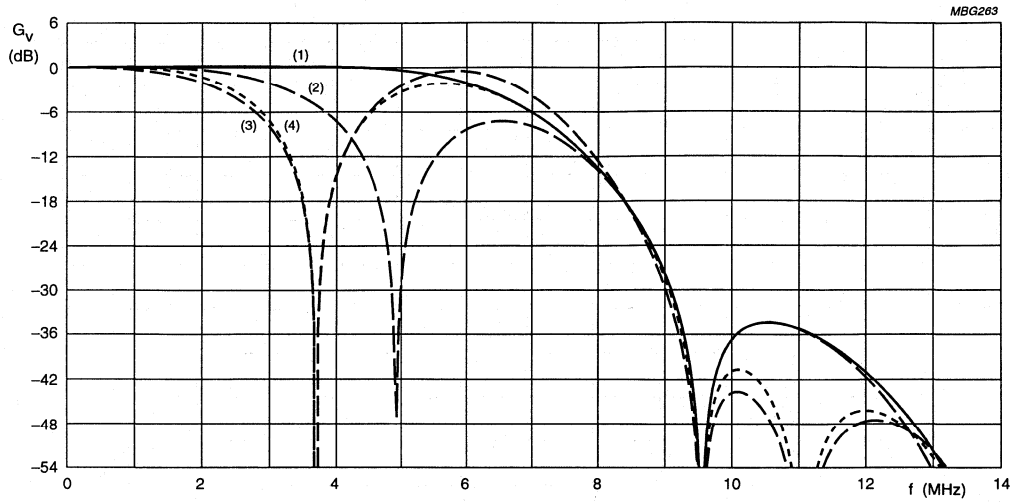
(1) SCBW = 1; 444 input.
(2) SCBW = 0; 444 input.

Fig.7 Chrominance transfer characteristic 1 (50 Hz).



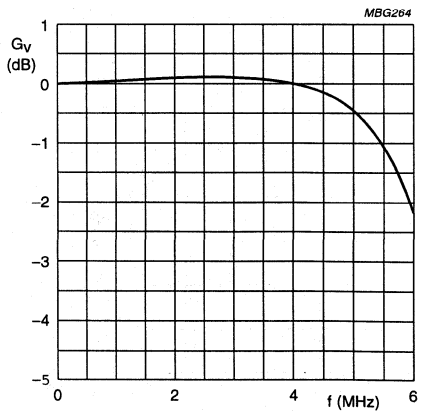
(1) SCBW = 1.
(2) SCBW = 0.
(3) SCBW = 1; 444 input.
(4) SCBW = 0; 444 input.

Fig.8 Chrominance transfer characteristic 2 (50 Hz).



(1) CCRS1 = 0; CCRS0 = 0.
(2) CCRS1 = 0; CCRS0 = 1.
(3) CCRS1 = 1; CCRS0 = 0.
(4) CCRS1 = 1; CCRS0 = 1.

Fig.9 Luminance transfer characteristic 1 (50 Hz).



CCRS1 = 0; CCRS0 = 0.

Fig.10 Luminance transfer characteristic 2 (50 Hz).

CHARACTERISTICS

V_{DDD} = 4.5 to 5.5 V; T_{amb} = 0 to 70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Supply					
V_{DDD}	digital supply voltage		4.5	5.5	V
V_{DDA}	analog supply voltage		4.75	5.25	V
I_{DDD}	digital supply current	note 1	–	210	mA
I_{DDA}	analog supply current	note 1	–	55	mA
Inputs					
V_{IL}	LOW level input voltage (except SDA, SCL, AP, SP and XTALI)		−0.5	+0.8	V
V_{IH}	HIGH level input voltage (except SDA, SCL, AP, SP and XTALI)		2.0	V_{DDD} + 0.5	V
	HIGH level input voltage (LLC)		2.4	V_{DDD} + 0.5	V
I_{LI}	input leakage current		–	1	µA
C_i	input capacitance	clocks operating	–	10	pF
		data available	–	8	pF
		I/Os at high impedance	–	8	pF
Outputs					
V_{OL}	LOW level output voltage (except SDA and XTALO)	note 2	0	0.6	V
V_{OH}	HIGH level output voltage (except SDA, $\overline{DTACK}$ and XTALO)	note 2	2.4	V_{DDD} + 0.5	V
	HIGH level output voltage (LLC)	note 2	2.6	V_{DDD} + 0.5	V
I²C-bus; SDA and SCL					
V_{IL}	LOW level input voltage		−0.5	+1.5	V
V_{IH}	HIGH level input voltage		3.0	V_{DDD} + 0.5	V
I_I	input current	V_I = LOW or HIGH	–	±10	µA
V_{OL}	LOW level output voltage (SDA)	I_{OL} = 3 mA	–	0.4	V
I_O	output current	during acknowledge	3	–	mA
Clock timing (LLC)					
T_{LLC}	cycle time	note 3	31	44	ns
δ	duty factor t_{HIGH}/T_{LLC}	note 4	40	60	%
t_r	rise time	note 3	–	5	ns
t_f	fall time	note 3	–	6	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Input timing					
$t_{SU;CREF}$	input data set-up time (CREF)		6	–	ns
$t_{HD;CREF}$	input data hold time (CREF)		3	–	ns
t_{SU}	input data set-up time (any other except SEL_MPU, CDIR, R$\overline{W}$/SCL, A0/SDA, $\overline{CS}$/SA, $\overline{RESET}$, AP and SP)		6	–	ns
t_{HD}	input data hold time (any other except SEL_MPU, CDIR, R$\overline{W}$/SCL, A0/SDA, $\overline{CS}$/SA, $\overline{RESET}$, AP and SP)		3	–	ns
Crystal oscillator					
f_n	nominal frequency (usually 24.545454 or 29.5 MHz)	3rd harmonic	–	30	MHz
$\Delta f/f_n$	permissible deviation of nominal frequency	note 5	–50	+50	10^{-6}
CRYSTAL SPECIFICATION					
T_{amb}	operating ambient temperature		0	70	°C
C_L	load capacitance		8	–	pF
R_S	series resonance resistance		–	80	Ω
C_1	motional capacitance (typical)		1.5 –20%	1.5 +20%	fF
C_0	parallel capacitance (typical)		3.5 –20%	3.5 +20%	pF
MPU interface timing					
t_{AS}	address set-up time	note 6	9	–	ns
t_{AH}	address hold time		0	–	ns
$t_{R\overline{W}S}$	read/write set-up time	note 6	9	–	ns
$t_{R\overline{W}H}$	read/write hold time		0	–	ns
t_{DD}	data valid from $\overline{CS}$ (read)	notes 7, 8 and 9; n = 9	–	440	ns
t_{DF}	data bus floating from $\overline{CS}$ (read)	notes 7 and 8; n = 5	–	275	ns
t_{DS}	data bus set-up time (write)	note 6	9	–	ns
t_{DH}	data bus hold time (write)	note 6	9	–	ns
t_{ACS}	acknowledge delay from $\overline{CS}$	notes 7 and 8; n = 11	–	520	ns
$t_{\overline{CS}D}$	$\overline{CS}$ HIGH from acknowledge		0	–	ns
t_{DAT}	$\overline{DTACK}$ floating from $\overline{CS}$ HIGH	notes 7 and 8; n = 7	–	360	ns
Data and reference signal output timing					
C_L	output load capacitance		7.5	40	pF
t_{OH}	output hold time		4	–	ns
t_{OD}	output delay time	CREF in output mode	–	25	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
CHROMA, Y and CVBS outputs					
$V_{o(p-p)}$	output signal voltage (peak-to-peak value)	note 10	1.9	2.1	V
R_I	internal serial resistance		18	35	Ω
R_L	output load resistance		80	–	Ω
B	output signal bandwidth of DACs	–3 dB	10	–	MHz
ILE	LF integral linearity error of DACs		–	±2	LSB
DLE	LF differential linearity error of DACs		–	±1	LSB

Notes

1. At maximum supply voltage with highly active input signals.
2. The levels have to be measured with load circuits of 1.2 kΩ to 3.0 V (standard TTL load) and C_L = 25 pF.
3. The data is for both input and output direction.
4. With LLC in input mode. In output mode, with a crystal connected to XTALO/XTALI duty factor is typically 50%.
5. If an internal oscillator is used, crystal deviation of nominal frequency (f_n) is directly proportional to the deviation of subcarrier frequency and line/field frequency.
6. The value is calculated via equation $t = t_{SU} + t_{HD}$
7. The value depends on the clock frequency. The numbers given are calculated with f_{LLC} = 24.54 MHz.
8. The values given are calculated via equation $t_{dmax} = t_{OD} + n \times t_{LLC} + t_{LLC} + t_{SU}$
9. The falling edge of $\overline{DTACK}$ will always occur1 × LLC after data is valid.
10. For full digital range, without load, V_{DDA} = 5.0 V. The typical voltage swing is 2.0 V, the typical minimum output voltage (digital zero at DAC) is 0.2 V.

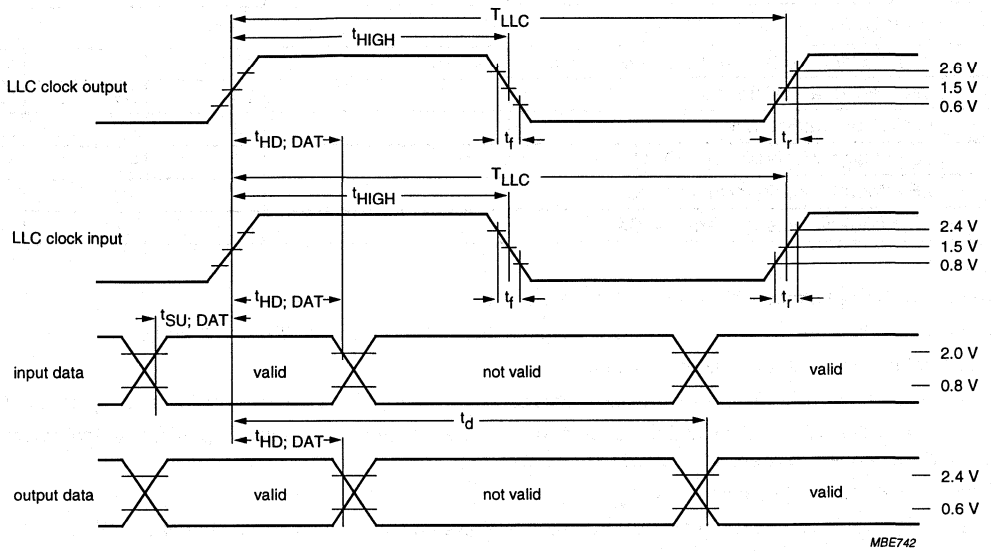
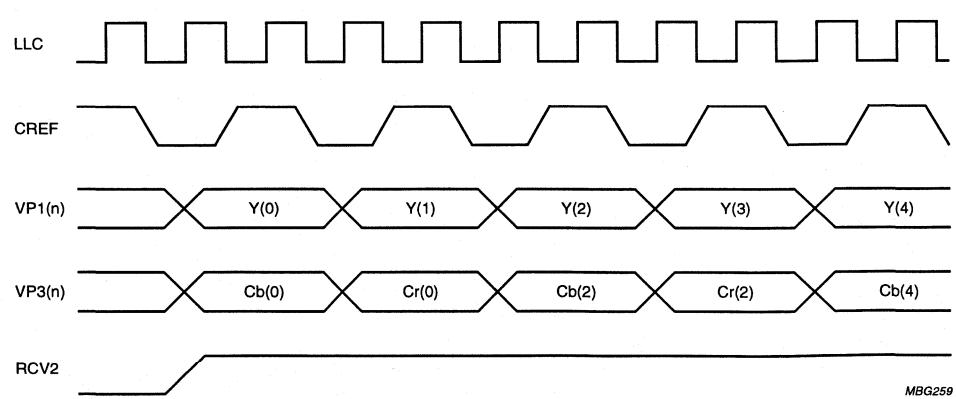
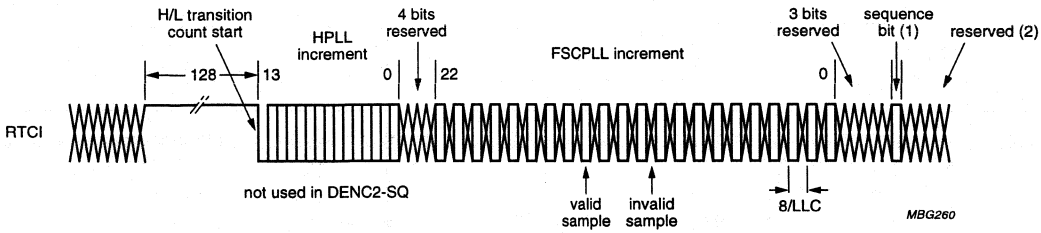


Fig.11 Clock data timing.



The data demultiplexing phase is coupled to the internal horizontal phase.
The CREF signal applies only for the 16 lines digital TV format, because these signals are only valid in 12.27 or 14.75 MHz.
The phase of the RCV2 signal is programmed to 0E1H (130H for 50 Hz) in this example in output mode (BRCV2).

Fig.12 Digital TV timing.



(1) Sequence bit:
PAL = logic 0 then (R – Y) line normal; PAL = logic 1 then (R – Y) line inverted.
NTSC = logic 0 then no change.

(2) Reserved bits: 276 with 50 Hz systems; 188 with 60 Hz systems.

Fig.13 RTCI timing.

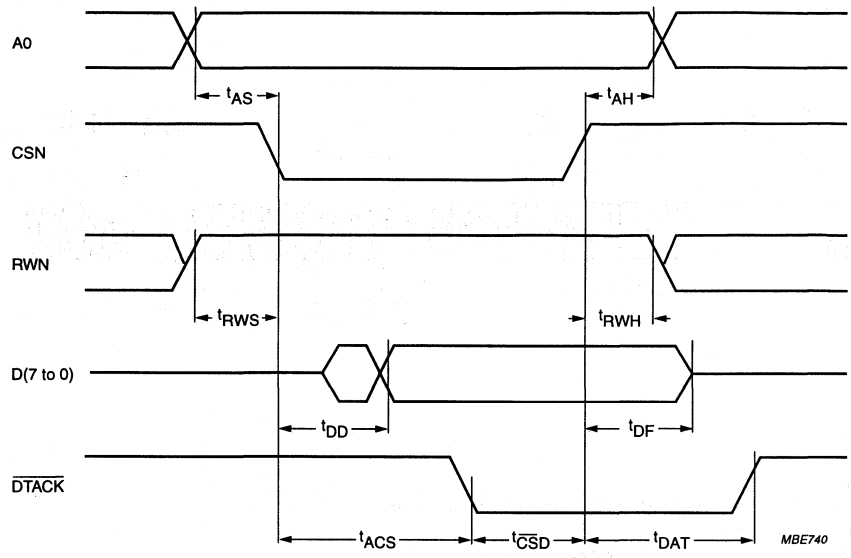


Fig.14 MPU interface timing (read cycle).

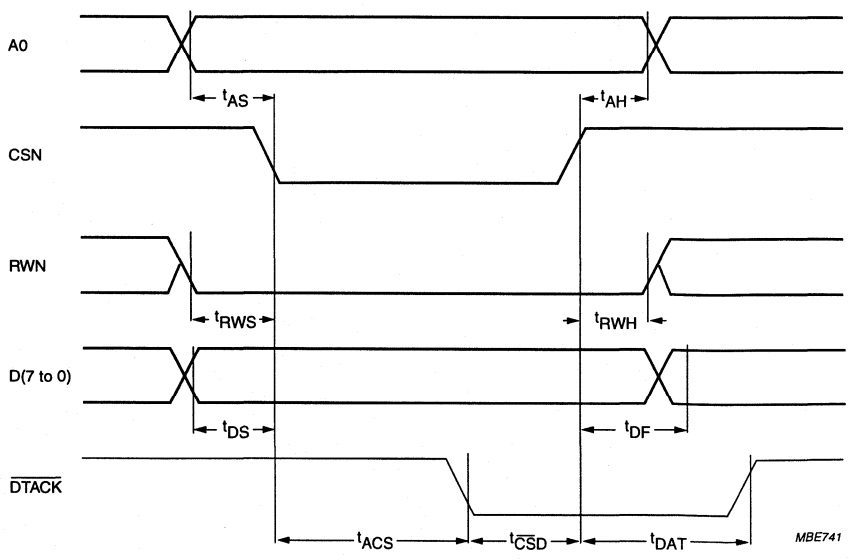


Fig.15 MPU interface timing (write cycle).

APPLICATION INFORMATION

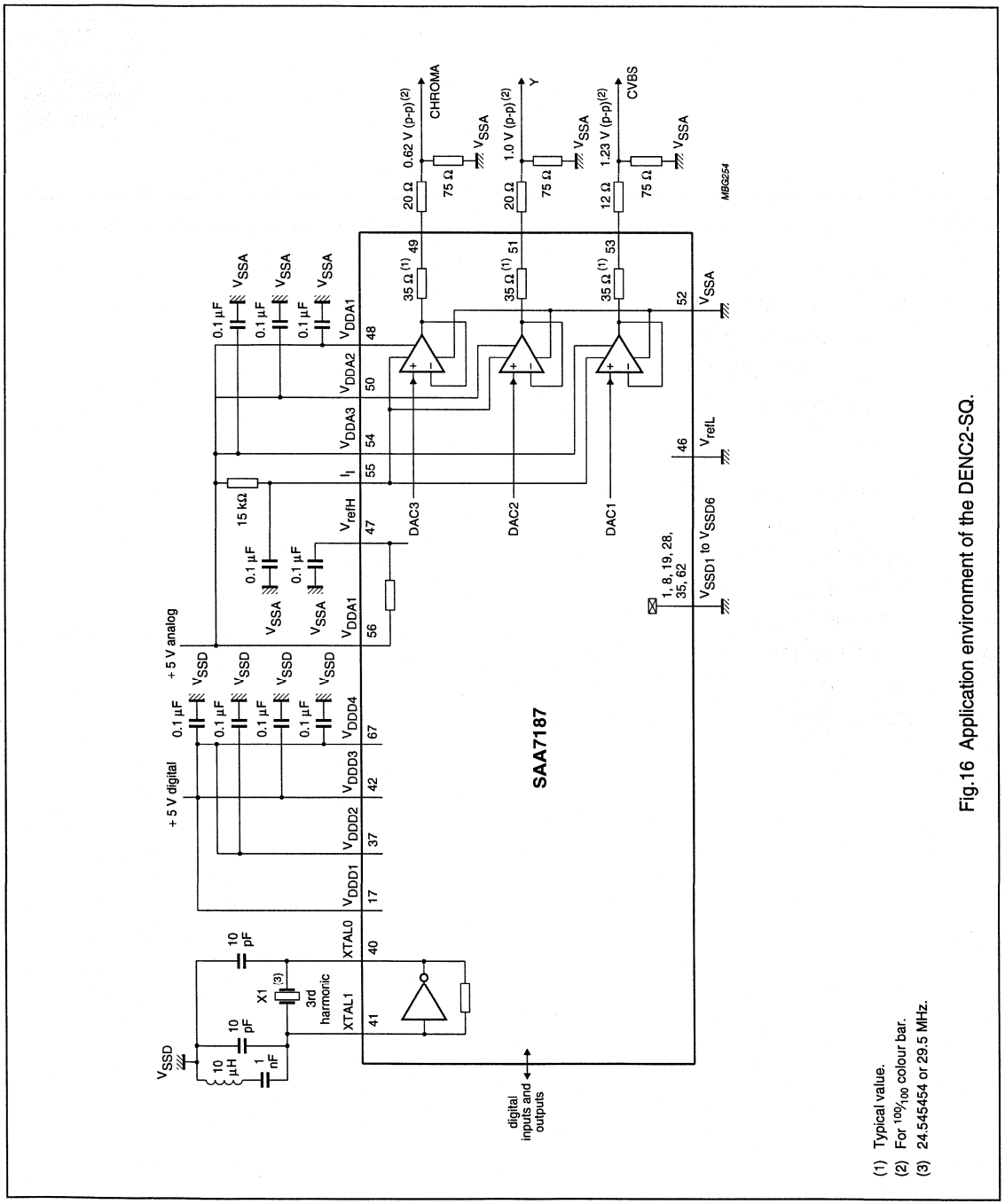
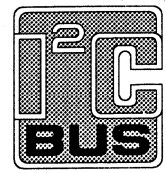


Fig.16 Application environment of the DENC2-SQ.

(1) Typical value.
(2) For $^{100}/_{100}$ colour bar.
(3) 24.545454 or 29.5 MHz.

Digital Multistandard Colour Decoder, Square Pixel (DMSD-SQP)

SAA7191B



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3. QUICK REFERENCE DATA
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Digital Multistandard Colour Decoder, Square Pixel (DMSD-SQP)

SAA7191B

1. FEATURES

- Separate 8-bit luminance (Y or CVBS) and 8-bit chrominance inputs (CVBS or C) from CVBS, Y/C, S-Video (S-VHS or Hi8) sources
- Luminance and chrominance signal processing for standards PAL-B/G, NTSC-M, SECAM
- Horizontal and vertical sync detection for all standards
- Real-time control output RTCO to be used for frequency-locked digital video encoder (SAA7199B). RTCO contains serialized information about actual clock frequency, subcarrier frequency and PAL/SECAM sequence.
- Controls via the I^2C-bus
- User programmable aperture correction (horizontal peaking)
- Compatible with memory-based features (line-locked clock)
- Cross-colour reduction by chrominance comb-filtering (NTSC) or by special cross colour cancellation (SECAM)
- 8-bit quantization of input signals
- 768/640 active samples per line equals 50/60 Hz (SQP)
- The YUV bus supports data rates of 780 x f_H equal to 12.2727 MHz for 60 Hz (NTSC-M) and 944 x f_H equal to 14.75 MHz for 50 Hz (PAL–B/G, SECAM) in 4 : 1 : 1 or 4 : 2 : 2 formats (via the I^2C-bus)
- One crystal oscillator of 26.8 MHz

2. GENERAL DESCRIPTION

The SAA7191B is a digital multistandard colour decoder suitable for 8-bit CVBS input signals or for 8-bit luminance and 8-bit chrominance input signals (Y/C).

The SAA7191B is down-compatible with SAA7191. The SAA7191B has additional outputs RTCO, GPSW0 and ODD. These new outputs are in high-impedance state when NFEN-bit = 0.

3. QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage (pins 5, 18, 28, 37 and 52)	4.5	5	5.5	V
I_{DD}	total supply current (pins 5, 18, 28, 37 and 52)	-	100	250	mA
V_{IL}	input levels	TTL-compatible			
V_{OL}	output levels	TTL-compatible			
T_{amb}	operating ambient temperature	0	-	70	°C

4. ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7191B	68	PLCC	plastic	SOT188-2

5. BLOCK DIAGRAM

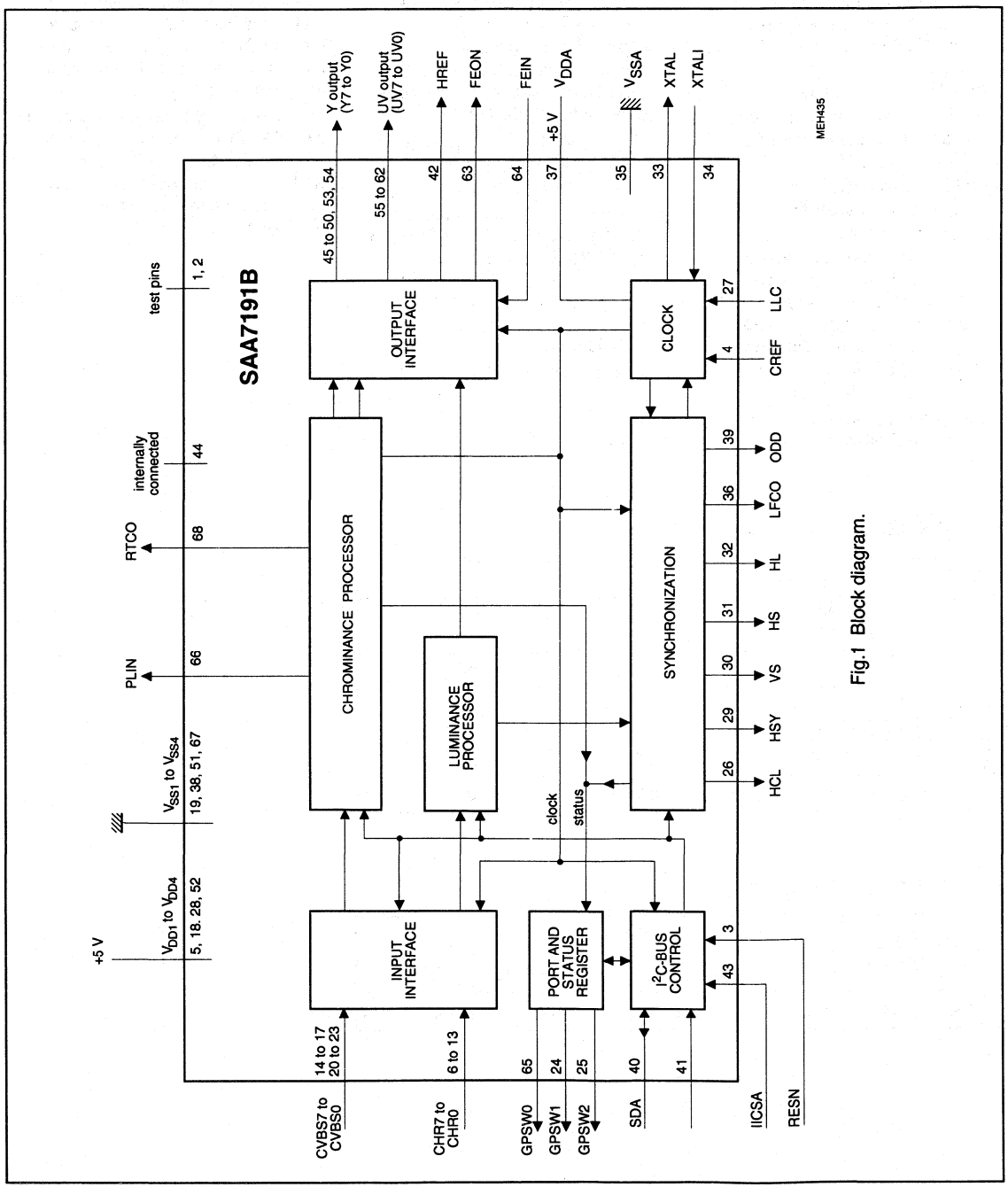


Fig.1 Block diagram.

6. PINNING

SYMBOL	PIN	DESCRIPTION
SP	1	connected to ground (shift pin for testing)
AP	2	connected to ground (action pin for testing)
RESN	3	reset, active LOW
CREF	4	clock reference, sync from external to ensure in-phase signals on the YUV-bus
V_{DD1}	5	+5 V supply input 1
CHR0	6	chrominance input data bits CHR7 to CHR0 from a Y/C (VHS, Hi8) source in two's complement format
CHR1	7	
CHR2	8	
CHR3	9	
CHR4	10	
CHR5	11	
CHR6	12	
CHR7	13	
CVBS0	14	luminance respectively CVBS lower input data bits CVBS3 to CVBS0 (CVBS with luminance, chrominance and all sync information in two's complement format)
CVBS1	15	
CVBS2	16	
CVBS3	17	
V_{DD2}	18	+5 V supply input 2
V_{SS1}	19	ground 1 (0 V)
CVBS4	20	luminance respectively CVBS upper input data bits CVBS7 to CVBS4 (CVBS with luminance, chrominance and all sync information in two's complement format)
CVBS5	21	
CVBS6	22	
CVBS7	23	
GPSW1	24	Port 1 output for general purpose (programmable)
GPSW2	25	Port 2 output for general purpose (programmable)
HCL	26	black level clamp pulse (programmable), e.g. for TDA8708 (ADC)
LLC	27	line-locked clock input signal (29.5 MHz for 50 Hz system; 24.5454 MHz for 60 Hz system)
V_{DD3}	28	+5 V supply input 3
HSY	29	horizontal sync indicator output signal (programmable), e.g. for TDA8708 (ADC)
VS	30	vertical sync output signal
HS	31	horizontal sync output signal (programmable)
HL	32	horizontal lock flag, HIGH = PLL locked
XTAL	33	26.8 MHz clock output
XTALI	34	26.8 MHz connection for crystal or external oscillator (TTL compatible squarewave)

SYMBOL	PIN	DESCRIPTION
V_{SSA}	35	analog ground
LFCO	36	line frequency control output signal, multiple of horizontal frequency (7.375 MHz/6.136363 MHz)
V_{DDA}	37	+5 V supply input for analog part
V_{SS2}	38	ground 2 (0 V)
ODD	39	odd/even field identification output (odd = HIGH); active only at NFEN-bit = 1
SDA	40	I^2C-bus data line
SCL	41	I^2C-bus clock line
HREF	42	horizontal reference output for valid YUV data (for active line 768Y or 640Y samples long)
IICSA	43	set module address input (LOW = 1000 101X; HIGH = 1000 111X)
i.c.	44	internally connected
Y7	45	Y signal output bits Y7 to Y2 (luminance), part of the digital YUV-bus
Y6	46	
Y5	47	
Y4	48	
Y3	49	
Y2	50	
V_{SS3}	51	ground 3 (0 V)
V_{DD4}	52	+5 V supply input 4
Y1	53	Y signal output bits Y1 to Y0 (luminance), part of the digital YUV-bus
Y0	54	
UV7	55	UV signal output bits UV7 to UV0 (colour-difference), part of the digital YUV-bus
UV6	56	
UV5	57	
UV4	58	
UV3	59	
UV2	60	
UV1	61	
UV0	62	
FEON	63	output active flag (active LOW when Y and UV data in high-impedance state)
FEIN	64	fast enable input (active LOW to control fast switching due to YUV data)
GPSW0	65	Port 0 output for general purpose (programmable); active only at NFEN-bit = 1
PLIN	66	PAL flag (active LOW at inverted line); SECAM flag (LOW equals DR, HIGH equals DB line)
V_{SS4}	67	ground 4 (0 V)
RTCO	68	real-time control output active at NFEN-bit = 1; Fig.7

PIN CONFIGURATION

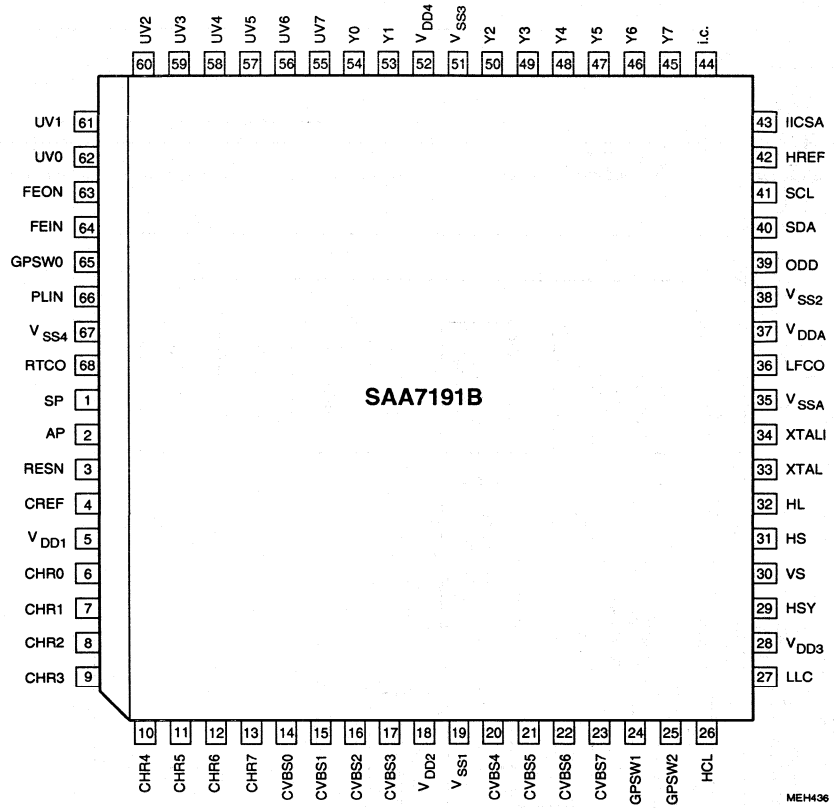


Fig.2 Pin configuration.

7. FUNCTIONAL DESCRIPTION

Chrominance processor

The 8-bit chrominance input signal (CVBS or chrominance format). passes a bandpass filter to eliminate DC components and to decimate the sample rate before it is fed to the two multipliers (quadrature demodulator), Fig.3(a).
Two subcarrier signals from a local oscillator (0 and 90 degree) are fed to the multiplicator inputs of the multipliers. The multipliers operate as a quadrature demodulator for all PAL and NTSC signals; it operates as a frequency down-mixer for SECAM signals.
The two multiplier output signals are converted to a serial data stream and applied to three low-pass filter stages, then to a gain controlled amplifier. A final multiplexed low-pass filter achieves, together with the preceding stages, the required bandwidth performance.
The signals, originated from PAL and NTSC, are applied to a comb-filter.
The signals, originated from SECAM, are fed through a Cloche filter (0 Hz centre frequency), a phase demodulator and a differentiator to obtain frequency-demodulated colour-difference signals.
The SECAM signals are fed after de-emphasis to a cross-over switch, to provide the both serial-transmitted colour-difference signals. These signals are fed finally to the output formatter stages and to the output interface.

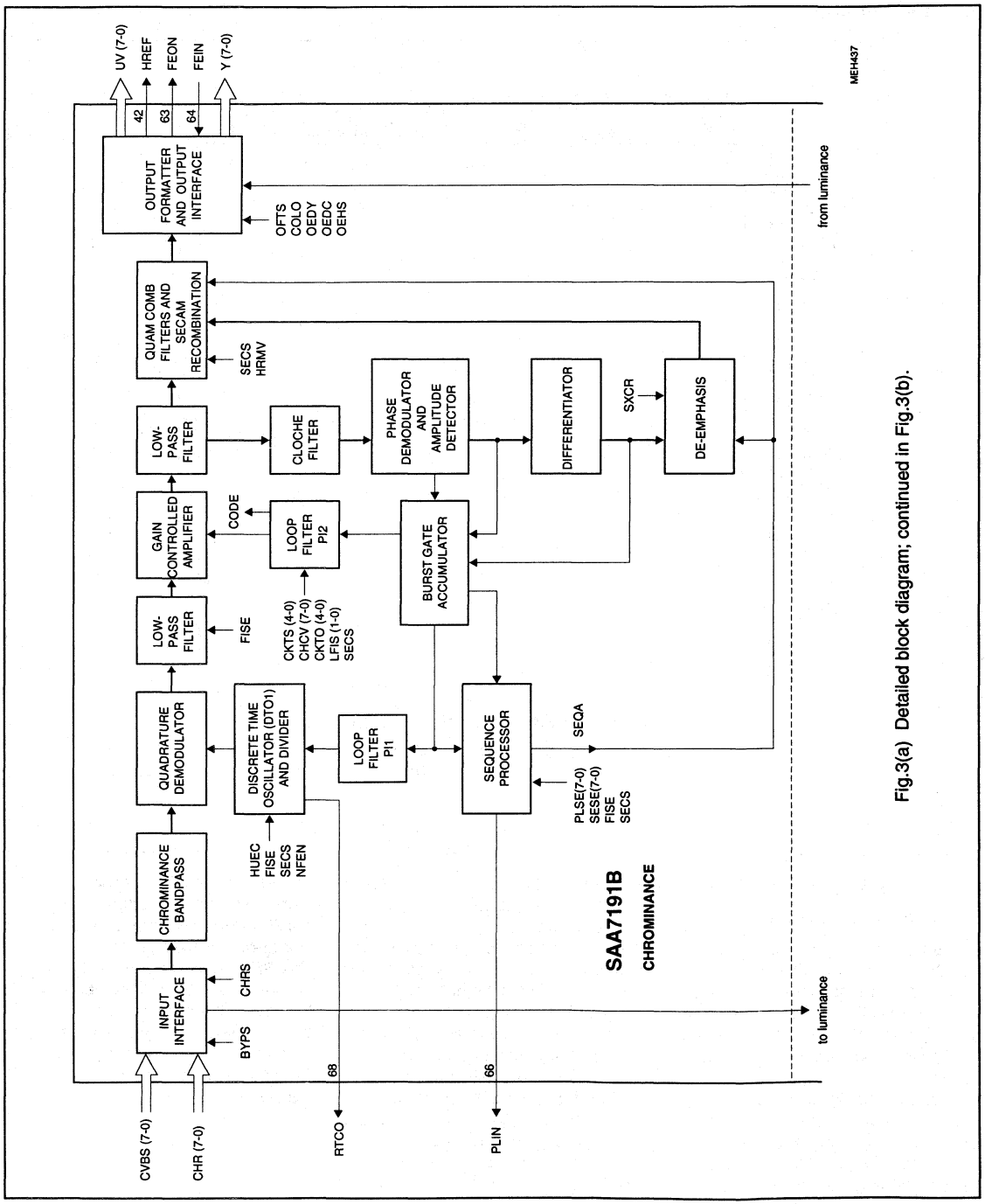


Fig.3(a) Detailed block diagram; continued in Fig.3(b).

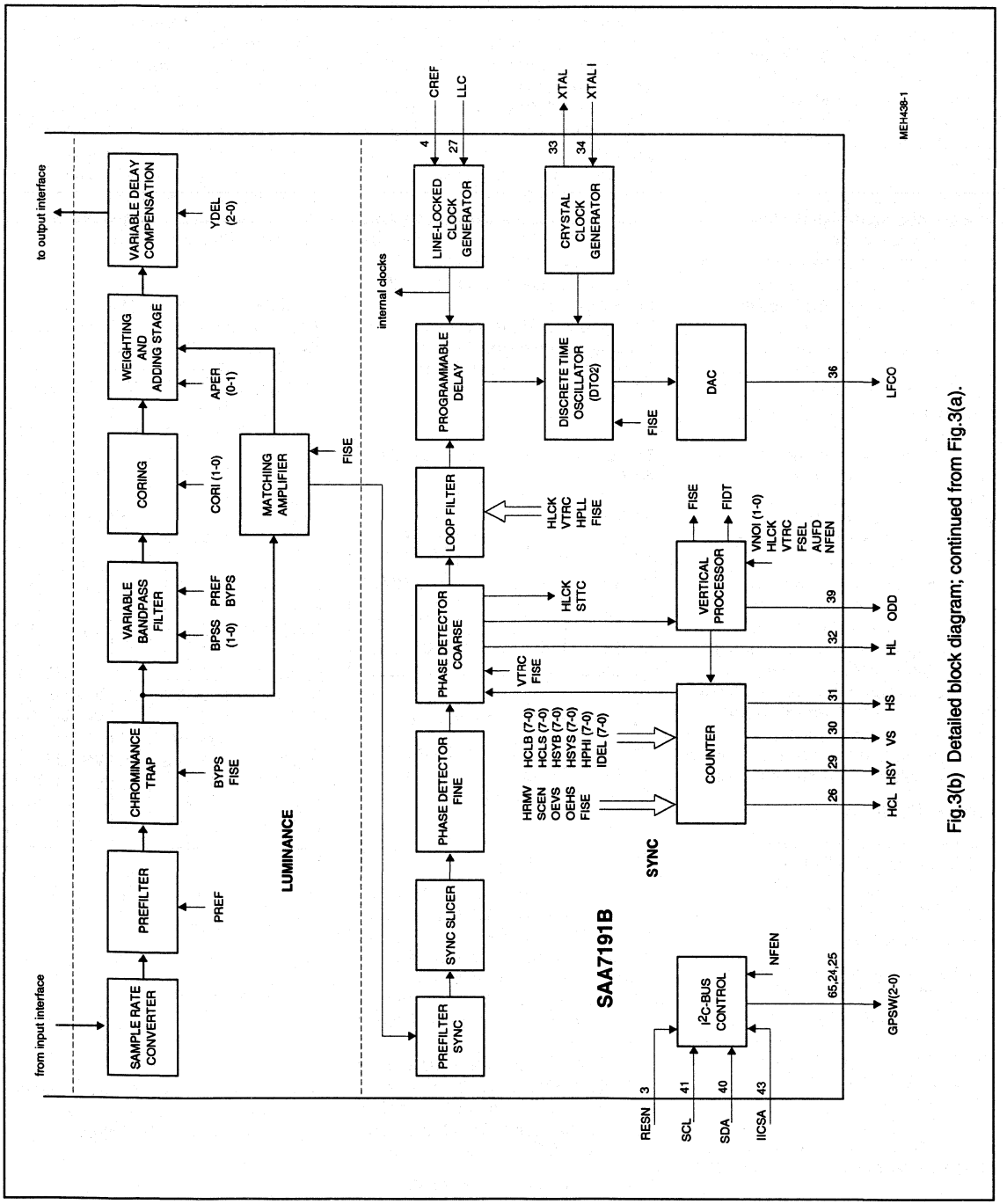


Fig.3(b) Detailed block diagram; continued from Fig.3(a).

Luminance processor

The luminance input signal, a digital CVBS format or an 8-bit luminance format (S-VHS, Hi8), is fed through a sample rate converter to reduce the data rate to 14.75 MHz for PAL and SECAM (12.2727 MHz for NTSC), Fig.3(b).

Sample rate is converted by means of a switchable pre-filter. High frequency components are emphasized to compensate for loss in the following chrominance trap filter. This chrominance trap filter (f_0 = 4.43 MHz or f_0 = 3.58 MHz centre frequency selectable) eliminates most of the colour carrier signal, therefore, it must be by-passed for S-Video (S-VHS and Hi8) signals.
The high frequency components of the luminance signal can be "peaked" (control for sharpness improvement via the I²C-bus) in two bandpass filters with selectable transfer characteristic.
A coring circuit with selectable characteristic improves the signal once more, this signal is then added to the original ("unpeaked") signal. A switchable amplifier achieves a common DC amplification, because the DC gains are different in both chrominance trap modes.
The improved luminance signal is fed to the variable delay compensation.

Processing delay

The delay from input to output is 220 LLC cycles if YDEL is set to 0. The processing delay will be influenced in future enhancements.

Synchronization

The luminance output signal is fed to the synchronization stage. Its bandwidth is reduced to 1 MHz in a low-pass filter. The sync pulses are sliced and fed to the phase detectors to be compared with the sub-divided clock frequency.
The resulting output signal is applied to the loop filter to accumulate all phase deviations. Adjustable output signals (e. g. HCL and HSY) are generated according to peripheral requirements (TDA8708A, TDA8709A). The output signals HS, VS and PLIN are locked to the timing reference signal HREF (Figures 6 and 7).
There is no absolute timing reference guaranteed between the input signal and the HREF signal as further improvements to the circuit may change the total processing delay. It is therefore not recommended to use them for applications, which ask for absolute timing accuracy to the input signals.
The loop filter signal drives an oscillator to generate the line frequency control output signal LFCO.

Table 1 Clock frequencies in MHz for 50/60 Hz systems

CLOCK	50 Hz	60 Hz
LLC	29.5	24.545454
LLC2	14.75	12.272727
LLC4	7.375	6.136136
LLC8	3.6875	3.068181

Line locked clock frequency

LFCO is required in an external PLL (SAA7197) to generate the line locked clock frequency.

YUV-bus, digital outputs

The 16-bit YUV-bus transfers digital data from the output interfaces to a feature box, or to the digital-to-analog converter (DAC). Outputs are controlled via the I²C-bus in normal selections, or they are controlled by output enable chain (FEIN on pin 64, Fig.4).
The YUV-bus data rate equals LLC2 in Table 1. Timing is achieved by marking each second positive rising edge of the clock LLC in conjunction with CREF (clock reference).

YUV-bus formats 4:2:2 and 4:1:1

The output signals Y7 to Y0 are the bits of the digital luminance signal. The output signals UV7 to UV0 are the bits of the multiplexed colour-difference signals (B–Y) and (R–Y). The frame in the following tables is the time, required to transfer a full set of samples. In case of 4 : 2 : 2 format two luminance samples are transmitted in comparision to one U and one V sample within one frame.

Table 2 4 : 2 : 2 format (768 pixels per line for 50 Hz system; 640 pixels per line for 60 Hz system)

OUTPUT	PIXEL BYTE SEQUENCE					
Y0 (LSB)	Y0	Y0	Y0	Y0	Y0	Y0
Y1	Y1	Y1	Y1	Y1	Y1	Y1
Y2	Y2	Y2	Y2	Y2	Y2	Y2
Y3	Y3	Y3	Y3	Y3	Y3	Y3
Y4	Y4	Y4	Y4	Y4	Y4	Y4
Y5	Y5	Y5	Y5	Y5	Y5	Y5
Y6	Y6	Y6	Y6	Y6	Y6	Y6
Y7 (MSB)	Y7	Y7	Y7	Y7	Y7	Y7
UV0 (LSB)	U0	V0	U0	V0	U0	V0
UV1	U1	V1	U1	V1	U1	V1
UV2	U2	V2	U2	V2	U2	V2
UV3	U3	V3	U3	V3	U3	V3
UV4	U4	V4	U4	V4	U4	V4
UV5	U5	V5	U5	V5	U5	V5
UV6	U6	V6	U6	V6	U6	V6
UV7(MSB)	U7	V7	U7	V7	U7	V7
Y frame	0	1	2	3	4	5
UV frame	0		2		4	

Notes to Table 2

1. Data rate: LLC2
2. Sample frequency:
   Y LLC2
   U LLC4
   V LLC4

The quoted frequencies are valid on the YUV-bus. The time frames are controlled by the HREF signal.

Table 3 4 : 1 : 1 format (768 pixels per line for 50 Hz system and 640 pixels per line for 60 Hz system)

OUTPUT	PIXEL BYTE SEQUENCE							
Y0 (LSB)	Y0	Y0	Y0	Y0	Y0	Y0	Y0	Y0
Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1	Y1
Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2	Y2
Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3	Y3
Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4	Y4
Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5
Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6	Y6
Y7 (MSB)	Y7	Y7	Y7	Y7	Y7	Y7	Y7	Y7
UV0 (LSB)	0	0	0	0	0	0	0	0
UV1	0	0	0	0	0	0	0	0
UV2	0	0	0	0	0	0	0	0
UV3	0	0	0	0	0	0	0	0
UV4	V6	V4	V2	V0	V6	V4	V2	V0
UV5	V7	V5	V3	V1	V7	V5	V3	V1
UV6	U6	U4	U2	U0	U6	U4	U2	U0
UV7 (MSB)	U7	U5	U3	U1	U7	U5	U3	U1
Y frame	0	1	2	3	4	5	6	7
UV frame	0				4			

Fast enable is achieved by setting input FEIN to LOW. This signal is used to control fast switching on the digital YUV-bus. HIGH on this pin forces the Y and U/V outputs to a high-impedance state. The signal FEON is LOW when the Y and U/V outputs are in this high-impedance state (Fig.4).
The quoted frequencies are valid on the YUV-bus. The time frames are controlled by the HREF signal.

Notes to Table 3

Data rate:		LLC2
sample frequency:	Y	LLC2
	U	LLC8
	V	LLC8

Table 4 Digital output control

OEDY	OEDC	FEIN	Y(7:0)	UV(7:0)	FEON
X	X	0	active	active	1
0	0	1	Z	Z	0
0	1	1	Z	active	1
1	0	1	active	Z	1
1	1	X	active	active	1

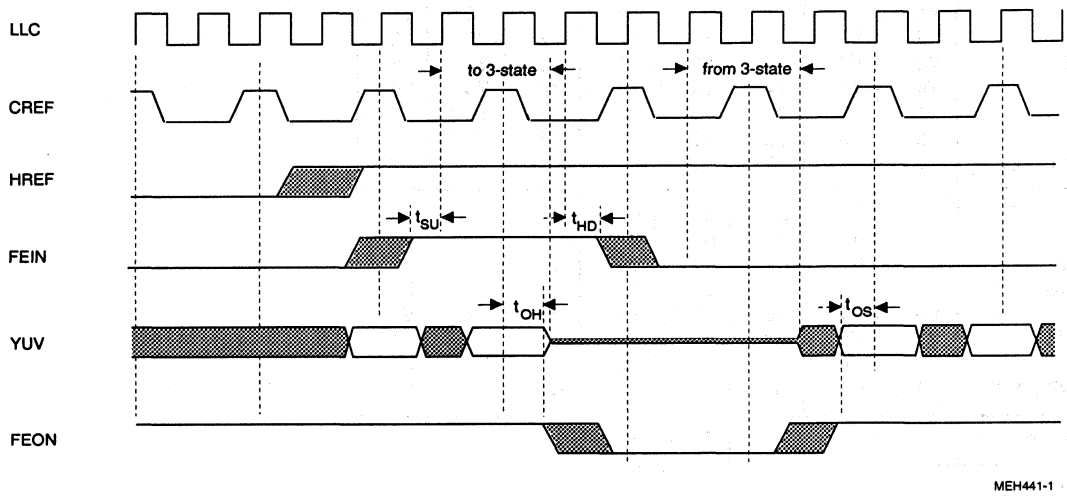
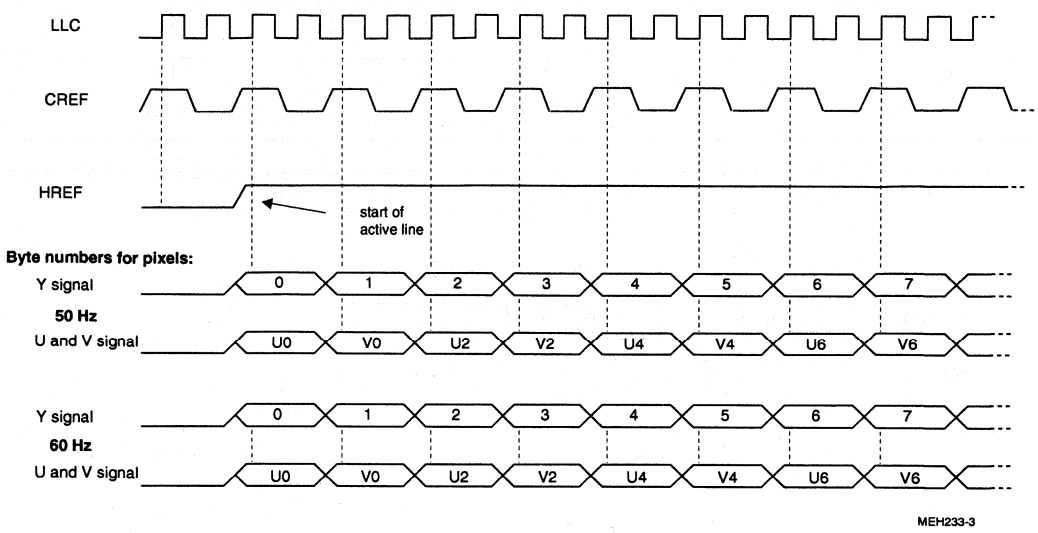


Fig.4 Timing example of fast enable input FEIN.



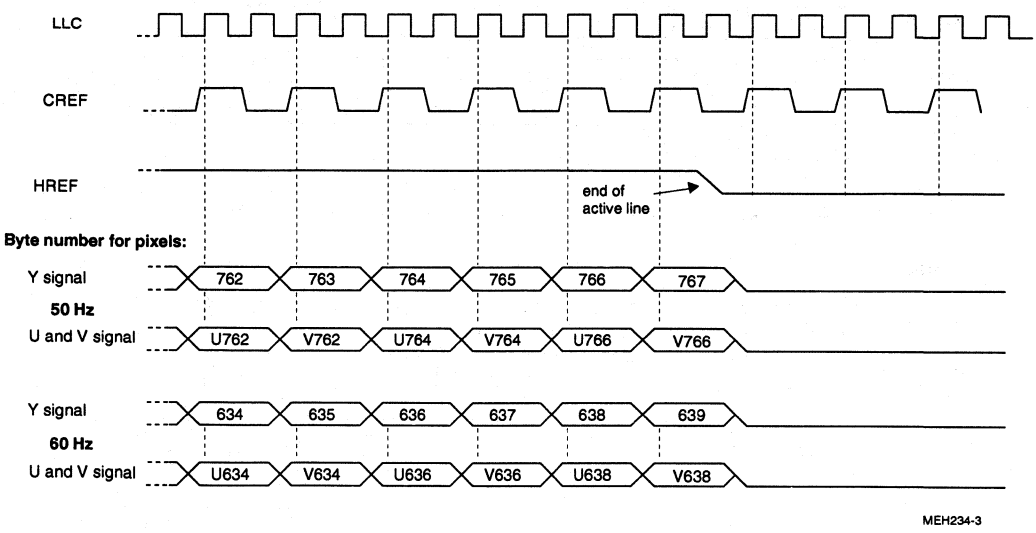


Fig.5 Line control by HREF in 4:2:2 format for 50 Hz and 60 Hz systems.

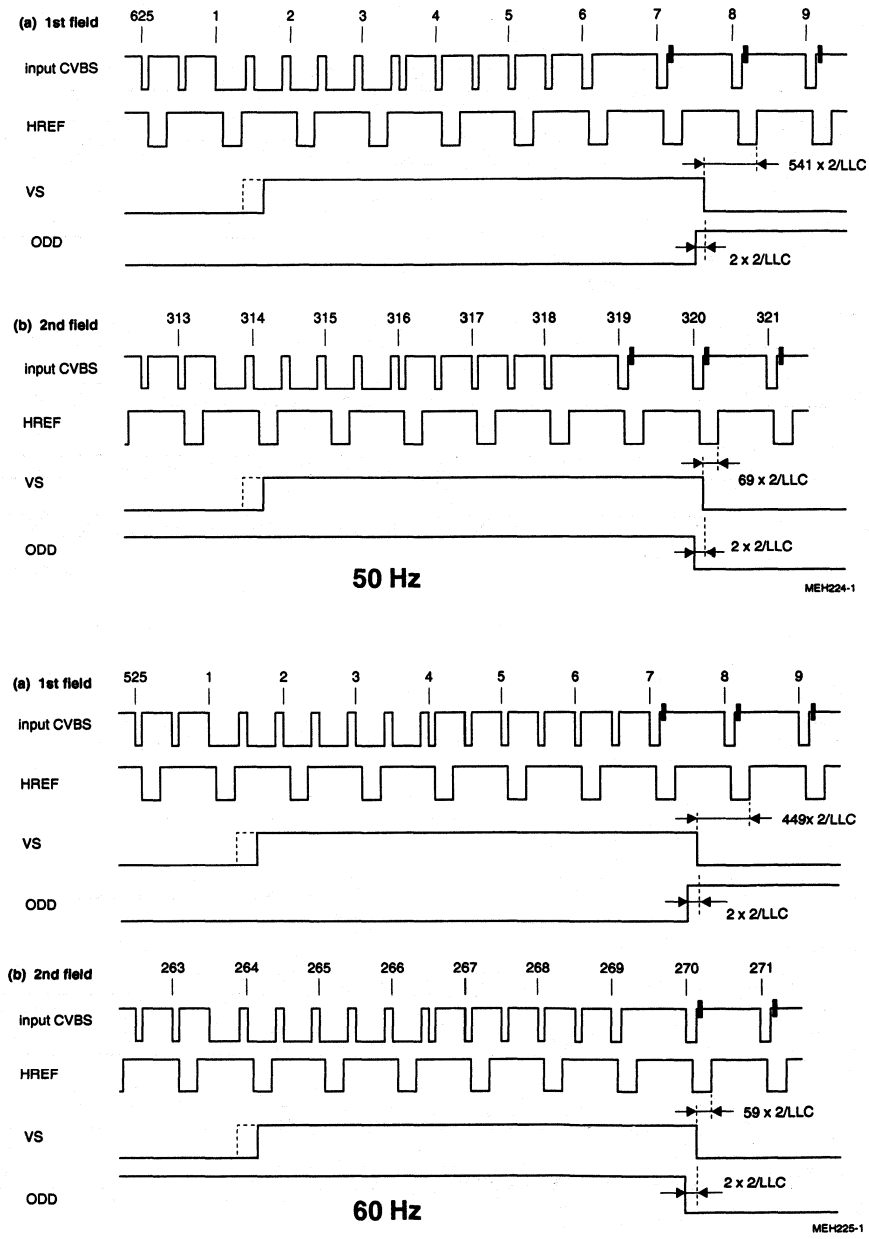


Fig.6 Vertical timing diagram for 50 / 60 Hz.

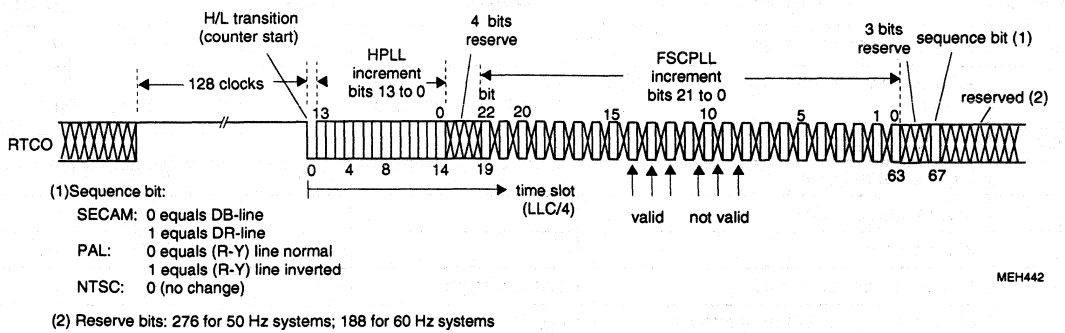


Fig.7 RTCO timing.

8. LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); ground pins 19, 35, 38, 51 and 67 as well as supply pins 5, 18, 28, 37 and 52 connected together.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (pins 5, 18, 28, 37, 52)	−0.5	7.0	V
$V_{diff\ GND}$	difference voltage $V_{SS\ A} - V_{SS\ (1\ to\ 4)}$	-	±100	mV
V_I	voltage on all inputs	−0.5	V_{DD}+0.5	V
V_O	voltage on all outputs ($I_{O\ max}$ = 20 mA)	−0.5	V_{DD}+0.5	V
P_{tot}	total power dissipation	-	2.5	W
T_{stg}	storage temperature range	−65	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling* for all pins	-	±2000	V

* Equivalent to discharging a 100 pF capacitor through an 1.5 kΩ series resistor.

9. CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; T_{amb} = 0 to 70 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage range (pins 5, 18, 28, 37, 52)		4.5	5	5.5	V
I_{DD}	total supply current (pins 5, 18, 28, 37, 52)	V_{DD} = 5 V; inputs LOW; outputs not connected	-	100	250	mA
I²C-bus, SDA and SCL (pins 40 and 41)						
V_{IL}	input voltage LOW		−0.5	-	1.5	V
V_{IH}	input voltage HIGH		3	-	V_{DD}+0.5	V
$I_{40,41}$	input current		-	-	±10	µA
I_{ACK}	output current on pin 40	acknowledge	3	-	-	mA
V_{OL}	output voltage at acknowledge	I_{40} = 3 mA	-	-	0.4	V
Data clock and control inputs (pins 3, 4, 6 to 17, 20 to 23, 27, 34, 43 and 64), Fig.10						
V_{IL}	LLC input voltage LOW (pin 27)		−0.5	-	0.6	V
V_{IH}	LLC input voltage HIGH		2.4	-	V_{DD}+0.5	V
V_{IL}	other input voltage LOW		−0.5	-	0.8	V
V_{IH}	other input voltage HIGH		2.0	-	V_{DD}+0.5	V
I_{LI}	input leakage current		-	-	10	µA
C_I	input capacitance	data inputs; note 1	-	-	8	pF
		I/O high-ohmic	-	-	8	pF
		clock inputs	-	-	10	pF
$t_{SU.DAT}$	input data set-up time	Fig.8	11	-	-	ns
$t_{HD.DAT}$	input data hold time		3	-	-	ns
LFCO output (pin 36)						
V_o	output signal (peak-to-peak value)	note 2	1.4	-	2.6	V
V_{36}	output voltage range		1	-	V_{DD}	V
YUV-bus, HREF and VS outputs (pins 30, 42, 45 to 50 and pins 53 to 62)			Figures 11 and 15 to 25			
V_{OL}	output voltage LOW	notes 1 and 2	0	-	0.6	V
V_{OH}	output voltage HIGH		2.4	-	V_{DD}	V
C_L	load capacitance		15	-	50	pF
Control outputs (pins 24 to 26, 29, 31, 32, 39, 63, 65,66 and 68); Fig.12						
V_{OL}	output voltage LOW	notes 1 and 2	0	-	0.6	V
V_{OH}	output voltage HIGH		2.4	-	V_{DD}	V
C_L	load capacitance		7.5	-	25	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing of YUV-bus and control outputs		Fig.7				
t_{OH}	output signal hold time	YUV, HREF, VS at C_L = 15 pF	13	-	-	ns
		controls at C_L = 7.5 pF	13	-	-	ns
t_{OS}	output set-up time	YUV, HREF, VS at C_L = 50 pF;	14	-	-	ns
		controls at C_L = 25 pF	14	-	-	ns
t_{SZ}	data output disable transition time	to 3-state condition	16	-	-	ns
t_{ZS}	data output enable transition time	from 3-state condition	14	-	-	ns
t_{RTCO}	RTCO timing			Fig.7		
Chrominance PLL						
f_C	catching range		±400	-	-	Hz
Crystal oscillator		Fig.9				
f_n	nominal frequency	3rd harmonic	-	26.8	-	MHz
$\Delta f / f_n$	permissible deviation f_n		-	-	±50	10^{-6}
	temperature deviation from f_n		-	-	±20	10^{-6}
X1	crystal specification:					
	temperature range T_{amb}		0	-	70	°C
	load capacitance C_L		8	-	-	pF
	series resonance resistance R_S		-	50	80	Ω
	motional capacitance C_1		-	1.1±20%	-	fF
	parallel capacitance C_0		-	3.5±20%	-	pF
	Philips catalogue number		9922 520 30004			
Line locked clock input LLC (pin 27)		Fig.8				
t_{LLC}	cycle time	note 3	31	-	45	ns
t_p	duty factor	t_{LLCH} / t_{LLC}	40	-	60	%
t_r	rise time		-	-	5	ns
t_f	fall time		-	-	6	ns

Notes to the characteristics

1. Data output signals are Y7 to Y0 and UV7 to UV0. All others are control output signals.
2. Levels are measured with load circuit. YUV-bus, HREF and VS outputs with 1.2 kΩ in parallel to 50 pF at 3 V (TTL load); LFCO output with 10 kΩ in parallel to 15 pF and other outputs with 1.2 kΩ in parallel to 25 pF at 3 V (TTL load).
3. t_{SU}, t_{HD}, t_{OH} and t_{OD} include t_r and t_f.

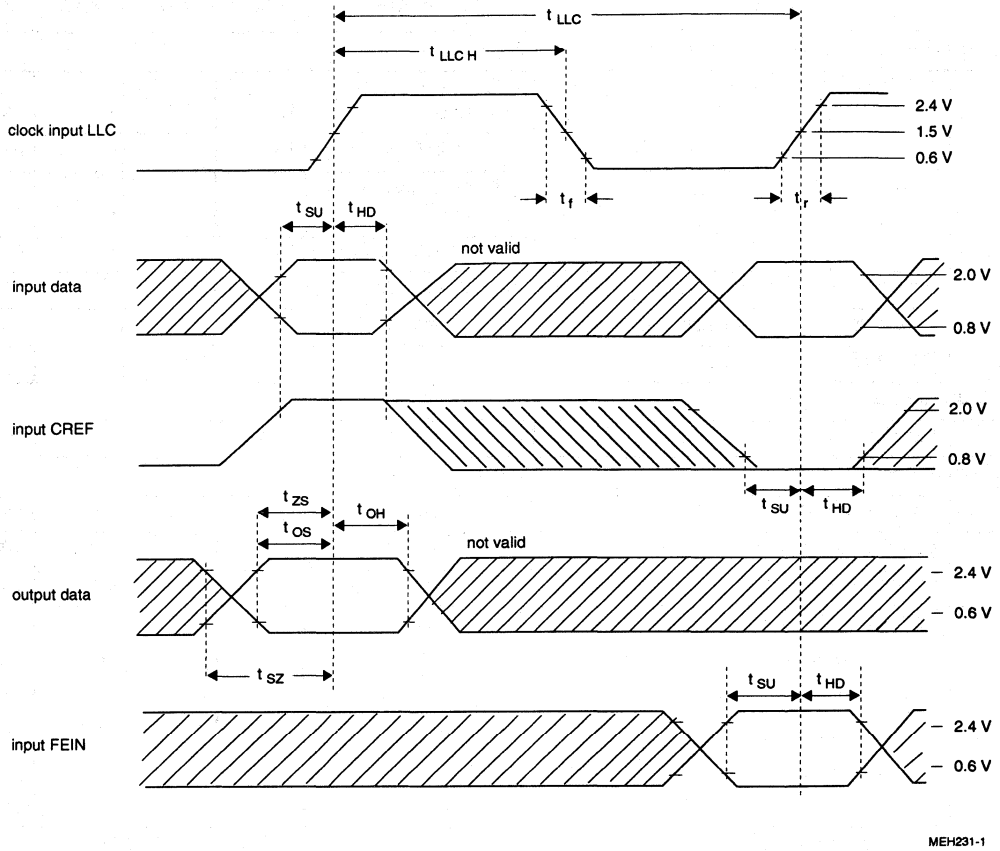


Fig.8 Data input and output timing diagram.

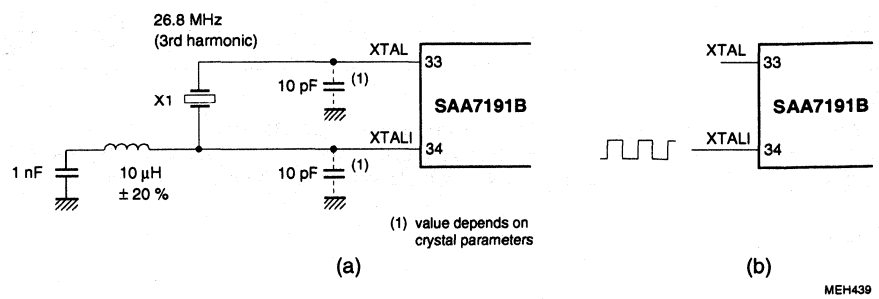
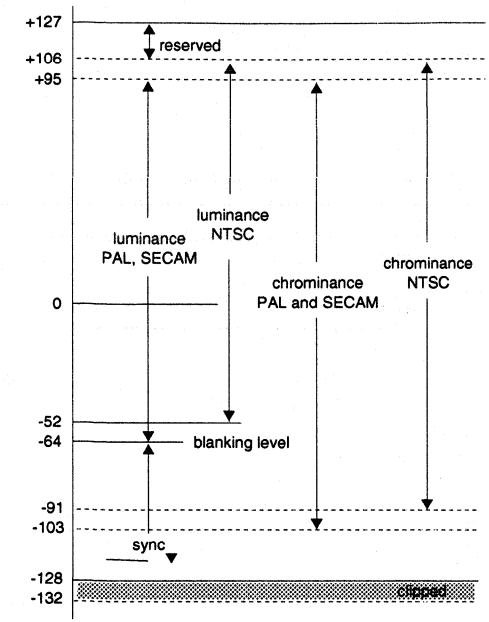
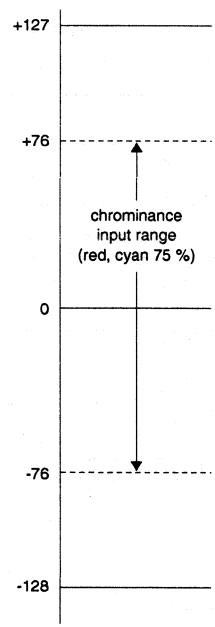


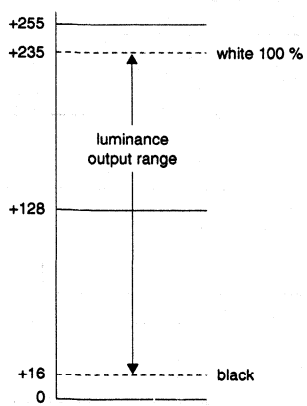
Fig.9 Oscillator application (a) and optional clock from external source (b).



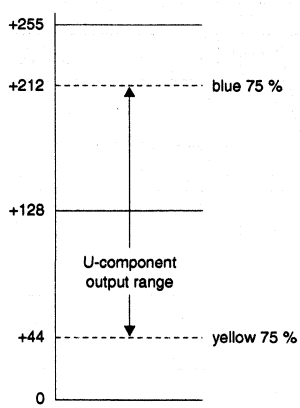
(a) CVBS7 to CVBS0 input signal range.



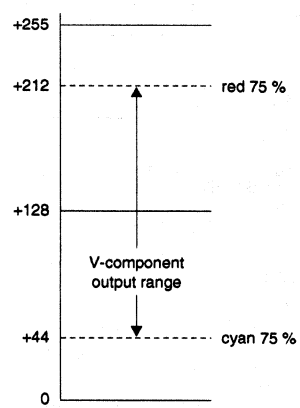
(b) CHR7 to CHR0 input signal range.



(c) Y output signal range.



(d) U output signal range (B-Y).



(e) V output signal range (R-Y).

MEH254-2

Notes: 1. All levels are related to EBU colour bar.
2. Values in decimal at 100 % luminance and 75 % chrominance amplitude.

Fig.10 Input and output signal ranges.

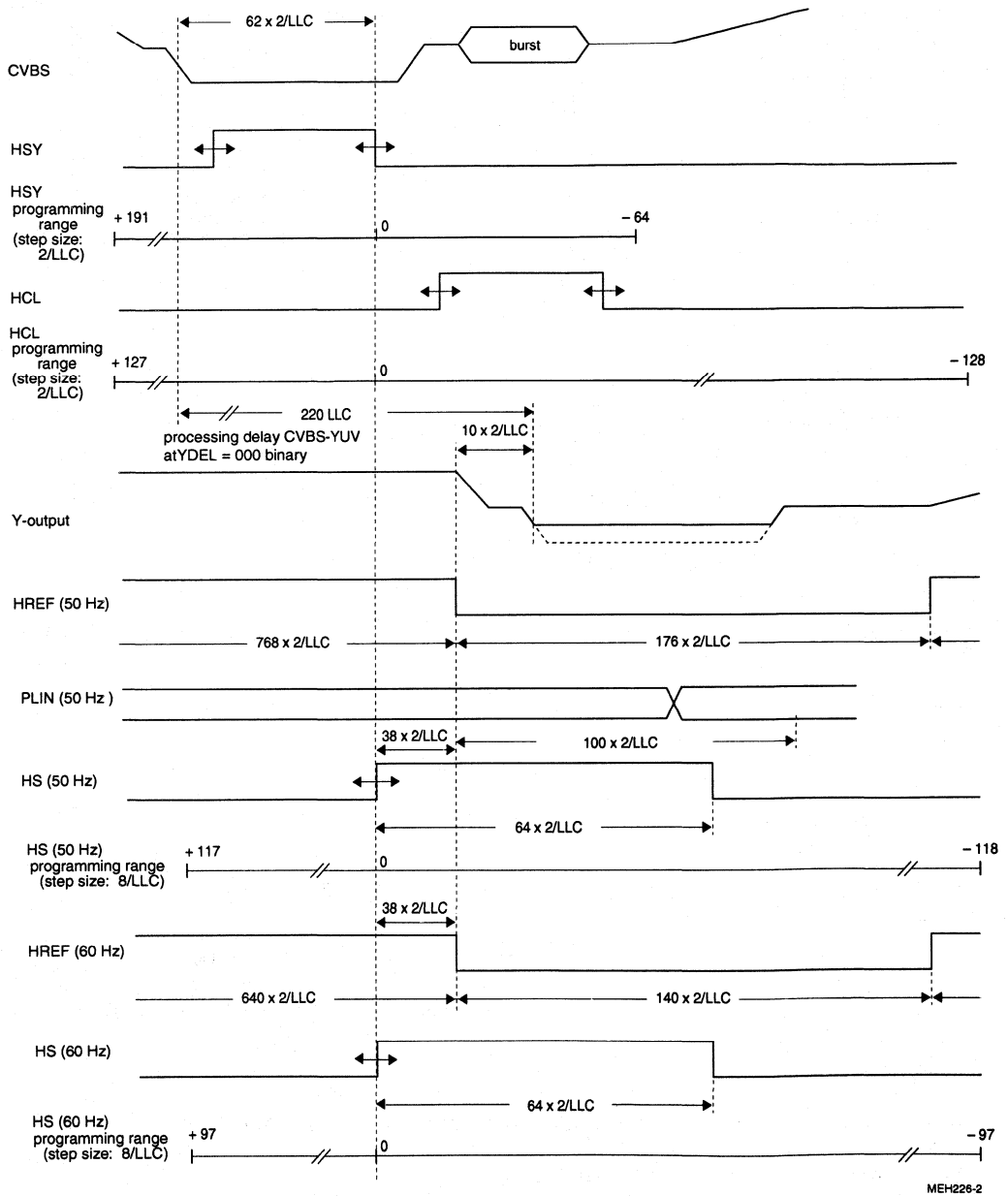


Fig.12 Horizontal sync at HRMV = 0 and HRFS = 0 for 50/60 Hz (signals HSY, HCL, HREF and PLIN).

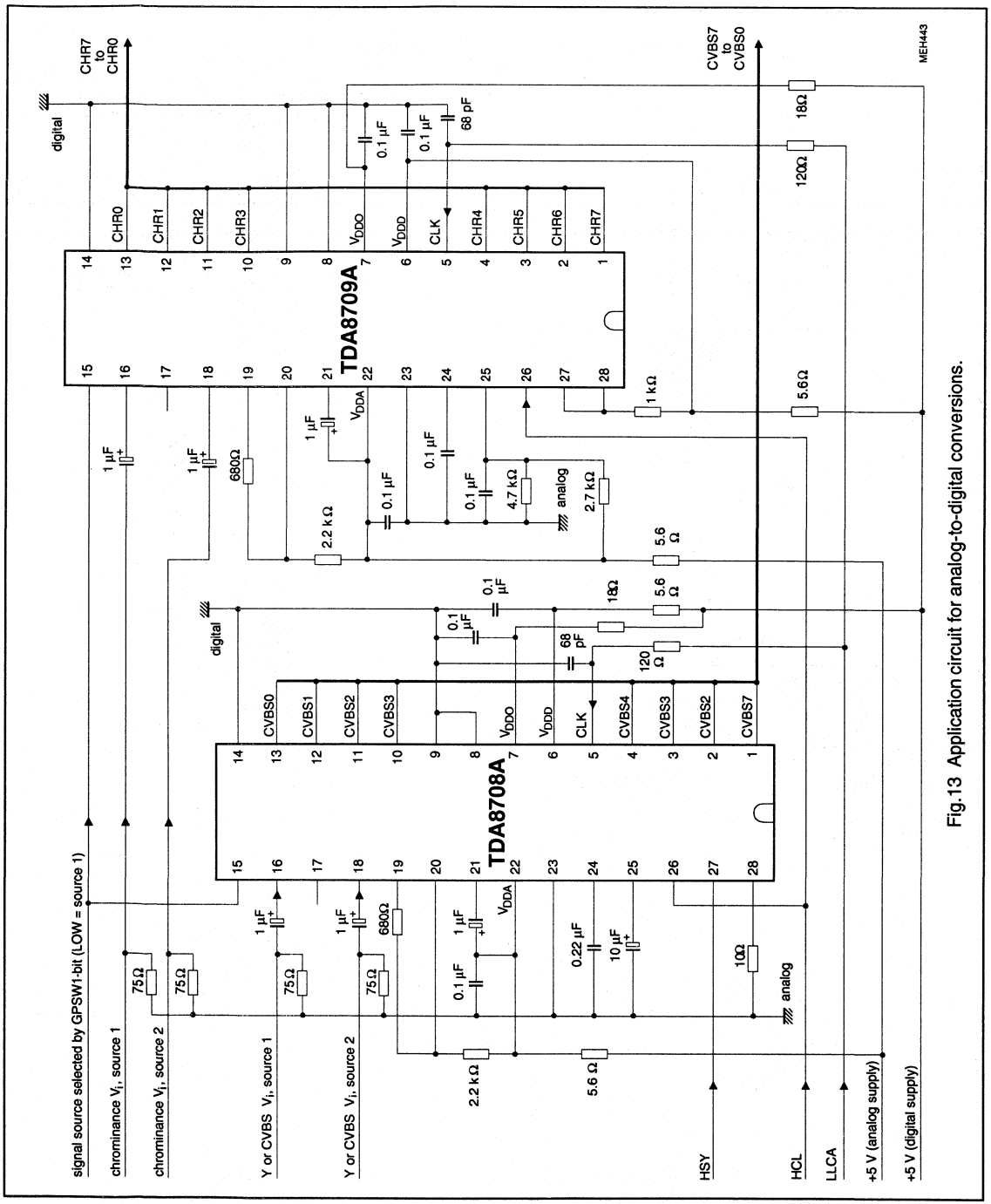


Fig.13 Application circuit for analog-to-digital conversions.

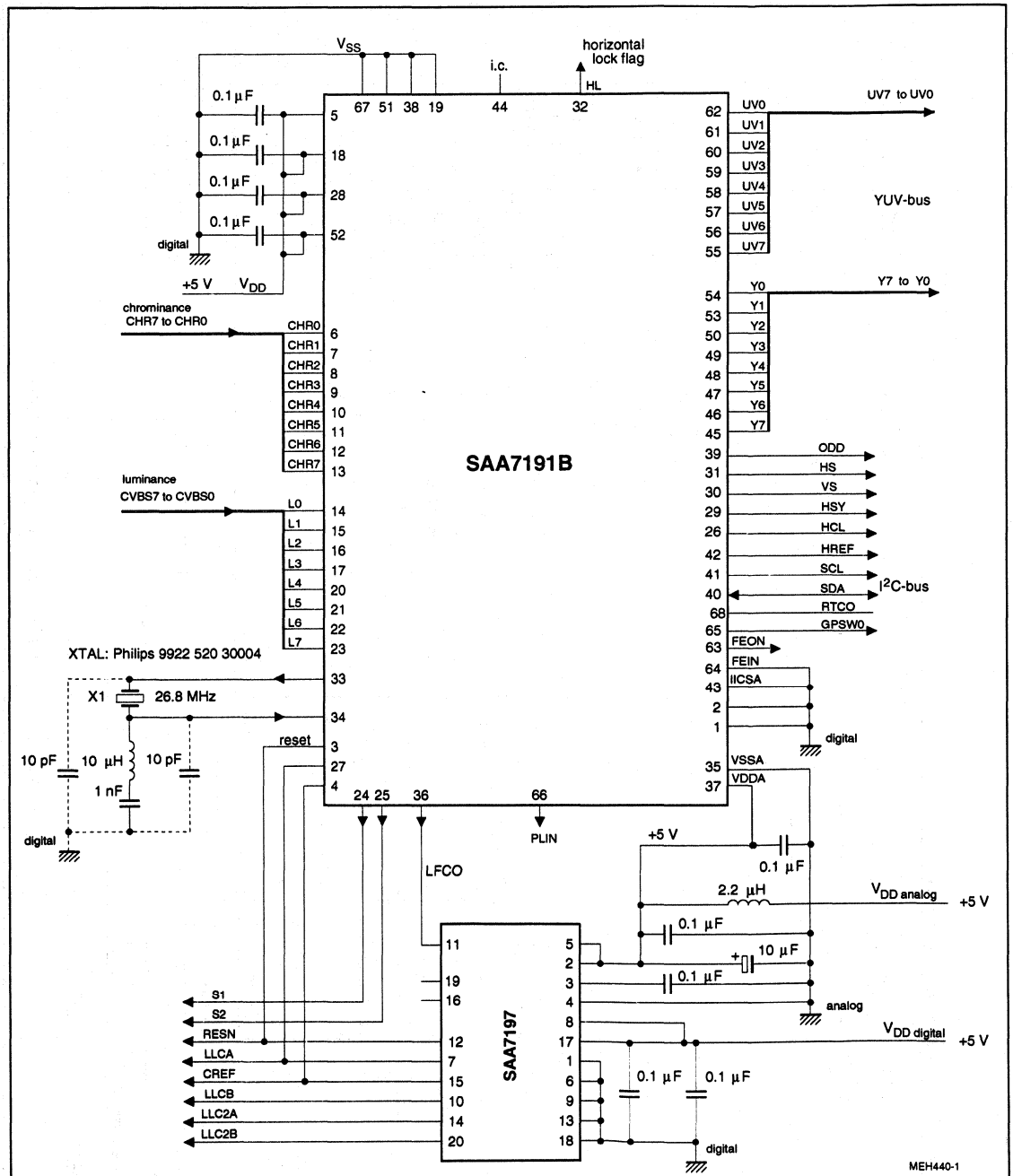


Fig.14 Application circuit for digital multistandard colour decoder.

10. I²C-BUS FORMAT

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA0	A		DATAn	A	P

S = start condition
SLAVE ADDRESS = **1000 101X** (IICSA = LOW) **or 1000 111X** (IICSA = HIGH)
A = acknowledge, generated by the slave
SUBADDRESS* = subaddress byte (Table 5)
DATA = data byte (Table 5)
P = stop condition

X = read/write control bit
X = 0, order to write (the circuit is slave receiver)
X = 1, order to read (the circuit is slave transmitter)

* If more than 1 byte DATA are transmitted, then auto-increment of the subaddress is performed.

Table 5 I²C-bus; DATA for status byte (X = 1 in address byte; 8Bh at IICSA = LOW or 8Fh at IICSA = HIGH).

FUNCTION		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
status byte		STTC	HLCK	FIDT	X	X	X	X	CODE

Function of the bits:

STTC — Horizontal time constant information for future application with logical combfilter only:
0 = TV time constant (slow);
1 = VCR time constant (fast)

HLCK — Horizontal PLL information: 0 = HPLL locked; 1 = HPLL unlocked

FIDT — Field information: 0 = 50 Hz system detected; 1 = 60 Hz system detected

CODE — Colour information: 0 = no colour detected; 1 = colour detected

Table 6 I²C-bus; subaddress and data bytes for writing (X = 0 in address byte; 8Ah at IICSA = LOW or 8Eh at IICSA = HIGH).

FUNCTION	SUBADDRESS	DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Increment delay	00	IDEL7	IDEL6	IDEL5	IDEL4	IDEL3	IDEL2	IDEL1	IDEL0
H sync begin, 50 Hz	01	HSYB7	HSYB6	HSYB5	HSYB4	HSYB3	HSYB2	HSYB1	HSYB0
H sync stop, 50 Hz	02	HSYS7	HSYS6	HSYS5	HSYS4	HSYS3	HSYS2	HSYS1	HSYS0
H clamp begin, 50 Hz	03	HCLB7	HCLB6	HCLB5	HCLB4	HCLB3	HCLB2	HCLB1	HCLB0
H clamp stop, 50 Hz	04	HCLS7	HCLS6	HCLS5	HCLS4	HCLS3	HCLS2	HCLS1	HCLS0
H sync after PHI1, 50 Hz	05	HPHI7	HPHI6	HPHI5	HPHI4	HPHI3	HPHI2	HPHI1	HPHI0
Luminance control	06	BYPS	PREF	BPSS1	BPSS0	CORI1	CORI0	APER1	APER0
Hue control	07	HUEC7	HUEC6	HUEC5	HUEC4	HUEC3	HUEC2	HUEC1	HUEC0
Colour killer threshold QAM	08	CKTQ4	CKTQ3	CKTQ2	CKTQ1	CKTQ0	0	0	0
Colour-killer threshold SECAM	09	CKTS4	CKTS3	CKTS2	CKTS1	CKTS0	0	0	0
PAL switch sensitivity	0A	PLSE7	PLSE6	PLSE5	PLSE4	PLSE3	PLSE2	PLSE1	PLSE0
SECAM switch sensitivity	0B	SESE7	SESE6	SESE5	SESE4	SESE3	SESE2	SESE1	SESE0
Chroma gain control settings	0C	COLO	LFIS1	LFIS0	0	0	0	0	0
Standard/mode control	0D	VTRC	0	0	0	NFEN	HRMV	GPSW0	SECS
I/O and clock control	0E	HPLL	OEDC	OEHS	OEVS	OEDY	CHRS	GPSW2	GPSW1
Control #1	0F	AUFD	FSEL	SXCR	SCEN	OFTS	YDEL2	YDEL1	YDEL0
Control #2	10	0	0	0	0	0	HRFS	VNOI1	VNOI0
Chroma gain reference	11	CHCV7	CHCV6	CHCV5	CHCV4	CHCV3	CHCV2	CHCV1	CHCV0
Not used, is acknowledged	12	0	0	0	0	0	0	0	0
Not used, is acknowledged	13	0	0	0	0	0	0	0	0
H sync begin, 60 Hz	14	HS6B7	HS6B6	HS6B5	HS6B4	HS6B3	HS6B2	HS6B1	HS6B0
H sync stop, 60 Hz	15	HS6S7	HS6S6	HS6S5	HS6S4	HS6S3	HS6S2	HS6S1	HS6S0
H clamp begin, 60 Hz	16	HC6B7	HC6B6	HC6B5	HC6B4	HC6B3	HC6B2	HC6B1	HC6B0
H clamp stop, 60 Hz	17	HC6S7	HC6S6	HC6S5	HC6S4	HC6S3	HC6S2	HC6S1	HC6S0
H sync after PHI1, 60 Hz	18	HP6I7	HP6I6	HP6I5	HP6I4	HP6I3	HP6I2	HP6I1	HP6I0

Note to Table 6

- Default values of register contents to obtain a picture see Table 6.
- All unused control bits must be programmed with "0" (zero) as indicated in Table 5.

Function of the bits of Table 5

IDEL7 to IDEL0 "00"	Increment delay time (dependent on application), step size = 4 / LLC. The delay time is selectable from –4 / LLC (–1 decimal multiplier) to –1024 / LLC (–256 decimal multiplier) equals data FF to 00 (hex). Different processing times in the chrominance channel and the clock generation could result in phase errors in the chrominance processing by transients in clock frequency. An adjustable delay (IDEL) is necessary if the processing time in the clock generation is unknown.
HSYB7 to HSYB0 "01"	Horizontal sync begin for 50 Hz, step size = 2 / LLC. The delay time is selectable from –382/LLC (+191 decimal multiplier) to +128/LLC (–64 decimal multiplier) equals data BF to C0 (hex). Two´s complement numbers with "hidden" sign-bit. The sign-bit is generated internally by evaluating the MSB and the MSB–1 bits.
HSYS7 to HSYS0 "02"	Horizontal sync stop for 50 Hz, step size = 2 / LLC. The delay time is selectable from –382/LLC (+191 decimal multiplier) to +128/LLC (–64 decimal multiplier) equals data BF to C0 (hex). Two´s complement numbers with "hidden" sign-bit. The sign-bit is generated internally by evaluating the MSB and the MSB–1 bits.
HCLB7 to HCLB0 "03"	Horizontal clamp start for 50 Hz, step size = 2 / LLC. The delay time is selectable from –254/LLC (+127 decimal multiplier) to +256/LLC (–128 decimal multiplier) equals data 7F to 80 (hex).
HCLS7 to HCLS0 "04"	Horizontal clamp stop for 50 Hz, step size = 2 / LLC. The delay time is selectable from –254/LLC (+127 decimal multiplier) to +256/LLC (–128 decimal multiplier) equals data 7F to 80 (hex).
HPHI7 to HPHI0 "05"	Horizontal sync after PHI1 for 50 Hz, step size = 8 / LLC. The delay time is selectable from –936 /LLC (+117 decimal multiplier) to +944 /LLC (–118 decimal multiplier) equals data 75 to 8A (hex).
BYPS "06"	input mode select bit: 0 = CVBS mode (chrominance trap active) 1 = S-Video mode (chrominance trap bypassed)
PREF	use of pre-filter: 0 = pre-filter off; 1 = pre-filter on; PREF may be used if chrominance trap is active.
BPSS1 to BPSS0	Aperture bandpass to select different characteristics with maximums (0.2 to 0.3 x LLC / 2): BPSS1 BPSS0 | characteristics 0 0 |) 0 1 |) Figures 16 to 25 1 0 |) 1 1 |)
CORI1 to CORI0 "06"	Coring range for high frequency components according to 8-bit luminance, Fig.15. CORI1 CORI0 | coring 0 0 | coring off 0 1 | ±1 LSB 1 0 | ±2 LSB 1 1 | ±3 LSB

<table>
<tr><td>APER1 to APER0
"06"</td><td>Aperture bandpass filter weights high frequency components of luminance signal:
<table>
<tr><th>APER1</th><th>APER0</th><th>factor</th></tr>
<tr><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>0.25</td></tr>
<tr><td>1</td><td>0</td><td>0.5</td></tr>
<tr><td>1</td><td>1</td><td>1</td></tr>
</table>
Figures 16 to 25</td></tr>
<tr><td>HUE7 to HUE0
"07"</td><td>Hue control from +178.6° to –180.0°, equals data bytes 7F to 80 (hex); 0° equals 00.</td></tr>
<tr><td>CKTQ4 to CKTQ0
"08"</td><td>Colour-killer threshold QAM from approximately –30 dB to –18 dB, equals data bytes F8 to 07 (hex)</td></tr>
<tr><td>CKTS4 to CKTS0
"09"</td><td>Colour-killer threshold SECAM from approximately –30 dB to –18 dB, equals data bytes. F8 to 07 (hex)</td></tr>
<tr><td>PLSE7 to PLSE0
"0A"</td><td>PAL switch sensitivity from LOW-to-HIGH (HIGH means immediate sequence correction), equals FF to 00 (hex), MEDIUM equals 80.</td></tr>
<tr><td>SESE7 to SESE0
"0B"</td><td>SECAM switch sensitivity from LOW-to-HIGH (HIGH means immediate sequence correction), equals FF to 00 (hex), MEDIUM equals 80.</td></tr>
<tr><td>COLO
"0C"</td><td>Colour on bit: 0 = automatic colour-killer enabled; 1 = forced colour on.</td></tr>
<tr><td>LFIS1 to LFIS0
"0C"</td><td>Chrominance gain control (AGC filter):
<table>
<tr><th>LFIS1</th><th>LFIS0</th><th></th><th>loop filter time constant</th></tr>
<tr><td>0</td><td>0</td><td>=</td><td>slow</td></tr>
<tr><td>0</td><td>1</td><td>=</td><td>medium</td></tr>
<tr><td>1</td><td>0</td><td>=</td><td>fast</td></tr>
<tr><td>1</td><td>1</td><td>=</td><td>actual gain, stored for test purposes only</td></tr>
</table></td></tr>
<tr><td>VTRC
"0D"</td><td>VTR/TV mode bit : 0 = TV mode (slow time constant); 1 = VTR mode (fast time constant)</td></tr>
<tr><td>NFEN</td><td>SAA7191B-specified functions enable (RTCO, ODD and GPSW0 outputs)
0 = outputs set to high-impedance (circuit equals SAA7191); 1 = outputs active</td></tr>
<tr><td>HRMV
GPSWO</td><td>HREF generation: 0 = like SAA7191; 1 = HREF is 8 x LLC2 clocks earlier
General purpose switch 0: 0 = output pin 65 LOW; 1 = output pin 65 HIGH</td></tr>
<tr><td>SECS</td><td>SECAM mode bit : 0 = other standards; 1 = SECAM</td></tr>
<tr><td>HPLL
"0E"</td><td>Horizontal clock PLL: 0 = PLL closed;
1 = PLL circuit open and horizontal frequency fixed.</td></tr>
<tr><td>OEDC</td><td>Colour-difference output enable: 0 = data outputs UV7 to UV0 can be set to high-impedance via FEIN
1 = data outputs UV7 to UV0 active.</td></tr>
<tr><td>OEHS</td><td>H-sync output enable (pins 31 and 42): 0 = HS and HREF outputs high-impedance
1 = HS and HREF outputs active.</td></tr>
<tr><td>OEVS</td><td>V-sync output enable (pin 30): 0 = VS output high-impedance
1 = VS output active.</td></tr>
</table>

OEDY

Luminance output enable: 0 = data outputs Y7 to Y0 can be set to high-impedance via FEIN
1 = data outputs Y7 to Y0 active.

CHRS

S-VHS bit (chrominance from CVBS or from chrominance input):
0 = controlled by BYPS-bit (subaddress 06)
1 = chrominance from chrominance input (CHR7 to CHR0)

GPSW2 to GPSW1

to "0E"

General purpose switches :

GPSW2	GPSW1	set port output pins 24 (GPSW2) and 25 (GPSW1)
0	0	use is dependent on application
0	1	
1	0	
1	1	

AUFD
"0F"

Automatic field detection: 0 = field selection by FSEL-bit;
1 = automatic field detection.

FSEL

Field select (AUFD-bit = 0): 0 = 50 Hz (625 lines);
1 = 60 Hz (525 lines)

SXCR

SECAM cross-colour reduction: 0 = reduction off;
1 = reduction on.

SCEN

Sync and clamping pulse enable: 0 = HCL and HSY outputs HIGH (pins 26 and 29);
1 = HCL and HSY outputs active

OFTS

Select output format: 0 = 4 : 1 : 1 format;
1 = 4 : 2 : 2 format.

YDEL2 to YDEL0

Luminance delay compensation:

YDEL2	YDEL1	YDEL0	figure
0	0	0	0 x 2 / LLC
0	0	1	+1 x 2 / LLC
0	1	0	+2 x 2 / LLC
0	1	1	+3 x 2 / LLC
1	0	0	–4 x 2 / LLC
1	0	1	–3 x 2 / LLC
1	1	0	–2 x 2 / LLC
1	1	1	–1 x 2 / LLC

step size = 2 / LLC = 67.8 ns for 50 Hz 81.5 ns for 60 Hz

HRFS
"10"

Select HREF position: 0 = normal, HREF is matched to YUV output port;
1 = HREF is matched to CVBS intput port.

VNOI1 to VNOI0

Vertical noise reduction

VNOI1	VNOI0	mode
0	0	normal
0	1	searching window
1	0	auto-deflection
1	1	vertical noise reduction bypassed

CHCV7 to CHCV0 UV "11"	Chrominance gain control (nominal values) for QAM-modulated input signals, effects output amplitude (SECAM with fixed gain): D7 D6 D5 D4 D3 D2 D1 D0 | gain 1 1 1 1 1 1 1 1 | maximum gain : to) 0 1 0 1 1 0 0 1 | CCIR level for PAL)) default programmed : to) values dependend 0 0 1 0 1 1 0 0 | CCIR level for NTSC)) on application : to) 0 0 0 0 0 0 0 0 | minimum gain
HS6B7 to HS6B0 "14"	Horizontal sync begin for 60 Hz, step size = 2 / LLC. The delay time is selectable from –382/LLC (+191 decimal multiplier) to +128/LLC (–64 decimal multiplier) equals data BF to C0 (hex). Two's complement numbers with "hidden" sign-bit. The sign-bit is generated internally by evaluating the MSB and the MSB–1 bits.
HS6S7 to HS6S0 "15"	Horizontal sync stop for 60 Hz, step size = 2 / LLC. The delay time is selectable from –382/LLC (+191 decimal multiplier) to +128/LLC (–64 decimal multiplier) equals data BF to C0 (hex). Two's complement numbers with "hidden" sign-bit. The sign-bit is generated internally by evaluating the MSB and the MSB–1 bits.
HC6B7 to HC6B0 "16"	Horizontal clamp begin for 60 Hz, step size = 2 / LLC. The delay time is selectable from –254/LLC (+127 decimal multiplier) to +256/LLC (–128 decimal multiplier) equals data 7F to 80 (hex).
HC6S7 to HC6S0 "17"	Horizontal clamp stop for 60 Hz, step size = 2 / LLC. The delay time is selectable from –254/LLC (+127 decimal multiplier) to +256/LLC (–128 decimal multiplier) equals data 7F to 80 (hex).
HP6I7 to HP6I0 "18"	Horizontal sync after PHI1 for 60 Hz, step size = 8 / LLC. The delay time is selectable from –776 /LLC (+97 decimal multiplier) to +776 /LLC (–97 decimal multiplier) equals data 61 to 9F (hex).

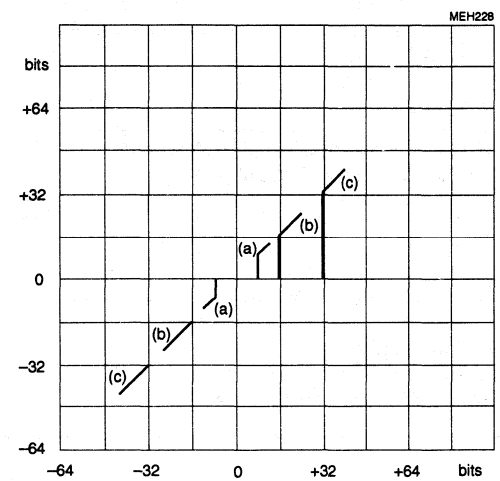


Fig.15 Coring function adjustment by subaddress 06 to affect the bandfilter output signal. The thresholds are related to the 13-bit word width in the luminance processing part and influence the 1LSB to 3LSB (Y0 to Y2) with respect to the 8-bit luminance output

(a) CORI1 = 0; CORI0 = 1

(b) CORI1 = 1; CORI0 = 0

(a) CORI1 = 1; CORI0 = 1

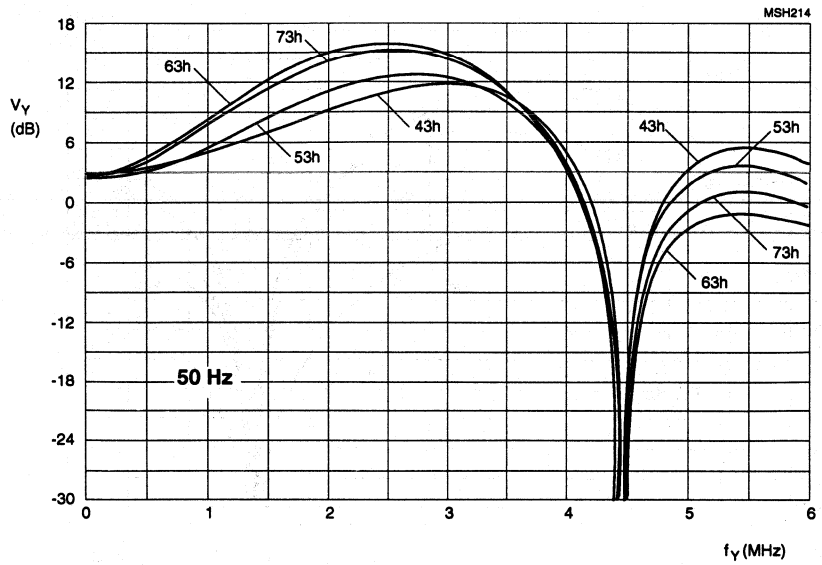


Fig.16 Luminance control in 50 Hz / CVBS mode controllable by subaddress byte 06; pre-filter on and coring off; maximum aperture bandpass filter characteristic.

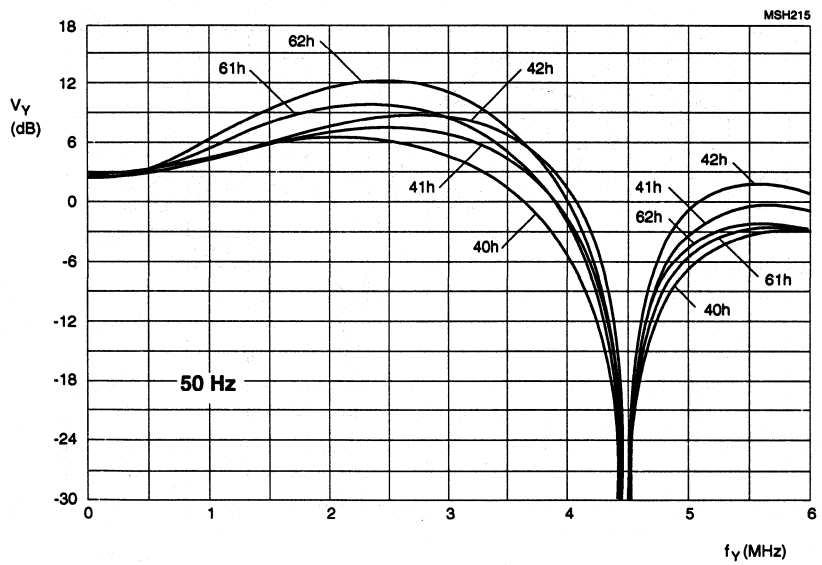


Fig.17 Luminance control in 50 Hz / CVBS mode controllable by subaddress byte 06; pre-filter on and coring off; other aperture bandpass filter characteristics.

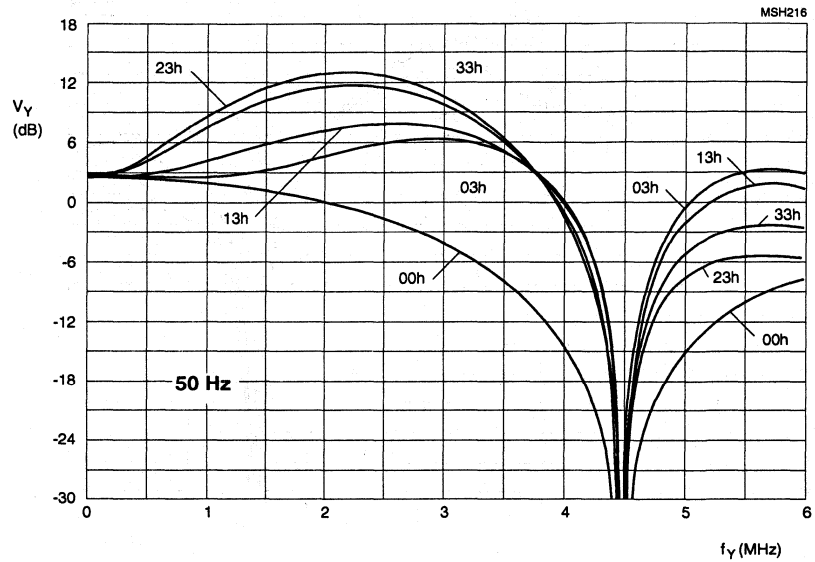


Fig.18 Luminance control in 50 Hz / CVBS mode controllable by subaddress byte 06; pre-filter off and coring off; maximum aperture bandpass filter characteristic.

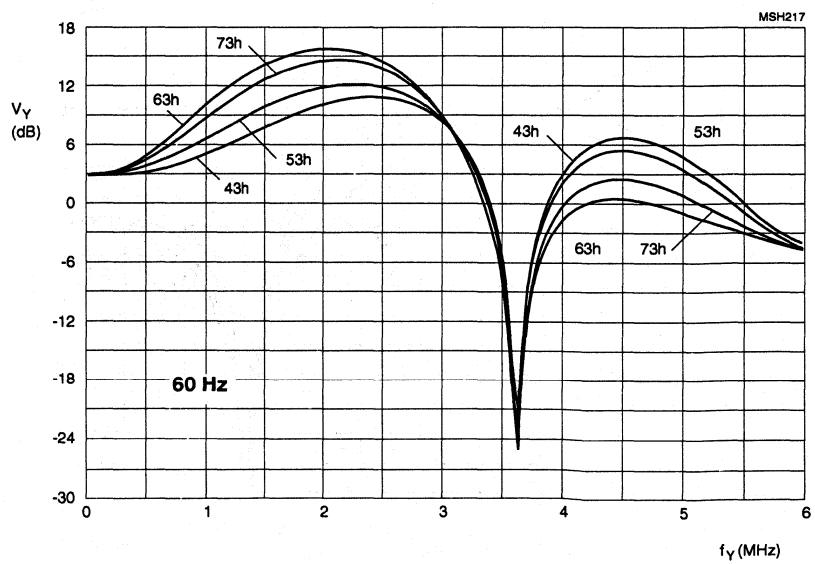


Fig.19 Luminance control in 60 Hz / CVBS mode controllable by subaddress byte 06; pre-filter on and coring off; maximum aperture bandpass filter characteristic.

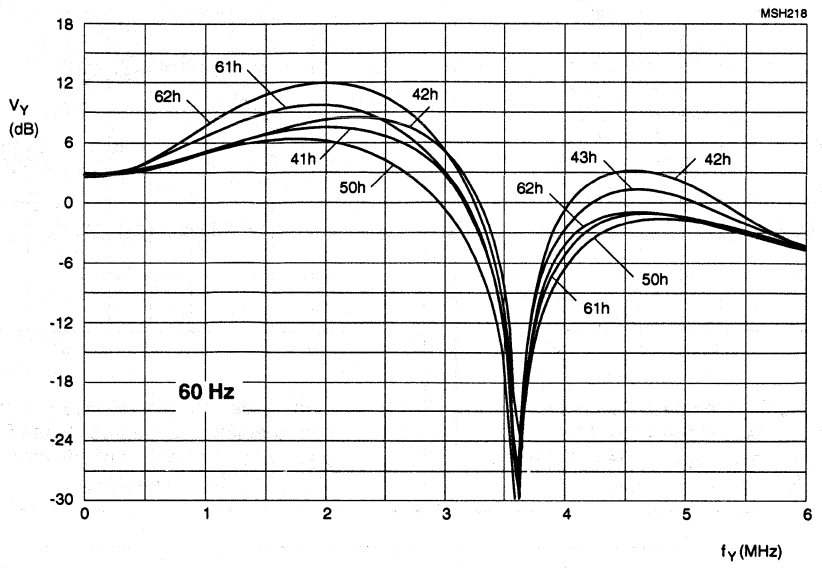


Fig.20 Luminance control in 60 Hz / CVBS mode controllable by subaddress byte 06; pre-filter on and coring off; other aperture bandpass filter characteristics.

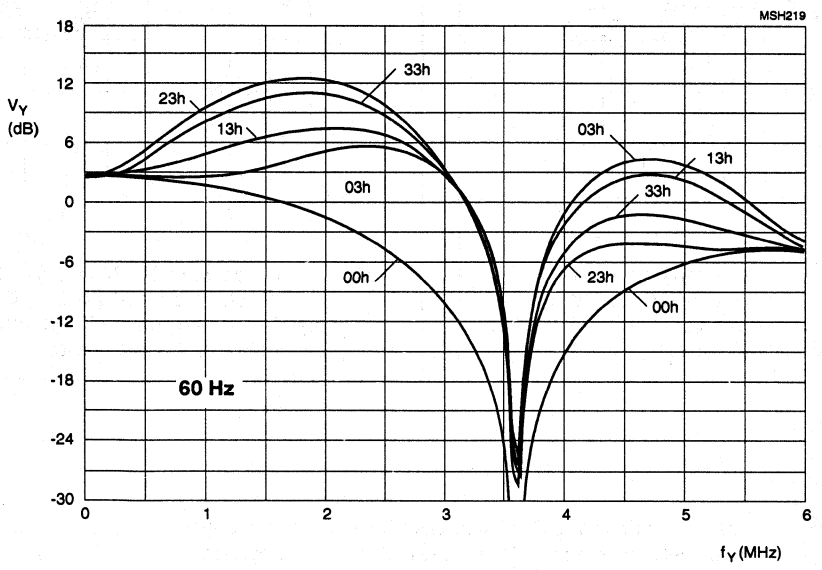


Fig.21 Luminance control in 60 Hz / CVBS mode controllable by subaddress byte 06; pre-filter off and coring off; maximum and minimum aperture bandpass filter characteristics.

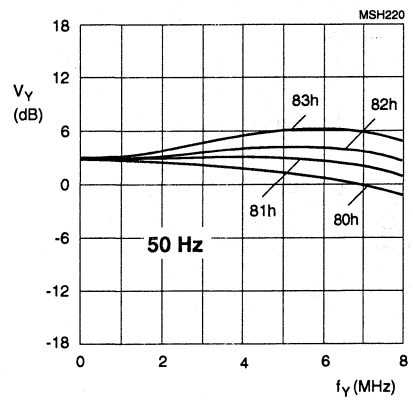


Fig.22 Luminance control in 50 Hz / S-VHS mode controllable by subaddress byte 06; pre-filter off and coring off; different aperture bandpass filter characteristics.

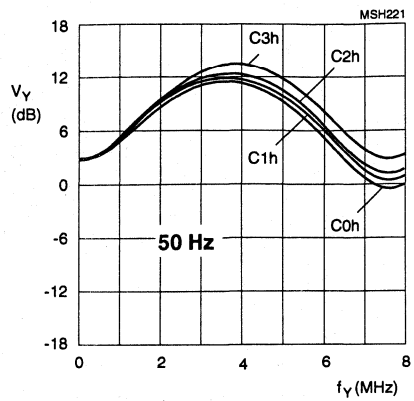


Fig.23 Luminance control in 50 Hz / S-VHS mode controllable by subaddress byte 06; pre-filter on and coring off; different aperture bandpass filter characteristics.

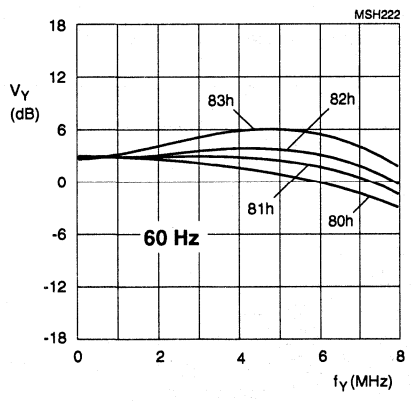


Fig.24 Luminance control in 60 Hz / S-VHS mode controllable by subaddress byte 06; pre-filter off and coring off; different aperture bandpass ffilter characteristics.

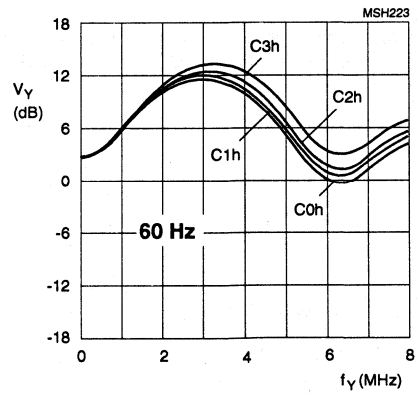


Fig.25 Luminance control in 60 Hz / S-VHS mode controllable by subaddress byte 06; pre-filter on and coring off; different aperture bandpass filter characteristics.

PROGRAMMING EXAMPLE

Coefficients to set operation for application circuits Figures 13 and 14. (All numbers of the Table 6 are hex values). Slave address byte is 8A at pin 43 = 0 V (or 8E at pin 43 = +5 V).

Table 7 Recommended default values

SUBADDRESS	BIT NAME	FUNCTION	VALUE (HEX)
00	IDEL(7-0)	increment delay	50
01	HSYB(7-0)	H sync beginning for 50 Hz	30
02	HSYS(7-0)	H sync stop for 50 Hz	00
03	HCLB(7-0)	H clamping beginning for 50 Hz	E8
04	HCLS(7-0)	H clamping stop for 50 Hz	B6
05	HPHI(7-0)	H sync position for 50 Hz	F4
06	BYPS, PREF, BPSS(1-0) CORI(1-0), APER(1-0)	luminance bandwidth control:	01[1]
07	HUEC(7-0)	hue control (0 degree)	00
08	CKTQ(4-0)	colour-killer threshold QUAM	F8
09	CKTS(4-0)	colour-killer threshold SECAM	F8
0A	PLSE(7-0)	PAL switch sensitivity	90
0B	SESE(7-0)	SECAM switch sensitivity	90
0C	COLO, LFIS(1-0)	chroma gain control settings	00
0D	VTRC, NFEN,HRMV, GPSW0 and SECS	standard/mode control	00[2][4], 01[3][4]
0E	HPLL, OEDC, OEHS, OEVS OEDY, CHRS, GPSW(2-1)	I/O and clock control	79, 7E[5]
0F	AUFD, FSEL, SXCR, SCEN, OFTS, YDEL(2-0)	miscellaneous control #1	91[6], 99[7]
10	HRFS, VNOI(1-0)	miscellaneous control #2	00
11	CHCV(7-0)	chrominance gain nominal value	2C[8], 59[9]
12	-	set to zero	00
13	-	set to zero	00
14	HS6B(7-0)	H sync beginning for 60 Hz	34
15	HS6S(7-0)	H sync stop for 60 Hz	0A
16	HC6B(7-0)	H clamping beginning for 60 Hz	F4
17	HC6S(7-0)	H clamping stop for 60 Hz	CE
18	HP6I(7-0)	H sync position for 60 Hz	F4

Notes to Table 7

(1) dependent on application (Figures 16 to 25)
(2) for QUAM standards
(3) for SECAM
(4) HPLL is in TV mode; value for VCR mode is 80 (81 for SECAM VCR mode)
(5) for Y/C mode
(6) 4:1:1 format
(7) 4:2:2 format
(8) nominal value for UV CCIR level with NTSC source
(9) nominal value for UV CCIR level with PAL source

SAA7197
Clock Generator Circuit for Desktop Video systems (CGC)

FEATURES

- Suitable for Desktop Video systems
- Two different sync sources selectable
- PLL frequency multiplier to generate 4 times of input frequency
- Dividers to generate clocks LLCA, LLCB, LLC2A and LLC2B (2nd and 4th multiples of input frequency)
- PLL mode or VCO mode selectable
- Reset control and power fail detection

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage (pin 5)	4.5	5.0	5.5	V
V_{DDD}	digital supply voltage (pins 8, 17)	4.5	5.0	5.5	V
I_{DDA}	analog supply current	3	-	9	mA
I_{DDD}	digital supply current	10	-	60	mA
V_{LFCO}	LFCO input voltage (peak-to-peak value)	1	-	V_{DDA}	V
f_i	input frequency range	5.5	-	8.0	MHz
V_I	input voltage LOW input voltage HIGH	0 2.0	- -	0.8 V_{DDD}	V V
V_O	output voltage LOW output voltage HIGH	0 2.6	- -	0.6 V_{DDD}	V V
T_{amb}	operating ambient temperature range	0	-	70	°C

GENERAL DESCRIPTION

The SAA7197 generates all clock signals required for a digital TV system suitable for the SAA719x family. The circuit operates in either the phase-locked loop mode (PLL) or voltage controlled oscillator mode (VCO).

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7197P	20	DIP	plastic	SOT146-1
SAA7197T	20	SO	plastic	SOT163-1

PHILIPS

Clock Generator Circuit for Desktop Video systems (CGC)

SAA7197

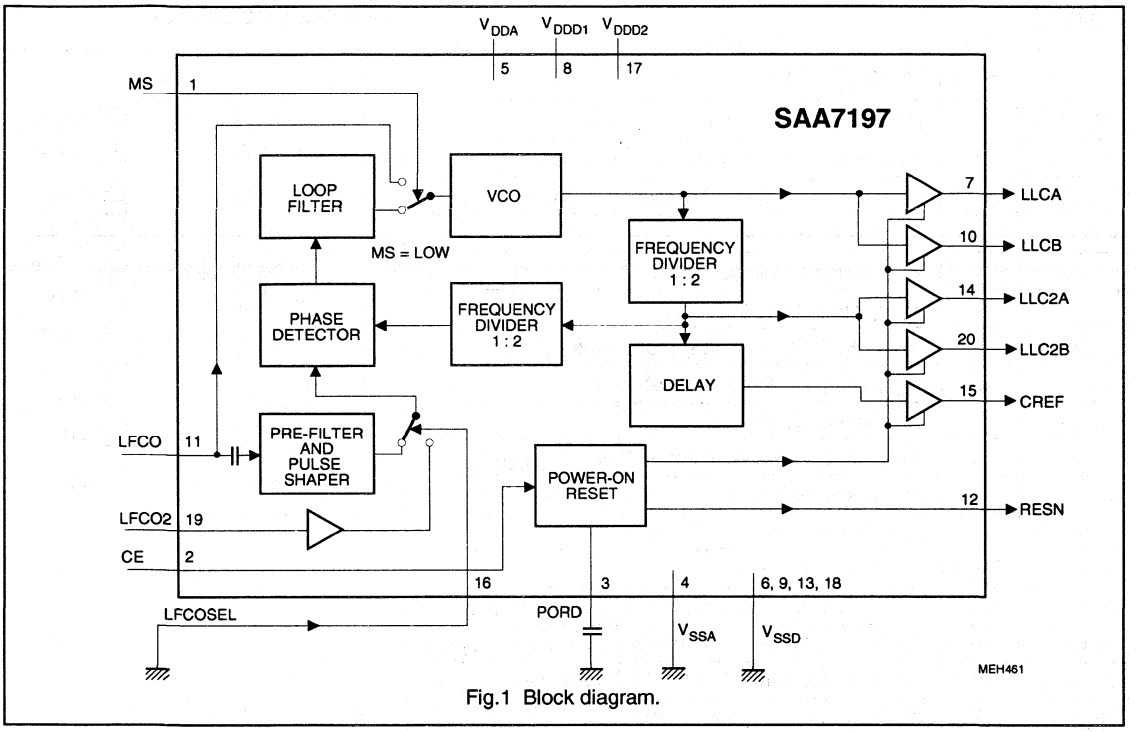


Fig.1 Block diagram.

FUNCTION DESCRIPTION

The SAA7197 generates all clock signals required for a digital TV system suitable for the SAA719x family consisting of an 8-bit analog-to-digital converter (ADC8), digital video multistandard decoder, square pixel (DMSD-SQP), digital video colour space converter (DCSC) and optional extentions. The SAA7197 completes a system for Desktop Video applications in conjunction with memory controllers.

The input signal LFCO is a digital-to-analog converted signal provided by the DMDS-SQPs horizontal PLL. It is the multiple of the line frequency:

7.38 MHz = 472 x f_H in 50 Hz systems
6.14 MHz = 360 x f_H in 60 Hz systems

LFCO2 (TTL-compatible signal from an external reference source) can be applied to pin 19 (LFCOSEL = HIGH).

The input signal LFCO or LFCO2 is multiplied by factors 2 or 4 in the PLL (including phase detector, loop filter, VCO and frequency divider) and output on LLCA (pin7), LLCB (pin 10), LLC2A (pin 14) and LLC2B (pin 20). The rectangular output signals have 50 % duty factor. Outputs with equal frequency may be connected together externally. The clock outputs go HIGH during power-on reset (and chip enable) to ensure that no output clock signals are available the PLL has locked-on.

Mode select MS

The LFCO input signal is directly connected to the VCO at MS = HIGH. The circuit operates as an oscillator and frequency divider. This function is not tested.

Source select LFCOSEL

Line frequency control signal LFCO (pin 11) is selected by LFCOSEL = LOW. LFCOSEL = HIGH selects LFCO2 input signal (pin 19). This function is not tested.

Chip enable CE

The buffer outputs are enabled and RESN set HIGH by CE = HIGH (Fig.4). CE = LOW sets the clock outputs HIGH and RESN output LOW.

CREF output

2 f_{LFCO} output to control the clock dividers of the DMSD-SQP chip family.

Power-on reset

Power-on reset is activated at power-on, when the supply voltage decreases below 3.5 V (Fig.4) or when chip enable is done. The indicator output RESN is LOW for a time determined by capacitor on pin 3. The RESN signal can be applied to reset other circuits of this digital TV system.
The LFCO or LFCO2 input signals have to be applied before RESN becomes HIGH.

Clock Generator Circuit for Desktop Video systems (CGC)

SAA7197

PINNING

SYMBOL	PIN	DESCRIPTION
MS	1	mode select input (LOW = PLL mode)*
CE	2	chip enable /reset (HIGH = outputs enabled)
PORD	3	power-on reset delay, dependent on external capacitor
V_{SSA}	4	analog ground (0 V)
V_{DDA}	5	analog supply voltage (+5 V)
V_{SSD1}	6	digital ground 1 (0 V)
LLCA	7	line-locked clock output signal (4 times f_{LFCO})
V_{DDD1}	8	digital supply voltage 1 (+5 V)
V_{SSD2}	9	digital ground 2 (0 V)
LLCB	10	line-locked clock output signal (4 times f_{LFCO})
LFCO	11	line-locked frequency control input signal 1
RESN	12	reset output (active-LOW, Fig.4)
V_{SSD3}	13	digital ground 3 (0 V)
LLC2A	14	line-locked clock output signal 2A (2 times f_{LFCO})
CREF	15	clock reference output, qualifier signal (2 times f_{LFCO})
LFCOSEL	16	LFCO source select (LOW = LFCO selected)*
V_{DDD2}	17	digital supply voltage 2 (+5 V)
V_{SSD4}	18	digital ground 4 (0 V)
LFCO2	19	line-locked frequency control input signal 2*
LLC2B	20	line-locked clock output signal 2B (2 times f_{LFCO})

PIN CONFIGURATION

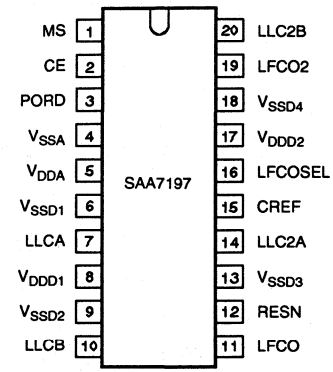


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); ground pins as well as supply pins together connected.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage (pin 5)	–0.5	7.0	V
V_{DDD}	digital supply voltage (pins 8 and 17)	–0.5	7.0	V
$V_{diff\ GND}$	difference voltage $V_{DDA} - V_{DDD}$	-	±100	mV
V_O	output voltage (I_{OM} = 20 mA)	–0.5	V_{DDD}	V
P_{tot}	total power dissipation (DIL20)	0	1.1	W
T_{stg}	storage temperature range	–65	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling** for all pins	-	tbf	V

* MS and LFCO2 functions are not tested. LFCO2 is a multiple of horizontal frequency.

** Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is recommended to take normal handling precautions appropriate to "Handling MOS devices ".

CHARACTERISTICS

$V_{DDA} = V_{DDD} = 4.5$ to 5.5 V; $f_{LFCO} = 5.5$ to 8.0 MHz and $T_{amb} = 0$ to 70 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage (pin 5)		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage (pins 8 and 17)		4.5	5.0	5.5	V
I_{DDA}	analog supply current (pin 5)		3	-	9	mA
I_{DDD}	digital supply current ($I_8 + I_{17}$)	note 1	10	-	60	mA
V_{reset}	power-on reset threshold voltage	Fig.4	-	3.5	-	V
Input LFCO (pin 11)						
V_{11}	DC input voltage		0	-	V_{DDA}	V
V_i	input signal (peak-to-peak value)		1	-	V_{DDA}	V
f_{LFCO}	input frequency range		5.5	-	8.0	MHz
C_{11}	input capacitance		-	-	10	pF
Inputs MS, CE, LFCOSEL and LFCO2 (pins 1, 2, 16 and 19); note 3						
V_{IL}	input voltage LOW		0	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{DDD}	V
f_{LFCO2}	input frequency range for LFCO2		5.5	-	8.0	MHz
I_{LI}	input leakage current	LFCOSEL	50	-	150	µA
		others	-	-	10	µA
C_I	input capacitance		-	-	5	pF
Output RESN (pin 12)						
V_{OL}	output voltage LOW	$I_{OL} = 2$ mA	0	-	0.4	V
V_{OH}	output voltage HIGH	$I_{OH} = -0.5$ mA	2.4	-	V_{DDD}	V
t_d	RESN delay time	$C_3 = 0.1$µF; Fig.4	20	-	200	ms
Output CREF (pin 15)						
V_{OL}	output voltage LOW	$I_{OL} = 2$ mA	0	-	0.6	V
V_{OH}	output voltage HIGH	$I_{OH} = -0.5$ mA	2.4	-	V_{DDD}	V
f_{CREF}	output frequency CREF	Fig.3	-	$2 f_{LFCO(2)}$		MHz
C_L	output load capacitance		15	-	40	pF
t_{SU}	set-up time	Fig.3; note 1	12	-	-	ns
t_{HD}	hold time	Fig.3; note 1	4	-	-	ns
Output signals LLCA, LLCB, LLC2A and LLC2B (pins 7, 10, 14, and 20); note 3						
V_{OL}	output voltage LOW	$I_{OL} = 2$ mA	0	-	0.6	V
V_{OH}	output voltage HIGH	$I_{OH} = -0.5$ mA	2.6	-	V_{DDD}	V
t_{comp}	composite rise time	Fig.3; notes 1 and 2	-	-	8	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{LL}	output frequency LLCA	Fig.3	-	4 $f_{LFCO(2)}$		MHz
	output frequency LLCB		-	4 $f_{LFCO(2)}$		MHz
	output frequency LLC2A		-	2 $f_{LFCO(2)}$		MHz
	output frequency LLC2B		-	2 $f_{LFCO(2)}$		MHz
t_r, t_f	rise and fall times	Fig.3	-	-	5	ns
t_{LL}	duty factor LLCA, LLCB, LLC2A and LLC2B (mean values)	note 1; Fig.3; at 1.5 V level	40	50	60	%

Notes to the characteristics

1. f_{LFCO} = 7.0 MHz and output load 40 pF (Fig.3). V_{SSA} and V_{SSD} short connected together.
2. t_{comp} is the rise time from LOW of all clocks to HIGH of all clocks (Fig.3) including rise time, skew and jitter components. Measurements taken between 0.6 V and 2.6 V. Skew between two LLx clocks will not deviate more than ±2 ns if output loads are matched within 20 %.
3. MS and LFCO2 functions not tested.

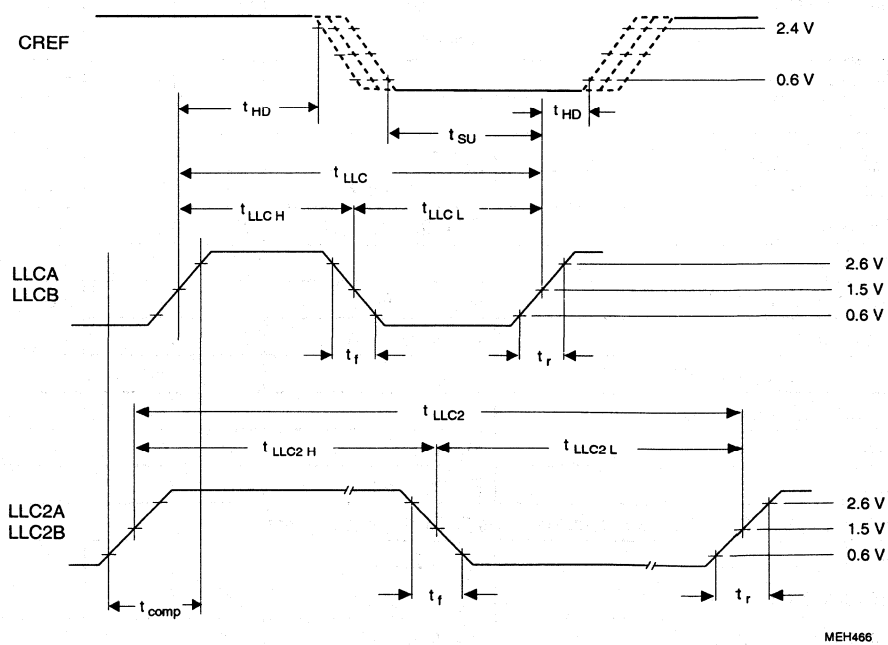


Fig.3 Output timing.

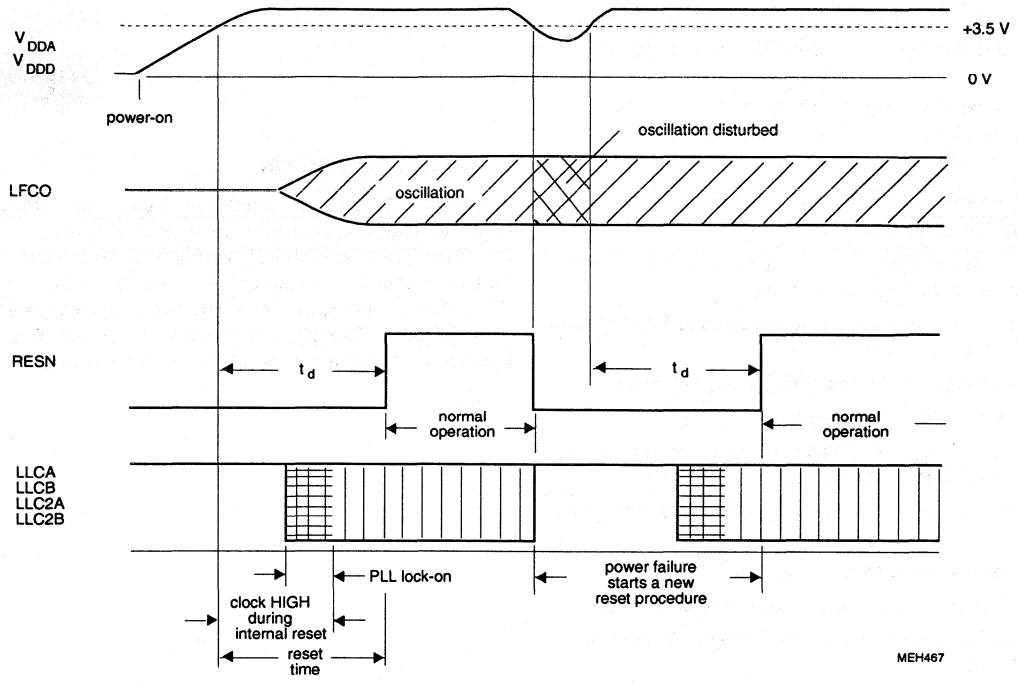


Fig.4 Reset procedure.

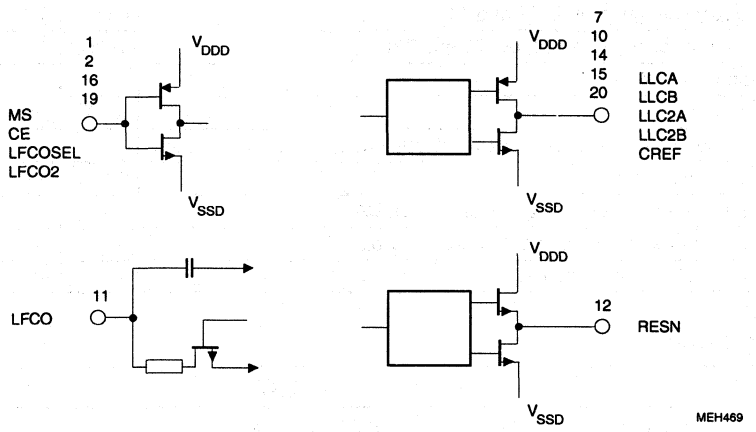


Fig.5 Internal circuit.

Digital Video Encoder (DENC) GENLOCK-capable

SAA7199B

FEATURES

- Monolithic integrated CMOS video encoder circuit
- Standard MPU (12 lines) and I²C-bus interfaces for controls
- Three 8-bit signal inputs PD7 to PD0 for RGB respectively YUV or indexed colour signals (Tables 19 to 26)
- Square pixel and CCIR input data rates
- Band limited composite sync pulses
- Three 256 × 8 colour look-up tables (CLUTs) for example for gamma correction
- External subcarrier from a digital decoder (SAA7151B or SAA7191B)
- Multi-purpose key for real time format switching
- Autonomous internal blanking
- Optional GENLOCK operation with adjustable horizontal sync timing and adjustable subcarrier phase
- Stable GENLOCK operation in VCR standard playback mode
- Optional still video capture extension
- Three suitable video 9-bit digital-to-analog converters
- Composite analog output signals CVBS, Y and C for PAL/NTSC
- Line 21 data insertion possible.

GENERAL DESCRIPTION

The SAA7199B encodes digital baseband colour/video data into analog Y, C and CVBS signals (S-video included). Pixel clock and data are line-locked to the horizontal scanning frequency of the video signal.
The circuit can be used in a square pixel or in a consumer TV application. Flexibility is provided by programming facilities via MPU-bus (parallel) or I²C-bus (serial).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage (pins 2, 21 and 41)	4.5	5.0	5.5	V
V_{DDA}	analog supply voltage (pins 64, 66, 70 and 72)	4.75	5.0	5.25	V
$I_{P(tot)}$	total supply current	–	–	200	mA
V_I	input signal levels	TTL-compatible			
V_o	analog output voltage Y, C and CVBS without load (peak-to-peak value)	–	2	–	V
R_L	output load resistance	90	–	–	Ω
ILE	LF integral linearity error in output signal (9-bit DAC)	–	–	±1	LSB
DLE	LF differential linearity error in output signal (9-bit DAC)	–	–	±0.5	LSB
T_{amb}	operating ambient temperature	0	–	70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7199BWP	PLCC84	plastic leaded chip carrier; 84 leads	SOT189-2

BLOCK DIAGRAM

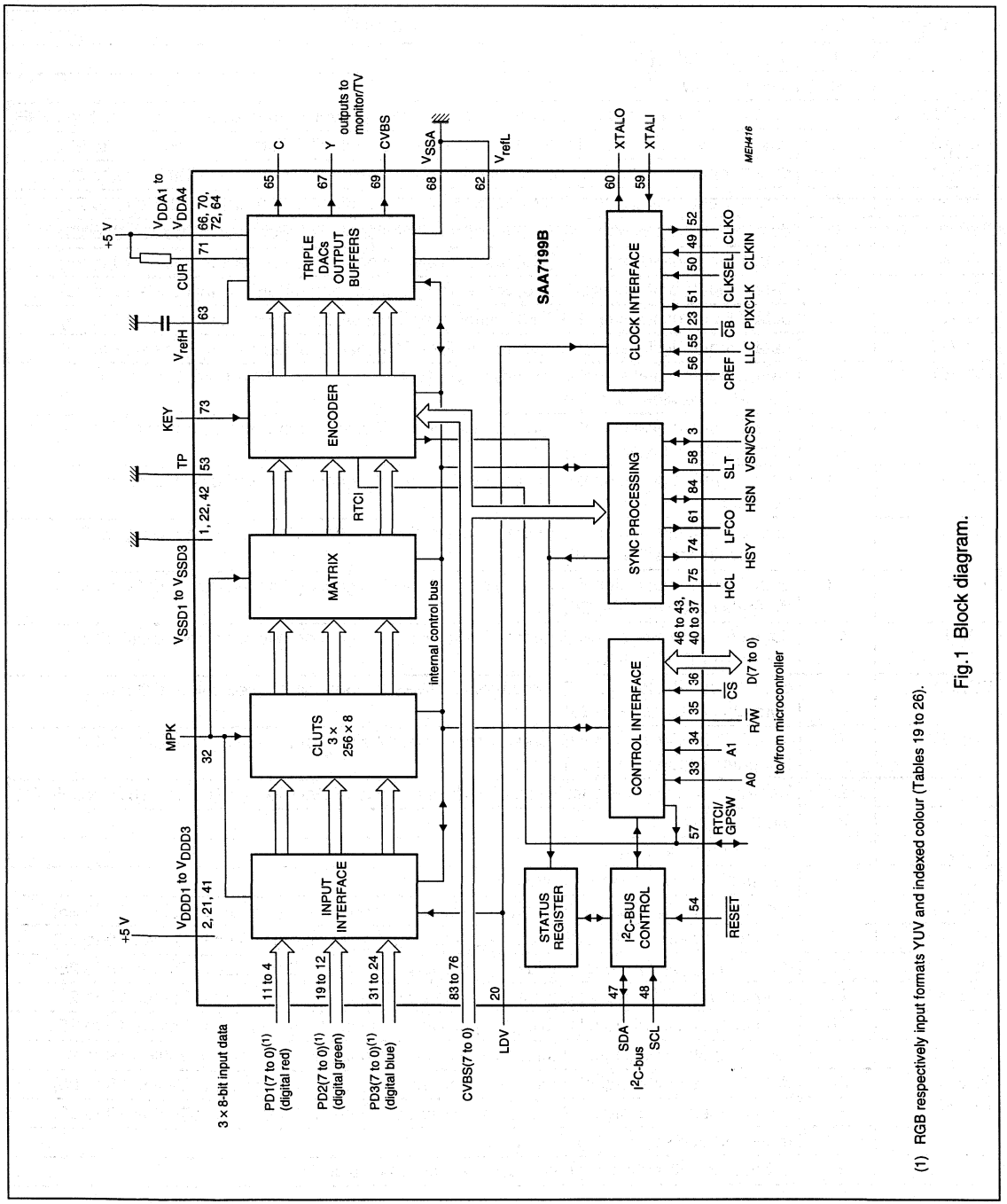


Fig.1 Block diagram.

(1) RGB respectively input formats YUV and indexed colour (Tables 19 to 26).

PINNING

SYMBOL	PIN	DESCRIPTION
V_{SSD1}	1	digital ground 1 (0 V)
V_{DDD1}	2	digital supply 1 (5 V)
VSN/CSYN	3	vertical sync output (3-state), conditionally composite sync output; active LOW or active HIGH
PD1(0)	4	data 1 input: digital signal R (red) respectively V signal; bit 0 (formats in Tables 19 to 25)
PD1(1)	5	data 1 input: digital signal R (red) respectively V signal; bit 1 (formats in Tables 19 to 25)
PD1(2)	6	data 1 input: digital signal R (red) respectively V signal; bit 2 (formats in Tables 19 to 25)
PD1(3)	7	data 1 input: digital signal R (red) respectively V signal; bit 3 (formats in Tables 19 to 25)
PD1(4)	8	data 1 input: digital signal R (red) respectively V signal; bit 4 (formats in Tables 19 to 25)
PD1(5)	9	data 1 input: digital signal R (red) respectively V signal; bit 5 (formats in Tables 19 to 25)
PD1(6)	10	data 1 input: digital signal R (red) respectively V signal; bit 6 (formats in Tables 19 to 25)
PD1(7)	11	data 1 input: digital signal R (red) respectively V signal; bit 7 (formats in Tables 19 to 25)
PD2(0)	12	data 2 input: digital signal G (green) respectively Y signal or indexed colour data; bit 0 (formats in Tables 19 to 25)
PD2(1)	13	data 2 input: digital signal G (green) respectively Y signal or indexed colour data; bit 1 (formats in Tables 19 to 25)
PD2(2)	14	data 2 input: digital signal G (green) respectively Y signal or indexed colour data; bit 2 (formats in Tables 19 to 25)
PD2(3)	15	data 2 input: digital signal G (green) respectively Y signal or indexed colour data; bit 3 (formats in Tables 19 to 25)
PD2(4)	16	data 2 input: digital signal G (green) respectively Y signal or indexed colour data; bit 4 (formats in Tables 19 to 25)
PD2(5)	17	data 2 input: digital signal G (green) respectively Y signal or indexed colour data; bit 5 (formats in Tables 19 to 25)
PD2(6)	18	data 2 input: digital signal G (green) respectively Y signal or indexed colour data; bit 6 (formats in Tables 19 to 25)
PD2(7)	19	data 2 input: digital signal G (green) respectively Y signal or indexed colour data; bit 7 (formats in Tables 19 to 25)
LDV	20	load data clock input signal to input interface (samples PDn(7 to 0), $\overline{CB}$, MPK, KEY and RTCI)
V_{DDD2}	21	digital supply 2 (5 V)
V_{SSD2}	22	digital ground 2 (0 V)
$\overline{CB}$	23	composite blanking input; active LOW
PD3(0)	24	data 3 input: digital signal B (blue) respectively U signal; bit 0 (formats in Tables 19 to 25)
PD3(1)	25	data 3 input: digital signal B (blue) respectively U signal; bit 1 (formats in Tables 19 to 25)
PD3(2)	26	data 3 input: digital signal B (blue) respectively U signal; bit 2 (formats in Tables 19 to 25)
PD3(3)	27	data 3 input: digital signal B (blue) respectively U signal; bit 3 (formats in Tables 19 to 25)
PD3(4)	28	data 3 input: digital signal B (blue) respectively U signal; bit 4 (formats in Tables 19 to 25)
PD3(5)	29	data 3 input: digital signal B (blue) respectively U signal; bit 5 (formats in Tables 19 to 25)
PD3(6)	30	data 3 input: digital signal B (blue) respectively U signal; bit 6 (formats in Tables 19 to 25)
PD3(7)	31	data 3 input: digital signal B (blue) respectively U signal; bit 7 (formats in Tables 19 to 25)
MPK	32	multi-purpose key input; active HIGH
A0	33	subaddress bit A0 input for microcontroller access (Table 3)

SYMBOL	PIN	DESCRIPTION
A1	34	subaddress bit A1 input for microcontroller access (Table 3)
R/$\overline{W}$	35	read/write not input signal from microcontroller
$\overline{CS}$	36	chip select input for parallel interface; active LOW
D0	37	bidirectional port from/to microcontroller; bit D0
D1	38	bidirectional port from/to microcontroller; bit D1
D2	39	bidirectional port from/to microcontroller; bit D2
D3	40	bidirectional port from/to microcontroller; bit D3
V_{DDD3}	41	digital supply 3 (5 V)
V_{SSD3}	42	digital ground 3
D4	43	bidirectional port from/to microcontroller; bit D4
D5	44	bidirectional port from/to microcontroller; bit D5
D6	45	bidirectional port from/to microcontroller; bit D6
D7	46	bidirectional port from/to microcontroller; bit D7
SDA	47	I²C-bus data input/output
SCL	48	I²C-bus clock input
CLKIN	49	external clock signal input (maximum frequency 60 MHz)
CLKSEL	50	clock source select input
PIXCLK	51	CLKO/2 or conditionally CLKO output signal
CLKO	52	selected clock output signal (LLC or CLKIN)
TP	53	test pin; connected to ground
$\overline{RESET}$	54	reset input; active LOW
LLC	55	line-locked clock input signal from external clock generation circuit (CGC)
CREF	56	clock qualifier input of external CGC
GPSW/RTCI	57	general purpose switch output (set via I²C-bus or MPU-bus); real time control input, defined by I²C or MPU programming
SLT	58	GENLOCK output flag (3-state): HIGH = sync lost in GENLOCK mode; LOW = otherwise
XTALI	59	crystal oscillator input (26.8 or 24.576 MHz)
XTALO	60	crystal oscillator output
LFCO	61	line frequency control output signal for external CGC
V_{refL}	62	reference voltage LOW of DACs (resistor chains)
V_{refH}	63	reference voltage HIGH of DACs (resistor chains)
V_{DDA4}	64	analog supply 4 for resistor chains of the DACs (5 V)
C	65	chrominance analog output signal
V_{DDA1}	66	analog supply 1 for output buffer amplifier of DAC1 (5 V)
Y	67	luminance analog output signal
V_{SSA}	68	analog ground (0 V)
CVBS	69	CVBS analog output signal
V_{DDA2}	70	analog supply 2 for output buffer amplifier of DAC2 (5 V)
CUR	71	current input for analog output buffers
V_{DDA3}	72	analog supply 3 for output buffer amplifier of DAC3 (5 V)
KEY	73	key input signal to insert CVBS input signal into encoded CVBS output signal; active HIGH

SYMBOL	PIN	DESCRIPTION
HSY	74	horizontal sync indicator output signal; active HIGH (3-state output to ADC)
HCL	75	horizontal clamping output; active HIGH (3-state output)
CVBS0	76	digital CVBS input signal; bit 0
CVBS1	77	digital CVBS input signal; bit 1
CVBS2	78	digital CVBS input signal; bit 2
CVBS3	79	digital CVBS input signal; bit 3
CVBS4	80	digital CVBS input signal; bit 4
CVBS5	81	digital CVBS input signal; bit 5
CVBS6	82	digital CVBS input signal; bit 6
CVBS7	83	digital CVBS input signal; bit 7
HSN	84	horizontal sync output; active LOW or active HIGH for 60/66/72 × PIXCLK at 12.27/13.5/14.75 MHz (3-state output)

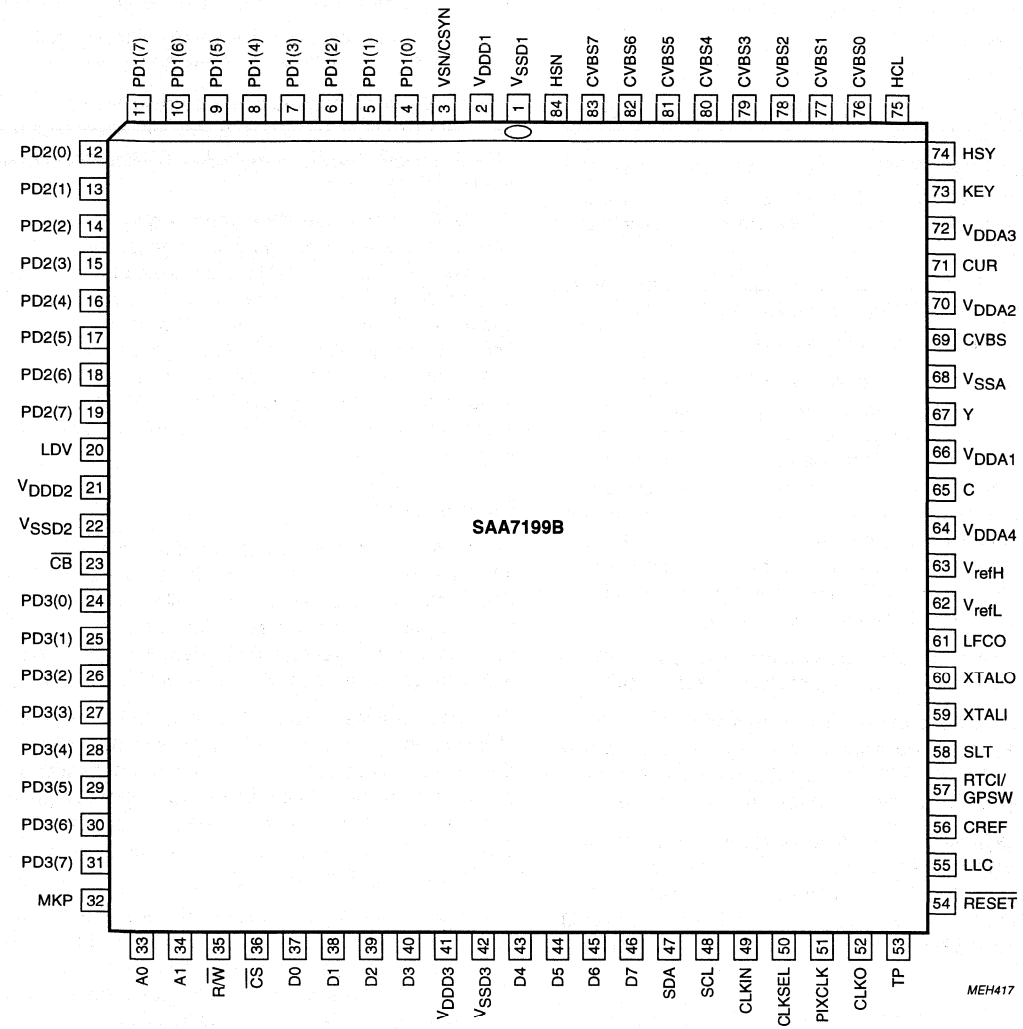


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The SAA7199B is a digital video encoder that translates digital RGB, YUV or 8-bit indexed colour signals into the analog PAL/NTSC output signals Y (luminance), C (4.43/3.58 MHz chrominance) and CVBS (composite signal including sync).

Four different modes are selectable (Table 18):

Stand-alone mode (horizontal and vertical timings are generated)

Slave mode (stand-alone unit that accepts external horizontal and vertical timing), and optional real time information for subcarrier/clock from a digital colour decoder

GENLOCK mode (GENLOCK capabilities are achieved in conjunction with determined ICs)

Test mode (only clock signal is required).

The input data rate (pixel sequence) has an integer relationship to the number of horizontal clock cycles (Table 1). A sufficient stable external clock signal ensures correct encoding. The generated clock frequency in the GENLOCK mode may deviate by ±7% depending on the reference signal which is corresponding to its input sync signal. The clock will be nominal in the GENLOCK mode when the reference signal is absent (nominal with crystal oscillator accuracy for TV time constants, and nominal ±1.4% for VCR time constants).

The on-chip colour conversion matrix provides *"CCIR 601"* code-compatible transcoding of RGB to YUV data.

RGB data out of bounds, with respect to *"CCIR 601"* specification, can be clipped to prevent over-loading of the colour modulator. RGB data input can be either in linear colour space or in gamma-corrected colour space.

YUV data must be gamma-corrected in accordance with *"CCIR 601"*. This circuit operates primarily in a 24-bit colour space (3 × 8-bit) but can also accommodate different data formats (4 : 1 : 1, 4 : 2 : 2 and 4 : 4 : 4) plus 8-bit indexed pseudo-colour space operations (FMT-bits in Table 8).

RGB CLUTs on-chip provide gamma-correction and/or other CLUT functions. They consist of programmable tables to be loaded independently, and they generate 24-bit gamma-corrected output signals from 24-bit data of one of the input formats or from 8-bit indexed pseudo-colour data.

Required modulation is performed. The digital YUV data is encoded in accordance with standards *"RS-170A"* (composite NTSC) and *"CCIR 624-4"* (composite PAL-B/G). S-video output signal is available (Y/C) also some sub-standard output signals (STD-bits in Table 12).

A 7.5 IRE set-up level is automatically selected in the 60 Hz mode, but not selected in the 50 Hz mode.

The analog signal outputs can drive directly into terminated 75 Ω coaxial lines, a passive external filter is recommended (Figs 3, 13 and 14). Analog post-filtering is required (LP in Fig.3).

GENLOCK to an external reference signal is achieved by addition of a video ADC and a clock generator combination. Thus, the system is enabled to lock on a stable video source or to a stable VCR source (normal playback). The SAA7199B, the ADC and the clock generator combination (Fig.3) form a control loop achieving a highly stable line-locked clock. The clock has to be generated by a crystal oscillator without this availability. The GENLOCK mode is not available in a single device set-up.

Control interface

The SAA7199B supports a standard parallel MPU interface and the serial I²C-bus interface. The MPU has direct access to internal control registers and colour tables. Update is possible at any time, excluding coincident internal reading and external writing of the same cell (the current pixel value could be destroyed).

The two interfaces of Table 2 are selected automatically. However, the I²C-bus control is inactive when the MPU interface is selected by $\overline{CS}$ = LOW. No simultaneous access may occur. I²C-bus and MPU control complement each other and have access to common registers controlled via a common internal bus. The programmer can use virtually identical programs.

The internal memory space is devided into the look-up table and the control table, each with its own 8-bit address register used as a pointer for specific location.
This address register is provided with auto-incrementation and can be written by only one addressing.

The look-up table contains three banks of 256 bytes. Therefore, each read or write cycle must access all three banks in a pre-determined order. The support logic is part of the control interface.

Timing (see Fig.3)

The reference to generate internal clocks from LLC in GENLOCK operation with SAA7197 is CREF

$$CREF = \frac{LLC}{2}.$$

In this event input CLKSEL is HIGH and the SRC-bit = 1.

In non-GENLOCK operation the signal from CLKIN is used and LDV is clock reference (input CLKSEL = 0; SCR-bit = CPR-bit = 0).

Pins LLC and CLKIN are tied together when no switching between LLC and CLKIN is applied. In Fig.3 it is assumed that LLC and CLKIN are double the pixel clock frequency of CREF and LDV respectively.

CREF must be at the same frequency (or constant HIGH or LOW) when LLC is at pixel clock frequency. CPR-bit = 1 if CLKIN is at pixel clock frequency.

The buffered CLKO signal is always delayed. LLC or CLKIN signals are in accordance with CLKSEL.

Mapping

The method of mapping external control signals on to the internal bus is simple. The MPU-bus contains the signals as shown in Table 4 (names in chip-internal nomenclature).

Bit allocation

The Bit Allocation Map (BAM) shows the individual control signals, used to control the different operational modes of the circuit. The I²C-bus is normally used for control. The SAA7199B also has an MPU-bus interface for direct microcontroller connection. The BAM shown in Table 6 resembles the I²C-bus type but can be also used for the parallel bus; the control registers are indexed from 00H to 0FH. Auto-incrementation is applied.

Digital-to-analog converters

The converters use a combination of resistor chains with low-impedance output buffers. The bottom output voltage is 200 mV to reduce integral non-linearity errors. The analog signal, without load on output pin, is between 0.2 and 2.2 V. Figure 16 shows the application for 1.23 V/75 Ω outputs, using the serial 25 + 22 Ω resistors.

Each digital-to-analog converter has its own supply pin for the purpose of decoupling. V_{DDA4} is the supply voltage for the resistor chains of the three DACs. The accuracy of this supply voltage directly influences the output amplitudes. The current CUR into pin 71 is 0.3 mA (V_{DDA4} = 5 V; $R_{64\text{-}71}$ = 20 kΩ); a larger current improves the bandwidth but increases the integral non-linearity.

Table 1 Pixel relationships

ACTIVE PIXELS PER LINE	FIELD RATE (Hz)	MULTIPLES OF LINE FREQUENCY	PIXCLK OUTPUT SIGNAL (MHz)	CRYSTAL (MHz)
640 (square)	60	780	12.27	26.8
720	60	858	13.5	24.576
768	50	944	14.75	26.8
720	50	864	13.5	24.576

Table 2 Access to the control interface

SYMBOL	DESCRIPTION
SDA	I²C-bus serial data line (bidirectional)
SCL	I²C-bus clock line
A1, A0	MPU-bus address inputs
R/$\overline{W}$	read/write control input
$\overline{CS}$	chip select input; I²C-bus disabled when LOW
GPSW	general purpose switch output (bit of control register)
$\overline{RESET}$	reset input signal; active-LOW

Table 3 Address assignment

ADDRESS INPUTS		I²C-BUS SUBADDRESS	SELECTION
A1	A0		
0	0	00	ADR-CLUT (address register of look-up tables)
0	1	01	DATA-CLUT
1	0	02	ADR-CTRL (index register of control table)
1	1	03	DATA-CTRL

Table 4 Signals on the internal bus

SYMBOL	DESCRIPTION
R/$\overline{W}$	select read/write (read = 1; write = 0)
C/$\overline{T}$	control table/look-up table (control table = 1; look-up table = 0)
D/$\overline{A}$	select data/address (data = 1; address = 0)
DI/DO (0 to 7)	data bus on port inputs/outputs D7 to D0
EN	enable from control interface to synchronize data transfer

Table 5 Signals on the internal bus

INTERNAL PARALLEL BUS	PARALLEL INTERFACE	I²C-BUS INTERFACE
R/$\overline{W}$	R/$\overline{W}$ (pin 35)	LSB of slave address byte (read = HIGH; write = LOW)
C/$\overline{T}$	A1 (pin 34)	X 4 subaddresses after decoding
A/$\overline{T}$	A0 (pin 33)	X 4 subaddresses after decoding
DI/DO (0 to 7)	D7 to D0	data bits D7 to D0 for each subaddress
EN	$\overline{CS}$ and R/$\overline{W}$	enable by every 9th clock of sample of SCL (control of serial-to-parallel conversion)

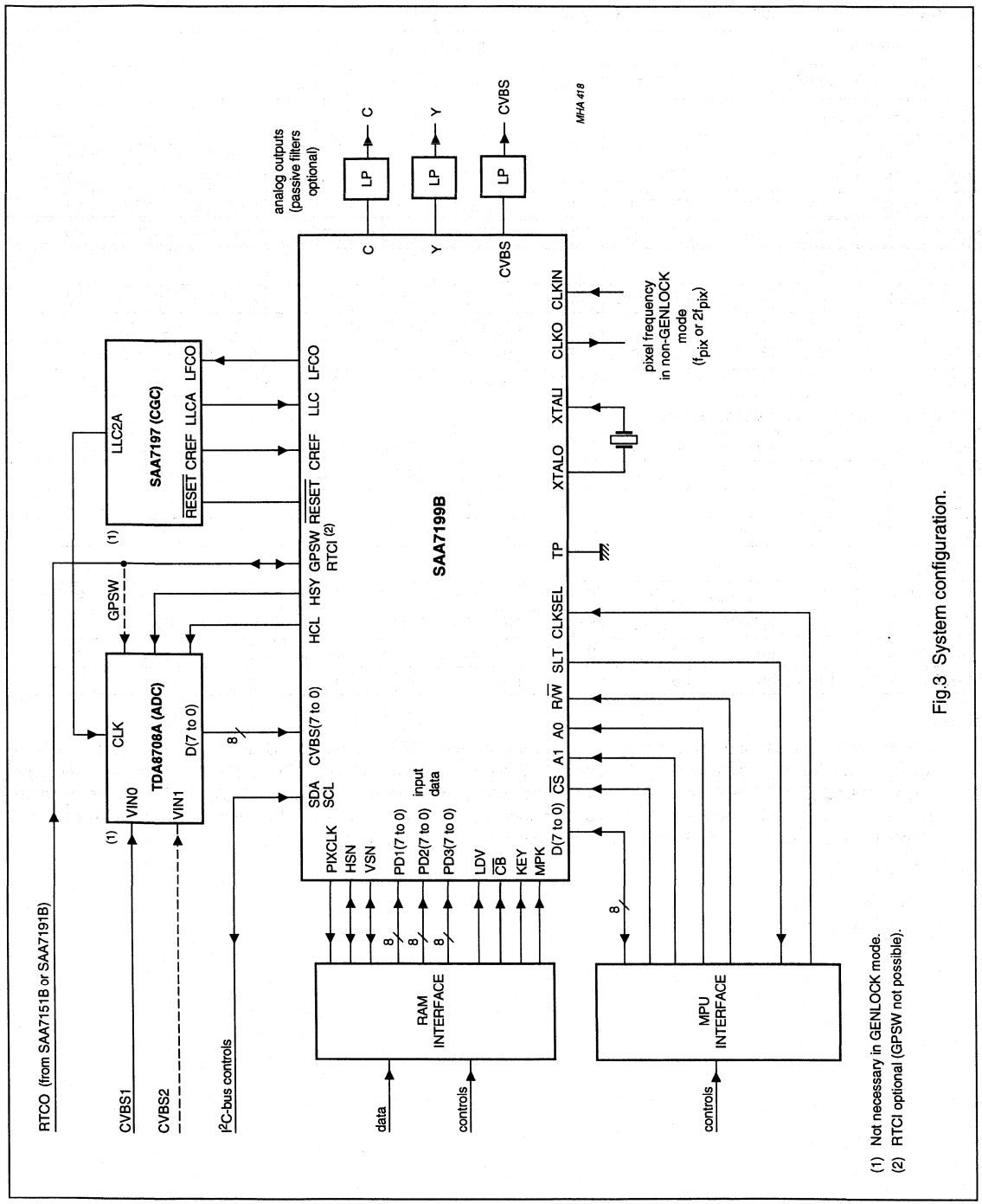


Fig.3 System configuration.

(1) Not necessary in GENLOCK mode.
(2) RTCI optional (GPSW not possible).

Table 6 Bit allocation map (I^2C-bus access in Table 17)

INDEX		DATA BYTE								DF[1]
BINARY	HEX	D7	D6	D5	D4	D3	D2	D1	D0	
Input processing										
0000 0000	00	VTBY	FMT2	FMT1	FMT0	SCBW	CCIR	MOD1	MOD0	5C
0000 0001	01	TRER7	TRER6	TRER5	TRER4	TRER3	TRER2	TRER1	TRER0	XX
0000 0010	02	TREG7	TREG6	TREG5	TREG4	TREG3	TREG2	TREG1	TREG0	XX
0000 0011	03	TREB7	TREB6	TREB5	TREB4	TREB3	TREB2	TREB1	TREB0	XX
Sync processing										
0000 0100	04	SYSEL1	SYSEL0	SCEN	VTRC	NINT	HPLL	HLCK[2]	OEF[2]	10
0000 0101	05	0	0	GDC5	GDC4	GDC3	GDC2	GDC1	GDC0	21
0000 0110	06	IDEL7	IDEL6	IDEL5	IDEL4	IDEL3	IDEL2	IDEL1	IDEL0	52
0000 0111	07	0	0	PSO5	PSO4	PSO3	PSO2	PSO1	PSO0	32
Control, clock and output formatter										
0000 1000	08	DD	KEYE	SRC	CPR	COKI	IM	GPSW	SRSN	64
0000 1001	09	0	BAME	MPKC1	MPKC0	IEPI	RTSC	RTIN	RTCE	02
0000 1010[3]	0A[3]	0	0	0	0	0	0	0	0	00
0000 1011[3]	0B[3]	0	0	0	0	0	0	0	0	00
Encoder control										
0000 1100	0C	CHPS7	CHPS6	CHPS5	CHPS4	CHPS3	CHPS2	CHPS1	CHPS0	XX[4]
0000 1101	0D	FSCO7	FSCO6	FSCO5	FSCO4	FSCO3	FSCO2	FSCO1	FSCO0	00
0000 1110	0E	0	0	0	CLCK[2]	STD3	STD2	STD1	STD0	0C
0000 1111[3]	0F[3]	0	0	0	0	0	0	0	0	

Notes

1. DF is the default value for a typical programming example: GENLOCK mode for a VCR; non-gamma-corrected RGB data (real time keying is possible). SLT will be set if there is no horizontal lock.NTSC-M standard with normal colour bandwidth and 12.2727 MHz pixel rate. CSYN signal will be provided, arriving 8 pixel clocks earlier, to compensate pipeline delay in the previous RAM interface. The encoded CVBS is 12 clocks earlier than the CVBS reference on the input of the previous ADC. The CLUTs are bypassed at MPK = HIGH in real time.
2. Read only bits.
3. Reserved.
4. Adjust as required.

Table 7 Function of registers bits of Table 6

BIT	FUNCTION
Index 00 VTBY	video look-up table by-pass: 0 = not bypassed; 1 = bypassed (logically OR-ed with MPK)
FMT2 to FMT0	input formats see Table 8
SCBW	chrominance bandwidth: 0 = enhanced; 1 = standard
CCIR	select level: 0 = DMSD2 levels; 1 = CCIR levels
MOD1 to MOD0	select mode see Table 9
Index 01 TRER7 to TRER0	test register red (read/write via MPU-bus; write only via I^2C-bus)
Index 02 TREG7 to TREG0	test register green (read/write via MPU-bus; write only via I^2C-bus)
Index 03 TREB7 to TREB0	test register blue (read/write via MPU-bus; write only via I^2C-bus)
Index 04 SYSEL1 to SYSEL0	sync select see Table 10
SCEN	sync/clamping (HSY/HCL) enable: 0 = disabled (set to HIGH); 1 = enabled
VTRC	select TV/VTR mode: 0 = TV mode (slow); 1 = VTR mode (fast)
NINT	select interlace of encoded signal: 0 = interlaced (262.5/262.5 or 312.5/312.5); 1 = non-interlaced (262/262 or 312/312 in modes 1 and 3 only)
HPLL	select horizontal lock: 0 = lock enabled; 1 = lock disabled (crystal reference)
OEF	status bit field organization (to be read): 0 = even field; 1 = odd field
HLCK	status bit sync indication (to be read): 0 = locked to external sync; 1 = external sync lost
Index 05 GDC5 to GDC0	GENLOCK delay compensation; note 1: data 00 to 3F equals timing of CVBS output signal which is (46 – GDC) pixel clocks = t_{ofs} earlier with respect to reference point t_{REF1}. (t_{REF1} corresponds to the falling edge of the horizontal sync pulse of CVBS input signal; t_{ofs} is designated for propagation delay of external GENLOCK source, Fig.10).
Index 06 IDEL7 to IDEL0	increment delay: update of line-locked clock frequency (Table 6, data '43' hex recommended)
Index 07 PSO7 to PSO0	Phase sync in output signal, note 1: data 00 to 3F equals to active slope of HSN, VSN/CSYN is (58 – PSO) pixel clocks = t_{Rint} earlier with respect to reference point t_{REF2} (t_{REF2} corresponds to PSO = 58; t_{Rint} is designated for pipeline delay of the feeding RAM interface, Fig.10).
Index 08 DD	digital video encoder disable: 0 = enabled; 1 = disabled
KEYE	keying enable: 0 = disabled; 1 = enabled (logically AND-connected with KEY)
SRCC	clock source: 0 = external system clock; 1 = DTV2 system clock
CPR	clock phase reference: 0 = LDV is input (pin 20); 1 = LDV is not
COKI	colour-killer: 0 = colour on; 1 = colour off (subcarrier is switched off)
IM	interrupt mask: 1 = interrupt not masked at sync lost (pin 58) 0 = interrupt masked at sync lost (pin 58)
GPSW	general purpose switch at bit RTIN = 1: 0 = pin 57 LOW; 1 = pin 57 HIGH
SRSN	software reset: 0 = no reset; 1 = reset (see "Reset" procedure)
Index 09 BAME	Burst amplitude indication: 0 = burst amplitude measurement is overridden; colour lock always assumed; 1 = burst amplitude is used to control the CLCK status bit, recommended for reference signal without subcarrier burst (pure black and white) in order to avoid PLL hunting.
MPKC1 to MPKC0	multipurpose key control: with MKP = LOW (pin 32) all functions are as given by software programming; MKP = HIGH sets in real time with respect to PDn (7 to 0); functions see Table 11

BIT	FUNCTION
IEPI	polarity of external PAL-ID signal (H/2 signal) from RTCI input (pin 57): 0 = not inverted; 1 = inverted
RTSC	Real time select control: 0 = real time control HPLL increment is selected, which means, information concerning actual clock frequency from the digital colour decoder is received (SAA7151B or SAA7191B); the corresponding subcarrier frequency is calculated; 1 = real time control FSC increment with PAL-ID is selected, which means, information concerning actual subcarrier frequency and PAL-ID from the digital colour decoder is received (SAA7151B or SAA7191B).
RTIN	select real time control input: 0 = pin 57 is input for RTCI signal; 1 = pin 57 is port output GPSW
RTCE	real time control enabled: 0 = disabled; 1 = enabled (RTIN = 0)
Index 0C CHPS7 to CHPS0	phase adjustment between chrominance output signal and reference: 00 to FF equals 0 to 358.59375 degrees in steps of 1.40625 degrees
Index 0D FSC7 to FSC0	fine adjustment of subcarrier frequency in non-GENLOCK modes: 00 to 7F increasing and FF to 80 decreasing equal approximately to 450×10^{-6} of the subcarrier frequency in 256 steps
Index 0E CLCK	lock to external chrominance (to be read): 0 = possible; 1 = not possible
STD3 to STD0	colour encoding standards; see Table 12
–	status bits to be read via I^2C-bus: see Table 15
–	status bits to be read by microcontroller: all registers from 00 up to 0F can be read via MPU-bus, read only bits are OEF, HCLK (index 04) and CLCK (index 0E)

Note

1. Field blanking (Figs 11 and 12): normally, video to be encoded should not become active after the active edge of VSN or CSYN before line 22.5 at 50 Hz (line 18 at 60 Hz). Total internal field blanking is 11 lines at 50 Hz (13 lines at 60 Hz).

Table 8 Input formats

FMT2	FMT1	FMT0	FORMAT
0	0	0	YUV 4 : 1 : 1 format; DMSD2 compatible
0	0	1	YUV 4 : 1 : 1 format; customized
0	1	0	YUV 4 : 2 : 2 format; DMSD2 compatible
0	1	1	YUV 4 : 2 : 2 format; customized
1	0	0	YUV 4 : 4 : 4 format
1	0	1	RGB 4 : 4 : 4 format
1	1	0	reserved
1	1	1	8-bit indexed colour

Table 9 Select mode

MOD1	MOD0	MODE
0	0	GENLOCK mode
0	1	stand alone mode
1	0	slave mode
1	1	test mode

Table 10 Sync select

SYSEL1	SYSEL0	SYNCHRONIZED FROM
0	0	CSYN (active LOW; pin 3)
0	1	HSN and VSN (active LOW; pins 84 and 3)
1	0	CSYN (active HIGH; pin 3)
1	1	HSN and VSN (active HIGH; pins 84 and 3)

Table 11 Multi-purpose key control

SET BY BITS		IN FUNCTION BLOCKS INPUT FORMATTER	CLUTs	MATRIX	LEVEL MATCHING
MPKC1	MPKC0				
0	0	control via CCIR bit and FMT bits	bypass	control via FMT bits	control via CCIR bit
0	1	format 5 (RGB) CCIR level	active, no indexed colour	active	CCIR level
1	X	format 7 (indexed colour) CCIR level	active, no indexed colour	active	CCIR level

Table 12 Colour encoding standards

STD3	STD2	STD1	STD0	STANDARD
0	0	0	0	NTSC 4.43; 60 Hz; SQP (12.27 MHz)
0	0	0	1	NTSC 4.43; 50 Hz; SQP (14.75 MHz)
0	0	1	0	PAL-B/G 4.43; 50 Hz; SQP (14.75 MHz)
0	0	1	1	NTSC 4.43; 60 Hz; CCIR (13.5 MHz)
0	1	0	0	NTSC 4.43; 50 Hz; CCIR (13.5 MHz)
0	1	0	1	PAL-B/G 4.43; 50 Hz; CCIR (13.5 MHz)
0	1	1	0	reserved
0	1	1	1	reserved
1	0	0	0	PAL-M; 60 Hz; SQP (12.27 MHz)
1	0	0	1	PAL-M; 60 Hz; CCIR (13.5 MHz)
1	0	1	0	PAL-N; 50 Hz; CCIR (13.5 MHz)
1	0	1	1	PAL-N; 50 Hz; SQP (14.75 MHz)
1	1	0	0	NTSC-M; 60 Hz; SQP (12.27 MHz)
1	1	0	1	NTSC-M; 60 Hz; CCIR (13.5 MHz)
1	1	1	0	reserved
1	1	1	1	reserved

Colour look-up tables (CLUTs)

The CLUTs consist of RAM tables. The RAM tables can be loaded with X = 0 to 255 in accordance with equation 1 for the signals R, G and B. Gamma-correction (pre-distortion) by the following equation:

$Y = \text{NINT}\,(b + a \times X1^{1/g})$; $Y(X \leq 16) = 16$; $Y(X \geq 235) = 235$ (equation 1) with $g = 2.2$: $a = \dfrac{219}{235^{-2.2} - 16^{-2.2}}$;
$b = 16 - a \times 16^{-2.2}$

The RAM tables are loaded via MPU-bus or via I²C-bus (Table 17).

I²C-bus format

Table 13 I²C-bus address; see Table 14

S	SLAVE ADDRESS	ACK	SUBADDRESS	ACK	DATA 0	ACK	--------	DATA n	ACK	P

Table 14 Explanation of Table 13

PART	DESCRIPTION
S	START condition
Slave address	1 0 1 1 0 0 0 X (note 1)
ACK	acknowledge, generated by the slave
Subaddress (note 2)	subaddress byte (Table 17)
DATA	data byte (Table 6)
--------	continued data bytes and ACKs
P	STOP condition

Notes

1. X is the read/write control bit; X = 0 is order to write (the circuit is slave receiver); X = 1 is order to read (the circuit is slave transmitter).
2. If more than 1 byte DATA is transmitted, then auto-increment of the subaddress is performed.

Table 15 I²C-bus status byte (address byte B1)

FUNCTION	STATUS BYTE							
	D7	D6	D5	D4	D3	D2	D1	D0
Read status	0	0	0	0	FFOS	OEF	CLCK	HLCK

Table 16 Function of the bits in Table 15

BIT	FUNCTION
FFOS	first field of sequence: 0 = false; 1 = first of 4 fields for NTSC (first of 8 fields for PAL). FFOS is not valid for non-interlaced signals.
OEF	field organization: 0 = even field; 1 = odd field
CLCK	lock to external chrominance: 0 = possible; 1 = not possible
HLCK	sync indication: 0 = locked to external sync; 1 = external sync lost

Table 17 I²C-bus write bytes (address byte B0)

ACCESS	DESCRIPTION OF BYTE			
Control registers	address byte B0	subaddress byte 02	index byte (00 to 0F); Table 6	data bytes (auto-increment)
CLUTs registers	address byte B0	subaddress byte 00	CLUT address bytes (00 to FF)	3 data bytes for one RGB sequence (auto-increment)

Modes of the SAA7199B

Table 18 The four different modes of the SAA7199B

MODE	DESCRIPTION
Stand alone	The SAA7199B receives a line-locked clock CLKIN and generates CSYN or HSN/VSN output signals, which trigger the RGB or the YUV source signal to provide data and composite blanking $\overline{CB}$.
Slave	The SAA7199B receives the line-locked clock CLKIN, CSYN or HSN/VSN, $\overline{CB}$ and data from an RGB or YUV source. The sync inputs are edge-sensitive; their minimum active length is 1 PIXCLK. A real time control signal RTCI is received from a digital colour decoder as an option.
GENLOCK	Horizontal and vertical sync plus colour are locked on a received CVBS reference signal. The CVBS reference signal also generates a line-locked clock by the SAA7197 clock generator. Auxiliary signals HCL and HSY plus CSYN or HSN/VSN are generated to trigger the RGB or the YUV source providing data and composite blanking $\overline{CB}$.
Test	Similar to stand alone mode, but the contents of the test registers TRER, TREG and TREB consists of data to be encoded. VSN/CSYN and HSN outputs are in 3-state condition.

RELATIONSHIP BETWEEN HORIZONTAL FREQUENCY AND COLOUR SUBCARRIER FREQUENCY IN NON-GENLOCK MODE

1. Internal subcarrier frequency with n = integer

   PAL: $f_{SC} = f_H (n/4 + 1/625)$ respectively $f_H (n/4 + 1/525)$

   NTSC: $f_{SC} = f_H (n/2)$

   Necessary conditions: non-GENLOCK mode; RTCE = 0, FSCO = 00H; phase coupling of the two frequencies is given by a definite phase reset every 8th field at PAL (4th field at NTSC).

   FSCO ≠ 00H adjusts the subcarrier frequency, phase reset is disabled and phase between f_{SC} and f_H is not constant.

2. External subcarrier frequency

   f_{SC} is given by RTCI real time input from a digital colour decoder

   Necessary conditions: Slave mode; RTCE = 1, RTSC = 1. The 8th respectively 4th field reset is enabled at FSCO = 00H (disabled at FSCO ≠ 00H). The subcarrier frequency is not influenced by FSCO bits, but is given by real time increment.

3. External HPLL increment

   f_{SC} is calculated by RTCI real time input signal from a digital colour decoder. The frequency of f_{SC} depends on the absolute crystal frequency value used by the digital colour decoder.

   Necessary conditions: Slave mode; RTCE = 1, RTSC = 0. The 8th respectively 4th field reset is enabled at FSCO = 00H (disabled at FSCO ≠ 00H). The subcarrier frequency is influenced by FSCO bits.

The absolute phase relationship between sync and subcarrier (colour burst output) can be influenced in all three events by CHPS7 to CHPS0 register byte (index 0C).

Data input formats

One clock cycle equals 12.27 MHz, 13.5 MHz or 14.75 MHz; Cb = (B – Y) equals U; Cr = (R – Y) equals V; (n) = number of pixels.

Table 19 Format 0; DMSD2 compatible YUV 4 : 1 : 1 format (FMT-bits in index 00 = 000)

INPUT SIGNAL	CLOCK CYCLE (PIXEL SEQUENCE)							
	0	1	2	3	4	5	6	7
PD2(7 to 0)	Y(0)	Y(1)	Y(2)	Y(3)	Y(4)	Y(5)	Y(6)	Y(7)
PD3(7)	Cb7(0)	Cb5(0)	Cb3(0)	Cb1(0)	Cb7(4)	Cb5(4)	Cb3(4)	Cb1(4)
PD3(6)	Cb6(0)	Cb4(0)	Cb2(0)	Cb0(0)	Cb6(4)	Cb4(4)	Cb2(4)	Cb0(4)
PD3(5)	Cr7(0)	Cr5(0)	Cr3(0)	Cr1(0)	Cr7(4)	Cr5(4)	Cr3(4)	Cr1(4)
PD3(4)	Cr6(0)	Cr4(0)	Cr2(0)	Cr0(0)	Cr6(4)	Cr4(4)	Cr2(4)	Cr0(4)
PD3(3 to 0)	not used							
PD1(7 to 0)	not used							

Table 20 Format 1; customized YUV 4 : 1 : 1 format (FMT-bits in index 00 = 001)

INPUT SIGNAL	CLOCK CYCLE (PIXEL SEQUENCE)							
	0	1	2	3	4	5	6	7
PD2(7 to 0)	Y(0)	Y(1)	Y(2)	Y(3)	Y(4)	Y(5)	Y(6)	Y(7)
PD3(7)	Cb7(0)	–	Cr7(0)	–	Cb7(4)	–	Cr7(4)	–
PD3(6)	Cb6(0)	–	Cr6(0)	–	Cb6(4)	–	Cr6(4)	–
PD3(5)	Cb5(0)	–	Cr5(0)	–	Cb5(4)	–	Cr5(4)	–
PD3(4)	Cb4(0)	–	Cr4(0)	–	Cb4(4)	–	Cr4(4)	–
PD3(3)	Cb3(0)	–	Cr3(0)	–	Cb3(4)	–	Cr3(4)	–
PD3(2)	Cb2(0)	–	Cr2(0)	–	Cb2(4)	–	Cr2(4)	–
PD3(1)	Cb1(0)	–	Cr1(0)	–	Cb1(4)	–	Cr1(4)	–
PD3(0)	Cb0(0)	–	Cr0(0)	–	Cb0(4)	–	Cr0(4)	–
PD1(7 to 0)	not used							

Table 21 Format 2; DMSD2 compatible YUV 4 : 2 : 2 format (FMT-bits in index 00 = 010)

INPUT SIGNAL	CLOCK CYCLE (PIXEL SEQUENCE)							
	0	1	2	3	4	5	6	7
PD2(7 to 0)	Y(0)	Y(1)	Y(2)	Y(3)	Y(4)	Y(5)	Y(6)	Y(7)
PD3(7)	Cb7(0)	Cr7(0)	Cb7(2)	Cr7(2)	Cb7(4)	Cr7(4)	Cb7(6)	Cr7(6)
PD3(6)	Cb6(0)	Cr6(0)	Cb6(2)	Cr6(2)	Cb6(4)	Cr6(4)	Cb6(6)	Cr6(6)
PD3(5)	Cb5(0)	Cr5(0)	Cb5(2)	Cr5(2)	Cb5(4)	Cr5(4)	Cb5(6)	Cr5(6)
PD3(4)	Cb4(0)	Cr4(0)	Cb4(2)	Cr4(2)	Cb4(4)	Cr4(4)	Cb4(6)	Cr4(6)
PD3(3)	Cb3(0)	Cr3(0)	Cb3(2)	Cr3(2)	Cb3(4)	Cr3(4)	Cb3(6)	Cr3(6)
PD3(2)	Cb2(0)	Cr2(0)	Cb2(2)	Cr2(2)	Cb2(4)	Cr2(4)	Cb2(6)	Cr2(6)
PD3(1)	Cb1(0)	Cr1(0)	Cb1(2)	Cr1(2)	Cb1(4)	Cr1(4)	Cb1(6)	Cr1(6)
PD3(0)	Cb0(0)	Cr0(0)	Cb0(2)	Cr0(2)	Cb0(4)	Cr0(4)	Cb0(6)	Cr0(6)
PD1(7 to 0)	not used							

Table 22 Format 3; customized YUV 4 : 2 : 2 format (FMT-bits in index 00 = 011)

INPUT SIGNAL	CLOCK CYCLE (PIXEL SEQUENCE)							
	0	1	2	3	4	5	6	7
PD2(7 to 0)	Y(0)	Y(1)	Y(2)	Y(3)	Y(4)	Y(5)	Y(6)	Y(7)
PD3(7 to 0)	Cb(0)	–	Cb(2)	–	Cb(4)	–	Cb(6)	–
PD1(7 to 0)	Cr(0)	–	Cr(2)	–	Cr(4)	–	Cr(6)	–

Table 23 Format 4; YUV 4 : 4 : 4 format (FMT-bits in index 00 = 100)

INPUT SIGNAL	CLOCK CYCLE (PIXEL SEQUENCE)							
	0	1	2	3	4	5	6	7
PD2(7 to 0)	Y(0)	Y(1)	Y(2)	Y(3)	Y(4)	Y(5)	Y(6)	Y(7)
PD3(7 to 0)	Cb(0)	Cb(1)	Cb(2)	Cb(3)	Cb(4)	Cb(5)	Cb(6)	Cb(7)
PD1(7 to 0)	Cr(0)	Cr(1)	Cr(2)	Cr(3)	Cr(4)	Cr(5)	Cr(6)	Cr(7)

Table 24 Format 5; RGB 4 : 4 : 4 format (FMT-bits in index 00 = 101)

INPUT SIGNAL	CLOCK CYCLE (PIXEL SEQUENCE)							
	0	1	2	3	4	5	6	7
PD2(7 to 0)	R(0)	R(1)	R(2)	R(3)	R(4)	R(5)	R(6)	R(7)
PD3(7 to 0)	G(0)	G(1)	G(2)	G(3)	G(4)	G(5)	G(6)	G(7)
PD1(7 to 0)	B(0)	B(1)	B(2)	B(3)	B(4)	B(5)	B(6)	B(7)

Table 25 Format 7; indexed colour format (FMT-bits in index 00 = 111), input codes 0 to 255 are allowed, output code of CLUTs should preferably be the same as given in format 5

INPUT SIGNAL	CLOCK CYCLE (PIXEL SEQUENCE)							
	0	1	2	3	4	5	6	7
PD2(7 to 0)	INC(0)	INC(1)	INC(2)	INC(3)	INC(4)	INC(5)	INC(6)	INC(7)

Table 26 Input data levels for formats 0 to 4 and 5; EBU colour bar; 100% white equals 100 IRE intensity, 5% colour saturation for formats 1 to 4, 100% for format 5

INPUT CHANNEL	LEVEL	DIGITAL LEVEL	CODE	CCRIR-BIT	FORMAT
Y	0 IRE	12	offset binary	0	0 to 4
	100 IRE	230			
Cb	bottom peak	−101	two's complement	0	0 to 4
	colourless	0			
	top peak	100			
Cr	bottom peak	−106	two's complement	0	0 to 4
	colourless	0			
	top peak	105			
Y	0 IRE	16	offset binary	1	0 to 4
	100 IRE	235			
Cb	bottom peak	44	offset binary	1	0 to 4
	colourless	128			
	top peak	212			
Cr	bottom peak	44	offset binary	1	0 to 4
	colourless	128			
	top peak	212			
R, G and B	0 IRE	16	offset binary	1	5
	100 IRE	235			

GENLOCK INPUT DATA

Table 27 Format 7; CVBS GENLOCK input data format has an 8-bit word length, the input data comes from an analog-to-digital converter (TDA8708) with gain controlled and clamped CVBS or VBS signals

INPUT SIGNAL	CLOCK CYCLE (PIXEL SEQUENCE)							
	0	1	2	3	4	5	6	7
CVBS(7-0)	CVBS(0)	CVBS(1)	CVBS(2)	CVBS(3)	CVBS(4)	CVBS(5)	CVBS(6)	CVBS(7)
Conditions of CVBS input signal					**two's complement representation**			
Sync bottom					corresponding to binary code −128			
0 IRE (black)					corresponding to binary code −64[1]			
100 IRE (white)					corresponding to binary code 95			
Top peak of 75% colour					corresponding to binary code 95			
Bottom peak of 75% colour					corresponding to binary code −100			

Note

1. If exactly matched levels are required in the internal multiplexer, the value 0 IRE should correspond to −68 and 100 IRE to 82.

ENCODING DATA LEVELS

Input data levels are transformed in three stages:

In the matrix when RGB or indexed colour is applied (formats 5 and 7)

In the normalizing amplifier depending on 50/60 Hz mode and CCIR-bit (index 00)

In the modulator.

Table 28 Y and C output levels for RGB input levels (100/100 colour bar)

SIGNAL	INPUT DATA			MATRIX OUTPUT DATA			NORMALIZER OUTPUT DATA			MODULATOR OUTPUT DATA	
	R	G	B	(R – Y)	Y	(B – Y)	V[1]	Y	U	Y	C[2]
Y and C output levels in 50 Hz mode (PAL)											
White	235	235	235	128	235	128	0	421	0	421	0
Yellow	235	235	16	146	210	16	29	387	−132	387	±135
Cyan	16	235	235	16	170	166	−184	332	44	332	±189
Green	16	235	16	34	145	54	−155	297	−87	297	±178
Magenta	235	16	235	221	107	202	152	245	86	245	±175
Red	235	16	16	240	82	90	183	211	−45	211	±188
Blue	16	16	235	110	41	240	−30	154	131	154	±134
Black	16	16	16	128	16	128	0	120	0	120	0
Blanking	X[3]	X[3]	X[3]	X[3]	X[3]	X[3]	X[3]	X[3]	X[3]	120	0
Burst	X[3]	X[3]	X[3]	X[3]	X[3]	X[3]	45	X[3]	−45	X[3]	±63
Top sync	X[3]	X[3]	X[3]	X[3]	X[3]	X[3]	X[3]	X[3]	X[3]	0	X[3]
Y and C output levels in 60 Hz mode (NTSC)											
White	235	235	235	128	235	128	0	416	0	416	0
Yellow	235	235	16	146	210	16	29	385	−132	385	±135
Cyan	16	235	235	16	170	166	−184	335	44	335	±189
Green	16	235	16	34	145	54	−155	303	−87	303	±178
Magenta	235	16	235	221	107	202	152	256	86	256	±175
Red	235	16	16	240	82	90	183	225	−45	225	±188
Blue	16	16	235	110	41	240	−30	173	131	173	±134
Black	16	16	16	128	16	128	0	142	0	142	0
Blanking	X[3]	X[3]	X[3]	X[3]	X[3]	X[3]	X[3]	X[3]	X[3]	120	0
Burst	X[3]	X[3]	X[3]	X[3]	X[3]	X[3]	0	X[3]	−64	X[3]	±64
Top sync	X[3]	X[3]	X[3]	X[3]	X[3]	X[3]	X[3]	X[3]	X[3]	0	X[3]

Notes

1. The V component is inverted in the PAL line.
2. The ± are peak values of the subcarrier signal.
3. X = not defined.

CHROMINANCE FILTERING IN THE ENCODER

1. Decimation for 4 : 4 : 4 format input data (formats 4, 5 and 7; Fig.4).
2. Interpolation for 4 : 1 : 1 input data into 4 : 2 : 2 data, also suitable to reduce the bandwidth of 4 : 2 : 2 data. This filter is controlled by the SCBW-bit (SCWB = 1 means active).
3. Interpolation at 13.5 MHz for 4 : 2 : 2 input data into 4 : 4 : 4 data before modulating baseband signals onto the colour subcarrier. Figures 5, 6 and 7 show the overall transfer characteristics of chrominance in "standard bandwidth condition" (SCBW = 1). Figures 8 and 9 show the overall transfer characteristics of chrominance in enhanced bandwidth condition (SCBW = 0), which is not possible for 4 : 1 : 1 input data. The transfer curves are slightly different at 12.27 and 14.75 MHz.

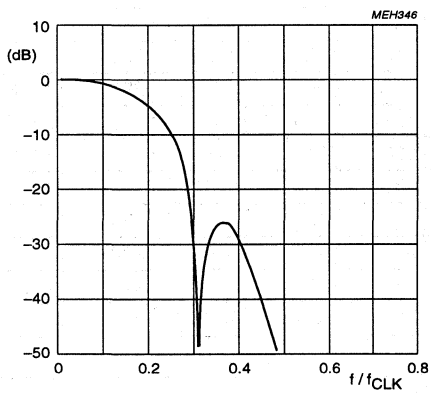


Fig.4 Transfer characteristics of 4 : 4 : 4 to 4 : 2 : 2 decimator.

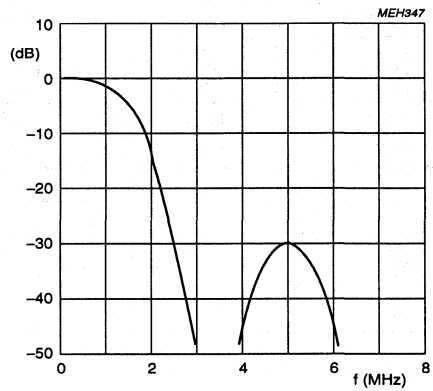


Fig.5 Overall transfer characteristics 4 : 1 : 1 input data.

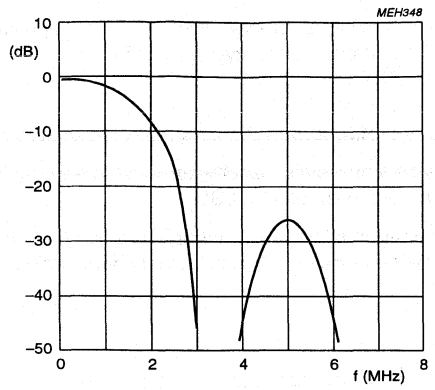


Fig.6 Overall transfer characteristics 4 : 2 : 2 input data (SCBW-bit = 1).

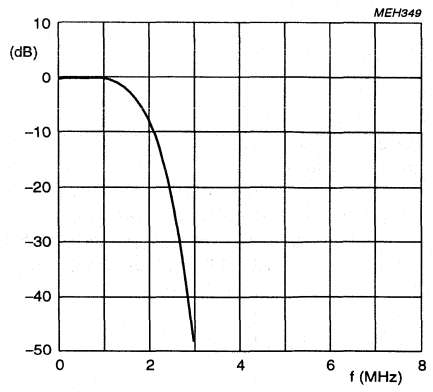


Fig.7 Overall transfer characteristics 4 : 4 : 4 input data (SCBW-bit = 1).

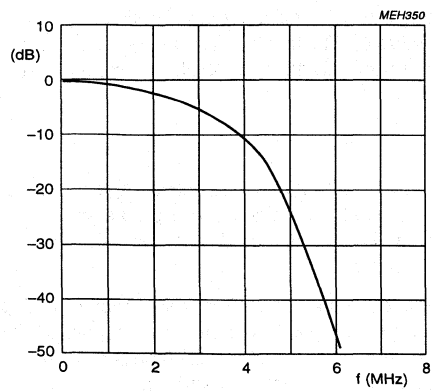


Fig.8 Overall transfer characteristics 4 : 2 : 2 input data (SCBW-bit = 0).

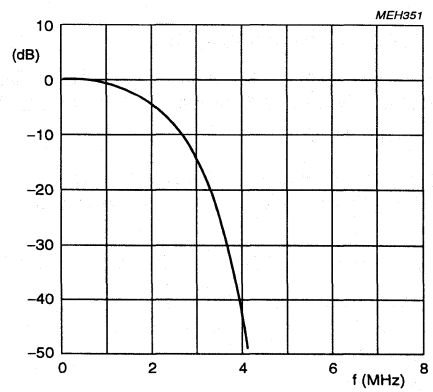


Fig.9 Overall transfer characteristics 4 : 4 : 4 input data (SCBW-bit = 0).

Accuracy of matrix

Evaluation of quantization errors.

The RGB to YUV matrix is achieved in accordance with the following algorithm:

Y = INT
[(NINT(R × 2 × 0.299) + NINT(G × 2 × 0.587) + NINT(B × 2 × 0.114) / 2]

U = NINT [(B – Y) × 0.57722]

V = NINT [(R – Y) × 0.72955].

Errors can occur in the calculation of Y, which as a result influence the U and V outputs. The greatest positive error occurs, if in all of the three for Y calculation used ROMs the values are rounded up to 0.5 LSB, and no truncation error of 0.5 LSB is generated after summation:

$$3 \times \frac{0.5\ \text{LSB}}{2} = +0.75\ \text{LSB};$$

with truncation "error":

$$3 \times \frac{0.5\ \text{LSB}}{2} - 0.5\ \text{LSB} = +0.25\ \text{LSB}.$$

The greatest negative error occurs at rounding off in all the three ROMs and by consecutive truncation:

$$3 \times \frac{-0.5\ \text{LSB}}{2} - 0.5\ \text{LSB} = -1.25\ \text{LSB}.$$

As a result, the matrix error can be ±1 digit, which corresponds to approximately ±0.5% differential non-linearity.

Estimation of noise by quantization

The sum of all sqared quantization errors is SS normalized to 220^3 input combinations (3-dimensional colour scale).

$SS = 0.187545\ LSB^2$.

Compared with noise energy for ideal quantization, $SSI = {}^1/_{12} LSB^2$ results in a deterioration by the conversion matrix of:

D = 10 log (0.187545 × 12) = 3.5 dB (equals 0.5 bit).

If SS is the sum of all squared quantization errors, normalized to 220 input combinations of a grey-scale (R = G = B), then:

$SS = 0.12273\ LSB^2$.

Compared with noise energy for ideal quantization, $SSI = {}^1/_{12} LSB^2$ results in a deterioration by the conversion matrix of:

D = 10 log (0.12273 × 12) = 1.7 dB (equals 0.25 bit).

Normalizing amplifiers in the luminance channel

The absolute amplification error for 50 Hz non-set-up signals is 0.375%; differential non-linearity is –0.333% (equals –1 LSB).

The absolute amplification error for 60 Hz set-up signals is –1.5%; differential non-linearity is –0.365% (equals –1 LSB).

Normalizing amplifiers in the chrominance channel

The absolute amplification error is approximately ±0.5% with a truncation error of –0.5 LSB.

The subcarrier amplitude for standards with luminance set-up is the same as for the standards without luminance set-up.

Modulator

The absolute amplification error is –0.39%; there is no truncation error.

Functional timing (see Fig.10)

GENLOCK MODE

The encoded signal can be generated earlier with respect to CVBS7 to CVBS0 bits (offset t_{ofs} set by GDC-bits; index 05). The HSN output signal can be generated early by PSO-bits (index 07) with respect to $\overline{CB}$ to compensate for pipelining delay t_{Rint} of the RAM interface (valid also in stand alone mode).

The horizontal timing is independent of active video at data inputs PDn(7 to 0). The line blanking period on the outputs is set to approximately 12 µs in 50 Hz standards (11 µs in 60 Hz standards).

SLAVE MODE

HSN pin is used as an input. The active edge of the input signal is assumed to fit to the incoming $\overline{CB}$ signal. Deviations can be compensated in the range of the GCD-bits (index 05).

The t_{enc} time is the total delay from data input to analog CVBS output; it is 55 pixel clock periods long (PIXCLK) plus the propagation delay of the LDV input register regardless of mode and colour standard.

The key input signal is delay compensated with respect to PDn(7 to 0) data input. The generated vertical field and burst blanking sequences are shown in Fig.11 (50 Hz PAL) and Fig.12 (60 Hz NTSC).

Reset

Prior to a reset all outputs are undefined. $\overline{\text{RESET}}$ = LOW sets the circuit into the slave mode.

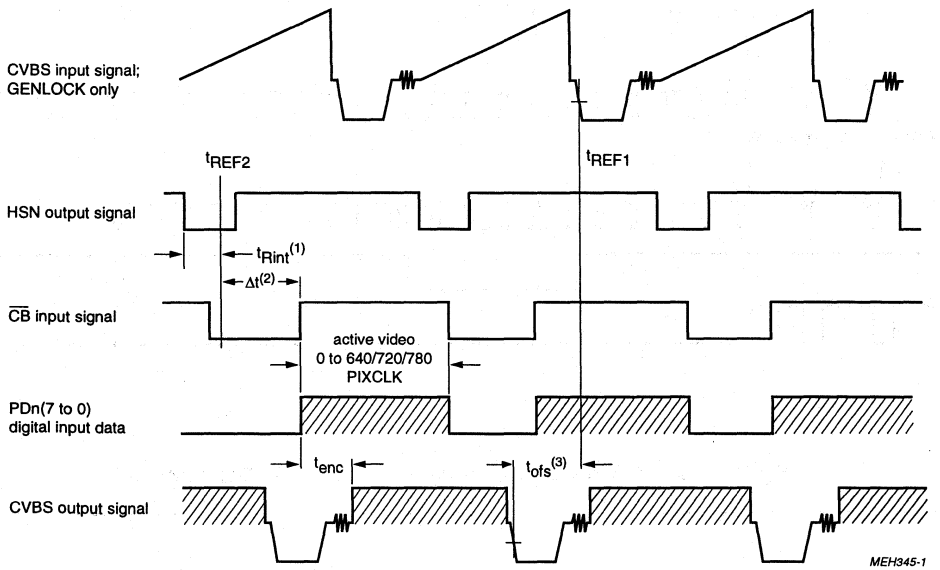
MOD1 bit = 1, MOD0-bit = 0. All other control register bits are set to zero. The outputs CSYN/VSN, HSN, SLT, HSY and HCL are automatically set to a high impedance state.The I^2C-bus interface is set to a slave receiver.

The D7 to D0 pins of the MPU interface are inputs during $\overline{\text{RESET}}$ = LOW. As the circuit requires an external clock signal on pin CLKIN in slave mode, the clock select signal CLKSEL (pin 50) must be LOW during $\overline{\text{RESET}}$ = LOW (pin 54). The LOW time of $\overline{\text{RESET}}$ is at least 50 pixel clock periods long.

Disable chip

All analog outputs are set to zero by DD-bit = 1 (index 08); while the outputs CSYN/VSN, HSN, HCL, HSY and SLT are set to a high impedance state. The internal clock is divided-by-4 at DD-bit = 1. The circuit can be disabled for any reason and it must be disabled when CLKIN exceeds 32 MHz. After setting DD-bit = 1, the CLKIN input signal can be set to a frequency of <60 MHz (modification of control registers and RAM tables is not certain).

To re-enable the circuit, CLKIN must be set to a frequency <32 MHz, a hardware reset is then required to set DD-bit to zero.



(1) t_{Rint} is the pipeline delay of the RAM interface adjustable from −5 to +58 pixel clocks (PIXCLK).
(2) Δt = 125 × PIXCLK at 12.27 MHz
Δt = 163 × PIXCLK at 14.75 MHz
Δt = 134 × PIXCLK at 13.50 MHz in 50 Hz mode
Δt = 122 × PIXCLK at 13.50 MHz in 60 Hz mode.
(3) t_{ofs} is the propagation delay of external GENLOCK line adjustable from −17 to +46 pixel clocks.

Fig.10 Horizontal timing.

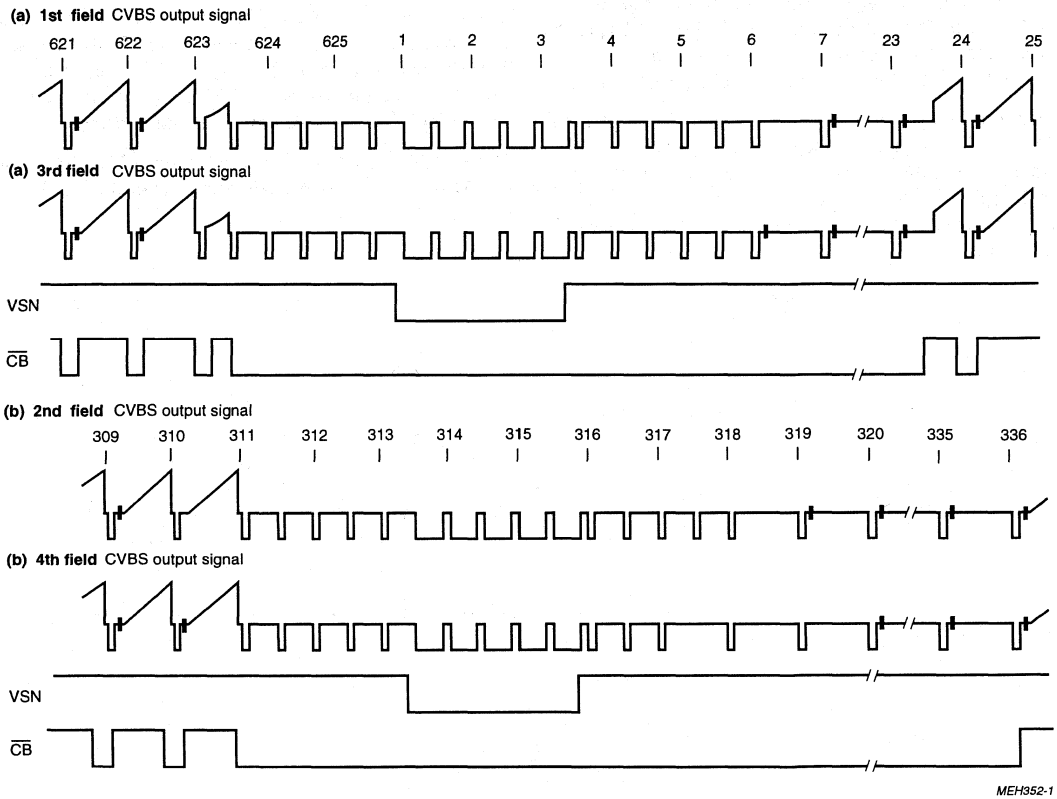


Fig.11 Vertical field and burst blanking sequence for PAL 50 Hz mode.

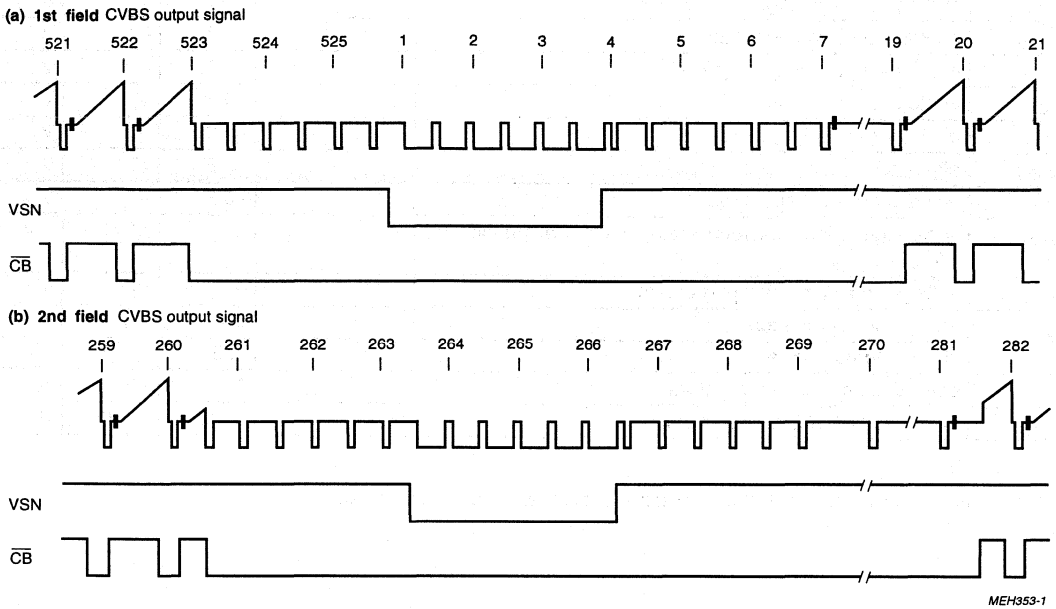


Fig.12 Vertical field and burst blanking sequence for NTSC 60 Hz mode.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDA1}	analog supply voltage 1 (pin 66)		−0.3	+7	V
V_{DDA2}	analog supply voltage 2 (pin 70)		−0.3	+7	V
V_{DDA3}	analog supply voltage 3 (pin 72)		−0.3	+7	V
V_{DDA4}	analog supply voltage 4 (pin 64)		−0.3	+7	V
V_{DDD1}	digital supply voltage 1 (pin 2)		−0.3	+7	V
V_{DDD2}	digital supply voltage 2 (pin 21)		−0.3	+7	V
V_{DDD3}	digital supply voltage 3 (pin 41)		−0.3	+7	V
$V_{diff(GND)}$	voltage difference between analog and digital ground pins ($V_{SSA} - V_{SSDn}$)		−	±100	mV
V_n	voltage on all pins except grounds		0	V_P	V
P_{tot}	total power dissipation		−	1.1	W
T_{stg}	storage temperature		−65	+150	°C
T_{amb}	operating ambient temperature		0	70	°C
V_{esd}	electrostatic handling for all pins	note 1	−2000	+2000	V

Note

1. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

CHARACTERISTICS

V_{DDA} = 4.75 to 5.25 V; V_{DDD} = 4.5 to 5.5 V; T_{amb} = 0 to 70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage (pins 64, 66, 70 and 72)		4.75	5.0	5.25	V
V_{DDD}	digital supply voltage (pins 2, 21 and 41)		4.5	5.0	5.5	V
I_{DDA}	analog supply current I_{DDA1} to I_{DDA4}	40 pF output load	–	–	60	mA
I_{DDD}	digital supply current I_{DDD1} to I_{DDD3}	40 pF output load	–	–	140	mA
Data and control inputs (pins 3 to 20, 23 to 40, 43 to 46, 49, 50, 54 to 56, 59, 73 and 76 to 84)						
V_{IL}	LOW level input voltage	note 1	0	–	0.8	V
V_{IH}	HIGH level input voltage	note 1	2.0	–	V_{DDD} + 0.5	V
I_{LI}	input leakage current		−1	–	+1	µA
C_i	input capacitance					
	data inputs		–	–	8	pF
	CLKIN, LLC and LDV		–	–	10	pF
	3-state I/O		–	–	10	pF
LFCO output (pin 61)						
$V_{o(p-p)}$	output voltage (peak-to-peak value)		1.4	–	2.6	V
V_{61}	output voltage range		0	–	V_{DDD}	V
Data and other control outputs (pins 3, 51, 52, 57, 58, 60, 74 and 75)						
V_{OL}	LOW level output voltage	note 2	0	–	0.6	V
V_{OH}	HIGH level output voltage	note 2	2.4	–	V_{DDD}	V
C, Y and CVBS analog outputs (pins 65, 67 and 69)						
$V_{o(p-p)}$	output voltage (peak-to-peak value)	without load; V_{DDA} = 5 V	–	2	–	V
$V_{o(min)}$	minimum output voltage	without load; V_{DDA} = 5 V	–	0.2	–	V
$V_{o(max)}$	maximum output voltage	without load; V_{DDA} = 5 V	–	2.2	–	V
$R_{o(int)}$	internal serial output resistance	not tested	18	25	35	Ω
R_L	output load resistance	recommendation	90	–	–	Ω
B	output signal bandwidth	−3 dB	10	–	–	MHz
ILE	LF integral linearity error	9-bit data	–	–	±1.0	LSB
DLE	LF differential linearity error	9-bit data	–	–	±0.5	LSB
I_{CUR}	input current (pin 71)	Fig.1; $R_{70\text{-}71}$ = 20 kΩ	–	300	–	µA
I²C-bus SDA and SCL (pins 47 and 48)						
V_{IL}	LOW level input voltage		−0.5	–	+1.5	V
V_{IH}	HIGH level input voltage		3.0	–	V_{DDD} + 0.5	V
I_I	input current	V_I = LOW or HIGH	−10	–	+10	µA
V_{OL}	SDA LOW level output voltage	I_{OL} = 3 mA	–	–	0.4	V
I_O	SDA output current	during acknowledge	3	–	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Crystal oscillator (see Fig.15)						
f_n	nominal frequency	3rd harmonic; Table 1	–	24.576	–	MHz
		3rd harmonic; Table 1	–	26.8	–	MHz
$\Delta f/f_n$	permissible deviation of f_n		–	50	–	10^{-6}
X1 crystal specification						
T_{amb}	ambient temperature range		0	–	70	°C
C_L	load capacitance		8	–	–	pF
R_S	series resonance resistance		–	40	80	Ω
C_{mot}	motional capacitance		–20%	1.5	+20%	fF
C_{par}	parallel capacitance		–20%	3.5	+20%	pF
LDV and LLC timing (pins 20 and 55) see Fig.17						
$T_{cy(LLC)}$	LLC cycle time	note 3	31.5	–	44.5	ns
$t_{W(CH)}$	pulse width		40	50	60	%
t_r	rise time		–	–	5	ns
t_f	fall time		–	–	6	ns
$t_{cy(LDV)}$	LDV cycle time		63	–	89	ns
$t_{su(LDV)}$	LDV set-up time		4	–	–	ns
$t_{h(LDV)}$	LDV hold time		10	–	–	ns
PIXCLK and CLKO timing (pins 51 and 52) see Fig.17						
$t_{d(CLK)}$	PIXCLK and CLKO delay time		–	–	25	ns
PD1 to 3(7 to 0), $\overline{CB}$, MPK, KEY and RTCI input timing (pins 4 to 19, 23 to 32, 57 and 73) see Fig.17						
$t_{SU;DAT}$	input data set-up time		4	–	–	ns
$t_{HD;DAT}$	input data hold time		6	–	–	ns
CVBS(7 to 0), VSN/CSYN and HSN timing (pins 76 to 83, 3 and 84) see Fig.18						
$t_{SU;DAT}$	input data set-up time		10	–	–	ns
$t_{HD;DAT}$	input data hold time		5	–	–	ns
CREF timing (pin 56) see Fig.18						
$t_{SU(CREF)}$	input set-up time		10	–	–	ns
$t_{h(CREF)}$	input hold time		2	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
MPU timing A1, A0, R/$\overline{W}$, $\overline{CS}$, D(7 to 0) (pins 33 to 36, 37 to 40 and 43 to 46) see Fig.19						
$t_{su(ADD)}$	A1 and A0 address set-up time (pins 33 and 34)		4	–	–	ns
$t_{h(ADD)}$	A1 and A0 address hold time		25	–	–	ns
$t_{su(R)}$	R/$\overline{W}$ set-up time (pin 35)		4	–	–	ns
$t_{h(R)}$	R/$\overline{W}$ hold time		25	–	–	ns
$t_{W(CL)}$	$\overline{CS}$ pulse width LOW	note 4	95	–	–	ns
$t_{W(CH)}$	$\overline{CS}$ pulse width HIGH	note 4	95	–	–	ns
$t_{su;DAT}$	data set-up time (D7 to D0)	write mode	80	–	–	ns
$t_{h;DAT}$	data hold time (D7 to D0)	write mode	5	–	–	ns
$t_{d(Q)}$	data output hold time (D7 to D0)	read mode	5	–	–	ns
t_{ZR}	delay to driven ports (D7 to D0)	read mode	5	–	–	ns
$t_{d(ZR)}$	delay to ports valid (D7 to D0)	read mode; note 5	–	–	275	ns
$t_{d(RZ)}$	port outputs disable time (D7 to D0)	read mode	–	–	25	ns
Output timing (pins 3, 74, 75 and 84); see Fig.18						
t_d	output delay time	minimum clock period; note 6	–	20	45	ns

Notes

1. XTALO, XTALI and TP are not characterized with respect to levels; CLKO is characterized up to 32 MHz and PIXCLK up to 16 MHz.
2. Levels are measured with load circuit. LFCO output with 10 kΩ in parallel with 15 pF and other outputs with 1.2 kΩ in parallel with 40 pF at 3 V (TTL load).
3. T_{LLC} must be 63 to 89 ns at CREF = HIGH (pin 56); T_{LLC} = 16.5 ns is only allowed if the multiplexer clock is active.
4. $t_{PIXCLK(min)}$ + 5 ns.
5. 3 × [$t_{PIXCLK(min)}$ + 5 ns].
6. 40 ns at low supply voltage (4 V) and high temperature (70 °C).

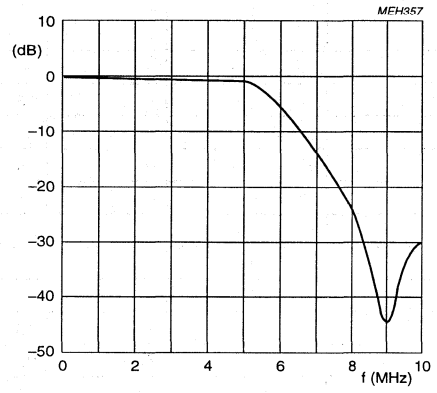


Fig.13 Characteristics of low-pass post-filters; without compensation of DC hold.

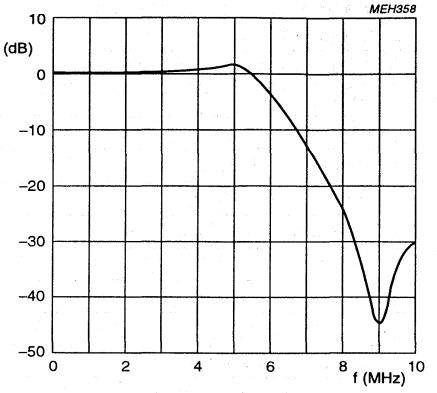
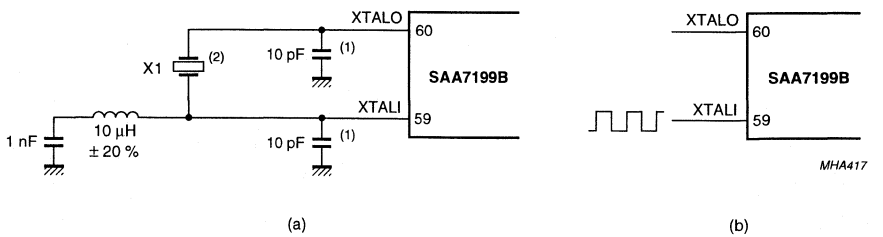
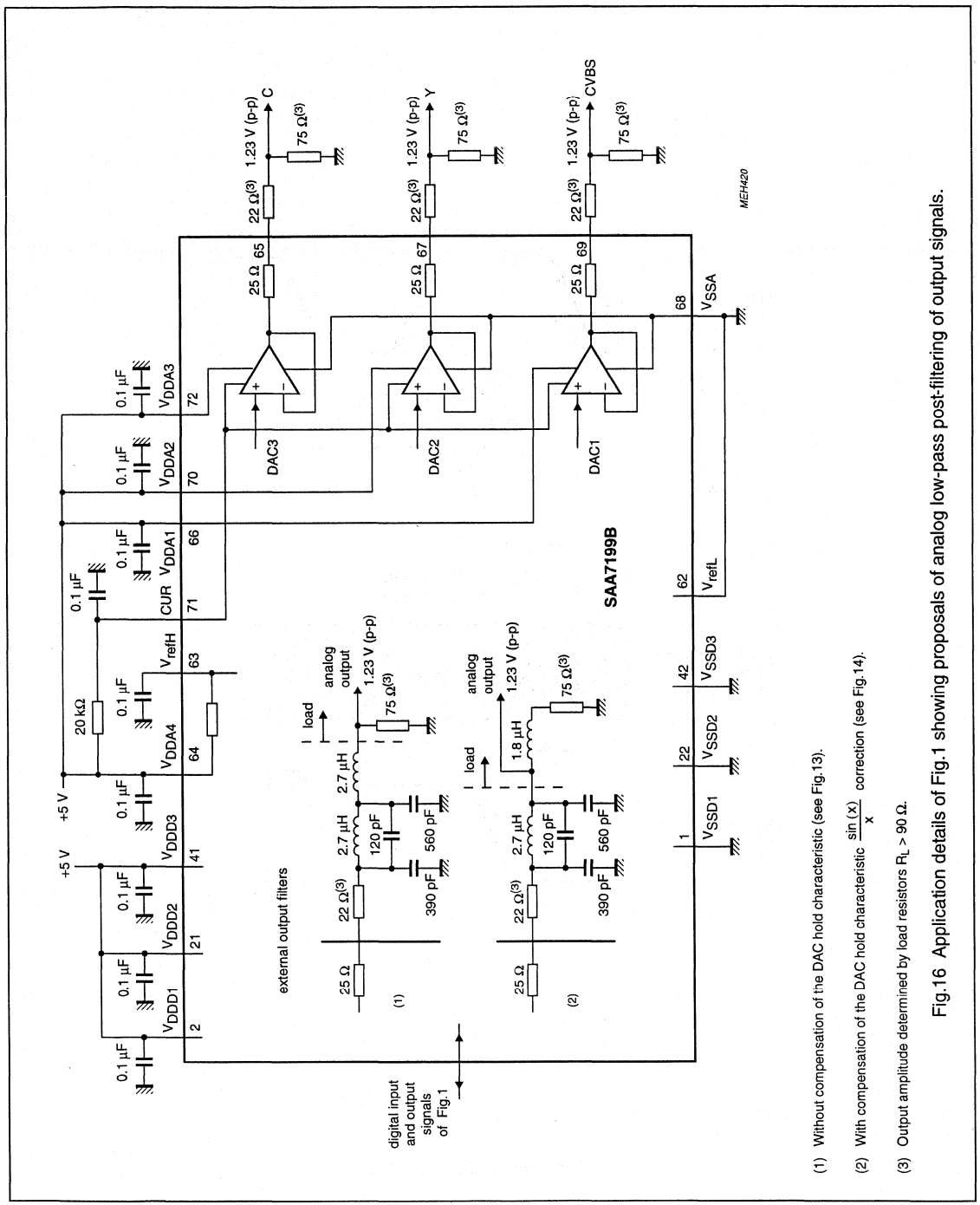


Fig.14 Characteristics of low-pass post-filters.; with compensation of DC hold.



(1) Value depends on crystal parameters.
(2) 24.576 MHz (3rd harmonic), Philips: 4322 143 05291; 26.8 MHz (3rd harmonic), Philips: 9922 520 30004.

Fig.15 Oscillator application (a) and optional external clock sync (b).



(1) Without compensation of the DAC hold characteristic (see Fig.13).

(2) With compensation of the DAC hold characteristic $\frac{\sin(x)}{x}$ correction (see Fig.14).

(3) Output amplitude determined by load resistors $R_L > 90\ \Omega$.

Fig.16 Application details of Fig.1 showing proposals of analog low-pass post-filtering of output signals.

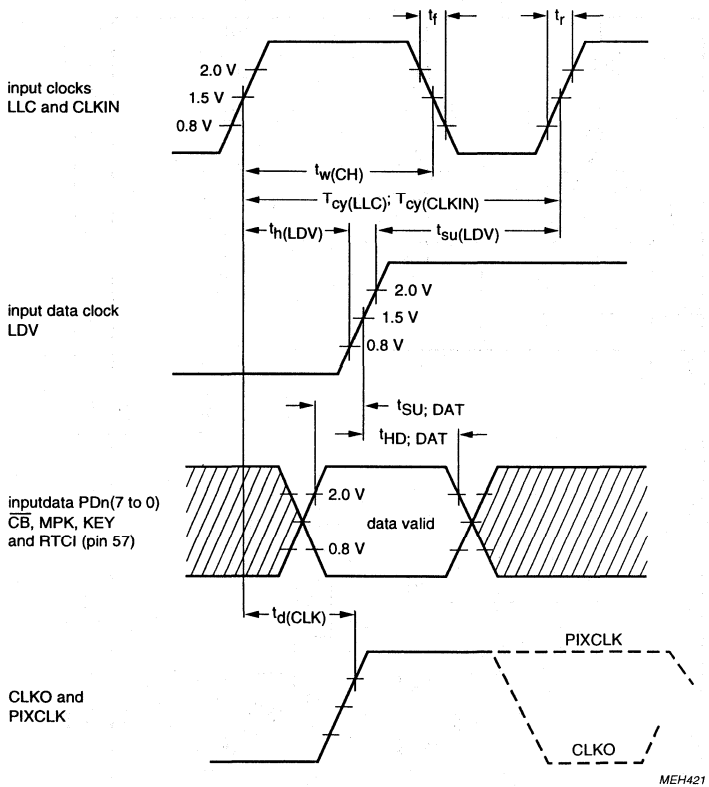


Fig.17 LDV input data timing.

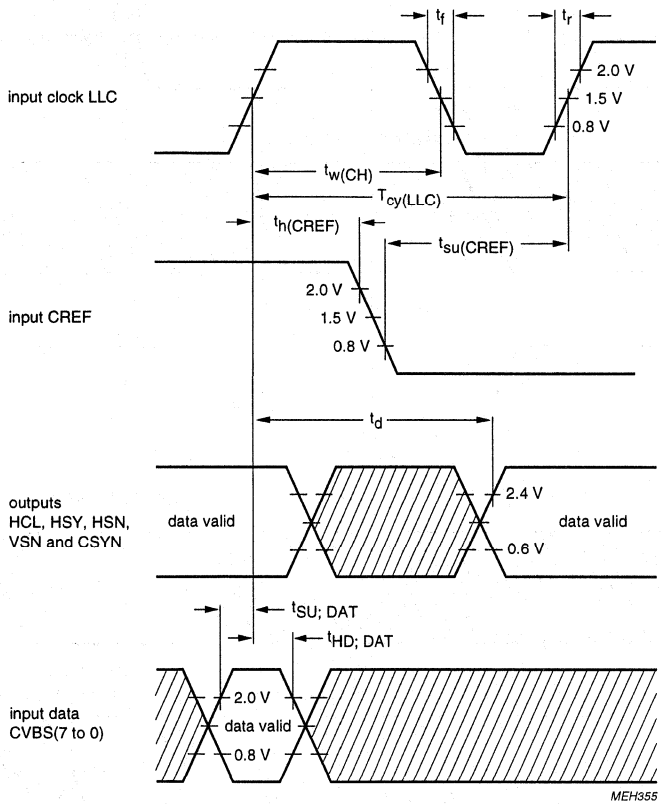


Fig.18 Clock and data timing.

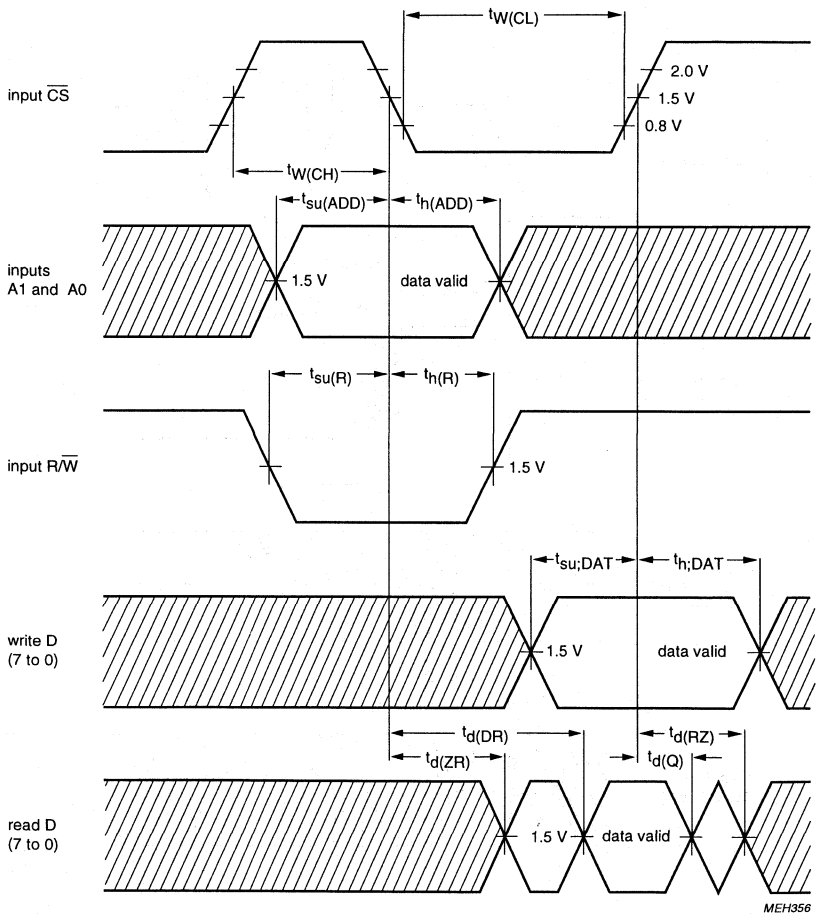


Fig.19 MPU-bus timing.

DVB compliant descrambler SAA7206H

FEATURES

- Input data fully compliant with the Transport Stream (TS) definition of the MPEG-2 systems specification
- Input data signals; [Forward Error Correction (FEC) Interface]
  - Modem data input bus (8-bit wide)
  - Valid input data indicator
  - Erroneous packet indicator
  - First packet byte indicator
  - Byte strobe signal (for asynchronous mode only)

  The interface can be programmed to one of two modes:
  - Asynchronous mode; byte strobe input signal (MBCLK) < 9 MHz, for connection to a modem (FEC)
  - Synchronous mode; MBCLK is not used. Data is delivered to the descrambler synchronized with the chip clock (DCLK) [9 MHz (typ.) with a 33% duty cycle].
- No external memory
- Effective bit rate; $f_{bit} \leq 72$ MHz
- Control interface; 8-bit multiplexed data/address, memory mapped I/O (90CE201 microcontroller parallel bus compatible), in combination with a microcontroller interrupt signal ($\overline{IRQ}$).
- Output ports are identical to the input data interface (demultiplexer interface)
  - Except for the packet error indicator ($\overline{MB}$/MB), as the descrambler translates an active MB signal to the 'transport_error_indicator' bit in the transport stream.
  - Except for the byte strobe input signal (MBCLK), as data is delivered to the demultiplexer, synchronized with the descrambler chip clock which is generated by the demultiplexer.
- Descrambler, based on the super descrambler mechanism algorithm with stream decipher and block decipher. The descrambler is initialized with a 64-bit Control Word (CW) at the beginning of a transport stream packet payload of a selected Packet Identification (PID). The descrambler operates on transport stream packet or Packetized Elementary Stream (PES) packet payloads.
- Microcontroller support; only for control, no specific descrambling tasks are performed by the microcontroller. However, parsing and processing of conditional access information (such as EMM and ECM data) is left to the system microcontroller.
- Boundary scan test port for boundary scan.

GENERAL DESCRIPTION

The SAA7206H (DVB compliant) is designed for use in MPEG-2 based digital TV receivers, incorporating conditional access filters. Such receivers are to be implemented in, for instance, a digital video broadcasting top set box, or an integrated digital TV receiver.

The main function of the descrambler is to descramble the payloads of MPEG-2 TS packets or PES packets. In addition, the descrambler retrieves Conditional Access (CA) data [such as Entitlement Management Messages (EMM) and Entitlement Control Messages (ECM) etc.] from the stream and passes it to the system microcontroller for processing.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7206H	QFP64	plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT319-2

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage		–	–	5.5	V
$V_{DDD(core)}$	digital supply voltage for core		–	–	3.6	V
P_{tot}	total power dissipation	$V_{DDD(core)}$ = 3.3 V, V_{DDD} = 5 V, C_L = 15 pF	–	–	250	mW
f_{clk}	clock frequency	duty cycle = 30 to 55%	–	–	9	MHz
T_{amb}	operating ambient temperature		0	–	70	°C

BLOCK DIAGRAM

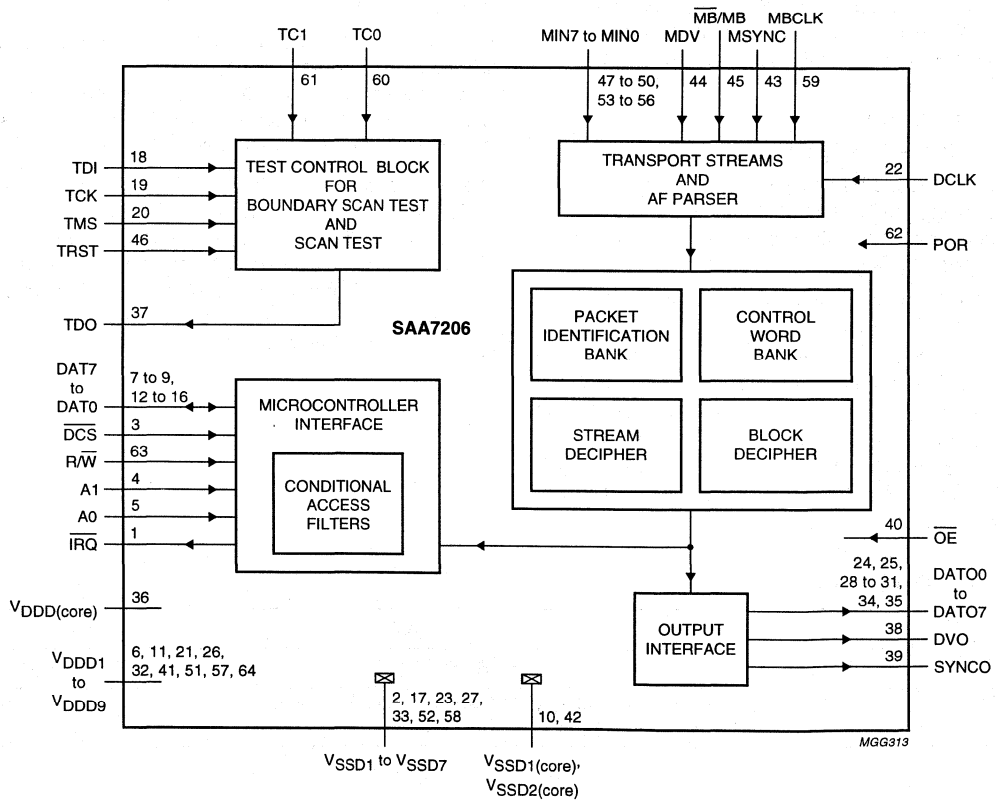


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	I/O	DESCRIPTION
$\overline{IRQ}$	1	O	interrupt request output for microcontroller (active LOW, open-drain output)
V_{SSD1}	2	GND	digital ground 1
$\overline{DCS}$	3	I	descrambler chip select input (active LOW)
A1	4	I	A1 = address/data indicator input
A0	5	I	A0 = MSByte indicator input
V_{DDD1}	6	supply	digital supply voltage 1 (+5 V)
DAT7	7	I/O	microcontroller bidirectional data bus bit 7
DAT6	8	I/O	microcontroller bidirectional data bus bit 6
DAT5	9	I/O	microcontroller bidirectional data bus bit 5
$V_{SSD1(core)}$	10	GND	digital ground 1 for core
V_{DDD2}	11	supply	digital supply voltage 2 (+5 V)
DAT4	12	I/O	microcontroller bidirectional data bus bit 4
DAT3	13	I/O	microcontroller bidirectional data bus bit 3
DAT2	14	I/O	microcontroller bidirectional data bus bit 2
DAT1	15	I/O	microcontroller bidirectional data bus bit 1
DAT0	16	I/O	microcontroller bidirectional data bus bit 0
V_{SSD2}	17	GND	digital ground 2
TDI	18	I	boundary scan test data input
TCK	19	I	boundary scan test clock input
TMS	20	I	boundary scan test mode select input
V_{DDD3}	21	supply	digital supply voltage 3 (+5 V)
DCLK	22	I	9 MHz descrambler chip clock input (duty cycle range: 30 to 55%)
V_{SSD3}	23	GND	digital ground 3
DATO0	24	O	data output to demultiplexer bit 0
DATO1	25	O	data output to demultiplexer bit 1
V_{DDD4}	26	supply	digital supply voltage 4 (+5 V)
V_{SSD4}	27	GND	digital ground 4
DATO2	28	O	data output to demultiplexer bit 2
DATO3	29	O	data output to demultiplexer bit 3
DATO4	30	O	data output to demultiplexer bit 4
DATO5	31	O	data output to demultiplexer bit 5
V_{DDD5}	32	supply	digital supply voltage 5 (+5 V)
V_{SSD5}	33	GND	digital ground 5
DATO6	34	O	data output to demultiplexer bit 6
DATO7	35	O	data output to demultiplexer bit 7
$V_{DDD(core)}$	36	supply	digital supply voltage for core (+3.3 V)
TDO	37	O	boundary scan test data output
DVO	38	O	valid output data indicator
SYNCO	39	O	indicates the first output byte (sync) of a transport packet

SYMBOL	PIN	I/O	DESCRIPTION
$\overline{OE}$	40	I	output enable (active LOW), if HIGH, device outputs are high impedance, (connected to logic 0 in normal operation)
V_{DDD6}	41	supply	digital supply voltage 6 (+5 V)
$V_{SSD2(core)}$	42	GND	digital ground 2 for core
MSYNC	43	I	indicates the first input byte (sync) of a transport packet
MDV	44	I	valid input data indicator
$\overline{MB}$/MB	45	I	packet error indicator input (programmable polarity)
TRST	46	I	boundary scan reset input (LOW in normal operation)
MIN7	47	I	8-bit wide modem data input bit 7
MIN6	48	I	8-bit wide modem data input bit 6
MIN5	49	I	8-bit wide modem data input bit 5
MIN4	50	I	8-bit wide modem data input bit 4
V_{DDD7}	51	supply	digital supply voltage 7 (+5 V)
V_{SSD6}	52	GND	digital ground 6
MIN3	53	I	8-bit wide modem data input bit 3
MIN2	54	I	8-bit wide modem data input bit 2
MIN1	55	I	8-bit wide modem data input bit 1
MIN0	56	I	8-bit wide modem data input bit 0
V_{DDD8}	57	supply	digital supply voltage 8 (+5 V)
V_{SSD7}	58	GND	digital ground 7
MBCLK	59	I	byte strobe input signal < 9 MHz
TC0	60	I	test control input 0 (not connected in normal operation)
TC1	61	I	test control input 1 (not connected in normal operation)
POR	62	I	power-on reset, must be active HIGH during at least 5 DCLK pulses
R/$\overline{W}$	63	I	read/$\overline{write}$ input selection
V_{DDD9}	64	supply	digital supply voltage 9 (+5 V)

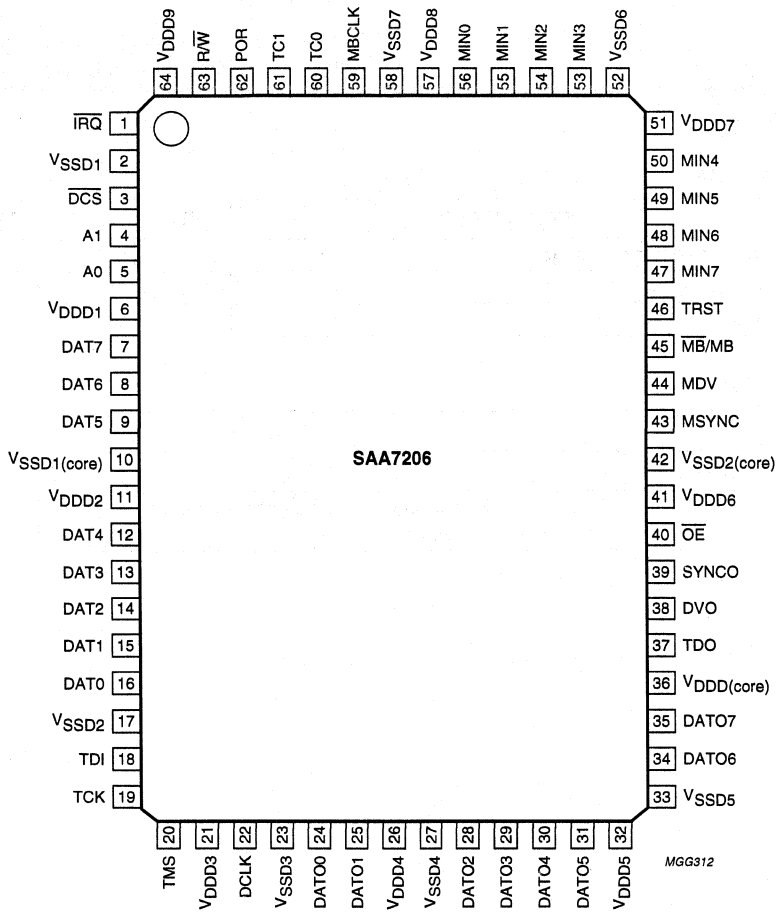


Fig.2 Pin configuration.

Reed Solomon decoder IC SAA7207H

FEATURES

- (204, 188 and 17) Digital Video Broadcasting (DVB) compliant Reed Solomon (RS) codes
- Automatic synchronization of bytes, blocks and frame
- Convolutional de-interleaving (I = 12)
- Energy dispersal de-randomizing
- Contained in a 44-pin quad flat package
- I²C-bus interface
- 6 quasi-bidirectional ports
- Boundary scan facility.

APPLICATIONS

- Forward Error Correction (FEC) for digital TV distribution according to the DVB standard.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	operational supply voltage	4.75	5.00	5.25	V
$I_{DD(tot)}$	total supply current	–	65	–	mA
T_{CLK}	input clock period	–	31.5	–	ns

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7207H/C1	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC02 OR DATA SHEET

BLOCK DIAGRAM

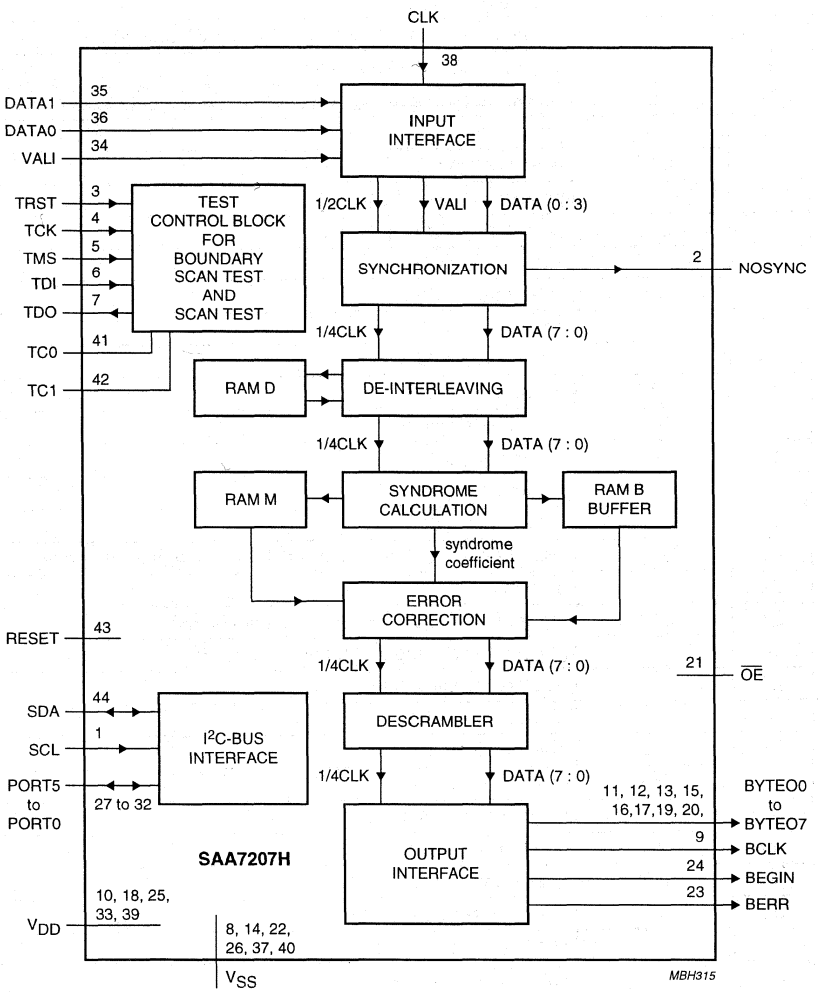


Fig.1 Block diagram.io

PINNING

SYMBOL	PIN	I/O	DESCRIPTION
SCL	1	I	serial clock input (I^2C-bus)
NOSYNC	2	O	not synchronized output (1 = not synchronized)
TRST	3	I	boundary scan test reset (0 = active)
TCK	4	I	boundary scan test clock
TMS	5	I	boundary scan test mode select (1 = BST select)
TDI	6	I	boundary scan test data input
TDO	7	O	boundary scan test data output
V_{SS}	8	–	ground
BCLK	9	O*(1)	byte clock output
V_{DD}	10	–	positive supply voltage
BYTEO0	11	O*(1)	output data byte 0 (LSB)
BYTEO1	12	O*(1)	output data byte 1
BYTEO2	13	O*(1)	output data byte 2
V_{SS}	14	–	ground
BYTEO3	15	O*(1)	output data byte 3
BYTEO4	16	O*(1)	output data byte 4
BYTEO5	17	O*(1)	output data byte 5
V_{DD}	18	–	positive supply voltage
BYTEO6	19	O*(1)	output data byte 6
BYTEO7	20	O*(1)	output data byte 7 (MSB)
$\overline{OE}$	21	I	output enable not (active LOW; 1 = O*(1) high impedance)
V_{SS}	22	–	ground
BERR	23	O*(1)	block error output (1 = uncorrectable block)
BEGIN	24	O*(1)	begin of block output (1st byte of block is output)
V_{DD}	25	–	positive supply voltage
V_{SS}	26	–	ground
PORT5	27	I/O	quasi-bidirectional port 5
PORT4	28	I/O	quasi-bidirectional port 4
PORT3	29	I/O	quasi-bidirectional port 3
PORT2	30	I/O	quasi-bidirectional port 2
PORT1	31	I/O	quasi-bidirectional port 1
PORT0	32	I/O	quasi-bidirectional port 0
V_{DD}	33	–	positive supply voltage
VALI	34	I	valid input (1 = data is valid)
DATA1	35	I	input data 1 (MSB)
DATA0	36	I	input data 0 (LSB)
V_{SS}	37	–	ground
CLK	38	I	master clock input (also acting as input data clock)
V_{DD}	39	–	positive supply voltage
V_{SS}	40	–	ground

SYMBOL	PIN	I/O	DESCRIPTION
TC0	41	I	test mode control input 0 (0 = application mode)
TC1	42	I	test mode control input 1 (0 = application mode)
RESET	43	I	master reset input (1 = active)
SDA	44	I/O	bidirectional serial data port (I^2C-bus)

Note

1. When $\overline{OE}$ is active (pin 21 = HIGH), all O* outputs become high impedance.

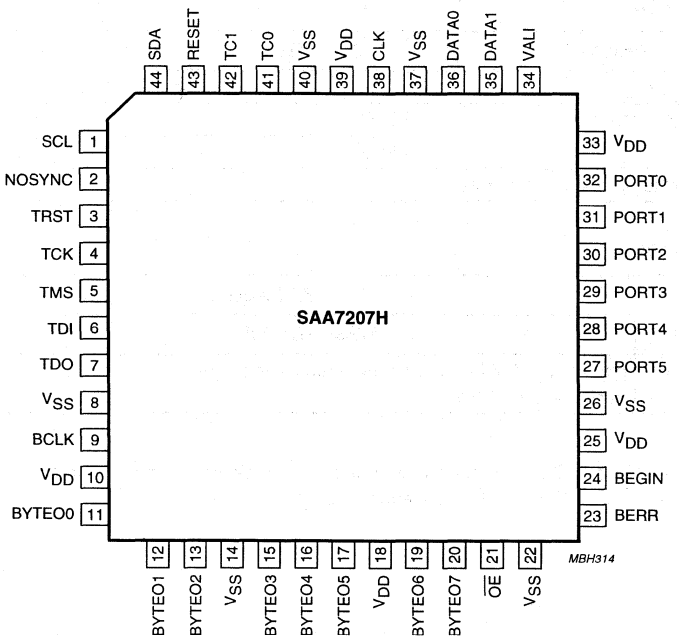


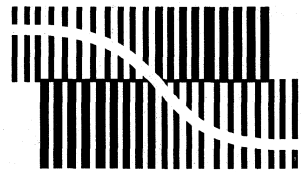
Fig.2 Pin configuration.

Bitstream conversion ADC for digital audio systems

SAA7360

FEATURES

- Stereo input
- Single-ended input
- Uncommitted input buffer for filtering and pre-scaling
- Fully differential analog-to-digital converter (ADC) using 3rd order Sigma-Delta modulation
- 128 times oversampling
- Four stage digital decimation filter
- Switchable high-pass filter to remove DC offsets
- 16-bit or 18-bit selectable output in a multiple of formats
- Sampling rates between 18 and 53 kHz supported
- Master or slave operation
- Choice of 2 crystal frequencies
- Single power supply operation (+5 V).



BITSTREAM CONVERSION

GENERAL DESCRIPTION

The SAA7360 is a CMOS ADC using Philips bitstream conversion technique. The device is designed for digital audio playback systems, such as digital amplifiers, CD-recordable and Digital Compact Cassette (DCC). The device is a complementary device to the SAA7350 bitstream conversion digital-to-analog converter (DAC).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		4.5	5.0	5.5	V
f_{xtal}	crystal frequency	$256f_s$	–	11.2896	–	MHz
		$512f_s$	–	22.5792	–	MHz
THD + N	total harmonic distortion + noise		–	–90	–85	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7360GP	QFP44[1]	plastic quad flat package; 44 leads (lead length 2.35 mm); body 14 × 14 × 2.2 mm	SOT205-1

Note

1. When using IR reflow soldering it is recommended that the Drypack instructions in the *"Quality Reference Pocketbook"* (order number 9398 510 34011) are followed.

BLOCK DIAGRAM

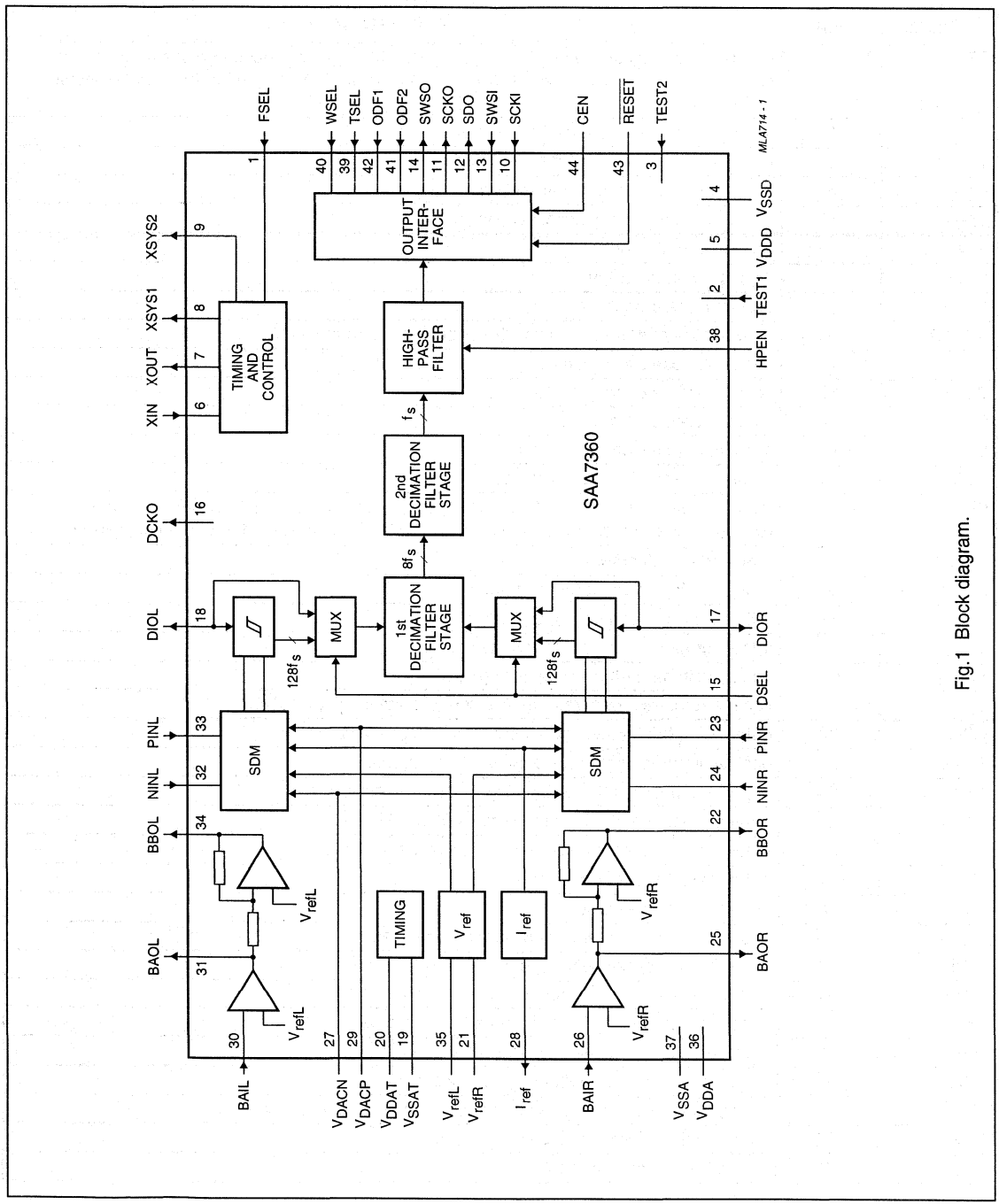


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
FSEL	1	Crystal frequency select input. This pin is used to select the master crystal frequency as follows: FSEL = HIGH = $256f_s$; FSEL = LOW = $512f_s$; if unconnected the pin will default HIGH.
TEST1	2	test input 1; this pin should be left open-circuit
TEST2	3	test input 2; this pin should be left open-circuit
V_{SSD}	4	supply ground for the digital section
V_{DDD}	5	supply voltage for the digital section (+5 V)
XIN	6	crystal oscillator input
XOUT	7	crystal oscillator output
XSYS1	8	system clock output
XSYS2	9	output clock at a frequency half the system clock frequency
SCKI	10	serial interface clock input
SCKO	11	serial interface clock output
SDO	12	serial interface data output
SWSI	13	serial interface word select input
SWSO	14	serial interface word select output
DSEL	15	input for selecting between the internally generated 1-bit code (DSEL = HIGH) or an externally generated 1-bit code (DSEL = LOW); if unconnected this pin defaults HIGH
DCKO	16	1-bit code clock output
DIOR	17	1-bit code input/output (right channel)
DIOL	18	1-bit code input/output (left channel)
V_{SSAT}	19	supply ground for the analog timing section
V_{DDAT}	20	supply voltage for the analog timing section (+5 V)
V_{refR}	21	voltage reference generator for the right channel analog section
BBOR	22	output of right channel buffer operational amplifier 'B'
PINR	23	positive input to right channel Sigma-Delta modulator
NINR	24	negative input to right channel Sigma-Delta modulator
BAOR	25	output of right channel buffer operational amplifier 'A'
BAIR	26	input of right channel buffer operational amplifier 'A'
V_{DACN}	27	negative voltage reference level input for the DACs
I_{ref}	28	current reference output
V_{DACP}	29	positive voltage reference level input for the DACs
BAIL	30	input of left channel buffer operational amplifier 'A'
BAOL	31	output of left channel buffer operational amplifier 'A'
NINL	32	negative input to left channel Sigma-Delta modulator
PINL	33	positive input to left channel Sigma-Delta modulator
BBOL	34	output of left channel buffer operational amplifier 'B'
V_{refL}	35	voltage reference generator for the left channel analog section
V_{DDA}	36	supply voltage for the analog section (+5 V)
V_{SSA}	37	supply ground for the analog section

SYMBOL	PIN	DESCRIPTION
HPEN	38	high-pass filter enable input (HPEN = HIGH = enabled); if unconnected this pin defaults HIGH
TSEL	39	input to select master (TSEL = LOW) or slave (TSEL = HIGH) operation of the serial interface; if unconnected this pin defaults HIGH
WSEL	40	input to indicate 16-bit (WSEL = HIGH) or 18-bit (WSEL = LOW) output data word length of the serial interface; if unconnected this pin defaults HIGH
ODF2 and ODF1	41 and 42	serial interface format inputs; these 2 pins determine the interface format in which the device will operate (see Chapter "Functional Description"); if unconnected these pins will default HIGH (I^2S format)
$\overline{RESET}$	43	Power-On Reset (POR) input (active LOW) to mute the digital output during power on
CEN	44	Chip enable input; this pin, when LOW, disables the operation of the device and 3-states the outputs of the serial interface bus. This enables the connection of one of more devices to the output bus; if unconnected this pin defaults HIGH.

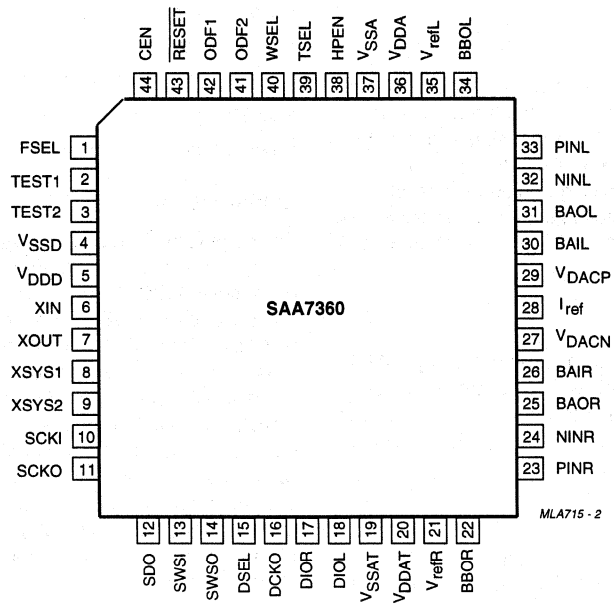


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

General

The SAA7360 is a bitstream conversion CMOS ADC for digital audio systems. The device consists of a input buffer which can be configured by the user for pre-scaling and anti-aliasing, a third order Sigma- Delta modulator with a performance of better than 90 dB THD + Noise, and decimation filters with anti-aliasing suppression of >93 dB and in band ripple of less than 0.0002 dB. The device outputs data in a number of formats compatible with a range of manufacturers.

Clock frequency

The SAA7360 can operate in either master or slave mode (CMOS input drive levels). The clock can be either $256f_s$ or $512f_s$ (where f_s is the sampling frequency) indicated via pin FSEL. System clock outputs equal to the input frequency (XSYS1) and half the input frequency (XSYS2) are provided to drive other ICs in the system. All performance parameters track with f_s which can vary between 18 and 53 kHz without degradation of performance.

Input buffer

The input buffer stage consists of an uncommitted input operational amplifier ('A') and a committed unity gain operational amplifier ('B') to perform a single-to-double ended conversion for the differential ADC. The input buffer can be configured for pre-scaling and second order anti-aliasing filtering. The scaling should be performed so as to provide a maximum of 1 V RMS value at the output of the operational amplifier.

Sigma-Delta modulator

The analog-to-digital conversion is performed by a third order Sigma-Delta modulator, which outputs a 1-bit code at $128f_s$ with a distortion plus noise figure of >90 dB. The modulator is scaled so that a 0 dB input results in an output of –3 dB, at the 1-bit outputs.

Digital decimation filter

The left and right channel 1-bit codes from the ADC are decimated from $128f_s$ to $1f_s$ in four stages of filtering. The first filter stage decimates by a factor of $16f_s$ to $8f_s$ using a 4th order combination type filter. The other three filter stages consist of three cascaded half-band filters each decimating by a factor of two. The half-band filter decimating from $8f_s$ to $4f_s$ has a gain of +2 dB to compensate for the –3 dB through the analog part and allow a headroom of 1 dB to prevent clipping with DC offsets.

The overall response of the digital decimation filter is a pass band from $0f_s$ to $0.454f_s$ (20 kHz at f_s = 44.1 kHz) with a ripple of <0.0002 dB and a transition band of $0.454f_s$ to $0.544f_s$. All frequencies between $0.544f_s$ and $64f_s$ which could result in aliasing into the base band are attenuated by >–93 dB.

High-pass filter

The operational amplifiers in the Sigma-Delta modulator can cause a small DC offset to be present in the 1-bit code passed to the digital section. This can result in the possibility of clicks when switching between devices and the recording of DC offsets which can upset offsets introduced in filters and noise shaping DACs in the playback path. A switchable high-pass filter is included on the IC after the decimation filter stage to allow the user to remove these DC offsets (selectable via pin HPEN). The filter does not affect the decimation process. The filter is 1st order high pass with following specifications:

- Corner frequency (–3 dB): 1.7 Hz
- Ripple: none
- Above 100 Hz: <0.00002 dB; <1 degree
- At 20 Hz: –0.03 dB, 5 degree phase deviation
- Noise floor: –116 dB.

Output interface

The output interface can operate in master or slave mode selectable by pin TSEL. Master mode drives pins SWSO (word select), SCKO (bit clock) and SDO (data output). Slave mode receives the word clock on pin SWSI and the bit clock on pin SCKI. In slave mode the internal circuitry runs on the incoming bit clock and therefore cannot operate with burst clocks. Slave mode causes the pins SWSO and SCKO to be 3-stated allowing systems to connect SWSO and SCKO to pins SWSI and SCKI respectively for applications where the device has to operate in master and slave modes. The bit clock in master mode is at $32f_s$ for 16-bit output, and $64f_s$ for 18-bit output. In slave mode the bit clock is a minimum of $32f_s$ and a maximum of $64f_s$.

Three output formats are supported, I^2S and two pseudo I^2S modes common in digital audio ADC systems. These formats are shown in Fig.3. Selection of the three formats is given in Table 1. 16-bit or 18-bit output words can be chosen (via pin WSEL).

Table 1 Output data formats

ODF2	ODF1	MODE
0	0	test
0	1	format 1
1	0	format 2
1	1	I^2S

Reset

When pin $\overline{RESET}$ is held LOW the data outputs are set to zero. The $\overline{RESET}$ pin operates as a Schmitt trigger, enabling a power-on reset function by using an external RC circuit.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage	note 1	−0.5	+6.5	V
V_I	DC input voltage		−0.5	+6.5	V
I_{IK}	DC input diode current		–	±20	mA
V_O	DC output voltage		−0.5	V_{DD} + 0.5	V
I_O	DC output source or sink current		–	±20	mA
I_{DD} or I_{SS}	total DC V_{DD} or V_{SS} current		–	±0.5	A
T_{amb}	operating ambient temperature		−40	+85	°C
T_{stg}	storage temperature		−65	+150	°C
V_{es}	electrostatic handling	note 2	−2000	+2000	V
		note 3	−200	+200	V

Notes

1. All V_{DD} and V_{SS} pins must be externally connected to the same power supply.
2. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor with a rise time of 15 ns.
3. Equivalent to discharging a 200 pF capacitor via a 2.5 μH series inductor.

CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = 25 °C; $f_{xtal} = 256f_s$; f_s = 44.1 kHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
I_{DDA}	analog supply current		–	43	–	mA
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
I_{DDD}	digital supply current		–	50	–	mA
P_{tot}	total power consumption		–	465	–	mW

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital part inputs						
FSEL, HPEN, DSEL, TSEL, WSEL, ODF2, ODF1 AND CEN						
V_{IL}	LOW level input voltage	note 1	−0.5	–	+0.8	V
V_{IH}	HIGH level input voltage	note 1	2.0	–	V_{DDD} + 0.5	V
Z_i	input impedance		–	35	–	kΩ
C_i	input capacitance		–	–	10	pF
$\overline{RESET}$						
V_{IL}	LOW level input voltage	note 1	−0.5	–	+0.2V_{DDD}	V
V_{IH}	HIGH level input voltage	note 1	0.6V_{DDD}	–	V_{DDD} + 0.5	V
ΔV_I	input hysteresis		0.2	–	–	V
I_{LI}	input leakage current	note 2	−10	–	+10	µA
C_i	input capacitance		–	–	10	pF
SCKI and SWSI						
V_{IL}	LOW level input voltage	note 1	−0.5	–	+0.8	V
V_{IH}	HIGH level input voltage	note 1	2.0	–	V_{DDD} + 0.5	V
I_{LI}	input leakage current		−10	–	+10	µA
C_i	input capacitance		–	–	10	pF
Crystal oscillator input XIN						
V_{IL}	LOW level input voltage		−0.5	–	+0.8	V
V_{IH}	HIGH level input voltage		0.7V_{DDD}	–	V_{DDD} + 0.5	V
I_{LI}	input leakage current	note 2	−10	–	+10	µA
C_i	input capacitance		–	–	10	pF
Outputs						
SWSO, SCKO AND SDO						
V_{OL}	LOW level output voltage	−400 µA; note 1	–	–	+0.4	V
V_{OH}	HIGH level output voltage	20 µA; note 1	2.4	–	–	V
C_L	load capacitance		–	–	50	pF
I_{LI}	leakage current in 3-state	note 2	−10	–	+10	µA
XSYS1 AND XSYS2						
V_{OL}	LOW level output voltage	−400 µA; note 1	–	–	0.4	V
V_{OH}	HIGH level output voltage	20 µA; note 1	2.4	–	–	V
C_L	load capacitance		–	–	35	pF
DCKO						
V_{OL}	LOW level output voltage	−400 µA; note 1	–	–	1.0	V
V_{OH}	HIGH level output voltage	20 µA; note 1	V_{DDD} − 1.0	–	–	V
C_L	load capacitance		–	–	20	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input/outputs DIOR and DIOL						
V_{IL}	LOW level input voltage	note 1	−0.5	–	+0.8	V
V_{IH}	HIGH level input voltage	note 1	2.0	–	V_{DDD} + 0.5	V
Z_i	input impedance		–	35	–	kΩ
C_i	input capacitance		–	–	10	pF
V_{OL}	LOW level output voltage	−400 μA; note 1	–	–	1.0	V
V_{OH}	HIGH level output voltage	20 μA; note 1	V_{DDD} − 1.0	–	–	V
C_L	load capacitance		–	–	20	pF
Crystal oscillator input XIN and output XOUT						
f_{xtal}	crystal operating frequency	note 3	4.608	$256f_s$ or $512f_s$	27.136	MHz
G_m	mutual conductance	100 kHz	1.5	–	–	mA/V
G_v	small signal voltage gain	$G_v = G_m \times R_o$	–	3.5	–	V/V
C_i	input capacitance		–	–	10	pF
C_{FB}	feedback capacitance		–	–	5	pF
C_o	output capacitance		–	–	10	pF
I_{LI}	input leakage current	note 2	−10	–	+10	μA
Timing						
External clock input XIN						
f_i	input frequency	note 3	4.608	$256f_s$ or $512f_s$	27.136	MHz
t_r	input rise time	V_{IL} to V_{IH}	–	–	10	ns
t_f	input fall time	V_{IH} to V_{IL}	–	–	10	ns
msr	mark-space ratio	slave mode; $256f_s$	45	–	55	%
		slave mode; $512f_s$	40	–	60	%
System clock outputs XSYS1 and XSYS2 (note 4)						
t_r	output rise time	V_{OL} to V_{OH}	–	–	15	ns
t_f	output fall time	V_{OH} to V_{OL}	–	–	15	ns
t_H	output HIGH time (relative to clock period)	note 5	40	50	60	%
1-bit code outputs (see Fig.4); **1-bit code inputs** (see Fig.5)						
CLOCK DCKO						
t_r	clock output rise time	note 6	–	–	15	ns
t_f	clock output fall time	note 6	–	–	15	ns
t_H	clock output HIGH time		45	–	–	ns
t_L	clock output LOW time		45	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DATA DIOL AND DIOR						
t_{dor}	data output rise time	note 6	–	–	15	ns
t_{dof}	clock output fall time	note 6	–	–	15	ns
t_d	data output delay time (relative to DCKO)	note 6	−30	–	+30	ns
t_{dir}	data input rise time		–	–	20	ns
t_{dif}	data input fall time		–	–	20	ns
t_{su}	data input set-up time (relative to DCKO)		30	–	–	ns
t_h	data input hold time (relative to DCKO)		30	–	–	ns
Serial data outputs (see Fig.6)						
CLOCK SCKO						
t_r	clock output rise time	note 7	–	–	30	ns
t_f	clock output fall time	note 7	–	–	30	ns
WORD SELECT SWSO						
t_r	word select output rise time	note 7	–	–	30	ns
t_f	word select output fall time	note 7	–	–	30	ns
t_{sr}	word select output set-up time	note 8	100	–	–	ns
t_{hr}	word select output hold time	note 8	100	–	–	ns
CLOCK SCKI (note 9)						
t_r	clock input rise time		–	–	100	ns
t_f	clock input fall time		–	–	100	ns
t_{HC}	clock input HIGH time		50	–	–	ns
t_{LC}	clock input LOW time		50	–	–	ns
WORD SELECT SWSI (note 9)						
t_r	word select input rise time		–	–	100	ns
t_f	word select input fall time		–	–	100	ns
t_{sr}	word select input set-up time	note 10	100	–	–	ns
t_{hr}	word select input hold time	note 10	100	–	–	ns
DATA SDO						
t_r	data output rise time	note 7	–	–	30	ns
t_f	data output fall time	note 7	–	–	30	ns
t_{dod}	data output delay time	note 10	−100	–	+100	ns
t_{sr}	data output set-up time	note 8	100	–	–	ns
t_{hr}	data output hold time	note 8	100	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog part						
VOLTAGE REFERENCE V_{refL} AND V_{refR}						
V_I	input voltage		2.0	2.3	2.7	V
Current reference I_{ref} (note 11)						
I_O	output current		–	$\frac{V_{refR}}{13\ k\Omega}$	–	A
DAC reference						
INPUT V_{DACN}						
V_I	input voltage		–	V_{SSA}	–	V
INPUT V_{DACP}						
V_I	input voltage		–	V_{DDA}	–	V
Sigma-Delta modulator inputs PINR, NINR, PINL and NINL						
$V_{I(rms)}$	input voltage (RMS value)	note 12	–	1	–	V
ADC performance (note 13)						
THD + N	total harmonic distortion + noise	at –1 dB digital output; note 14	–	–90 (0.003%)	–85 (0.0056%)	dB
DR	dynamic range	note 14	93	97	–	dB
α_{cs}	channel separation	f_i = 1 kHz; note 15	–	100	–	dB
G	gain		–1.5	–1	–0.5	dB
t_{gd}	group delay (in pass band)	note 16	–	1.25	–	ms

Notes

1. Minimum V_{IL}, V_{OL} and maximum V_{IH}, V_{OH} are peak values to allow for transients.
2. I_{LI} minimum and I_{LO} minimum measured at V_I = 0 V; I_{LI} maximum and I_{LO} maximum measured at $V_I = V_{DDD}$.
3. f_{xtal} is a multiple of the system sampling frequency f_s which can vary between 18 and 53 kHz.
4. Output times are measured with a capacitive load of 35 pF; XSYS2 is the master clock frequency divided by 2.
5. t_H valid only when used with XTAL, with 50% input mark space ratio; XSYS1 (t_H) is measured at $\frac{1}{2}V_{DDD}$.
6. Output times are measured with a capacitive load of 20 pF.
7. Output times are measured with a capacitive load of 50 pF.
8. Relative to SCKO in master mode.
9. In slave mode the number of SCKI clocks in each channel should be <33 and the same in both. The polarity of SWSI indicates left/right channel.
10. Relative to SCKI in slave mode.
11. I_{ref} connected to 0 V via a 13 kΩ resistor.
12. The maximum recommended input voltage (referred to as 0 dB) yields a –1 dB output (relative to full-scale digital swing). The input voltage scales with $V(V_{DACP}) - V(V_{DACN})$; almost equal to V_{DDA}, hence:

$$V_I\ (0\ dB) = \frac{[V(V_{DACP}) - V(V_{DACN})]}{5} V\ (RMS\ value)$$

13. Device measured with external components as shown in recommended application diagram (see Fig.7).

14. Typical values are for 18-bit performance, minimum and/or maximum values are for 16-bit performance.
15. This is the ratio (in dB) of the digital output amplitude of single tone, in one channel, to the digital output amplitude of the same tone in the measurement channel. This definition presupposes that the channels have the same gain.
16. Group delay $= \frac{(55.5 \pm 1)}{f_s}$, where f_s is the output sampling frequency. Typical value given is for $f_s = 44.1$ kHz.

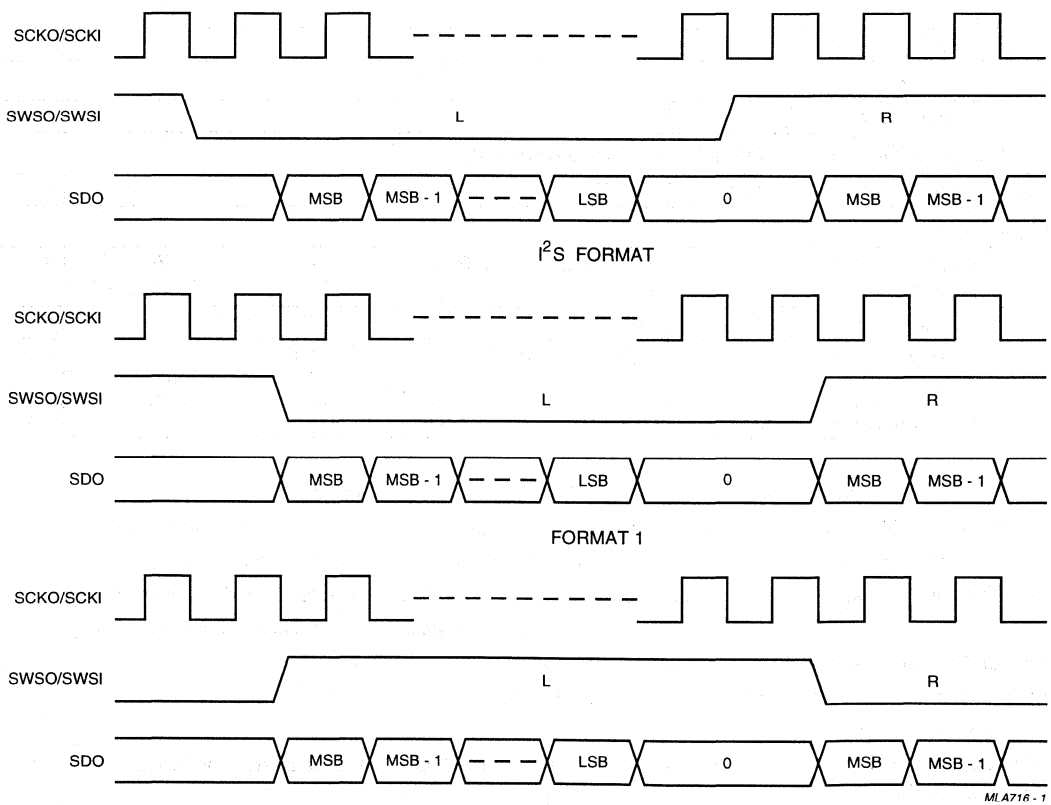


Fig.3 Output interface modes.

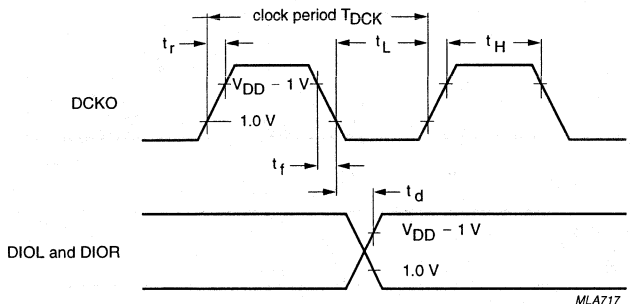


Fig.4 One bit code output timing.

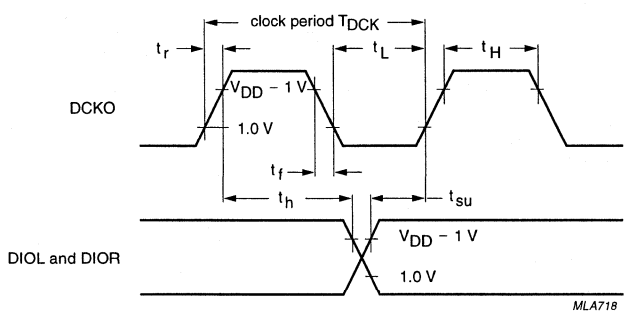


Fig.5 One bit code input timing.

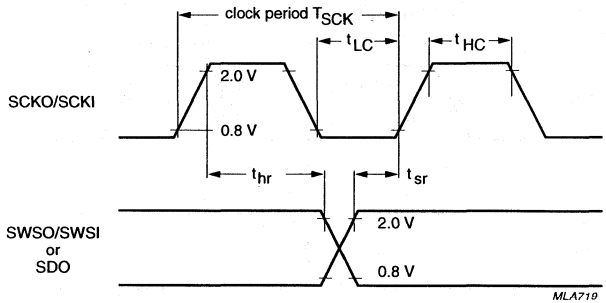


Fig.6 Serial output timing.

APPLICATION INFORMATION

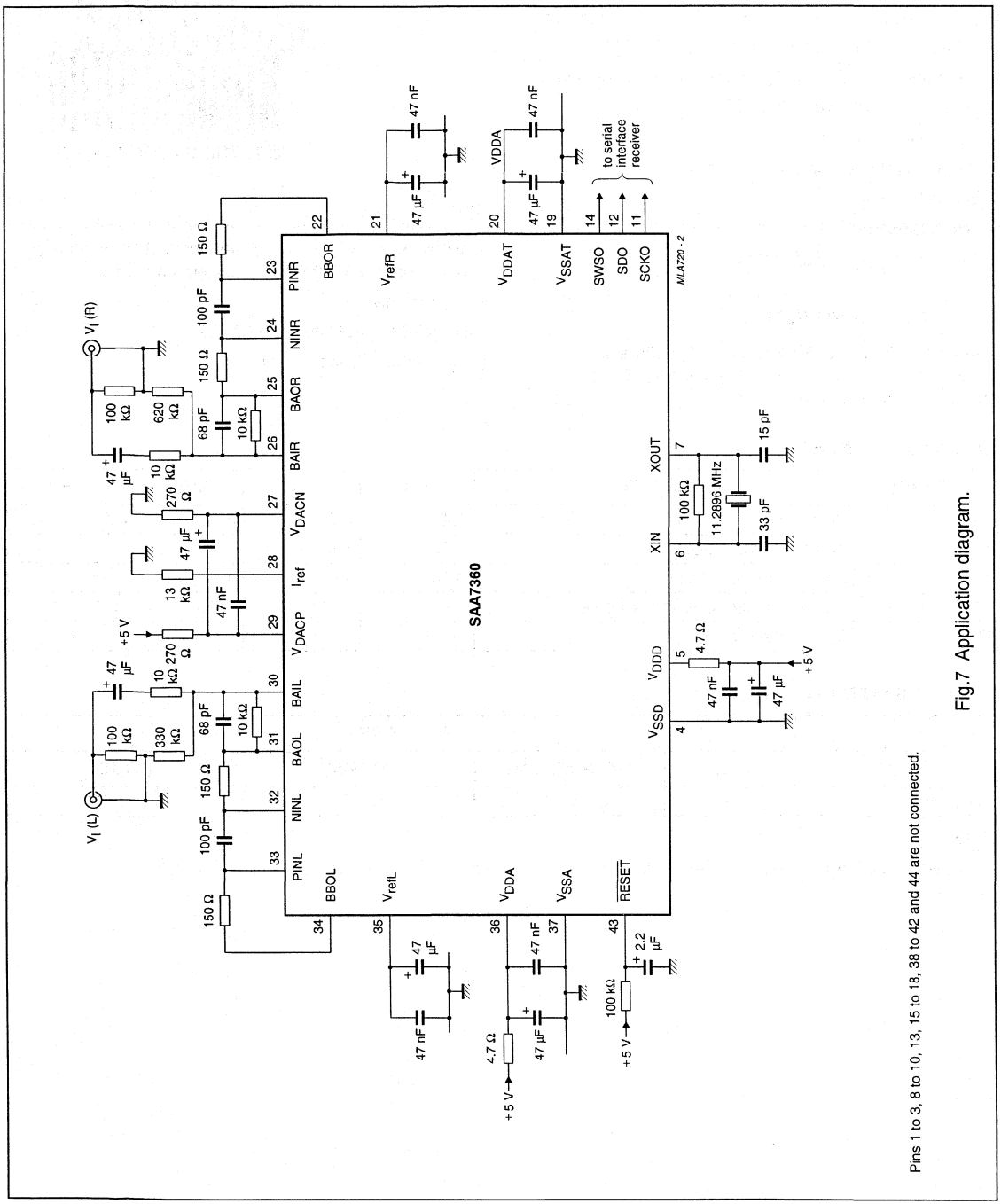


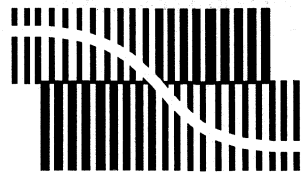
Fig.7 Application diagram.

Bitstream conversion ADC for digital audio systems

SAA7366

FEATURES

- Integrated buffers for simple interfacing to analog inputs
- 4 flexible serial interface modes
- Overload detection of digital signal ≥−1 dB amplitude
- Selectable high-pass filter
- 18-bit serial output
- 3.4 to 5.5 V operation of digital part
- Standby mode
- SO24 package
- Small non-critical PCB layout.



BITSTREAM CONVERSION

GENERAL DESCRIPTION

The SAA7366 is a CMOS cost effective stereo analog-to-digital converter (ADC) using the Philips bitstream conversion technique.

APPLICATIONS

The device is designed for digital acquisition of analog audio signals for digital audio systems such as:

- CD-recordable
- Digital Compact Cassette (DCC)
- Digital Audio Tape (DAT).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage	3.4	5.0	5.5	V
V_{DDA}	analog supply voltage	4.5	5.0	5.5	V
f_i	clock input frequency	4.608	12.288	13.568	MHz
THD + N	total harmonic distortion + noise	–	–	−80	dB
DR	dynamic range	90	–	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7366T[1]	24	SO24L	plastic	SOT137A

Note

1. Plastic small outline package; 24 leads; body width 7.5 mm; (SOT137A); SOT137-1; 1996 Oct 29.

BLOCK DIAGRAM

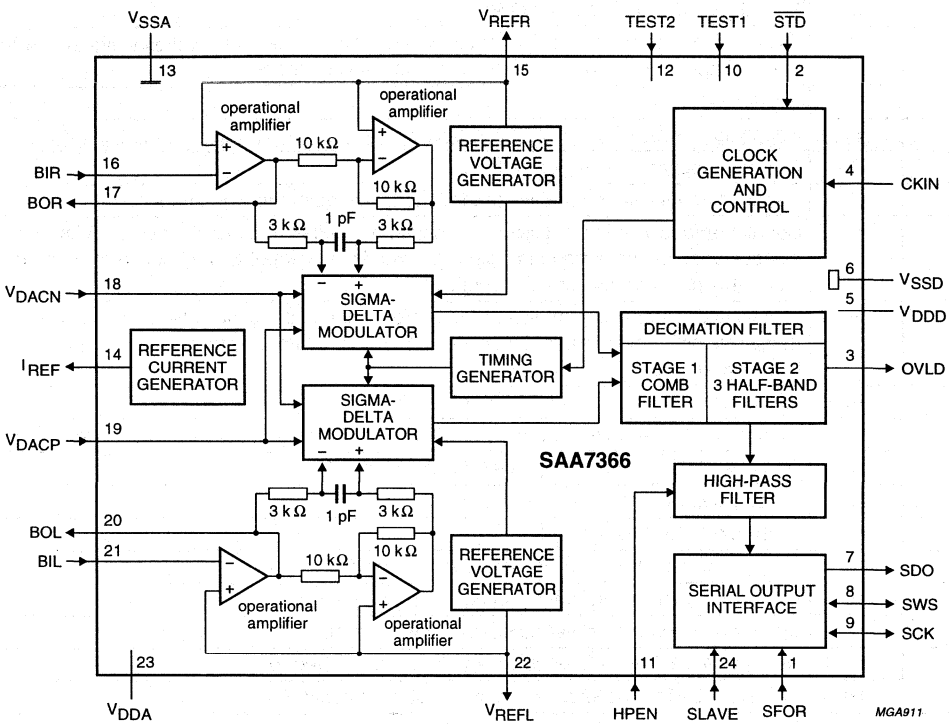


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SFOR	1	Serial interface output format select. Output format is selected as follows: SFOR HIGH = Format 1; SFOR LOW = Format 2.
$\overline{STD}$	2	Standby mode input (active LOW).
OVLD	3	Overload indication output. This pin indicates whether the internal digital signal is within 1 dB of maximum. In standby mode this output is high impedance.
CKIN	4	System clock input.
V_{DDD}	5	Supply for the digital section (3.4 to 5.5 V).
V_{SSD}	6	Ground supply for the digital section.
SDO	7	Serial interface data output. In standby mode this output is high impedance.
SWS	8	Serial interface word select signal. In master mode this pin outputs the serial interface word select signal. In slave mode this pin is the word select input to the serial interface. In standby mode this pin is always an input (high impedance).
SCK	9	Serial interface clock. In master mode this pin outputs the serial interface bit clock. In slave mode this pin is the input for the external bit clock. In standby mode this output is high impedance.
TEST1	10	Test input 1. This pin should be left open-circuit.
HPEN	11	High-pass filter enable input. (HPEN HIGH = enabled). If unconnected this pin defaults HIGH.
TEST2	12	Test input 2. This pin should be left open-circuit.
V_{SSA}	13	Ground supply for the analog section.
I_{REF}	14	Current reference output node.
V_{REFR}	15	$\frac{1}{2}V_{DDA}$ reference generator output for the right channel analog section.
BIR	16	Buffer operational amplifier inverting input for right channel.
BOR	17	Buffer operational amplifier output for right channel.
V_{DACN}	18	Negative 1-bit DAC reference voltage input, connected to 0 V.
V_{DACP}	19	Positive 1-bit DAC reference voltage input, connected to +5 V.
BOL	20	Buffer operational amplifier output for left channel.
BIL	21	Buffer operational amplifier inverting input for left channel.
V_{REFL}	22	$\frac{1}{2}V_{DDA}$ reference generator output for the left channel analog section.
V_{DDA}	23	Supply for the analog section.
SLAVE	24	Serial interface operating output mode master/slave select as follows: HIGH = slave mode; LOW = master mode. If unconnected the pin will default LOW.

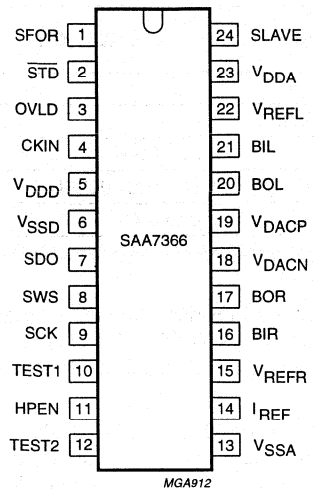


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

General

The SAA7366 is a bitstream conversion CMOS ADC for digital audio systems. The conversion is achieved using a third order Sigma-Delta modulator (SDM), operating at 128 times the output sample frequency (f_s). The high oversampling ratio greatly simplifies the design of the analog input anti-alias filter. In most cases the internal buffer operational amplifier, configured as a low-pass filter will suffice. The 1-bit code from the Sigma-Delta modulator is filtered and down-sampled (decimated) to $1f_s$ in two stages of filtering. An optional high-pass filter is provided to remove DC, if required. The device has been designed with ease of use, low board area and low application costs in mind.

Clock frequency

The external clock, input on pin CKIN, operates at 256 times f_s, which can range from 18 kHz to 53 kHz.

Input buffer

Two input buffers are provided, one for each channel, for signal amplitude matching, signal buffering and anti-alias filter purposes. These are configured for inverting use. Access is provided by pins BIL, BIR (inverting inputs) and BOL, BOR (outputs) for left and right channels respectively. By the choice of feedback component values, the application signal amplitude can be matched to the requirements of the ADC. Typically the operational amplifiers are configured as low-pass filters with a gain of 1 and a pole at approximately $5f_s$.

Remark: The complete ADC is non-inverting. Hence a positive DC input (referenced to V_{ref}) will yield a positive digital output.

Input level

The overall system gain is proportional V_{DDA}, or more accurately $\{V(V_{DACP}) - V(V_{DACN})\}$. For convenience the ADC input signal amplitude is defined as that amplitude seen on BOL or BOR, the operational amplifier outputs (i.e. the input to the Sigma-Delta modulator). Also, the 0 dB input level is defined as that which provides a –1 dB (actually –1.08 dB) digital output, relative to full-scale swing. This offset provides headroom to accommodate small random DC offsets without causing the digital output to clip.

Hence:

$$V_I(0\ dB) = \frac{V(V_{DACP}) - V(V_{DACN})}{5} = V\ (RMS)$$

The user of the IC should ensure, that when all sources of signal amplitude variation are taken into account, the maximum input signal should conform to the 0 dB level. If not, clipping may occur. In the event that the maximum signal level cannot be pre-determined, e.g. a live microphone input, the average signal level should be set at –10 to –20 dB down. The exact value will depend on the application and the balance between head room and operating signal-to-noise ratio.

Behaviour during overload

As defined earlier the maximum input level for normal operation is 0 dB. If the input level exceeds this value clipping may occur. Infringements are limited to the maximum permitted positive or negative values, $2^{17} - 1$ or -2^{17} respectively. If the high-pass filter has been enabled the clipped output samples may have non-maximum values due to the removal of the DC content. Input signals in the range of 0 to 1 dB may or may not be clipped depending on the values of DC dither and small random offsets in the analog circuitry.

When using the recommended application circuitry, clipping will initially be observed on negative peaks due to the use of negative DC dither.

The maximum level of overload that can be safely tolerated is application circuit dependent. In the case of the

recommended circuit the following applies: the inverting operational amplifier inputs BIL/BIR are protected from excessive voltages (currents) by diodes to V_{DDA} and V_{SSA}. These have absolute maximum ratings of $I_{IK} = \pm 20$ mA, with a safe practical limit of ±2 mA. Given the input resistor of 10 kΩ, ±2 mA diode current and the operation of the operational amplifier a maximum signal (applied to the input resistor) of ±30 V can be handled safely. This level represents an overload of 26 dB.

During overload the in-band portion of the waveform will be correctly converted. The out-of-band portion will be limited as detailed above.

Sigma-Delta modulator

The SAA7366 has two third order Sigma-Delta modulators with a quantization noise floor of approximately −104 dB. The scaling of the feedback has been optimized for stable operation even during overload. Thus with a maximum signal swing of 0 V to V_{DDA} on the input the digital output remains well behaved, i.e. it does not burst into random oscillation. During overload the output is simply a clipped version of the input. The gain of this stage is −4.95 dB.

Decimation filter

Decimation from $128f_s$ is performed in two stages. The first stage is a comb filter, which decimates from 128 to $8f_s$. The second stage, consists of 3 half-band filters, each decimating by a factor of 2.

The overall characteristics are given in Table 1.

Table 1 Overall filter characteristics.

ITEM	CONDITION	VALUE (dB)
Pass band ripple	0 to $0.45f_s$ Hz	±0.1
	0.45 to $0.47f_s$	−0.5
Stop band	$>0.55f_s$	−60
Dynamic range	0 to $0.42f_s$	110
Gain	DC	3.87

High-pass filter

An optional high-pass filter is provided to remove unwanted DC components. The operation is selected when HPEN is HIGH. The filter has the characteristics given in Table 2.

Table 2 High-pass filter characteristics.

ITEM	CONDITION	VALUE (dB)
Pass band ripple		none
Pass band gain		0
Droop	at $0.00045f_s$	0.029
Attenuation at DC	at $0.00000036f_s$	>40
Dynamic range	0 to $0.45f_s$	116

Serial interface

The serial interface provides 2 formats in both master and slave modes (see Figs 3 and 4). In both modes the interface provides up to 18 significant bits of output data per channel.

During standby mode ($\overline{STD}$ = LOW) all interface pins are in their high-impedance state. On recovery from standby the serial data output SDO is held LOW until valid data is available from the decimation filter. This time depends on whether the high-pass filter is selected or not as follows:

HPEN = 0; $T = 1024/f_s$, T = 21.3 ms when f_s = 48 kHz

HPEN = 1; $T = 8192/f_s$, T = 170.6 ms when f_s = 48 kHz

Overload Detection Indication (OVLD)

The OVLD output is used to indicate whenever the data, in either the left or right channel, is within 1 dB of the maximum possible digital swing. When this condition is detected the OVLD output is forced HIGH for at least $512f_s$ cycles (10.6 ms at f_s = 48 kHz). This time-out is reset for each infringement.

Standby mode ($\overline{STD}$)

The $\overline{STD}$ pin activates a power saving mode when the device function is not required. This pin can also be used as a chip enable, as follows.

On a HIGH-to-LOW transition, of the $\overline{STD}$ pin, the internal control circuitry starts a timed power-down sequence. This takes approximately 32 system clock cycles to complete. Transitions on $\overline{STD}$ which are shorter than 32 clock cycles have an indeterminate effect. However, the device will always recover correctly.

During standby the following occurs:

- The internal logic clock is disabled
- The serial interface pins are forced to high impedance
- The OVLD output is forced LOW
- The analog circuitry is disabled
- The nominal external analog node voltages are maintained by a low-power circuit. This feature ensures a fast recovery from standby mode.

On a LOW-to-HIGH transition the device reverts back to its normal function. This process takes approximately 32 system clock cycles. Before SDO is enabled the output data is forced LOW. SDO remains LOW until good data is available from the decimation filter.

The $\overline{STD}$ pin has a Schmitt-trigger input. A simple power-on reset function can be effected using an external capacitor to V_{SSD} and resistor to V_{DDD}.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage	note 1	−0.5	+6.5	V
V_I	DC input voltage		−0.5	+6.5	V
I_{IK}	DC input diode current		–	±20	mA
V_O	DC output voltage		−0.5	V_{DD} + 0.5	V
I_O	DC output source or sink current		–	±20	mA
I_{DDtot}	total DC supply current		–	±0.5	A
I_{SStot}	total DC supply current		–	±0.5	A
T_{amb}	operating ambient temperature		−40	+85	°C
T_{stg}	storage temperature		−65	+150	°C
V_{es1}	electrostatic handling	note 2	−2000	+2000	V
V_{es2}	electrostatic handling	note 3	−200	+200	V

Notes

1. V_{SSD} and V_{SSA} pins must be externally connected to a common potential.
2. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor with a rise time of 15 ns.
3. Equivalent to discharging a 200 pF capacitor via a 2.5 μH series inductor.

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS

V_{DDD} = 3.4 to 5.5 V; V_{DDA} = 4.5 to 5.5 V; T_{amb} = −40 to +85 °C; f_s = 18 to 53 kHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
I_{DDA}	analog supply current	f_s = 48 kHz	–	13	–	mA
V_{DDD}	digital supply voltage		3.4	5.0	5.5	V
I_{DDD}	digital supply current	f_s = 48 kHz	–	56	–	mA
P_{tot}	total power consumption	f_s = 48 kHz	–	345	–	mW

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{STD}	standby supply current		–	65	–	μA
P_{STD}	standby power consumption		–	325	–	μW
Digital part: inputs						
SFOR, SLAVE AND HPEN						
V_{IL}	LOW level input voltage	note 1	−0.5	–	+0.8	V
V_{IH}	HIGH level input voltage	note 1	2.0	–	V_{DDD} + 0.5	V
I_{LI}	input leakage current	note 2	−10	–	+10	μA
C_I	input capacitance		–	–	10	pF
CLKIN						
V_{IL}	LOW level input voltage		−0.5	–	$+0.3V_{DDD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DDD}$	–	V_{DDD} + 0.5	V
I_{LI}	input leakage current	note 2	−10	–	+10	μA
C_I	input capacitance		–	–	10	pF
$\overline{STD}$ (SCHMITT-TRIGGER)						
V_{IL}	LOW level input voltage	note 1	−0.5	–	$+0.4V_{DDD}$	V
V_{IH}	HIGH level input voltage	note 1	2.4	–	V_{DDD} + 0.5	V
ΔV_I	input hysteresis		–	600	–	mV
I_{LI}	input leakage current	note 2	−10	–	+10	μA
C_I	input capacitance		–	–	10	pF
Digital part: Input/Outputs						
SWS AND SCK						
V_{IL}	LOW level input voltage	note 1	−0.5	–	+0.8	V
V_{IH}	HIGH level input voltage	note 1	2.0	–	V_{DDD} + 0.5	V
I_{LI}	leakage current in 3-state	note 2	−10	–	+10	μA
C_I	input capacitance		–	–	10	pF
V_{OL}	LOW level output voltage	I_O = −400 μA; note 1	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_O = 20 μA; note 1	2.4	–	–	V
C_L	output load capacitance		–	–	50	pF
Digital part: Outputs						
OVLD						
V_{OL}	LOW level output voltage	I_O = −400 μA; note 1	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_O = 20 μA; note 1	2.4	–	–	V
C_L	output load capacitance		–	–	50	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SDO						
V_{OL}	LOW level output voltage	I_O = –400 μA; note 1	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_O = 20 μA; note 1	2.4	–	–	V
I_{LI}	leakage current in 3-state	note 2	–10	–	+10	μA
C_L	output load capacitance		–	–	50	pF
Digital part: timing						
CKIN						
t_r	clock input rise time		–	–	10	ns
t_f	clock input fall time		–	–	10	ns
f_i	clock input frequency	note 3	4.608	12.288	13.568	MHz
msr	mark-to-space ratio	f_s > 32 kHz	40	–	60	%
		$f_s \leq$ 32 kHz	30	–	70	%
Serial interface master and slave modes (see Figs 5, 6 and 7)						
SCK						
t_r	clock rise time	note 4	–	–	50	ns
t_f	clock fall time	note 4	–	–	50	ns
t_L	clock LOW time	T = 1/64f_s	0.40T	–	0.60T	
t_H	clock HIGH time	T = 1/64f_s	0.40T	–	0.60T	
f_{clk}	clock frequency	master mode	64f_s	64f_s	64f_s	
		slave mode	–	–	64f_s	
t_{idle}	burst clock idle time	slave mode; T = 1/f_s	0	–	0.05T	
SWS						
t_r	word select rise time	note 4	–	–	50	ns
t_f	word select fall time	note 4	–	–	50	ns
t_{wL}	word select LOW time	T = 1/f_s	0.45T	0.50T	0.55T	
t_{wH}	word select HIGH time	T = 1/f_s	0.45T	0.50T	0.55T	
f_{wc}	word select frequency		1f_s	1f_s	1f_s	
t_d	word select delay from SCK	master mode	–50	–	+50	ns
t_d	word select delay from SCK	slave mode	50	–	–	ns
t_{su}	word select set-up time to SCK	slave mode	150	–	–	ns
SDO						
t_h	data output hold time		100	–	–	ns
t_{su}	data output set-up time		100	–	–	ns
t_r	data output rise time	note 4	–	–	50	ns
t_f	data output fall time	note 4	–	–	50	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog part (V_{DDD} = V_{DDA} = 5 V; T_{amb} = 25 °C; f_s = 48 kHz)						
VOLTAGE REFERENCE: V_{REFL} AND V_{REFR}						
V_O	output voltage		$0.475V_{DDA}$	$0.5V_{DDA}$	$0.525V_{DDA}$	V
Z_n	DC impedance	normal mode	–	750	–	Ω
Z_s	DC impedance	standby mode	–	100	–	kΩ
CURRENT REFERENCE: I_{REF}						
V_O	output voltage		–	$0.5V_{DDA}$	–	V
I_O	output current	R = 33 kΩ	–	76	–	μA
DAC REFERENCE: V_{DACN}						
V_I	input voltage		–	V_{SSA}	–	V
V_{DACP}						
V_I	input voltage		–	V_{DDA}	–	V
BUFFER OPERATIONAL AMPLIFIERS: BIL, BOL, BIR AND BOR						
V_{offset}	input offset voltage		–	< ±10	–	mV
R_{Lmax}	maximum load resistance; (drive capability)	decoupled to V_{REF}	–	10	–	kΩ
Z_O	output impedance		–	100	–	Ω
THD + N	total harmonic distortion plus noise	f = 0 to 20 kHz	–	–85	–	dB
ADC PERFORMANCE; NOTE 5						
t_{gd}	group delay	$T = 1/f_s$	tbf	–	tbf	μs
α_{sb}	stop band attenuation	$f > 0.546f_s$	60	–	–	dB
DR	dynamic range	note 6	90	–	–	dB
THD + N	total harmonic distortion plus noise	note 7	–	–	–80	dB
S/N	signal-to-noise ratio	A-weighted	–	tbf	–	dB
α_{cs}	channel separation	note 8	–	tbf	–	dB
G	gain	note 9	–1.2	–1	–0.8	dB

Notes

1. Minimum V_{IL}, V_{OL} and maximum V_{IH}, V_{OH} are peak values to allow for transients.
2. I_{LImin} and I_{LOmin} measured at V_I = 0 V; I_{LImax} and I_{LOmax} measured at $V_I = V_{DDD}$.
3. f_i is a multiple (×256) of the system sampling frequency (f_s) which can vary between 18 kHz and 53 kHz.
4. C_L = 50 pF (valid for master mode only).
5. Device measured with external components shown in recommended application diagram Fig.8.
6. Input is 1 kHz and –60 dB.
7. Input is 1 kHz and 0 dB.
8. Measured by applying a 1 kHz, 0 dB signal to one channel and monitoring the level of 1 kHz (fundamental) on the other channel.
9. See also Section "Input level" of Chapter "Functional description"; valid for left or right channel.

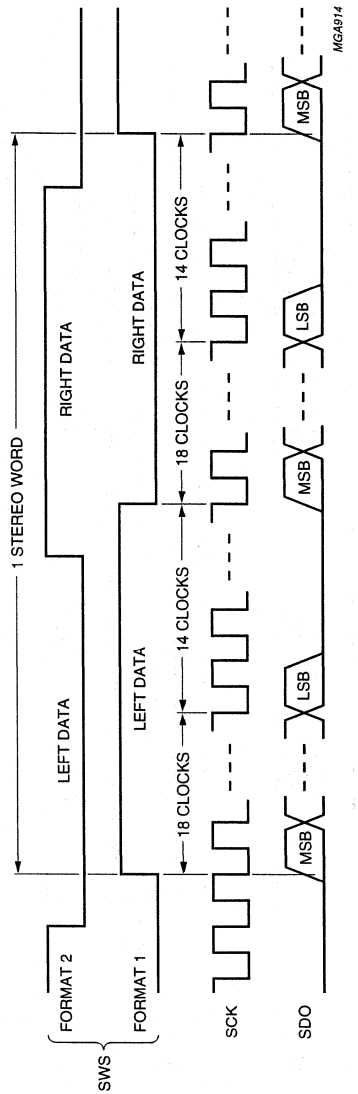


Fig.3 Serial interface master mode format.

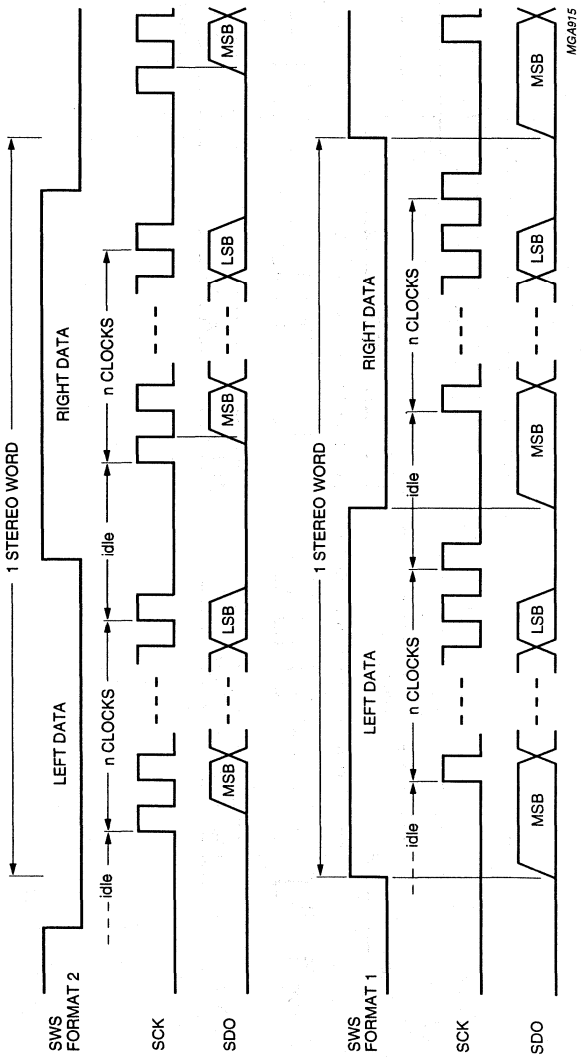


Fig.4 Serial interface slave mode formats.

1 < n < 33.
Up to 18 significant bits are available.

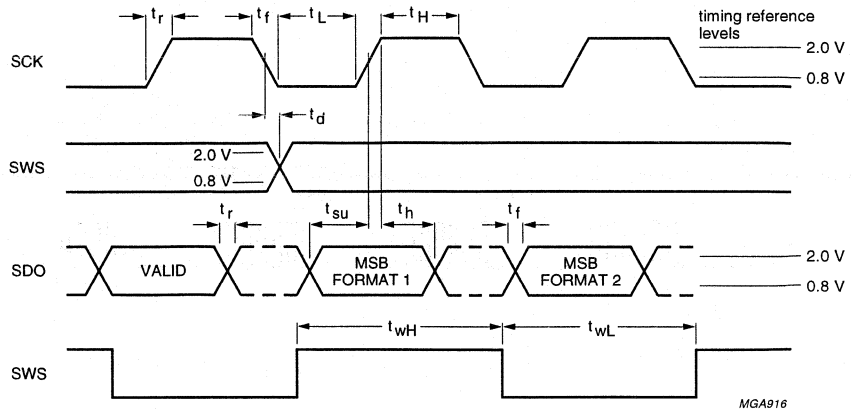


Fig.5 Serial interface master mode timing.

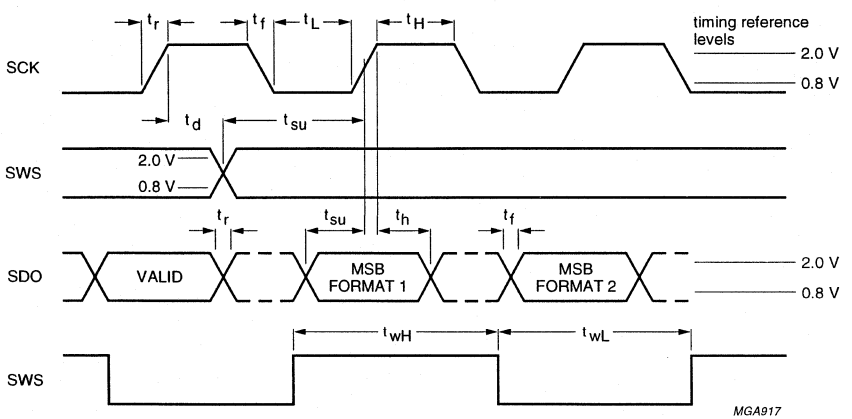


Fig.6 Serial interface slave mode timing.

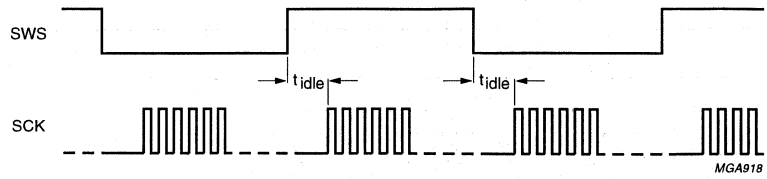


Fig.7 Serial interface slave mode burst clock.

APPLICATION INFORMATION

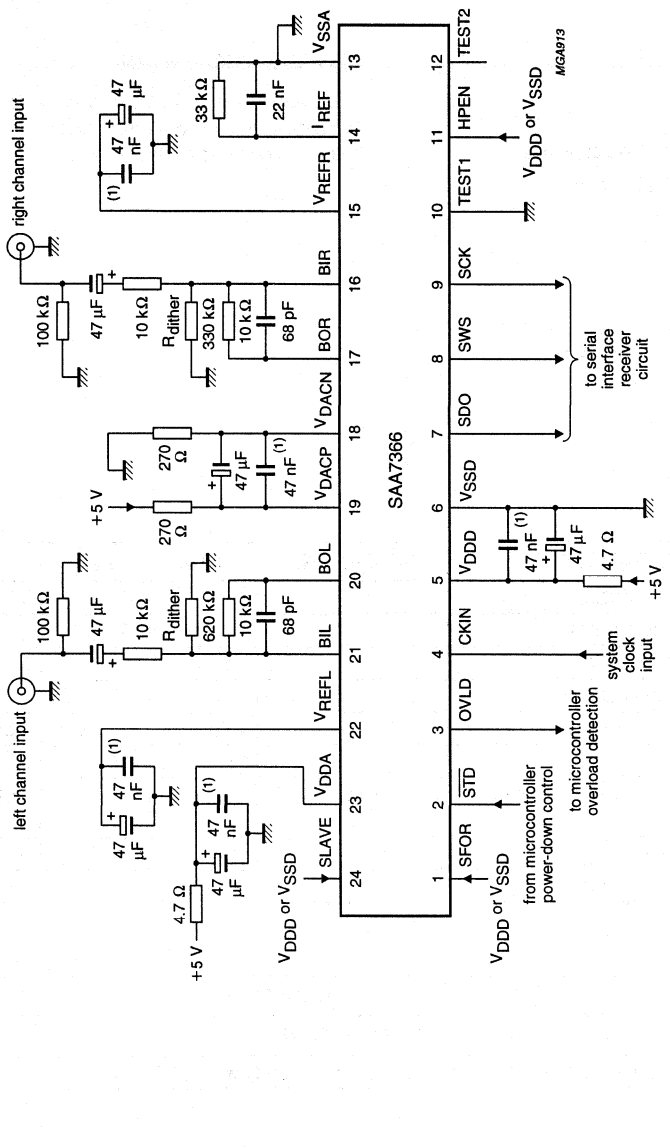


Fig.8 Application circuit.

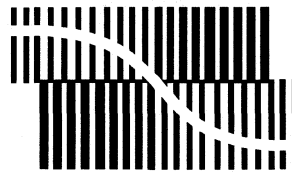
(1) These capacitors should preferably be surface mounted components located as close as possible to the device pins.

Bitstream conversion ADC for digital audio systems

SAA7367

FEATURES

- Total Harmonic Distortion plus Noise (THD + N) = −88 dB (0.004%); DR = 93 dB; S/N = 97 dB
- Simple interfacing to analog inputs
- Small, non-critical PCB layout
- Low pin-out SO24 package (pin-compatible to SAA7366)
- 4 flexible serial interface modes
- 4.5 to 5.5 V operation
- Standby mode
- Detection of digital signal ≥−1 dB amplitude
- Up to 18 significant bits serial output
- Selectable high-pass filter.



BITSTREAM CONVERSION

GENERAL DESCRIPTION

The SAA7367 is a CMOS low-cost stereo Analog-to-Digital Converter (ADC) using the Philips bitstream conversion technique.

APPLICATIONS

The device is designed for the digital acquisition of analog audio signals for digital audio systems such as:

- Compact Disc-Recordable (CD-R)
- Digital Compact Cassette (DCC)
- Digital Audio Tape (DAT).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
I_{DDD}	digital supply current		–	17	–	mA
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
I_{DDA}	analog supply current		–	13	–	mA
f_{BCK}	clock input frequency		4.60	12.288	12.8	MHz
f_s	sample rate		18	48	50	kHz
THD + N	total harmonic distortion plus noise	at 0 dB input	–	−88	−80	dB
DR	dynamic range	at −60 dB	90	93	–	dB
S/N	signal-to-noise ratio		–	97	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7367	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1

BLOCK DIAGRAM

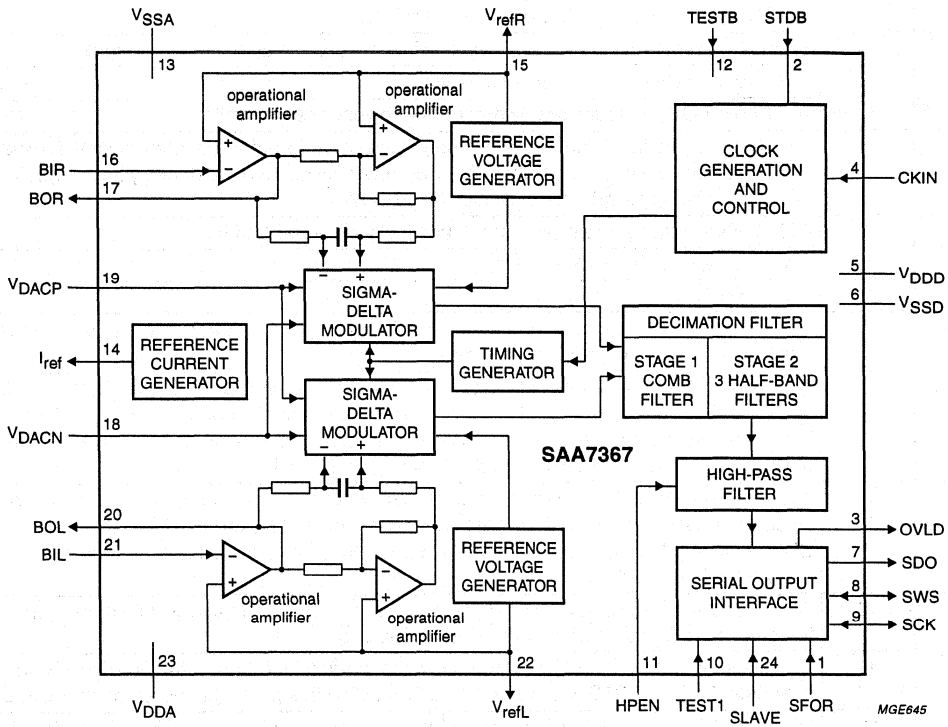


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SFOR	1	TTL level input; in normal mode this input selects the serial interface output format; output format is selected as follows: SFOR = HIGH selects Format 1 SFOR = LOW selects Format 2 (similar to I^2S)
STDB	2	schmitt-trigger input; in normal mode, this input is used to select standby mode:
		STDB = HIGH selects normal operation
		STDB = LOW selects standby mode (low power consumption)
OVLD	3	TTL level output; in normal mode this output indicates whether the internal digital signal is within 1 dB of maximum; if so, the output will go HIGH for 131072 clock cycles (approximately 11 ms); in standby mode this output is forced LOW
CKIN	4	CMOS level input; system clock input; nominally clocked at $256f_s$
V_{DDD}	5	digital supply voltage (4.5 to 5.5 V)
V_{SSD}	6	digital ground
SDO	7	TTL level output (3-state); in normal mode this pin outputs data from the serial interface; in standby mode, this output is high impedance
SWS	8	TTL level input/output; serial interface word select signal; in master mode (SLAVE = LOW), this pin outputs the serial interface word select signal; in slave mode (SLAVE = HIGH), this pin is the word select input to the serial interface; in standby mode (STDB = LOW) this pin is always an input (high impedance); for polarity: see Table 1
SCK	9	TTL level input/output; in master mode (SLAVE = LOW) the pin outputs the serial interface bit clock; in slave mode (SLAVE = HIGH) this pin is the input for the external bit clock; data on SDO is clocked out on the HIGH-to-LOW transition of SCK; the data is valid on the LOW-to-HIGH transition
TEST1	10	Test 1; TTL level input with internal pull-down; in slave mode (slave = HIGH), this pin is used to select extra serial interface formats (see Table 2)
HPEN	11	TTL level input; this input is used to enable the internal high-pass filter when HIGH; in scan-test mode (TESTB = LOW and TEST1 = LOW) this pin functions as 'scan chain c' input
TESTB	12	Test B; CMOS level input with internal pull-up; in normal applications, this input should be left HIGH
V_{SSA}	13	analog ground; this pin is internally connected to V_{SS} via the on-chip substrate contacts
I_{ref}	14	current reference generator output; 33 kΩ in parallel with 22 nF is connected from this pin to V_{SSA}
V_{refR}	15	right channel analog reference output voltage ($\frac{1}{2}V_{DDA}$)
BIR	16	buffer operational amplifier inverting input for right channel
BOR	17	buffer operational amplifier output for right channel
V_{DACN}	18	negative 1-bit DAC reference voltage input, connected to 0 V
V_{DACP}	19	positive 1-bit DAC reference voltage input, connected to +5 V
BOL	20	buffer operational amplifier output for left channel
BIL	21	buffer operational amplifier inverting input for left channel
V_{refL}	22	left channel analog reference output voltage ($\frac{1}{2}V_{DDA}$)
V_{DDA}	23	analog supply voltage (4.5 to 5.5 V)

SYMBOL	PIN	DESCRIPTION
SLAVE	24	TTL level input; used to select the serial interface operating mode: SLAVE = HIGH selects slave mode SLAVE = LOW selects master mode

Table 1 SWS polarity

CONDITIONS			POLARITY
SLAVE AND TEST1	SWS	SFOR	
SLAVE = LOW or TEST1 = LOW	LOW	LOW	left data
	LOW	HIGH	right data
SLAVE = HIGH and TEST1 = HIGH	LOW	LOW	right data
	LOW	HIGH	left data

Table 2 Selection of serial interface formats via TEST1

CONDITIONS		SELECTED FORMAT
SFOR	TEST1	
HIGH	LOW	format 1
	HIGH	format 2
LOW	LOW	format 3
	HIGH	format 4

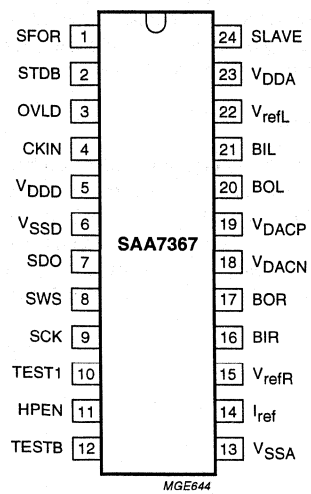


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

General

The SAA7367 is a bitstream conversion CMOS ADC for digital audio systems. The conversion is achieved using a third-order Sigma-Delta Modulator (SDM), running at 128 times the output sample frequency (f_s). The high oversampling ratio greatly simplifies the design of the analog input anti-alias filter. In most events, the internal buffer operational amplifier, configured as a low-pass filter, will suffice. The 1-bit code from the SDM is filtered and down-sampled (decimated) to $1f_s$ by Finite Impulse Response (FIR) filters. An optional I^2R high-pass filter is provided to remove DC, if required. The device has been designed with ease of use, low board area and low application costs in mind.

Clock frequency

The external clock input on pin CKIN runs at $256f_s$, which can range from 18 to 50 kHz.

Input buffer

Two input buffers are provided, one for each channel, for signal amplitude matching, signal buffering and anti-alias filter purposes. These are configured for inverting use. Access is provided by pins BIL, BIR (inverting inputs) and BOL, BOR (outputs), for left and right channels respectively. By the choice of feedback component values, the application signal amplitude can be matched to the requirements of the ADC.

Typically, the operational amplifiers are configured as low-pass filters with a gain of 1 and a pole at approximately $5f_s$.

Remark: the complete ADC is non-inverting. Hence, a positive DC input (referenced to V_{ref}) will yield a positive digital output.

Input level

The overall system gain is proportional V_{DDA}, or more accurately the potential difference between the DAC reference voltages (V_{VDACP}) and (V_{VDACN}). For convenience, the ADC input signal amplitude is defined as that amplitude seen on BOL or BOR, the operational amplifier outputs (i.e. the input to the SDM). Also, the 0 dB input level is defined as that which gives a –1 dB (actually –1.12 dB) digital output, relative to full-scale swing. This reduced gain provides headroom to accommodate small random DC offsets, without causing the digital output to clip.

Hence:

$$V_I(0\ dB) = \frac{(V_{VDACP} - V_{VDACN})}{5\ V\ (RMS)}$$

The user of the IC should ensure that, when all sources of signal amplitude variation are taken into account, the maximum input signal should conform to the 0 dB level. In the event that the maximum signal level cannot be pre-determined, e.g. live microphone input, the average signal level should be set at –10 to –20 dB down. The exact value will depend on the application and the balance between headroom and operating Signal-to-Noise Ratio (SNR).

Behaviour during overload

As previously defined, the maximum input level for normal operation is 0 dB. If the input level exceeds this value, clipping may occur. Within the system, excessive amplitudes are detected after the high-pass filter. Infringements are limited to the maximum permitted positive or negative values $2^{17} - 1$ or -2^{17} respectively.

Input signals in the range 0 to 1 dB may or may not be clipped, depending on the values of DC dither and small random offsets in the analog circuitry.

When using the recommended application circuitry, clipping will initially be observed on negative peaks, due to the use of negative DC dither.

The maximum level of overload that can be safely tolerated is application circuit dependent. In the case of the recommended circuit, the following applies: the inverting operational amplifier inputs BIL and BIR are protected from excessive voltages (currents) by diodes to V_{DDA} and V_{SSA}. These have absolute maximum ratings of $I_d = \pm 20$ mA, with a safe practical limit of ±2 mA.

Given the input resistor of 10 kΩ, ±2 mA diode current and the operation of the operational amplifier, a maximum signal (applied to the input resistor) of ±30 V can be handled safely. This level represents an overload of 26 dB.

During overload, the in-band portion of the waveform will be correctly converted. The out-of-band portion will be limited as previously detailed.

Sigma-Delta Modulator (SDM)

The SAA7367 uses two third-order SDMs with a quantization noise floor of approximately –104 dB. The scaling of the feedback has been optimized for stable operation, even during overload. Thus, with a maximum signal swing of 0 V to V_{DDA} on the input, the digital output remains well-behaved, i.e. it does not burst into random oscillation. During overload, the output is simply a clipped version of the input. The gain of this stage is –4.64 dB.

Decimation filter

Decimation from $128f_s$ is performed in two stages. The first stage, a comb filter, uses 64 symmetrical coefficients to implement a 3rd $\sin x/x$ characteristic. This filter decimates from 128 to $8f_s$. The second stage, an FIR filter, consists of three half-band filters, each decimating by a factor of 2. The overall characteristics are given in Table 3.

Table 3 Overall filter characteristics

ITEM	CONDITION	VALUE (dB)
Pass band ripple	0 to $0.45f_s$	±0.1
	0.45 to $0.47f_s$	−0.5
Stop band	$>0.55f_s$	−60
Dynamic range	0 to $0.42f_s$	110
Gain	DC	3.52

High-pass filter

An optional I^2R high-pass filter is provided to remove unwanted DC components. The operation is selected when HPEN is HIGH and deselected when LOW. The filter has the characteristics given in Table 4.

Table 4 High-pass filter characteristics

ITEM	CONDITION	VALUE (dB)
Pass band ripple		none
Pass band gain		0
Droop	at $0.00042f_s$	0.146
Attenuation at DC	at $0.00000036f_s$	>40
Dynamic range	0 to $0.45f_s$	>110

Serial interface

The serial interface provides 2 formats in master mode and 4 in slave mode (see Figs 3 and 4). Format 2 is similar to Philips I^2S. In all modes, the interface provides up to 18 significant bits of output data per channel. During standby mode (STDB = LOW), all interface pins are in their high impedance state. On recovery from standby, the serial data output SDO is held LOW until valid data is available from the decimation filter. This time depends on whether the high-pass filter is selected:

HPEN = 0; $T = 1024/f_s$, T = 21.3 ms when f_s = 48 kHz

HPEN = 1; $T = 12288/f_s$, T = 256.0 ms when f_s = 48 kHz

Overload detection

The OVLD output is used to indicate when the output data, in either the left or right channel, is greater than −1 dB (actual figure −1.023 dB) of the maximum possible digital swing. When this condition is detected, the OVLD output is forced HIGH for at least $512f_s$ cycles (10.6 ms at f_s = 48 kHz). This time-out is reset for each infringement.

Standby mode

The STDB pin activates a power saving mode when the device function is not required. This pin can also be used as a chip enable.

On a HIGH-to-LOW transition of the STDB pin, the internal control circuitry starts a timed power-down sequence. This takes approximately 32 system clock cycles to complete. Transitions on STDB that are shorter than 32 clock cycles may have an indeterminate effect. However, the device will always recover correctly.

During standby, the following occurs:

- The internal logic clock is disabled
- The serial interface pins are forced to high impedance
- The OVLD output is forced LOW
- The analog circuitry is disabled
- The nominal external analog node voltages are maintained by a low-power circuit. This feature ensures a fast recovery from standby mode.

Note: since the serial interface pins are high impedance during standby, these pins could be wire-ORed with other serial interface ICs.

On a LOW-to-HIGH transition, the device reverts back to normal operation. This process takes approximately 256 system clock cycles. Before SDO is enabled, the output data is forced LOW. SDO remains LOW until good data is available from the decimation filter (see Section "Serial interface").

The STDB pin has a Schmitt-trigger input. A simple power-on-reset function can be effected using an external capacitor to V_{SS} and resistor to V_{DD}.

TEST1

This pin is used to select the serial interface format in slave mode.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage (note 1)	−0.5	+6.5	V
V_I	DC input voltage	−0.5	+6.5	V
I_{IK}	DC input clamp diode current	−	±20	mA
V_O	DC output voltage	−0.5	V_{DD} + 0.5	V
I_O	DC output source or sink current	−	±20	mA
$I_{DD(tot)}$	total DC supply current	−	±0.5	A
I_{SStot}	total DC supply current	−	±0.5	A
T_{amb}	operating ambient temperature	−40	+85	°C
T_{stg}	storage temperature	−65	+150	°C

Note

1. V_{SSD} and V_{SSA} must be connected to a common potential.

QUALITY SPECIFICATION

In accordance with *"SNW-FQ-611-E"*. The number of the quality specification can be found in the *"Quality Reference Handbook"*. The handbook can be ordered using the code 9397 750 00192.

CHARACTERISTICS

V_{DDD} = 4.5 to 5.5 V; V_{DDA} = 4.5 to 5.5 V; f_s = 18 to 50 kHz; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDD}	digital supply voltage		4.5	5	5.5	V
I_{DDD}	digital supply current	f_s = 48 kHz	−	17	−	mA
V_{DDA}	analog supply voltage		4.5	5	5.5	V
I_{DDA}	analog supply current		−	13	−	mA
P_{tot}	total power dissipation	f_s = 48 kHz	−	150	−	mW
I_{stb}	standby supply current		−	160	−	µA
P_{stb}	standby power consumption		−	800	−	µW
Digital part: inputs						
SFOR, SLAVE AND HPEN						
V_{IL}	LOW level input voltage		−0.5	−	+0.8	V
V_{IH}	HIGH level input voltage		2.0	−	V_{DD} + 0.5	V
I_{LI}	input leakage current		−10	−	+10	µA
C_i	input capacitance		−	−	10	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CKIN						
V_{IL}	LOW level input voltage		−0.5	−	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	−	V_{DD} + 0.5	V
I_{LI}	input leakage current		−10	−	+10	μA
C_i	input capacitance		−	−	10	pF
TEST1						
V_{IL}	LOW level input voltage		−0.5	−	+0.8	V
V_{IH}	HIGH level input voltage		2.0	−	V_{DD} + 0.5	V
R_i	internal resistance to V_{SS}		−	50	−	kΩ
C_i	input capacitance		−	−	10	pF
TESTB						
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	−	V_{DD} + 0.5	V
R_i	internal resistance to V_{DD}		−	50	−	kΩ
STDB (SCHMITT TRIGGER)						
V_{IL}	LOW level input voltage		−0.5	−	$0.4V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.6V_{DD}$	−	V_{DD} + 0.5	V
V_{hys}	hysteresis voltage		200	−	−	mV
I_{LI}	input leakage current		−10	−	+10	μA
C_i	input capacitance		−	−	10	pF
Digital part: inputs/outputs						
SWS AND SCK						
V_{IL}	LOW level input voltage		−0.5	−	+0.8	V
V_{IH}	HIGH level input voltage		2.0		V_{DD} + 0.5	V
I_{LI}	3-state leakage current		−10	−	+10	μA
C_i	input capacitance		−	−	10	pF
V_{OL}	LOW level output voltage	I_O = −400 μA	−	−	0.4	V
V_{OH}	HIGH level output voltage	I_O = 20 μA	2.4	−	−	V
C_L	output load capacitance	note 1	−	−	50	pF
Digital part: outputs						
OVLD						
V_{OL}	LOW level output voltage	I_O = −400 μA	−	−	0.4	V
V_{OH}	HIGH level output voltage	I_O = 20 μA	2.4	−	−	V
C_L	output load capacitance	note 1	−	−	50	pF
SDO						
V_{OL}	LOW level output voltage	I_O = −400 μA	−	−	0.4	V
V_{OH}	HIGH level output voltage	I_O = 20 μA	2.4	−	−	V
I_{LI}	3-state leakage current		−10	−	+10	μA
C_L	output load capacitance	note 1	−	−	50	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital part: timings						
CKIN						
t_r	input rise time		–	–	10	ns
t_f	input fall time		–	–	10	ns
f_i	input frequency		4.60	–	12.8	MHz
msr	mark-to-space ratio	$f_s > 32$ kHz	40	–	60	%
		$f_s \leq 32$ kHz	30	–	70	%
Serial Interface master and slave modes (see Figs 5 and 6)						
SCK						
t_r	rise time	$C_L = 50$ pF; note 1	–	–	50	ns
t_f	fall time	$C_L = 50$ pF; note 1	–	–	50	ns
t_L	LOW time	$T = 1/64 f_s$	0.4T	–	0.6T	ns
t_H	HIGH time	$T = 1/64 f_s$	0.4T	–	0.6T	ns
f_{clk}	clock frequency	master mode	$64f_s$	$64f_s$	$64f_s$	MHz
		slave mode	–	–	$64f_s$	MHz
t_{idle}	burst clock idle time	slave mode; $T = 1/f_s$	0	–	0.5T	ns
SWS						
t_r	rise time	$C_L = 50$ pF; note 1	–	–	50	ns
t_f	fall time	$C_L = 50$ pF; note 1	–	–	50	ns
t_L	LOW time	$T = 1/f_s$	0.05T	0.5T	0.95T	ns
t_H	HIGH time	$T = 1/f_s$	0.05T	0.5T	0.95T	ns
f_S	frequency		$1f_s$	$1f_s$	$1f_s$	MHz
t_d	delay from SCK	master mode	–50	–	+50	ns
		slave mode	50	–		ns
t_{su}	set-up time to SCK	slave mode	150	–	–	ns
SDO						
t_h	data output hold time		100	–	–	ns
t_{su}	data output set-up time		50	–	–	ns
t_r	data output rise time	$C_L = 50$ pF; note 1	–	–	50	ns
t_f	data output fall time	$C_L = 50$ pF; note 1	–	–	50	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog part at: $V_{DD} = V_{DDA} = 5$ V; $T_{amb} = 25$ °C						
V_{refL} AND V_{refR}						
V_O	output voltage		$0.475V_{DDA}$	$0.5V_{DDA}$	$0.525V_{DDA}$	V
R_{DC}	DC impedance	normal mode	–	1.3	–	kΩ
		standby mode	–	100	–	kΩ
CURRENT REFERENCE: I_{ref}						
V_O	out put voltage		–	$0.5V_{DDA}$	–	V
I_O	output current	R = 33 kΩ	–	76	–	μA
V_{DACN}						
V_I	input voltage		–	V_{SS}	–	V
V_{DACP}						
V_I	input voltage		–	V_{DDA}	–	V
BUFFER OPERATIONAL AMPLIFIERS: BIL, BOL, BIR AND BOR						
$V_{I(off)}$	input offset voltage		–	<10	–	mV
R_L	load resistance; (drive capability)	decoupled to V_{ref}	–	10	–	kΩ
Z_O	output impedance		–	100	–	Ω
THD + N	total harmonic distortion plus noise	f = 0 to 20 kHz	–	–87	–	dB
OVERALL PERFORMANCE (ANALOG IN, DIGITAL OUT)						
t_{gd}	group delay time	$T = 1/f_s$	–	25T	–	s
α_{sb}	stop band attenuation	$f > 0.546\ f_s$	60	–	–	dB
DR	dynamic range	0 to 20 kHz	90	93	–	dB
THD + N	total harmonic distortion plus noise	0 to 20 kHz	–	–88	–80	dB
S/N	signal-to-noise ratio	A-weighted	–	97	–	dB
α_{cs}	channel separation		–	92	–	dB
G	gain	note 2	–1.4	–1	–0.8	dB

Notes

1. Load capacitance is valid for master mode only.
2. See also Section "Input level" of Chapter "Functional description"; valid for left or right channel.

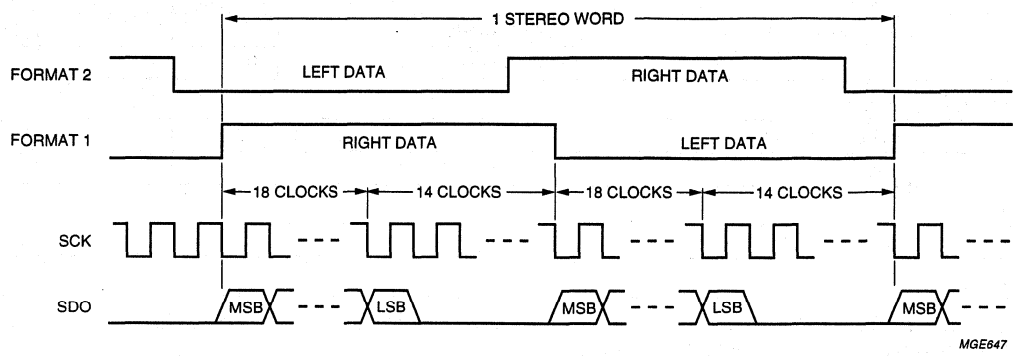


Fig.3 Serial interface master mode format.

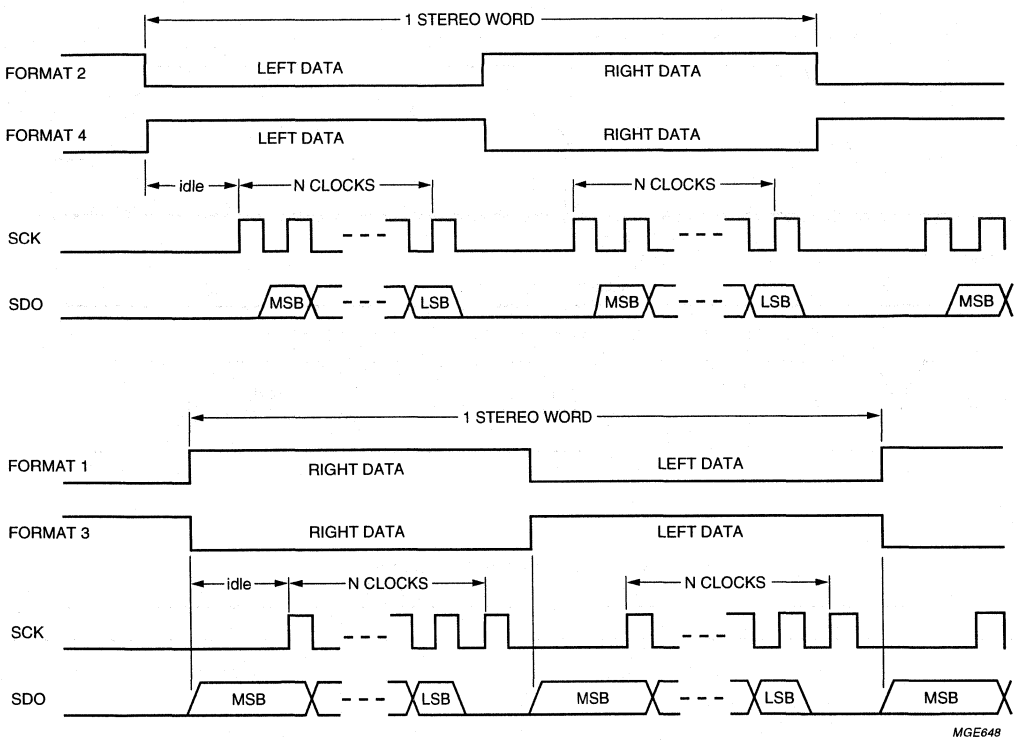


Fig.4 Serial interface slave mode format.

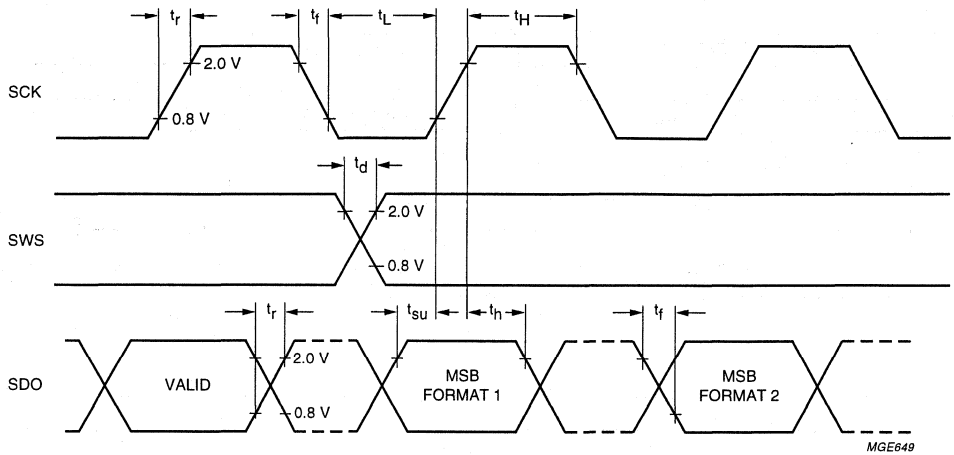


Fig.5 Serial interface master mode timing.

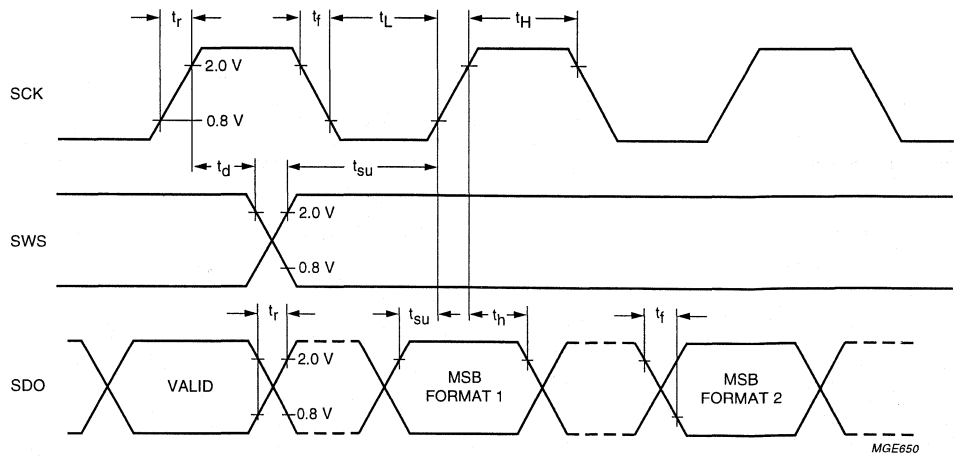
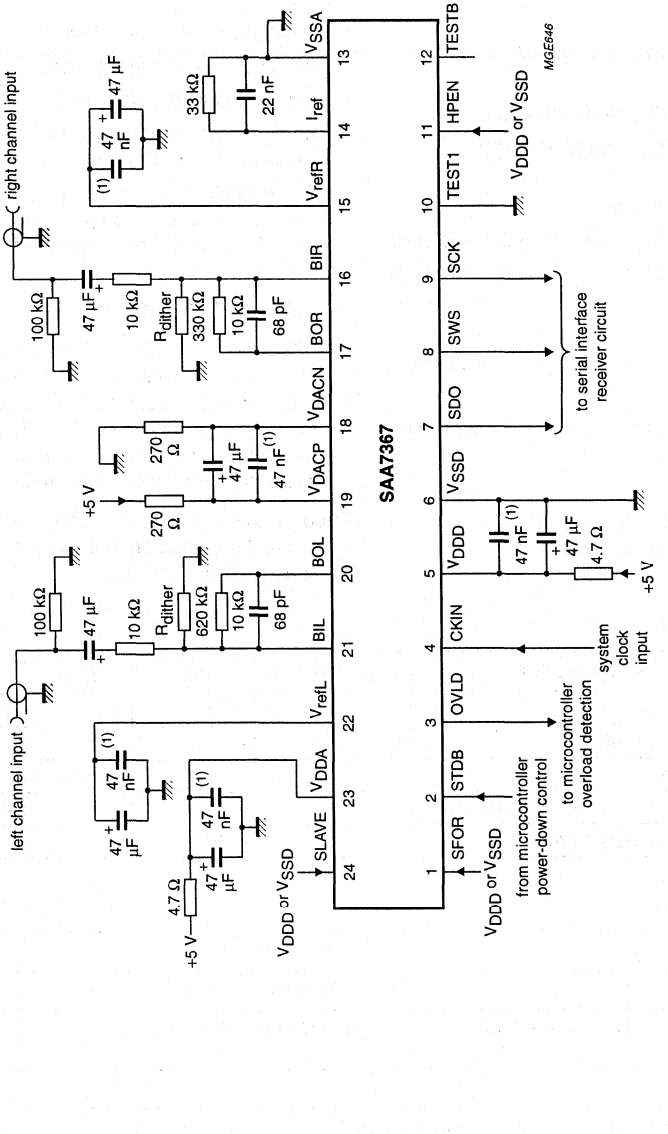


Fig.6 Serial interface slave mode timing.

APPLICATION INFORMATION



(1) These capacitors should preferably be surface-mounted components located as close as possible to the device pins.

Fig.7 Application circuit.

Digital servo processor and Compact Disc decoder (CD7)

SAA7370A

FEATURES

- CD-ROM mode
- Up to 8 times-speed mode
- Lock-to-disc mode
- Full error correction strategy, t = 2 and e = 4
- Full CD graphics interface
- All standard decoder functions implemented digitally on chip
- FIFO overflow concealment for rotational shock resistance
- Digital audio interface (EBU), audio and data
- 2 and 4 times oversampling integrated digital filter, including f_s mode
- Audio data peak level detection
- Kill interface for DAC deactivation during digital silence
- All TDA1301 (DSIC2) digital servo functions, plus extra high level functions
- Low focus noise
- Improved playability on ABEX TCD-721R, TCD-725 and TCD-714 discs
- Automatic closed-loop gain control available for focus and radial loops
- Pulsed sledge support
- Up to 80 kHz (8.4672 MHz crystal) or 16 MHz (16.9344 MHz crystal) jump performance
- Electronic damping of fast radial actuator during long jump
- Microcontroller loading LOW
- High level servo control option
- High level mechanism monitor
- Communication may be via TDA1301/SAA7345 compatible bus or I²C-bus
- On-chip clock multiplier allows the use of 8.4672 MHz crystal for up to 4 times speed mode or 16.9344 MHz crystal for up to 8 times-speed mode.

GENERAL DESCRIPTION

The SAA7370A (CD7) is a single chip combining the functions of a CD decoder IC and digital servo IC. The decoder part is based on the SAA7345 (CD6) with an improved error correction strategy. The servo part is based on the TDA1301T (DSIC2) with improvements incorporated, extra features have also been added.

Supply of this Compact Disc IC does not convey an implied license under any patent right to use this IC in any Compact Disc application.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		4.75	5.0	5.25	V
I_{DD}	supply current	n = 1 mode	–	49	–	mA
f_{xtal}	crystal frequency		8	8.4672	35	MHz
T_{amb}	operating ambient temperature		0	–	+70	°C
T_{stg}	storage temperature		−55	–	+125	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7370A	QFP64	plastic quad flat package; 64 leads (lead length 1.6 mm); body 14 × 14 × 2.7 mm	SOT393-1

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATA SHEET

Digital servo processor and Compact Disc decoder (CD7)

SAA7370A

BLOCK DIAGRAM

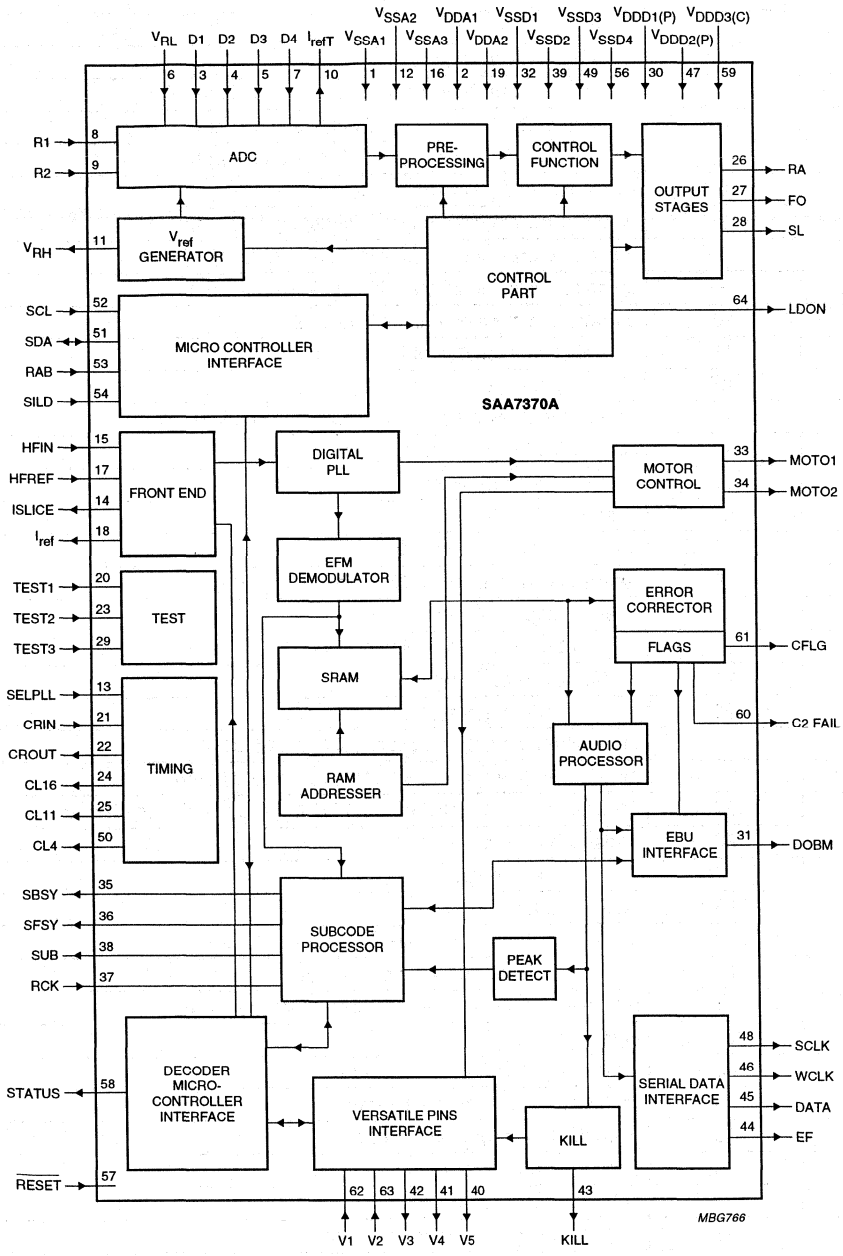


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{SSA1}	1[1]	analog ground 1
V_{DDA1}	2[1]	analog supply voltage 1
D1	3	unipolar current input (central diode signal input)
D2	4	unipolar current input (central diode signal input)
D3	5	unipolar current input (central diode signal input)
V_{RL}	6	reference voltage input for ADC
D4	7	unipolar current input (central diode signal input)
R1	8	unipolar current input (satellite diode signal input)
R2	9	unipolar current input (satellite diode signal input)
I_{refT}	10	current reference output for ADC calibration
V_{RH}	11	reference voltage output from ADC
V_{SSA2}	12[1]	analog ground 2
SELPLL	13	selects whether internal clock multiplier PLL is used
ISLICE	14	current feedback output from data slicer
HFIN	15	comparator signal input
V_{SSA3}	16[1]	analog ground 3
HFREF	17	comparator common mode input
I_{ref}	18	reference current output pin (nominally $0.5V_{DD}$)
V_{DDA2}	19[1]	analog supply voltage 2
TEST1	20	test control input 1; this pin should be tied LOW
CRIN	21	crystal/resonator input
CROUT	22	crystal/resonator output
TEST2	23	test control input 2; this pin should be tied LOW
CL16	24	16.9344 MHz (or 33.8688 MHz) system clock output
CL11	25	11.2896 or 5.6448 MHz (or 22.5792 MHz) clock output (3-state)
RA	26	radial actuator output
FO	27	focus actuator output
SL	28	sledge control output
TEST3	29	test control input 3; this pin should be tied LOW
$V_{DDD1(P)}$	30[1]	digital supply voltage 1 for periphery
DOBM	31	bi-phase mark output (externally buffered; 3-state)
V_{SSD1}	32[1]	digital ground 1
MOTO1	33	motor output 1; versatile (3-state)
MOTO2	34	motor output 2; versatile (3-state)
SBSY	35	subcode block sync output (3-state)
SFSY	36	subcode frame sync output (3-state)
RCK	37	subcode clock input
SUB	38	P-to-W subcode bits output (3-state)
V_{SSD2}	39[1]	digital ground 2
V5	40	versatile output pin 5

SYMBOL	PIN	DESCRIPTION
V4	41	versatile output pin 4
V3	42	versatile output pin 3 (open-drain)
KILL	43	kill output (programmable; open-drain)
EF	44	C2 error flag; output only defined in CD ROM modes (3-state)
DATA	45	serial data output (3-state)
WCLK	46	word clock output (3-state)
$V_{DDD2(P)}$	47[1]	digital supply voltage 2 for periphery
SCLK	48	serial bit clock output (3-state)
V_{SSD3}	49[1]	digital ground 3
CL4	50	4.2336 MHz (or 8.4672 MHz) microcontroller clock output
SDA	51	microcontroller interface data I/O line (open-drain output)
SCL	52	microcontroller interface clock line input
RAB	53	microcontroller interface R/$\overline{W}$ and load control line input (4-wire bus mode)
SILD	54	microcontroller interface $\overline{R}$/W and load control line input (4-wire-bus mode)
n.c.	55	not connected
V_{SSD4}	56[1]	digital ground 4
$\overline{RESET}$	57	power-on reset input (active LOW)
STATUS	58	servo interrupt request line/decoder status register output (open-drain)
$V_{DDD3(C)}$	59[1]	digital supply voltage 3 for core
C2FAIL	60	indication of correction failure output (open-drain)
CFLG	61	correction flag output (open-drain)
V1	62	versatile input pin 1
V2	63	versatile input pin 2
LDON	64	laser drive on output (open-drain)

Note

1. All supply pins must be connected to the same external power supply voltage.

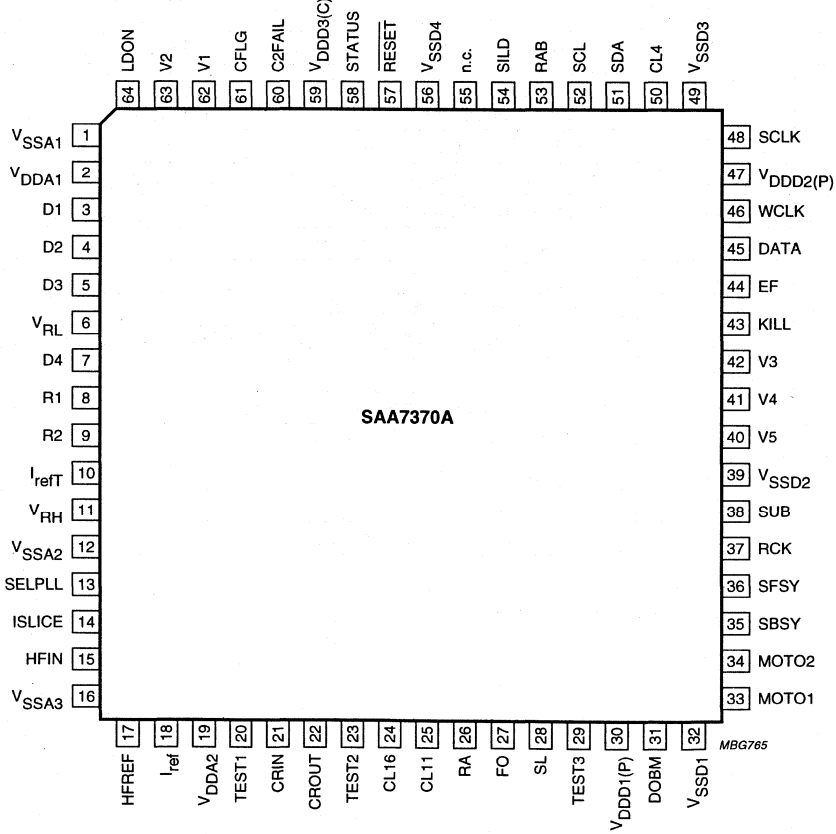


Fig.2 Pin configuration.

Error correction and host interface IC for CD-ROM (SEQUOIA)

SAA7385

FEATURES

General

- Single chip digital solution for an 8 × speed CD-ROM controller chip
- 10 Mbytes/s NCR53CF94 equivalent SCSI controller included
- High-speed 80C32 microcontroller with 256 × 8 scratch-pad SRAM included
- High performance CD-ROM interface logic
- 128 pin QFP package.

53CF94 SCSI controller

- Separate clock input to allow operation up to the maximum 10 Mbytes/s
- Fast synchronous SCSI-2 compatible
- 24-bit transfer counter for single transfers up to 16 Mbytes
- High-speed 16-bit DMA interface to the buffer manager DRAM
- On-chip 48 mA SCSI drivers
- Software compatible with members of the 53C90 family
- Allows for SCAM support.

80C32 high-speed microcontroller

- 33.87 MHz full system speed operation
- Three timers/event counters
- Programmable full duplex serial channel
- Eight general purpose microcontroller I/O pins
- External program ROM.

Front-end interface logic

- Full 8 × speed hardware operation
- Block decoder
- Sector sequencer
- CRC checking of Mode 1 and Mode 2, Form 1 sectors
- 212 ms watch-dog timer
- Sub-code interface with synchronization
- C-flag interface for absolute time stamp.

Buffer controller

- Ten level arbitration logic
- Utilizes low cost 70 ns DRAMs
- Page mode DRAM access for high-speed error correction and SCSI data transfer
- Data organization by 3 kbyte frames
- 256 kbyte or 1 Mbyte DRAM supported.

Hardware third-level error correction

- Third-level correction provides superior performance in unfavourable conditions
- Full hardware error correction to reduce microcontroller overhead
- Corrections are automatically written to the DRAM frame buffer.

Additional product support

- All control registers mapped into 80C32 special function memory space
- Dedicated S2B interface UART
- Input clock synthesizer
- Red book audio pass through.

GENERAL DESCRIPTION

The SAA7385 is a high integration ASIC that incorporates all of the digital electronics necessary to connect a CD decoder to a SCSI host. An 80C32 microcontroller and a 53CF94 SCSI controller are embedded in the ASIC. The following functions are supported:

- Input clock doubler
- Block decoder
- CRC checking of Mode 1 and Mode 2, Form 1 sectors
- Red book audio pass through to SCSI
- Buffer manager
- Third-level error correction
- Sub-code and Q-channel support
- Dedicated S2B interface UART
- Embedded 80C32 microcontroller
- Embedded 53CF94 SCSI controller.

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATA SHEET

Error correction and host interface IC for CD-ROM (SEQUOIA)

SAA7385

The SAA7385 uses a 33.8688 MHz clock and is capable of accepting data at eight times (n = 8 or 1.4 Mbytes/s) the normal CD-ROM data rate.

Third level error correction hardware is included to improve the correction efficiency of the system. The buffer manager hardware utilizes a ten-level arbitration unit and can stop the clock to the microcontroller to emulate a wait condition when necessary.

The SAA7385 comprises five major functional blocks:

- The 80C32 microcontroller is an industry standard core
- The 53CF94 is an industry standard core
- The front-end block connects to the external CD-60 based decoder and fully processes the incoming data stream to provide bytes of data that are stored in the external buffer
- The buffer manager block provides the address generation and timing control for the external DRAM buffer
- The ECC block performs the error correction functions in hardware on the data in the DRAM buffer.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	digital supply voltage	4.5	5.0	5.5	V
T_{amb}	operating ambient temperature	0	–	70	°C
T_{stg}	storage temperature	−55	–	+150	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7385GP	SQFP128	plastic quad flat package; 128 leads (lead length 1.6 mm); body 14 × 20 × 2.8 mm	SOT387-2

BLOCK DIAGRAM

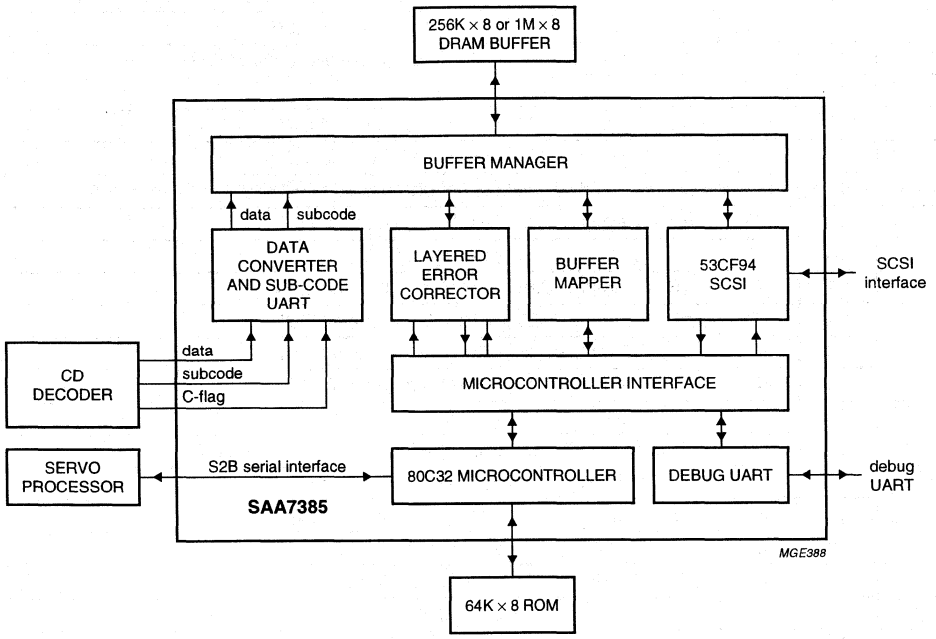


Fig.1 Block diagram (simplified).

PINNING

All input, output and bidirectional signals are TTL level unless otherwise stated (Pull-Down = PD25 = 25 μA; Pull-Up = PU25 = 25 μA, PU400 = 400 μA; Slew = S2 = 2 mA, S4 = 4 mA; CMOS slew = CMOS S2 = CMOS 2 = 2 mA; SCSI pad = SCSI = 48 mA).

SYMBOL	PIN	I/O	PAD	DESCRIPTION
DA2	1	O	S4	DRAM address bus; bit DA2
DA3	2	O	S4	DRAM address bus; bit DA3
DA4	3	O	S4	DRAM address bus; bit DA4
V_{SS1}	4	–	–	ground 1
DA5	5	O	S4	DRAM address bus; bit DA5
DA6	6	O	S4	DRAM address bus; bit DA6
DA7	7	O	S4	DRAM address bus; bit DA7
DA8	8	O	S4	DRAM address bus; bit DA8
DA9	9	O	S4	DRAM address bus; bit DA9
V_{DD1}	10	–	–	power supply 1

SYMBOL	PIN	I/O	PAD	DESCRIPTION
$\overline{RAS}$	11	O	S4	DRAM row address section; active LOW
$\overline{CAS}$	12	O	S4	DRAM column address selection; active LOW
$\overline{DWR}$	13	O	S4	DRAM write; active LOW
$\overline{DOE}$	14	O	S4	DRAM output enable; active LOW
V_{SS2}	15	–	–	ground 2
DD0	16	I/O	4 mA, Schmitt, PD25	DRAM data bus; bit DD0
DD1	17	I/O	4 mA, Schmitt, PD25	DRAM data bus; bit DD1
DD2	18	I/O	4 mA, Schmitt, PD25	DRAM data bus; bit DD2
DD3	19	I/O	4 mA, Schmitt, PD25	DRAM data bus; bit DD3
V_{DD2}	20	–	–	power supply 2
DD4	21	I/O	4 mA, Schmitt, PD25	DRAM data bus; bit DD4
DD5	22	I/O	4 mA, Schmitt, PD25	DRAM data bus; bit DD5
DD6	23	I/O	4 mA, Schmitt, PD25	DRAM data bus; bit DD6
DD7	24	I/O	4 mA, Schmitt, PD25	DRAM data bus; bit DD7
V_{SS3}	25	–	–	ground 3
$\overline{LED}$	26	O	24 mA, CMOS test	panel LED; active LOW; WTGCTL(4)
$\overline{TRAYSW}$	27	I	Schmitt, PU25	active LOW when tray is in
$\overline{EJECT}$	28	I	Schmitt, PU25	opens tray; active LOW
LQDATA	29	O	2 mA	serial data to DAC
LWCLK	30	O	2 mA	word strobe to DAC
V_{SS4}	31	–	–	ground 4
SCLK	32	O	2 mA	data serial clock
V_{SS5}	33	–	–	ground 5
SYSRES	34	O	2 mA, PU25	system reset; OR of $\overline{POR}$, $\overline{SCSIRST}$ and watch-dog timer
CFLAG	35	I	Schmitt, PU400	C1 and C2 status
$\overline{CPR}$	36	O	2 mA	S2B interface ready to accept data; active LOW
$\overline{SPR}$	37	I	Schmitt	S2B interface ready to send data; active LOW
$\overline{SKIPFWD}$	38	I	Schmitt, PU25	skip forwards; active LOW; RDSW(3)
$\overline{SKIPBACK}$	39	I	Schmitt, PU25	skip backwards; active LOW; RDSW(2)
SCSICLK	40	I	standard	SCSI interface clock
V_{DD3}	41	–	–	power supply 3
AD0	42	I/O	S4, Schmitt	microcontroller multiplexed data bus; bit AD0
AD1	43	I/O	S4, Schmitt	microcontroller multiplexed data bus; bit AD1
AD2	44	I/O	S4, Schmitt	microcontroller multiplexed data bus; bit AD2
AD3	45	I/O	S4, Schmitt	microcontroller multiplexed data bus; bit AD3
AD4	46	I/O	S4, Schmitt	microcontroller multiplexed data bus; bit AD4
AD5	47	I/O	S4, Schmitt	microcontroller multiplexed data bus; bit AD5
AD6	48	I/O	S4, Schmitt	microcontroller multiplexed data bus; bit AD6
AD7	49	I/O	S4, Schmitt	microcontroller multiplexed data bus; bit AD7
V_{SS6}	50	–	–	ground 6
LA0	51	O	CMOS S2, PU25	EPROM latched lower address; bit LA0

SYMBOL	PIN	I/O	PAD	DESCRIPTION
LA1	52	O	CMOS S2, PU25	EPROM latched lower address; bit LA1
LA2	53	O	CMOS S2, PU25	EPROM latched lower address; bit LA2
LA3	54	O	CMOS S2, PU25	EPROM latched lower address; bit LA3
V_{DD4}	55	–	–	power supply 4
LA4	56	O	CMOS S2, PU25	EPROM latched lower address; bit LA4
LA5	57	O	CMOS S2, PU25	EPROM latched lower address; bit LA5
LA6	58	O	CMOS S2, PU25	EPROM latched lower address; bit LA6
LA7	59	O	CMOS S2, PU25	EPROM latched lower address; bit LA7
V_{SS7}	60	–	–	ground 7
A8	61	O	CMOS S2, PU25	EPROM upper address; bit A8
A9	62	O	CMOS S2, PU25	EPROM upper address; bit A9
A10	63	O	CMOS S2, PU25	EPROM upper address; bit A10
A11	64	O	CMOS S2, PU25	EPROM upper address; bit A11
A12	65	O	CMOS S2, PU25	EPROM upper address; bit A12
A13	66	O	CMOS S2, PU25	EPROM upper address; bit A13
A14	67	O	CMOS S2, PU25	EPROM upper address; bit A14
A15	68	O	CMOS S2, PU25	EPROM upper address; bit A15
$\overline{PSEN}$	69	O	CMOS 2, PU25	program store enable; active LOW
V_{SS8}	70	–	–	ground 8
$\overline{IO}$	71	I/O	SCSI	SCSI phase signal, active LOW
$\overline{REQ}$	72	I/O	SCSI	SCSI request, active LOW
$\overline{CD}$	73	I/O	SCSI	SCSI phase signal, active LOW
$\overline{SEL}$	74	I/O	SCSI	SCSI select, active LOW
V_{SS9}	75	–	–	ground 9
$\overline{MSG}$	76	I/O	SCSI	SCSI phase signal, active LOW
$\overline{ACK}$	77	I/O	SCSI	SCSI acknowledge, active LOW
$\overline{BSY}$	78	I/O	SCSI	SCSI busy, active LOW
V_{SS10}	79	–	–	ground 10
$\overline{ATN}$	80	I/O	SCSI	output in initiator mode; input in target mode, active LOW
V_{DD5}	81	–	–	power supply 5
$\overline{SDP}$	82	I/O	SCSI	SCSI parity, active LOW
SD7	83	I/O	SCSI	SCSI data bus; bit SD7
SD6	84	I/O	SCSI	SCSI data bus; bit SD6
SD5	85	I/O	SCSI	SCSI data bus; bit SD5
V_{SS11}	86	–	–	ground 11
SD4	87	I/O	SCSI	SCSI data bus; bit SD4
SD3	88	I/O	SCSI	SCSI data bus; bit SD3
SD2	89	I/O	SCSI	SCSI data bus; bit SD2
SD1	90	I/O	SCSI	SCSI data bus; bit SD1
SD0	91	I/O	SCSI	SCSI data bus; bit SD0
V_{SS12}	92	–	–	ground 12

SYMBOL	PIN	I/O	PAD	DESCRIPTION
RXS2B	93	I	Schmitt, PU25	S2B interface receive
TXS2B	94	O	4 mA	S2B interface transmit
$\overline{\text{TRAYIN}}$	95	I/O	4 mA, PD25	tray extend control; active LOW (general purpose signal)
$\overline{\text{TRAYOUT}}$	96	I/O	4 mA, PD25	tray retract control; active LOW (general purpose signal)
$\overline{\text{SCSIRST}}$	97	I	Schmitt	SCSI reset, active LOW; also causes a system reset
$\overline{\text{POR}}$	98	I	CMOS	power-on reset; active LOW
V_{DD6}	99	–	–	power supply 6
UC_PORT1.7	100	I/O	CMOS 2, PU25	drive speed select; microcontroller port 1.7
RAB_MUSB	101	I/O	CMOS 2, PU25	RD/WR, acknowledge; microcontroller port 1.2
NRST_SEQ	102	I/O	CMOS 2, PU25	reset to engine; microcontroller port 1.5
UC_PORT1.4	103	I/O	CMOS 2, PU25	general purpose microcontroller I/O port; port 1.4
UC_PORT1.3	104	I/O	CMOS 2, PU25	general purpose microcontroller I/O port; port 1.3
UC_PORT1.1	105	I/O	CMOS 2, PU25	general purpose microcontroller I/O port; port 1.1
$\overline{\text{HOMESW}}$	106	I/O	2 mA, PU25	actuator sled home; active LOW; microcontroller port 1.0
$\overline{\text{PLAY}}$	107	I	Schmitt	laser on and focused status; active LOW; RDSW(4)
UC_PORT1.6	108	I/O	CMOS 2, PU25	general purpose microcontroller I/O port; port 1.6
V_{SS13}	109	–	–	ground 13
GPI1	110	I	Schmitt, PU25	general purpose input; microcontroller port 3.4
GPI2	111	I	Schmitt, PU25	general purpose input; microcontroller port 3.5
$\overline{\text{KILL}}$	112	I	Schmitt, PU25	shut off audio; active LOW
TXICE	113	O	4 mA	debug UART output; from 80C32 serial port
RXICE	114	I	Schmitt, PU25	debug UART input; to 80C32 serial port
RXSUB	115	I	Schmitt, PU25	sub-code input
V_{DD7}	116	–	–	power supply 7
OSCIN	117	I	standard	master input clock; 34 or 16 MHz
V_{SS14}	118	–	–	ground 14
CLAB	119	I	Schmitt	clock
V_{SS15}	120	–	–	ground 15
DAAB	121	I	Schmitt	data
WSAB	122	I	Schmitt	word strobe
EFAB	123	I	Schmitt	error flag
CLK34	124	O	2 mA	34 MHz output clock
TEST	125	I	Schmitt, PD25	test pin; must be ground
V_{SS16}	126	–	–	ground 16
DA0	127	O	S4	DRAM address bus; bit DA0
DA1	128	O	S4	DRAM address bus; bit DA1

Error correction and host interface IC for CD-ROM (SEQUOIA)

SAA7385

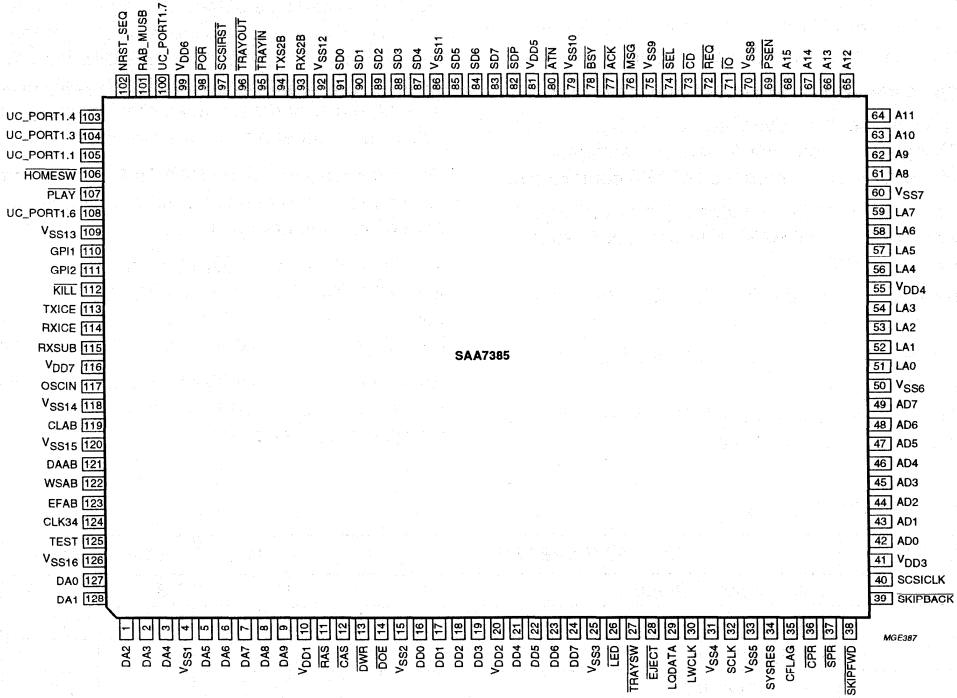


Fig.2 Pin configuration.

Error correction and host interface IC for CD-ROM (ELM)

SAA7388

FEATURES

- CD-ROM (Mode 1) and CD-I (Mode 2 - Form 1 and Form 2) formats supported
- Real-time error detection and correction in hardware
- Suitable for octal speed, n = 8
- Maximum host transfer burst rate of 13.3 Mbyte/s
- Corrects two errors per symbol with erasure correction
- 36 kbit of on-chip error correction buffer RAM
- 12-byte command FIFO and 12-byte status FIFO
- Compatible with the Advanced Technology Attachment (ATA) register set and the Advanced Technology Attachment Program Interface (ATAPI) command set
- Operates with popular memories. (up to 128 kbyte SRAM; 1 to 16 Mbit DRAM, different speed grades, nibble or byte wide)
- Interface to Integrated Drive Electronics (IDE) bus without external bus drivers
- Q-to-W subcode buffering, de-interleaving and correction are supported
- Device can operate with audio RAMs. A RAM test allows bad segments to be identified.

GENERAL DESCRIPTION

The SAA7388 decoder is a block decoder buffer manager for high-speed CD-ROM applications that integrates real-time error correction and detection and host interface data transfer functions into a single chip.

The SAA7388 has an on-chip 36-kbit memory. This memory is used as a buffer memory for error and erasure corrections. The chip also has a buffer memory interface thus enabling the connection of SRAM up to 128 kbytes, or DRAM up to 16 Mbits. The on-chip memory is sufficient to buffer 1 sector of data. The external memory can buffer many more, depending on memory size.

The error corrector of the SAA7388 can perform 2-pass error correction in real-time. Buffer memory for this correction is integrated on-chip.

The SAA7388 has an host interface that is compatible with the SANYO LC89510 or OAK OTI-012 and also compatible with the ATA/IDE/ATAPI hard disc interface bus. (All ATAPI registers are present in hardware).

Supply of this Compact Disc IC does not convey an implied license under any patent right to use this IC in any Compact Disc application.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDD1}	digital supply voltage 1	3.0	3.3	3.6	V
V_{DDD2}	digital supply voltage 2	4.5	5	5.5	V
I_{DDD}	supply current	–	60	–	mA
f_{clk}	clock frequency	15.2	48	50.4	MHz
T_{amb}	operating ambient temperature	0	–	+70	°C
T_{stg}	storage temperature	−55	–	+125	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7388GP	QFP80	plastic quad flat package; 80 leads; lead length 1.95 mm; body 14 × 20 × 2.8 mm	SOT318-2

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATA SHEET

BLOCK DIAGRAM

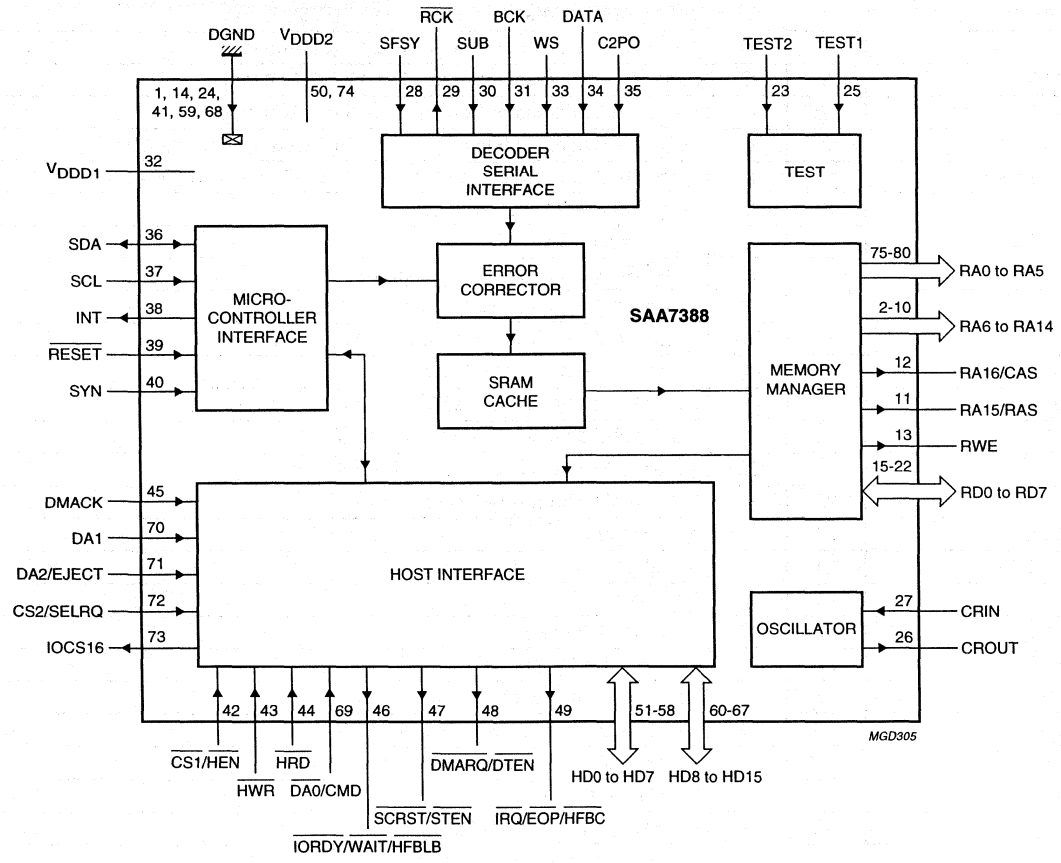


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	I/O	DESCRIPTION
DGND1	1	–	digital ground 1
RA6	2	O	buffer RAM address bus output line 6
RA7	3	O	buffer RAM address bus output line 7
RA8	4	O	buffer RAM address bus output line 8
RA9	5	O	buffer RAM address bus output line 9
RA10	6	O	buffer RAM address bus output line 10
RA11	7	O	buffer RAM address bus output line 11 (SRAM) only
RA12	8	O	buffer RAM address bus output line 12 (SRAM) only
RA13	9	O	buffer RAM address bus output line 13 (SRAM) only
RA14	10	O	buffer RAM address bus output line 14 (SRAM) only
RA15/RAS	11	O	buffer RAM address bus output line 15 (SRAM) or RAS (DRAM)
RA16/CAS	12	O	buffer RAM address bus output line 16 (SRAM) or CAS (DRAM)
RWE	13	O	buffer RAM write enable output
DGND2	14	–	digital ground 2
RD0	15	I/O	buffer RAM data bus bidirectional line 0
RD1	16	I/O	buffer RAM data bus bidirectional line 1
RD2	17	I/O	buffer RAM data bus bidirectional line 2
RD3	18	I/O	buffer RAM data bus bidirectional line 3
RD4	19	I/O	buffer RAM data bus bidirectional line 4
RD5	20	I/O	buffer RAM data bus bidirectional line 5
RD6	21	I/O	buffer RAM data bus bidirectional line 6
RD7	22	I/O	buffer RAM data bus bidirectional line 7
TEST2	23	I	test input 2
DGND3	24	–	digital ground 3
TEST1	25	I	test input 1
CROUT	26	O	clock oscillator output
CRIN	27	I	clock oscillator input
SFSY	28	I	serial subcode input frame sync input
$\overline{\text{RCK}}$	29	O	serial subcode clock output (active LOW)
SUB	30	I	serial input for Q-to-W subcode input
BCK	31	I	serial interface bit clock input
V_{DDD1}	32	–	digital supply voltage 1 (3.3 V)
WS	33	I	serial interface word clock input
DATA	34	I	serial data input
C2PO	35	I	serial interface flag input
SDA	36	I/O	sub-CPU serial data input/output
SCL	37	I	sub-CPU serial clock input
INT	38	O	sub-CPU open-collector interrupt output
$\overline{\text{RESET}}$	39	I	power-on reset input (active LOW)
SYN	40	I	sync signal input from sub-CPU

SYMBOL	PIN	I/O	DESCRIPTION
DGND4	41	–	digital ground 4
$\overline{CS1}/\overline{HEN}$	42	I	host interface enable input (active LOW)
$\overline{HWR}$	43	I	host interface write enable input (active LOW)
$\overline{HRD}$	44	I	host interface read enable input (active LOW)
DMACK	45	I	DMA acknowledge input
$\overline{IORDY}/\overline{WAIT}/\overline{HFBLB}$	46	O	host interface wait output (active LOW); 3-state control
$\overline{SCRST}/\overline{STEN}$	47	O	host interface status enable output ATAPI sub-CPU reset signal (active LOW)
$\overline{DMARQ}/\overline{DTEN}$	48	O	ATAPI DMA request host interface data enable output (active LOW); 3-state control
$\overline{IRQ}/\overline{EOP}/\overline{HFBC}$	49	O	host interface end of process flag output ATAPI host interrupt request (active LOW); 3-state control
V_{DDD2}	50	–	digital supply voltage 2 (5 V)
HD0	51	I/O	host interface data bus input/output line 0
HD1	52	I/O	host interface database input/output line 1
HD2	53	I/O	host interface database input/output line 2
HD3	54	I/O	host interface data bus input/output line 3
HD4	55	I/O	host interface data bus input/output line 4
HD5	56	I/O	host interface data bus input/output line 5
HD6	57	I/O	host interface data bus input/output line 6
HD7	58	I/O	host interface data bus input/output line 7
DGND5	59	–	digital ground 5
HD8	60	I/O	host interface data bus input/output line 8
HD9	61	I/O	host interface data bus input/output line 9
HD10	62	I/O	host interface data bus input/output line 10
HD11	63	I/O	host interface data bus input/output line 11
HD12	64	I/O	host interface data bus input/output line 12
HD13	65	I/O	host interface data bus input/output line 13
HD14	66	I/O	host interface data bus input/output line 14
HD15	67	I/O	host interface data bus input/output line 15
DGND6	68	–	digital ground 6
$\overline{DA0}$/CMD	69	I	host interface data input (active LOW)/command select input host interface address line 0
DA1	70	I	ATAPI address line input 1
DA2/EJECT	71	I	ATAPI address line input 2
CS2/SELRQ	72	I	ATAPI chip select input 2
IOCS16	73	O	ATAPI 16-bit data select output
V_{DDD2}	74	–	digital supply voltage 2 (5 V)
RA0	75	O	buffer RAM address bus output line 0
RA1	76	O	buffer RAM address bus output line 1
RA2	77	O	buffer RAM address bus output line 2

SYMBOL	PIN	I/O	DESCRIPTION
RA3	78	O	buffer RAM address bus output line 3
RA4	79	O	buffer RAM address bus output line 4
RA5	80	O	buffer RAM address bus output line 5

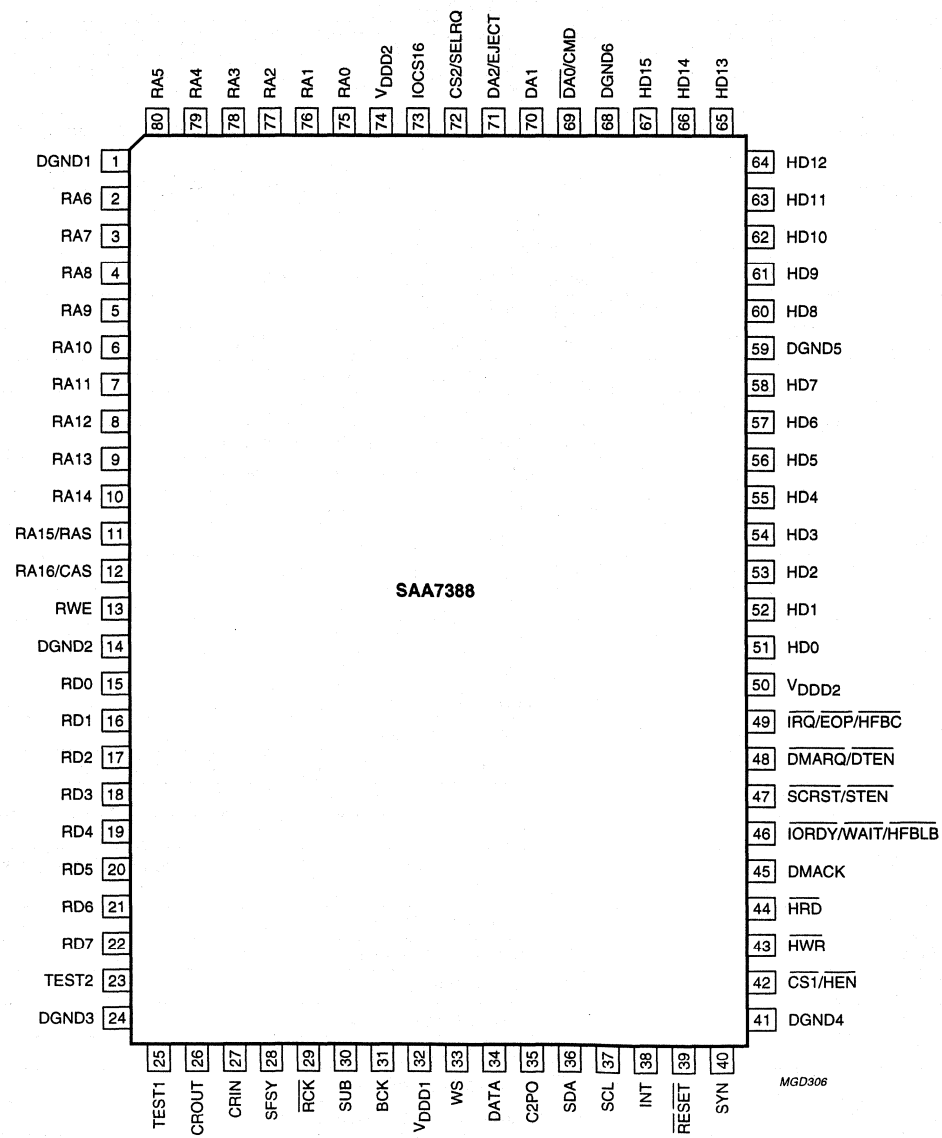


Fig.2 Pin configuration.

Pin functions

RA0 TO RA14

External memory address signals.

RA16/CAS

External memory RA16 signal if SRAM or, CAS signal if DRAM.

RA15/RAS

External memory RA15 signal if SRAM or, RAS signal if DRAM.

RWE

Write output enable signal for external buffer memory. This is LOW when the SAA7388 wants to write data into the external memory.

RD0 TO RD7

External buffer memory bidirectional data signals.

SFSY

Frame sync for the Q-to-W subcode, indicates when P-channel is available by a HIGH-to-LOW transition. Frame 0 is also indicated by no transition on this line.

$\overline{RCK}$

In response to SFSY going LOW data is clocked into the SAA7388 before each rising edge using this clock output.

SUB

Q-to-W subcode is input in response to $\overline{RCK}$ in 3-wire EIAJ mode or WS in "V4" mode compatible with the SAA7345.

BCK

Bit clock for the serial data input from the CD decoder.

WS

Word clock for the serial data input from the CD decoder.

DATA

Serial data input from the CD decoder. This may be either I^2S-bus or EIAJ 16-bit format.

C2PO

Error flag from the CD decoder. A HIGH indicates that a byte has not been corrected by the C2 error corrector and therefore is not valid. This is taken into account by the SAA7388 error corrector.

SDA

Sub-CPU bidirectional data signal. This signal forms part of the 3-wire serial interface between the SAA7388 and the sub-CPU.

SCL

Sub-CPU sync signal. This signal forms part of the 3-wire serial interface between the SAA7388 and the sub-CPU. This signal is used to synchronize data transfers between the sub-CPU and the SAA7388.

INT

Sub-CPU interrupt signal. This active LOW output signals to the sub-CPU that the SAA7388 has an interrupt request.

$\overline{RESET}$

Forcing this input LOW resets the SAA7388.

SYN

Sub-CPU clock signal. This signal forms part of the 3-wire serial interface between the SAA7388 and the sub-CPU. This signal is the sub-CPU driven bit clock used to synchronize the signals on the SDA line.

$\overline{CS1}/\overline{HEN}$

In the ATAPI mode this is the host chip select 1 address signal. In the Sanyo and Oak compatibility modes setting this input LOW enables the host interface.

$\overline{HWR}$

This active LOW signal is the host write request.

$\overline{HRD}$

This active LOW signal is the host read request.

DMACK

This signal is used in the ATAPI and Oak compatibility modes during DMA transfers. The host pulls this signal LOW in response to a $\overline{\text{DMARQ}}$ request to indicate that it is ready to transfer data.

If this signal is not being used then it must be pulled HIGH for SAA7388 to operate correctly.

$\overline{\text{IORDY}}$/$\overline{\text{WAIT}}$/$\overline{\text{HFBLB}}$

In the ATAPI mode this signal is negated to extend the host transfer cycle of any host register access. It is used in PIO transfers. When $\overline{\text{IORDY}}$ is not negated it is in a high-impedance state.

In the Sanyo compatibility mode the function of this signal depends on the SELRQ input. If SELRQ is HIGH then $\overline{\text{WAIT}}$ is set LOW to extend the host transfer cycle. If SELRQ is LOW then $\overline{\text{WAIT}}$ acts as the DRQ signal in a DMA transfer.

In the Oak compatibility mode this signal is the Host First Byte Latch signal. A rising edge on this signal is used to latch the first byte in a pseudo 16-bit DMA read. $\overline{\text{HFBLB}}$ can only be HIGH when pseudo 16-bit DMA transfer mode is selected.

$\overline{\text{SCRST}}$/$\overline{\text{STEN}}$

In the ATAPI or Oak compatibility mode this signal is pulled LOW to reset the sub-CPU in response to a reset command from the host.

In the Sanyo compatibility mode this signal is pulled LOW to signal to the host that status bytes are available for transfer.

$\overline{\text{DMARQ}}$/$\overline{\text{DTEN}}$

In the ATAPI or Oak compatibility mode this signal is asserted when the SAA7388 is ready to transfer data between the host and itself. In ATAPI single word and Oak DMA transfers this occurs at every word. In ATAPI multi-word DMA transfers this occurs at the start of the transfer.

In the Sanyo compatibility mode this signal is pulled LOW to signal to the host that data bytes are available for transfer.

$\overline{\text{IRQ}}$/$\overline{\text{EOP}}$/$\overline{\text{HFBC}}$

In the ATAPI mode this active HIGH signal indicates a host interrupt request. It is asserted when the sub-CPU writes to the ITRG register and is negated when the host reads the status register or writes to the command register.

In the Sanyo compatibility mode this signal is set LOW when the last data byte is transferred to or from the host.

In the Oak compatibility mode this is the Host First Byte Cycle output and is HIGH while the first byte in the pseudo 16-bit DMA transfer is accessed. It should be used to inhibit non-DMA transactions while the first byte is latched.

HD0 TO HD15

These are the bidirectional Host Data signals. In the Sanyo and Oak compatibility modes HD8 to HD15 are never used.

$\overline{\text{DA0}}$/CMD

In the ATAPI mode this is the host Data Address 0 signal. In the Sanyo and Oak compatibility modes this input selects between command or data transfers.

DA1

This is the ATAPI Data Address 1 signal.

DA2/ EJECT

In the ATAPI mode this is the Data Address 2 signal. In the Oak compatibility mode this is the door switch input pin. Its state is reflected in the TSTAT register.

CS2/SELRQ

In the ATAPI mode this is the Chip Select 2 signal. In the Oak and Sanyo compatibility mode this is the data transfer mode select input. It is used to select between PIO and DMA transfers.

IOCS16

This open-collector signal is used in the ATAPI mode to signal to the host that a 16-bit data port has been addressed. It is not activated during DMA transfers.

High performance Compact Disc-Recordable (CD-R) controller

SAA7390

FEATURES

General

- 8× speed CD-ROM, 4× speed Compact Disc-Recordable (CD-R) controller
- 16.9 Mbytes/s burst rate to host controller
- High performance CD-ROM and CD-R interface logic
- 128 pin QFP package.

Interface logic (CD-ROM operation)

- Full 8× speed hardware operation
- Block decoder
- Sector sequencer
- CRC checking of Mode 1 and Mode 2, Form 1 sectors
- 212 ms watch-dog timer
- Sub-code interface with synchronization
- C-flag interface for absolute time stamp.

Hardware third-level error correction

- Third-level correction provides superior performance in unfavourable conditions
- Full hardware error correction to reduce microcontroller overhead
- Corrections are automatically written to the DRAM frame buffer.

Interface logic (CD-R operation)

- Block encoder (using a modified CDB2).

DRAM buffer controller (256 kbytes × 8, 1 Mbyte × 8, 4 Mbytes × 8)

- DRAM buffer manager
- Ten level arbitration logic
- Utilizes low cost 70 ns DRAMs
- Page mode DRAM access for high-speed error correction and host interface data transfers
- Data organization by 3 kbytes frames.

Additional product support

- Input clock doubler
- All control registers mapped into 80C32 special function memory space
- Red book audio pass through to host interface
- Sub-code and Q-channel support
- Dedicated Serial Peripheral Interface (SPI)
- Third level error correction and encoding
- 80C32 microcontroller interface
- 53CF90 or 53CF92A/B fast SCSI processor interface (may also use ATAPI processor).

GENERAL DESCRIPTION

The SAA7390 is a high integration ASIC that incorporates all of the logic necessary to connect a CD-60 based decoder to a SCSI or ATAPI host. It also supports a data path from the host to the CDCEP (compact disc encoder) for CD-R applications. An 80C32 microcontroller and a 53CF94/92A (or an ATAPI interface device) are required to provide the full block encode/decode functions. The following functions are supported:

- Input clock doubler
- Block encoder (using a modified CDB2)
- Block decoder
- CRC checking of Mode 1 and Mode 2, Form 1 sectors
- Red book audio pass through to SCSI or ATAPI
- Sub-code and Q-channel support
- Dedicated S2B interface UART
- Dedicated SPI interface UART
- Up to 4 Mbytes DRAM buffer manager
- Third-level error correction and encoding
- Automatic storage of audio and data
- 80C32 microcontroller interface
- 53CF90 or 53CF92A/B fast SCSI or Wapiti ATAPI processor interface.

The SAA7390 uses a 33.8688 MHz clock and is capable of accepting data at eight times (n = 8 or 1.4 Mbytes/s) the normal CD-ROM data rate. The minimum host burst rate capability of the SAA7390 is 5 Mbytes/s.

Third level error correction hardware is included to improve the correction efficiency of the system. The buffer manager hardware utilizes a ten-level arbitration unit and can stop the clock to the static microcontroller to emulate a wait condition when necessary. The host interface is capable of burst rates to 16.9 Mbytes/s.

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATA SHEET

High performance Compact Disc-Recordable (CD-R) controller

SAA7390

The SAA7390 comprises four major functional blocks:

- The front-end block connects to the external CD-60 based decoder and fully processes the incoming data stream
- The buffer manager block provides the address generation and timing control for the external DRAMs
- The ECC block performs the error correction functions in hardware on the data stored in the DRAM buffer.
- The block encoder function (realized via a modified CDB2) serializes the data from the buffer, appends the sync pattern, header, sub-header, third level ECC parity and EDC bytes as necessary, performs the required scrambling and outputs them to the CDCEP using a special data clock (98 clock cycles per word selection period).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	digital supply voltage	4.5	5.0	5.5	V
T_{amb}	operating ambient temperature	0	–	70	°C
T_{stg}	storage temperature	–55	–	+150	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7390GP[1]	SQFP128	plastic quad flat package; 128 leads (lead length 1.6 mm); body 14 × 20 × 2.8 mm	SOT387-2

Note

1. This device uses a Symbios logic package.

BLOCK DIAGRAM

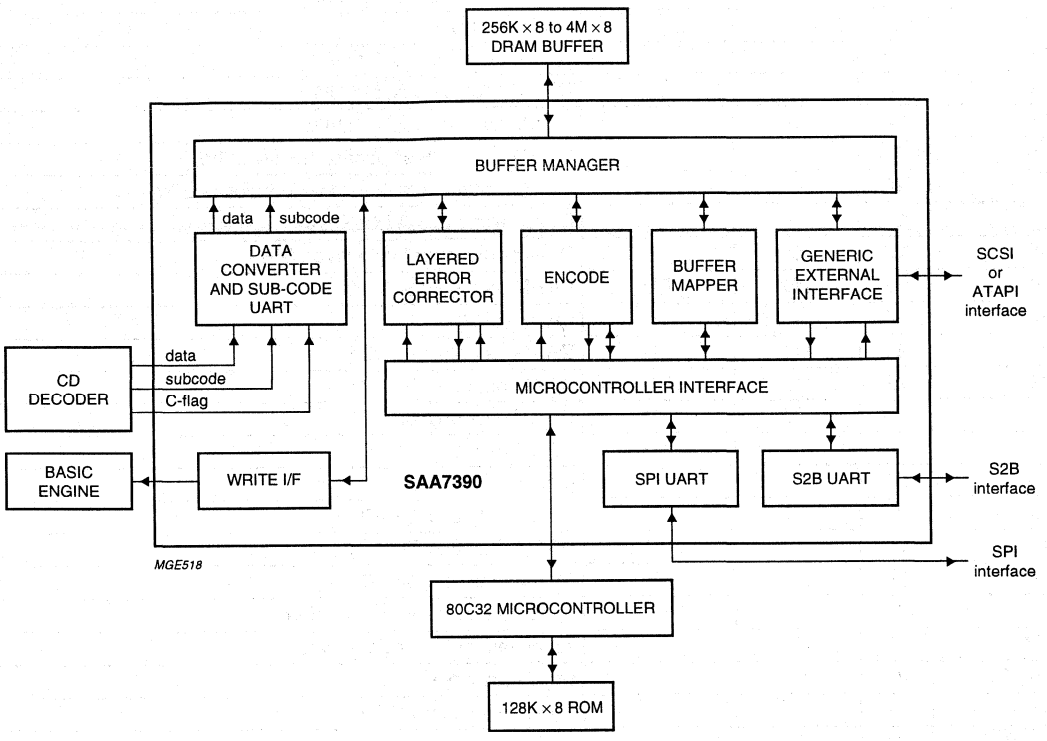


Fig.1 Block diagram (simplified).

PINNING

All input and bidirectional signals are TTL level with Schmitt-trigger logic, with the exception of OSCIN. All output signals are TTL levels unless otherwise stated. (PD = internal pull-down; PU = internal pull-up).

SYMBOL	PIN	I/O	TYPE	DESCRIPTION
DA0	1	O		DRAM address bus; bit DA0
DA1	2	O		DRAM address bus; bit DA1
DA2	3	O		DRAM address bus; bit DA2
V_{SS1}	4	–		ground 1
DA3	5	O		DRAM address bus; bit DA3
DA4	6	O		DRAM address bus; bit DA4
DA5	7	O		DRAM address bus; bit DA5
V_{SS2}	8	–		ground 2
DA6	9	O		DRAM address bus; bit DA6

SYMBOL	PIN	I/O	TYPE	DESCRIPTION
DA7	10	O		DRAM address bus; bit DA7
V_{DD1}	11	–		power supply 1
DA8	12	O		DRAM address bus; bit DA8
DA9	13	O		DRAM address bus; bit DA9
DA10	14	O		DRAM address bus; bit DA10
$\overline{RAS}$	15	O		DRAM row address section; active LOW
$\overline{CAS}$	16	O		DRAM column address selection; active LOW
$\overline{DWR}$	17	O		DRAM write; active LOW
$\overline{DOE}$	18	O		DRAM output enable; active LOW
DD0	19	I/O	PD	DRAM data bus; bit DD0
V_{DD2}	20	–		power supply 2
DD1	21	I/O	PD	DRAM data bus; bit DD1
DD2	22	I/O	PD	DRAM data bus; bit DD2
DD3	23	I/O	PD	DRAM data bus; bit DD3
DD4	24	I/O	PD	DRAM data bus; bit DD4
V_{SS3}	25	–		ground 3
DD5	26	I/O	PD	DRAM data bus; bit DD5
DD6	27	I/O	PD	DRAM data bus; bit DD6
DD7	28	I/O	PD	DRAM data bus; bit DD7
COM_IN	29	I		serial data in from basic engine
COM_OUT	30	O		serial data out to basic engine
COM_CLK	31	O		serial data clock
COM_ACK	32	I		serial data acknowledge
$\overline{TRAYSW}$	33	I	PU	active LOW when tray is in
$\overline{EJECT}$	34	I	PU	opens tray; active LOW
LQDATA	35	O		latched qualified data
LWCLK	36	O		latched word clock
V_{DD3}	37	–		power supply 3
$\overline{LED}$	38	O	CMOS; 24 mA	panel LED; active LOW; open drain; 24 mA (min.) sink capability
V_{SS4}	39	–		ground 4
SCLK	40	O		audio data clock
V_{SS5}	41	–		ground 5
SYSRES	42	O		system reset; active HIGH
$\overline{SYSRES}$	43	O		system reset; active LOW
V_{DD4}	44	–		power supply 4
GPIO3	45	I/O	PD	general purpose input/output 3
GPIO4	46	I/O	PD	general purpose input/output 4
$\overline{VOLUP}$	47	I	PU	volume up; active LOW
$\overline{VOLDN}$	48	I	PU	volume down; active LOW
UC_AD0	49	I/O		microprocessor multiplexed address/data bus; bit UC_AD0
UC_AD1	50	I/O		microprocessor multiplexed address/data bus; bit UC_AD1

SYMBOL	PIN	I/O	TYPE	DESCRIPTION
UC_AD2	51	I/O		microprocessor multiplexed address/data bus; bit UC_AD2
UC_AD3	52	I/O		microprocessor multiplexed address/data bus; bit UC_AD3
V_{SS6}	53	–		ground 6
UC_AD4	54	I/O		microprocessor multiplexed address/data bus; bit UC_AD4
UC_AD5	55	I/O		microprocessor multiplexed address/data bus; bit UC_AD5
UC_AD6	56	I/O		microprocessor multiplexed address/data bus; bit UC_AD6
UC_AD7	57	I/O		microprocessor multiplexed address/data bus; bit UC_AD7
V_{DD5}	58	–		power supply 5
UC_LA0	59	O		latched lower address; bit UC_LA0
UC_LA1	60	O		latched lower address; bit UC_LA1
UC_LA2	61	O		latched lower address; bit UC_LA2
V_{SS7}	62	–		ground 7
UC_LA3	63	O		latched lower address; bit UC_LA3
UC_LA4	64	O		latched lower address; bit UC_LA4
UC_LA5	65	O		latched lower address; bit UC_LA5
UC_LA6	66	O		latched lower address; bit UC_LA6
UC_LA7	67	O		latched lower address; bit UC_LA7
V_{SS8}	68	–		ground 8
PCLK	69	O		33.8688 MHz microprocessor clock
V_{DD6}	70	–		power supply 6
ALE	71	I		address latch enable
$\overline{UC\_WR}$	72	I		write enable
$\overline{UC\_RD}$	73	I		read enable
$\overline{INT}$	74	O	CMOS	interrupt to microcontroller; active LOW; open drain
UC_A8	75	I		upper address; bit UC_A8
UC_A9	76	I		upper address; bit UC_A9
UC_A10	77	I		upper address; bit UC_A10
SYS_SYNC	78	I		system synchronization from basic engine
UC_A11	79	I		upper address; bit UC_A11
UC_A12	80	I		upper address; bit UC_A12
UC_A13	81	I		upper address; bit UC_A13
COM_SYNC	82	I		communication synchronization from basic engine
UC_A14	83	I		upper address; bit UC_A14
UC_A15	84	I		upper address; bit UC_A15
SD0	85	I/O		internal data bus; bit SD0
V_{DD6}	86	–		power supply 6
SD1	87	I/O		internal data bus; bit SD1
SD2	88	I/O		internal data bus; bit SD2
V_{SS9}	89	–		ground 9
SD3	90	I/O		internal data bus; bit SD3
SD4	91	I/O		internal data bus; bit SD4

SYMBOL	PIN	I/O	TYPE	DESCRIPTION
SD5	92	I/O		internal data bus; bit SD5
SD6	93	I/O		internal data bus; bit SD6
SD7	94	I/O		internal data bus; bit SD7
V_{SS10}	95	–		ground 10
DREQ	96	I	PD	DMA request
$\overline{DACK}$	97	O		DMA acknowledge; active LOW
$\overline{HOSTRD}$	98	O		read enable; active LOW
$\overline{HOSTWR}$	99	O		write enable; active LOW
$\overline{HOSTSEL}$	100	O		chip select; active LOW
CSAB	101	I		word strobe for write data
CCLAB	102	I		clock for write data
CDAAB	103	O		write data stream
RXS2B	104	I	PU	receive data
TXS2B	105	O		transmit data
$\overline{CPR}$	106	O		ready to accept data; active LOW
$\overline{SCSIRST}$	107	I		reset from SCSI bus; active LOW
$\overline{POR}$	108	I		power-on reset; active LOW
TCL_GPIO1	109	I/O	PD	general purpose input/output 1 (also used as test-mode clock)
$\overline{SPR}$	110	I		ready to send data; active LOW
TDA_GPIO2	111	I/O	PD	general purpose input/output 2 (also used as test-mode data)
$\overline{HFD}$	112	I		laser on and focused status; active LOW
$\overline{KILL}$	113	I	PU	mute audio; active LOW
V_{SS11}	114	–		ground 11
MCOUT	115	O		motor control output from PWM
MCIN	116	I	PD	motor control input from decoder
RXSUB	117	I	PU	sub-code input
CFLAG	118	I	PU	C1 and C2 status
V_{SS12}	119	–		ground 12
OSCIN	120	I		input clock from decoder
V_{DD7}	121	–		power supply 7
CLAB	122	I		clock input
DAAB	123	I		data input
WSAB	124	I		word strobe input
EFAB	125	I		error flags
V_{SS13}	126	–		ground 13
CLK34	127	O		33.8688 MHz output clock
V_{DD8}	128	–		power supply 8

High performance Compact Disc-Recordable (CD-R) controller

SAA7390

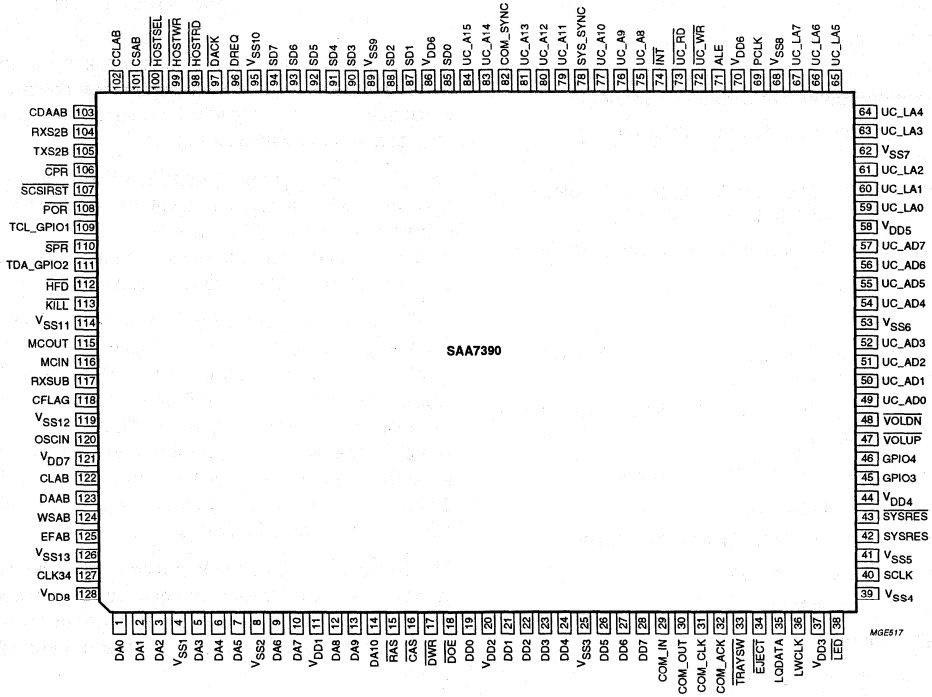


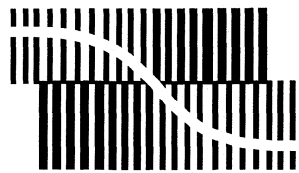
Fig.2 Pin configuration.

Stereo 1fs data input up-sampling filter with bitstream continuous dual DAC (BCC-DAC2)

TDA1305T

FEATURES

- Easy application
- $16f_s$ Finite-duration Impulse-Response (FIR) filter incorporated
- Selectable system clock (f_{sys}) $256f_s$ or $384f_s$
- I^2S-bus serial input format (at $f_{sys} = 256f_s$) or LSB fixed 16, 18 or 20 bits serial input mode (at $f_{sys} = 384f_s$)
- Slave-mode clock system
- Cascaded 4-stage digital filter incorporating 2-stage FIR filter, linear interpolator and sample-and-hold
- Smoothed transitions before and after muting (soft mute)
- Digital de-emphasis filter for three sampling rates of 32 kHz, 44.1 kHz and 48 kHz
- 12 dB attenuation via the attenuation input control
- Double speed mode
- 2nd order noise shaper
- 96 ($f_{sys} = 384f_s$) or 128 ($f_{sys} = 256f_s$) times oversampling in normal speed mode
- 48 ($f_{sys} = 384f_s$) or 64 ($f_{sys} = 256f_s$) times oversampling in double speed mode
- Bitstream continuous calibration concept
- Small outline SO28 package
- Voltage output 1.5 V (RMS) at line drive level
- Low total harmonic distortion
- No zero crossing distortion
- Inherently monotonic
- No analog post filtering required
- Superior signal-to-noise ratio
- Wide dynamic range (18-bit)
- Single rail supply (3.4 to 5.5 V).



BITSTREAM CONVERSION

GENERAL DESCRIPTION

The TDA1305T is a new generation of filter-DAC which features a unique combination of bitstream and continuous calibration techniques. The converter functions as a bitstream converter for low signals while large signals are generated using the dynamic continuous calibration technique, thus resulting in low power consumption, small chip size and easy application.

The TDA1305T is a dual CMOS DAC with up-sampling filter and noise shaper. The combination of high oversampling up to $16f_s$, 2nd order noise shaping and continuous calibration conversion ensures that only simple 1st order analog post filtering is required.

The TDA1305T supports the I^2S-bus data input mode with word lengths of up to 20 bits (at $f_{sys} = 256f_s$) and the LSB fixed serial data input format with word lengths of 16, 18 and 20 bits (at $f_{sys} = 384f_s$). Four cascaded FIR filters increase the oversampling rate to 16 times. A sample-and-hold function increases the oversampling rate to 96 times ($f_{sys} = 384f_s$) or 128 times ($f_{sys} = 256f_s$). A 2nd order noise shaper converts this oversampled data to a bitstream for the 5-bit DACs.

The DACs are of the continuous calibration type and incorporate a special date coding. This ensures an extremely high signal-to-noise ratio, superior dynamic range and immunity to process variation and component ageing.

Two on-board operational amplifiers convert the digital-to-analog current to an output voltage. Externally connected capacitors perform the required 1st order filtering so that no further post filtering is required.

The unique combination of bitstream and continuous calibration techniques, together with a high degree of analog and digital integration, results in a single filter-DAC with 18-bit dynamic range, high linearity and simple low cost application.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1305T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage	note 1	3.4	5.0	5.5	V
V_{DDA}	analog supply voltage	note 1	3.4	5.0	5.5	V
V_{DDO}	operational amplifier supply voltage	note 1	3.4	5.0	5.5	V
I_{DDD}	digital supply current	V_{DDD} = 5 V; at code 00000H	–	30	–	mA
I_{DDA}	analog supply current	V_{DDA} = 5 V; at code 00000H	–	5.5	8	mA
I_{DDO}	operating amplifier supply current	V_{DDO} = 5 V; at code 00000H	–	6.5	9	mA
$V_{FS(rms)}$	full-scale output voltage (RMS value)	$V_{DDD} = V_{DDA} = V_{DDO}$ = 5 V	1.425	1.5	1.575	V
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB signal level	–	–90	–81	dB
			–	0.003	0.009	%
		at –60 dB signal level	–	–44	–40	dB
			–	0.63	0.1	%
		at –60 dB signal level; A-weighted	–	–46	–	dB
			–	0.5	–	%
S/N	signal-to-noise ratio at bipolar zero	A-weighting; at code 00000H	100	108	–	dB
BR_{ns}	input bit rate at data input	f_s = 48 kHz; normal speed	–	–	3.072	Mbits
BR_{ds}	input bit rate at data input	f_s = 48 kHz; double speed	–	–	6.144	Mbits
f_{sys}	system clock frequency		6.4	–	18.432	MHz
TC_{FS}	full scale temperature coefficient at analog outputs (VOL and VOR)		–	$\pm 100 \times 10^{-6}$	–	
T_{amb}	operating ambient temperature		–30	–	+85	°C

Note

1. All V_{DD} and V_{SS} pins must be connected to the same supply.

BLOCK DIAGRAM

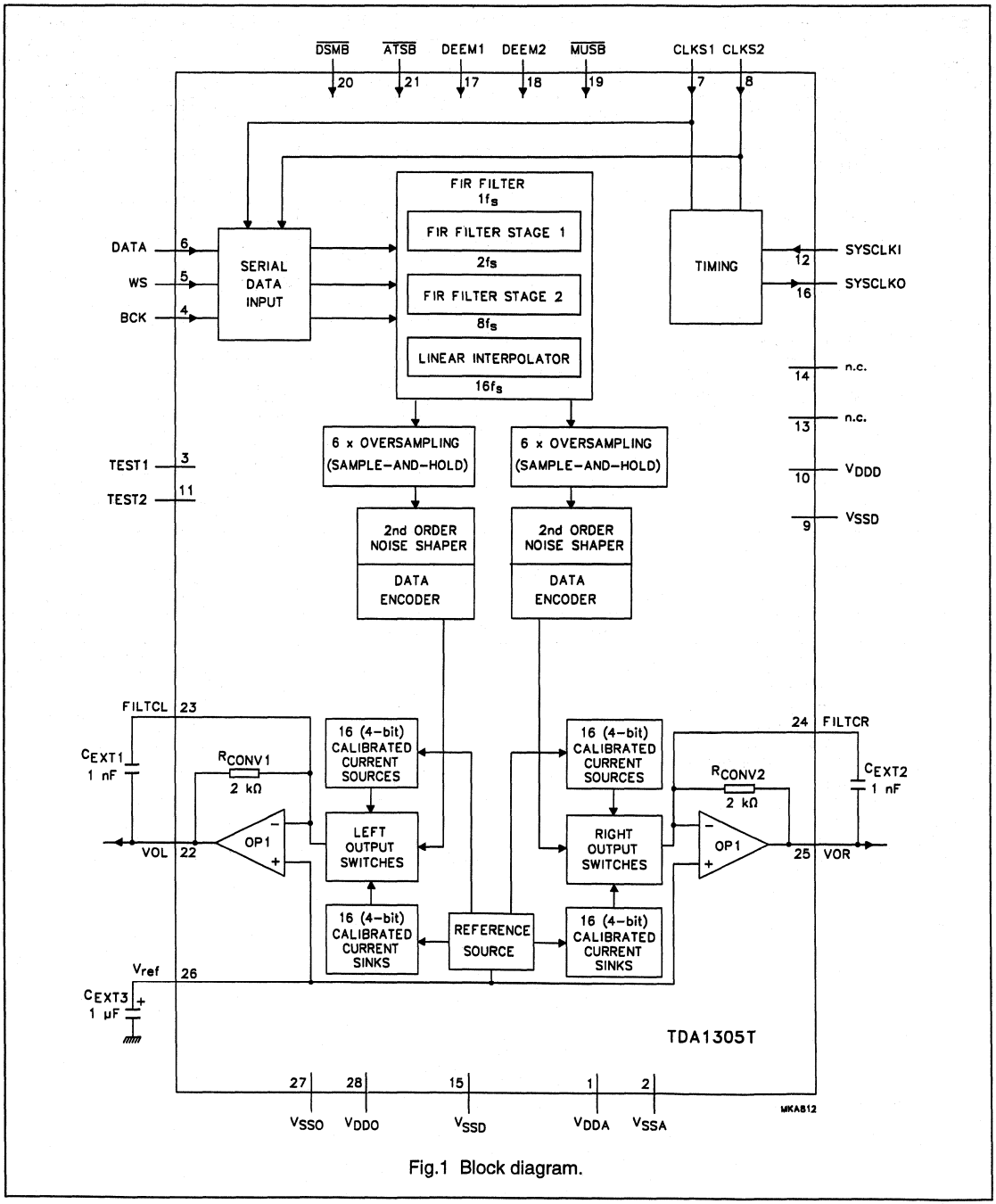


Fig.1 Block diagram.

Stereo 1fs data input up-sampling filter with bitstream continuous dual DAC (BCC-DAC2)

TDA1305T

PINNING

SYMBOL	PIN	DESCRIPTION
V_{DDA}	1	analog supply voltage
V_{SSA}	2	analog ground
TEST1	3	test input; pin should be connected to ground (internal pull-down resistor)
BCK	4	bit clock input
WS	5	word select input
DATA	6	data input
CLKS1	7	clock selection 1 input
CLKS2	8	clock selection 2 input
V_{SSD}	9	digital ground
V_{DDD}	10	digital supply voltage
TEST2	11	test input; pin should be connected to ground (internal pull-down resistor)
SYSCLKI	12	system clock input
n.c.	13	not connected (this pin should be left open-circuit)
n.c.	14	not connected (this pin should be left open-circuit)
V_{SSD}	15	digital ground
SYSCLKO	16	system clock output
DEEM1	17	de-emphasis on/off; f_{DEEM} 32 kHz, 44 kHz and 48 kHz
DEEM2	18	de-emphasis on/off; f_{DEEM} 32 kHz, 44 kHz and 48 kHz
$\overline{MUSB}$	19	mute input (active LOW)
$\overline{DSMB}$	20	double-speed mode input (active LOW)
$\overline{ATSB}$	21	12 dB attenuation input (active LOW)
VOL	22	left channel output
FILTCL	23	capacitor for left channel 1st order filter function should be connected between pins 22 and 23
FILTCR	24	capacitor for right channel 1st order filter function should be connected between pins 25 and 24
VOR	25	right channel output
V_{ref}	26	internal reference voltage for output channels ($0.5V_{DD}$)
V_{SSO}	27	operational amplifier ground
V_{DDO}	28	operational amplifier supply voltage

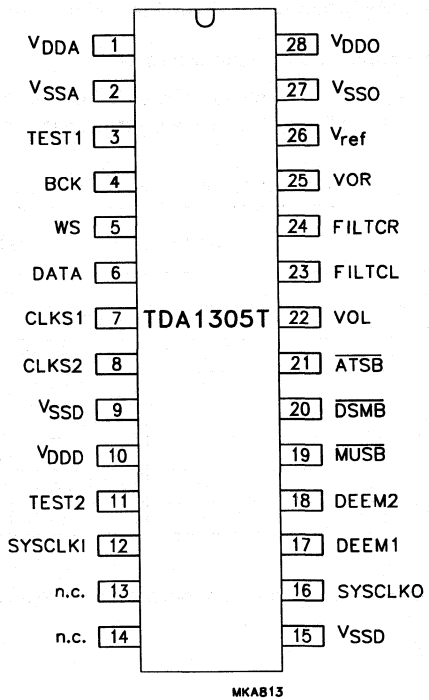


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA1305T CMOS digital-to-analog bitstream converter incorporates an up-sampling filter and noise shaper which increase the oversampling rate of $1f_s$ input data to $96f_s$ ($f_{sys} = 192f_s$) or $128f_s$ ($f_{sys} = 256f_s$) in the normal speed mode. In the double speed mode the oversample rate of $1f_s$ input data is increased to $48f_s$ ($f_{sys} = 384f_s$) or $64f_s$ ($f_{sys} = 256f_s$). This oversampling, together with the 5-bit DAC, enables the filtering required for waveform smoothing and out-of-band noise reduction to be achieved by simple 1st order analog post filtering.

System clock and data input format

The TDA1305T accommodates slave mode only, this means that in all applications the system devices must provide a system clock of 256 or $384f_s$ (f_s = 32, 44.1 or 48 kHz). The system frequency is selectable by means of pin CLKS1 and pin CLKS2. The SYSCLKO output (pin 16) provides the system clock for external use.

The TDA1305T supports the following data input modes:

- I^2S-bus with data word lengths of up to 20 bits (at $f_{sys} = 256f_s$).
- LSB fixed serial format with data word lengths of 16, 18 and 20 bits (at $f_{sys} = 384f_s$). As this format idles on the MSB it is necessary to know how many bits are being transmitted.

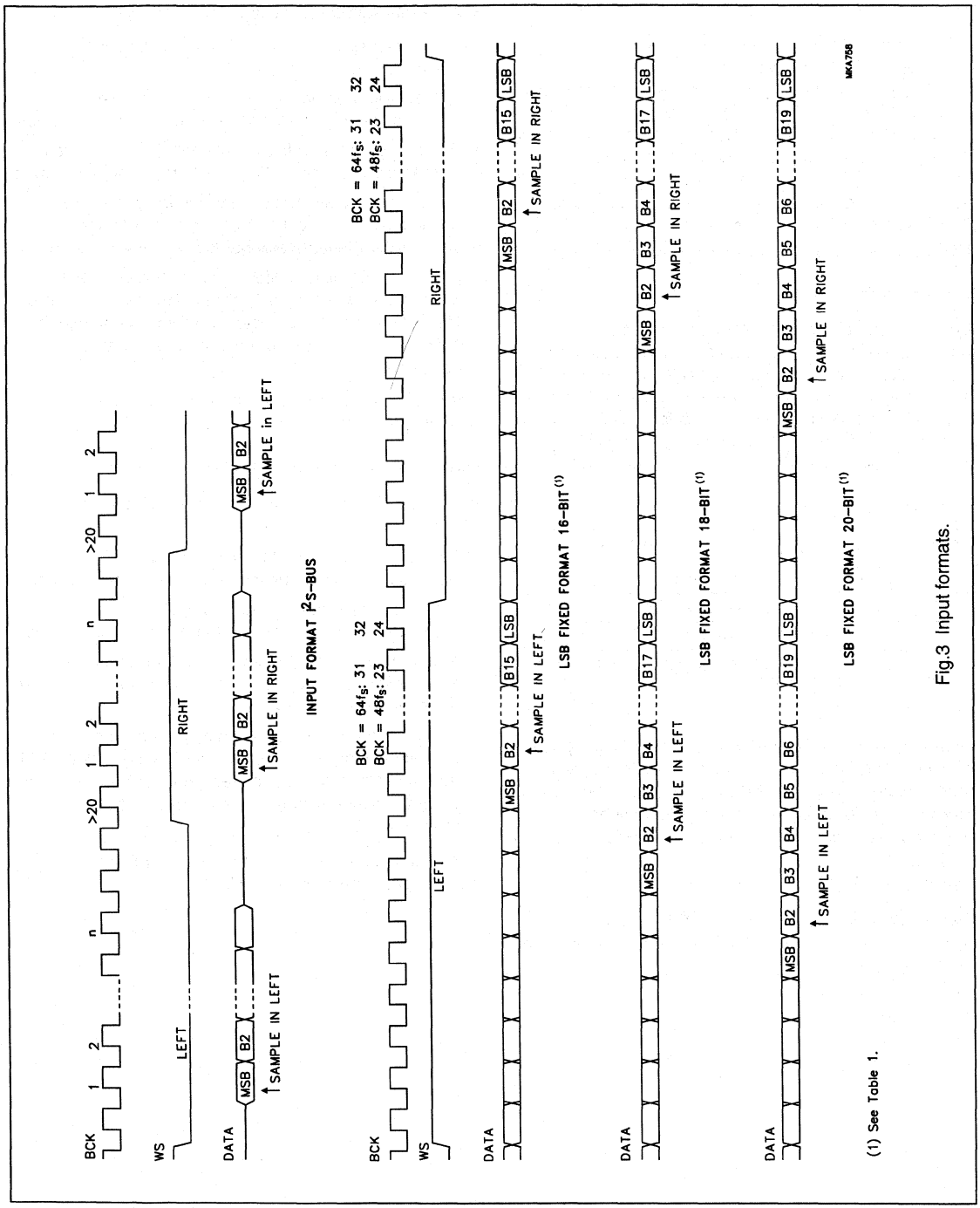
The input format is shown in Fig.3. Left and right data-channel words are time-multiplexed.

Table 1 Data input format and system clock.

TEST1	CLKS1	CLKS2	DATA INPUT FORMAT	SYSTEM CLOCK	DATA CLOCK(1)	SYSCLKO
0	0	0	I^2S up to 20 bits	$256f_s$	>20	$256f_s$
0	0	1	LSB fixed 16 bits	$384f_s$	24	$384f_s$
0	1	0	LSB fixed 18 bits	$384f_s$	24	$384f_s$
0	1	1	LSB fixed 20 bits	$384f_s$	24	$384f_s$
1	0	0	reserved	–	–	–
1	0	1	LSB fixed 16 bits	$384f_s$	32	$384f_s$
1	1	0	LSB fixed 18 bits	$384f_s$	32	$384f_s$
1	1	1	LSB fixed 20 bits	$384f_s$	32	$384f_s$

Note

1. Number of clock pulses within half an audio sample.



(1) See Table 1.

Fig.3 Input formats.

Mute

Soft mute is controlled by the $\overline{MUSB}$ at pin 9. When the input is active LOW the value of the samples is decreased smoothly to zero following a cosine curve. To step down the value of the data 32 coefficients are used, each one being used 31 times before stepping onto the next. When MUTE is released (pin 19 = HIGH), the samples are returned to the full level again following a cosine curve with the same coefficients being used in the reverse order. Mute is synchronized to prevent operation in the middle of a word.

De-emphasis

A digital de-emphasis is implemented for three sample rates (32, 44.1 and 48 kHz). By selecting DEEM1 and DEEM2 de-emphasis can be applied by means of a FIR filter. Time constants of the de-emphasis are 50 µs and 15 µs. De-emphasis is synchronized to prevent operation in the middle of a word. The de-emphasis deviation from ideal 50 µs and 15 µs de-emphasis is given in Table 4.

Table 2 De-emphasis.

DEEM1	DEEM2	CONDITION
0	0	de-emphasis disabled
0	1	de-emphasis for f_s = 32 kHz
1	0	de-emphasis for f_s = 4.1 kHz
1	1	de-emphasis for f_s = 48 kHz

Attenuation

Attenuation is controlled by the $\overline{ATSB}$ input (pin 21). When the input is active LOW the sample is multiplied by a coefficient that provides 12 dB attenuation. If the input is HIGH the multiplication factor is 1. Attenuation is synchronized to prevent operation in the middle of a word.

Double-speed mode

Double speed is controlled by the $\overline{DSMB}$ input (pin 20). When the input is active LOW the device operates in the double-speed mode.

Oversampling filter (normal-speed mode)

In the normal-speed mode the oversampling filter consists of:

- A 91st order half-band low-pass FIR filter which increases the oversampling rate from 1 time to 2 times.
- A 23rd order quarter band low-pass FIR filter which increases the oversampling rate from 2 times to 8 times.
- A linear interpolation section which increases the oversampling rate to 16 times. This removes the spectral components around $8f_s$.
- A sample-and-hold section which provides another 6 times oversampling to 96 times. The zero-order hold characteristic of this sample-and-hold section plus the 1st order analog filtering remove the spectral components around $16f_s$.

Pass-band ripple and stop-band attenuation for normal-speed are given in Table 3.

Oversampling filter (double-speed mode)

In the double-speed mode the oversampling filter consists of:

- A 51st order half-band low-pass FIR filter which increases the oversampling rate from 1 time to 2 times.
- A 7th order half-band low-pass FIR filter which increases the oversampling rate from 2 times to 4 times.
- A linear interpolation section which increases the oversampling rate to 8 times. This removes the spectral components around $4f_s$.
- A sample-and-hold section which provides another 6 times oversampling to 48 times. The zero-order hold characteristic of this sample-and-hold section plus the 1st order analog filtering remove the spectral components around $8f_s$.

Pass-band ripple and stop-band attenuation for double-speed are given in Table 3.

Noise shaper

In the normal speed mode the 2nd order digital noise shaper operates at $96f_s$ ($f_{sys} = 384f_s$) or $128f_s$ ($f_{sys} = 256f_s$). The digital noise shaper operates at $48f_s$ ($f_{sys} = 384f_s$) or $64f_s$ ($f_{sys} = 256f_s$) in double-speed mode. It shifts in-band quantization noise to frequencies well above the audio band. This noise shaping technique used in combination with a special data coding enables extremely high signal-to-noise ratios to be achieved. The noise shaper outputs a 5-bit pulse duration modulation (PDM) bitstream signal to the DAC.

Continuous calibration DAC

The dual 5-bit DAC uses the continuous calibration technique. This method, based on charge storage, involves exact duplication of a single reference current source. In the TDA1305T, 32 such current sources plus 1 spare source are continuously calibrated. The spare source is included to allow continuous converter operation.

The DAC receives a 5-bit data bitstream from the noise shaper. This data is then converted so that only small currents are switched to the output during digital silence (input 00000H). Using this technique extremely high signal-to-noise performance is achieved.

Operational amplifiers

High precision, low-noise amplifiers together with the internal conversion resistors R_{CONV1} and R_{CONV2} convert the converter output current to a voltage capable of driving a line output. This voltage is available at VOL and VOR (1.5 V RMS typical).

Connecting external capacitors CEXT1 and CEXT2 between FILTCL and VOL and between FILTCR and VOR respectively provides the required 1st order post filtering for the left and right channels (see Fig.1). The combinations of R_{CONV1} with CEXT1 and R_{CONV2} with CEXT2 determine the 1st order fall-off frequencies.

Internal reference circuitry

Internal reference circuitry ensures that the output voltage signal is proportional to the supply voltage, thereby maintaining maximum dynamic range for supply voltages from 3.4 to 5.5 V and making the circuit also suitable for battery-powered applications.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDD}	digital supply voltage		–	7.0	V
V_{DDA}	analog supply voltage		–	7.0	V
V_{DDO}	operational amplifier supply voltage		–	7.0	V
T_{xtal}	maximum crystal temperature		–	+150	°C
T_{stg}	storage temperature		−65	+150	°C
T_{amb}	ambient operating temperature		−30	+85	°C
V_{es}	electrostatic handling	note 1	−2000	+2000	V
		note 2	−200	+200	V

Notes

1. Human body model; C = 100 pF, R = 1500 Ω, V = 2000 V, 3 pulses positive and 3 pulses negative.
2. Machine model; C = 200 pF, R = 10 Ω, L = 0.5 μH.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	75	K/W

QUALITY SPECIFICATION

In accordance with *"SNW-FQ-611E"*. The number of this quality specification can be found in the *"Quality Reference Handbook"*. The handbook can be ordered using the code 9398 510 63011.

DIGITAL CHARACTERISTICS

V_{DD} = 3.4 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDD}	digital supply voltage	note 1	3.4	5.0	5.5	V
I_{DDD}	digital supply current	V_{DDD} = 5 V; at code 00000H	–	30	40	mA
V_{DDA}	analog supply voltage	note 1	3.4	5.0	5.5	V
I_{DDA}	analog supply current	V_{DDA} = 5 V; at code 00000H	–	5.5	8	mA
V_{DDO}	operational amplifier supply voltage	note 1	3.4	5.0	5.5	V
I_{DDO}	operational amplifier supply current	V_{DDO} = 5 V; at code 00000H	–	6.5	9	mA
RR	ripple rejection to V_{DDA}	note 2	–	25	–	dB
System clock input						
f_{sys}	system frequency	$f_{sys} = 384f_s$	9.6	16.93	18.4	MHz
		$f_{sys} = 256f_s$	6.4	11.29	12.28	MHz
V_{IL}	LOW level input voltage	note 3	−0.5	–	$0.2V_{DD}$	V
V_{IH}	HIGH level input voltage	note 3	$0.8V_{DD}$	–	V_{DD} + 0.5	V
$\|I_{LI}\|$	input leakage current	note 4	–	–	10	µA
C_i	input capacitance		–	–	10	pF
T_{cy}	clock cycle time	$f_{sys} = 384f_s$	104	59.1	54.2	ns
		$f_{sys} = 256f_s$	156	88.6	81.3	ns
Digital inputs; WS, BCK, DATA, $\overline{\text{DSMB}}$, $\overline{\text{MUSB}}$, DEEM1, DEEM2, $\overline{\text{ATSB}}$, CLKS1, CLKS2, TEST1 and TEST2						
V_{IL}	LOW level input voltage	note 3	−0.5	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage	note 3	$0.7V_{DD}$	–	V_{DD} + 0.5	V
$\|I_{LI}\|$	input leakage current	note 4	–	–	10	µA
C_i	input capacitance		–	–	10	pF
Digital output; CDEC						
V_{OL}	LOW level output voltage	I_{OL} = 0.4 mA	0	–	0.5	V
V_{OH}	HIGH level output voltage	I_{OH} = −0.2 mA	V_{DD} − 0.5	–	V_{DD}	V
t_r	output rise time	note 5	–	–	20	ns
t_f	output fall time	note 5	–	–	20	ns
C_L	load capacitance		–	–	30	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Serial input data timing (see Fig.4)						
f_{BCK}	bit-clock input (data input rate) frequency	$f_{sys} = 384f_s$	–	$48f_s$	–	MHz
		$f_{sys} = 256f_s$	–	$64f_s$	–	MHz
f_{WS}	word select input frequency	normal speed	25	44.1	48	kHz
		double speed	50	88.2	96	kHz
t_r	rise time		–	–	20	ns
t_f	fall time		–	–	20	ns
t_H	bit clock time HIGH		55	–	–	ns
t_L	bit clock time LOW		55	–	–	ns
t_{su}	data set-up time		40	–	–	ns
t_h	data hold time		10	–	–	ns
t_{suWS}	word select set-up time		40	–	–	ns
t_{hWS}	word select hold time		10	–	–	ns

Notes

1. All V_{DD} and V_{SS} pins must be connected externally to the same supply.
2. V_{ripple} = 1% of supply voltage; f_{ripple} = 100 Hz. Ripple rejection RR to V_{DDA} is dependent on the value of the external capacitor (C_{EXT3} in Fig.1) connected to V_{ref}. The value here assumes that C_{EXT3} = 1 µF.
3. Minimum V_{IL} and maximum V_{IH} are peak values to allow for transients.
4. I_{LImni} measured at V_I = 0 V; I_{LImax} measured at V_I = 5.5 V.
5. Reference levels = 10% and 90%.

ANALOG CHARACTERISTICS

$V_{DD} = V_{DDA} = V_{DDO}$ = 5 V; V_{SS} = 0 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reference values						
V_{ref}	reference voltage level		2.45	2.5	2.55	V
R_{CONV}	current-to-voltage conversion resistor		1.6	2.2	2.8	kΩ
Analog outputs						
RES	resolution		–	–	18	bit
$V_{FS(rms)}$	full-scale output voltage (pins 23 and 25) (RMS value)		1.425	1.5	1.575	V
V_{OFF}	output voltage DC offset with respect to reference voltage level V_{ref}		–80	–65	–50	mV
TC_{FS}	full scale temperature coefficient		–	$\pm 100 \times 10^{-6}$	–	

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB input level; note 1	–	–90	–81	dB
			–	0.003	0.009	%
		at –60 dB input level; note 2	–	–44	–40	dB
			–	0.63	1.0	%
		at –60 dB input level; A-weighted; note 3	–	–46	–	dB
			–	0.5	–	%
		at 0 dB input level; (20 Hz to 20 kHz); note 4	–	–90	–81	dB
			–	0.003	0.003	%
S/N	signal-to-noise ratio at bipolar zero	A weighted; at code (00000H)	100	108	–	dB
α_{cs}	channel separation		85	100	–	dB
$\lvert\delta V_O\rvert$	unbalance between outputs		–	0.2	0.3	dB
$\lvert Z_O\rvert$	dynamic output impedance		–	10	–	Ω
R_L	output load resistance		3	–	–	kΩ
C_L	output load capacitance		–	–	200	pF

Notes

1. Measured with a 1 kHz, 0 dB, 18-bit sine wave generated at a sampling rate of 48 kHz. The (THD + N)/S measured over a bandwidth of 20 Hz to 20 kHz.
2. Measured with a 1 kHz, -60 dB, 18-bit sine wave generated at a sampling rate of 48 kHz. The (THD + N)/S measured over a bandwidth of 20 Hz to 20 kHz. For 16-bit input signals, the performance is limited to the theoretical maximum.
3. Measured with a 1 kHz, -60 dB, 18-bit sine wave generated at a sampling rate of 48 kHz. The (THD + N)/S measured over a bandwidth of 20 Hz to 20 kHz and filtered with a A-weighted characteristic. For 16-bit input signals, the performance is limited to the theoretical maximum.
4. Measured with a sine wave from 20 Hz to 20 kHz generated at a sampling rate of 48 kHz. The (THD + N)/S measured over a bandwidth of 20 Hz to 20 kHz.

TEST AND APPLICATION INFORMATION

Filter characteristics (theoretical values)

Table 3 Normal speed filter characteristics.

ITEM	SAMPLE FREQUENCY	RANGE	CONDITIONS	CHARACTERISTICS
Pass band	44.1 kHz	0 to 20 kHz		0 ±0.025 dB
	32 kHz	14.5 to 15 kHz		–0.15 dB (min.)
Stop band	44.1 kHz	24.1 to 150 kHz	typical	–60 dB (max.)
			worst case	–57 dB (max.)
		150 kHz to infinity	typical	–57 dB (max.)
			worst case	–47 dB (max.)
	32 kHz	17 to 17.5 kHz		–40 dB (max.)

De-emphasis filter characteristics (theoretical values)

Table 4 De-emphasis deviation from ideal 50 μs to 15 μs de-emphasis network.

ITEM	SAMPLE FREQUENCY	RANGE	CHARACTERISTICS
Gain deviation	44.1 and 48 kHz	0 to 18 kHz	0 ±0.05 dB
		18 to 20 kHz	0.12 dB (max.)
	32 kHz	0 to 13 kHz	0 ±0.06 dB
		13 to 15 kHz	0.22 dB (max.)
Phase deviation	44.1 and 48 kHz	0 to 15 kHz	10 deg (max.)
		15 to 20 kHz	15 deg (max.)
	32 kHz	0 to 9 kHz	10 deg (max.)
		9 to 15 kHz	16 deg (max.)

Double-speed characteristics

Table 5 Double-speed filter characteristics.

ITEM	RANGE	CONDITIONS	CHARACTERISTICS
Pass band	0 to 17 kHz		0 ±0.075 dB
	17 to 20 kHz		−0.3 dB (min.)
Stop band	24.1 to 150 kHz	typical	−47 dB (max.)
		worst case	−45 dB (max.)
	150 kHz to infinite	typical	−33 dB (max.)
		worst case	−25 dB (max.)

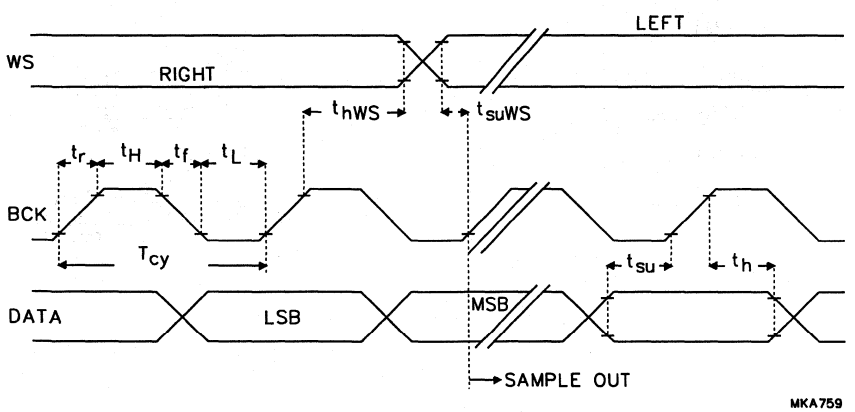


Fig.4 Timing of input signals.

APPLICATION INFORMATION

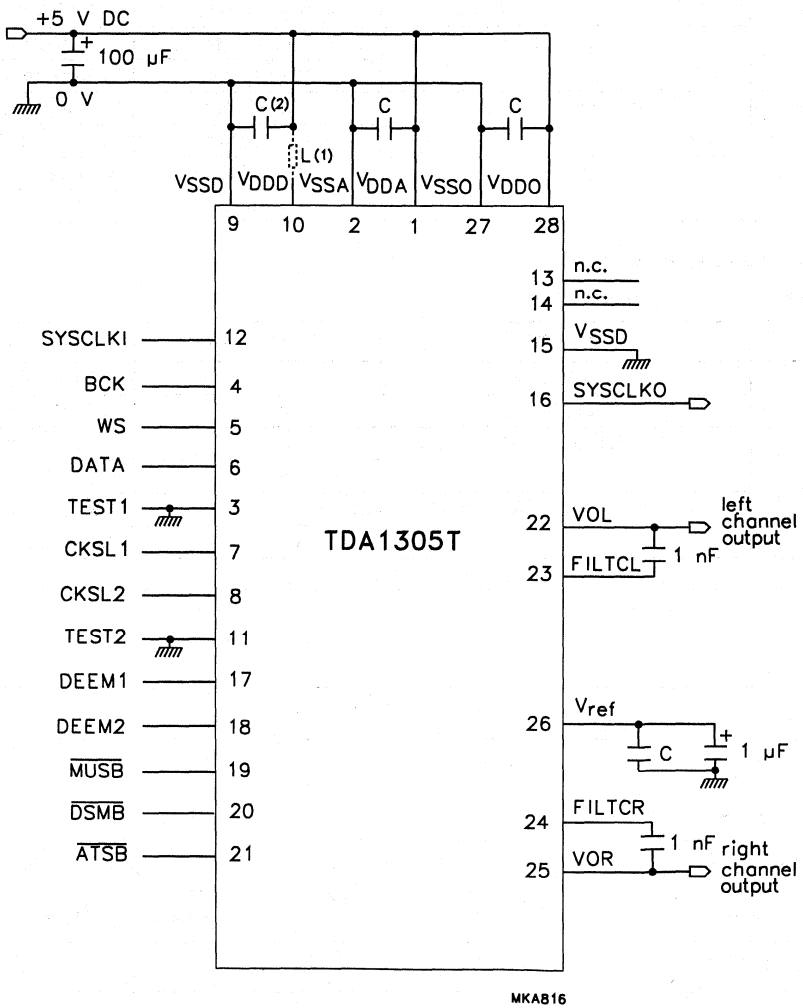
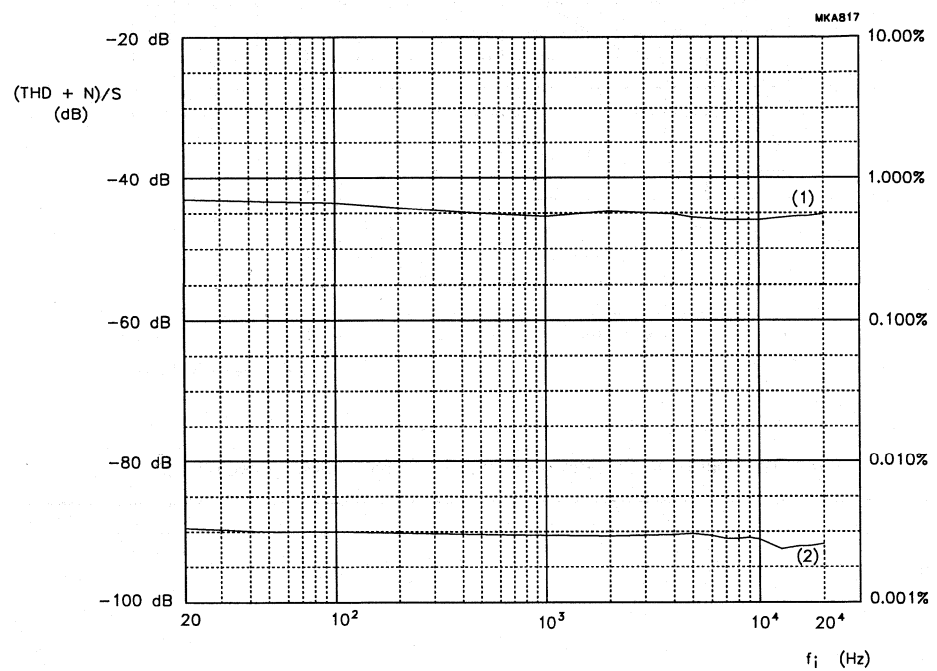


Fig.5 Application diagram.

A typical application diagram is illustrated in Fig.5. The left and right channel outputs can drive a line output directly. The series inductor (L) in the digital supply line, though not strictly necessary, helps to reduce crosstalk between the digital and analog circuits.

In Fig.6 measurements were taken with an 18-bit sine wave generated at a sampling rate of 48 kHz. The (THD + N)/S was measured over a bandwidth of 20 Hz to 20 kHz. The graph was constructed from average measurement values of a small amount of engineering samples. No guarantee for typical values is implied.

In Fig.6 measurements were taken with an 18-bit sine wave generated at a sampling rate of 48 kHz. The (THD + N)/S was measured over a bandwidth of 20 Hz to 20 kHz and filtered with A-weighted characteristics. The graph was constructed from average measurement values of a small amount of engineering samples. No guarantee for typical values is implied.



(1) Level = −60 dB.
(2) Level = 0 dB.

Fig.6 Total harmonic distortion as a function of signal frequency.

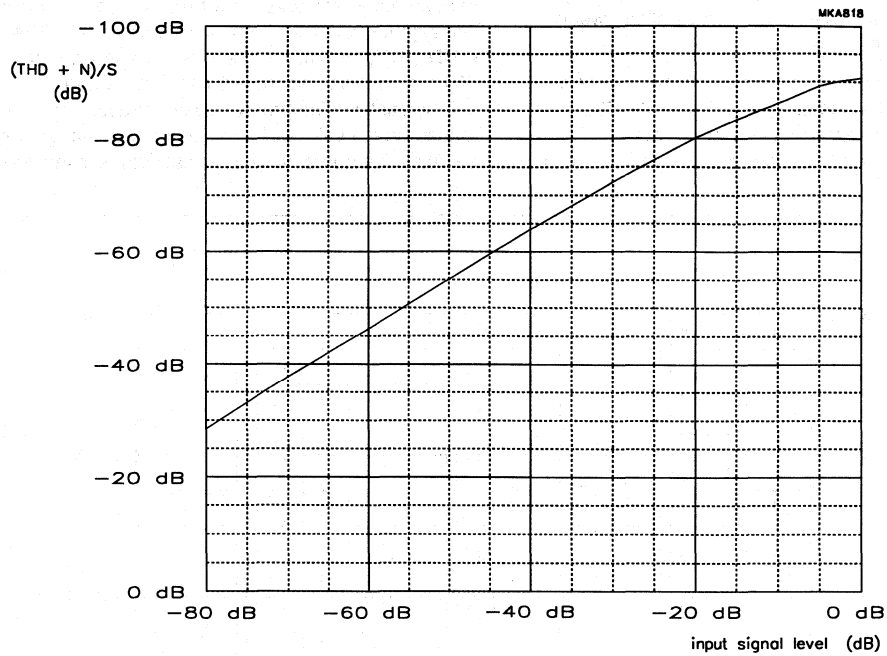


Fig.7 Total harmonic distortion as a function of signal level; (A-weighted).

Noise shaping filter DAC TDA1306T

FEATURES

General

- Double-speed mode
- Digital volume control
- Soft mute function
- 12 dB attenuation
- Low power dissipation
- Digital de-emphasis
- TDA1305T pin compatible.

Easy application

- Voltage output
- Only 1st-order analog post-filtering required
- Operational amplifiers and digital filter integrated
- Selectable system clock (f_{sys}) $256f_s$ or $384f_s$
- I^2S-bus ($f_{sys} = 256f_s$) or 16, 18 or 20 bits LSB fixed serial input format ($f_{sys} = 384f_s$).
- Single rail supply.

High performance

- Superior signal-to-noise ratio
- Wide dynamic range
- No zero crossing distortion
- Inherently monotonic
- Continuous calibration digital-to-analog conversion combined with noise shaping technique.

GENERAL DESCRIPTION

The TDA1306T is a dual CMOS digital-to-analog converter with up-sampling filter and noise shaper. The combination of oversampling up to $4f_s$, noise shaping and continuous calibration conversion ensures that only simple 1st-order analog post-filtering is required.

The TDA1306T supports the I^2S-bus data input mode ($f_{sys} = 256f_s$) with word lengths of up to 20 bits and the LSB fixed serial data input format ($f_{sys} = 384f_s$) with word lengths of 16, 18 or 20 bits. Two cascaded IIR filters increase the sampling rate 4 times.

The DACs are of the continuous calibration type and incorporate a special data coding. This ensures a high signal-to-noise ratio, wide dynamic range and immunity to process variation and component ageing.

Two on-board operational amplifiers convert the digital-to-analog current to an output voltage.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1306T	SO24	plastic small outline package; 24 leads; body width 7.5 mm.	SOT137–1

QUICK REFERENCE DATA

All power supply pins V_{DD} and V_{SS} must be connected to the same external supply unit.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
V_{DDO}	operational amplifier supply voltage		4.5	5.0	5.5	V
I_{DDD}	digital supply current	V_{DDD} = 5 V; at code 00000H	–	5	8	mA
I_{DDA}	analog supply current	V_{DDA} = 5 V; at code 00000H	–	3	5	mA
I_{DDO}	operational amplifier supply current	V_{DDO} = 5 V; at code 00000H	–	2	4	mA
Analog signals						
$V_{FS(rms)}$	full-scale output voltage (RMS value)	$V_{DDD} = V_{DDA} = V_{DDO}$ = 5 V; R_L > 5 kΩ	0.935	1.1	1.265	V
R_L	output load resistance		5	–	–	kΩ
DAC performance						
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB signal level; f_i = 1 kHz;	–	–70	–	dB
			–	0.032	–	%
		at –60 dB signal level; f_i = 1 kHz;	–	–42	–32	dB
			–	0.8	2.5	%
S/N_{ds}	signal-to-noise ratio at digital silence	no signal; A-weighted	–	–108	–96	dB
BR	input bit rate at data input	f_s = 44.1 kHz; normal speed	–	–	2.822	Mbits/s
		f_s = 44.1 kHz; double speed	–	–	5.645	Mbits/s
f_{sys}	system clock frequency (pin 12)		6.4	–	18.432	MHz
T_{amb}	operating ambient temperature		–40	–	+85	°C

BLOCK DIAGRAM

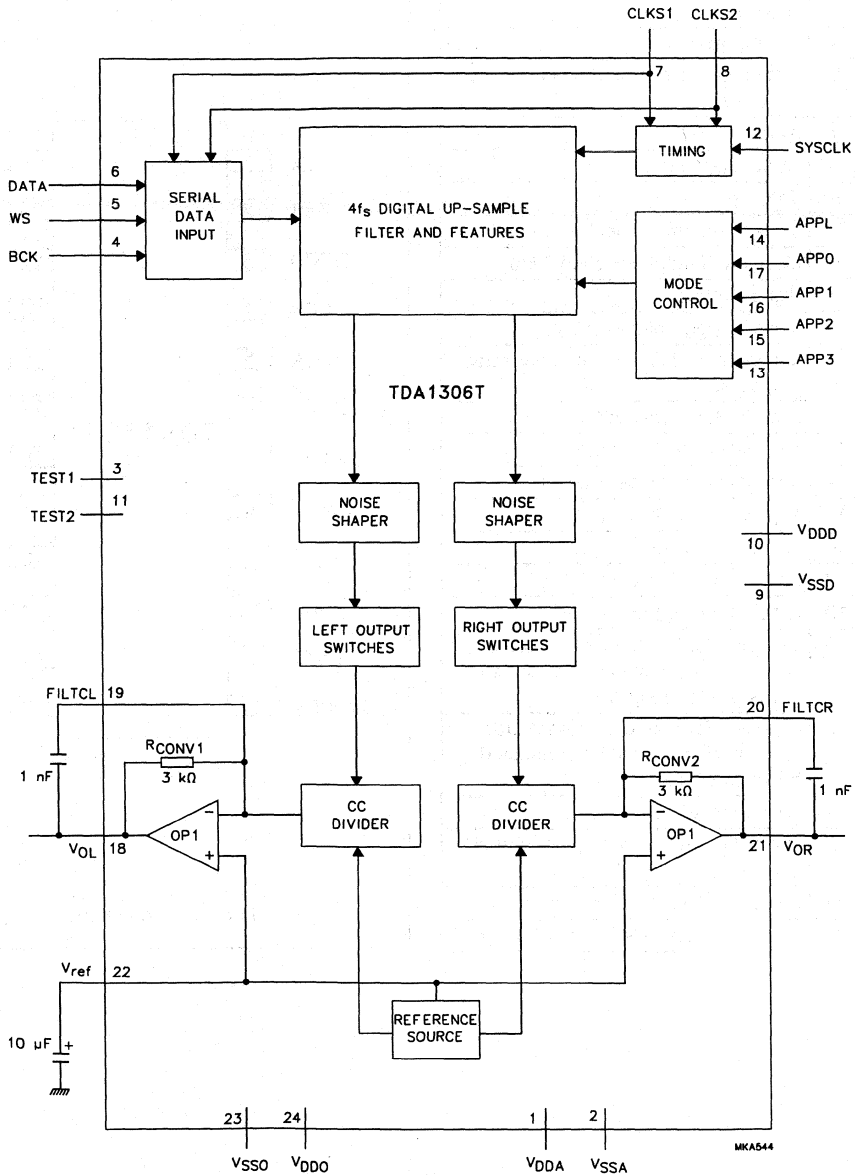


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{DDA}	1	analog supply voltage (+5 V)
V_{SSA}	2	analog ground
TEST1	3	test input 1; pin should be connected to ground
BCK	4	bit clock input
WS	5	word select input
DATA	6	data input
CLKS1	7	clock and format selection 1 input
CLKS2	8	clock and format selection 2 input
V_{SSD}	9	digital ground
V_{DDD}	10	digital supply voltage (+5 V)
TEST2	11	test input 2; pin should be connected to ground
SYSCLK	12	system clock input $256f_s$ or $384f_s$
APP3	13	application mode 3 input
APPL	14	application mode selection input
APP2	15	application mode 2 input
APP1	16	application mode 1 input
APP0	17	application mode 0 input
V_{OL}	18	left channel output
FILTCL	19	capacitor for left channel 1st order filter function; should be connected between pins 19 and 18
FILTCR	20	capacitor for right channel 1st order filter function; should be connected between pins 20 and 21
V_{OR}	21	right channel output
V_{ref}	22	internal reference voltage for output channels; $0.5V_{DDO}$ (typ.)
V_{SSO}	23	operational amplifier ground
V_{DDO}	24	operational amplifier supply voltage

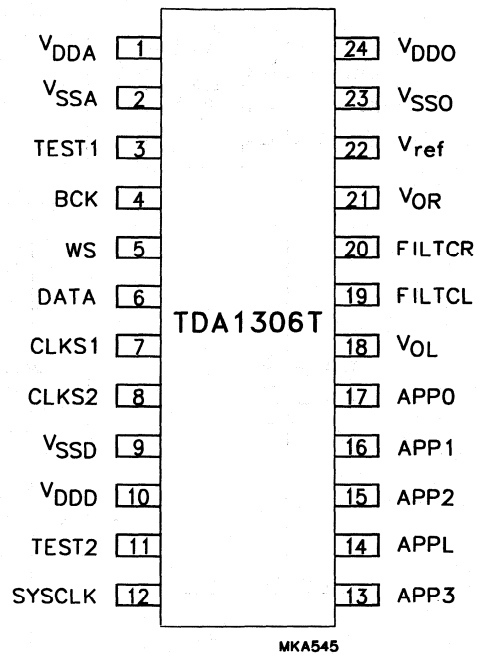


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA1306T CMOS DAC incorporates an up-sampling filter, a noise shaper, continuous calibrated current sources and operational amplifiers.

System clock and data input format

The TDA1306T accommodates slave mode only. Consequently, in all applications, the system devices must provide the system clock. The system frequency is selectable at pins CLKS1 and CLKS2 (see Table 1).

The TDA1306T supports the following data input modes:

- I^2S-bus with data word length of up to 20 bits ($f_{sys} = 256f_s$)
- LSB fixed serial format with data word length of 16, 18 or 20 bits ($f_{sys} = 384f_s$). As this format idles on the MSB it is necessary to know how many bits are being transmitted.

The input formats are illustrated in Fig.9. Left and right data channel words are time multiplexed.

Table 1 Data input format and system clock.

CLKS1	CLKS2	DATA INPUT FORMAT	SYSTEM CLOCK	
			NORMAL SPEED	DOUBLE SPEED
0	0	I^2S-bus	$256f_s$	$128f_s$
0	1	LSB fixed 16 bits	$384f_s$	$192f_s$
1	0	LSB fixed 18 bits	$384f_s$	$192f_s$
1	1	LSB fixed 20 bits	$384f_s$	$192f_s$

Device operation

When the APPL pin is held HIGH and APP3 is held LOW, pins APP0, APP1 and APP2 form a microcontroller interface. When the APPL pin is held LOW, pins APP0, APP1, APP2 and APP3 form a pseudo-static application (TDA1305T pin compatible).

PSEUDO-STATIC APPLICATION MODE (APPL = LOGIC 0)

In this mode, the device operation is controlled by pseudo-static application pins where:

APP0 = attenuation mode control

APP1 = double-speed mode control

APP2 = mute mode control

APP3 = de-emphasis mode control.

In the pseudo-static application mode the TDA1306T is pin compatible with the TDA1305T slave mode. The correspondence between TDA1306T pin number, TDA1306T pin name, TDA1305T pin mnemonic and a description of the effects is given in Table 2.

Table 2 Pseudo-static application mode.

PIN MNEMONIC	PIN NUMBER	TDA1305T FUNCTION	VALUE	DESCRIPTION
APP0	17	ATSB	0	12 dB attenuation (from full scale) activated (only if MUSB = logic 1)
			1	full scale (only if MUSB = logic 1)
APP1	16	DSMB	0	double-speed mode
			1	normal-speed mode
APP2	15	MUSB	0	samples decrease to mute level
			1	level according to ATSB
APP3	13	DEEM1	0	de-emphasis OFF (44.1 kHz)
			1	de-emphasis ON (44.1 kHz)

MICROCONTROLLER APPLICATION MODE (APPL = LOGIC 1, APP3 = LOGIC 0).

In this mode, the device operation is controlled by a set of flags in an 8-bit mode control register. The 8-bit mode control register is written by a microcontroller interface where:

APPL = logic 1

APP0 = Data

APP1 = Clock

APP2 = RAB

APP3 = logic 0.

The correspondence between serial-to-parallel conversion, mode control flags and a summary of the effect of the control flags is given in Table 3. Figures 3 and 4 illustrate the mode set timing.

MICROCONTROLLER WRITE OPERATION SEQUENCE

The microcontroller write operation follows the following sequence:

- APP2 is held LOW by the microcontroller
- Microcontroller data is clocked into the internal shift register on the LOW-to-HIGH transition on pin APP1
- Data D7 to D0 is latched into the appropriate control register on the LOW-to-HIGH transition of pin APP2 (APP1 = HIGH)
- If more data is clocked into the TDA1306T before the LOW-to-HIGH transition on pin APP2 then only the last 8 bits are used
- If less data is clocked into the TDA1306T unpredictable operation will result
- If the LOW-to-HIGH transition of pin APP2 occurs when APP1 = LOW, the command will be disregarded.

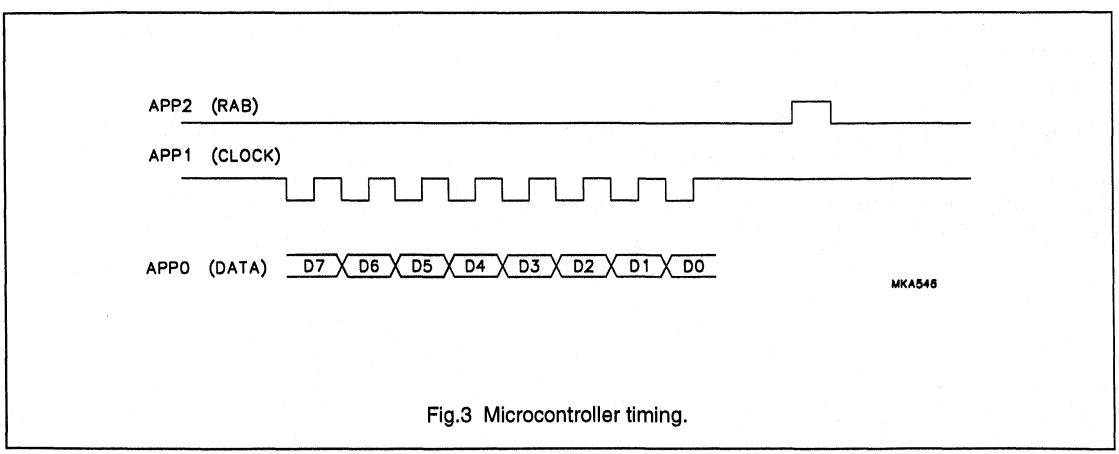


Fig.3 Microcontroller timing.

MICROCONTROLLER WRITE OPERATION SEQUENCE (REPEAT MODE)

The same command can be repeated several times (e.g. for fade function) by applying APP2 pulses as shown in Fig.4. It should be noted that APP1 must stay HIGH between APP2 pulses. A minimum pause of 22 ms is necessary between any two step-up or step-down commands.

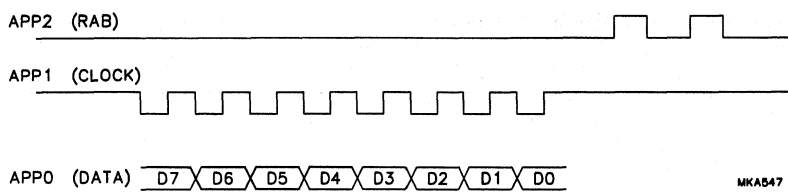


Fig.4 Microcontroller timing (repeat mode).

Table 3 Microcontroller mode control register.

BIT POSITION	FUNCTION	DESCRIPTION	ACTIVE LEVEL
D7	ATSB	12 dB attenuation (from full scale)	LOW
D6	DSMB	double speed	LOW
D5	MUSB	mute	LOW
D4	DEEM	de-emphasis	HIGH
D3	FS	full scale	HIGH
D2	INCR	increment	HIGH
D1	DECR	decrement	HIGH
D0	not applicable	reserved	not applicable

Volume control

A digital level control is incorporated in the TDA1306T which performs the function of soft mute and attenuation (pseudo-static application mode) or soft mute, attenuation, fade, increment and decrement (microcontroller application mode). The volume control of both channels can be varied in small step changes determined by the value of the internal fade counter where:

audio level = counter × maximum level/120,

where the counter is a 7-bit binary number between 0 and 120. The time taken for mute to vary from 120 to 0 is $1/120f_s$. For example, when f_s = 44.1 kHz, the time taken is approximately 3 ms.

VOLUME CONTROL (PSEUDO-STATIC APPLICATION MODE)

In the pseudo-static application mode (APPL = logic 0) the digital audio output level is controlled by APP0 (attenuation) and APP2 (mute) so only the final volume levels full scale, 12 dB (attenuate) and mute (–infinity dB) can be selected. The mute function has priority over the attenuation function. Accordingly, if MUSB is LOW, the state of ATSB has no effect. An example of volume control in this application mode is illustrated in Fig.5.

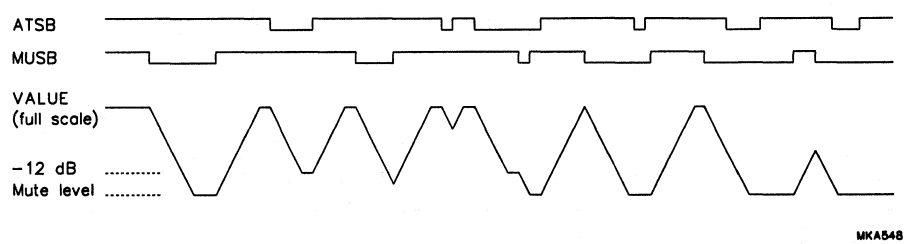


Fig.5 Volume control (pseudo-static application mode).

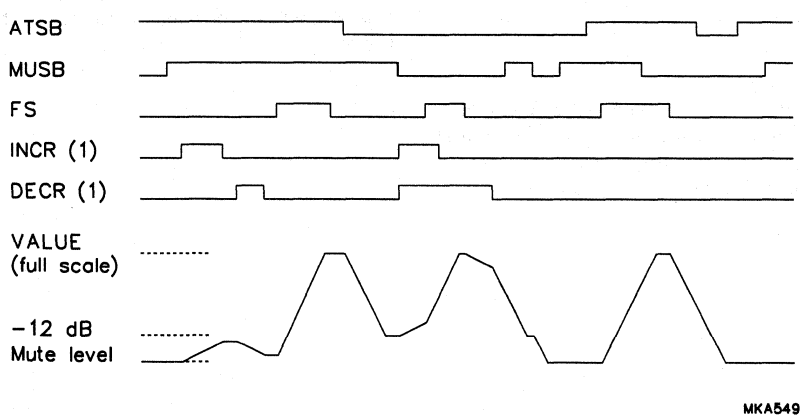
VOLUME CONTROL (MICROCONTROLLER APPLICATION MODE)

In the microcontroller application mode (APPL = logic 1, APP3 = logic 0) the audio output level is controlled by volume control bits ATSB, MUSB, FS, INCR and DECR.

Mute is activated by sending the MUSB command to the mode control register via the microcontroller interface. The audio output level will be reduced to zero in a maximum of 120 steps (depending on the current position of the fade counter) and taking a maximum of 3 ms. Mute, attenuation and full scale are synchronized to prevent operation in the middle of a word.

- The counter is preset to 120 by the full scale command.
- The counter is preset to 30 by the attenuate command when its value is more then 30. If the value of the counter is less than 30 dB the ATSB command has no effect.
- The counter is preset to logic 0 by the mute command MUSB.
- Attenuation (−12 dB) is activated by sending the ATSB command to the fade control register (D7).
- Attenuation and mute are cancelled by sending the full-scale command to the fade control register (Register D3).

To control the fade counter in a continuous way, the INCREMENT and DECREMENT commands are available (fade control Registers D1 and D2). They will increment and decrement the counter by 1 for each register write operation. When issuing more than 1 step-up or step-down command in sequence, the write repeat mode may be used (see microcontroller application mode). An example of volume control in this application mode is illustrated in Fig.6.



(1) INCR and DECR in repeat mode.

Fig.6 Volume control (microcontroller application mode).

There are two recommended application situations within the microcontroller mode:

- The customer wants to use the microcontroller interface without the volume setting facility. In this event the operation is as follows:
  - Mute ON; by sending the MUSB command
  - Mute OFF; by sending the FS command
  - Attenuation ON; by sending the ATSB command
  - Attenuation OFF; by sending the FS command.

  It is possible to switch from 'Attenuation ON' to 'Mute ON' but not vice-versa.
- Incorporating the volume control feature operates as follows:
  - Mute ON; by sending the MUSB command the microcontroller has to store the previous volume setting
  - Mute OFF; by sending succeeding INCR commands until the previous volume is reached
  - Attenuation ON; by sending succeeding DECR commands until a relative downstep of –12 dB is reached. The microcontroller has to store the previous volume
  - Attenuation OFF; by sending the succeeding INCR commands until the previous volume is reached
  - Volume UP; by sending succeeding INCR commands
  - Volume DOWN; by sending succeeding DECR commands.

De-emphasis

A digital de-emphasis is implemented in the TDA1306T. By selecting the DEEM bit at register D4 (microcontroller application mode) or activating the APP3 pin (pseudo-static application mode), de-emphasis can be applied by means of an IIR filter. De-emphasis is synchronized to prevent operation in the middle of a word.

Double-speed mode

The double-speed mode is controlled by the DSMB bit at register D6 (microcontroller application mode) or by activating the APP1 pin (pseudo-static application mode). When the control bit is active LOW the device operates in the double-speed mode.

Oversampling filter and noise shaper

The digital filter is a four times oversampling filter. It consists of two sections which each increase the sample rate by 2. The noise-shaper operates on $4f_s$ and reduces the in-band noise density.

DAC and operational amplifiers

In this noise shaping filter DAC a special data code and bidirectional current sources are used in order to achieve true low-noise performance. The special data code guarantees that only small values of current flow to the output during small signal passages while larger positive or negative values are generated using the bidirectional current sources. The noise shaping filter-DAC uses the continuous calibration conversion technique.

The operational amplifiers and the internal conversion resistors R_{CONV1} and R_{CONV2} convert the DAC current to an output voltage available at V_{OL} and V_{OR}. Connecting an external capacitor between FILTCL and V_{OL}, FILTCR and V_{OR} respectively provides the required 1st-order post filtering.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage	note 1	–	7.0	V
T_{xtal}	maximum crystal temperature		–	+150	°C
T_{stg}	storage temperature		−65	+125	°C
T_{amb}	operating ambient temperature		−40	+85	°C
V_{es}	electrostatic handling	note 2	−2000	+2000	V
		note 3	−200	+200	V

Notes

1. All V_{DD} and V_{SS} connections must be made to the same power supply.
2. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor.
3. Equivalent to discharging a 200 pF capacitor via a 2.5 mH series inductor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	69	K/W

QUALITY SPECIFICATION

In accordance with *"UZW-BO/FQ-0601"*. The numbers of the quality specification can be found in the *"Quality Reference Handbook"*. The handbook can be ordered using the code 9398 510 63011.

DC CHARACTERISTICS

$V_{DDD} = V_{DDA} = V_{DDO} = 5$ V; $T_{amb} = 25$ °C; all voltages referenced to ground (pins 2, 9 and 23); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage (pin 10)	note 1	4.5	5.0	5.5	V
V_{DDA}	analog supply voltage (pin 1)	note 1	4.5	5.0	5.5	V
V_{DDO}	operational amplifier supply voltage (pin 24)	note 1	4.5	5.0	5.5	V
I_{DDD}	digital supply current	f_{sys} = 11.28 MHz	–	5	8	mA
I_{DDA}	analog supply current	at digital silence	–	3	6	mA
I_{DDO}	operational amplifier supply current	no operational amplifier load resistor	–	2	4	mA
P_{tot}	total power dissipation	f_{sys} = 11.28 MHz; digital silence; no operational amplifier load resistor	–	50	90	mW
V_{IH}	HIGH level digital input voltage (pins 3 to 8 and 11 to 17)		$0.7V_{DDD}$	–	V_{DDD} + 0.5	V
V_{IL}	LOW level digital input voltage (pins 3 to 8 and 11 to 17)		–0.5	–	$0.3V_{DDD}$	V
R_{pd}	internal pull-down resistor to V_{SSD} (pins 3 and 11)		17	–	134	kΩ
$\|I_{LI}\|$	input leakage current		–	–	10	μA
C_i	input capacitance		–	–	10	pF
V_{ref}	reference voltage (pin 22)	with respect to V_{SSO}	$0.45V_{DDO}$	$0.5V_{DDO}$	$0.55V_{DDO}$	V
R_{CONV}	current-to-voltage conversion resistor		2.4	3.0	3.6	kΩ
$V_{FS(rms)}$	full-scale output voltage (RMS value)	R_L > 5 kΩ; note 2	0.935	1.1	1.265	V
R_L	output load resistance		5	–	–	kΩ

Notes

1. All power supply pins (V_{DD} and V_{SS}) must be connected to the same external power supply unit.
2. R_L is the AC resistance of the external circuitry connected to the audio outputs of the application circuit.

AC CHARACTERISTICS (ANALOG)

$V_{DDD} = V_{DDA} = V_{DDO} = 5$ V; $T_{amb} = 25$ °C; all voltages referenced to ground (pins 2, 9 and 23); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DACs						
SVRR	supply voltage ripple rejection V_{DDA} and V_{DDO}	f_{ripple} = 1 kHz; V_{ripple} = 100 mV (p-p); C22 = 10 µF	–	40	–	dB
ΔG_v	unbalance between the 2 DAC voltage outputs (pins 18 and 21)	maximum volume	–	–	0.5	dB
α_{ct}	crosstalk between the 2 DAC voltage outputs (pins 18 and 21)	one output digital silence the other maximum volume	–	–110	–85	dB
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB signal level; f_i = 1 kHz	–	–70	–	dB
			–	0.032	–	%
		at –60 dB signal level; f_i = 1 kHz	–	–42	–32	dB
			–	0.8	2.5	%
S/N_{ds}	signal-to-noise ratio at digital silence	no signal; A-weighted	–	–108	–96	dB
Operational amplifiers						
G_v	open-loop voltage gain		–	85	–	dB
PSRR	power supply rejection ratio	f_{ripple} = 3 kHz; V_{ripple} = 100 mV (p-p); A-weighted	–	90	–	dB
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	$R_L > 5$ kΩ; f_i = 1 kHz; V_o = 2.8 V (p-p)	–	–100	–	dB
f_{UG}	unity gain frequency	open loop	–	4.5	–	MHz
$\lvert Z_o \rvert$	AC output impedance	$R_L > 5$ kΩ	–	1.5	150	Ω

AC CHARACTERISTICS (DIGITAL)

$V_{DDD} = V_{DDA} = V_{DDO}$ 4.5 to 5.5 V; all voltages referenced to ground (pins 2, 9 and 23); T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
T_{WX}	clock cycle time	$f_{sys} = 384f_s$; normal speed	54.2	59.1	104	ns
		$f_{sys} = 192f_s$; double speed	54.2	59.1	104	ns
		$f_{sys} = 256f_s$; normal speed	81.3	88.6	156	ns
		$f_{sys} = 128f_s$; double speed	81.3	88.6	156	ns
t_{CWL}	f_{sys} LOW level pulse width		22	–	–	ns
t_{CWH}	f_{sys} HIGH level pulse width		22	–	–	ns
Serial input data timing (see Fig.8)						
f_s	word select input audio sample frequency	normal speed	25	44.1	48	kHz
		double speed	50	88.2	96	kHz
f_{BCK}	clock input frequency (data input rate)	$f_{sys} = 384f_s$; normal speed; note 1	–	–	$64f_s$	kHz
		$f_{sys} = 192f_s$; double speed; note 1	–	–	$64f_s$	kHz
		$f_{sys} = 256f_s$; normal speed	–	–	$64f_s$	kHz
		$f_{sys} = 128f_s$; double speed; note 2	–	–	$48f_s$	kHz
t_r	rise time		–	–	20	ns
t_f	fall time		–	–	20	ns
t_H	bit clock HIGH time		55	–	–	ns
t_L	bit clock LOW time		55	–	–	ns
t_{su}	data set-up time		20	–	–	ns
t_h	data hold time		10	–	–	ns
t_{suWS}	word select set-up time		20	–	–	ns
t_{hWS}	word select hold time		10	–	–	ns
Microcontroller interface timing (see Fig.9)						
t_L	input LOW time		2	–	–	µs
t_H	Input HIGH time		2	–	–	µs
t_{suDC}	set-up time DATA to CLOCK		1	–	–	µs
t_{hCD}	hold time CLOCK to DATA		1	–	–	µs
t_{suCR}	set-up time CLOCK to RAB		1	–	–	µs

Notes

1. A clock frequency of up to $96f_s$ is possible in the event of a rising edge of BCK occurring during SYSCLK = LOW.
2. A clock frequency of up to $64f_s$ is possible in the event of a rising edge of BCK occurring during SYSCLK = LOW.

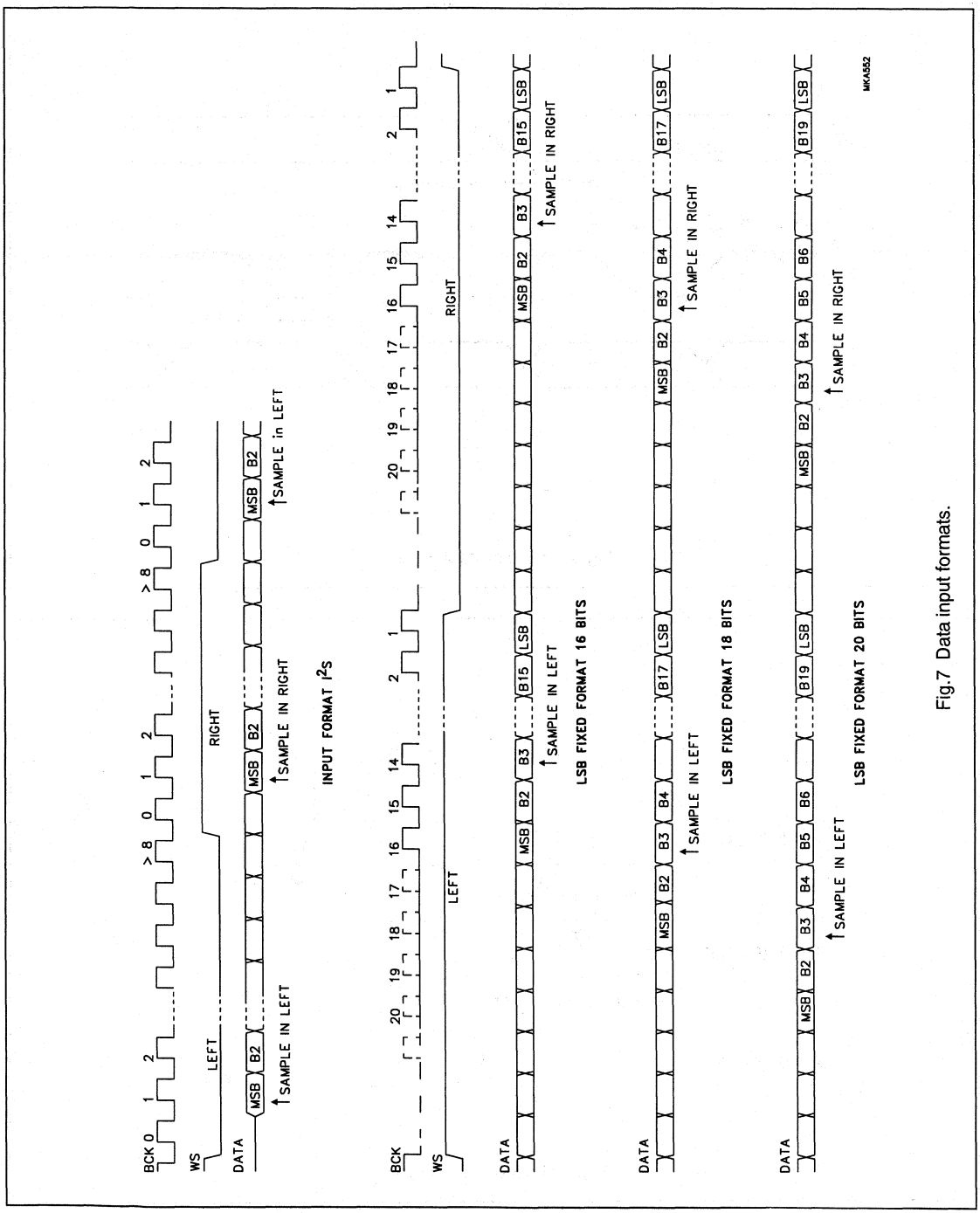


Fig.7 Data input formats.

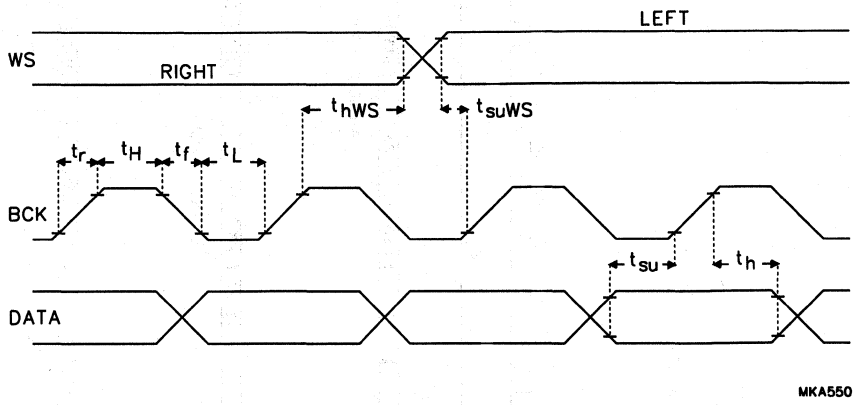


Fig.8 Timing of input signals.

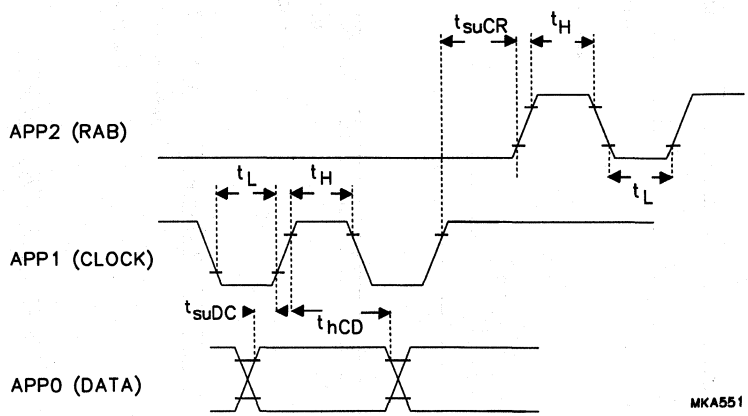


Fig.9 Microcontroller timing.

TEST AND APPLICATION INFORMATION

Filter characteristics

Table 4 Digital filter specification (f_s = 44.1 kHz).

BAND	ATTENUATION
0 to 19 kHz	< 0.001 dB
19 to 20 kHz	< 0.03 dB
24 kHz	> 25 dB
25 to 35 kHz	> 40 dB
35 to 64 kHz	> 50 dB
64 to 68 kHz	> 31 dB
68 kHz	> 35 dB
69 to 88 kHz	> 40 dB

Table 5 Digital filter phase distortion (f_s = 44.1 kHz).

BAND	PHASE DISTORTION
0 to 16 kHz	< ±1°

Class AB stereo headphone driver TDA1308

FEATURES

- Wide temperature range
- No switch ON/OFF clicks
- Excellent power supply ripple rejection
- Low power consumption
- Short-circuit resistant
- High performance
  - high signal-to-noise ratio
  - high slew rate
  - low distortion
- Large output voltage swing.

GENERAL DESCRIPTION

The TDA1308 is an integrated class AB stereo headphone driver contained in an SO8 or a DIP8 plastic package. The device is fabricated in a 1 mm CMOS process and has been primarily developed for portable digital audio applications.

QUICK REFERENCE DATA

V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = 25 °C; f_i = 1 kHz; R_L = 32 Ω; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage					
	single		3.0	5.0	7.0	V
	dual		1.5	2.5	3.5	V
V_{SS}	negative supply voltage		−1.5	−2.5	−3.5	V
I_{DD}	supply current	no load	–	3	5	mA
P_{tot}	total power dissipation	no load	–	15	25	mW
P_o	maximum output power	THD < 0.1%; note 1	–	60	–	mW
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	note 1				
			–	0.03	0.06	%
			–	−70	−65	dB
		R_L = 5 kΩ	–	−101	–	dB
S/N	signal-to-noise ratio		100	110	–	dB
α_{cs}	channel separation		–	70	–	dB
		R_L = 5 kΩ	–	105	–	dB
PSRR	power supply ripple rejection	f_i = 100 Hz; $V_{ripple(p-p)}$ = 100 mV	–	90	–	dB
T_{amb}	operating ambient temperature		−40	–	+85	°C

Note

1. V_{DD} = 5 V; $V_{O(p-p)}$ = 3.5 V (at 0 dB).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1308	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
TDA1308T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

BLOCK DIAGRAM

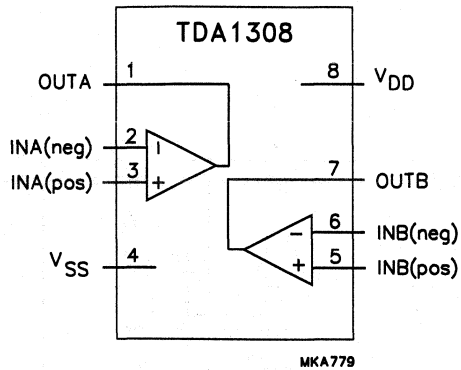


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
OUTA	1	output A
INA(neg)	2	inverting input A
INA(pos)	3	non-inverting input A
V_{SS}	4	negative supply
INB(pos)	5	non-inverting input B
INB(neg)	6	inverting input B
OUTB	7	output B
V_{DD}	8	positive supply

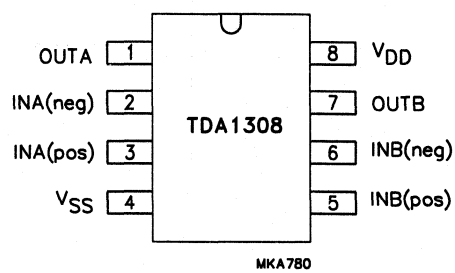


Fig.2 Pin configuration.

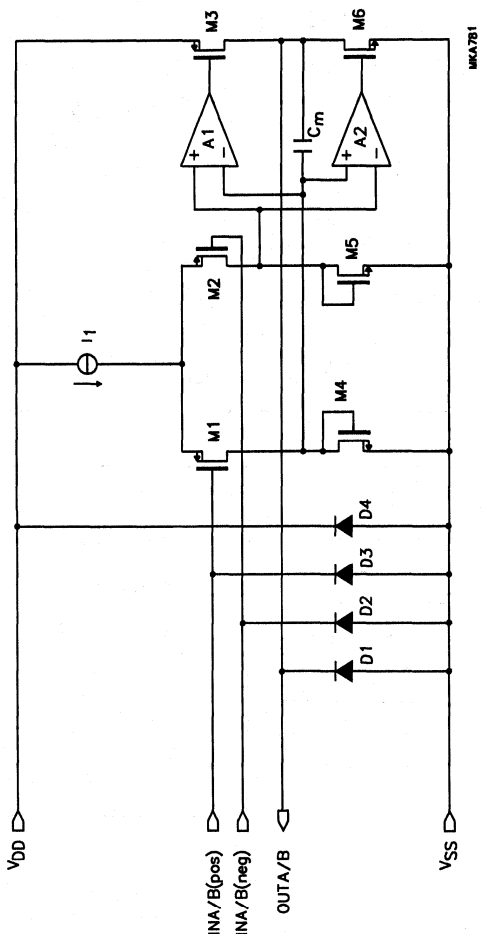


Fig.3 Equivalent schematic diagram.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		0	8.0	V
$t_{SC(O)}$	output short-circuit duration	T_{amb} = 25 °C; P_{tot} = 1 W	20	–	s
T_{stg}	storage temperature		−65	+150	°C
T_{amb}	operating ambient temperature		−40	+85	°C
V_{esd}	electrostatic discharge	note 1	−2000	+2000	V
		note 2	−200	+200	V

Notes

1. Human body model: C = 100 pF; R = 1500 Ω; 3 pulses positive plus 3 pulses negative.
2. Machine model: C = 200 pF: L = 0.5 mH: R = 0 Ω; 3 pulses positive plus 3 pulses negative.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	DIP8	109	K/W
	SO8	210	K/W

QUALITY SPECIFICATION

In accordance with *"UZW-BO/FQ-0601"*. The numbers of the quality specification can be found in the *"Quality Reference Handbook"*. The handbook can be ordered using the code 9398 510 63011.

CHARACTERISTICS

V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = 25 °C; f_i = 1 kHz; R_L = 32 Ω; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage					
	single		3.0	5.0	7.0	V
	dual		1.5	2.5	3.5	V
V_{SS}	negative supply voltage		−1.5	−2.5	−3.5	V
I_{DD}	supply current	no load	–	3	5	mA
P_{tot}	total power dissipation	no load	–	15	25	mW
DC characteristics						
$V_{I(os)}$	input offset voltage		–	10	–	mV
I_{bias}	input bias current		–	10	–	pA
V_{CM}	common mode voltage		0	–	3.5	V
G_v	open-loop voltage gain	R_L = 5 kΩ	–	70	–	dB
I_O	maximum output current	(THD + N)/S < 0.1%	–	60	–	mA
R_O	output resistance		–	0.25	–	Ω
V_O	output voltage swing	note 1	0.75	–	4.25	V
		R_L = 16 Ω; note 1	1.5	–	3.5	V
		R_L = 5 kΩ; note 1	0.1	–	4.9	V
PSRR	power supply rejection ratio	f_i = 100 Hz; $V_{ripple(p-p)}$ = 100 mV	–	90	–	dB
α_{cs}	channel separation		–	70	–	dB
		R_L = 5 kΩ	–	105	–	dB
C_L	load capacitance		–	–	200	pF
AC characteristics						
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	note 2	–	−70	−65	dB
			–	0.03	0.06	%
		note 2; R_L = 5 kΩ	–	−101	–	dB
			–	0.0009	–	%
S/N	signal-to-noise ratio		100	110	–	dB
f_G	unity gain frequency	open-loop; R_L = 5 kΩ	–	5.5	–	MHz
P_o	maximum output power	(THD + N)/S < 0.1%	–	60	–	mW
C_i	input capacitance		–	3	–	pF
SR	slew rate	unity gain inverting	–	5	–	V/μs
B	power bandwidth	unity gain inverting	–	20	–	kHz

Notes

1. Values are proportional to V_{DD}; (THD + N)/S < 0.1%.
2. V_{DD} = 5.0 V; $V_{O(p-p)}$ = 3.5 V (at 0 dB).

TEST AND APPLICATION INFORMATION

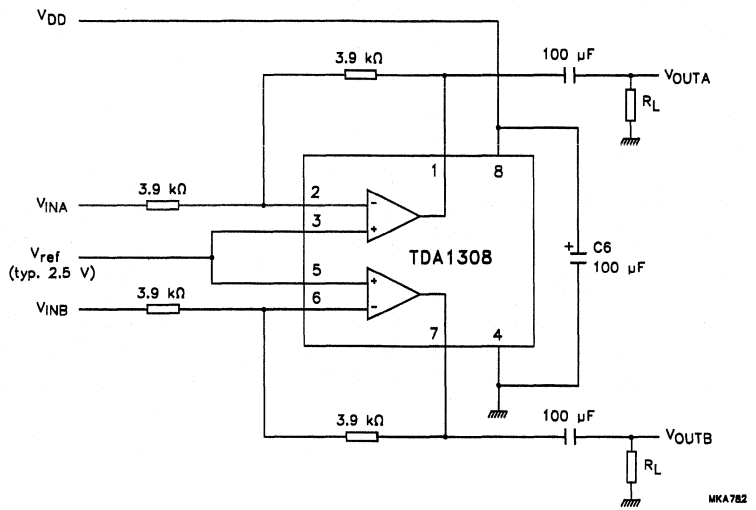


Fig.4 Measurement circuit for inverting application.

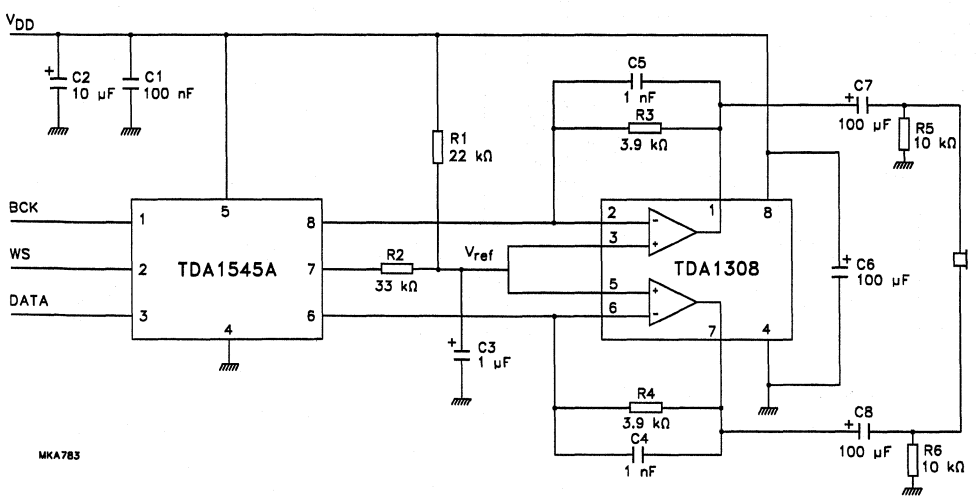


Fig.5 Example of application with TDA1545A (stereo continuous calibration DAC).

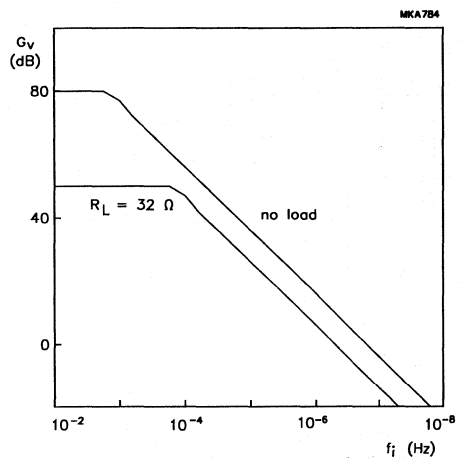


Fig.6 Open-loop gain as a function of input frequency.

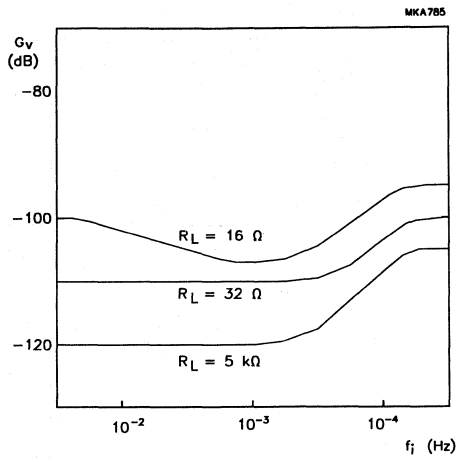


Fig.7 Crosstalk as a function of input frequency.

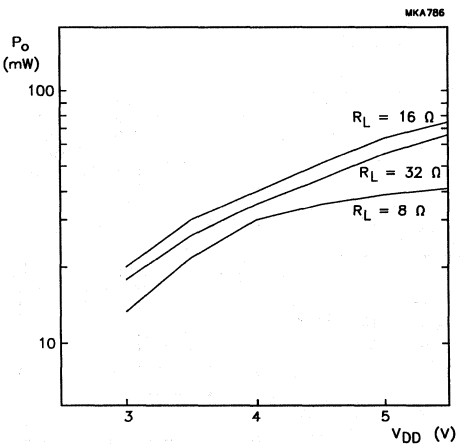


Fig.8 Output power as a function of supply voltage.

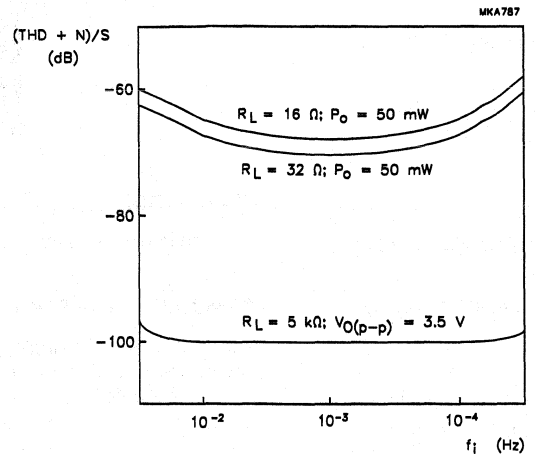


Fig.9 Total harmonic distortion plus noise-to-signal ratio as a function of input frequency.

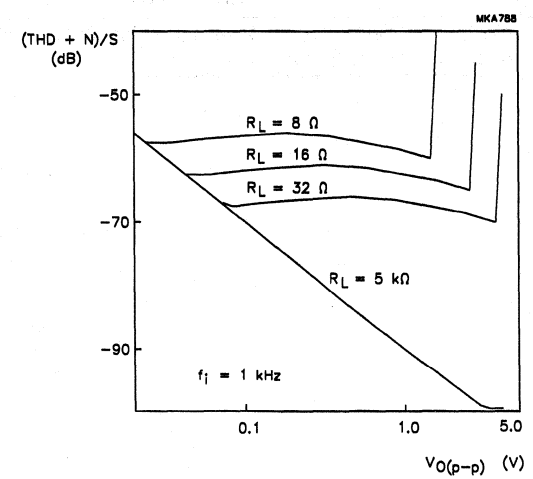


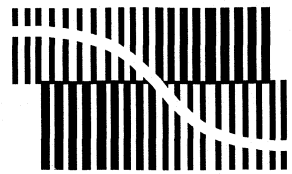
Fig.10 Total harmonic distortion plus noise-to-signal ratio as a function of output voltage level.

Low-voltage low-power stereo bitstream ADC/DAC

TDA1309H

FEATURES

- Low power
- Low supply voltage (2.7 V)
- Integrated high-pass filter to cancel DC offset (ADC)
- Analog loop-through function
- Multiple digital input/output formats possible
- $256f_s$ system clock frequency
- Several power-down modes
- Digital de-emphasis (DAC)
- Overload detector to enable automatic recording level adjustment (ADC)
- Input pads suitable for 5.5 V; low supply voltage interfacing
- High dynamic range
- DAC requires only one capacitor for post-filtering
- Small 44-pin quad flat pack with 0.8 mm pitch
- $256f_s$ system clock frequency in Analog-to-Digital (AD) and Digital-to-Analog (DA) mode
- Choice of three system clock frequencies ($192f_s$, $256f_s$ or $384f_s$) in DA mode.



BITSTREAM CONVERSION

APPLICATION

- Portable digital audio equipment.

GENERAL DESCRIPTION

The TDA1309H is a single chip stereo analog-to-digital and digital-to-analog converter employing bitstream conversion techniques. The low voltage requirement makes the device eminently suitable for use in low-voltage low-power portable digital audio equipment which incorporates recording and playback functions.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1309H	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2

QUICK REFERENCE DATA

$V_{DDD} = V_{DDA} = V_{DDO} = V_{DDD(F)} = 3$ V; $V_{SSD} = V_{SSA} = V_{SSO} = V_{SSD(F)} = 0$ V; $T_{amb} = 25$ °C; full scale sine wave input; mode 1; $f_i = 1$ kHz; 16-bit input data; conversion rate = 44.1 kHz; measurement bandwidth = 10 Hz to 20 kHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
$V_{DDA(AD)}$	ADC analog supply voltage (pin 8)		2.7	3.0	4.0	V
$V_{DDA(DA)}$	DAC analog supply voltage (pin 25)		2.7	3.0	4.0	V
V_{DDO}	operational amplifiers supply voltage (pin 19)		2.7	3.0	4.0	V
V_{DDD}	ADC and DAC digital supply voltage (pin 28)		2.7	3.0	4.0	V
$V_{DDD(F)}$	digital filters supply voltage (pin 34)		2.7	3.0	4.0	V
$I_{DDA(AD)}$	ADC analog supply current (pin 8)		–	8	12.5	mA
$I_{DDA(DA)}$	DAC analog supply current (pin 25)		–	3.5	7	mA
I_{DDO}	operational amplifiers supply current (pin 19)		–	12	18	mA
I_{DDD}	ADC and DAC digital supply current (pin 28)		–	0.2	0.5	mA
$I_{DDD(F)}$	digital filters supply current (pin 34)		–	20	30	mA
$I_{PD(DA)}$	DAC power-down current		–	15	20	mA
$I_{PD(AD)}$	ADC power-down current		–	7	10	mA
T_{amb}	operating ambient temperature		–20	–	+75	°C
Analog-to-digital converter						
$V_{I(rms)}$	input voltage (RMS value)	note 1	–	0.5	0.54	V
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB	–	–85	–80	dB
		at –60 dB; A-weighted	–	–35	–30	dB
S/N	idle channel signal-to-noise ratio	$V_I = 0$ V; A-weighted	90	95	–	dB
α_{cs}	channel separation		–	90	–	dB
Digital-to-analog converter						
$V_{O(rms)}$	output voltage (RMS value)	note 2	0.43	0.5	0.57	V
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB	–	–90	–82	dB
		at –60 dB; A-weighted	–	–38	–34	dB
		at –60 dB; A-weighted; note 3	–	–44	–	dB
S/N	idle channel signal-to-noise ratio	code 0000H; A-weighted	–	104	–	dB
α_{cs}	channel separation		90	100	–	dB

Notes

1. The input voltage for full scale digital output is a function of $V_{DDA(AD)}$.
2. At full scale digital input; no de-emphasis; $V_{O(rms)}$ is a function of $V_{DDA(DA)}$.
3. 18-bit input data.

BLOCK DIAGRAM

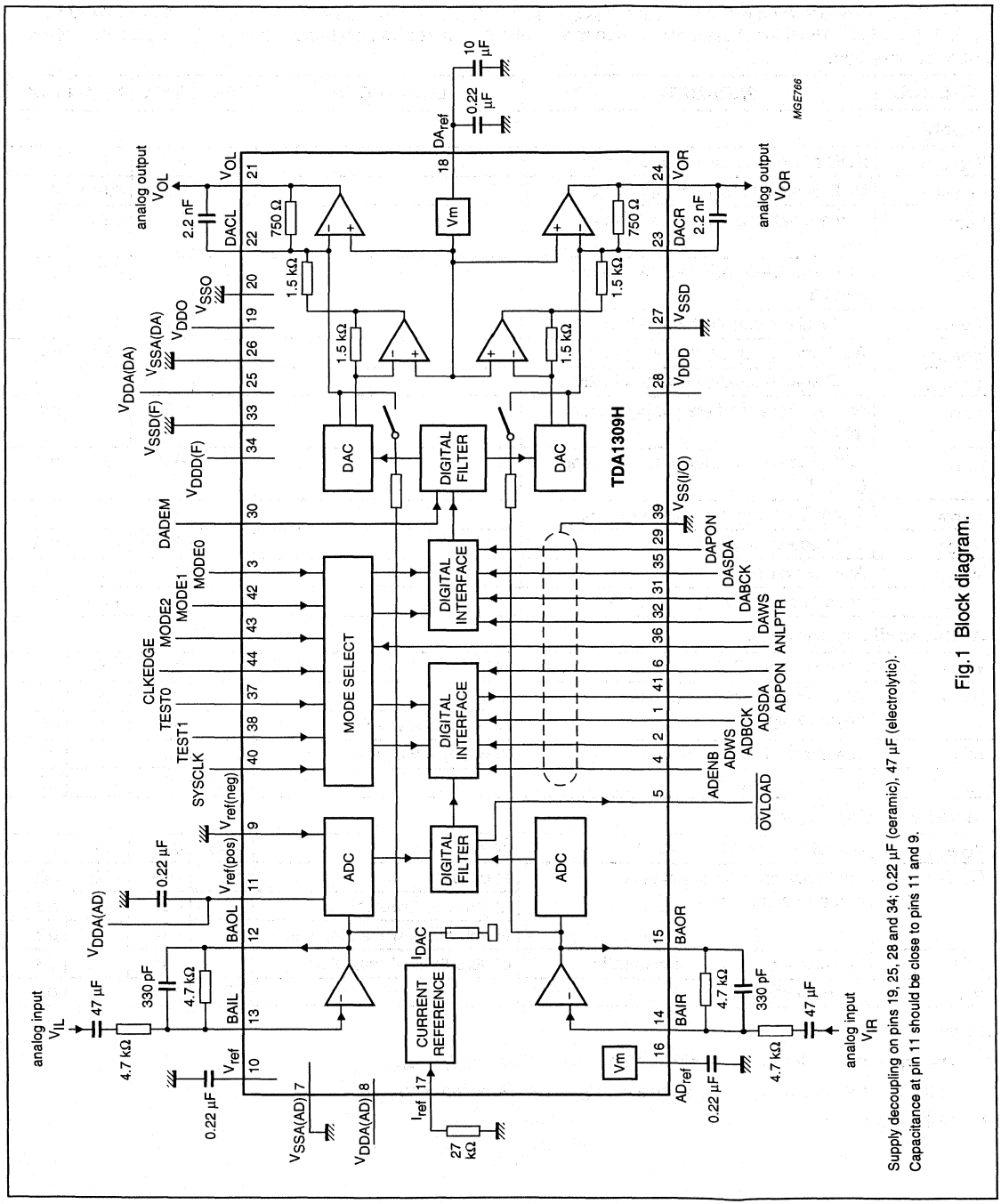


Fig.1 Block diagram.

Supply decoupling on pins 19, 25, 28 and 34; 0.22 µF (ceramic), 47 µF (electrolytic).
Capacitance at pin 11 should be close to pins 11 and 9.

PINNING

SYMBOL	PIN	DESCRIPTION
ADBCK	1	ADC input bit clock; $32f_s$ or $64f_s$
ADWS	2	ADC word select input at f_s
MODE0	3	ADC/DAC mode select input
ADENB	4	ADC serial data enable input (active HIGH)
$\overline{\text{OVLOAD}}$	5	ADC output overload flag (active LOW)
ADPON	6	ADC power-on-mode input (active HIGH)
$V_{SSA(AD)}$	7	ADC analog ground supply voltage
$V_{DDA(AD)}$	8	ADC analog supply voltage
$V_{ref(neg)}$	9	ADC negative reference voltage input (ground)
V_{ref}	10	ADC decoupling capacitor
$V_{ref(pos)}$	11	ADC positive reference voltage decoupling capacitor
BAOL	12	ADC input amplifier output left
BAIL	13	ADC input amplifier virtual ground left
BAIR	14	ADC input amplifier virtual ground right
BAOR	15	ADC input amplifier output right
AD_{ref}	16	ADC decoupling capacitor
I_{ref}	17	ADC/DAC reference current resistor input
DA_{ref}	18	DAC decoupling capacitor
V_{DDO}	19	ADC/DAC operational amplifier supply voltage
V_{SSO}	20	ADC/DAC operational amplifier ground supply voltage
V_{OL}	21	DAC output voltage left
DACL	22	DAC output current left
DACR	23	DAC output current right
V_{OR}	24	DAC output voltage right
$V_{DDA(DA)}$	25	DAC analog supply voltage
$V_{SSA(DA)}$	26	DAC analog ground supply voltage
V_{SSD}	27	ADC/DAC digital ground supply voltage
V_{DDD}	28	ADC/DAC digital supply voltage
DAPON	29	DAC power-on-mode input (active HIGH)
DADEM	30	DAC digital de-emphasis input (active HIGH)
DABCK	31	DAC input bit clock; $32f_s$, $48f_s$ or $64f_s$
DAWS	32	DAC word select input at f_s
$V_{SSD(F)}$	33	ADC/DAC digital filters ground supply voltage
$V_{DDD(F)}$	34	ADC/DAC digital filters supply voltage
DASDA	35	DAC serial data input
ANLPTR	36	ADC/DAC analog loop-through input (active HIGH)
TEST0	37	ADC/DAC enable test mode 0 input (LOW is normal mode)
TEST1	38	ADC/DAC enable test mode 1 input (LOW is normal mode)
$V_{SS(I/O)}$	39	ADC/DAC digital input/output ground supply voltage
SYSCLK	40	ADC/DAC system clock input ($f_{sys} = 256f_s$; DAC also $192f_s$ and $384f_s$)

SYMBOL	PIN	DESCRIPTION
ADSDA	41	ADC serial data output
MODE1	42	ADC/DAC mode 1 select input
MODE2	43	ADC/DAC mode 2 select input
CLKEDGE	44	ADC/DAC input bit clock rising/falling edge

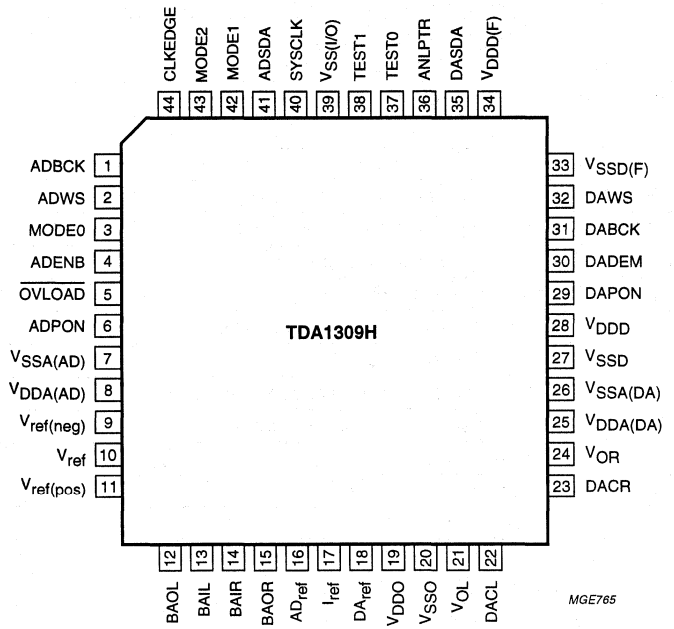


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Figure 1 illustrates the various components of the TDA1309H.
The analog-to-digital converter is a bitstream type converter, both channels are sampled simultaneously. The digital-to-analog converter is a BCC (Bitstream Continuous Calibration) type converter. The digital filter for the ADC is a bit serial IIR filter that produces a fairly linear phase response up to 15 kHz. A high-pass filter is incorporated in the down-sampling path to remove DC offsets. An overload detection circuit is incorporated to facilitate automatic recording level adjustment.

The digital up-sample filter for the DAC is partly IIR, with virtual linear phase response up to 15 kHz, and partly FIR. A switchable digital de-emphasis circuit is also incorporated. Due to the BCC principle used, the DAC needs only single pole post-filtering (one external capacitor) to meet the out-of-band suppression requirement.

The ADC and DAC channels have separate power-down modes, to reduce power if one of them is not in use. An analog loop-through function enables analog-input analog-output mode without using the ADC and DAC converters or filters, thereby switching them off to reduce power consumption.

The digital interfaces accommodates, 16 and 18-bit, I^2S-bus and LSB justified formats. The ADC digital output can be made 3-state by means of the ADENB signal, this enables the use of a digital bus.

The TDA1309H interface accommodates slave mode only, therefore, the system ICs must provide the system clock, bit clock and word clock signals. For the DAC, the TDA1309H accepts the data together with these clocks, for the ADC it delivers the data in response to these clocks. Within one stereo frame, the first sample always represents the left channel. When sending data the unused bit positions are set to zero, when receiving data these bit positions are don't cares.

To accommodate the various interface formats and system clock frequencies four control pins are provided, MODE0 to MODE2 for mode selection and CLKEDGE which selects the active edge of the BCK signal. Table 1 gives the interface mode selection, Fig.3 illustrates the ADC/DAC data formats and Fig.5 the operating modes.

The section of the TDA1309H is designed to accommodate two main modes:

1. The $256f_s$ mode in which analog-to-digital and digital-to-analog can be used
2. The $192f_s$ or $384f_s$ mode (digital-to-analog only).

Table 1 Interface mode selection

DEVICE PIN			ADC/DAC FORMATS				
MODE 2	MODE 1	MODE 0	TYPE	BITS	BCK	SYS; f_{sys}	FIGURE
0	0	0	LSB justified	16	$32f_s$	$256f_s$	3(a)
0	0	1	LSB justified	16	$64f_s$	$256f_s$	3(b)
0	1	0	LSB justified	16	$48f_s$	$192f_s$(1)	4(a)
0	1	1	LSB justified	18	$64f_s$	$256f_s$	3(c)
1	0	0	I^2S-bus	16	$32f_s$	$256f_s$	3(d)
1	0	1	I^2S-bus	16	$64f_s$	$256f_s$	3(e)
1	1	0	I^2S-bus	16	$48f_s$	$384f_s$(1)	4(b)
1	1	1	I^2S-bus	18	$64f_s$	$256f_s$	3(f)

Note

1. Only digital-to-analog.

Table 2 Clock edge mode

CLKEDGE	VALID EDGE OF BCK	
	ADC	DAC
0	falling	rising
1	rising	falling

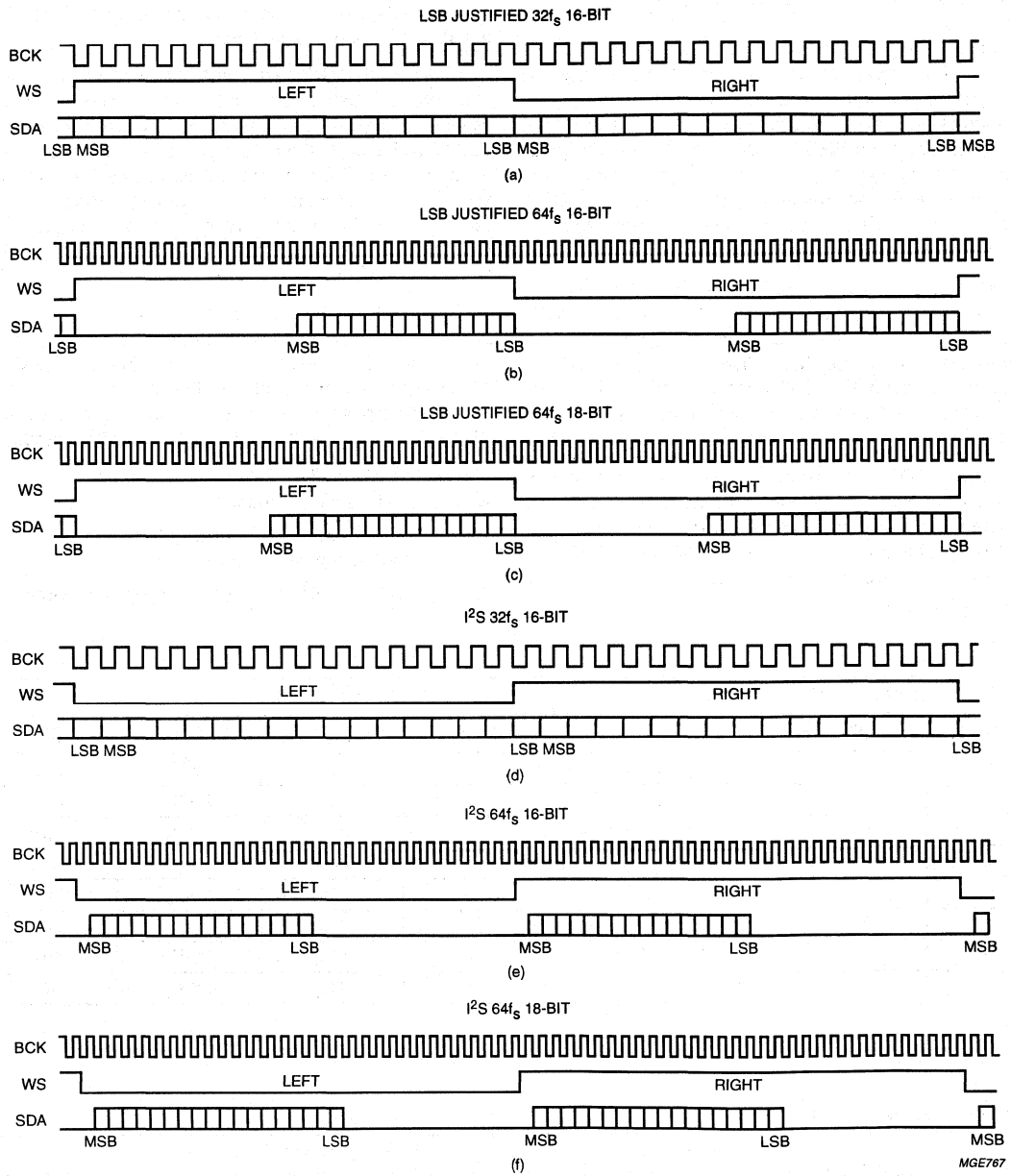


Fig.3 DAC and ADC data formats (continued in Fig.4).

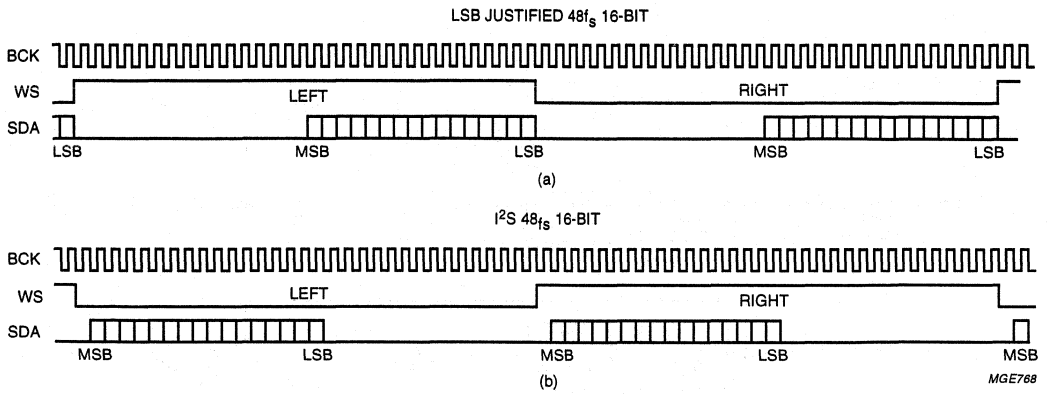


Fig.4 DAC and ADC data formats (continued from Fig.3).

There are different modes in which the TDA1309H can operate. These modes can be selected as shown in Table 3 and Fig.5. In mode a, the digital filters clock is switched off. Switching over to one of the ADC active modes (b, c or d) initiates a reset sequence of the digital filters. This mode should be activated immediately after power-on for at least 2 clock periods.

Table 3 Operating mode selection

MODE	DESCRIPTION	DEVICE PIN LOGIC		
		ANLPTR	ADPON	DAPON
a	not used	0	0	0
b	record and playback	0	1	1
c	record only	0	1	0
d	record and analog loop-through	1	1	0
e	analog loop-through	1	0	0
f	playback only	0	0	1
g and h	reserved	1	X[1]	1

Note

1. X = don't care.

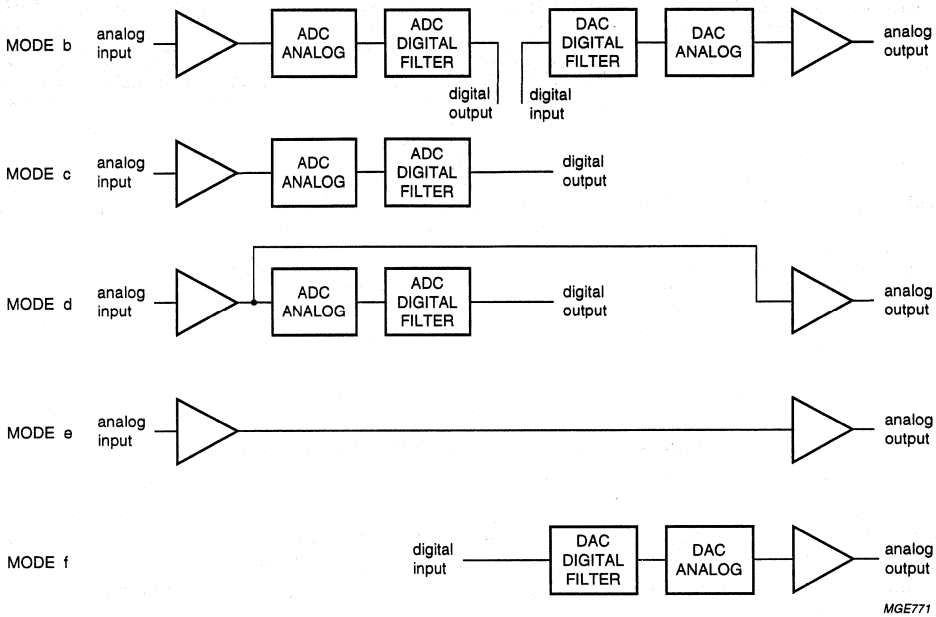


Fig.5 Schematic diagram of operating modes.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DDA(AD)}$	analog supply voltage (pin 8)		–	4.5	V
$V_{DDA(DA)}$	analog supply voltage (pin 25)		–	4.5	V
V_{DDO}	operational amplifiers supply voltage (pin 19)		–	4.5	V
V_{DDD}	digital supply voltage (pin 28)		–	4.5	V
$V_{DDD(F)}$	digital filters supply voltage (pin 34)		–	4.5	V
ΔV_{DD}	maximum supply voltage difference		–	100	mV
ΔV_{SS}	maximum ground supply voltage difference		–	100	mV
V_I	maximum input voltage		−0.5	V_{DD} + 0.5	V
I_{IK}	DC clamp input diode current	V_I < −0.5 V or V_I > V_{DD} + 0.5 V	–	±10	mA
I_{OK}	DC output clamp diode current; (output type 2 mA)	V_O < −0.5 V or V_O > V_{DD} + 0.5 V	–	±10	mA
T_{stg}	storage temperature		−65	+150	°C
T_{amb}	operating ambient temperature		−20	+75	°C
V_{es}	electrostatic handling	note 1	−1500	+1500	V
		note 2	−300	+300	V

Notes

1. Human body model: C = 100 pF; R = 1.5 kΩ; 3 zaps positive and 3 zaps negative.
2. Machine model: C = 200 pF; L = 0.5 μH; R = 10 Ω; 3 zaps positive and 3 zaps negative.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	60	K/W

QUALITY SPECIFICATION

In accordance with *"SNW-FQ-611E"*. The number of this quality specification can be found in the *"Quality Reference Handbook"*. The handbook can be ordered using the code 9397 750 00192.

CHARACTERISTICS

$V_{DDD} = V_{DDA} = V_{DDO} = V_{DDD(F)} = 3$ V; $V_{SSD} = V_{SSA} = V_{SSO} = V_{SSD(F)} = 0$ V; $T_{amb} = 25$ °C; full scale sine wave input; mode 1; $f_i = 1$ kHz; 16-bit input data; conversion rate = 44.1 kHz; measurement bandwidth = 10 Hz to 20 kHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
$V_{DDA(AD)}$	ADC analog supply voltage (pin 8)		2.7	3.0	4.0	V
$V_{DDA(DA)}$	DAC analog supply voltage (pin 25)		2.7	3.0	4.0	V
V_{DDO}	operational amplifiers supply voltage (pin 19)		2.7	3.0	4.0	V
V_{DDD}	ADC/DAC digital supply voltage (pin 28)		2.7	3.0	4.0	V
$V_{DDD(F)}$	digital filters supply voltage (pin 34)		2.7	3.0	4.0	V
$I_{DDA(AD)}$	ADC analog supply current (pin 8)		–	8	12.5	mA
		ADC power-down	–	0.3	1	mA
$I_{DDA(DA)}$	DAC analog supply current (pin 25)		–	3.5	7	mA
		DAC power-down	–	1.4	2	mA
I_{DDO}	operational amplifiers supply current (pin 19)		–	12	18	mA
		DAC power-down	–	5.5	9	mA
		ADC power-down	–	7	11	mA
		ADC/DAC power-down	–	0	–	mA
I_{DDD}	ADC/DAC digital supply current (pin 28)		–	0.2	0.5	mA
$I_{DDD(F)}$	digital filters supply current (pin 34)		–	20	30	mA
		DAC power-down	–	15	20	mA
		ADC power-down	–	7	10	mA
$I_{DDD(F)q}$	digital filters quiescent current		–	–	100	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog-to-digital converter						
$V_{I(rms)}$	input voltage (RMS value)	note 1	–	0.5	0.54	V
I_I	input current (pins 13 and 14)		–	–	10	nA
ΔV_O	unbalance between channels		–	–	0.3	dB
RES	resolution	16-bit format	–	16	–	bits
		18-bit format	–	18	–	bits
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB	–	–85	–80	dB
		at –20 dB	–	–75	–	dB
		at –60 dB; A-weighted	–	–35	–30	dB
S/N	idle channel signal-to-noise ratio	V_I = 0 V; A-weighted	90	95	–	dB
α_{cs}	channel separation		–	90	–	dB
PSRR	power supply rejection ratio	note 2	–	–30	–	dB
Digital-to-analog converter						
$V_{O(rms)}$	output voltage (RMS value)	note 3	0.43	0.5	0.57	V
ΔV_O	unbalance between channels		–	0.1	–	dB
R_L	load resistance		5	–	–	kΩ
C_L	load capacitance	note 4	–	–	200	pF
RES	resolution	16-bit format	–	16	–	bits
		18-bit format	–	18	–	bits
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB	–	–90	–82	dB
		at –20 dB	–	–75	–	dB
		at –60 dB; A-weighted	–	–38	–34	dB
		at –60 dB; A-weighted; note 5	–	–44	–	dB
S/N	idle channel signal-to-noise ratio	code 0000H; A-weighted	–	104	–	dB
α_{cs}	channel separation		90	100	–	dB
PSRR	power supply rejection ratio	note 2	–	–30	–	dB
Analog loop-through (mode e)						
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB	–	–85	–	dB
S/N	idle channel signal-to-noise ratio	V_I = 0 V; A-weighted	–	95	–	dB
G_{ltr}	loop-through gain	note 1	–	–1.1	–	dB
E_{os}	DC offset error		–	1.0	–	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog-to-digital decimation filter						
$f_{s(o)}$	output sample frequency		28	44.1	54	kHz
$f_{s(i)}$	input sample frequency		–	$128f_s$	–	
f_{sys}	system clock frequency		$256f_s$	–	$256f_s$	
B	signal bandwidth	$f_{s(o)}$ = 44.1 kHz	0.02	–	20	kHz
A_{sup}	aliasing suppression	$f_{s(o)} - B < f_i < 2f_{s(o)} - B$; note 6	60	–	–	dB
		$f_i > 2f_{s(o)} - B$; note 6	80	–	–	dB
α	frequency response	f_i = 20 Hz to 20 kHz	−0.2	–	+0.2	dB
OL_{det}	overload detection level	note 7	–	0.11	–	dB
Digital-to-analog interpolation filter						
$f_{s(o)}$	output sample frequency		–	$64f_s$	–	
$f_{s(i)}$	input sample frequency		28	44.1	54	kHz
f_{sys}	system clock frequency		$256f_s$	–	$256f_s$	
B	signal bandwidth	$f_{s(i)}$ = 44.1 kHz	0.02	–	20	kHz
α	frequency response	f_i = 20 Hz to 20 kHz	−0.2	–	+0.2	dB
SUP	out-of-band suppression		40	50	–	dB
Digital part; note 8						
INPUTS (PINS 1 TO 4, 6, 29 TO 32, 35 TO 38, 40 AND 42 TO 44)						
V_{IL}	LOW level input voltage		−0.5	–	$0.3V_{DDD}$	V
$\lvert I_{IL} \rvert$	LOW level input current	$V_I = V_{SSD}$	–	–	10	μA
$\lvert I_{IH} \rvert$	HIGH level input current	$V_I = V_{DDD}$	–	–	10	μA
$C_{I(max)}$	maximum input capacitance		–	–	10	pF
INPUTS (PINS 1 TO 4, 6, 29 TO 32, 35 TO 38, 40 AND 42)						
V_{IH}	HIGH level input voltage		$0.7V_{DDD}$	–	5.5	V
INPUTS (PINS 43 AND 44)						
V_{IH}	HIGH level input voltage		$0.7V_{DDD}$	–	V_{DDD} + 0.5	V
OUTPUTS (PINS 5 AND 41)						
V_{OL}	LOW level output voltage	I_{OL} = 2 mA	–	–	0.5	V
V_{OH}	HIGH level output voltage	I_{OH} = −2 mA	V_{DDD} − 0.5	–	–	V
$\lvert I_{OZ} \rvert$	3-state leakage current	$V_O = V_{DDD}$ or V_{SSD}	–	–	10	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing						
BIT CLOCK (BCK) RELATED SIGNALS (see Fig.6); CLKEDGE = 0						
T_{cy}	clock period		300	–	–	ns
t_{HC}	clock HIGH time		100	–	–	ns
t_{LC}	clock LOW time		100	–	–	ns
t_r	rise time		–	–	20	ns
t_f	fall time		–	–	20	ns
t_{suWS}	set-up time WS to rising edge of BCK		20	–	–	ns
t_{hWS}	hold time WS to rising edge of BCK		0	–	–	ns
t_{suDA}	set-up time SDA (DAC) to rising edge of BCK		20	–	–	ns
t_{hDA}	hold time SDA (DAC) to rising edge of BCK		0	–	–	ns
t_{hAD}	hold time SDA (ADC) to falling edge of BCK		0	–	–	ns
t_{dAD}	delay time SDA (ADC) to falling edge of BCK		–	–	80	ns
SYSTEM CLOCK (SYSCLK) RELATED SIGNALS (see Fig.7)						
T_{cy}	clock period		72	–	–	ns
t_{HC}	clock HIGH time		22	–	–	ns
t_{LC}	clock LOW time		22	–	–	ns
t_r	rise time		–	–	10	ns
t_f	fall time		–	–	10	ns

Notes

1. V_I for full scale digital output is a function of $V_{DDA(AD)}$, 0.5 V (RMS) (at 3 V the digital voltages are equivalent to −1.1 dB in the digital domain).
2. V_{ripple} = 1% of the supply voltage and f_{ripple} = 100 Hz.
3. At full scale digital input; no de-emphasis; $V_{O(rms)}$ is a function of $V_{DDA(DA)}$.
4. For a load capacitance greater than 33 pF a series resistor of 200 Ω is recommended.
5. 18 bits input data.
6. The aliasing suppression frequency is mirrored around $128f_s$.
7. V_{DDA} = 3 V; indicated digital level is with respect to −1.1 dB (no overload).
8. All digital voltages = 2.7 to 4.0 V; all ground supply voltages = 0 V; T_{amb} = −20 to +75 °C.

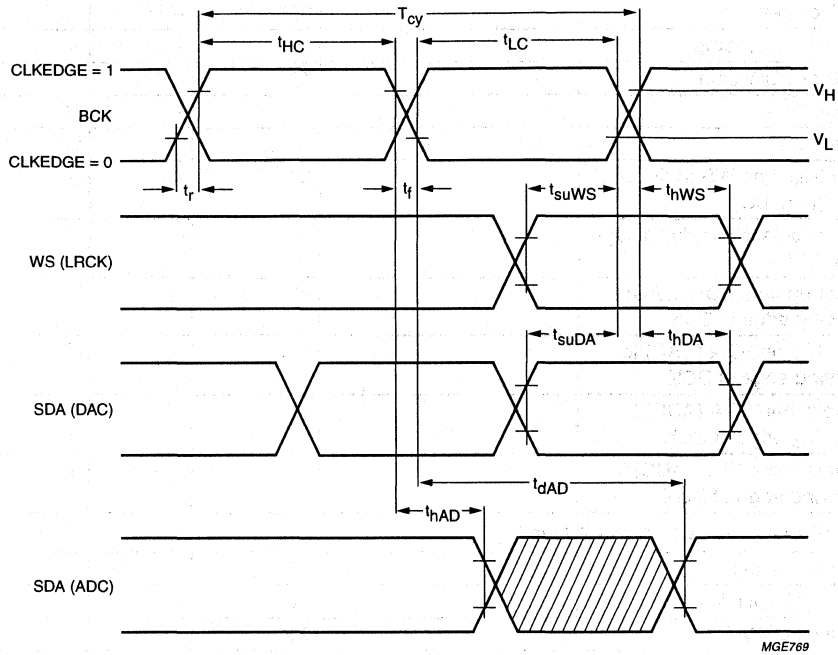


Fig.6 Serial timing of BCK related signals.

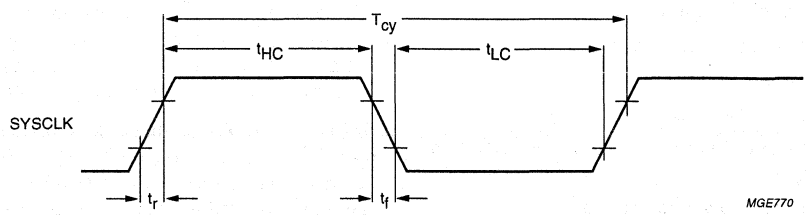


Fig.7 Serial timing of SYSCLK related signals.

Stereo Continuous Calibration DAC (CC-DAC)

TDA1311A

FEATURES

- Voltage output
- Space saving packages SO8 or DIP8
- Low power consumption
- Wide dynamic range (16-bit resolution)
- Continuous Calibration (CC) concept
- Easy application:
  - single 4 to 5.5 V rail supply
  - output current and bias current are proportional to the supply voltage
  - integrated current-to-voltage converter
- Fast settling time permits 2, 4 and 8 × oversampling (serial input) or double-speed operation at 4 × oversampling
- Internal bias current ensures maximum dynamic range
- Wide operating temperature range (–40 °C to +85 °C)
- Compatible with most current Japanese input formats: time multiplexed, two's complement, TTL
- No zero-crossing distortion
- Cost efficient.

GENERAL DESCRIPTION

The TDA1311A; AT is a voltage-driven digital-to-analog converter and is new generation of DAC devices which embodies the innovative technique of Continuous Calibration (CC). The largest bit-currents are repeatedly generated by one single current reference source. This duplication is based upon an internal charge storage principle which has an accuracy insensitive to ageing, temperature matching and process variations.

The TDA1311A; AT is fabricated in a 1.0 μm CMOS process and features an extremely low-power dissipation, small package size and easy application. Furthermore, the accuracy of the intrinsic high coarse-current combined with the implemented symmetrical offset decoding method preclude zero-crossing distortion and ensures high quality audio reproduction. Therefore, the CC-DAC is eminently suitable for use in (portable) digital audio equipment.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1311A	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
TDA1311AT	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		4	5	5.5	V
I_{DD}	supply current	V_{DD} = 5 V at code 0000H	–	3.4	6.0	mA
V_{FS}	full scale output voltage	V_{DD} = 5 V	1.8	2.0	2.2	V
(THD+N)/S	total harmonic distortion plus noise	at 0 dB signal level	–	–68	–63	dB
			–	0.04	0.07	%
		at –60 dB signal level	–	–30	–24	dB
			–	3	6	%
		at –60 dB signal level; A-weighted	–	–33	–	dB
			–	2	–	%
S/N	signal-to-noise ratio at bipolar zero	A-weighted at code 0000H	86	92	–	dB
t_{cs}	current settling time to ±1 LSB		–	0.2	–	µs
BR	input bit rate at data input		–	–	18.4	Mbits/s
f_{BCK}	clock frequency at clock input		–	–	18.4	MHz
TC_{FS}	full scale temperature coefficient at analog outputs (I_{OL}; I_{OR})		–	±400	–	ppm
T_{amb}	operating ambient temperature		–40	–	+85	°C
P_{tot}	total power dissipation	V_{DD} = 5 V at code 0000H	–	17	30	mW

Stereo Continuous Calibration DAC (CC-DAC)

TDA1311A

BLOCK DIAGRAM

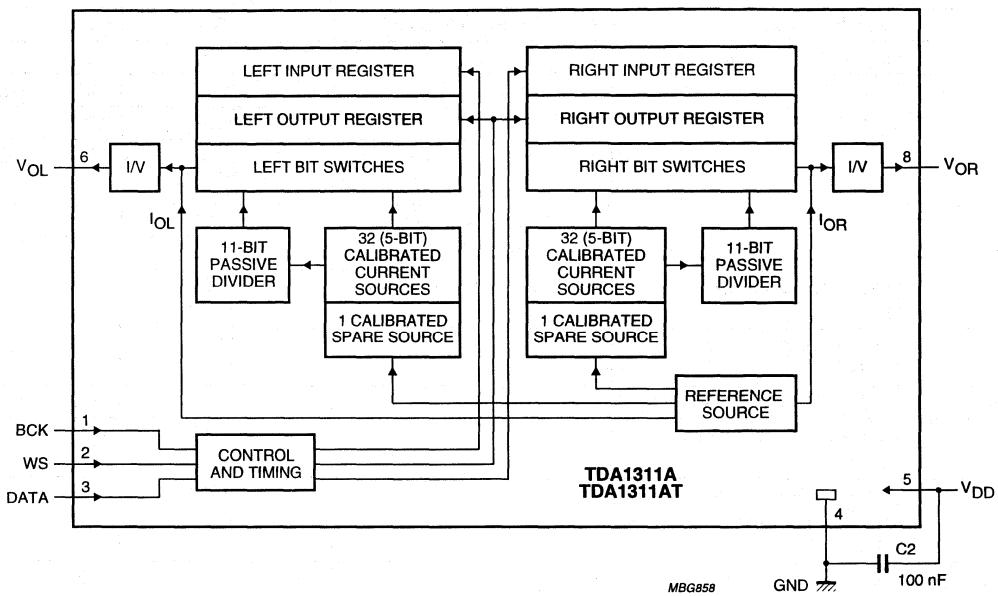


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
BCK	1	bit clock input
WS	2	word select input
DATA	3	data input
GND	4	ground
V_{DD}	5	supply voltage
V_{OL}	6	left channel output
n.c.	7	not connected
V_{OR}	8	right channel output

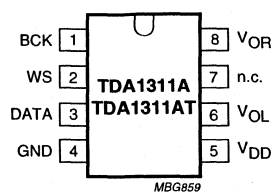


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The basic operation of the continuous calibration DAC is illustrated in Fig.3. The figure shows the calibration and operation cycle. During calibration of the MOS current source (see Fig.3a) transistor M1 is connected as a diode by applying a reference current. The voltage V_{gs} on the intrinsic gate-source capacitance C_{gs} of M1 is then determined by the transistor characteristics. After calibration of the drain current to the reference value I_{REF}, the switch S1 is opened and S2 is switched to the other position (see Fig.3b). The gate-to-source voltage V_{gs} of M1 is not changed because the charge on C_{gs} is preserved. Therefore, the drain current of M1 will still be equal to I_{REF} and this exact duplicate of I_{REF} is now available at the OUT terminal.

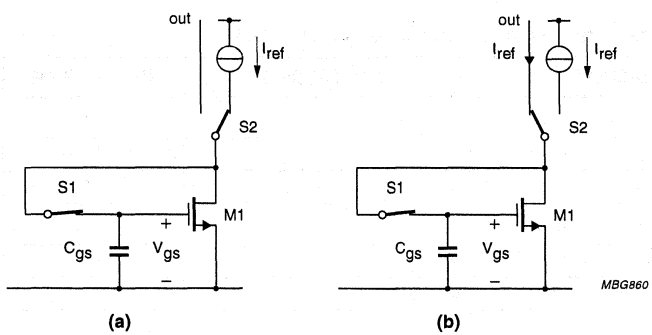
The 32 current sources and the spare current source of the TDA1311A; AT are continuously calibrated (see Fig.1). The spare current source is included to allow continuous converter operation. The output of one calibrated source is connected to an 11-bit binary current divider consisting of 2048 transistors.

A symmetrical offset decoding principle is incorporated that arranges the bit switching in such a way that the zero-crossing is performed only by switching the LSB currents.

The TDA1311A; AT (CC-DAC) accepts serial input data formats of 16-bit word length. Left and right data words are time multiplexed. The most significant bit (bit 1) must always be first. The input data format is shown in Figs 4 and 5.

With a HIGH level on the word select input (WS), data is placed in the left input register and with a LOW level on the WS input, data is placed in the right input register (see Fig.1). The data in the input registers are simultaneously latched in the output registers which control the bit switches.

An internal offset voltage V_{OS} is added to the full scale output voltage V_{FS}; V_{OS} and V_{FS} are proportional to V_{DD}: $V_{DD1}/V_{DD2} = V_{FS1}/V_{FS2} = V_{OS1}/V_{OS2}$.



(a) = calibration.
(b) = operation.

Fig.3 Calibration principle.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		–	6.0	V
T_{stg}	storage temperature		–55	+150	°C
T_{XTAL}	maximum crystal temperature		–	+150	°C
T_{amb}	operating ambient temperature		–40	+85	°C
V_{es}	electrostatic handling	note 1	–2000	+2000	V
		note 2	–200	+200	V

Note

1. Human body model: C = 100 pF, R = 1500 Ω, 3 pulses positive and 3 pulses negative.
2. Machine model: C = 200 pF, L = 0.5 µH, R = 10 Ω, 3 pulses positive and 3 pulses negative.

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	DIL8	100	K/W
	SO8	210	K/W

QUALITY SPECIFICATION

In accordance with SNW-FQ-0611.

CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = 25 °C; measured in Fig.1; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		4.0	5.0	5.5	V
I_{DD}	supply current	at code 0000H	–	3.4	6.0	mA
Digital inputs; pins WS, BCK and DATA						
$\|I_{IL}\|$	input leakage current LOW	V_I = 0.8 V	–	–	10	µA
$\|I_{IH}\|$	input leakage current HIGH	V_I = 2.4 V	–	–	10	µA
f_{BCK}	clock frequency		–	–	18.4	MHz
BR	bit rate data input		–	–	18.4	Mbits/s
f_{WS}	word select input frequency		–	–	384	kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing (see Fig.4)						
t_r	rise time		–	–	12	ns
t_f	fall time		–	–	12	ns
t_{CY}	bit clock cycle time		54	–	–	ns
t_{BCKH}	bit clock pulse width HIGH		15	–	–	ns
t_{BCKL}	bit clock pulse width LOW		15	–	–	ns
$t_{SU;DAT}$	data set-up time		12	–	–	ns
$t_{HD;DAT}$	data hold time to bit clock		2	–	–	ns
$t_{HD;WS}$	word select hold time		2	–	–	ns
$t_{SU;WS}$	word select set-up time		12	–	–	ns
Analog outputs; pins V_{OL} and V_{OR}						
V_{FS}	full-scale voltage		1.8	2.0	2.2	V
TC_{FS}	full-scale temperature coefficient		–	±400	–	ppm
V_{os}	offset voltage	$V_{DD} = V_{OL/ORmax}$	0.45	0.50	0.55	V
(THD+N)/S	total harmonic distortion plus noise	at 0 dB signal level; note 1	–	–68	–63	dB
			–	0.04	0.07	%
		at –60 dB signal level; note 1	–	–30	–24	dB
			–	3	6	%
		at –60 dB signal level; A-weighted; note 1	–	–33	–	dB
			–	2	–	%
		at 0 dB signal level; f = 20 Hz to 20 kHz	–	–65	–61	dB
			–	0.05	0.09	%
t_{cs}	current settling time to ±1 LSB		–	0.2	–	µs
α_{cs}	channel separation		75	80	–	dB
$\lvert\delta I_O\rvert$	unbalance between outputs	note 1	–	0.2	0.3	dB
$\lvert t_d\rvert$	time delay between outputs		–	±0.2	–	µs
S/N	signal-to-noise ratio at bipolar zero	A-weighted at code 0000H	86	92	–	dB

Note

1. Measured with 1 kHz sinewave generated at sampling rate of 192 kHz.

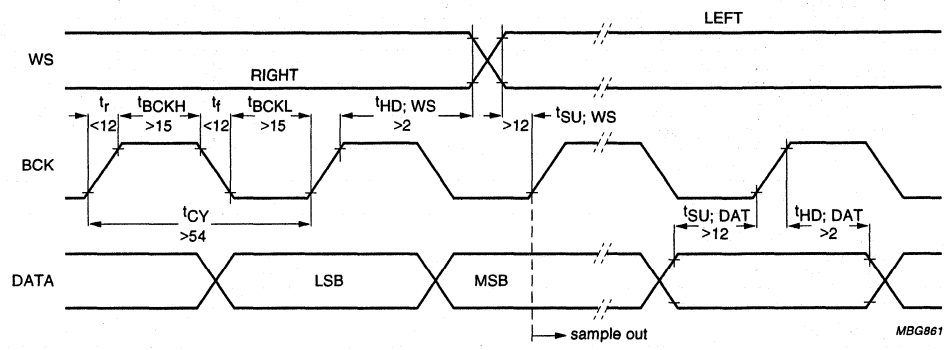


Fig.4 Timing and input signals.

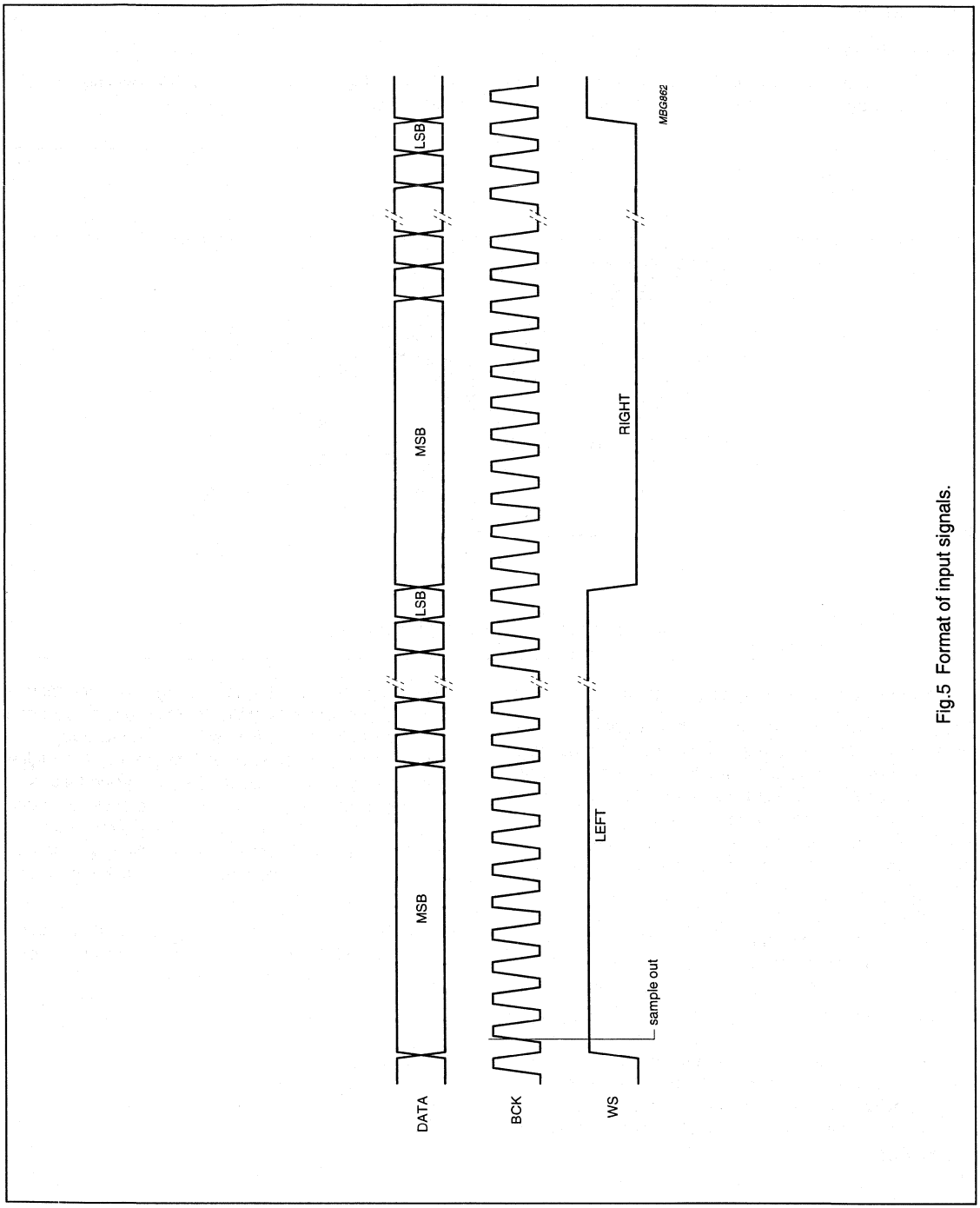


Fig.5 Format of input signals.

APPLICATION INFORMATION

Basic application example

A typical example of a CD-application with the TDA1311A; AT is shown in Fig.6. It features typical decoupling components and a third-order analog post-filter stage providing a line output.

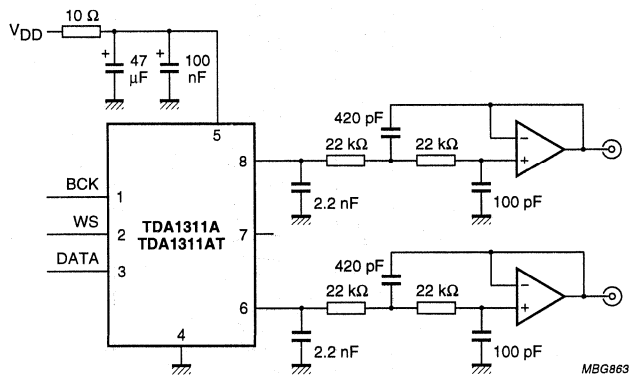


Fig.6 Example of a 3rd order filter application.

Attention to printed circuit board layout

The TDA1311A and even more so the TDA1311AT offers great ease in designing-in to printed-circuit boards due to its small size and low pin count. The TDA1311A; AT being a mixed-signal IC in CMOS, some attention needs to be paid to layout and topology of the application PCB. Following some basic rules will yield the desired performance. The most important considerations are:

1. Supply: care should be taken to supply the TDA1311A; AT with a clean, noiseless V_{DD}, for a good noise performance of the analog parts of the DAC. Supply purity can easily be achieved by using an RC-filtered supply.
2. Grounding: preferably a ground plane should be used, in order to have a low-impedance return available at any point in the layout. It is advantageous to make a partitioning of the ground plane according to the nature of the expected return currents (digital input returns separate from supply returns and separate from the analog section).
3. Topology: the capacitor decoupling high-frequency supply interference from V_{DD} to GND should be placed as close as is physically possible to the IC body, ensuring a low-inductance path to ground. The digital input conductors may be shielded by ground leads running alongside. The placement of a passive ground plane underside the entire IC surface gives `free` additional decoupling from the IC body to ground as well as providing a shield between the digital input pins and the analog output pins.

Figure 7 shows recommended layouts for printed-circuit boards for the SO8 and DIL8 versions respectively. Both layouts use a single-interconnect layer.

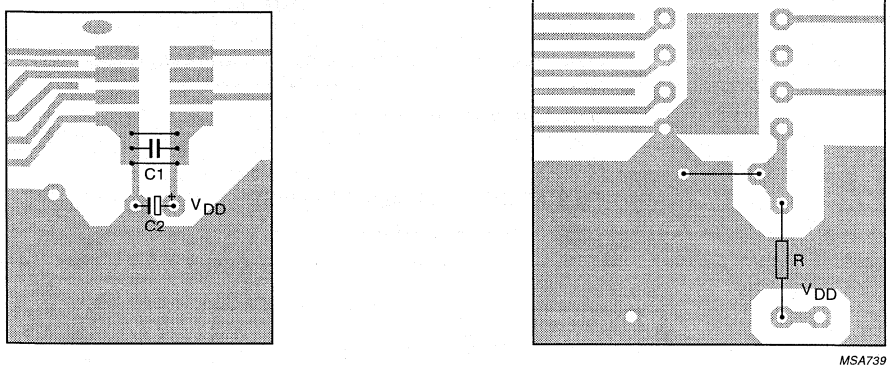
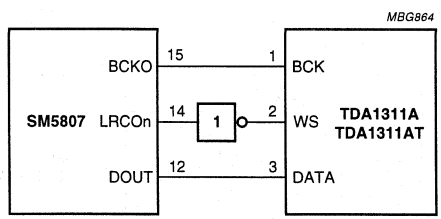


Fig.7 Recommended printed-circuit board layouts.

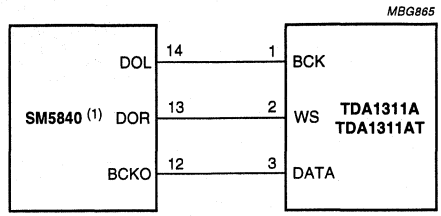
Interface examples

The following figures (Figs 8 to 14) show examples of connections to commonly used decoder and digital filter ICs. The digital interface part is shown only, for clarity. The diagrams are for guidance purposes only - **no** guarantee for industrial exploitation is implied.



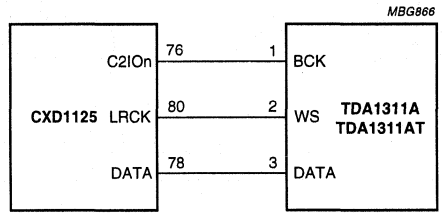
remark: SCSLn – signal SM5807 both "L" and "H" supported by TDA1311A and TDA1311AT

Fig.8 NPC SM5807 digital filter (4FS).



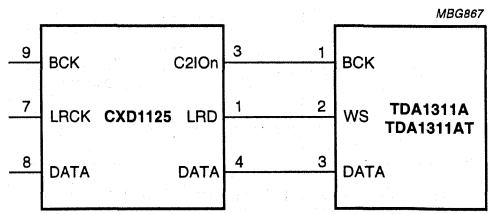
OMODn pin 19: "L" for 4FS operation
(1) versions A/B/G

Fig.9 NPC SM5840 digital filter (4FS).



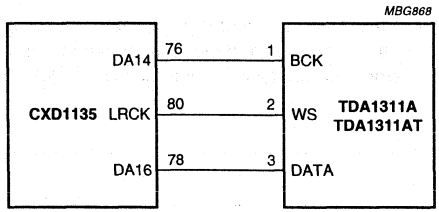
MODE SELECT:
MD1 pin 55: "L"
MD2 pin 56: "L" to use DOTX function
MD3 pin 57: "H"
PSSL pin 59: "L"
SLOB pin 58: "L"

Fig.10 Sony CXD1125 decoder (1FS).



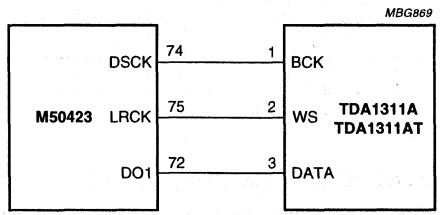
remark: CXD1162 input connectable to CXD1125
in the same way as for TDA1311A; AT to CXD1125

Fig.11 Sony CXD1162 digital filter (4FS).



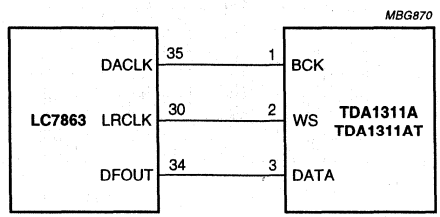
MODE SELECT:
MD1 pin 55: "L"
MD2 pin 56: "L" to use DOTX function
MD3 pin 57: "H" for 1FS; "L" for 2FS
PSSL pin 59: "L"
SLOB pin 58: "L"

Fig.12 Sony CXD1135 decoder (1FS) and digital filter (2FS).



MODE SELECT:
DOBSEL pin 7: "L"
DASEL1 pin 8: "H"
DASEL2 pin 9: "L"
DASEL3 pin 10: "H"
DASEL4 pin 11: "L"

Fig.13 Mitsubishi M50423 decoder (1FS) and digital filter (4FS).



MODE SELECT:
DFOFF pin 27: "L"
MSBF pin 38: "H"

Fig.14 Sanyo LC7863 decoder (1FS).

Evaluation of audio parameters

The following measurement graphs are performed on singular engineering samples; therefore **no** guarantee of typical parameter values is implied. Measurement conditions are typical, as stated in the section Characteristics, unless otherwise indicated. The normal measurement set-up includes a 20 kHz band-limiting filter for bandwidth definition, and an A-weighting filter where indicated.

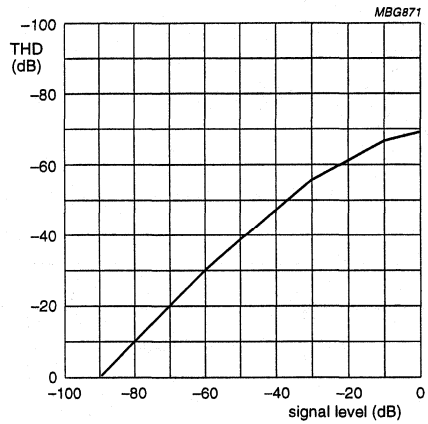
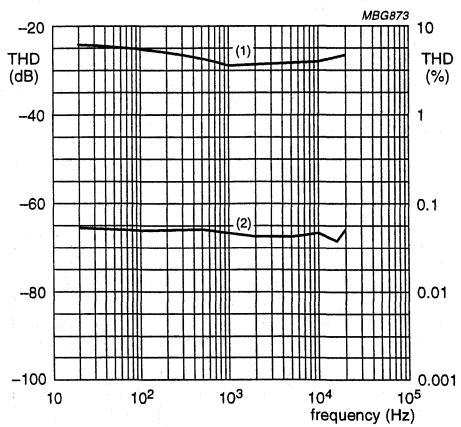
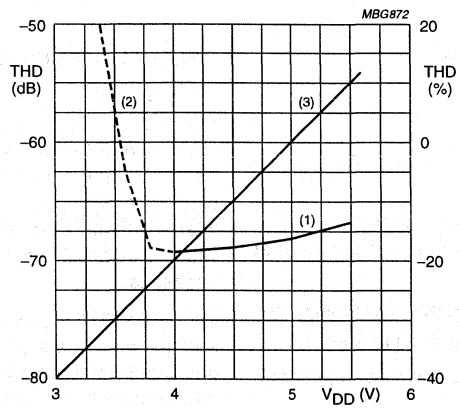


Fig.15 Total harmonic distortion plus noise as a function of signal level (4FS).



(1) Measured including all distortion plus noise at a signal level of −60 dB.
(2) Measured including all distortion plus noise at a signal level of 0 dB.

Fig.16 Total harmonic distortion plus noises as a function of frequency (4FS).



(1) Measured including all distortion plus noise within the specified operating supply voltage range.
(2) Measured including all distortion plus noise outside the specified operating supply voltage range.
(3) V_{FS} relative to nominal.

Fig.17 Total harmonic distortion plus noise as a function of supply voltage (4FS).

Stereo Continuous Calibration DAC (CC-DAC) TDA1387T

FEATURES

- Low power consumption
- Low total harmonic distortion
- Wide dynamic range (16-bit resolution)
- Continuous Calibration (CC) concept
- Single 3 to 5.5 V supply rail
- Output and bias current are proportional to the supply voltage
- Fast settling time enables 2, 4 and 8 times oversampling (serial input) or double-speed operation at 4 times oversampling
- Internal bias current ensures maximum dynamic range
- Wide operating temperature range (–40 to + 85 °C)
- I^2S-bus input format (time multiplex, two's complement, TTL)
- No zero-crossing distortion
- Large DC output voltage compliance
- Contained in small outline package.

APPLICATIONS

- Portable digital audio equipment.

GENERAL DESCRIPTION

The TDA1387T is a member of a generation of digital-to-analog converters which incorporates the innovative technique of Continuous Calibration. The largest bit currents are repeatedly generated from one single reference current. This duplication is based upon an internal charge storage principle and has an accuracy which is insensitive to ageing, temperature and process variations.

The TDA1387T is fabricated in a 1.0 μm CMOS process and features an extremely low power dissipation, small package size and easy application. The intrinsic high coarse current accuracy combined with the implemented symmetrical offset decoding method preclude zero-crossing distortion and ensure high quality audio reproduction. The CC-DAC is eminently suitable for use in portable digital audio equipment.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1387T	SO8	plastic small outline package; 8 leads; body width 3.9 mm.	SOT96-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		3.0	5.0	5.5	V
I_{DD}	supply current	V_{DD} = 5 V at code 0000H	–	5.5	6.5	mA
I_{FS}	full scale output current	V_{DD} = 5 V	0.86	1.0	1.14	mA
		V_{DD} = 3 V	–	0.6	–	mA
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB signal level	–	–88	–78	dB
		at 0 dB signal level	–	0.004	0.012	%
		at –60 dB signal level	–	–33	–24	dB
		at –60 dB signal level	–	2.2	6	%
		at –60 dB; A-weighted	–	–35	–	dB
		at –60 dB; A-weighted	–	1.7	–	%
S/N	signal-to-noise ratio at bipolar zero	A-weighted at code 0000H	86	98	–	dB
t_{cs}	current settling time to ±1 LSB		–	0.2	–	µs
BR	input bit rate (pin 3)		–	–	18.4	Mbits/s
f_{clk}	clock frequency		–	–	18.4	MHz
TC_{FS}	full scale temperature coefficient at pins 6 and 8		–	$\pm 400 \times 10^{-6}$	–	
T_{amb}	operating ambient temperature		–40	–	+85	°C
P_{tot}	total power dissipation	V_{DD} = 5 V at code 0000H	–	27.5	36	mW
		V_{DD} = 3 V at code 0000H	–	10	–	mW

BLOCK DIAGRAM

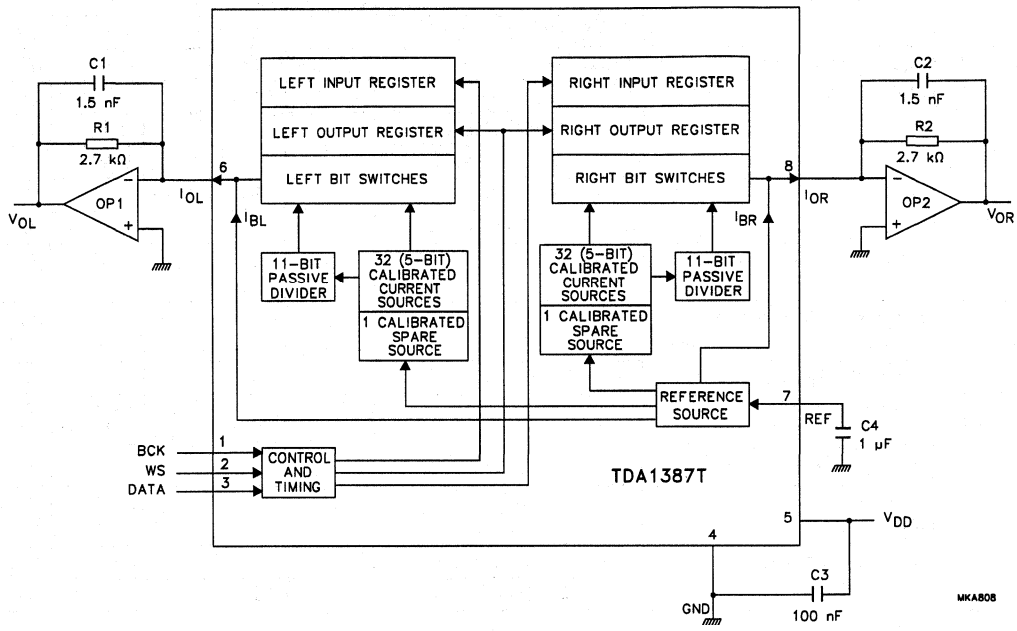


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
BCK	1	bit clock input
WS	2	word selection input
DATA	3	data input
GND	4	ground
V_{DD}	5	supply voltage input
I_{OL}	6	left channel output
REF	7	reference decoupling
I_{OR}	8	right channel output

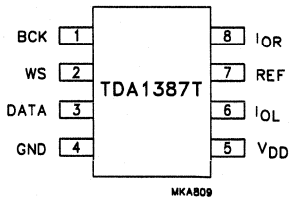


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The basic operation of the continuous calibration DAC is illustrated in Fig.3 which shows the calibration and operation cycle. During calibration of the MOS current source (Fig.3a) transistor M1 is connected as a diode by applying a reference current. The voltage V_{gs} on the intrinsic gate-source capacitance C_{gs} of M1 is then determined by the transistor characteristics. After the drain current has been calibrated to the reference value I_{ref}, the switch S1 is opened and S2 is switched to the other position (Fig.3b). The gate-to-source voltage V_{gs} of M1 is not changed because the charge on C_{gs} is preserved. Therefore, the drain current of M1 will still be equal to I_{ref} and this exact duplication of I_{ref} is now available at the OUT terminal.

In the TDA1387T, 32 current sources and one spare current source are continuously calibrated (see Fig.1). The spare current source is included to allow continuous converter operation. The output of one calibrated source is connected to an 11-bit binary current divider which consists of 2048 transistors. A symmetrical offset decoding principle is incorporated and arranges the bit switching such that the zero-crossing is performed by switching only the LSB currents.

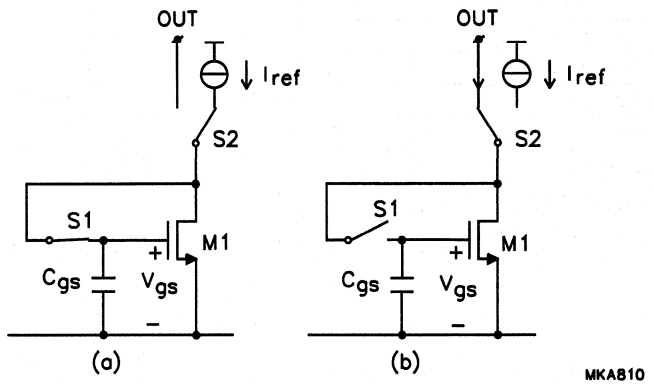
The TDA1387T (CC-DAC) accepts serial input data format of 16-bit word length. Left and right data words are time multiplexed. The input data format is shown in Figs 4 and 5.

With a HIGH level on the WS input, data is placed in the right input register, with a LOW level on the WS input, data is placed in the left input register. The data in the input registers are simultaneously latched to the output registers which control the bit switches. An internal bias current I_{bias} is added to the full scale output current I_{FS} in order to achieve maximum dynamic range at the outputs of OP1 and OP2.

The signal current I_{FS} and the bias current I_{bias} are both proportional to the supply voltage V_{DD}, and have a fixed mutual relation A_{bias} (where $A_{bias} = I_{bias}/I_{FS}$).

It is preferred that the non-inverting input of operational amplifiers OP1 and OP2 is tied to ground to achieve a maximum dynamic range over the supply voltage range.

A decoupling capacitor C4 is recommended for enhancing the supply voltage ripple rejection of the DAC. It has no significant effect on the noise performance.



(a) Calibration.
(b) Operation.

Fig.3 Calibration principle.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	DESCRIPTION	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		–	6.0	V
$T_{xtal(max)}$	maximum crystal temperature		–	+150	°C
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–40	+85	°C
V_{es}	electrostatic handling	note 1	–2000	+2000	V
		note 2	–200	+200	V

Notes

1. Human body model: C = 100 pF; R = 1.5 kΩ; 3 zaps positive and 3 zaps negative.
2. Machine model: C = 200 pF; L = 0.5 μH; R = 10 Ω; 3 zaps positive and 3 zaps negative.

THERMAL CHARACTERISTICS

SYMBOL	DESCRIPTION	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	210	K/W

CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		3.0	5.0	5.5	V
I_{DD}	supply current	at code 0000H	–	5.5	6.5	mA
SVRR	supply voltage ripple rejection	note 1	–	30	–	dB
Digital inputs; WS, BCK and DATA						
$\|I_{LI}\|$	LOW level input leakage current	V_i = 0 V	–	–	10	µA
$\|I_{HI}\|$	HIGH level input leakage current	V_i = 5 V	–	–	10	µA
f_{BCK}	clock frequency		–	–	18.4	MHz
BR	data bit rate		–	–	18.4	Mbits/s
f_{WS}	word select input frequency		–	–	384	kHz
Timing						
t_r	rise time		–	–	12	ns
t_f	fall time		–	–	12	ns
T_{cy}	bit clock cycle time		54	–	–	ns
t_{HB}	bit clock HIGH time		15	–	–	ns
t_{LB}	bit clock LOW time		15	–	–	ns
$t_{su;DA}$	data set-up time		12	–	–	ns
$t_{h;DA}$	data hold time		2	–	–	ns
$t_{h;WS}$	word select hold time		2	–	–	ns
$t_{su;WS}$	word select set-up time		12	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog outputs; I_{OL} and I_{OR}						
RES	output resolution		–	–	16	bits
V_{DCC}	DC output voltage compliance		0	–	3.5	V
$I_{o(p-p)}$	AC output signal current (peak-to-peak value)	note 2	0.86	1.0	1.14	mA
TC_{FS}	full-scale temperature coefficient		–	$\pm 400 \times 10^{-6}$	–	
I_{bias}	output bias current	note 2	0.93	1.08	1.23	mA
V_{ref}	output reference voltage	note 2	–	$\frac{1}{6}V_{DD}$	–	V
R_{ref}	output resistance at pin 7		7.6	11.4	14.8	kΩ
(TDH + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB signal level; note 3	–	–88	–78	dB
		at 0 dB signal level; note 3	–	0.004	0.01	%
		at –60 dB signal level; note 3	–	–33	–24	dB
		at –60 dB signal level; note 3	–	2.2	6	%
		at –60 dB; A-weighted; note 3	–	–35	–	dB
		at –60 dB; A-weighted; note 3	–	1.8	–	%
		f_i = 20 Hz to 20 kHz; at 0 dB signal level; note 3	–	–84	–70	dB
		f_i = 20 Hz to 20 kHz; at 0 dB signal level; note 3	–	0.006	0.03	%
t_{cs}	current settling time to ±1 LSB		–	0.2	–	µs
α_{cs}	channel separation		86	95	–	dB
$\lvert\Delta I_O\rvert$	unbalance between outputs	note 3	–	0.2	0.3	dB
$\lvert t_d\rvert$	delay time between outputs		–	±0.2	–	µs
S/N	signal-to-noise ratio at bipolar zero	A-weighted at code 0000H	86	98	–	dB

Notes

1. V_{ripple} = 1% of the supply voltage; f_{ripple} = 100 Hz.
2. Values are proportional to V_{DD}.
3. Measured with 1 kHz sine wave generated at a sampling rate of 192 kHz.

QUALITY SPECIFICATION

In accordance with *"SNW-FQ-611E"*. The numbers of the quality specification can be found in the *"Quality Reference Handbook"*. The handbook can be ordered using the code 9397 750 00192.

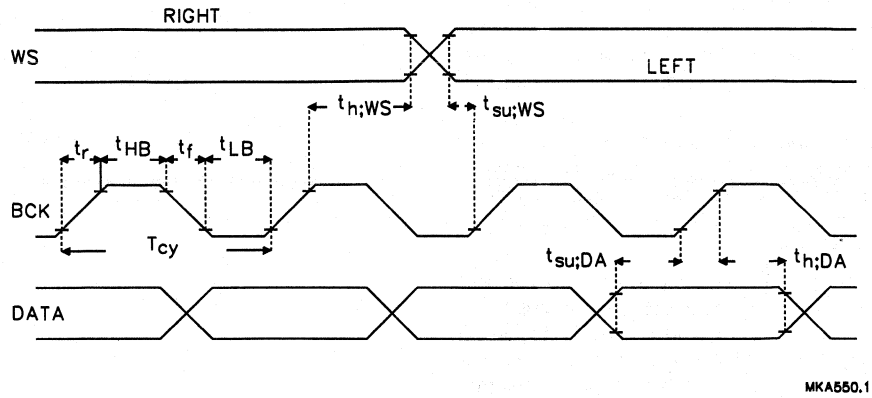


Fig.4 Input signal timing (I^2S-bus).

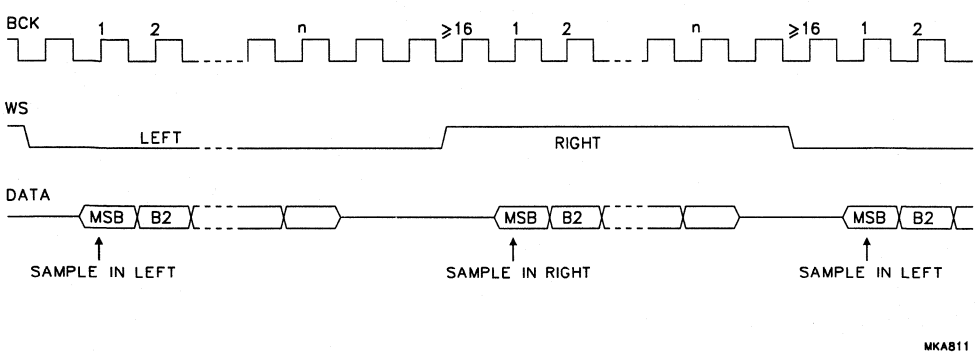


Fig.5 Input signal format (I^2S-bus).

APPLICATION INFORMATION

The TDA1387T offers great ease in designing-in to printed-circuit board due to its small size and low pin count. The TDA1387T being a mixed-signal IC in CMOS, some attention needs to be paid to layout and topology of the application PCB. The following basic rules will yield the desired performance. The most important considerations are:

1. Supply: care should be taken to supply the TDA1387T with a clean, noiseless supply voltage, for a good noise performance of the analog parts of the DAC. Supply purity can easily be achieved by using an RC-filtered supply.
2. Grounding: preferably a ground plane should be used, in order to have a low-impedance return available at any point in the layout. It is advantageous to make a partitioning of the ground plane according to the nature of the expected return currents (digital input returns separate from supply returns separate from the analog section).
3. Topology: the capacitor decoupling high-frequency supply interference from V_{DD} to GND should be placed as close as is physically possible to the IC body, ensuring a low-inductance path to ground. The digital input conductors may be shielded by ground leads running alongside. The placement of a passive ground plane underside the entire IC surface gives 'free' additional decoupling from the IC body to ground as well as providing a shield between the digital input pins and the analog output pins.

Bitstream continuous calibration filter-DAC for CD-ROM audio

TDA1388T

FEATURES

Multiple format input interface

- I^2S-bus and LSB-justified input format compatible
- $1f_s$ input format data rate.

Extensive channel manipulation features

- Separate soft mute on left and right channel
- Channel interchange function (left to right and right to left)
- Monaural function (left to right or right to left)
- True mono function (left plus right)/2.

Digital sound processing

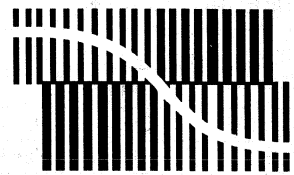
- Separate digital volume control for left and right channels
- Digital tone control, bass boost and treble
- dB-linear volume and tone control (low microcontroller load)
- Digital de-emphasis
- Soft mute.

Advanced audio output configuration

- Stereo line output (under microcontroller volume control)
- Stereo headphone output (under 5-tap potentiometer volume control)
- Line output independent of headphone output volume
- Power on/off click prevention circuitry
- High linearity, dynamic range, low distortion.

General

- Integrated digital filter plus DAC plus headphone driver
- No analog post filter required
- Easy application
- Functions controllable by static pins or by microcontroller interface
- 5 V power supply
- Low power consumption
- Small package size (SO28 and SSOP28).



BITSTREAM CONVERSION

GENERAL DESCRIPTION

The TDA1388T CMOS digital-to-analog bitstream convertor incorporates an up-sampling digital filter and noise shaper, unique signal processing features and integrated line and headphone drivers. The digital processing features are of high sound quality due to the wide dynamic range of the bitstream conversion technique.

The TDA1388T supports the I^2S-bus data input mode with word lengths of up to 20 bits and the LSB justified serial data input format with word lengths of 16, 18 and 20 bits. Two cascaded half-band filters and a sample-and-hold function increase the oversampling rate from $1f_s$ to $64f_s$. A 2nd-order noise shaper converts this oversampled data to a bitstream for the 5-bit continuous calibration digital-to-analog convertors (DACs).

On board amplifiers convert the output current to a voltage signal capable of driving a line output. The signal is also used to feed the integrated headphone amplifiers. The volume of the headphone is controlled by an external potentiometer.

The TDA1388T has special sound processing features for use in CD-ROM audio applications, which can be controlled by static pins or microcontroller interface. These functions are de-emphasis, volume, bass boost, treble, soft mute and the channel manipulation functions needed for ATAPI-compliant functionality in CD-ROM audio processing.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1388T	SO28	plastic small outline package; 28 leads; body width 7.5 mm.	SOT136-1
TDA1388TZ	SSOP28	plastic shrink small outline package; 28 leads; body width 5.3 mm.	SOT341-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage	note 1	4.5	5.0	5.5	V
I_{DD}	supply current	note 2	–	22	–	mA
$V_{FS(rms)}$	full-scale output voltage (RMS value)	V_{DD} = 5 V	0.9	1.0	1.1	V
(THD+N)/S	total harmonic distortion plus noise as a function of signal for the line output	0 dB signal	–	–85	–80	dB
		R_L = 5 kΩ	–	0.006	0.013	%
		–60 dB signal	–	–35	–30	dBA
		R_L = 5 kΩ	–	1.8	3.2	%
	total harmonic distortion plus noise as a function of signal for the headphone output	0 dB signal	–	–65	–60	dB
		R_L = 16 Ω	–	0.056	0.1	%
		0 dB signal	–	–70	–	dB
		R_L = 32 Ω	–	0.032	–	%
		–60 dB signal	–	–35	–30	dBA
		R_L = 16 Ω or R_L = 32 Ω	–	1.8	3.2	%
S/N	signal-to-noise ratio	A-weighted; at code 00000H	90	95	–	dBA
BR	input bit rate at data input	$f_{sys} = 256f_s$	–	$64f_s$	–	bits
		$f_{sys} = 384f_s$	–	$48f_s$	–	bits
f_{sys}	system clock frequency		8.192	–	18.432	MHz
T_{amb}	operating ambient temperature		–20	–	+70	°C

Notes

1. All V_{DD} and V_{SS} pins must be connected to the same supply or ground respectively.
2. Measured at input code 00000H and V_{DD} = 5 V.

BLOCK DIAGRAM

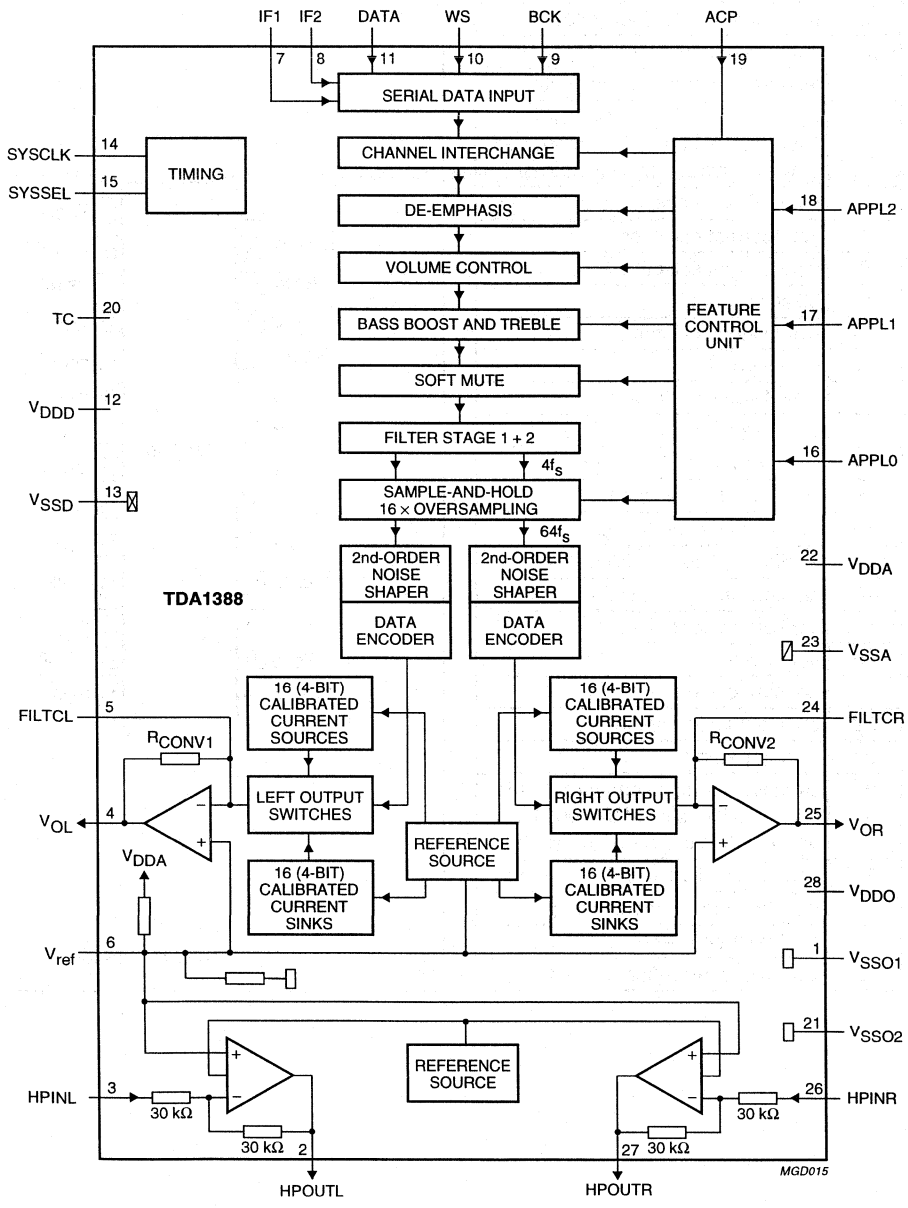


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{SSO}	1	operational amplifier ground
HPOUTL	2	left headphone output voltage
HPINL	3	left headphone input voltage
V_{OL}	4	left channel audio voltage output
FILTCL	5	capacitor for left channel 1st-order filter function, should be connected between this pin and V_{OL} (pin 4)
V_{ref}	6	internal reference voltage
IF1	7	input format selection 1
IF2	8	input format selection 2
BCK	9	bit clock input
WS	10	word selection input
DATA	11	data input
V_{DDD}	12	digital supply voltage
V_{SSD}	13	digital ground
SYSCLK	14	system clock $256f_s$ or $384f_s$
SYSSEL	15	system clock selection
APPL0	16	application mode 0 input
APPL1	17	application mode 1 input
APPL2	18	application mode 2 input
ACP	19	application control input
TC	20	test control
n.c.	21	not connected
V_{DDA}	22	analog supply voltage
V_{SSA}	23	analog ground
FILTCR	24	capacitor for right channel 1st-order filter function, should be connected between this pin and V_{OR} (pin 25)
V_{OR}	25	right channel audio voltage output
HPINR	26	right headphone input voltage
HPOUTR	27	right headphone output voltage
V_{DDO}	28	operational amplifier supply voltage

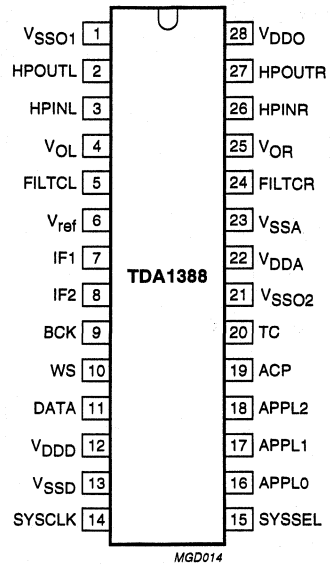


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA1388T CMOS DAC incorporates an up-sampling digital filter, a sample-and-hold register, a noise shaper, continuously calibrated current sources, line amplifiers and headphone amplifiers. The $1f_s$ input data is increased to an oversampled rate of $64f_s$. This high-rate oversampling, together with the 5-bit DAC, enables the filtering required for waveform smoothing and out-of-band noise reduction to be achieved by simple 1st-order analog post-filtering.

System clock

The TDA1388T accommodates slave mode only, this means that in all applications the system devices must provide the system clock. The system frequency is selectable. The options are $256f_s$ and $384f_s$. The system clock must be locked in frequency to the I²S-bus input signals.

Table 1 System clock selection

SYSSEL	DESCRIPTION
0	$256f_s$
1	$384f_s$

Multiple format input interface

The TDA1388T supports the following data input formats;

- I²S-bus with data word length of up to 20 bits.
- LSB justified serial format with data word length of 16, 18 or 20 bits.

Table 2 Data input formats

IF1	IF2	FORMAT
0	0	I²S-bus
0	1	LSB-justified, 16 bits
1	0	LSB-justified, 18 bits
1	1	LSB-justified, 20 bits

The input formats are illustrated in Fig.3. Left and right data-channel words are time multiplexed.

Input mode

The TDA1388T has two input modes, a static-pin mode and a microcontroller mode. In the static-pin mode, the digital sound processing features such as mute left, mute right and de-emphasis are controlled by external pins. The other digital sound processing features have a default value. In the microcontroller mode, all the digital sound processing features can be controlled by the microcontroller. The controllable features are;

- De-emphasis.
- Volume left channel.
- Volume right channel.
- Flat/min/max switch.
- Bass boost.
- Treble.
- Channel manipulation modes.

The selection of one of the two modes is controlled by the ACP pin. When this pin is at logic 0 then the static pin mode will be selected. When the pin is at logic 1 then the microcontroller mode will be selected.

Table 3 Selectable values of the digital sound processing features

FEATURES	STATIC-PIN MODE	MICROCONTROLLER MODE
De-emphasis	0 Hz or 44.1 kHz	0 Hz or 44.1 kHz
Volume left channel	0 dB (fixed)	0 dB to −∞ dB
Volume right channel	0 dB (fixed)	0 dB to −∞ dB
Flat/min/max switch	flat (fixed)	flat/min/max
Bass boost	flat set (fixed)	flat, min or max set
Treble	flat set (fixed)	flat, min or max set
Mute left channel	external pin	selectable (see Table 4)
Mute right channel	external pin	selectable (see Table 4)
Channel manipulation modes	L_CHANNEL = L (fixed)	see Table 10
	R_CHANNEL = R (fixed)	

STATIC-PIN MODE

In the static-pin mode most of the features have a default value (see Table 3). The features that are controlled by the external pins are, mute left channel, mute right channel and de-emphasis.

Table 4 External pin feature control in the static-pin mode

PIN	FEATURE
APPL0	mute left channel
APPL1	mute right channel
APPL2	de-emphasis

MICROCONTROLLER MODE

The exchange of data and control information between the microcontroller and the TDA1388T is accomplished through a serial hardware interface comprising the following pins;

APPL0: microcontroller interface data line.

APPL1: microcontroller interface mode line.

APPL2: microcontroller interface clock line.

Information transfer through the microcontroller bus is organized in accordance with the so-called 'L3' format, in which two different modes of operation can be distinguished; address mode and data transfer mode (see Figs 4 and 5).

The address mode is required to select a device communicating via the L3-bus and to define the destination registers for the data transfer mode. Data transfer for the TDA1388T can only be in one direction, input to the TDA1388T to program its sound processing and other functional features.

Address mode

The address mode is used to select a device for subsequent data transfer and to define the destination registers. The address mode is characterized by APPL1 being LOW and a burst of 8 pulses on APPL2, accompanied by 8 data bits. The fundamental timing is shown in Fig.4. Data bits 0 to 1 indicate the type of the subsequent data transfer as shown in Table 5.

Table 5 Selection of data transfer

BIT 1	BIT 0	TRANSFER
0	0	data (volume left, volume right, bass boost and treble)
0	1	not used
1	0	status (de-emphasis, mode and channel-manipulation)
1	1	not used

Data bits 7 to 2 represent a 6-bit device address, with bit 7 being the MSB and bit 2 the LSB. The address of the TDA1388T is 000101 (bit 7 to bit 2). In the event that the TDA1388T receives a different address, it will deselect its microcontroller interface logic.

Data transfer mode

The selection preformed in the address mode remains active during subsequent data transfers, until the TDA1388T receives a new address command. The fundamental timing of data transfers is essentially the same as in the address mode, shown in Fig.4. The maximum input clock and data rate is $64f_s$. All transfers are bitwise, i.e. they are based on groups of 8 bits. Data will be stored in the TDA1388T after the eighth bit of a byte has been received. A multibyte transfer is illustrated in Fig.6.

Programming the sound processing and other features

The sound processing and other feature values are stored in independent registers. The first selection of the registers is achieved by the choice of data type that is transferred. This is performed in the address mode, BIT 1 and BIT 0 (see Table 5). The second selection is performed by the 2 MSBs of the data byte (BIT 7 and BIT 6). The other bits in the data byte (BIT 5 to BIT 0) is the value that is placed in the selected registers.

When the data transfer of type "data" is selected, the features VOLUME_R, VOLUME_L, BASS BOOST and TREBLE can be controlled. When the data transfer of type "status" is selected, the features MODE, DE-EMPHASIS, CHANNEL_MANIP_R and CHANNEL_MANIP_L can be controlled.

Table 6 Data transfer of type "status"

BIT 7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REGISTER SELECTED
0	M1	M0	DE	OR1	OR0	OL1	OL0	MODE (1 : 0), DEEMPHASIS, CHANNEL_MANIP_R (1 : 0), CHANNEL_MANIP_L (1 : 0)

Table 7 Data transfer of type "data"

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REGISTER SELECTED
0	0	VR5	VR4	VR3	VR2	VR1	VR0	VOLUME_R (5 : 0)
0	1	VL5	VL4	VL3	VL2	VL1	VL0	VOLUME_L (5 : 0)
1	0	X[1]	BB4	BB3	BB2	BB1	BB0	BASS BOOST (4 : 0)
1	1	X[1]	TR4	TR3	TR2	TR1	TR0	TREBLE (4 : 0)

Note

1. X = don't care

MODE: a 2-bit value to program the mode of the sound processing filters of Bass Boost and Treble. There are three modes: flat, min and max.

Table 8 The flat/min/max switch

MODE 1	MODE 0	FUNCTION
0	0	flat
0	1	min
1	0	min
1	1	max

DE-EMPHASIS: a 1-bit value to enable the digital de-emphasis filter.

Table 9 De-emphasis

DEEM	FUNCTION
0	no de-emphasis
1	de-emphasis, 44.1 kHz

CHANNEL_MANIP_R and CHANNEL_MANIP_L: both are a 2 bit value to program the right or left channel manipulation.

Table 10 Channel manipulation modes

CHANNEL_MANIP_L<1 : 0>	CHANNEL_MANIP_R<1 : 0>	L_CHANNEL	R_CHANNEL
00	00	MUTE	MUTE
00	01	MUTE	R
00	10	MUTE	L
00	11	MUTE	(L + R)/2
01	00	R	MUTE
01	01	R	R
01	10	R	L
01	11	R	(L + R)/2
10	00	L	MUTE
10	01	L	R
10	10	L	L
10	11	L	(L + R)/2
11	00	(L + R)/2	MUTE
11	01	(L + R)/2	R
11	10	(L + R)/2	L
11	11	(L + R)/2	(L + R)/2

VOLUME_R: a 6-bit value to program the right channel volume attenuation (VR5 to VR0). The range is 0 dB to −∞ dB in steps of 1 dB.

Table 11 Volume right settings

VR5	VR4	VR3	VR2	VR1	VR0	VOLUME (dB)
0	0	0	0	0	0	0
0	0	0	0	0	1	0
0	0	0	0	1	0	−1
0	0	0	0	1	1	−2
:	:	:	:	:	:	:
1	1	1	0	1	1	−58
1	1	1	1	0	0	−59
1	1	1	1	0	1	−60
1	1	1	1	1	0	−∞
1	1	1	1	1	1	−∞

VOLUME_L: a 6-bit value to program the left channel volume attenuation (VL5 to VL0). The range is 0 dB to −∞ dB in steps of 1 dB.

Table 12 Volume left settings

VR5	VR4	VR3	VR2	VR1	VR0	VOLUME (dB)
0	0	0	0	0	0	0
0	0	0	0	0	1	0
0	0	0	0	1	0	−1
0	0	0	0	1	1	−2
:	:	:	:	:	:	:
1	1	1	0	1	1	−58
1	1	1	1	0	0	−59
1	1	1	1	0	1	−60
1	1	1	1	1	0	−∞
1	1	1	1	1	1	−∞

BASS BOOST: a 5-bit value to program the bass boost setting. The used set depends on the MODE bits.

Table 13 Bass boost settings

BB4	BB3	BB2	BB1	BB0	BASS BOOST		
					FLAT SET (dB)	MIN SET (dB)	MAX SET (dB)
0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0
0	0	0	1	0	0	0	0
0	0	0	1	1	0	0	0
0	0	1	0	0	0	2	2
0	0	1	0	1	0	2	2
0	0	1	1	1	0	4	4
0	0	1	1	0	0	4	4
0	1	0	0	1	0	6	6
0	1	0	0	0	0	6	6
0	1	0	1	1	0	8	8
0	1	0	1	0	0	8	8
0	1	1	0	1	0	10	10
0	1	1	0	0	0	10	10
0	1	1	1	1	0	12	12
0	1	1	1	0	0	12	12
1	0	0	0	0	0	14	14
1	0	0	0	1	0	14	14
1	0	0	1	0	0	16	16
1	0	0	1	1	0	16	16
1	0	1	0	0	0	18	18
1	0	1	0	1	0	18	18
1	0	1	1	1	0	18	20
1	0	1	1	0	0	18	20
1	1	0	0	1	0	18	22
1	1	0	0	0	0	18	22
1	1	0	1	1	0	18	24
1	1	0	1	0	0	18	24
:	:	:	:	:	:	:	:
1	1	1	1	0	0	18	24

TREBLE: a 5-bit value to program the treble setting. The used set depends on the MODE bits.

Table 14 Treble settings

TR4	TR3	TR2	TR1	TR0	TREBLE		
					FLAT SET (dB)	MIN SET (dB)	MAX SET (dB)
0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0
0	0	0	1	0	0	0	0
0	0	0	1	1	0	0	0
0	0	1	0	0	0	2	2
0	0	1	0	1	0	2	2
0	0	1	1	1	0	2	2
0	0	1	1	0	0	2	2
0	1	0	0	1	0	4	4
0	1	0	0	0	0	4	4
0	1	0	1	1	0	4	4
0	1	0	1	0	0	4	4
0	1	1	0	1	0	6	6
0	1	1	0	0	0	6	6
0	1	1	1	1	0	6	6
0	1	1	1	0	0	6	6
:	:	:	:	:	:	:	:
1	1	1	1	0	0	6	6

Flat/min/max setting selection

In the TDA1388T has three setting for the digital sound features bass boost and treble. The possible settings are called 'flat', 'min' and 'max'. The flat setting has no influence on the audio signal, the minimum setting has a small influence on the audio signal and the maximum setting has a large influence on the audio signal. In the static-pin mode, the flat setting is used for the bass boost and treble filters. In the microcontroller mode, all three settings can by controlled by a register.

Channel manipulation modes

In the TDA1388T there is a channel manipulation function implemented. This function has a fixed value in the static-pin mode, the left signal on the left channel and the right signal on the right channel. In the microcontroller mode several option are possible. The different modes are as follows;

- Normal stereo output.
- Left/right reverse output.
- Mono left/right output: (L + R)/2.
- Output muting with soft mute.

De-emphasis

De-emphasis is controlled by an external pin in the static-pin mode and by a register in the microcontroller mode.The digital de-emphasis filter is dimensioned to produce the de-emphasis frequency characteristics for the sample rate 44.1 kHz. With its 18-bit dynamic range, the digital de-emphasis filter of the TDA1388T is a convenient and component saving alternative to analog de-emphasis. De-emphasis is synchronized to the sample clock, so that operation always takes place on complete samples.

Volume control

The volume of the left and right channels are controlled by a fixed value (0 dB) in the static-pin mode and by separate registers in the microcontroller mode. In the microcontroller mode the values of both channels can vary, independent of each other, from 0 dB to $-\infty$ dB.

Since there is no headroom included into the sound control section, the volume control precedes the sound control. Full volume and neutral setting (flat) of the sound control results in full-scale output. Any tone boost will directly cause clipping, which can be avoided by reduction of the volume setting.

Bass boost

A strong bass boost effect, which is useful in compensating for poor response of portable headphone sets, is implemented digitally in the TDA1388T and can be controlled in the microcontroller mode. In the static-pin mode, the flat setting is fixed. In the microcontroller mode, valid settings range from flat (no influence on audio) to +18 dB with step sizes of 2 dB in minimum and to +24 dB with step sizes of 2 dB in maximum. The programmable bass boost filter is a 2nd-order shelving type with a fixed corner frequency of 130 Hz for the minimum setting and a fixed corner frequency of 230 Hz for the maximum setting and has a Butterworth characteristic. Because of the exceptional amount of programmable gain, bass boost should be used with adequate prior attenuation, using the volume control.

Treble

A treble effect is implemented digitally in the TDA1388T and can be controlled in the microcontroller mode. In the static-pin mode, the flat setting is fixed. In the microcontroller mode, valid settings range from flat (no influence on audio) to +6 dB with step sizes of 2 dB in minimum and to +6 dB with step sizes of 2 dB in maximum. The programmable treble filter is a 1st-order shelving type with a fixed corner frequency of 2.8 kHz for the minimum setting and a fixed corner frequency of 5.0 kHz for the maximum setting. Because of the exceptional amount of programmable gain, treble should be used with adequate prior attenuation, using the volume control.

Soft mute

Soft mute is controlled by external pins, for each channel one, in the static-pin mode and by the channel manipulation modes of left or right in the microcontroller mode.

When the mute is active for a channel, the value of the sample is decreased smoothly to zero following a raised cosine curve. 32 coefficients are used to step down the value of the data, each one being used 32 times before stepping on to the next. This amounts to a mute transition of 23 ms at f_s = 44.1 kHz. When the mute is released, the samples are returned to the full level again following a raised cosine curve with the same coefficients being used in the reverse order. The mute, on the left or right channel, is synchronized to the sample clock, so that operation always takes place on complete samples.

Oversampling and noise shaper

The digital filter is four times oversampling filter. It consists of two sections which each increase the sample rate by 2. The 2nd-order noise shaper operates at $64f_s$. It shifts in-band quantization noise to frequencies well above the audio band. This noise shaping technique used in combination with a sign-magnitude coding enables high signal-to-noise ratios to be achieved. The noise shaper outputs a 5-bit PDM bitstream signal to the DAC.

Continuous calibration DAC

The dual 5-bit DAC uses the continuous calibration technique. This method, based on charge storage, involves exact duplication of a single reference current source. In the TDA1388T, 32 such current sources plus 1 spare source are continuously calibrated. The spare source is included to allow continuous convertor operation. The DAC receives a 5-bit data bitstream from the noise shaper. This data is converted so that no current is switched to the output during digital silence (input 00000H). In this way very high signal-to-noise performance is achieved.

Stereo line driver

High precision, low-noise amplifiers together with the internal conversion resistor R_{CONV1} and R_{CONV2} convert the converter output current to a voltage capable of driving a headphone. The voltage is available at V_{OL} and V_{OR} (pins 4 and 25).

Stereo headphone driver

High precision, low-noise amplifiers are capable of driving a headphone load. The voltage is available at HPOUTL and HPOUTR (pins 2 and 27).

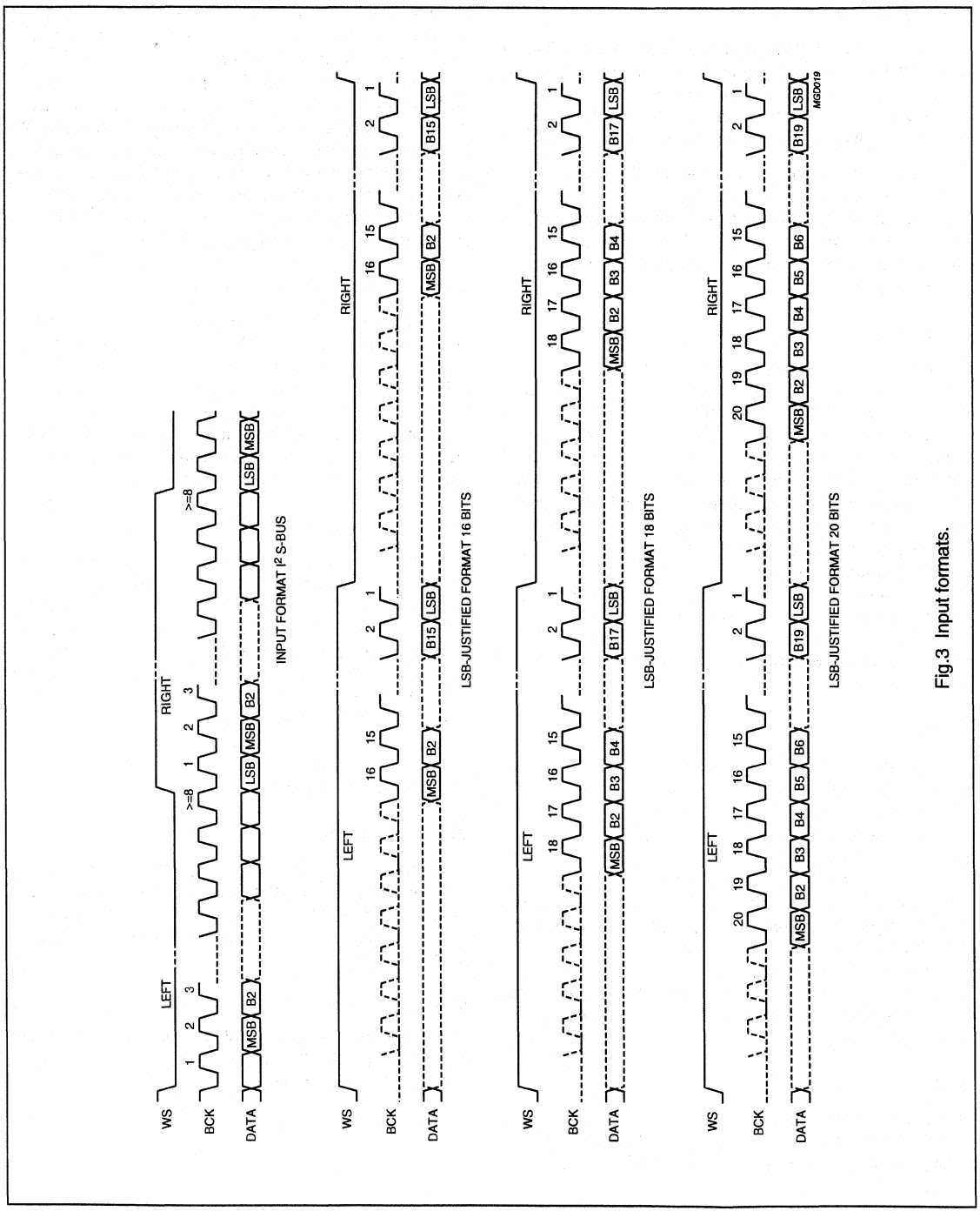


Fig.3 Input formats.

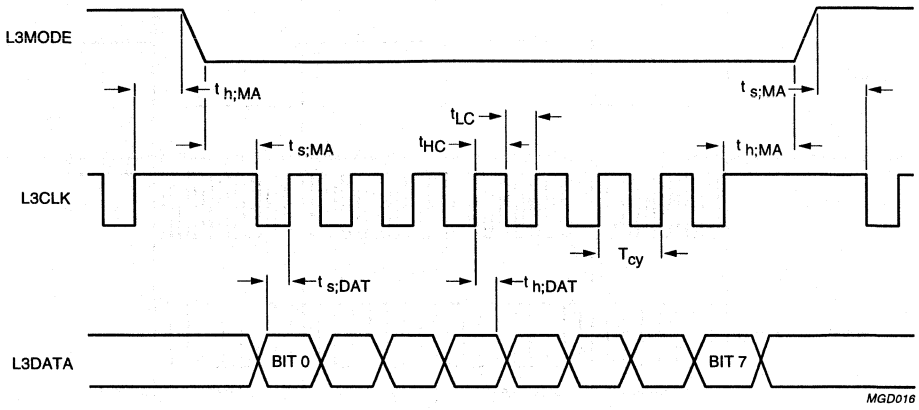


Fig.4 Timing address mode.

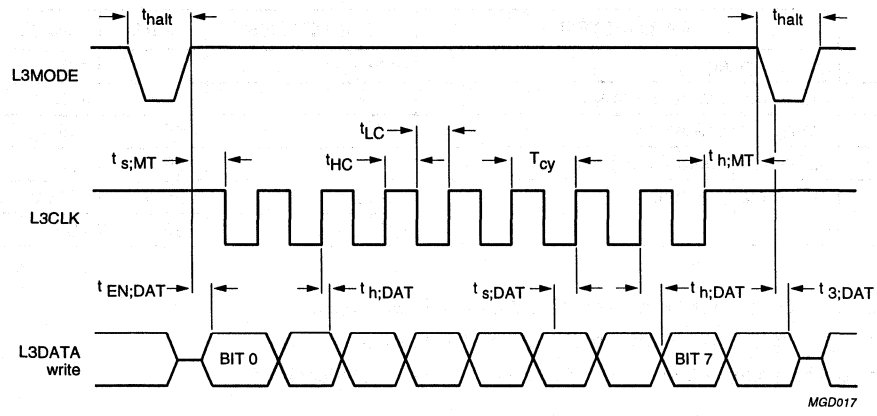


Fig.5 Timing for data transfer mode.

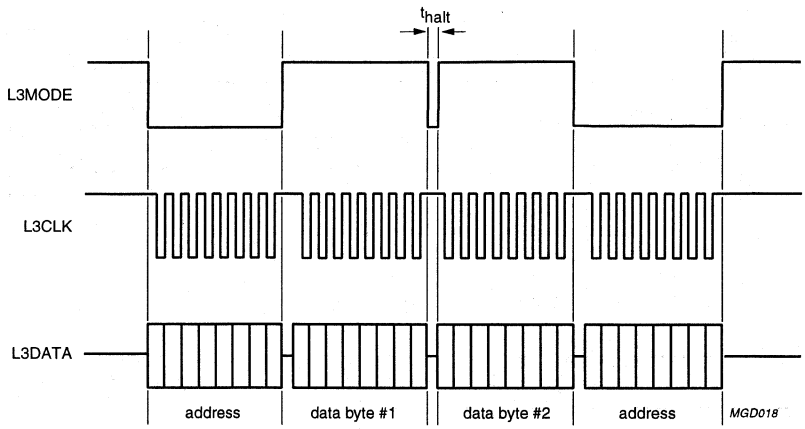


Fig.6 Multibyte transfer.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134). All voltage referenced to ground, $V_{DDD} = V_{DDA} = V_{DDO}$ 5 V; T_{amb} = 25 °C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage	note 1	–	7.0	V
$T_{xtal(max)}$	maximum crystal temperature		–	+150	°C
T_{stg}	storage temperature		–65	+125	°C
T_{amb}	operating ambient temperature		–20	+70	°C
V_{es}	electrostatic handling	note 2	–3000	+3000	V
		note 3	–300	+300	V

Notes

1. All V_{DD} and V_{SS} connections must be made to the same power supply.
2. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor.
3. Equivalent to discharging a 200 pF capacitor via a 2.5 μH series inductor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	SOP28	tbf	K/W
	SSOP28	tbf	K/W

DC CHARACTERISTICS

$V_{DDD} = V_{DDA} = V_{DDO} = 5$ V; $T_{amb} = 25$ °C; $R_L = 5$ kΩ; all voltages referenced to ground (pins 1, 13 and 23); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage	note 1	4.5	5.0	5.5	V
V_{DDA}	analog supply voltage	note 1	4.5	5.0	5.5	V
V_{DDO}	operational amplifier supply voltage	note 1	4.5	5.0	5.5	V
I_{DDD}	digital supply current	at digital silence	–	7.0	–	mA
I_{DDA}	analog supply current	at digital silence	–	5.0	–	mA
I_{DDO}	operational amplifier supply current	at digital silence	–	10	–	mA
P_{tot}	total power dissipation	note 2	–	110	–	mW
Digital input pins						
V_{IH}	HIGH level input voltage		$0.7V_{DDD}$	–	$V_{DDD} + 0.5$	V
V_{IL}	LOW level input voltage		–	–	$0.3V_{DDD}$	V
$\|I_{LI}\|$	input leakage current		–	–	10	μA
C_{in}	input capacitance		–	–	10	pF
Analog audio pins						
V_{ref}	reference voltage	with respect to V_{SSA}	$0.45V_{DDA}$	$0.5V_{DDA}$	$0.55V_{DDA}$	V
$R_{out(ref)}$	output reference resistance		–	3	–	kΩ
R_{CONV}	current-to-voltage conversion resistor		–	2.0	–	kΩ
$I_{o(max)}$	maximum output current	(THD+N)/S < 0.1% $R_L = 32$ Ω	–	88	–	mA
		(THD+N)/S < 0.1% $R_L = 16$ Ω	–	44	–	mA
C_L	output load capacitance	note 3	–	–	50	pF

Notes

1. All power supply pins (V_{DD} and V_{SS}) must be connected to the same external power supply unit.
2. No operational amplifier load resistor.
3. Load capacitance larger than 50 pF, a 22 μH inductor in parallel with a 270 Ω resistor must be inserted between the load and the operational amplifier output.

AC CHARACTERISTICS (ANALOG)

$V_{DDD} = V_{DDA} = V_{DDO} = 5$ V; $f_i = 1$ kHz; $T_{amb} = 25$ °C; $R_L = 5$ kΩ all voltages referenced to ground (pins 1, 13 and 23); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RES	resolution		–	–	18	bits
$V_{FS(rms)}$	output voltage swing (RMS value)	note 1	0.9	1.0	1.1	V
$V_{DC(os)}$	output voltage DC offset with respect to reference voltage level V_{ref}		–	20	–	mV
SVRR	supply voltage ripple rejection V_{DDA} and V_{DDO}	$f_{ripple} = 1$ kHz; $V_{ripple(p-p)} = 100$ mV(peak); $C_{pin} = 10$ µF	–	40	–	dB
$\lvert\Delta V_o\rvert$	unbalance between the 2 DAC voltage outputs	maximum volume	–	0.1	–	dB
α_{ct}	crosstalk between the 2 DAC voltage outputs for line outputs	$R_L = 5$ kΩ, note 2	–	90	–	dB
	crosstalk between the 2 DAC voltage outputs for headphone outputs	$R_L = 16$ kΩ, note 2	–	60	–	dB
		$R_L = 32$ kΩ, note 2	–	65	–	dB
(THD+N)/S	total harmonic distortion plus noise as a function of signal for the line output	0 dB signal	–	–85	–80	dB
		$R_L = 5$ kΩ	–	0.006	0.013	%
		–60 dB signal	–	–35	–30	dBA
		$R_L = 5$ kΩ	–	1.8	3.2	%
	total harmonic distortion plus noise as a function of signal for the headphone output	0 dB signal	–	–65	–60	dB
		$R_L = 16$ kΩ	–	0.056	0.1	%
		0 dB signal	–	–70	–	dB
		$R_L = 32$ kΩ	–	0.032	–	%
		–60 dB signal	–	–35	–30	dBA
		$R_L = 16$ kΩ or $R_L = 32$ kΩ	–	1.8	3.2	%
S/N	signal-to-noise ratio at bipolar zero	A weighting; at code 00000H	90	95	–	dBA

Notes

1. Proportional to V_{DDA}.
2. One output digital silence, the other maximum volume.

AC CHARACTERISTICS (DIGITAL)

$V_{DDD} = V_{DDA} = V_{DDO} = 4.5$ to 5.5 V; $T_{amb} = -20$ to +70 °C; $R_L = 5$ kΩ; all voltages referenced to ground (pins 1, 13 and 23); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX	UNIT
T_{cy}	clock cycle	$f_{sys} = 256f_s$	81.3	88.6	122	ns
		$f_{sys} = 384f_s$	54.2	59.1	81.3	ns
t_{CWL}	f_{sys} LOW level pulse width		22	–	–	ns
t_{CWH}	f_{sys} HIGH level pulse width		22	–	–	ns
Serial input data timing (see Fig.7)						
BR	clock input = data input rate	$f_{sys} = 256f_s$	–	$64f_s$	–	
		$f_{sys} = 384f_s$	–	$48f_s$	–	
f_{sys}	system clock frequency		8.192	–	18.432	MHz
f_{WS}	word selection input frequency		–	44.1	48	kHz
t_r	rise time		–	–	20	ns
t_f	fall time		–	–	20	ns
$t_{BCK(H)}$	bit clock HIGH time		55	–	–	ns
$t_{BCK(L)}$	bit clock LOW time		55	–	–	ns
$t_{s;DAT}$	data set-up time		10	–	–	ns
$t_{h;DAT}$	data hold time		20	–	–	ns
$t_{s;WS}$	word selection set-up time		20	–	–	ns
$t_{h;WS}$	word selection hold time		10	–	–	ns

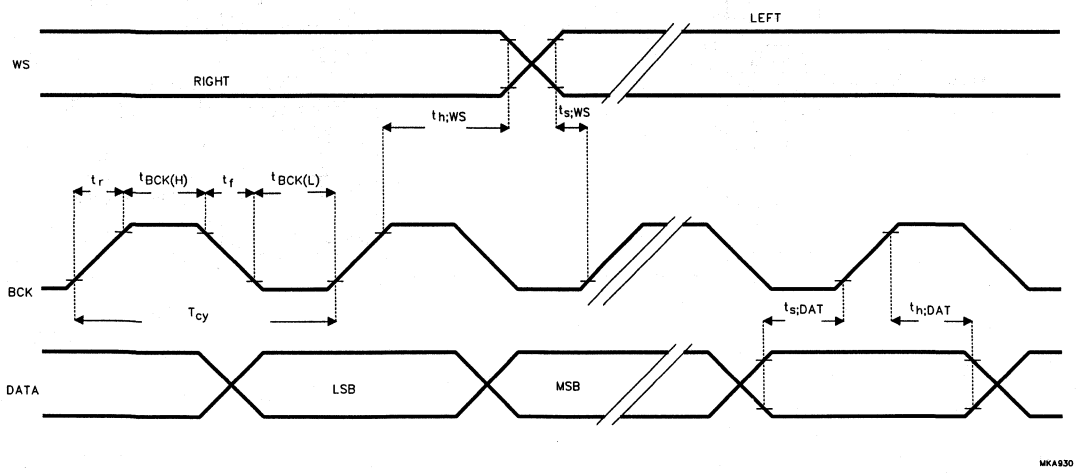
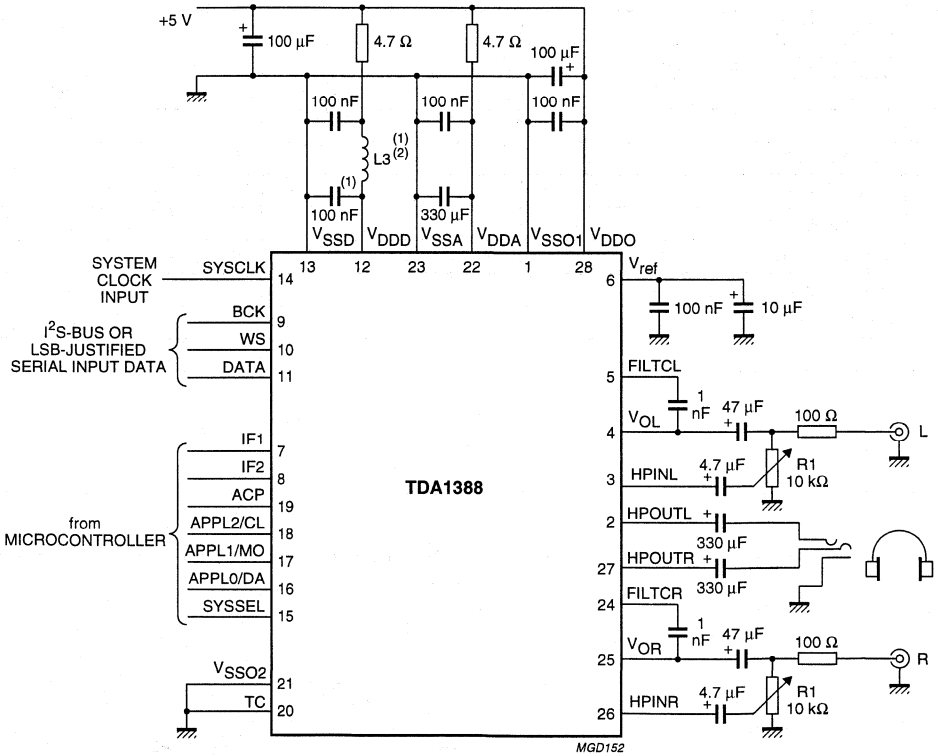


Fig.7 Timing and input signals.

TEST AND APPLICATION INFORMATION



(1) Optional.
(2) Chip inductor BLM32A07.

Fig.8 Application diagram.

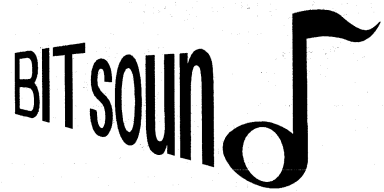
BITsound; multimedia digital sound IC TDA1396

FEATURES

- 16-bit true stereo audio CODEC
- Full duplex operation with different sample rate inputs and outputs
- Full stereo Input/Output (I/O) capabilities at sample rates from 3.6 to 55 kHz in infinite steps
- 6 stereo channels MPC3 compatible digital mixer
- 3 stereo analog inputs; 1 analog output
- 2 digital inputs; 1 digital output
- Adaptive sample rate conversion on PCM in and out
- Adaptive sample rate conversion on all digital inputs and outputs
- Preamplifier with Automatic Gain Control (AGC) for direct microphone input
- Integrated digital music synthesis
- Incredible Sound™ 3D enhancement
- Hardware echo cancellation support
- MIDI MPU-401 Interface
- Game Port with quad timer supporting up to two joysticks
- Two button hardware interface for volume up/down control
- Supports IMA ADPCM, A-Law and micro-Law compression and decompression
- Power management
- Plug & Play interface, supporting 6 logical devices
- Software support for Windows™ 3.1x, Windows™ 95
- Full 16-bit ISA address decode
- 24 mA ISA-Bus drive capability
- Type 'F' DMA timing
- SoundBlaster™ 16 and Windows™ Sound System(WSS) compatibility
- 128-pin LQFP package.

APPLICATIONS

- PC sound cards
- PC motherboards.



GENERAL DESCRIPTION

The TDA1396 BITsound(1) is a low cost digital audio solution for multimedia PC applications.

The TDA1396 is an integrated digital audio solution for a PC sound card, notebook and motherboard applications. This single chip solution offers Philips patented bitstream CODEC performance with 16-bit dynamic range, while enabling recording and playback of high performance stereo audio and music.

The TDA1396 is the first PC CODEC solution capable of mixing 'digitally' all stereo audio sources from three analog and three digital inputs. The dual mixer concept allows separated mixing for record and playback. With its digital inputs, patented 'sample rate conversion' and digital mixing, external DACs for use with digital sources are unnecessary, leaving for a much simpler and cost effective integration into a PC audio design.

Integrated on-chip are both a music synthesizer and Philips patented Incredible Sound audio enhancement.

This chip supports host software acoustic echo cancellation.

This Philips PC audio solution is fully compatible with all current PC standards including SoundBlaster™ 16 and Windows™ Sound System(2).

The advanced integration of other features such as Game Port with quad timer, Wave table synthesizer interface and MIDI interface make the TDA1396 the competitive choice for the next audio add-in card, motherboard or notebook computer applications.

(1) BITsound is the development name for this project.
(2) All trademarks are properties of their respective owners. This hardware incorporates Eusynth music synthesis software.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	supply voltage (5 V I/O)		4.75	5.0	5.25	V
V_{DDA}	supply voltage (core and analog parts)		3.0	3.3	3.6	V
THD + N	total harmonic distortion + noise, ADC and DAC	0 dB; 1 kHz	–	–85	–80	dB
		–60 dB; 1 kHz	–	–35	–30	dBA
S/N	signal to noise at full-scale input	from any line level input to I^2S output; all other channels muted	85	90	–	dBA
T_{amb}	operating ambient temperature		0	25	70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1396H	LQFP128	plastic low profile quad flat package; 128 leads; body 14 × 20 × 1.4 mm	SOT425-1

BLOCK DIAGRAM

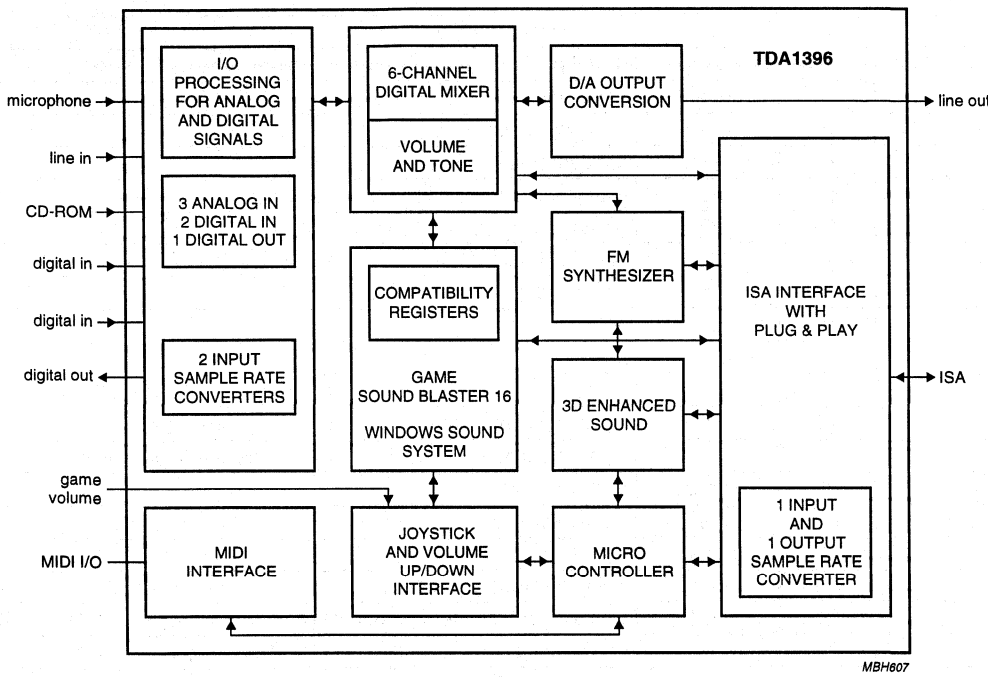


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	I/O	DESCRIPTION[1]
SA(4)	1	I	digital input address line 4
SA(3)	2	I	digital input address line 3
SA(2)	3	I	digital input address line 2
SA(1)	4	I	digital input address line 1
SA(0)	5	I	digital input address line 0
V_{DDD3_6}	6	supply	3.3 V digital supply voltage
V_{SSD_10}	7	supply	digital ground
n.c.	8	open	not connected
n.c.	9	open	not connected
n.c.	10	open	not connected
DRQ3	11	O	digital output for DMA channel request line 3 (n = 0,1,3)
DRQ1	12	O	digital output for DMA channel request line 1 (n = 0,1,3)
DRQ0	13	O	digital output for DMA channel request line 0 (n = 0,1,3)
n.c.	14	open	not connected
n.c.	15	open	not connected
n.c.	16	open	not connected
DACK3	17	I	digital input for DMA request acknowledge line 3 (as DRQn)
DACK1	18	I	digital input for DMA request acknowledge line 1 (as DRQn)
DACK0	19	I	digital input for DMA request acknowledge line 0 (as DRQn)
V_{SSD_11}	20	supply	digital ground
V_{DDD3_7}	21	supply	3.3 V digital supply voltage
V_{SSD_12}	22	supply	digital ground
V_{DDD3_8}	23	supply	3.3 V digital supply voltage
IRQ15	24	O	digital output for interrupt request line 15 (n = 3, 4, 5, 7, 9, 10, 11, 12, 15)
IRQ12	25	O	digital output for interrupt request line 12 (n = 3, 4, 5, 7, 9, 10, 11, 12, 15)
IRQ11	26	O	digital output for interrupt request line 11 (n = 3, 4, 5, 7, 9, 10, 11, 12, 15)
IRQ10	27	O	digital output for interrupt request line 10 (n = 3, 4, 5, 7, 9, 10, 11, 12, 15)
IRQ9	28	O	digital output for interrupt request line 9 (n = 3, 4, 5, 7, 9, 10, 11, 12, 15)
V_{DDD5_3}	29	supply	5 V digital supply voltage
V_{SSD5_3}	30	supply	digital ground
IRQ7	31	O	digital output for interrupt request line 7 (n = 3, 4, 5, 7, 9, 10, 11, 12, 15)
IRQ5	32	O	digital output for interrupt request line 5 (n = 3, 4, 5, 7, 9, 10, 11, 12, 15)
IRQ4	33	O	digital output for interrupt request line 4 (n = 3, 4, 5, 7, 9, 10, 11, 12, 15)
IRQ3	34	O	digital output for interrupt request line 3 (n = 3, 4, 5, 7, 9, 10, 11, 12, 15)
V_{DDD_5V}	35	supply	5 V supply for game port
GBBB	36	I	digital joystick b; button 2; pull-up
GBBA	37	I	digital joystick b; button 1; pull-up
GABB	38	I	digital joystick a; button 2; pull-up
GABA	39	I	digital joystick a; button 1; pull-up
GBRY	40	I	analog joystick b; y position

SYMBOL	PIN	I/O	DESCRIPTION[1]
GBRX	41	I	analog joystick b; x position
GARY	42	I	analog joystick a; y position
GARX	43	I	analog joystick a; x position
V_{DDA}	44	supply	3.3 V analog supply voltage
AGND	45	supply	analog ground
OUTR	46	O	analog line output right channel
AGND	47	supply	analog ground
V_{DDA}	48	supply	3.3 V analog supply voltage
OUTL	49	O	analog line output left channel
RTCB[TST1]	50	I	digital test pin 1; in application connected to ground
MICL	51	I	analog microphone input left channel
V_{ref}	52	O	analog reference voltage ADC
MICR	53	I	analog microphone input right channel
AGND	54	supply	analog ground
V_{DDA}	55	supply	3.3 V analog supply voltage
VCOM	56	O	analog 1.65 V reference voltage V_{DDA2}
LINEL	57	I	analog line input left channel
TST_IN[TST2]	58	I	digital test pin 2; in application connected to ground
LINER	59	I	analog line input right channel
SHTCB[TST3]	60	I	digital test pin 3; in application connected to ground
CDL	61	I	analog CD input left channel
TSCAN[TST4]	62	I	digital test pin 4; in application connected to ground
CDR	63	I	analog CD input right channel
$V_{ref(n)}$	64	I	analog 0 V reference voltage ADC (negative)
$V_{ref(p)}$	65	I	analog 3.3 V reference voltage ADC (positive)
XTALGND	66	supply	digital ground
XTALCLK	67	I	digital input for external clock (14.31818 MHz)
DIGAUD_BCK	68	I	digital I^2S input bit clock
DIGAUD_WS	69	I	digital I^2S input word select
DIGAUD_SD	70	I	digital I^2S input data
V_{SSD_1}	71	supply	digital ground
SCK	72	O	digital I^2S output bit clock
WS	73	O	digital I^2S output word select
SD	74	O	digital I^2S output data
V_{SSD_2}	75	supply	digital ground
FM_SD	76	I	digital input for data
FM_BCK	77	I	digital input for bit clock
FM_WS	78	I	digital input for word select
FM_SMPBD	79	I	digital input for word select
V_{DDD3_1}	80	supply	3.3 V digital supply voltage
V_{SSD_3}	81	supply	digital ground

SYMBOL	PIN	I/O	DESCRIPTION[1]
V_{DDD3_2}	82	supply	3.3 V digital supply voltage
V_{SSD_4}	83	supply	digital ground
V_{DDD5_1}	84	supply	5 V digital supply voltage
V_{SSD5_1}	85	supply	digital ground
MIDI_IN	86	I	digital MIDI input
MIDI_OUT	87	O	digital MIDI output
V_{SSD_5}	88	supply	digital ground
V_{DDD3_3}	89	supply	3.3 V digital supply voltage
VOL_UP	90	I	digital volume control; up button
VOL_DOWN	91	I	digital volume control; down button
$V_{SSA\ PLL}$	92	supply	PLL analog ground
$V_{DDA\ PLL}$	93	supply	PLL 3.3 V analog supply voltage
TST5	94	I	digital test pin 5; in application connected to ground
SLOT	95	I	digital signal to indicate 8 or 16-bit ISA slot
V_{SSD_6}	96	supply	digital ground
V_{DDD3_4}	97	supply	3.3 V digital supply voltage
FS256	98	O	digital bit clock at $256f_s$
n.c.	99	open	not connected
RESET	100	I	digital input for reset from ISA bus
V_{DDD5_2}	101	supply	5 V digital supply voltage
V_{SSD5_2}	102	supply	digital ground
SD(7)	103	I/O	digital input/output data line 7
SD(6)	104	I/O	digital input/output data line 6
SD(5)	105	I/O	digital input/output data line 5
SD(4)	106	I/O	digital input/output data line 4
SD(3)	107	I/O	digital input/output data line 3
SD(2)	108	I/O	digital input/output data line 2
SD(1)	109	I/O	digital input/output data line 1
SD(0)	110	I/O	digital input/output data line 0
V_{DDD3_5}	111	supply	3.3 V digital supply voltage
V_{SSD_7}	112	supply	digital ground
AEN	113	I	digital input address enable line
IOR	114	I	digital input for I/O read enable signal
IOW	115	I	digital input for I/O write enable signal
V_{SSD_8}	116	supply	digital ground
SA(15)	117	I	digital input address line 15
SA(14)	118	I	digital input address line 14
SA(13)	119	I	digital input address line 13
SA(12)	120	I	digital input address line 12
SA(11)	121	I	digital input address line 11
SA(10)	122	I	digital input address line 10

SYMBOL	PIN	I/O	DESCRIPTION[1]
SA(9)	123	I	digital input address line 9
SA(8)	124	I	digital input address line 8
V_{SSD_9}	125	supply	digital ground
SA(7)	126	I	digital input address line 7
SA(6)	127	I	digital input address line 6
SA(5)	128	I	digital input address line 5

Note

1. Digital; all digital levels at 5 V unless otherwise indicated.

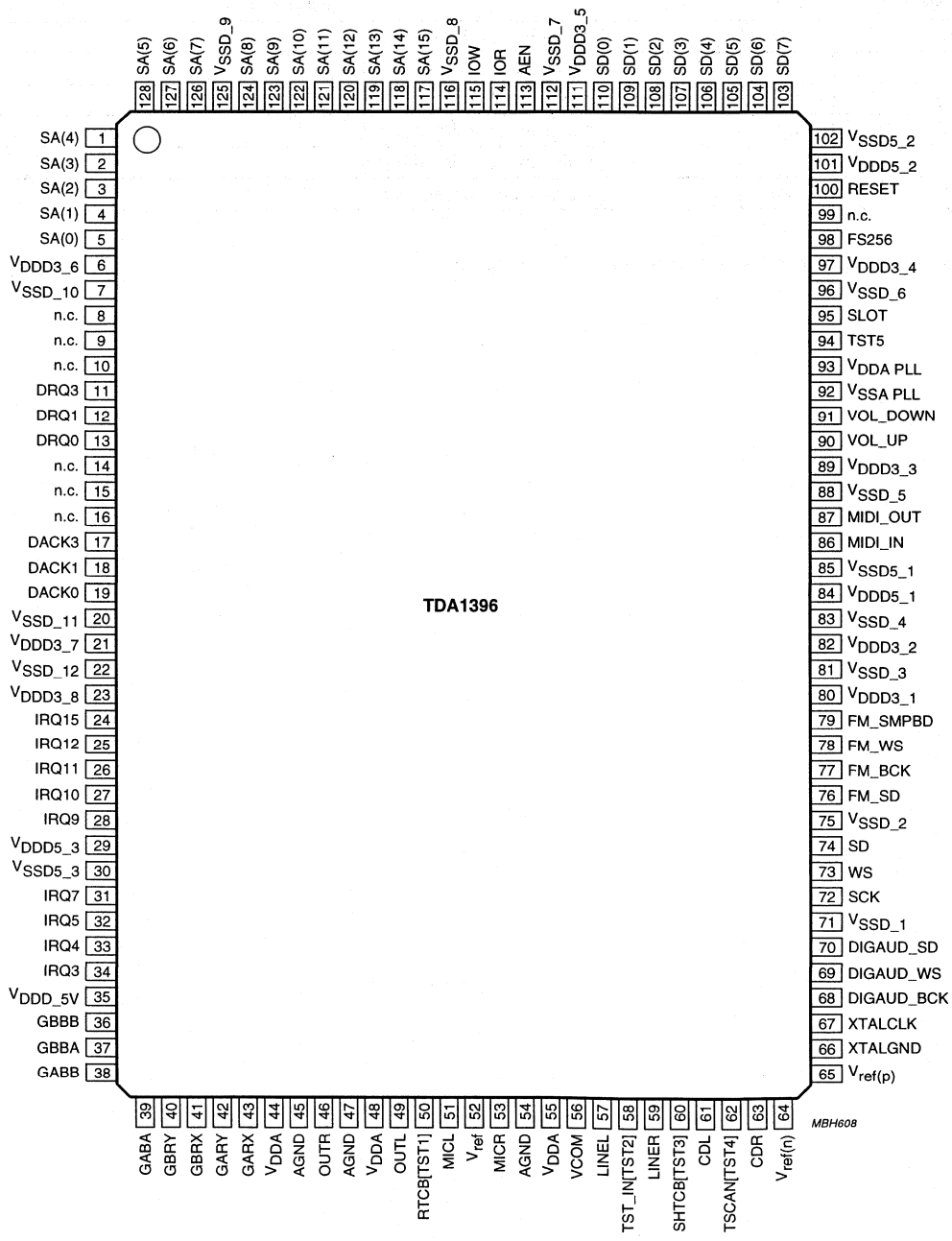


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Fully digital solution

For the highest flexibility and outstanding audio performance all possible internal functions have been achieved in the digital domain.

Full duplex Audio CODEC

The TDA1396 has all required Analog-to-Digital (A/D) and Digital-to-Analog (D/A) functionality on-chip. It offers a number of analog and digital inputs for a variety of different signal sources, e.g. analog microphone (with fixed gain and/or AGC), stereo analog or digital line input, stereo analog or digital CD audio etc.

A wide range of input sampling rates is accepted without any additional hardware or software. These CODEC functions are derived from the Philips world famous bitstream digital audio IC family to make the highest audio performance accessible in the PC-world.

SoundBlaster™ support

The TDA1396 supports SoundBlaster ™-Pro and SoundBlaster™-16 compatibility. A complete register set is integrated to support all required functionality.

Windows™ Sound System (WSS) support

The TDA1396 supports WWS for business audio and Windows-based multimedia application.

Compression/decompression

IMA ADPCM, A-Law and micro-Law compression algorithms are supported.

Digital mixer

The system includes a sophisticated 6-stereo channel MPC3 compatible digital mixer that features volume, treble and bass control at the finest resolution available. A dual mixer allows separated mixing for record and playback.

Digital and analog inputs

The TDA1396 provides 3 stereo analog inputs and 2-multistandard digital inputs.

Digital output

The system contains 1 multistandard digital output.

Analog output

The TDA1396 offers a versatile analog output that can be fed directly to a power amplifier.

Sample rate converters

There are 3 input and 1 output high quality Sample Rate Converters (SRCs) used. They can handle sample rates from 3.6 to 55 kHz in infinite steps.

Integrated FM synthesis

The system features integrated OPL3 compatible FM synthesis on-chip.

Integrated 3D enhanced audio

The system features Philips Incredible Sound implemented on-chip software.

Echo cancellation support

The chip supports host software acoustic echo cancellation.

MIDI/MPU-401 support

The TDA1396 supports MPU-401 MIDI. All necessary components are included in the device.

Game/Joystick Port support

A Game/Joystick Port interface and a quad timer are integrated. All functions for direct connection to the port is integrated in the device.

Hardware volume control

The device is equipped with up and down switch inputs for direct volume control.

Plug & Play compatible ISA bus interface

The TDA1396 incorporates a function block that makes it compliant with the Plug & Play specification. All system elements are automatically configured when the system is powered up.

Power management

The system offers the possibility to power down blocks that are currently not in use to fulfil power management requirements.

Package

The TDA1396 is available in a LQFP128 package.

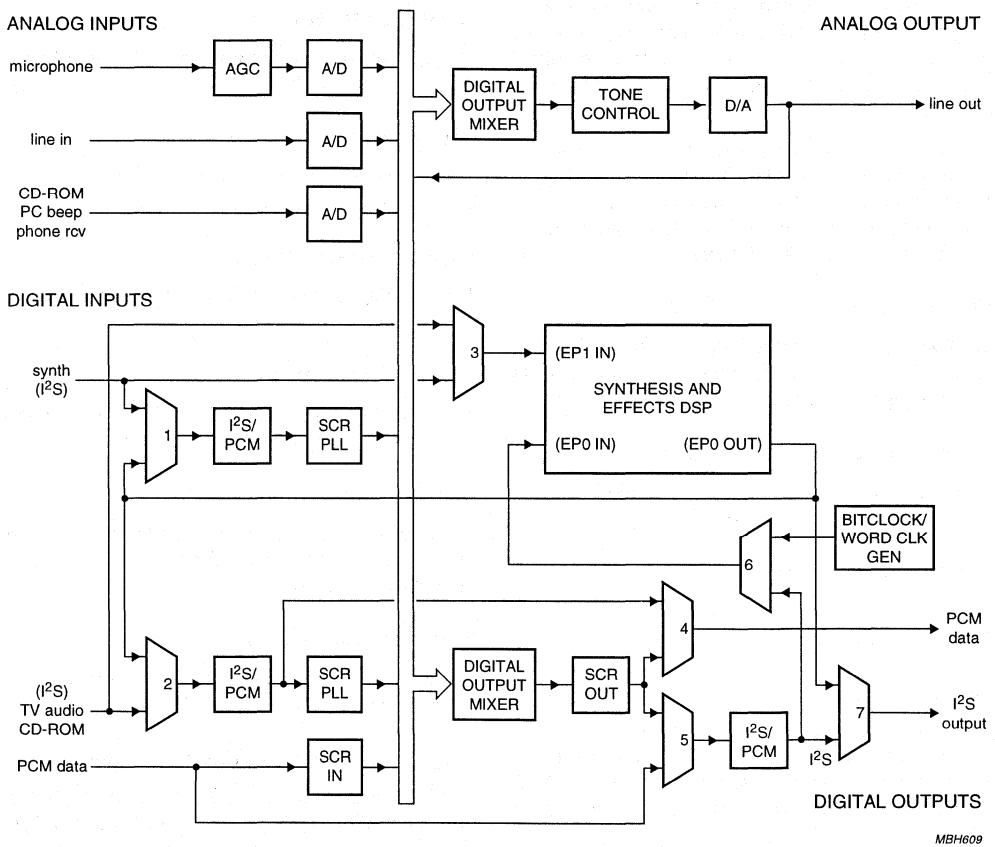


Fig.3 Functional diagram of mixer; (TDA1396 audio I/O processing).

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
T_j	junction temperature	0	–	125	°C
T_{amb}	operating ambient temperature	0	25	70	°C
T_{stg}	storage temperature	–55	–	+150	°C

DC CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage (5 V I/O)	4.75	5.0	5.25	V
V_{DDA}	analog supply voltage (core and analog parts)	3.0	3.3	3.6	V
I_{DDD}	digital supply current 5 V parts	–	10	–	mA
I_{DDA}	analog supply current 3.3 V parts	–	180	–	mA

AC CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Analog-to-Digital Converter (ADC)						
$V_{i(FS)\ rms}$	full-scale input voltage (RMS value)		–	0.66	–	V
THD + N	total harmonic distortion plus noise	0 dB; 1 kHz	–	–85	–80	dB
		–60 dB; 1 kHz	–	–35	–30	dBA
S/N	signal-to-noise ratio	V_i = 0 V	90	95	–	dBA
f_s	sample frequency ($128f_s$)		–	7.15	–	MHz
System performance (capture)						
S/N_{FS}	signal-to-noise ratio at full-scale input	from any line level input to I^2S output; all other channels muted	85	90	–	dBA
THD_{FS}	total harmonic distortion at full-scale input	from any line level input to I^2S output; all other channels muted	–	–80	–75	dB
Digital-to-Analog Converter (DAC)						
$V_{o(FS)\ rms}$	full-scale output voltage (RMS value)		–	0.66	–	V
THD + N	total harmonic distortion plus noise	0 dB; 1 kHz	–	–85	–80	dB
		–60 dB; 1 kHz	–	–35	–30	dBA
S/N	signal-to-noise ratio	V_i = 0 V	90	95	–	dBA
f_s	sample frequency ($128f_s$)		–	7.15	–	MHz

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
System performance (playback)						
S/N_{FS}	signal-to-noise ratio at full-scale input	from I^2S input to line level output; all other channels muted	85	90	–	dBA
THD_{FS}	total harmonic distortion at full-scale input	from I^2S input to line level output; all other channels muted	–	–80	–75	dB
Volume control						
$G_{max(vol)}$	maximum gain (volume)		–	0	–	dB
α_{max}	maximum attenuation		–	∞	–	dB
$G_{step(vol)}$	step size (volume)		–	1.0	–	dB
N_{steps}	number of steps		–	2^{12}	–	
Tone control						
BASS						
$B_{B(max)}$	maximum bass boost	20 Hz; 0 dB at 1 kHz	–	13.5	–	dB
α_{max}	maximum attenuation	20 Hz; 0 dB at 1 kHz	–	9.0	–	dB
$G_{step(bass)}$	step size		–	1.5	–	dB
N_{steps}	number of steps		–	16	–	
TREBLE						
$T_{B(max)}$	maximum treble boost	20 kHz; 0 dB at 1 kHz	–	12.0	–	dB
α_{max}	maximum attenuation	20 kHz; 0 dB at 1 kHz	–	10.5	–	dB
$G_{step(treble)}$	step size		–	1.5	–	dB
N_{steps}	number of steps		–	16	–	
AGC and microphone inputs						
$V_{i(rms)}$	maximum input sensitivity voltage (RMS value)		–	10	–	mV
G	gain control range		–	26	–	dB
Z_i	input impedance		–	10	–	kΩ
$t_{att(FS)}$	full-scale attack time carouser		–	10	–	ms
$t_{decay(FS)}$	full-scale decay time		–	300	–	ms

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Game Port						
$Z_{joy,min}$	minimum joystick impedance		–	0	–	kΩ
$Z_{joy,max}$	maximum joystick impedance		–	100	300	kΩ
I_{sense}	sense current		–	10	–	μA
t_d	fixed delay time	note 1	–	24	–	μs
δt_d	variable delay time	note 1	–	11	–	μs/kΩ
	accuracy	note 2	–	8	–	bits
t_{step}	time step		–	–	6	μs

Notes

1. Delay is given by the expression (delay in μs, R in kΩ): $t_d = 24 + 11 \times R$.
2. Accuracy and time step are related parameters; both are based on the assumption that 300 kΩ coincides with approximately 512 user units (stated otherwise, that 100 kΩ coincides with approximately 180 user units) so the maximal time step equals: $\frac{300 \times 11}{512} \approx 6$ μs.

APPLICATION INFORMATION

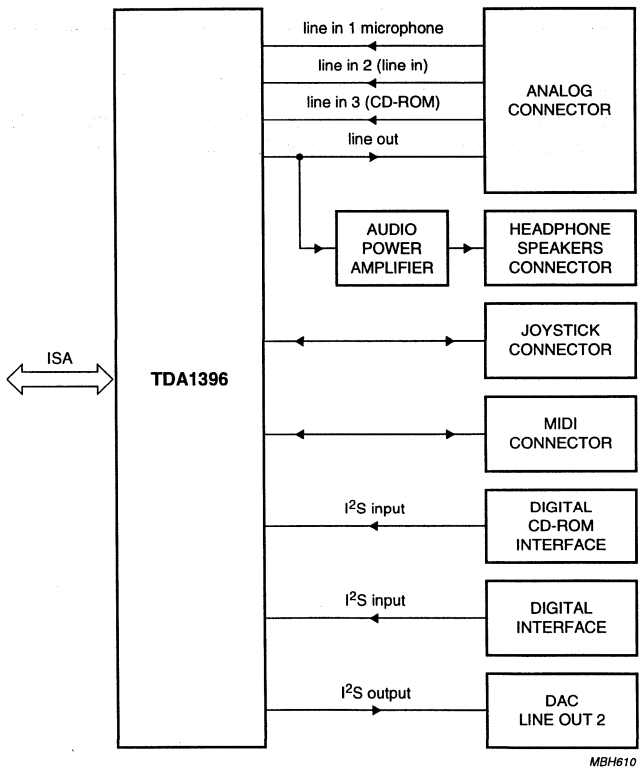


Fig.4 Application diagram.

2 × 6 W stereo car radio power amplifier TDA1517

FEATURES

- Requires very few external components
- High output power
- Fixed gain
- Good ripple rejection
- Mute/standby switch
- Load dump protection
- AC and DC short-circuit safe to ground and V_P
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs (V_P = 0 V)
- No switch-on/switch-off plop
- Electrostatic discharge protection
- Compatible with TDA1519 (except gain).

GENERAL DESCRIPTION

The TDA1517 is an integrated class-B dual output amplifier in a plastic single in-line medium power package with fin; 9 leads (SIL9MPF) and a plastic heat-dissipating dual in-line package (HDIP18). The device is primarily developed for car radio and multi-media applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage					
	operating		6.0	14.4	18.0	V
	non-operating		–	–	30.0	V
	load dump protected		–	–	45.0	V
I_{ORM}	repetitive peak output current		–	–	2.5	A
$I_{q(tot)}$	total quiescent current		–	40	80	mA
I_{sb}	standby current		–	0.1	100	μA
I_{sw}	switch-on current		–	–	40	μA
$\|Z_I\|$	input impedance		50	–	–	kΩ
P_o	output power	R_L = 4 Ω; THD = 0.5%	–	5	–	W
		R_L = 4 Ω; THD = 10%	–	6	–	W
SVRR	supply voltage ripple rejection	f_i = 100 Hz to 10 kHz	48	–	–	dB
α_{cs}	channel separation		40	–	–	dB
G_v	closed loop voltage gain		19	20	21	dB
$V_{no(rms)}$	noise output voltage (RMS value)		–	50	–	μV
T_c	crystal temperature		–	–	150	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1517	SIL9MPF	plastic single in-line medium power package with fin; 9 leads	SOT110-1
TDA1517P	HDIP18	plastic heat-dissipating dual in-line; 18 leads	SOT398-1

BLOCK DIAGRAM

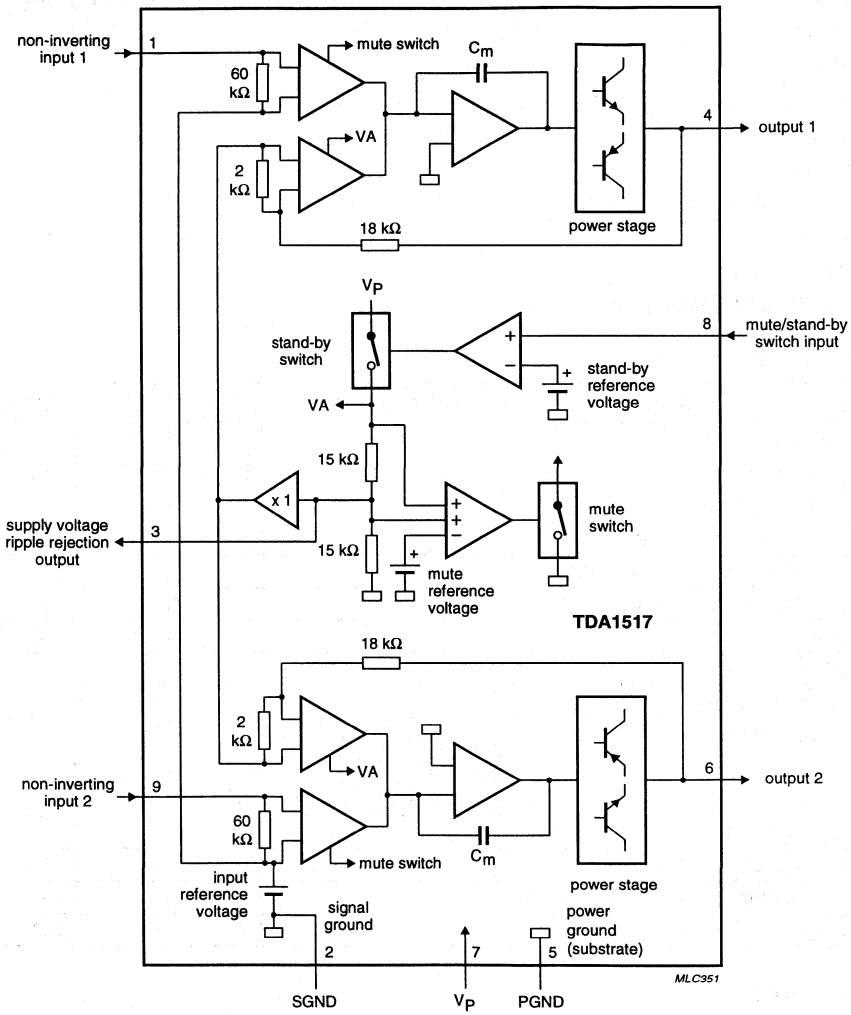


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
−INV1	1	non-inverting input 1
SGND	2	signal ground
SVRR	3	supply voltage ripple rejection output
OUT1	4	output 1
PGND	5	power ground
OUT2	6	output 2
V_P	7	supply voltage
M/SS	8	mute/standby switch input
−INV2	9	non-inverting input 2

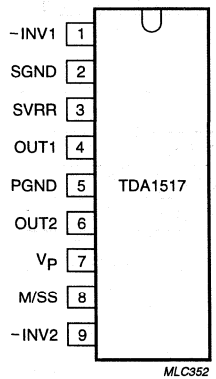
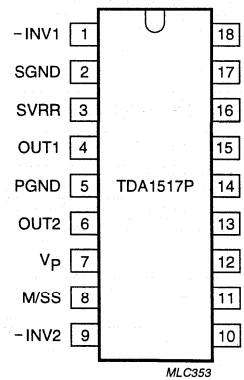


Fig.2 Pin configuration for SOT110-1.



Pins 10 to 18 connected to GND or floating.

Fig.3 Pin configuration for SOT398-1.

FUNCTIONAL DESCRIPTION

The TDA1517 contains two identical amplifiers with differential input stages. The gain of each amplifier is fixed at 20 dB. A special feature of the device is the mute/standby switch which has the following features:

- Low standby current (<100 μA)
- Low mute/standby switching current (low cost supply switch)
- Mute condition.

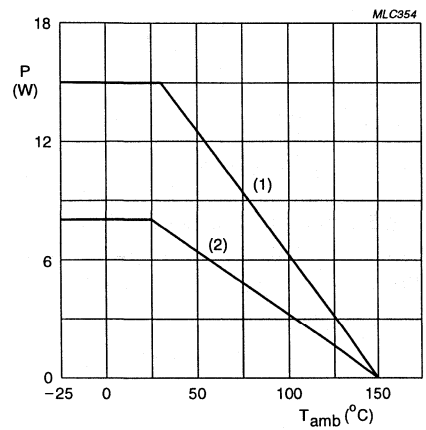
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage				
	operating		–	18	V
	non-operating		–	30	V
	load dump protection	during 50 ms; $t_r \geq 2.5$ ms	–	45	V
$V_{P(sc)}$	AC and DC short-circuit safe voltage		–	18	V
$V_{P(r)}$	reverse polarity		–	6	V
ERG_O	energy handling capability at outputs	$V_P = 0$ V	–	200	mJ
I_{OSM}	non-repetitive peak output current		–	4	A
I_{ORM}	repetitive peak output current		–	2.5	A
P_{tot}	total power dissipation	see Fig.4	–	15	W
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–40	+85	°C
T_c	crystal temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	TYPE NUMBER	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}c}$	TDA1517	thermal resistance from junction to case	8	K/W
$R_{th\ j\text{-}p}$	TDA1517P	thermal resistance from junction to pins	15	K/W
$R_{th\ j\text{-}a}$	TDA1517; TDA1517P	thermal resistance from junction to ambient	50	K/W



(1) $R_{th\ j\text{-}c}$ = 8 K/W.
(2) $R_{th\ j\text{-}p}$ = 15 K/W.

Fig.4 Power derating curve.

DC CHARACTERISTICS

V_P = 14.4 V; T_{amb} = 25 °C; measured in Fig.6; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage	note 1	6.0	14.4	18.0	V
$I_{q(tot)}$	total quiescent current		–	40	80	mA
V_O	DC output voltage	note 2	–	6.95	–	V
Mute/standby switch						
V_8	switch-on voltage level	see Fig.5	8.5	–	–	V
Mute condition						
V_O	output signal in mute position	$V_{I(max)}$ = 1 V; f_i = 20 Hz to 15 kHz	–	–	2	mV
Standby condition						
I_{sb}	DC current in standby condition		–	–	100	μA
V_{sw}	switch-on current		–	12	40	μA

Notes

1. The circuit is DC adjusted at V_P = 6 to 18 V and AC operating at V_P = 8.5 to 18 V.
2. At 18 V < V_P < 30 V the DC output voltage ≤ ½V_P.

AC CHARACTERISTICS

V_P = 14.4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; measured in Fig.6; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_o	output power	THD = 0.5%; note 1	4	5	–	W
		THD = 10%; note 1	5.5	6.0	–	W
THD	total harmonic distortion	P_o = 1 W	–	0.1	–	%
f_{lr}	low frequency roll-off	at –3 dB; note 2	–	45	–	Hz
f_{hr}	high frequency roll-off	at –1 dB	20	–	–	kHz
G_v	closed loop voltage gain		19	20	21	dB
SVRR	supply voltage ripple rejection	note 3				
	on		48	–	–	dB
	mute		48	–	–	dB
	standby		80	–	–	dB
$\|Z_i\|$	input impedance		50	60	75	kΩ
V_{no}	noise output voltage					
	on	R_s = 0 Ω; note 4	–	50	–	μV
	on	R_s = 10 Ω; note 4	–	70	100	μV
	mute	note 5	–	50	–	μV
α_{cs}	channel separation	R_s = 10 Ω	40	–	–	dB
$\|\Delta G_v\|$	channel unbalance		–	0.1	1	dB

Notes

1. Output power is measured directly at the output pins of the IC.
2. Frequency response externally fixed.
3. Ripple rejection measured at the output with a source impedance of 0 Ω, maximum ripple amplitude of 2 V (p-p) and a frequency between 100 Hz and 10 kHz.
4. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
5. Noise output voltage independent of R_s (V_I = 0 V).

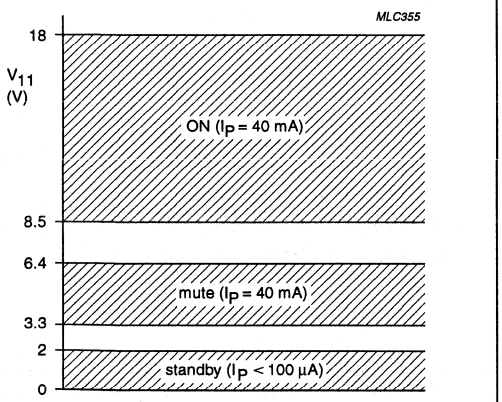


Fig.5 Standby, mute and on conditions.

APPLICATION INFORMATION

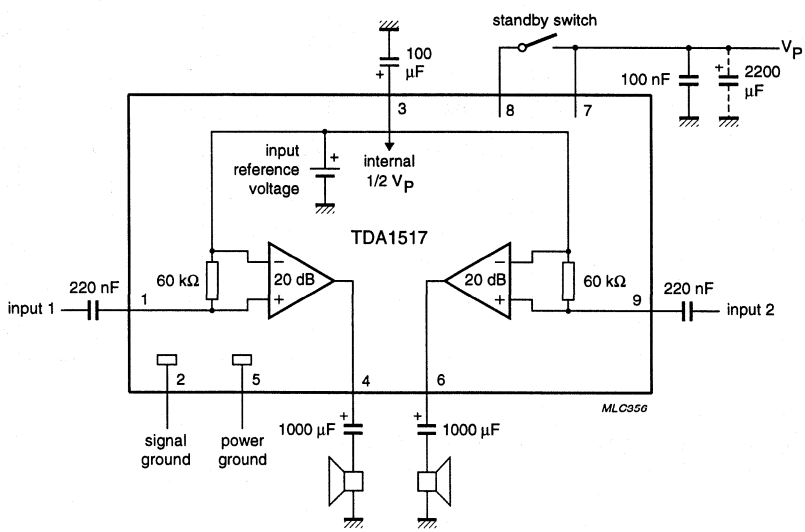


Fig.6 Application circuit diagram.

2 x 6 W stereo car radio power amplifier TDA1519

GENERAL DESCRIPTION

The TDA1519 is an integrated class-B dual output amplifier in a 9-lead single in-line (SIL) plastic medium power package. The device is primarily developed for car radio applications.

Features

- Requires very few external components
- High output power
- Fixed gain
- Good ripple rejection
- Mute/stand-by switch
- Load dump protection
- AC and DC short-circuit-safe to ground and V_P
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs (V_P = 0 V)
- No switch-on/switch-off plop
- Protected against electrostatic discharge
- Compatible with TDA1517 (except gain).

QUICK REFERENCE DATA

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage range						
operating		V_P	6,0	14,4	18,0	V
non-operating		V_P	–	–	30	V
load dump protected		V_P	–	–	45	V
Repetitive peak output current		I_{ORM}	–	–	2,5	A
Total quiescent current		I_{tot}	–	40	80	mA
Stand-by current		I_{sb}	–	0,1	100	μA
Switch-on current		I_{sw}	–	–	40	μA
Input impedance		$\|Z_I\|$	50	–	–	kΩ
Output power	THD = 0,5%; 4 Ω	P_o	–	5	–	W
	THD = 10%; 4 Ω	P_o	–	6	–	W
Channel separation		α	40	–	–	dB
Noise output voltage		$V_{no(rms)}$	–	150	–	μV
Supply voltage ripple rejection	f = 100 Hz	SVRR	40	–	–	dB
	f = 1 kHz to 10 kHz	SVRR	48	–	–	dB
Crystal temperature		T_c	–	–	150	°C

PACKAGE OUTLINE

9-lead SIL-bent-to-DIL; plastic (SOT110B); SOT110-1; 1996 July 19.

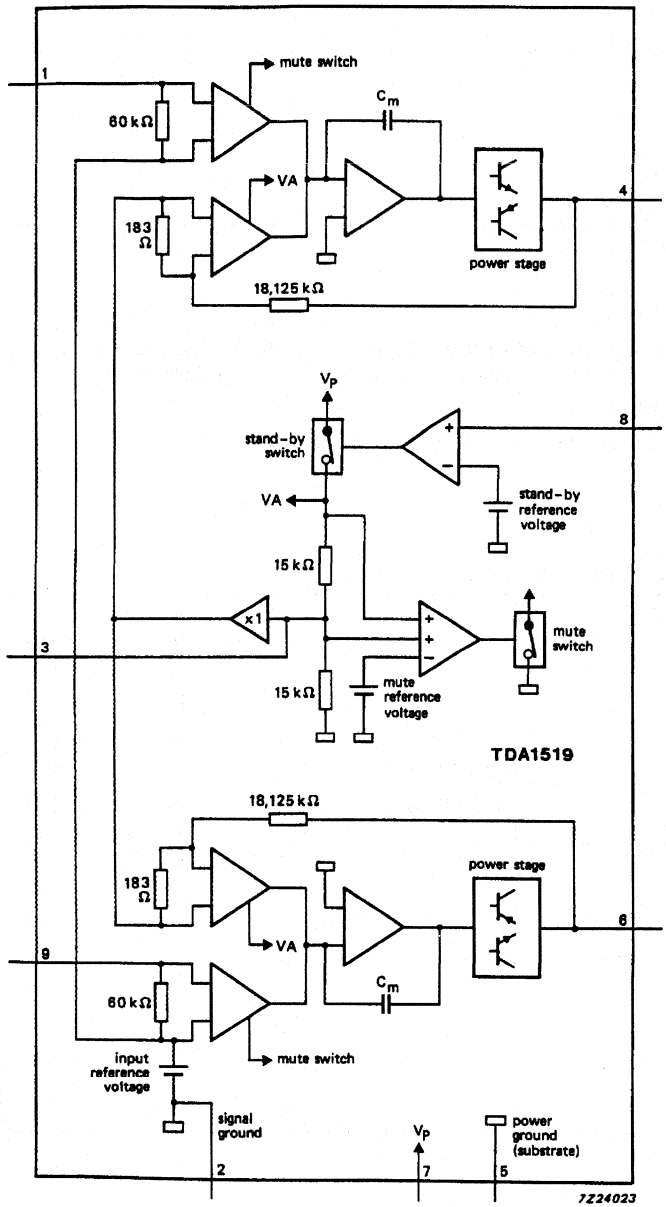


Fig.1 Block diagram.

PINNING

1	INV1	non-inverting input 1
2	GND1	ground (signal)
3	SVRR	supply voltage ripple rejection
4	OUT1	output 1
5	GND2	ground (substrate)
6	OUT2	output 2
7	V_P	supply voltage
8	M/SS	mute/stand-by switch
9	–INV2	non-inverting input 2

FUNCTIONAL DESCRIPTION

The TDA1519 contains two identical amplifiers with differential input stages. The gain of each amplifier is fixed at 40 dB. A special feature of this device is the mute/stand-by switch which has the following features:

- low stand-by current (< 100 μA)
- low mute/stand-by switching current (low cost supply switch)
- mute condition.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
Supply voltage					
operating		V_P	–	18	V
non-operating		V_P	–	30	V
load dump protected	during 50 ms;				
	$t_r \geq 2{,}5$ ms	V_P	–	45	V
AC and DC short-circuit-safe voltage		V_{PSC}	–	18	V
Reverse polarity		V_{PR}	–	6	V
Energy handling capability at outputs	$V_P = 0$ V		–	200	mJ
Non-repetitive peak output current		I_{OSM}	–	4	A
Repetitive peak output current		I_{ORM}	–	2,5	A
Total power dissipation	see Fig.2	P_{tot}	–	15	W
Crystal temperature		T_c	–	150	°C
Storage temperature range		T_{stg}	–55	+ 150	°C

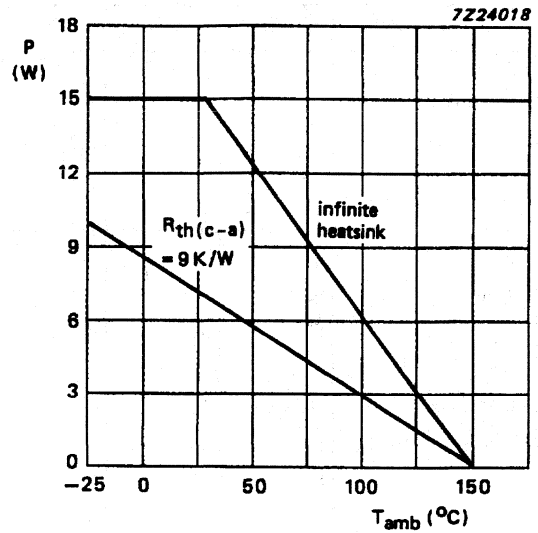


Fig.2 Power derating curve.

DC CHARACTERISTICS (note 1)

V_P = 14,4 V; T_{amb} = 25 °C; unless otherwise specified

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply						
Supply voltage range	note 2	V_P	6,0	14,4	18,0	V
Quiescent current		I_P	–	40	80	mA
DC output voltage	note 3	V_O	–	6,95	–	V
Mute/stand-by switch						
Switch-on voltage level	see Fig.3	V_{ON}	8,5	–	–	V
Mute condition		V_{mute}	3,3	–	6,4	V
Output signal in mute position	V_I = 1 V (max.); f = 20 Hz to 15 kHz	V_O	–	–	20	mV
Stand-by condition		V_{sb}	0	–	2	V
DC current in stand-by condition		I_{sb}	–	–	100	µA
Switch-on current		I_{sw}	–	12	40	µA

AC CHARACTERISTICS (note 1)

V_P = 14,4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Output power	note 4;					
	THD = 0,5%	P_o	4	5	–	W
	THD = 10%	P_o	5,5	6,0	–	W
Total harmonic distortion	P_o = 1 W	THD	–	0,1	–	%
Low frequency roll-off	note 5;					
	–3 dB	f_L	–	45	–	Hz
High frequency roll-off	–1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	39	40	41	dB
Supply voltage ripple rejection	note 6					
ON	f = 100 Hz	SVRR	40	–	–	dB
ON	f = 10 Hz to 10 kHz	SVRR	48	–	–	dB
mute		SVRR	48	–	–	dB
stand-by		SVRR	80	–	–	dB
Input impedance		$\|Z_i\|$	50	60	75	kΩ
Noise output voltage	note 7;					
ON	R_S = 0 Ω	$V_{no(rms)}$	–	150	–	μV
ON	R_S = 10 kΩ	$V_{no(rms)}$	–	250	500	μV
mute	note 8	$V_{no(rms)}$	–	120	–	μV
Channel separation	R_S = 10 kΩ	α	40	–	–	dB
Channel balance		$\|\Delta G_v\|$	–	0,1	1	dB

Notes to the characteristics

1. All characteristics are measured using the circuit shown in Fig.4.
2. The circuit is DC adjusted at V_P = 6 V to 18 V and AC operating at V_P = 8,5 V to 18 V.
3. At 18 V < V_P < 30 V the DC output voltage ≤ V_P/2.
4. Output power is measured directly at the output pins of the IC.
5. Frequency response externally fixed.
6. Ripple rejection measured at the output with a source impedance of 0 Ω (maximum ripple amplitude of 2 V) and a frequency between 100 Hz and 10 kHz.
7. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
8. Noise output voltage independent of R_S (V_I = 0 V).

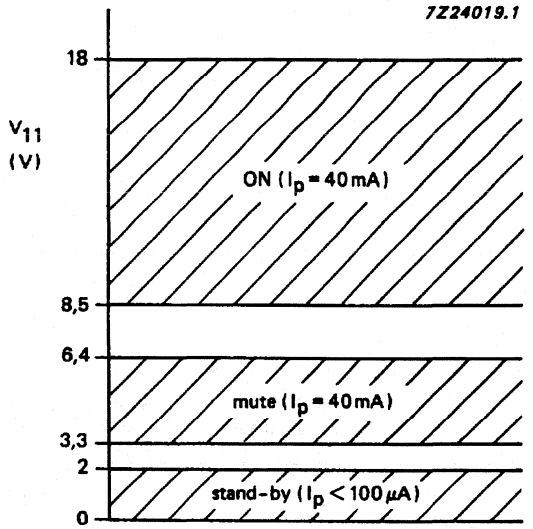


Fig.3 Stand-by, mute and ON conditions.

APPLICATION INFORMATION

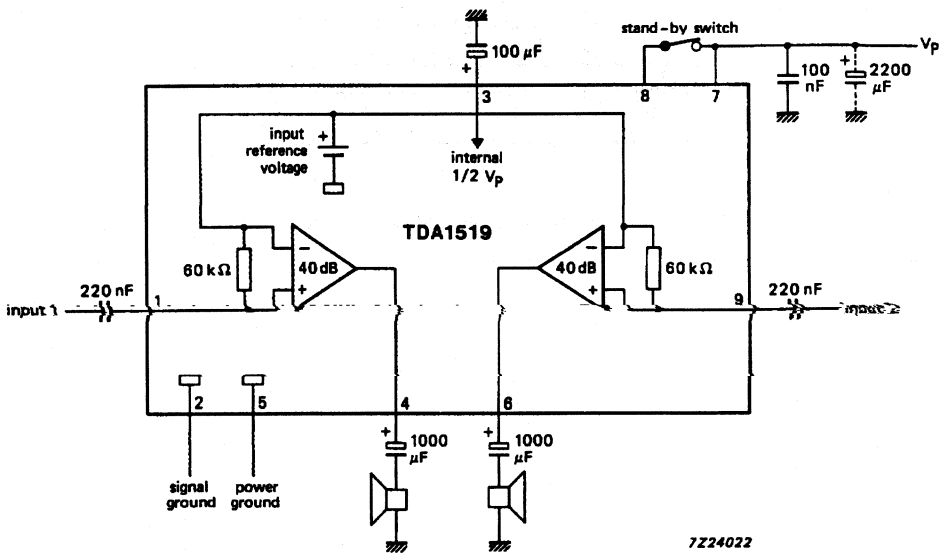


Fig.4 Application circuit diagram.

Bitstream continuous calibration filter-DAC with headphone driver and DSP

TDA1548T

FEATURESPRODUCT SPECIFICATION

Easy application

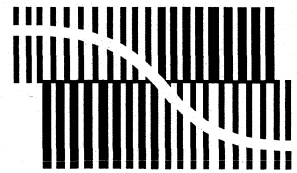
- Only first-order analog post-filtering required
- Headphone amplifiers and digital filter integrated
- Component saving common headphone output
- Selectable system clock (SYSCLK) $64f_s$, $256f_s$ or $384f_s$
- 16, 18 or 20 bits I^2S-bus or LSB justified serial input format
- Input pins suitable with 5 V low supply voltage interfacing
- Small package (SSOP28)
- Single rail supply (3 V).

High performance

- Superior signal-to-noise ratio
- Wide dynamic range
- Continuous calibration digital-to-analog conversion combined with noise shaping technique.

Features

- Low power dissipation
- Digital volume control
- Soft mute
- Digital tone control (Bass Boost and Treble)
- Digital de-emphasis
- Analog control of digital sound control functions.



BITSTREAM CONVERSION

GENERAL DESCRIPTION

The TDA1548T is a dual CMOS digital-to-analog converter (DAC) with up-sampling filter and noise shaper and integrated headphone driver featuring unique signal processing functions. The digital processing features are of high sound processing quality due to the wide dynamic range of the bitstream conversion technique.

The TDA1548T supports the I^2S-bus data input mode with word lengths of up to 20 bits and the LSB justified serial data input format with word lengths of 16, 18 or 20 bits. The clock system is selectable ($64f_s$, $256f_s$ or $384f_s$) by means of selection pins. Two cascaded half band filters, linear interpolator and a sample-and-hold function increase the oversampling rate from $1f_s$ to $64f_s$.
A second-order noise shaper converts this oversampled data into a bitstream for the 5-bit continuous calibration DACs.

On board amplifiers convert the output current to a voltage signal capable of driving a headphone or line output. The common operational amplifier application eliminates the need for capacitors.

The TDA1548T has some sound processing functions which are controllable by a potentiometer. These functions are volume, bass boost and treble. The flat/min/max switch can also be controlled by a potentiometer.
The analog values are converted to a digital code, which is then further translated internally to a set of coefficients for either volume, bass boost or treble.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1548T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
TDA1548TZ	SSOP28	plastic shrink small outline package; 28 leads; body width 5.3 mm	SOT341-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	note 1	2.7	3.0	4.0	V
I_{DD}	supply current	note 2	–	15	–	mA
$V_{oFS(rms)}$	full-scale output voltage	V_{DD} = 3 V	0.57	0.64	0.71	V
(THD+N)/S	total harmonic distortion plus noise as a function of signal	0 dB signal	–	–65	–60	dB
			–	0.056	0.1	%
		0 dB signal; R_{OL} = 5 kΩ	–	–85	–78	dB
			–	0.006	0.013	%
		–60 dB signal; R_{OL} = 32 Ω or R_{OL} = 5 kΩ	–	–35	–30	dBA
			–	1.778	3.162	%
S/N	signal-to-noise ratio	A-weighted; at code 00000H	90	95	–	dBA
BR	input bit rate at data input	$f_{sys} = 384f_s$	–	$48f_s$	–	
		$f_{sys} = 256f_s$	–	$64f_s$	–	
		$f_{sys} = 64f_s$	–	$64f_s$	–	
f_{sys}	system clock frequency		2.048	–	18.432	MHz
TC_{FS}	full-scale temperature coefficient at analog outputs (VOL and VOR)		–	$\pm 100 \times 10^{-6}$	–	
T_{amb}	operating ambient temperature		–20	–	+70	°C

Notes

1. All V_{DD} and V_{SS} pins must be connected to the same supply or ground respectively.
2. Measured at input code 00000H and V_{DD} = 3 V.

BLOCK DIAGRAM

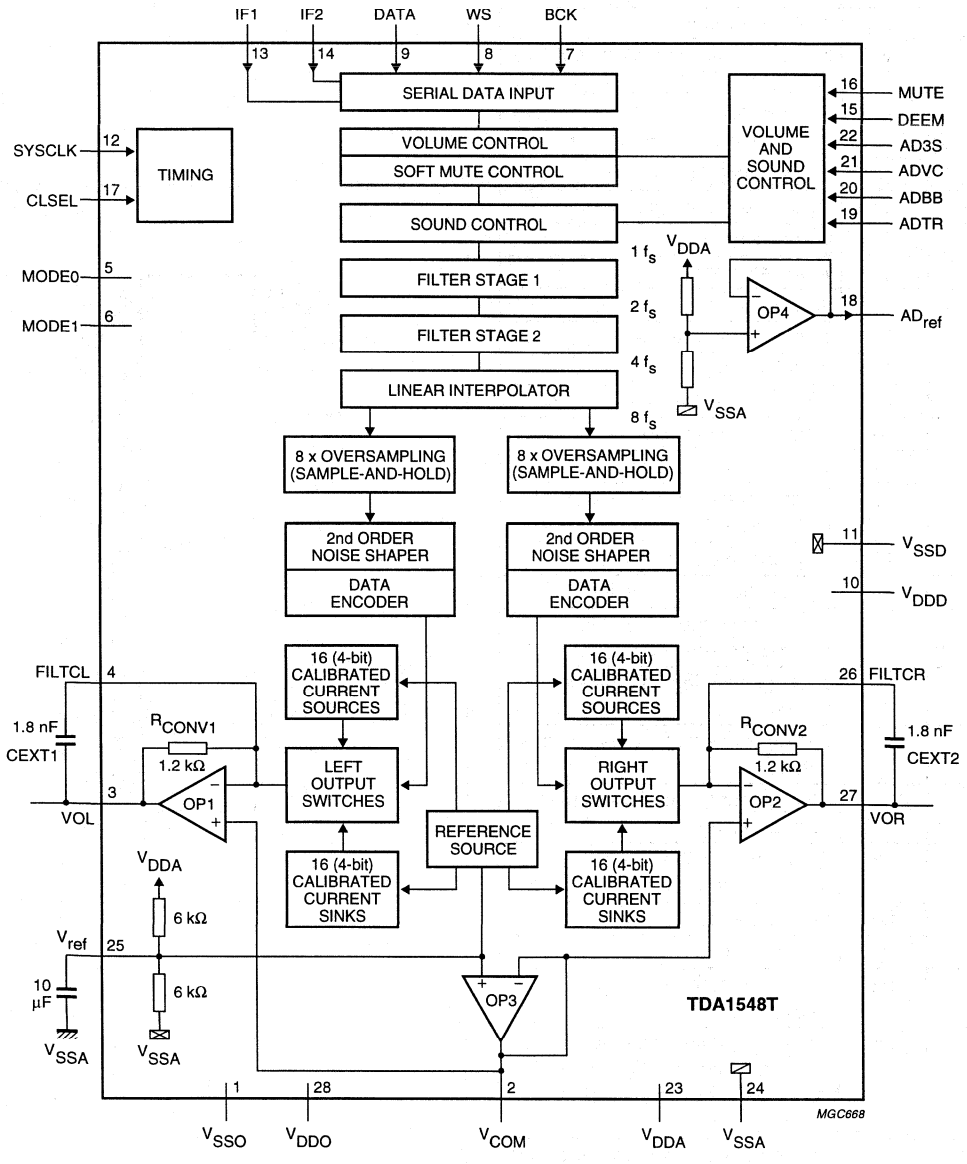


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{SSO}	1	operational amplifier ground
V_{COM}	2	common output pin
VOL	3	left channel audio voltage output
FILTCL	4	capacitor for left channel first-order filter function should be connected between this pin and VOL (pin 3)
MODE0	5	mode 0 selection pin
MODE1	6	mode 1 selection pin
BCK	7	bit clock input
WS	8	word select input
DATA	9	data input
V_{DDD}	10	digital supply voltage
V_{SSD}	11	digital ground
SYSCLK	12	system clock $64f_s$, $256f_s$ or $384f_s$
IF1	13	input format selection 1
IF2	14	input format selection 2
DEEM	15	de-emphasis input (f_s = 44.1 kHz) (active HIGH)
MUTE	16	soft-mute input (active HIGH)
CLSEL	17	system clock selection input
AD_{ref}	18	reference voltage output to external potentiometer
ADTR	19	analog sense input for treble setting
ADBB	20	analog sense input for bass boost setting
ADVC	21	analog sense input for volume control setting
AD3S	22	3-position switch input for flat/min/max setting
V_{DDA}	23	analog supply voltage
V_{SSA}	24	analog ground
V_{ref}	25	internal reference voltage ($0.5V_{DDA}$ typ)
FILTCR	26	capacitor for right channel first-order filter function should be connected between this pin and VOR (pin 27)
VOR	27	right channel audio voltage output
V_{DDO}	28	operational amplifier supply voltage

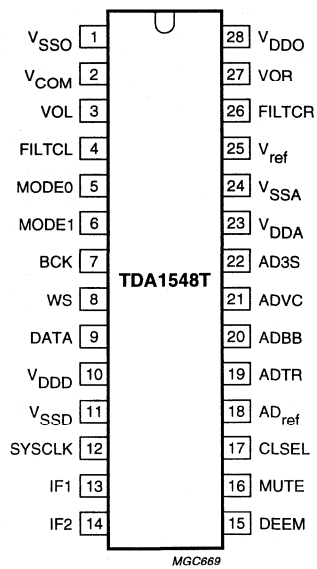


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA1548T CMOS DAC incorporates an up-sampling digital filter, a linear interpolator, a noise shaper, continuous calibrated current sources and headphone amplifiers. The $1f_s$ input data is increased to an oversampling rate of $64f_s$. This high-rate oversampling, together with the 5-bit DAC, enables the filtering required for waveform smoothing and out-of-band noise reduction to be achieved by simple first-order analog post-filtering.

System clock and data input format

The TDA1548T accommodates slave mode only, this means that in all applications the system devices must provide the system clock. The system frequency is selectable at pins CLSEL, MODE0 and MODE1 (see Table 1).

The TDA1548T supports the following data input modes (see Table 2):

I^2S-bus with data word length of up to 20 bits

LSB justified serial format with data word length of 16, 18 or 20 bits.

The input formats are illustrated in Fig.4. Left and right data-channel words are time multiplexed.

Analog control of digital sound processing features

Digital sound processing settings are controlled via analog sense inputs that translate an analog voltage from, for example, a potentiometer wiper to a digital code, which is then further translated internally to a set of coefficients for either treble, bass boost or volume.

The analog input value is acquired by an internal 6-bit ADC, sampling the three input pins ADVC, ADBB and ADTR and the three-mode selection pin ADS3 (see Section "Single pin three mode selection") in a multiplexed fashion. Sampling of the input voltage is performed by a straight forward technique of linear approximation; from the starting value of 0 V, an internal linear approximation voltage is incremented periodically in steps of 1/66th of the scale, with an internal comparator detecting when the approximation value oversteps the input value. Tolerance is built in at the top and bottom end of the scale by dimensioning the resistive elements at the top and bottom of the ladder equals 1R. Thus the ladder is built up of 64 elements of value R, two of value R, making a typical quantization step size of approximately 1.5 V (AD_{ref}) divided-by-66 (amount of Rs), equals 22.7 mV.

For each multiplexed timeslot the full approximation cycle is completed, immediately after which the next input will start being sampled.

The time slot for one input lasts 64 steps at a step advance rate of $8 \times f_s$, which amounts to 181 µs at f_s = 44.1 kHz. Because four inputs are multiplexed, the sample rate for each analog input is 1.38 kHz.

A buffered version of an internally generated reference voltage is available at output pin AD_{ref}. Because the internal AD derives from the same reference voltage, this allows for optimum mapping of the external analog control value onto the useful AD input voltage range. The idea is to bias a potentiometer to AD_{ref}, using a wiper to control the input voltage between 0 V and AD_{ref}. Hysteresis is implemented to improve noise immunity of the AD in order to prevent a stable setting of the potentiometer, to a point near a quantization threshold, from producing two alternating digital codes which could give rise to audible volume or boost changes. An hysteresis of 1 LSB is implemented digital. A shift in code must be at least 2 LSB either up or down from the current value, otherwise the internal digital code will remain at the current value.

SINGLE PIN THREE MODE SELECTION

A special input pin AD3S (pin 22), controls the mode in which the sound processing block operates. Not between two but three modes; whether the DSP should follow the AD inputs applying maximum effect, the minimum effect or overrule the boost effects thereby resulting in a flat frequency characteristic in the treble and bass boost sections.

Internally the same AD is used to detect the input level present at this pin as is used for the three sound control pins. An internal bias circuit containing of two MOSTs supplies a mid-range voltage so that this input can be operated with a minimum of external components. A HIGH or LOW input level is created by tying the pin to AD_{ref} or ground respectively, the intermediate value is achieved by leaving the pin open-circuit.

Volume control

Since there is no headroom included into the sound control section, the volume control precedes the sound control. Full volume and neutral setting (flat) of the sound control results in a full-scale output. Any tone boost will immediately cause clipping, which can be avoided by reducing the volume setting.

Soft mute

Soft mute is controlled by MUTE (pin 16). When the input is active HIGH the value of the sample is decreased smoothly to zero following a raised cosine curve. 32 coefficients are used to step down the value of the data, each one being used 32 times before stepping on to the next. This amounts to a mute transition time of 23 ms at f_s = 44.1 kHz. When MUTE is released (LOW), the samples are returned to the full level again following a raised cosine curve with the same coefficients being used in the reverse order. Mute is synchronized to the sample clock, so that the operation always takes place on complete samples.

Digital sound processing features

BASS BOOST

A strong bass boost effect, which is useful in compensating for poor bass response of portable headphone sets, is implemented digitally in the TDA1548T and can be controlled by ADBB (pin 20) and AD3S (pin 22). Table 3 shows the bass boost values at different input voltages. Table 4 shows the selection mode status (flat/min/max) at different input voltages. Valid settings range from "flat" (no influence on audio) to +18 dB with step sizes of 2 dB in "minimum" and to +24 dB with step sizes of 2 dB in "maximum". The programmable bass boost filter is a second-order shelving type with a fixed corner frequency of 130 Hz for the "minimum" setting and a fixed corner frequency of 230 Hz for the "maximum" setting and has a Butterworth characteristic. Because of the exceptional amount of programmable gain, bass boost should be used in conjunction with adequate prior attenuation, using the volume control.

TREBLE

A treble effect is implemented digitally in the TDA1548T and can be controlled by ADTR (pin 19) and AD3S (pin 22). Table 3 shows the treble values at different input voltages. Table 4 shows the selection mode status (flat/min/max) at different input voltages. Valid settings range from "flat" (no influence on audio) to +6 dB with step sizes of 2 dB in "minimum" and to +6 dB with a step size of 2 dB in "maximum". The programmable treble filter is a first-order shelving type with a fixed corner frequency of 2.8 kHz for the "minimum" setting and a fixed corner frequency of 5.0 kHz for the "maximum" setting.

DE-EMPHASIS

De-emphasis is controlled by DEEM (pin 15). The digital de-emphasis filter is dimensioned to produce the de-emphasis frequency characteristics for the sample rate 44.1 kHz. With its 18-bit dynamic range, the digital de-emphasis of the TDA1548T is a convenient and component-saving alternative to analog de-emphasis.

When the DEEM pin is active HIGH, de-emphasis is enabled. De-emphasis is synchronized to the sample clock, so that operation always takes place on complete samples.

Oversampling filter and noise shaper

The digital filter is a four times oversampling filter. It consists of two sections which each increase the sample rate by 2.

The second order noise shaper operates at 64f_s. It shifts in-band quantization noise to frequencies well above the audio band. This noise shaping technique, used in combination with a sign-magnitude coding, enables high signal-to-noise ratios to be achieved. The noise shaper outputs a 5-bit PDM bitstream signal to the DAC.

Continuous calibration DAC

The dual 5-bit DAC uses the continuous calibration technique. This method, based on charge storage, involves exact duplication of a single reference current source. In the TDA1548T, 32 such current sources plus 1 spare source are continuously calibrated. The spare source is included to allow continuous converter operation.

The DAC receives a 5-bit data bitstream from the noise shaper. This data is converted to a sign-magnitude code so that no current is switched to the output during digital silence (input 00000H). In this way very high signal-to-noise performance is achieved.

Component-saving stereo headphone driver

High precision, low-noise amplifiers together with the internal conversion resistors R_{CONV1} and R_{CONV2} convert the converter output current to a voltage capable of driving a line output or headphone. The voltage is available at VOL and VOR (0.64 V RMS typical).

A major component saving feature of the TDA1548T is that no DC-blocking capacitors are needed in the application, despite the asymmetrical supply. The V_{COM} output, pin 2, is biased to the same voltage that the right and left channel voltage outputs are, V_{ref}, and is capable of sinking the sum of left and right channel load currents. Therefore, connecting a load between one of the outputs and V_{COM} only gives rise to a negligible amount of DC current through the load.

Table 1 System clock selection

PINS			DESCRIPTION
CLSEL	MODE0	MODE1	
0	0	0	$256f_s$
0	0	1	$64f_s$
0	1	X	reserved 1
1	0	0	$384f_s$
1	0	1	reserved 2
1	1	X	reserved 3

Table 2 Data input formats

PINS		FORMAT
IF1	IF2	
0	0	I^2S-bus
0	1	LSB justified, 16 bits
1	0	LSB justified, 18 bits
1	1	LSB justified, 20 bits

Table 3 Relationship between VC, BB and TR

ANALOG INPUT VALUES (V); PINS ADTR, ADBB AND ADVC	VOLUME (ADVC)	BASS BOOST (ADBB)		TREBLE (ADTR)	
		MAX.	MIN.	MAX.	MIN.
$AD_{ref} \times 65/66$	–0	0	0	0	0
$AD_{ref} \times 64/66$	–0	0	0	0	0
$AD_{ref} \times 63/66$	–1	0	0	0	0
$AD_{ref} \times 62/66$	–2	0	0	0	2
$AD_{ref} \times 61/66$	–3	2	2	2	2
$AD_{ref} \times 60/66$	–4	2	2	2	2
$AD_{ref} \times 59/66$	–5	4	4	2	2
$AD_{ref} \times 58/66$	–6	4	4	2	2
$AD_{ref} \times 57/66$	–7	6	6	4	4
$AD_{ref} \times 56/66$	–8	6	6	4	4
$AD_{ref} \times 55/66$	–9	8	8	4	4
$AD_{ref} \times 54/66$	–10	8	8	4	4
$AD_{ref} \times 53/66$	–11	10	10	6	6
$AD_{ref} \times 52/66$	–12	10	10	6	6
$AD_{ref} \times 51/66$	–13	12	12	6	6
$AD_{ref} \times 50/66$	–14	12	12	6	6
$AD_{ref} \times 49/66$	–15	14	14	....	....
$AD_{ref} \times 48/66$	–16	14	14	....	....
$AD_{ref} \times 47/66$	–17	16	16	....	....
$AD_{ref} \times 46/66$	–18	16	16	....	....
$AD_{ref} \times 45/66$	–19	18	18	....	....
$AD_{ref} \times 44/66$	–20	18	18	....	....
$AD_{ref} \times /4366$	–21	20	18	....	....
$AD_{ref} \times 42/66$	–22	20	18	....	....
$AD_{ref} \times 41/66$	–23	22	....	....	....
$AD_{ref} \times 40/66$	–24	22	....	....	....
$AD_{ref} \times 39/66$	–25	24	....	....	....

ANALOG INPUT VALUES (V); PINS ADTR, ADBB AND ADVC	VOLUME (ADVC)	BASS BOOST (ADBB)		TREBLE (ADTR)	
		MAX.	MIN.	MAX.	MIN.
$AD_{ref} \times 38/66$	−26	24	....	....	....
$AD_{ref} \times 37/66$	−27	....	....	....	....
$AD_{ref} \times 36/66$	−28	....	....	....	....
....	....	....	....	....	....
....	....	....	....	....	....
$AD_{ref} \times 5/66$	−59	24	18	6	6
$AD_{ref} \times 4/66$	−60	24	18	6	6
$AD_{ref} \times 3/66$	$-\infty$	24	18	6	6
$AD_{ref} \times 2/66$	$-\infty$	24	18	6	6

Table 4 Relationship mode selection

ANALOG INPUT VALUE (V); PIN AD3S	FLAT, MINIMUM OR MAXIMUM
$AD_{ref} \times 65/66$	flat
$AD_{ref} \times 64/66$	flat
....	....
....	....
$AD_{ref} \times 51/66$	flat
$AD_{ref} \times 50/66$	flat
$AD_{ref} \times 49/66$	minimum
$AD_{ref} \times 48/66$	minimum
....	....
....	....
$AD_{ref} \times 19/66$	minimum
$AD_{ref} \times 18/66$	minimum
$AD_{ref} \times 17/66$	maximum
$AD_{ref} \times 16/66$	maximum
....	....
....	....
$AD_{ref} \times 3/66$	maximum
$AD_{ref} \times 2/66$	maximum

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage	note 1	–	4.5	V
T_{xtal}	maximum crystal temperature		–	+150	°C
T_{stg}	storage temperature		−65	+125	°C
T_{amb}	operating ambient temperature		−20	+70	°C
V_{es}	electrostatic handling	note 2	−3000	+3000	V
		note 3	−300	+300	V

Notes

1. All V_{DD} and V_{SS} connections must be made to the same power supply.
2. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor. Pin 18 = −1500 V (min) and +1500 V (max).
3. Equivalent to discharging a 200 pF capacitor via a 2.5 μH series inductor.

THERMAL CHARACTERISTICS

SYMBOL	DESCRIPTION	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	SO28	60	K/W
	SSOP28	80	K/W

QUALITY SPECIFICATION

In accordance with UZW-BO/FQ-0601. The numbers of the quality specification can be found in the *"Quality Reference Handbook"*. The Handbook can be ordered using the code 9397 750 00192.

DC CHARACTERISTICS

All voltages referenced to ground (pins 1, 11 and 24); $V_{DDD} = V_{DDA} = V_{DDO} = 3$ V; $T_{amb} = 25$ °C, $R_L = 32\ \Omega$ (note 1); common operational amplifier application; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage pin 10	note 2	2.7	3.0	4.0	V
V_{DDA}	analog supply voltage pin 23	note 2	2.7	3.0	4.0	V
V_{DDO}	opamp supply voltage pin 28	note 2	2.7	3.0	4.0	V
I_{DDD}	digital supply current	at digital silence	–	4.5	–	mA
I_{DDA}	analog supply current	at digital silence	–	4.5	–	mA
I_{DDO}	opamp supply current	at digital silence; note 3	–	6.0	–	mA
P_{tot}	total power dissipation	note 3	–	50	–	mW
Digital inputs						
V_{IH}	HIGH level input voltage on pins 5 to 9 and 12 to 17		$0.7V_{DDD}$	–	–	V
V_{IL}	LOW level input voltage on pins 5 to 9 and 12 to 17		–	–	$0.3V_{DDD}$	V
$\lvert I_{LI} \rvert$	input leakage current on pins 7 to 9 and 12 to 17		–	–	10	µA
C_I	input capacitance on pins 5 to 9 and 12 to 17		–	–	10	pF
Analog inputs pins ADVC, ADBB, ADTR and AD3S						
RES	input resolution		–	–	6	bit
C_I	input capacitance		–	10	–	pF
R_I	input resistance	pins ADBB, ADTR and ADVC	1	–	–	MΩ
		pin AD3S	–	20	–	kΩ
Analog reference pin AD_{ref}						
V_{ADref}	reference voltage pin 18		$0.45V_{DDA}$	$0.5V_{DDA}$	$0.55V_{DDA}$	V
$R_{L(ADref)}$	reference output load pin 18		3.0	–	–	kΩ
Analog audio pins						
V_{ref}	reference voltage pin 25	with respect to V_{SSO}	$0.45V_{DDA}$	$0.5V_{DDA}$	$0.55V_{DDA}$	V
R_O	output resistance pin 25		–	3	–	kΩ
R_{CONV}	current-to-voltage conversion resistor		–	1.2	–	kΩ
$I_{O(max)}$	maximum output current	(THD + N)/S < 0.1%	–	35	–	mA
C_L	output load capacitance	note 4	–	–	50	pF

Notes

1. R_L is the AC impedance of the external circuitry connected to the audio outputs of the application circuit.
2. All power supply pins (V_{DD} and V_{SS}) must be connected to the same external power supply unit.
3. No operational amplifier load resistor.
4. Load capacitance greater than 50 pF, an inductor of 22 µH connected in parallel with a resistor of 270 Ω must be inserted between the load and the operational amplifier output.

AC CHARACTERISTICS (ANALOG)

All voltages referenced to ground (pins 2, 9 and 23); $V_{DDD} = V_{DDA} = V_{DDO} = 3$ V; $f_i = 1$ kHz; $T_{amb} = 25$ °C, $R_L = 32\ \Omega$ (note 1); common operational amplifier application; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RES	input resolution		–	–	18	bit
f_{sAD}	AD sample frequency		–	$f_s/32$	–	kHz
V_{ADref}	input voltage range		0	–	V_{ADref}	V
$V_{FS(rms)}$	output voltage swing (RMS value) (pins 3 and 27)		0.57	0.64	0.71	V
$V_{DC(os)}$	DC offset output voltage w.r.t. reference voltage level V_{ref}		–	20	–	mV
TC_{FS}	full scale temperature coefficient		–	$\pm 100 \times 10^{-6}$	–	
SVRR	supply voltage ripple rejection V_{DDA} and V_{DDO}	$C_{25} = 10\ \mu F$; $f_{ripple} = 1$ kHz; $V_{ripple} = 100$ mV (peak)	–	40	–	dB
UNBAL	unbalance between the 2 DAC voltage outputs (pins 3 and 27)	maximum volume	–	0.1	–	dB
α_{ct}	crosstalk between the 2 DAC voltage outputs (pins 3 and 27)	one output digital silence the other maximum volume	–	50	–	dB
		one output digital silence the other maximum volume $R_L = 5$ kΩ	–	90	–	dB
	crosstalk between the 2 DAC voltage outputs (pins 3 and 27) with R_L connected to ground	one output digital silence the other maximum volume	–	70	–	dB
		one output digital silence the other maximum volume $R_L = 5$ kΩ	–	100	–	dB
(THD+N)/S	total harmonic distortion plus noise as a function of signal	0 dB signal	–	–65	–60	dB
			–	0.056	0.1	%
		0 dB signal; $R_L = 5$ kΩ	–	–85	–78	dB
			–	0.006	0.013	%
		–60 dB signal; $R_L = 32\ \Omega$ or $R_L = 5$ kΩ	–	–35	–30	dBA
			–	1.778	3.162	%
S/N	signal-to-noise ratio at bipolar zero	A-weighted at code 00000H	90	95	–	dBA

Note

1. R_L is the AC impedance of the external circuitry connected to the audio outputs of the application circuit.

AC CHARACTERISTICS (DIGITAL)

All voltages referenced to ground (pins 2, 9 and 23); $V_{DDD} = V_{DDA} = V_{DDO} = 2.7$ to 4.0 V; $T_{amb} = +70$ °C, $R_L = 32\ \Omega$ (note 1); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
T_{cy}	clock cycle	$f_{sys} = 384f_s$	54.2	59.1	81.3	ns
		$f_{sys} = 256f_s$	81.3	88.6	122	ns
		$f_{sys} = 64f_s$	325.5	354.3	488.3	ns
$t_{CW(L)}$	f_{sys} LOW level pulse width		22	–	–	ns
$t_{CW(H)}$	f_{sys} HIGH level pulse width		22	–	–	ns
Serial input data timing (see Fig.3)						
BR	clock input = data input rate	$f_{sys} = 384f_s$	–	$48f_s$	–	
		$f_{sys} = 256f_s$	–	$64f_s$	–	
		$f_{sys} = 64f_s$	–	$64f_s$	–	
f_{sys}	system clock frequency		2.048	–	18.432	MHz
f_{WS}	word select input frequency		–	44.1	48.0	kHz
t_r	rise time		–	–	20	ns
t_f	fall time		–	–	20	ns
$t_{BCK(H)}$	bit clock HIGH time		55	–	–	ns
$t_{BCK(L)}$	bit clock LOW time		55	–	–	ns
$t_{s;DAT}$	data set-up time		20	–	–	ns
$t_{h;DAT}$	data hold time		10	–	–	ns
$t_{s;WS}$	word select set-up time		20	–	–	ns
$t_{h;WS}$	word select hold time		10	–	–	ns

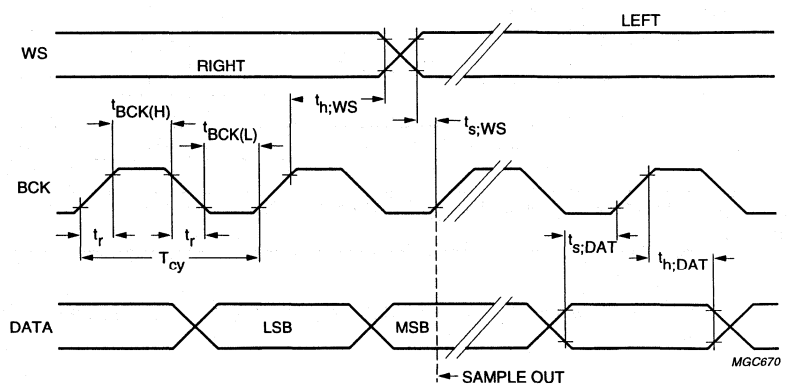


Fig.3 Timing of input signals.

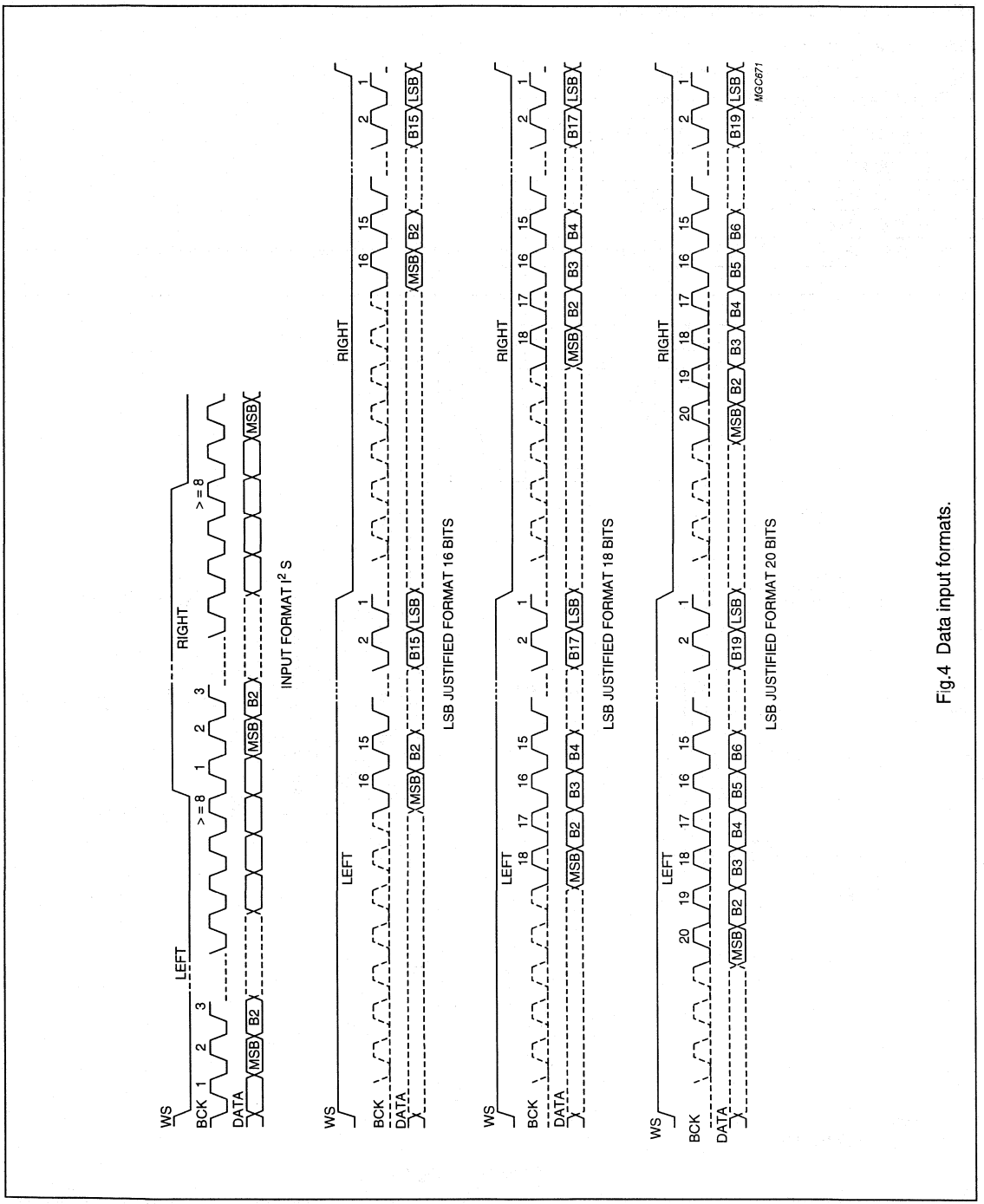


Fig.4 Data input formats.

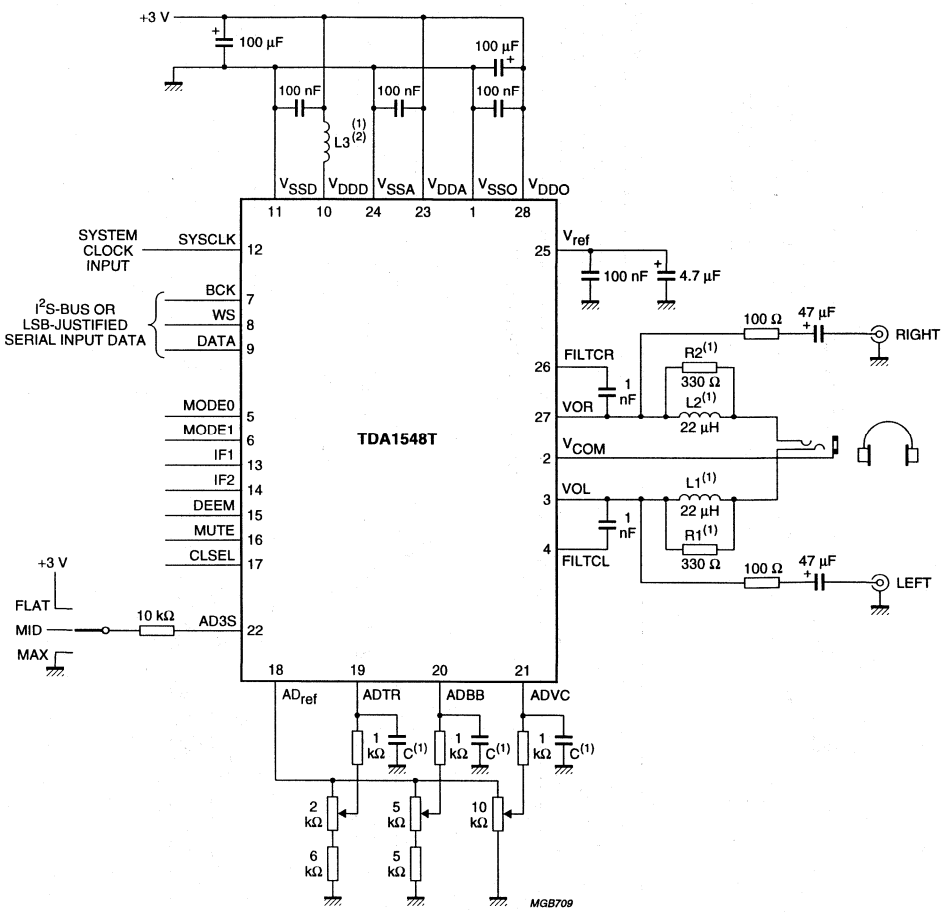
TEST AND APPLICATION INFORMATION

Filter characteristics

Table 5 Digital filter characteristics (f_s = 44.1 kHz)

The band frequencies scale with the sample frequency.

BAND	ATTENUATION
0 to 20 kHz	< 0.001 dB
24 to 64 kHz	> 39 dB
64 to 69 kHz	> 33 dB
69 to 88 kHz	> 37 dB



(1) Optional.

(2) Chip inductor BLM32A07.

Fig.5 Application diagram.

2 × 6 W hi-fi audio power amplifier TDA2615

FEATURES

- Requires very few external components
- No switch-on/switch-off clicks
- Input mute during switch-on and switch-off
- Low offset voltage between output and ground
- Excellent gain balance of both amplifiers
- Hi-fi in accordance with *"IEC 268"* and *"DIN 45500"*
- Short-circuit proof and thermal protected
- Mute possibility.

GENERAL DESCRIPTION

The TDA2615 is a dual power amplifier in a 9-lead plastic single-in-line (SIL9MPF) medium power package. It has been especially designed for mains fed applications, such as stereo radio and stereo TV.

QUICK REFERENCE DATA

Stereo application.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\pm V_P$	supply voltage range		7.5	–	21	V
P_O	output power	$V_S = \pm 12$ V; THD = 0.5%	–	6	–	W
G_v	internal voltage gain		–	30	–	dB
$\lvert G_v \rvert$	channel unbalance		–	0.2	–	dB
α	channel separation		–	70	–	dB
SVRR	supply voltage ripple rejection		–	60	–	dB
V_{no}	noise output voltage		–	70	–	μV

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA2615	SIL9MPF	plastic single in-line medium power package with fin; 9 leads	SOT110-1

BLOCK DIAGRAM

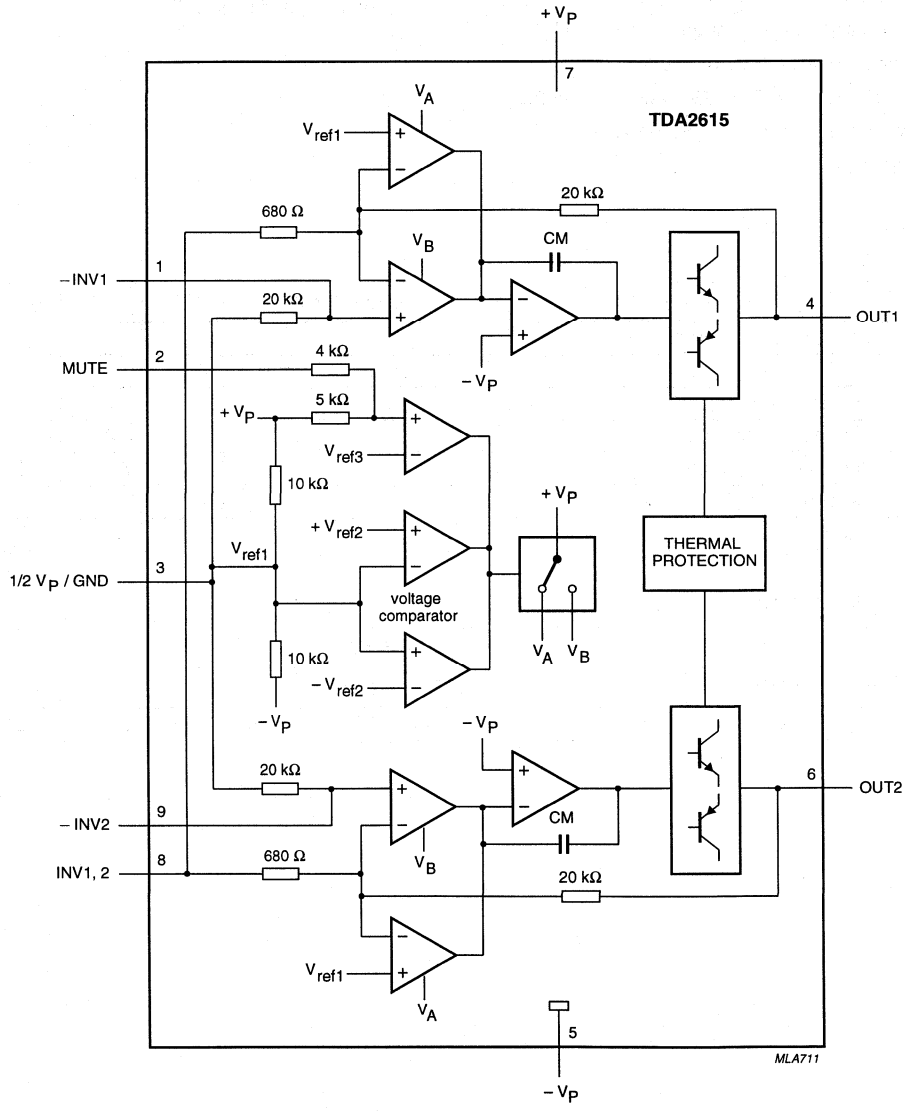


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
–INV1	1	non-inverting input 1
MUTE	2	mute input
$\frac{1}{2}V_P$/GND	3	$\frac{1}{2}$ supply voltage or ground
OUT1	4	output 1
$-V_P$	5	supply voltage (negative)
OUT2	6	output 2
$+V_P$	7	supply voltage (positive)
INV1, 2	8	inverting input 1 and 2
–INV2	9	non-inverting input 2

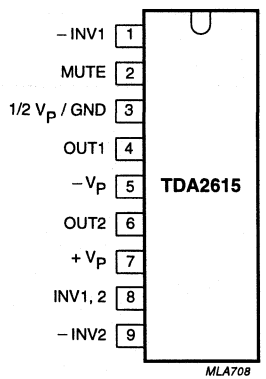


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA2615 is a hi-fi stereo amplifier designed for mains fed applications, such as stereo radio and stereo TV. The circuit is optimally designed for symmetrical power supplies, but is also well-suited to asymmetrical power supply systems.

An output power of 2 × 6 W (THD = 0.5%) can be delivered into an 8 Ω load with a symmetrical power supply of ±12 V. The gain is internally fixed at 30 dB, thus offering a low gain spread and a very good gain balance between the two amplifiers (0.2 dB).

A special feature is the input mute circuit. This circuit disconnects the non-inverting inputs when the supply voltage drops below ±6 V, while the amplifier still retains its DC operating adjustment. The circuit features suppression of unwanted signals at the inputs, during switch-on and switch-off.

The mute circuit can also be activated via pin 2. When a current of 300 μA is present at pin 2, the circuit is in the mute condition.

The device is provided with two thermal protection circuits. One circuit measures the average temperature of the crystal and the other measures the momentary temperature of the power transistors. These control circuits attack at temperatures in excess of +150 °C, so a crystal operating temperature of max. +150 °C can be used without extra distortion.

With the derating value of 6 K/W, the heatsink can be calculated as follows:

at R_L = 8 Ω and V_S = ±12 V, the measured maximum dissipation is 7.8 W.

With a maximum ambient temperature of +60 °C, the thermal resistance of the heatsink is:

$$R_{th} = \frac{150 - 60}{7.8} - 6 = 5.5 \text{ K/W}$$

The metal tab has the same potential as pin 5.

LIMITING VALUES

In accordance with the Absolute maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_P$	supply voltage		–	21	V
I_{OSM}	non-repetitive peak output current		–	4	A
P_{tot}	total power dissipation	see Fig.3	–	15	W
T_{stg}	storage temperature range		−55	+150	°C
T_{xtal}	crystal temperature		–	+150	°C
T_{amb}	ambient operating temperature range		−25	+150	°C
t_{sc}	short-circuit time	short-circuit to ground; note 1	–	1	h

Note

1. For asymmetrical power supplies (with the load short-circuited), the maximum unloaded supply voltage is limited to V_P = 28 V and with an internal supply resistance of $R_S \geq 4\ \Omega$, the maximum unloaded supply voltage is limited to 32 V **(with the load short-circuited)**. For symmetrical power supplies the circuit is short-circuit-proof up to V_P = 21 V.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}c}$	thermal resistance from junction to case	6	K/W

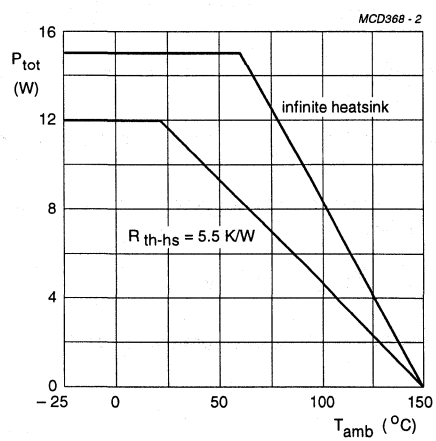


Fig.3 Power derating curve.

CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
$\pm V_P$	supply voltage range		–	12	21	V
I_{ORM}	repetitive peak output current		2.2	–	–	A
Operating position; note 1						
$\pm V_P$	supply voltage range		7.5	12	21	V
$I_{q(tot)}$	total quiescent current	$R_L = \infty$	18	40	70	mA
P_O	output power	THD = 0.5%	5	6	–	W
		THD = 10%	6.5	8	–	W
THD	total harmonic distortion	P_O = 4 W	–	0.15	0.2	%
B	power bandwidth	THD = 0.5%; note 2	–	20 to 20000	–	Hz
G_v	voltage gain		29	30	31	dB
$\lvert G_v \rvert$	gain unbalance		–	0.2	1	dB
V_{no}	noise output voltage	note 3	–	70	140	μV
$\lvert Z_i \rvert$	input impedance		14	20	26	kΩ
SVRR	supply voltage ripple rejection	note 4	40	60	–	dB
α_{cs}	channel separation	$R_S = 0$	46	70	–	dB
I_{bias}	input bias current		–	0.3	–	μA
$\lvert \Delta V_{GND} \rvert$	DC output offset voltage		–	30	200	mV
$\lvert \Delta V_{4-6} \rvert$	DC output offset voltage	between two channels	–	4	150	mV
MUTE POSITION (AT $I_{MUTE} \geq 300$ μA)						
V_O	output voltage	V_I = 600 mV	–	0.3	1.0	mV
Z_{2-7}	mute input impedance		–	9	–	kΩ
$I_{q(tot)}$	total quiescent current	$R_L = \infty$	18	40	70	mA
V_{no}	noise output voltage	note 3	–	70	140	μV
SVRR	supply voltage ripple rejection	note 4	40	55	–	dB
$\lvert \Delta V_{GND} \rvert$	DC output offset voltage		–	40	200	mV
$\lvert \Delta V_{off} \rvert$	offset voltage with respect to operating position		–	4	150	mV
I_2	current if pin 2 is connected to pin 5		–	–	6	mA
Mute position; note 5						
$\pm V_P$	supply voltage range		2	–	5.8	V
I_P	total quiescent current	$R_L = \infty$	9	30	40	mA
V_O	output voltage	V_I = 600 mV	–	0.3	1.0	mV
V_{no}	noise output voltage	note 3	–	70	140	μV
SVRR	supply voltage ripple rejection	note 4	40	55	–	dB
$\lvert \Delta V_{GND} \rvert$	DC output offset voltage		–	40	200	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operating position; note 6						
$I_{q(tot)}$	total quiescent current		18	40	70	mA
P_O	output power	THD = 0.5%	5	6	–	W
		THD = 10%	6.5	8	–	W
THD	total harmonic distortion	P_O = 4 W	–	0.13	0.2	%
B	power bandwidth	THD = 0.5%; note 1	–	40 to 20000	–	Hz
G_v	voltage gain		29	30	31	dB
$\lvert G_v \rvert$	gain unbalance		–	0.2	1	dB
V_{no}	noise output voltage	note 3	–	70	140	μV
$\lvert Z_i \rvert$	input impedance		14	20	26	kΩ
SVRR	supply voltage ripple rejection		35	44	–	dB
α_{cs}	channel separation		–	45	–	dB
MUTE POSITION ($I_{MUTE} \geq 300$ μA)						
V_O	output voltage	V_I = 600 mV	–	0.3	1.0	mV
Z_{2-7}	mute input impedance	note 7	6.7	9	11.3	kΩ
$I_{q(tot)}$	total quiescent current		18	40	70	mA
V_{no}	noise output voltage	note 3	–	70	140	μV
SVRR	supply voltage ripple rejection	note 4	35	44	–	dB
$\lvert \Delta V_{off} \rvert$	offset voltage with respect to operating position		–	4	150	mV
I_2	current if pin 2 is connected to pin 5		–	–	6	mA

Notes

1. $V_P = \pm 12$ V; $R_L = 8\ \Omega$; $T_{amb} = 25$ °C; $f_i = 1$ kHz; symmetrical power supply $I_{MUTE} = < 30$ μA (see Fig.4).
2. The power bandwidth is measured at a maximum output power (P_{Omax}) of –3 dB.
3. The noise output voltage (RMS value) is measured at $R_S = 2$ kΩ, unweighted (20 Hz to 20 kHz).
4. The ripple rejection is measured at $R_S = 0$ and $f_i = 100$ Hz to 20 kHz. The ripple voltage (200 mV) is applied in phase to the positive and the negative supply rails. With asymmetrical power supplies, the ripple rejection is measured at $f_i = 1$ kHz.
5. $\pm V_P = 4$ V; $R_L = 8\ \Omega$; $T_{amb} = 25$ °C; $f_i = 1$ kHz; symmetrical power supply (see Fig.4).
6. $V_P = 24$ V; $R_L = 8\ \Omega$; $T_{amb} = 25$ °C; $f_i = 1$ kHz; asymmetrical power supply $I_{MUTE} < 30$ μA (see Fig.5).
7. The internal network at pin 2 is a resistor divider of typical 4 kΩ and 5 kΩ to the positive supply rail. At the connection of the 4 kΩ and 5 kΩ resistor a zener diode of typical 6.6 V is also connected to the positive supply rail. The spread of the zener voltage is 6.1 to 7.1 V.

TEST AND APPLICATION INFORMATION

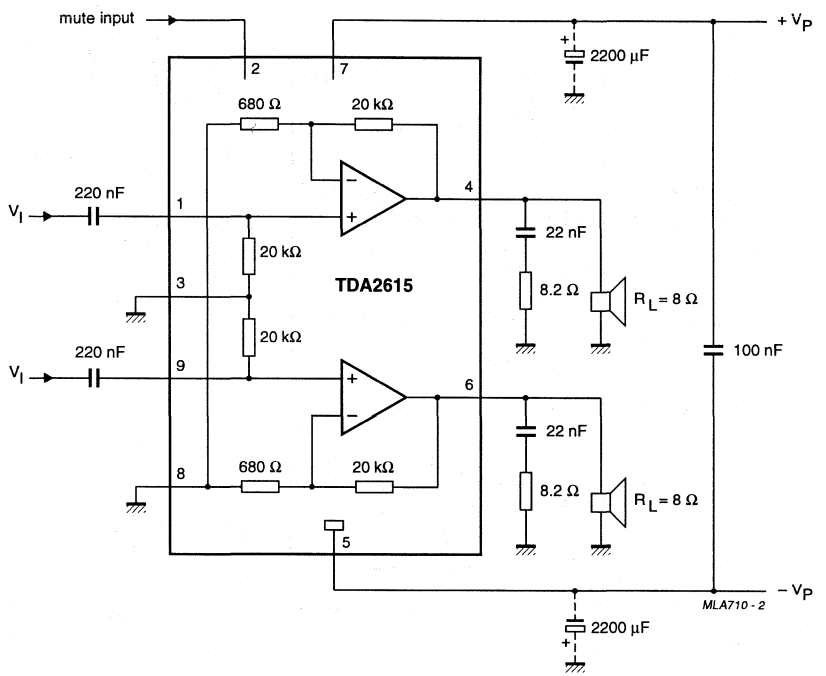


Fig.4 Test and application circuit with symmetrical power supply.

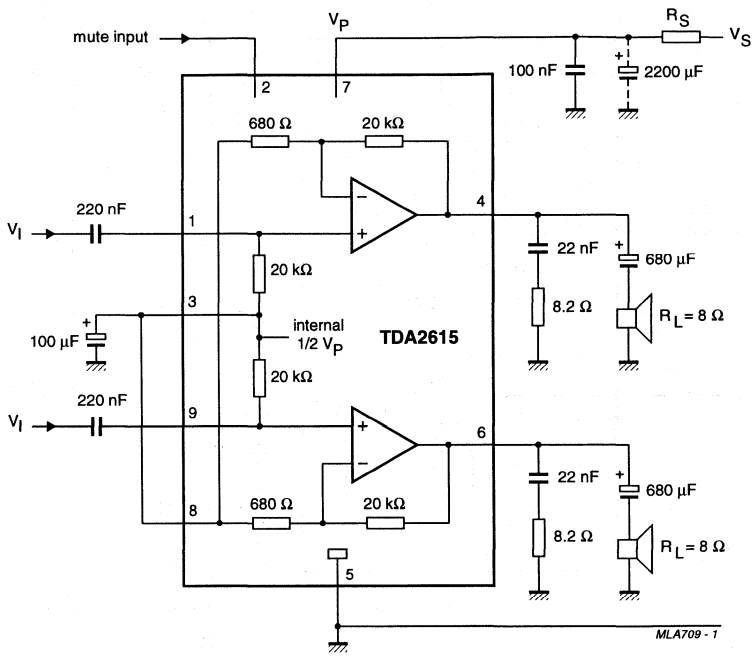


Fig.5 Test and application circuit with asymmetrical power supply.

2 x 12 W hi-fi audio power amplifiers with mute

TDA2616/TDA2616Q

FEATURES

- Requires very few external components
- No switch-on/switch-off clicks
- Input mute during switch-on and switch-off
- Low offset voltage between output and ground
- Excellent gain balance of both amplifiers
- Hi-fi in accordance with IEC 268 and DIN 45500
- Short-circuit proof and thermal protected
- Mute possibility.

GENERAL DESCRIPTION

The TDA2616 and TDA2616Q are dual power amplifiers. The TDA2616 is supplied in a 9-lead single-in-line (SIL9) plastic power package (SOT131), while the TDA2616Q is supplied in a 9-lead SIL-bent-to-DIL plastic power package (SOT157). They have been especially designed for mains fed applications, such as stereo radio and stereo TV.

QUICK REFERENCE DATA

Stereo application

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\pm V_P$	supply voltage range		7.5	–	21	V
P_O	output power	$V_P = \pm 16$ V; THD = 0.5%	–	12	–	W
G_v	internal voltage gain		–	30	–	dB
$\lvert G_v \rvert$	channel unbalance		–	0.2	–	dB
α	channel separation		–	70	–	dB
SVRR	supply voltage ripple rejection		–	60	–	dB
V_{no}	noise output voltage		–	70	–	μV

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA2616	9	SIL	plastic	SOT131[1]
TDA2616Q	9	SIL-bent-to-DIL	plastic	SOT157[2]

Notes

1. SOT131-2; 1996 August 27.
2. SOT157-2; 1996 August 27.

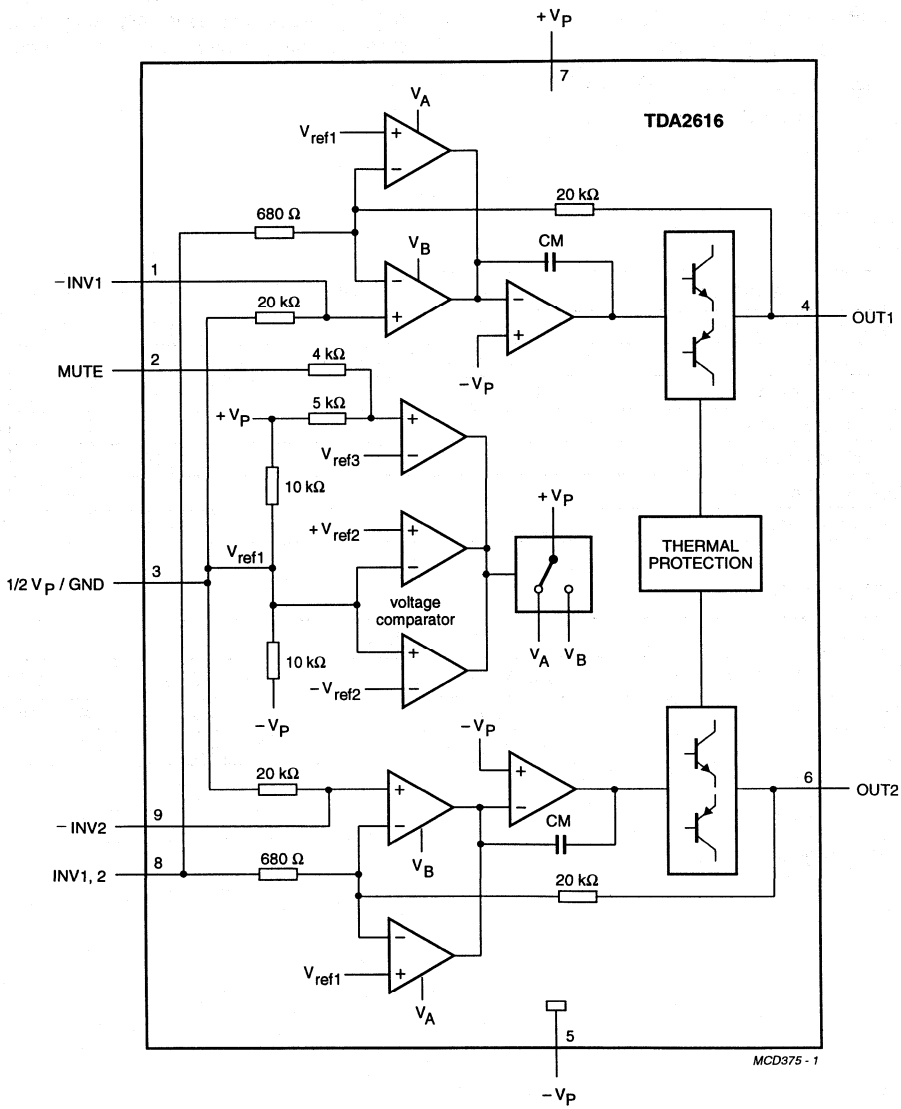


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
–INV1	1	non-inverting input 1
MUTE	2	mute input
1/2V_P/GND	3	1/2 supply voltage or ground
OUT1	4	output 1
$-V_P$	5	supply voltage (negative)
OUT2	6	output 2
$+V_P$	7	supply voltage (positive)
INV1, 2	8	inverting inputs 1 and 2
–INV2	9	non-inverting input 2

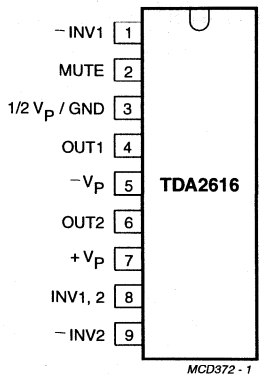


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA2616 is a hi-fi stereo amplifier designed for mains fed applications, such as stereo radio and TV. The circuit is optimally designed for symmetrical power supplies, but is also well-suited to asymmetrical power supply systems.

An output power of 2 × 12 W (THD = 0.5%) can be delivered into an 8 Ω load with a symmetrical power supply of ±16 V. The gain is internally fixed at 30 dB, thus offering a low gain spread and a very good gain balance between the two amplifiers (0.2 dB).

A special feature is the input mute circuit. This circuit disconnects the non-inverting inputs when the supply voltage drops below ±6 V, while the amplifier still retains its DC operating adjustment. The circuit features suppression of unwanted signals at the inputs, during switch-on and switch-off.

The mute circuit can also be activated via pin 2. When a current of 300 μA is present at pin 2, the circuit is in the mute condition.

The device is provided with two thermal protection circuits. One circuit measures the average temperature of the crystal and the other measures the momentary temperature of the power transistors. These control circuits attack at temperatures in excess of +150 °C, so a crystal operating temperature of max. +150 °C can be used without extra distortion.

With the derating value of 2.5 K/W, the heatsink can be calculated as follows:

at R_L = 8 Ω and V_P = ±16 V, the measured maximum dissipation is 14.6 W.

With a maximum ambient temperature of +65 °C, the thermal resistance of the heatsink is:

$$R_{th} = \frac{150 - 65}{14.6} - 2.5 = 3.3 \text{ K/W}.$$

The internal metal block has the same potential as pin 5.

LIMITING VALUES

In accordance with the Absolute maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_P$	supply voltage		–	21	V
I_{OSM}	non-repetitive peak output current		–	4	A
P_{tot}	total power dissipation	see Fig.3	–	25	W
T_{stg}	storage temperature range		–55	+150	°C
T_{XTAL}	crystal temperature		–	+150	°C
T_{amb}	ambient operating temperature range		–25	150	°C
t_{sc}	short circuit time	short-circuit to ground; note 1	–	1	h

Note to the limiting values

1. For asymmetrical power supplies (with the load short-circuited), the maximum unloaded supply voltage is limited to $V_P = 28$ V and with an internal supply resistance of $R_S \geq 4\ \Omega$, the maximum unloaded supply voltage is limited to 32 V **(with the load short-circuited)**. For symmetrical power supplies the circuit is short-circuit-proof up to $V_P = \pm 21$ V.

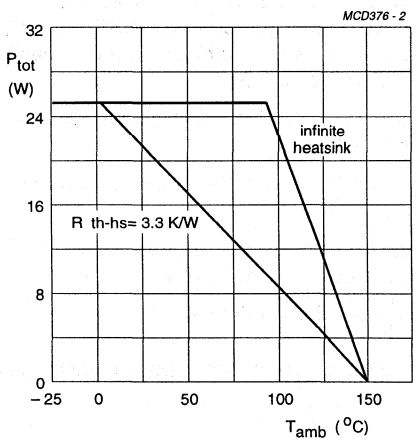


Fig.3 Power derating curve.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	2.5 K/W

CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
$\pm V_P$	supply voltage range		–	16	21	V
I_{ORM}	repetitive peak output current		–	2.2	–	A
Operating position; note 1						
$\pm V_P$	supply voltage range		7.5	16	21	V
I_P	total quiescent current	$R_L = \infty$	18	40	70	mA
P_O	output power					
		THD = 0.5%	10	12	–	W
		THD = 10%	12	15	–	W
THD	total harmonic distortion	P_O = 6 W	–	0.15	0.2	%
B	power bandwidth	THD = 0.5%; note 2	–	20 to 20 000	–	Hz
G_v	voltage gain		29	30	31	dB
$\lvert G_v \rvert$	gain unbalance		–	0.2	1	dB
V_{no}	noise output voltage	note 3	–	70	140	μV
$\lvert Z_i \rvert$	input impedance		14	20	26	kΩ
SVRR	supply voltage ripple rejection	note 4	40	60	–	dB
α	channel separation	R_S = 0	46	70	–	dB
I_{bias}	input bias current		–	0.3	–	μA
$\lvert \Delta V_{GND} \rvert$	DC output offset voltage		–	30	200	mV
$\lvert \Delta V_{4-6} \rvert$	DC output offset voltage	between two channels	–	4	150	mV
MUTE POSITION (AT $I_{MUTE} \geq 300$ μA)						
V_O	output voltage	V_I = 600 mV	–	0.3	1.0	mV
Z_{2-7}	mute input impedance	note 7	6.7	9	11.3	kΩ
I_P	total quiescent current	$R_L = \infty$	18	40	70	mA
V_{no}	noise output voltage	note 3	–	70	140	μV
SVRR	supply voltage ripple rejection	note 4	40	55	–	dB
$\lvert \Delta V_{GND} \rvert$	DC output offset voltage		–	40	200	mV
$\lvert \Delta V_{off} \rvert$	offset voltage with respect to operating position		–	4	150	mV
I_2	current if pin 2 is connected to pin 5		–	–	8.2	mA
Mute position; note 5						
$\pm V_P$	supply voltage range		2	–	5.8	V
I_P	total quiescent current	$R_L = \infty$	9	30	40	mA
V_O	output voltage	V_I = 600 mV	–	0.3	1.0	mV
V_{no}	noise output voltage	note 3	–	70	140	μV
SVRR	supply voltage ripple rejection	note 4	40	55	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert\Delta V_{GND}\rvert$	DC output offset voltage		–	40	200	mV
Operating position; note 6						
I_P	total quiescent current		18	40	70	mA
P_O	output power					
		THD = 0.5%	5	6	–	W
		THD = 10%	6.5	8	–	W
		THD = 0.5%; R_L = 4 Ω	–	10	–	W
		THD = 10%; R_L = 4 Ω	–	14	–	W
THD	total harmonic distortion	P_O = 4 W	–	0.13	0.2	%
B	power bandwidth	THD = 0.5%; note 2	–	40 to 20 000	–	Hz
G_v	voltage gain		29	30	31	dB
$\lvert G_v\rvert$	gain unbalance		–	0.2	1	dB
V_{no}	noise output voltage	note 3	–	70	140	μV
$\lvert Z_i\rvert$	input impedance		14	20	26	kΩ
SVRR	supply voltage ripple rejection		35	44	–	dB
α	channel separation		–	45	–	dB
MUTE POSITION ($I_{MUTE} \geq 300$ μA)						
V_O	output voltage	V_I = 600 mV	–	0.3	1.0	mV
Z_{2-7}	mute input impedance	note 7	6.7	9	11.3	kΩ
I_P	total quiescent current		18	40	70	mA
V_{no}	noise output voltage	note 3	–	70	140	μV
SVRR	supply voltage ripple rejection	note 4	35	44	–	dB
$\lvert\Delta V_{off}\rvert$	offset voltage with respect to operating position		–	4	150	mV
I_2	current if pin 2 is connected to pin 5		–	–	8.2	mA

Notes to the characteristics

1. V_P = ±16 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz; symmetrical power supply I_{MUTE} < 30 μA. See Fig.4
2. The power bandwidth is measured at an output power of $P_{O\,max}$ – 3 dB
3. The noise output voltage (RMS value) is measured at R_S = 2 kΩ, unweighted (20 Hz to 20 kHz)
4. The ripple rejection is measured at R_S = 0 and f = 100 Hz to 20 kHz. The ripple voltage (200 mV) is applied in phase to the positive and the negative supply rails. With asymmetrical power supplies, the ripple rejection is measured at f = 1 kHz
5. ±V_P = 4 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz; symmetrical power supply. See Fig.4
6. V_P = 24 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz; asymmetrical power supply I_{MUTE} < 30 μA. See Fig.5
7. The internal network at pin 2 is a resistor devider of typical 4 kΩ and 5 kΩ to the positive supply rail. At the connection of the 4 kΩ and 5 kΩ resistor a zener diode of typical 6.6 V is also connected to the positive supply rail. The spread of the zener voltage is 6.1 to 7.1 V.

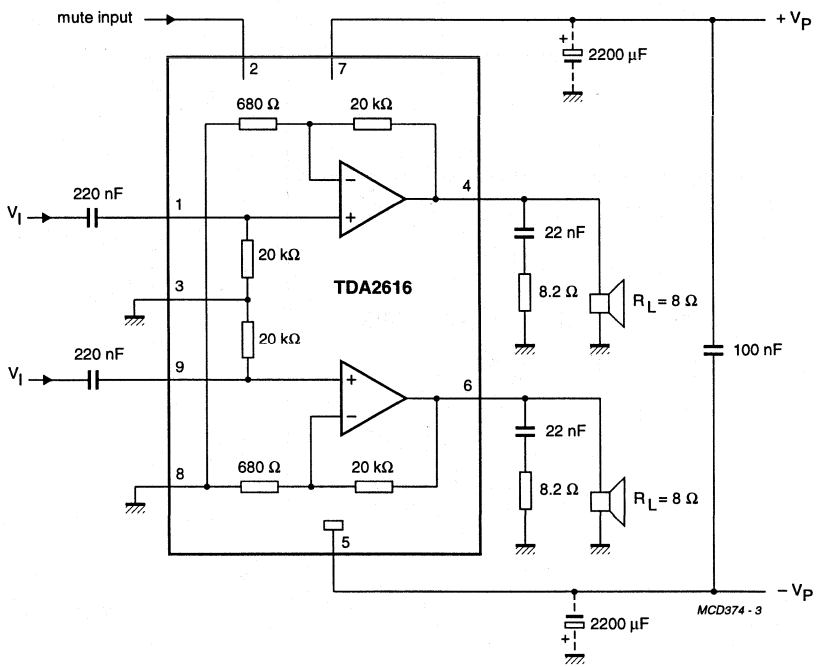


Fig.4 Test and application circuit with symmetrical power supply.

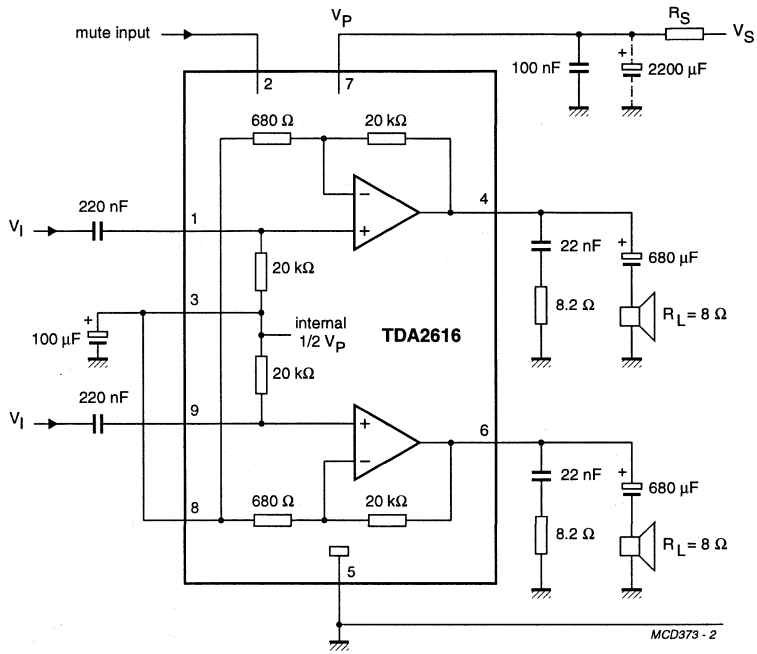


Fig.5 Test and application circuit with asymmetrical power supply.

Autosync Deflection Controller ASDC TDA4855

FEATURES

Concept features

- Full Horizontal (H) plus Vertical (V) autosync capability
- Completely DC controllable for analog and digital concepts
- Excellent geometry control functions (e.g. automatic correction of East-West (EW) parabola during adjustment of vertical size and vertical shift)
- Flexible Switched Mode Power Supply (SMPS) function block for feedback and feed forward converters
- Horizontal focus parabola with amplitude control
- X-ray protection
- Start-up and switch-off sequence for safe operation of all power components
- Very good vertical linearity
- Internal supply voltage stabilization
- SDIP32 package.

Synchronization inputs

- Can handle all sync signals (Horizontal, Vertical, Composite and Sync-on-video)
- Combined output for video clamping, vertical blanking and protection blanking.

Horizontal section

- Extremely low jitter
- Frequency locked loop for smooth catching of line frequency
- Simple frequency preset of f_{min} and f_{max} by external resistors
- DC controllable wide range linear picture position
- Soft start for horizontal driver.

Vertical section

- Vertical amplitude independent of frequency
- Automatic correction of picture height for VGA350 and VGA400 modes
- DC controllable picture height, picture position and S-correction
- Differential current outputs for DC coupling to vertical booster.

EW section

- Output for DC adjustable EW parabola with smoothed top
- DC controllable picture width and trapezium correction
- Optional tracking of EW parabola with line frequency
- Prepared for additional DC controls of vertical linearity, EW-corner, EW pin balance, EW parallelogram, vertical focus by extended application.

GENERAL DESCRIPTION

The TDA4855 is a high performance and efficient solution for autosync monitors. The concept is fully DC controllable and can be used in applications with a microcontroller and stand-alone in rock bottom solutions.

The TDA4855 provides synchronization processing, H + V synchronization with full autosync capability, and very short settling times after mode changes. External power components are given a great deal of protection. The IC generates the drive waveforms for DC-coupled vertical boosters such as TDA486X and TDA8351.

The TDA4855 provides extended functions e.g. as a flexible SMPS block and an extensive set of geometry control facilities, providing excellent picture quality.

Together with the Philips TDA488X video processor family a very advanced system solution is offered.

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC02 OR DATA SHEET

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	9.2	–	16	V
I_{CC}	supply current	–	49	–	mA
ΔHPOS	horizontal shift adjustment range	–	±10.5	–	%
ΔVAMP	vertical size adjustment range	60	–	100	%
ΔVPOS	vertical shift adjustment range	–	±11.5	–	%
ΔVSCOR	vertical S-correction adjustment range	2	–	46	%
ΔV_{EWPAR}	EW parabola adjustment range	0.15	–	3.0	V
ΔV_{EWWID}	horizontal size adjustment range	0.2	–	4.0	V
ΔV_{EWTRP}	trapezium correction adjustment range	–	±0.5	–	V
T_{amb}	operating ambient temperature	0	–	70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA4855	SDIP32	plastic shrink dual in-line package; 32 leads (400 mil)	SOT232-1

BLOCK DIAGRAM

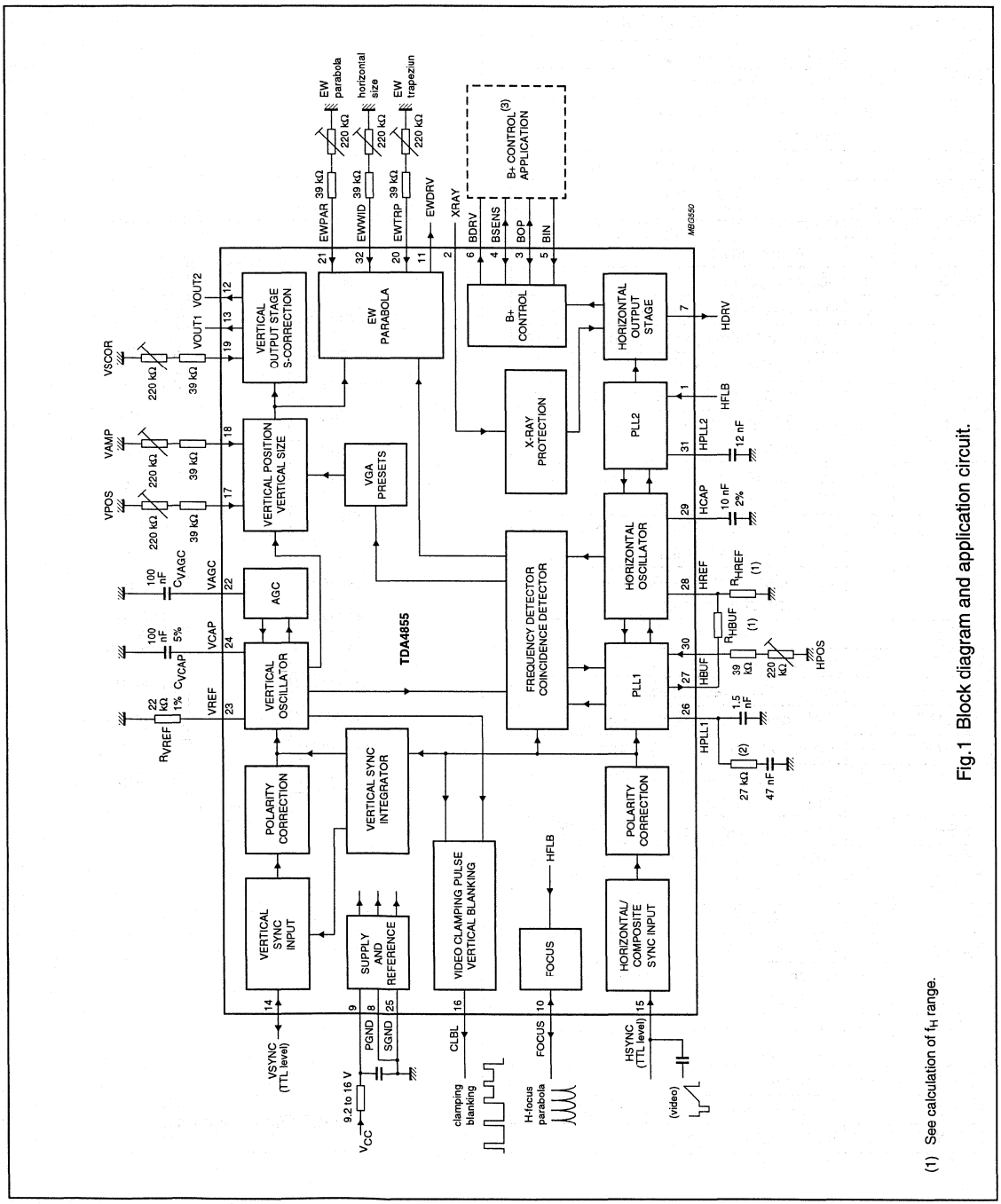


Fig.1 Block diagram and application circuit.

PINNING

SYMBOL	PIN	DESCRIPTION
HFLB	1	horizontal flyback input
XRAY	2	X-ray protection input
BOP	3	B+ control OTA output; comparator input
BSENS	4	B+ control comparator input/output
BIN	5	B+ control OTA input
BDRV	6	B+ control driver output
HDRV	7	horizontal driver output
PGND	8	power ground
V_{CC}	9	supply voltage
FOCUS	10	horizontal focus parabola input/output
EWDRV	11	EW parabola output
VOUT2	12	vertical output 2 (ascending sawtooth)
VOUT1	13	vertical output 1 (descending sawtooth)
VSYNC	14	vertical synchronization input/output (TTL level)
HSYNC	15	horizontal/composite synchronization input (TTL level or sync-on-video)
CLBL	16	video clamping pulse/vertical blanking and protection output
VPOS	17	vertical shift input
VAMP	18	vertical size input
VSCOR	19	vertical S-correction input
EWTRP	20	EW trapezium correction input
EWPAR	21	EW parabola amplitude input
VAGC	22	external capacitor for vertical amplitude control
VREF	23	external resistor for vertical oscillator
VCAP	24	external capacitor for vertical oscillator
SGND	25	signal ground
HPLL1	26	external filter for PLL1
HBUF	27	buffered f/v voltage output
HREF	28	reference current for horizontal oscillator
HCAP	29	external capacitor for horizontal oscillator
HPOS	30	horizontal shift input
HPLL2	31	external filter for PLL2/soft start
EWWID	32	horizontal size input

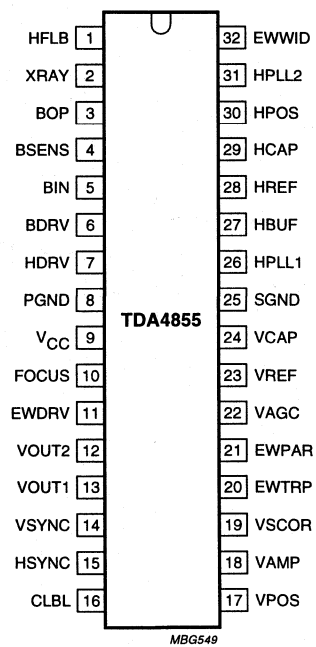


Fig.2 Pin configuration.

Vertical deflection power amplifier for monitors

TDA4861

FEATURES

- Vertical pre-amplifier with differential inputs
- Powerless vertical shift
- Flyback voltage generation suitable for two operating modes (doubling the supply voltage or external supply for the short flyback time, this achieves a minimum of power dissipation)
- Vertical output stage with thermal and SOAR protection
- High deflection frequency up to 140 Hz
- High linear sawtooth signal amplification
- Possibility of guarding the deflection
- Voltage stabilizer.

GENERAL DESCRIPTION

The TDA4861 is a vertical power amplifier for differential input signals suitable for colour monitor/TV systems with deflection frequency up to 140 Hz.

QUICK REFERENCE DATA

SYMBOL	PARAMETER[1]	MIN.	TYP.	MAX.	UNIT
V_{P1}	positive supply voltage (pin 1)	9	–	30	V
V_{P2}	positive supply voltage (pin 4)	9	–	60	V
V_{P3}	flyback supply voltage (pin 8)	9	–	60	V
I_{P1}	supply current (pin 1)	–	–	10	mA
I_{P2}	supply quiescent current (pin 4)	–	9	–	mA
V_I	input voltage range (pins 2 and 3)	1.6	–	$V_{P1} - 0.5$	V
I_5	deflection output current (peak-to-peak value, pin 5)	–	–	2.8	A
T_{amb}	operating ambient temperature range	–20	–	+75	°C

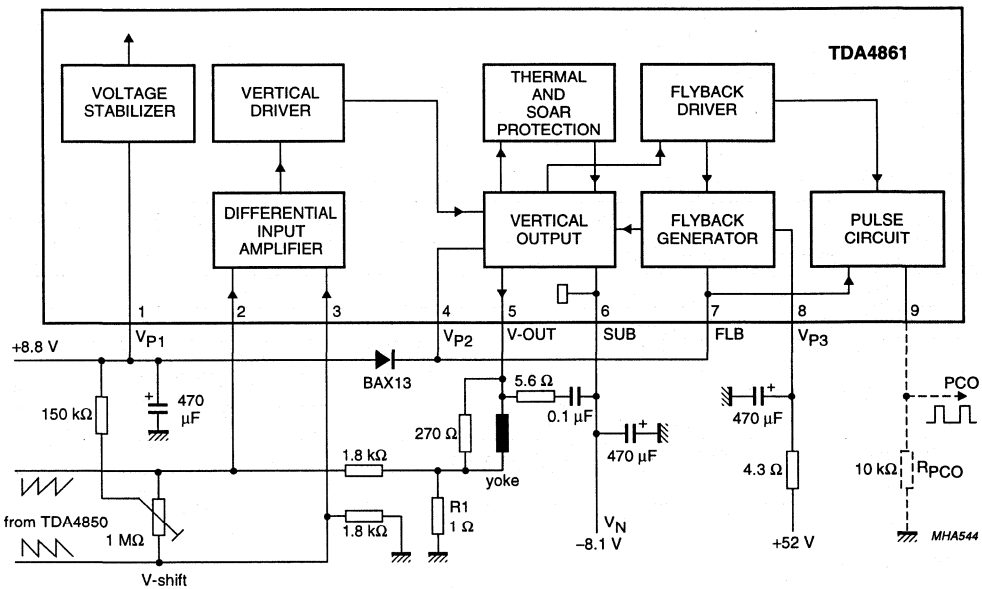
Note

1. Measurements referenced to substrate (pin 6).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA4861	SIL9P	plastic single in-line power package; 9 leads	SOT131-2

BLOCK DIAGRAM



Assumed values:

I_{yoke} = 1.42 A.
R_{yoke} = 4.17 Ω + 7% + ΔR(T) = 6.12 Ω.
L_{yoke} = 5.25 mH.
R_1 = 1.0 Ω ±1%.
T_{amb} = 65 °C.
T_{jmax} = 105 °C.
T_{yoke} = 75 °C.
P_{yoke} = 1.2 W.
P_{IC} = 1.8 W.
P_{tot} = 3.0 W.
$t_{p\ FLB}$ = typically 250 µs.

Attention: the heatsink of the IC must be isolated against ground (it is connected to pin 6).

Fig.1 Block diagram and application circuit with flyback supply voltage V_{P3} from an external source (deflection frequency range from 50 Hz up to 100 Hz).

PINNING

SYMBOL	PIN	DESCRIPTION
V_{P1}	1	positive supply voltage 1
INP1	2	input 1 of differential input amplifier
INP2	3	input 2 of differential input amplifier
V_{P2}	4	positive supply voltage 2 for vertical output stage
V-OUT	5	vertical output
SUB	6	substrate
FLB	7	flyback generator output
V_{P3}	8	positive flyback supply voltage 3
PCO	9	pulse circuit output

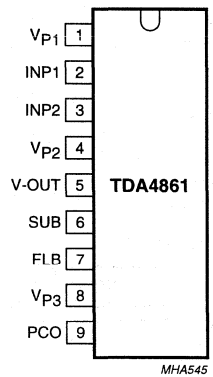


Fig.2 Pin configuration.

Stereo BTL audio output amplifier with DC volume control

TDA7053A

FEATURES

- DC volume control
- Few external components
- Mute mode
- Thermal protection
- Short-circuit proof
- No switch-on and switch-off clicks
- Good overall stability
- Low power consumption
- Low HF radiation
- ESD protected on all pins.

GENERAL DESCRIPTION

The TDA7053A (2 × 1 W) and TDA7053AT (2 × 0.5 W) are stereo BTL output amplifiers with DC volume control. The devices are designed for use in TV and monitors, but are also suitable for battery-fed portable recorders and radios.

Missing Current Limiter (MCL)

A MCL protection circuit is built-in. The MCL circuit is activated when the difference in current between the output terminal of each amplifier exceeds 100 mA (typical 300 mA). This level of 100 mA allows for headphone applications (single-ended).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		4.5	–	18	V
P_{out}	output power	V_P = 6 V				
	TDA7053A	R_L = 8 Ω	0.85	1.0	–	W
	TDA7053AT	R_L = 16 Ω	0.5	0.6	–	W
G_v	voltage gain		39.5	40.5	41.5	dB
G_C	gain control		68.0	73.5	–	dB
$I_{q(tot)}$	total quiescent current	V_P = 6 V; R_L = ∞	–	22	25	mA
THD	total harmonic distortion					
	TDA7053A	P_{out} = 0.5 W	–	0.3	1	%
	TDA7053AT	P_{out} = 0.25 W	–	0.3	1	%

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA7053A	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1
TDA7053AT	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1

BLOCK DIAGRAM

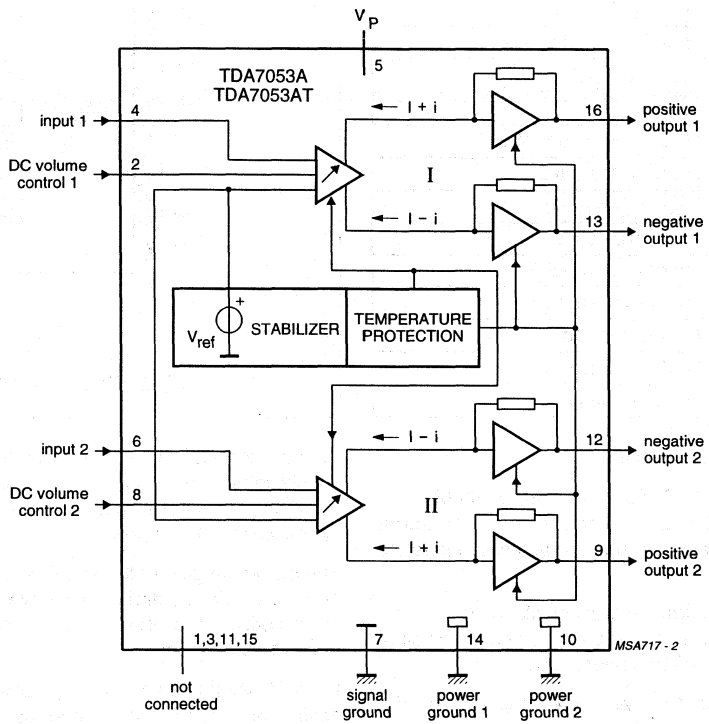


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
VC1	2	DC volume control 1
n.c.	3	not connected
$V_{I(1)}$	4	voltage input 1
V_P	5	positive supply voltage
$V_{I(2)}$	6	voltage input 2
SGND	7	signal ground
VC2	8	DC volume control 2
OUT2+	9	positive output 2
PGND2	10	power ground 2
n.c.	11	not connected
OUT2–	12	negative output 2
OUT1–	13	negative output 1
PGND1	14	power ground 1
n.c.	15	not connected
OUT1+	16	positive output 1

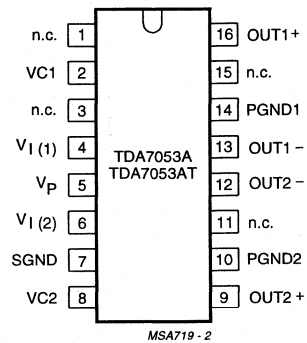


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA7053A and TDA7053AT are stereo output amplifiers with two DC volume control stages, designed for TV and monitors, but also suitable for battery-fed portable recorders and radios.

In conventional DC volume control circuits the control or input stage is AC coupled to the output stage via external capacitors to keep the offset voltage low.

The two DC volume control stages are integrated into the input stages so that no coupling capacitors are required and a low offset voltage is still maintained. The minimum supply voltage also remains low.

The BTL principle offers the following advantages:

- Lower peak value of the supply current
- The frequency of the ripple on the supply voltage is twice the signal frequency.

Consequently, a reduced power supply with smaller capacitors can be used which results in cost reductions.

For portable applications there is a trend to decrease the supply voltage, resulting in a reduction of output power at conventional output stages. Using the BTL principle increases the output power.

The maximum gain of the amplifier is fixed at 40.5 dB. The DC volume control stages have a logarithmic control characteristic. Therefore, the total gain can be controlled from +40.5 to –33 dB.

If the DC volume control voltage falls below 0.4 V, the device will switch to the mute mode.

The amplifier is short-circuit protected to ground, V_P and across the load. A thermal protection circuit is also implemented. If the crystal temperature rises above 150 °C the gain will be reduced, thereby reducing the output power.

Special attention is given to switch-on and switch-off clicks, low HF radiation and a good overall stability.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage		–	18	V
I_{ORM}	repetitive peak output current		–	1.25	A
I_{OSM}	non-repetitive peak output current		–	1.5	A
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C			
	TDA7053A		–	2.5	W
	TDA7053AT		–	1.32	W
t_{sc}	short-circuit time		–	1	hr
V_n	input voltage pins 2, 4, 6 and 8		–	5	V
T_{amb}	operating ambient temperature		–40	+85	°C
T_{stg}	storage temperature		–55	+150	°C
T_{vj}	virtual junction temperature		–	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	TDA7053A	50	K/W
	TDA7053AT	95	K/W

Power dissipation

TDA7053A:

Assume $V_P = 6$ V and $R_L = 8\ \Omega$.

The maximum sine wave dissipation is 2×0.9 W = 1.8 W.

The $R_{th\ j\text{-}a}$ of the package is 50 K/W therefore $T_{amb(max)} = 150 - (50 \times 1.8) = 60$ °C.

TDA7053AT:

Assume $V_P = 6$ V and $R_L = 16\ \Omega$.

The maximum sine wave dissipation is 2×0.46 W = 0.92 W.

The $R_{th\ j\text{-}a}$ of the package is 95 K/W therefore $T_{amb(max)} = 150 - (95 \times 0.92) = 62.6$ °C.

CHARACTERISTICS

V_P = 6 V; T_{amb} = 25 °C; f_i = 1 kHz; TDA7053A: R_L = 8 Ω; TDA7053AT: R_L = 16 Ω; unless otherwise specified (see Fig.13).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		4.5	–	18	V
$I_{q(tot)}$	total quiescent current	V_P = 6 V; R_L = ∞; note 1	–	22	25	mA
Maximum gain; $V_{2,8} \geq$ 1.4 V						
P_{out}	output power	THD = 10%				
	TDA7053A		1.0	1.1	–	W
	TDA7053AT		0.5	0.6	–	W
THD	total harmonic distortion					
	TDA7053A	P_{out} = 0.5 W	–	0.3	1	%
	TDA7053AT	P_{out} = 0.25 W	–	0.3	1	%
G_v	voltage gain		39.5	40.5	41.5	dB
$V_{I(rms)}$	input signal handling (RMS value)	G_v = 0 dB; THD < 1%	1	–	–	V
V_{no}	noise output voltage	f_i = 500 kHz; note 2	–	210	–	μV
B	bandwidth	at –1 dB	–	note 3	–	Hz
SVRR	supply voltage ripple rejection	note 4	34	38	–	dB
$V_{O(os)}$	DC output offset voltage	$\lvert V_{16} - V_{13} \rvert$ and $\lvert V_{12} - V_9 \rvert$	–	0	200	mV
Z_i	input impedance (pins 4 and 6)		15	20	25	kΩ
α_{cs}	channel separation	R_S = 5 kΩ	40	–	–	dB
$\lvert G_v \rvert$	channel unbalance	note 5	–	–	1	dB
		G_1 = 0 dB; note 6	–	–	1	dB
Mute position; $V_{2,8}$ = 0.4 V ±30 mV						
V_O	output voltage in mute position	V_i = 1.0 V; note 7	–	–	30	μV
DC volume control						
G_C	gain control		68.5	73.5	–	dB
I_{DC}	volume control current	$V_2 = V_8$ = 0 V	–20	–25	–30	μA

Notes

1. With a load connected to the outputs the quiescent current will increase, the maximum value of this increase being equal to the DC output offset voltage divided by R_L.
2. The noise output voltage (RMS value) at f_i = 500 kHz is measured with R_S = 0 Ω and bandwidth = 5 kHz.
3. 20 Hz to 300 kHz (typical).
4. The ripple rejection is measured with R_S = 0 Ω and f_i = 100 Hz to 10 kHz. The ripple voltage of 200 mV (RMS value) is applied to the positive supply rail.
5. The channel unbalance is measured with $V_{DC1} = V_{DC2}$.
6. The channel unbalance at G_1 = 0 dB is measured with $V_{DC1} = V_{DC2}$.
7. The noise output voltage (RMS value) is measured with R_S = 5 kΩ unweighted.

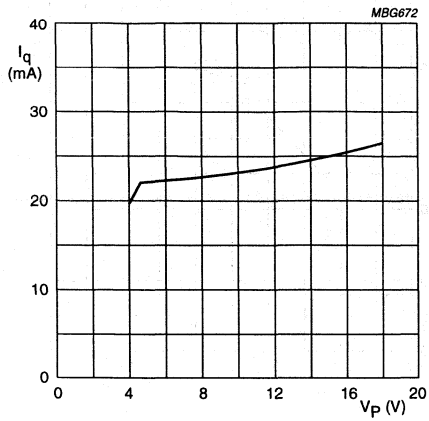
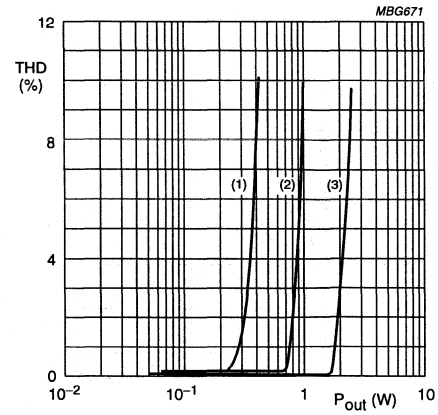
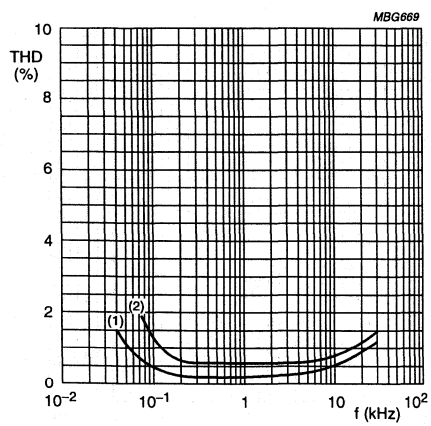


Fig.3 Quiescent current as a function of supply voltage.



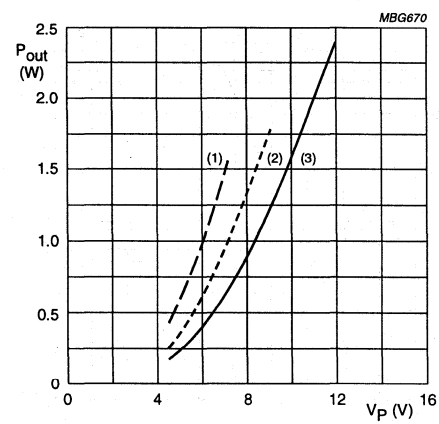
(1) V_P = 4.5 V.
(2) V_P = 6 V; R_L = 8 Ω.
(3) V_P = 12 V; R_L = 25 Ω.

Fig.4 THD as a function of output power.



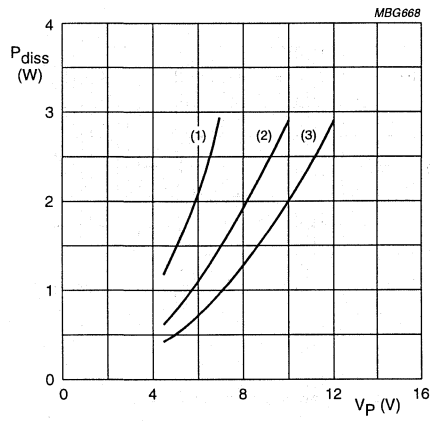
(1) G_v = 30 dB; P_o = 0.1 W.
(2) G_v = 40 dB; P_o = 0.1 W.

Fig.5 THD as a function of frequency.



(1) R_L = 8 Ω.
(2) R_L = 16 Ω.
(3) R_L = 25 Ω.

Fig.6 Output power as a function of supply voltage.



(1) R_L = 8 Ω.
(2) R_L = 16 Ω.
(3) R_L = 25 Ω.

Fig.7 Total worst case power dissipation as a function of supply voltage.

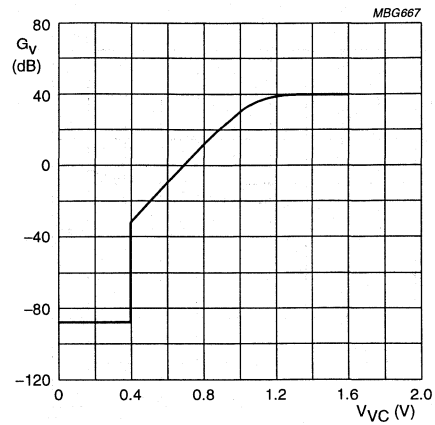
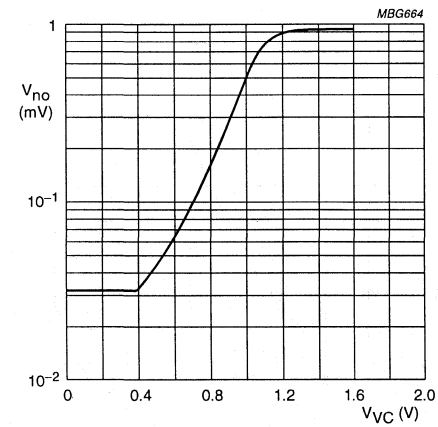
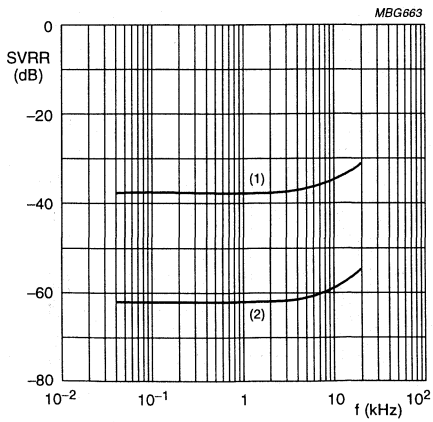


Fig.8 Voltage gain as a function of volume control voltage.



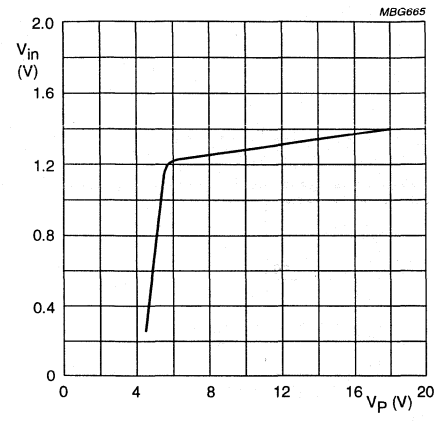
f = 22 Hz to 22 kHz.

Fig.9 Noise voltage as a function of volume control voltage.



(1) V_{DC} = 1.4 V; V_{ripple} = 0.2 V.
(2) V_{DC} = 0.4 V; V_{ripple} = 0.2 V.

Fig.10 SVRR as a function of frequency.



THD = 1 %.

Fig.11 Input signal handling.

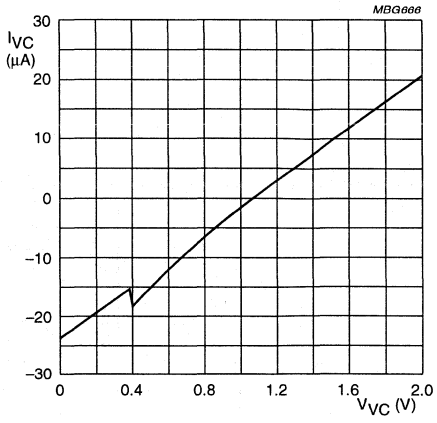


Fig.12 Volume control current as a function of volume control voltage.

APPLICATION INFORMATION

The application diagram is illustrated in Fig.13.

Test conditions

T_{amb} = 25 °C unless otherwise specified; V_P = 6 V; V_{DC} = 1.4 V; f_i = 1 kHz; R_L = 8 Ω.

The quiescent current has been measured without load impedance.

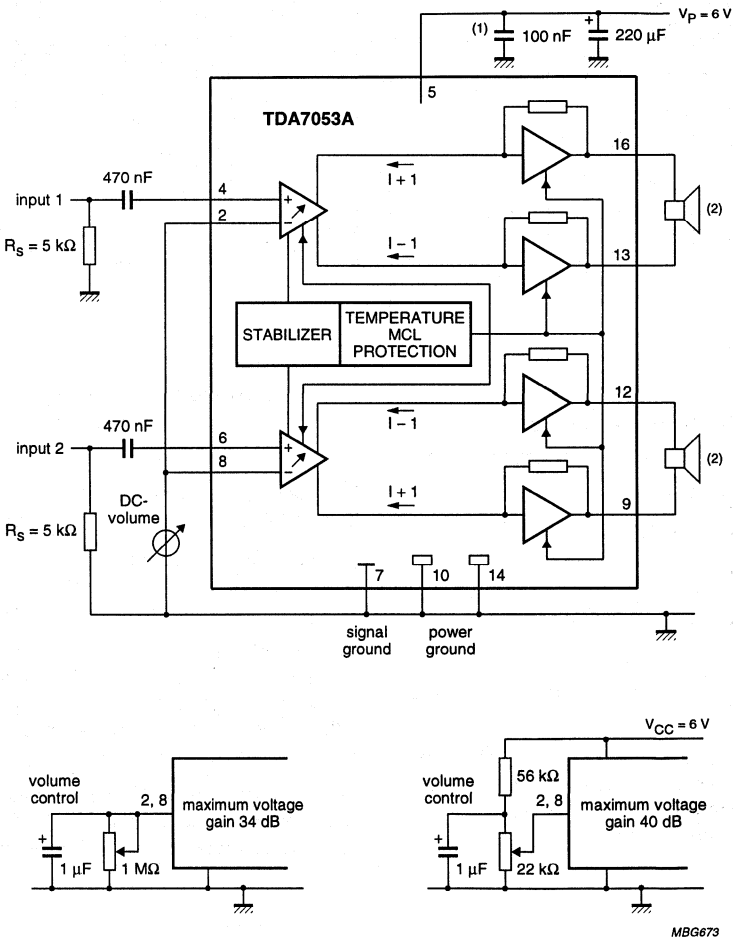
The output power as a function of the supply voltage has been measured at THD = 10%. The maximum output power is limited by the maximum power dissipation and the maximum available output current.

The maximum input signal voltage is measured at THD = 1% at the output with a voltage gain of 0 dB.

To avoid instabilities and too high distortion, the input ground and power ground must be separated as far as possible and connected as close as possible to the IC.

The DC volume control can be applied in several ways. Two possible circuits are shown below the main application diagram. The circuits at the control pin will influence the switch-on and switch-off behaviour and the maximum voltage gain.

For single-end applications the output peak current must not exceed 100 mA. At higher output currents the short-circuit protection (MCL) will be active.



(1) This capacitor can be omitted if the 220 µF electrolytic capacitor is connected close to pin 5.
(2) R_L = 8 Ω.

Fig.13 Test and application diagram.

2 x 5 W stereo BTL audio output amplifier with DC volume control

TDA7057AQ

FEATURES

- DC volume control
- Few external components
- Mute mode
- Thermal protection
- Short-circuit proof
- No switch-on and switch-off clicks
- Good overall stability
- Low power consumption
- Low HF radiation
- ESD protected on all pins.

GENERAL DESCRIPTION

The TDA7057AQ is a stereo BTL output amplifier with DC volume control. The device is designed for use in TV and monitors, but are also suitable for battery-fed portable recorders and radios.

Missing Current Limiter (MCL)

A MCL protection circuit is built-in. The MCL circuit is activated when the difference in current between the output terminal of each amplifier exceeds 100 mA (typical 300 mA). This level of 100 mA allows for headphone applications (single-ended).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		4.5	–	18	V
P_{out}	output power	V_P = 12 V; R_L = 16 Ω	3.0	3.5	–	W
		V_P = 12 V; R_L = 8 Ω	–	5.3	–	W
G_v	voltage gain		39.5	40.5	41.5	dB
G_C	gain control		68	73.5	–	dB
$I_{q(tot)}$	total quiescent current	V_P = 12 V; R_L = ∞	–	22	25	mA
THD	total harmonic distortion	P_{out} = 0.5 W	–	0.3	1	%

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA7057AQ	DBS13P	plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm)	SOT141-6

2 x 5 W stereo BTL audio output amplifier with DC volume control

TDA7057AQ

BLOCK DIAGRAM

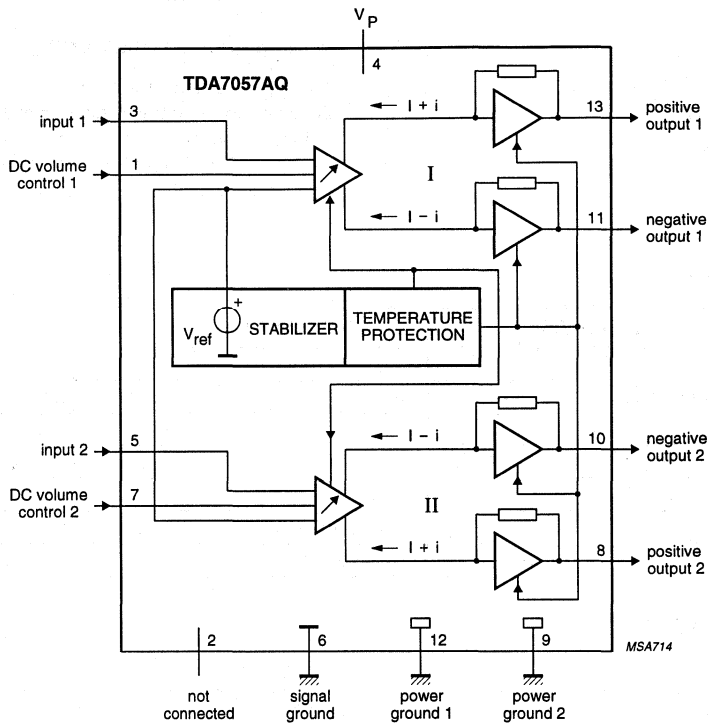


Fig.1 Block diagram.

2 x 5 W stereo BTL audio output amplifier with DC volume control

TDA7057AQ

PINNING

SYMBOL	PIN	DESCRIPTION
VC1	1	DC volume control 1
n.c.	2	not connected
$V_{I(1)}$	3	voltage input 1
V_P	4	positive supply voltage
$V_{I(2)}$	5	voltage input 2
SGND	6	signal ground
VC2	7	DC volume control 2
OUT2+	8	positive output 2
PGND2	9	power ground 2
OUT2–	10	negative output 2
OUT1–	11	negative output 1
PGND1	12	power ground 1
OUT1+	13	positive output 1

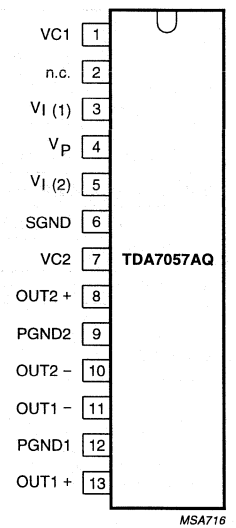


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA7057AQ is a stereo output amplifier with two DC volume control stages. The device is designed for TV and monitors, but are also suitable for battery-fed portable recorders and radios.

In conventional DC volume control circuits the control or input stage is AC coupled to the output stage via external capacitors to keep the offset voltage low.

In the TDA7057AQ the two DC volume control stages are integrated into the input stages so that no coupling capacitors are required and a low offset voltage is still maintained. The minimum supply voltage also remains low.

The BTL principle offers the following advantages;

- Lower peak value of the supply current
- The frequency of the ripple on the supply voltage is twice the signal frequency.

Consequently, a reduced power supply with smaller capacitors can be used which results in cost reductions.

For portable applications there is a trend to decrease the supply voltage, resulting in a reduction of output power at conventional output stages. Using the BTL principle increases the output power.

The maximum gain of the amplifier is fixed at 40.5 dB. The DC volume control stages have a logarithmic control characteristic. Therefore, the total gain can be controlled from +40.5 dB to –33 dB. If the DC volume control voltage falls below 0.4 V, the device will switch to the mute mode.

The amplifier is a short-circuit protected to ground, V_P and across the load. A thermal protection circuit is also implemented. If the crystal temperature rises above +150 °C the gain will be reduced, thereby reducing the output power.

Special attention is given to switch-on and switch-off clicks, low HF radiation and a good overall stability.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage		–	18	V
I_{ORM}	repetitive peak output current		–	1.25	A
I_{OSM}	non-repetitive peak output current		–	1.5	A
P_{tot}	total power dissipation	$T_{case} < 60$ °C	–	22.5	W
T_{amb}	operating ambient temperature		–40	+85	°C
T_{stg}	storage temperature		–55	+150	°C
T_{vj}	virtual junction temperature		–	+150	°C
t_{sc}	short-circuit time		–	1	hr
V_n	input voltage pins 1, 3, 5 and 7		–	5	V

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	4	K/W
$R_{th\ j\text{-}c}$	thermal resistance from junction to case	40	K/W

Power dissipation

Assume $V_P = 12$ V and $R_L = 16\ \Omega$. The maximum sine wave dissipation is 2×1.8 W = 3.6 W.

At $T_{amb\ (max)} = 60$ °C;

$R_{th\ tot} = (150 - 60)/3.6 = 25$ K/W

$R_{th\ tot} = R_{th\ j\text{-}c} + R_{th\ c\text{-}hs} + R_{th\ hs}$

$R_{th\ c\text{-}hs} + R_{th\ hs} = 25 - 4 = 21$ K/W

CHARACTERISTICS

V_P = 12 V;T_{amb} = 25 °C; f_i = 1 kHz; R_L = 16 Ω; unless otherwise specified (see Fig.13).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	voltage supply		4.5	–	18.5	V
$I_{q(tot)}$	total quiescent current	V_P = 12 V; R_L = ∞; note 1	–	22	25	mA
Maximum gain; $V_{1,7} \geq$ 1.4 V						
P_{out}	output power	THD = 10%; R_L = 16 Ω	3.0	3.5	–	W
		THD = 10%; R_L = 8 Ω	–	5.3	–	W
THD	total harmonic distortion	P_{out} = 0.5 W	–	0.3	1	%
G_v	voltage gain		39.5	40.5	41.5	dB
$V_{I(rms)}$	input signal handling (RMS value)	G_v = 0 dB; THD < 1%	1	–	–	V
V_{no}	noise output voltage	f_i = 500 kHz; note 2	–	210	–	μV
B	bandwidth	at –1 dB	–	note 3	–	dB
SVRR	supply voltage ripple rejection	note 4	34	38	–	dB
$V_{O(os)}$	DC output offset voltage	$\lvert V_{13}-V_{11}\rvert$ and $\lvert V_{10}-V_8\rvert$	–	0	200	mV
Z_i	input impedance (pins 3 and 5)		15	20	25	kΩ
α_{cs}	channel separation	R_s = 5 kΩ	40	–	–	dB
$\lvert G_v\rvert$	channel unbalance	note 5	–	–	1	dB
		G_1 = 0 dB; note 6	–	–	1	dB
Mute position; $V_1 = V_7$ =0.4 V ±30 mV						
V_O	output voltage in mute position	V_I = 1.0 V; note 7	–	35	40	μV
DC volume control						
G_C	gain control range		68	73.5	–	dB
I_{DC}	volume control current	$V_1 = V_7$ = 0 V	–20	–25	–30	μA

Notes

1. With a load connected to the outputs the quiescent current will increase, the maximum value of this increase being equal to the DC output offset voltage divided by R_L.
2. The noise output voltage (RMS value) at f_i = 500 kHz is measured with R_S = 0 Ω and bandwidth = 5 kHz.
3. 20 Hz to 300 kHz (typical.
4. The ripple rejection is measured with R_S = 0 Ω and f = 100 Hz to 10 kHz. The ripple voltage of 200 mV (RMS value) is applied to the positive supply rail.
5. The channel unbalance is measured with $V_{DC1} = V_{DC2}$.
6. The channel unbalance at G_1 = 0 dB is measured with $V_{DC1} = V_{DC2}$.
7. The noise output voltage (RMS value) is measured with R_S = 5 kΩ unweighted.

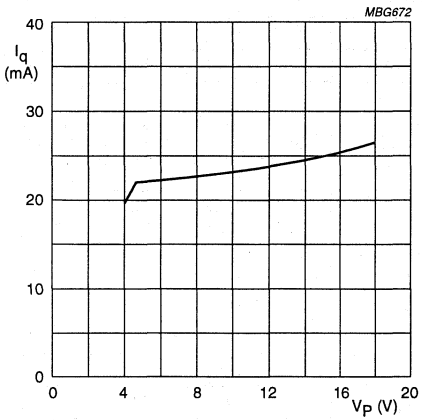
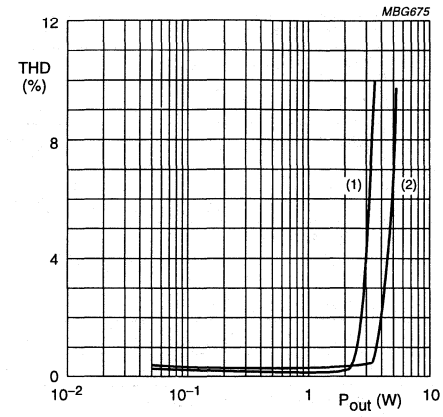
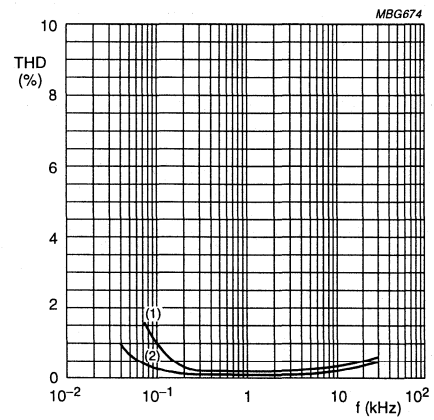


Fig.3 Quiescent current as a function of supply voltage.



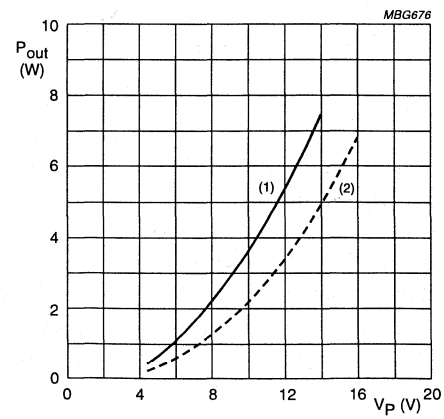
(1) R_L = 16 Ω.
(2) R_L = 8 Ω.

Fig.4 THD as a function of output power.



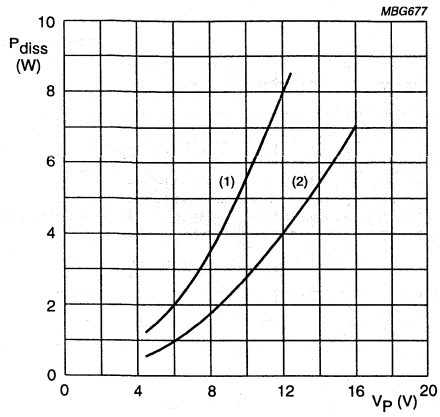
(1) G_v = 40 dB; P_o = 0.5 W.
(2) G_v = 30 dB; P_o = 0.5 W.

Fig.5 THD as a function of frequency.



(1) R_L = 8 Ω.
(2) R_L = 16 Ω.

Fig.6 Output power as a function of supply voltage.



(1) R_L = 8 Ω.
(2) R_L = 16 Ω.

Fig.7 Total worst case power dissipation as a function of supply voltage.

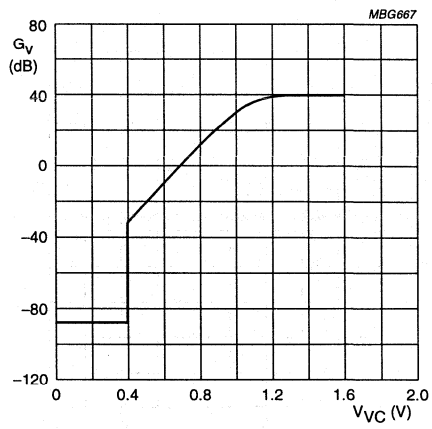
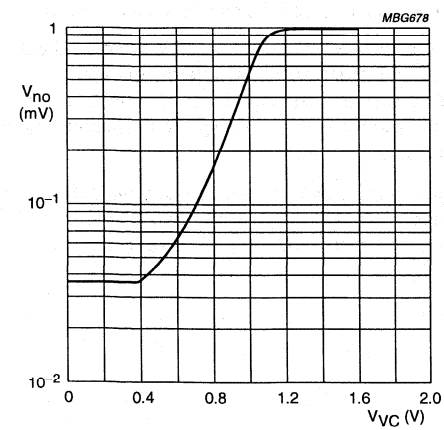
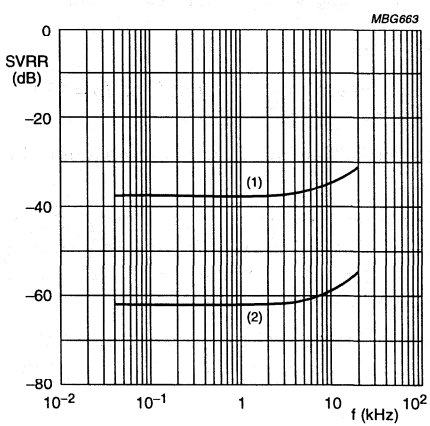


Fig.8 Voltage gain as a function of volume control voltage.



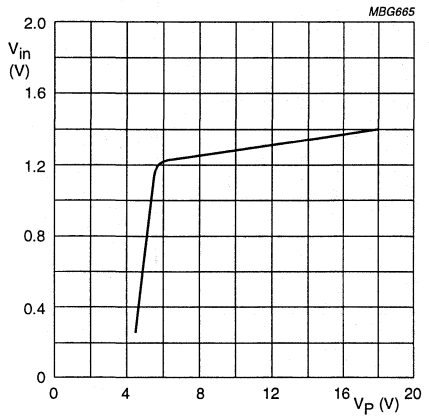
Frequency = 22 Hz to 22 kHz.

Fig.9 Noise voltage as a function of volume control voltage.



(1) V_{DC} = 1.4 V; V_{ripple} = 0.2 V.
(2) V_{DC} = 0.4 V; V_{ripple} = 0.2 V.

Fig.10 SVRR as a function of frequency.



THD = 1 %.

Fig.11 Input signal handling

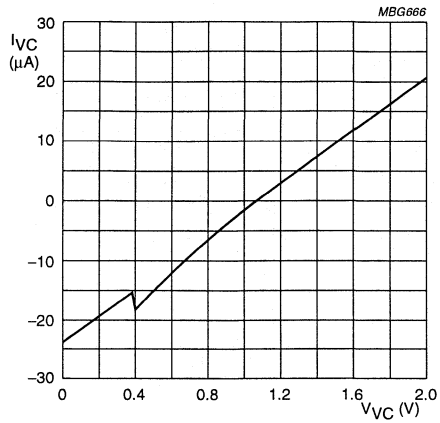


Fig.12 Volume control current as a function of volume control voltage.

APPLICATION INFORMATION

The application diagram is illustrated in Fig.13.

Test conditions

T_{amb} = 25 °C unless otherwise specified; V_P = 12 V; V_{DC} = 1.4 V; f_i = 1 kHz; R_L = 16 Ω.

The quiescent current has been measured without load impedance.

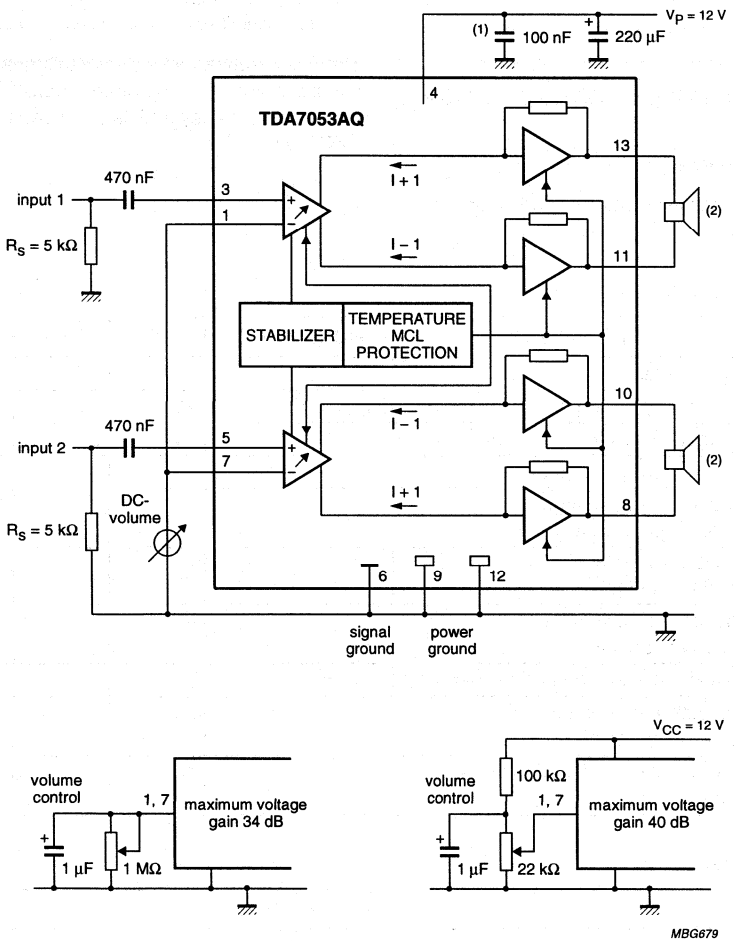
The output power as a function of the supply voltage has been measured at THD = 10%. The maximum output power is limited by the maximum power dissipation and the maximum available output current.

The maximum input signal voltage is measured at THD = 1% at the output with a voltage gain of 0 dB.

To avoid instabilities and too high a distortion, the input ground and power ground must be separated as far as possible and connected as close as possible to the IC.

The DC volume control can be applied in several ways. Two possible circuits are shown below the main application diagram. The circuits at the control pin will influence the switch-on and switch-off behaviour and the maximum voltage gain.

For single-end applications the output peak current must not exceed 100 mA. At higher output currents the short-circuit protection (MCL) will be active.



(1) This capacitor can be omitted if the 220 µF electrolytic capacitor is connected close to pin 5.
(2) R_L = 16 Ω.

Fig.13 Test and application diagram.

Quadrature demodulator TDA8040T

FEATURES

- +5 V supply voltage
- Bandgap internal reference voltage
- Low crosstalk between I (in-phase) and Q (quadrature) channel outputs
- High operating input sensitivity
- High Carrier-to-Noise Ratio (CNR) of the VCO.

APPLICATIONS

- Quadrature Phase Shift Keying (QPSK) demodulation.

GENERAL DESCRIPTION

The TDA8040T is a monolitic bipolar IC dedicated for quadrature demodulation.

It has been designed to operate in conjunction with the TDA8041H to provide a complete QPSK demodulator.

The design of this circuit has been optimized to provide the best quadrature accuracy necessary for digital receiver applications and particularly for digital television.

The TDA8040T includes two matched mixers, an RF amplifier, a symmetrical Voltage Controlled Oscillator (VCO), a frequency divider and two matched amplifiers. Two external filters are required for the baseband filtering.

The VCO requires an external LC tank circuit with two varicap diodes. This oscillator operates at twice the IF carrier frequency and can be used in a carrier recovery AFC loop.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		4.5	5.0	5.5	V
$I_{CC(tot)}$	total supply current	V_{CC} = 5 V	70	79	90	mA
$V_{i(RF)}$	operating input voltage level		64	67	70	dBμV
$f_{i(RF)}$	RF input signal frequency		10.7	–	150	MHz
$V_{oIQ(p-p)}$	I and Q output voltage (peak-to-peak value)		–	0.5	–	V
$E\phi_{(IQ)}$	phase error between the I and Q channels		–	–	3	deg
$E_{G(IQ)}$	gain error between the I and Q channels		–	–	1	dB
$E_{G(tilt)}$	gain tilt error in the I and Q channels		–	–	1	dB
$\alpha_{ct(IQ)}$	crosstalk between the I and Q channels		30	–	–	dB
IM3	intermodulation distortion in the I and Q channels		40	–	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8040T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC02 OR DATA SHEET

BLOCK DIAGRAM

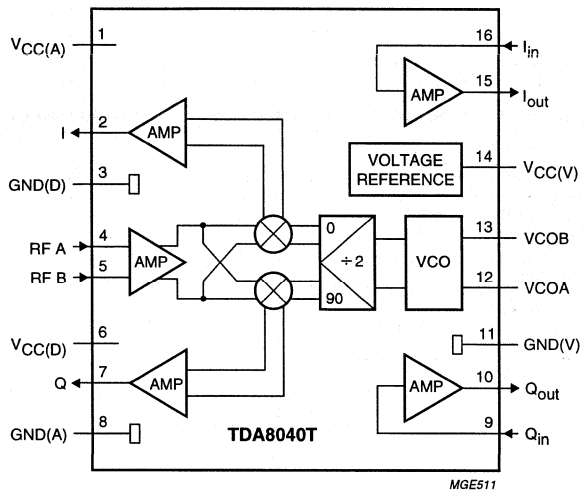


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$V_{CC(A)}$	1	supply voltage for I and Q amplifiers
I	2	I channel buffer output
GND(D)	3	demodulator ground
RF A	4	RF input A
RF B	5	RF input B
$V_{CC(D)}$	6	supply voltage for demodulator
Q	7	Q channel buffer output
GND(A)	8	I and Q amplifiers ground
Q_{in}	9	Q channel amplifier input
Q_{out}	10	Q channel amplifier output
GND(V)	11	VCO ground
VCOA	12	VCO tank circuit A
VCOB	13	VCO tank circuit B
$V_{CC(V)}$	14	supply voltage for VCO
I_{out}	15	I channel amplifier output
I_{in}	16	I channel amplifier input

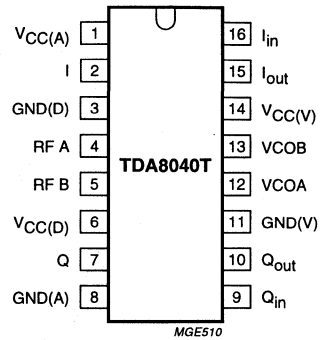


Fig.2 Pin configuration.

Quadrature demodulator controller TDA8041H

FEATURES

- Generates all control signals for Quadrature Phase-Shift Keying (QPSK) and Binary Phase-Shift Keying (BPSK) demodulation
- Can be used in applications with low E_b/N_o and high symbol rate (up to 30×10^6 symbols/s)
- Digital I and Q outputs (3 bits) for soft decision within error correction
- Two matched analog-to-digital converters to quantize the I and Q signals
- A digital detector for each control loop to generate the required control signals
- Digital-to-analog converters and operational amplifiers to allow high flexibility for loop time constants
- Special input stage to interface with the voltage controlled crystal oscillator
- Positive 5 V supply voltage.

APPLICATIONS

- Demodulation of BPSK and QPSK modulated signals in satellite and telephone applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{DD(A)}$	supply voltage for operational amplifiers (pin 5)		4.75	5.0	5.25	V
$V_{DDA(C)}$	analog supply voltage for converters (pin 20)		4.75	5.0	5.25	V
$V_{DD(I/O)}$	supply voltage for digital inputs/outputs (pin 30)		4.75	5.0	5.25	V
V_{DDD}	supply voltage for digital section (pin 35)		4.75	5.0	5.25	V
$V_{DD(C)}$	supply voltage for digital part of ADC and DAC (pin 42)		4.75	5.0	5.25	V
$I_{DD(tot)}$	total supply current	V_{DD} = 5 V	–	30	–	mA
V_{IQ}	I and Q input voltage		–	1.0	–	V
R_{sym}	symbol rate		–	–	30×10^6	symbols/s
$I_{O(DAC)}$	DAC output current		−100	–	+100	mA

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8041H	QFP44[1]	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm; high stand-off height	SOT307-2

Note

1. When using reflow soldering it is recommended that the Drypack instructions in the *"Quality Reference Handbook"* (order number 9398 510 63011) are followed.

BLOCK DIAGRAM

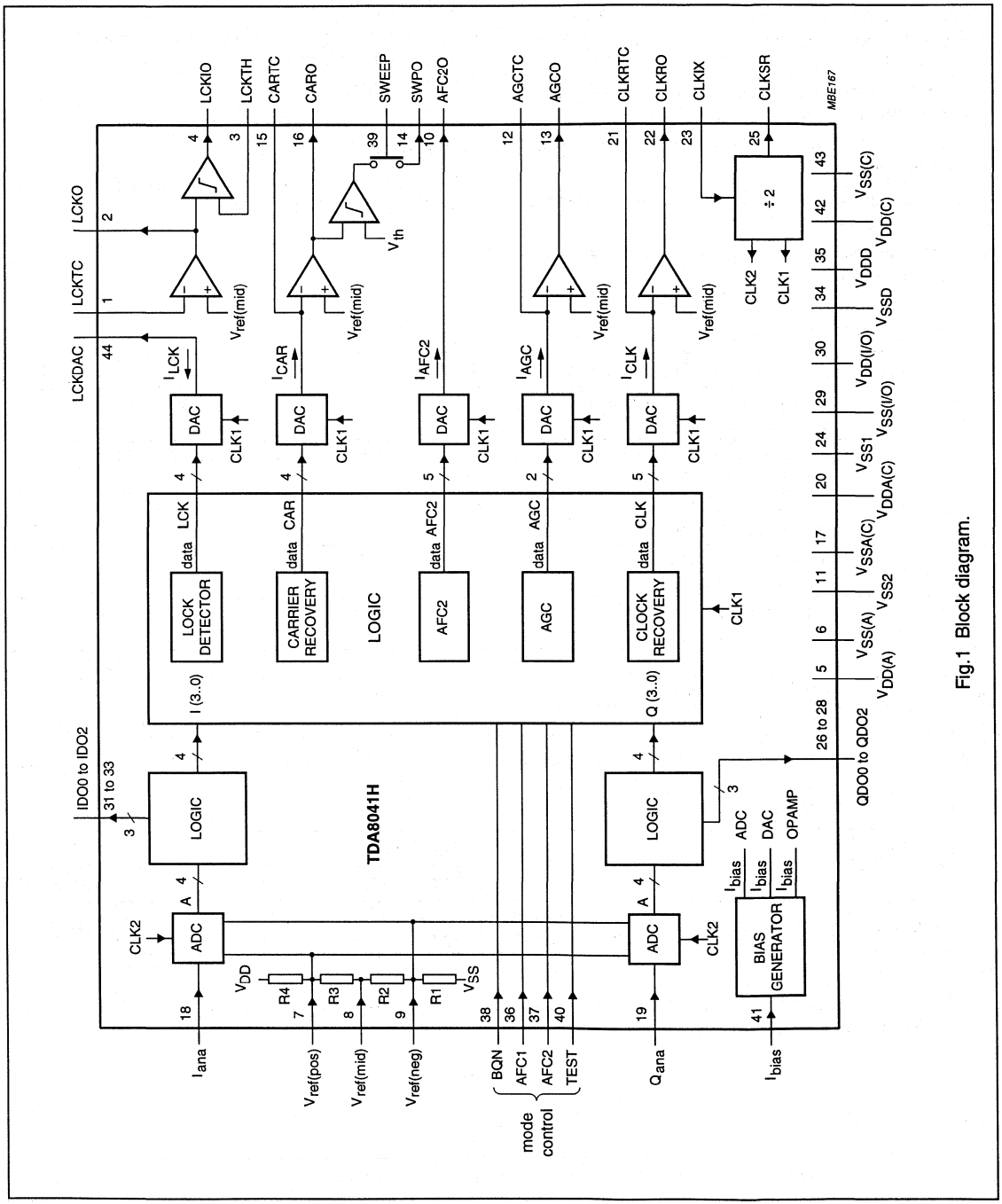


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
LCKTC	1	carrier lock time constant
LCKO	2	carrier lock output
LCKTH	3	carrier lock threshold voltage
LCKIO	4	carrier lock indicator output
$V_{DD(A)}$	5	supply voltage for operational amplifiers
$V_{SS(A)}$	6	negative supply voltage for operational amplifiers
$V_{ref(pos)}$	7	positive reference voltage for converters
$V_{ref(mid)}$	8	middle reference voltage for converters
$V_{ref(neg)}$	9	negative reference voltage for converters
AFC2O	10	AFC 2 output
V_{SS2}	11	negative supply voltage 2
AGCTC	12	automatic gain control time constant
AGCO	13	automatic gain control output
SWPO	14	sweep current output
CARTC	15	carrier recovery time constant
CARO	16	carrier recovery output
$V_{SSA(C)}$	17	analog negative supply voltage for converters
I_{ana}	18	analog input I
Q_{ana}	19	analog input Q
$V_{DDA(C)}$	20	analog supply voltage for converters
CLKRTC	21	clock recovery time constant
CLKRO	22	clock recovery output
CLKIX	23	clock input from crystal circuit (at double symbol rate)

SYMBOL	PIN	DESCRIPTION
V_{SS1}	24	negative supply voltage 1
CLKSR	25	clock output at symbol rate
QDO2	26	Q digital output (bit 2)
QDO1	27	Q digital output (bit 1)
QDO0	28	Q digital output (bit 0)
$V_{SS(I/O)}$	29	negative supply voltage for digital inputs/outputs
$V_{DD(I/O)}$	30	supply voltage for digital inputs/outputs
IDO2	31	I digital output (bit 2)
IDO1	32	I digital output (bit 1)
IDO0	33	I digital output (bit 0)
V_{SSD}	34	negative supply voltage for digital section
V_{DDD}	35	supply voltage for digital section
AFC1	36	AFC control switch 1 (1 = on; 0 = off)
AFC2	37	AFC control switch 2 (1 = on; 0 = off)
BQN	38	BPSK/QPSK control switch (1 = BPSK; 0 = QPSK)
SWEEP	39	sweep control switch (1 = on; 0 = off)
TEST	40	test control switch (1 = on; 0 = off)
I_{bias}	41	input bias current for analog blocks
$V_{DD(C)}$	42	supply voltage for digital part of ADC and DAC
$V_{SS(C)}$	43	negative supply voltage for digital part of ADC and DAC
LCKDAC	44	carrier lock DAC output

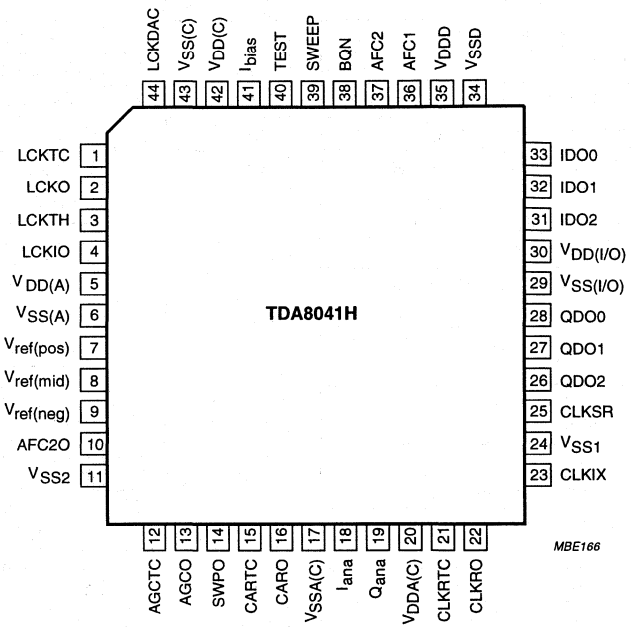


Fig.2 Pin configuration.

Multi-mode QAM demodulator TDA8046

FEATURES

- Different modulation schemes: 4, 16, 32, 64 and 256-QAM
- Digital demodulator and square root raised cosine Nyquist filter with roll-off of 15% or 20%
- High performance adaptive equalizer (no training sequence needed)
- Digital detectors for generation of required control voltages for carrier recovery, clock recovery and AGC
- Digital-to-analog converters and operational amplifiers allowing high flexibility for selection of the (PLL) loop time constants
- High maximum symbol rate (r_s) of 7 Msymbols/s
- Input format: Straight binary or 2's complement (up to 9 bits, TTL compatible)
- Output format: 8-bit wide bus (CMOS compatible)
- I²C-bus interface to initialize and monitor the demodulator. When no I²C-bus usage; 64-QAM, 20% roll-off factor in default mode
- 5 V peripheral and analog supply voltage
- 3.3 V core supply voltage
- Boundary scan test.

APPLICATION

Demodulation for digital cable TV and cable modem.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{DDD(core)}$	core supply voltage		3.00	3.30	3.60	V
V_{DDD}	digital peripheral supply voltage		4.75	5.00	5.25	V
V_{DDA}	analog supply voltage		4.75	5.00	5.25	V
$I_{DDD(core)}$	core supply current	$V_{DDD(core)}$ = 3.3 V; note 1	–	100	–	mA
I_{DDD}	digital peripheral supply current	V_{DDD} = 5 V; note 1	–	14	–	mA
I_{DDA}	analog supply current	V_{DDA} = 5 V; note 1	–	16	–	mA
r_s	symbol rate		–	–	7	Msym/s
IL	implementation loss	note 2	–	0.7	–	dB
α	Nyquist roll-off (programmable)		–	15 or 20	–	%
SNR_{lock}	signal-to-noise ratio for locking a 64-QAM constellation		21	–	–	dB
	signal-to-noise ratio for locking a 256-QAM constellation		27	–	–	dB

Note

1. The supply currents are specified for the maximum symbol frequency.
2. The implementation loss (IL) of the demodulator is defined as the distance between the measured and theoretical BER curve as function of signal-to-noise ratio at a BER = 10^{-6} for a back-to-back measurement at the IF frequency. This performance depends on the chosen loop parameters (see *Application notes*).

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC02 OR DATA SHEET

BLOCK DIAGRAM

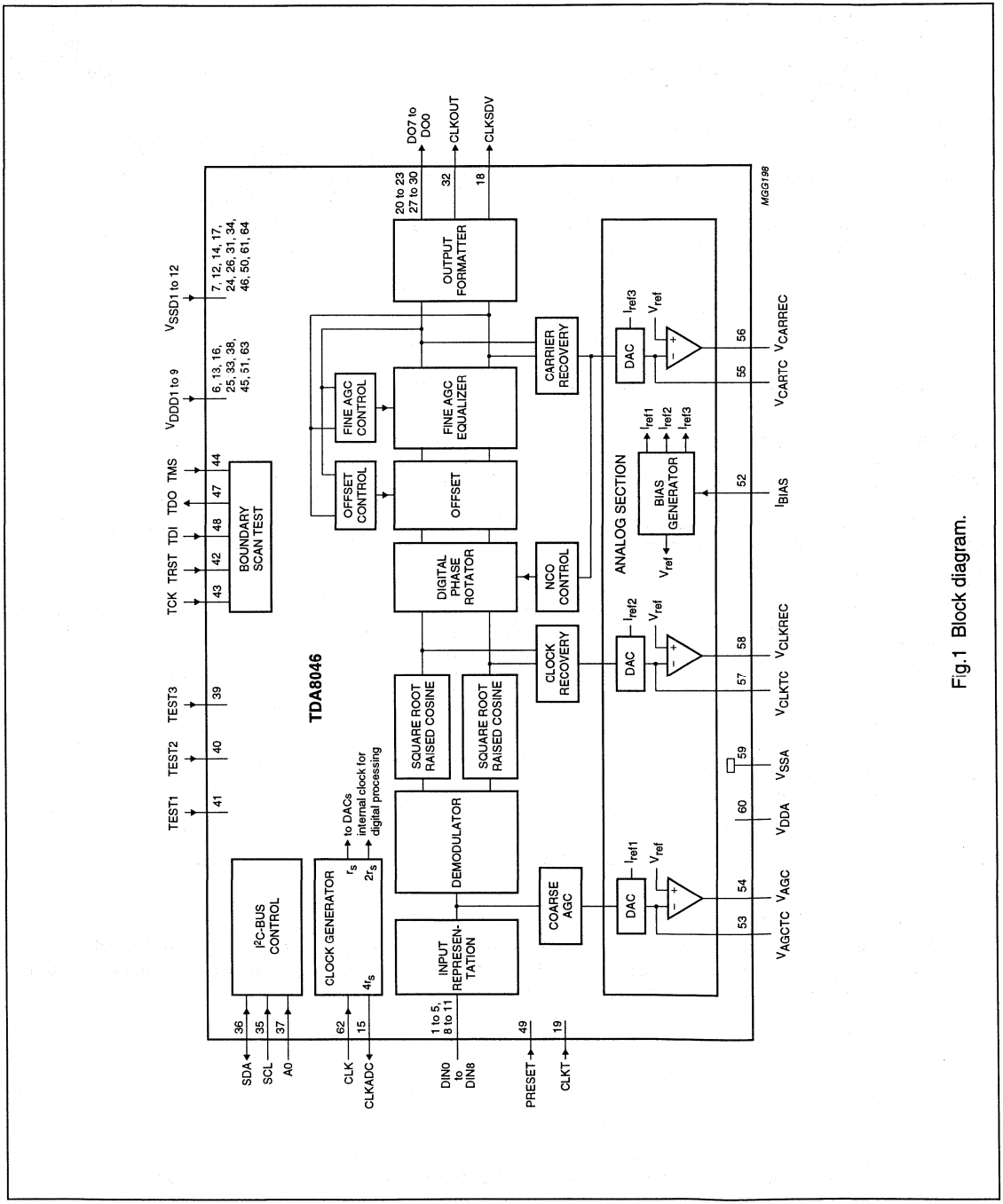


Fig.1 Block diagram.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8046H	QFP64	plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT319-2

PINNING

SYMBOL	PIN	I/O	DESCRIPTION
DIN0	1	I	digital input bit 0 (LSB)
DIN1	2	I	digital input bit 1
DIN2	3	I	digital input bit 2
DIN3	4	I	digital input bit 3
DIN4	5	I	digital input bit 4
V_{DDD1}	6	supply	digital peripheral supply voltage 1 (+5 V)
V_{SSD1}	7	supply	digital ground 1; for input peripheral and core
DIN5	8	I	digital input bit 5
DIN6	9	I	digital input bit 6
DIN7	10	I	digital input bit 7
DIN8	11	I	digital input bit 8 (MSB)
V_{SSD2}	12	supply	digital ground 2; for core and clock buffers
V_{DDD2}	13	supply	digital supply voltage 2; for core and clock buffers (+3.3 V)
V_{SSD3}	14	supply	digital peripheral ground 3
CLKADC	15	O	clock output to ADC ($4 \times r_s$)
V_{DDD3}	16	supply	digital peripheral supply voltage 3 (+5 V)
V_{SSD4}	17	supply	digital ground 4; for core
CLKSDV	18	O	clock symbol data valid output
CLKT	19	I	for test purpose only
DO7	20	O	parallel data output (bit 7)
DO6	21	O	parallel data output (bit 6)
DO5	22	O	parallel data output (bit 5)
DO4	23	O	parallel data output (bit 4)
V_{SSD5}	24	supply	digital peripheral ground 5
V_{DDD4}	25	supply	digital peripheral supply voltage 4 (+5 V)
V_{SSD6}	26	supply	digital ground 6; for core
DO3	27	O	parallel data output (bit 3)
DO2	28	O	parallel data output (bit 2)
DO1	29	O	parallel data output (bit 1)
DO0	30	O	parallel data output (bit 0)
V_{SSD7}	31	supply	digital peripheral ground 7
CLKOUT	32	I	output formatter clock output
V_{DDD5}	33	supply	digital peripheral supply voltage 5 (+5 V)

SYMBOL	PIN	I/O	DESCRIPTION
V_{SSD8}	34	supply	digital peripheral ground 8
SCL	35	I	serial clock input (I^2C-bus)
SDA	36	I/O	serial data input/output (I^2C-bus)
A0	37	I	hardware address input (I^2C-bus)
V_{DDD6}	38	supply	digital peripheral supply voltage 6 (+5 V)
TEST3	39	I	test input 3 (normally connected to ground)
TEST2	40	I	test input 2 (normally connected to ground)
TEST1	41	I	test input 1 input (normally connected to ground)
TRST	42	I	optional asynchronous reset input
TCK	43	I	dedicated test clock input
TMS	44	I	input control signal
V_{DDD7}	45	supply	digital supply voltage 7; for core (+3.3 V)
V_{SSD9}	46	supply	digital ground 9; for core
TDO	47	O	serial test data output
TDI	48	I	serial test data input
PRESET	49	I	set device into default mode input
V_{SSD10}	50	supply	digital ground 10; for the digital section of the analog block
V_{DDD8}	51	supply	digital supply voltage 8; for the digital section of the analog block (+5 V)
I_{BIAS}	52	I	input bias current for DACs
V_{AGCTC}	53	O	inverted operational amplifier input voltage for loop filtering
V_{AGC}	54	O	analog output voltage for AGC
V_{CARTC}	55	O	inverted operational amplifier input voltage for carrier recovery loop filtering
V_{CARREC}	56	O	analog output voltage for carrier recovery
V_{CLKTC}	57	O	inverted operational amplifier input voltage for clock recovery loop filtering
V_{CLKREC}	58	O	analog output voltage for clock recovery
V_{SSA}	59	supply	analog ground
V_{DDA}	60	supply	analog supply voltage (+5 V)
V_{SSD11}	61	supply	digital ground 11; for clock
CLK	62	I	clock input ($4 \times r_s$)
V_{DDD9}	63	supply	digital supply voltage 9; for clock
V_{SSD12}	64	supply	digital peripheral ground 12

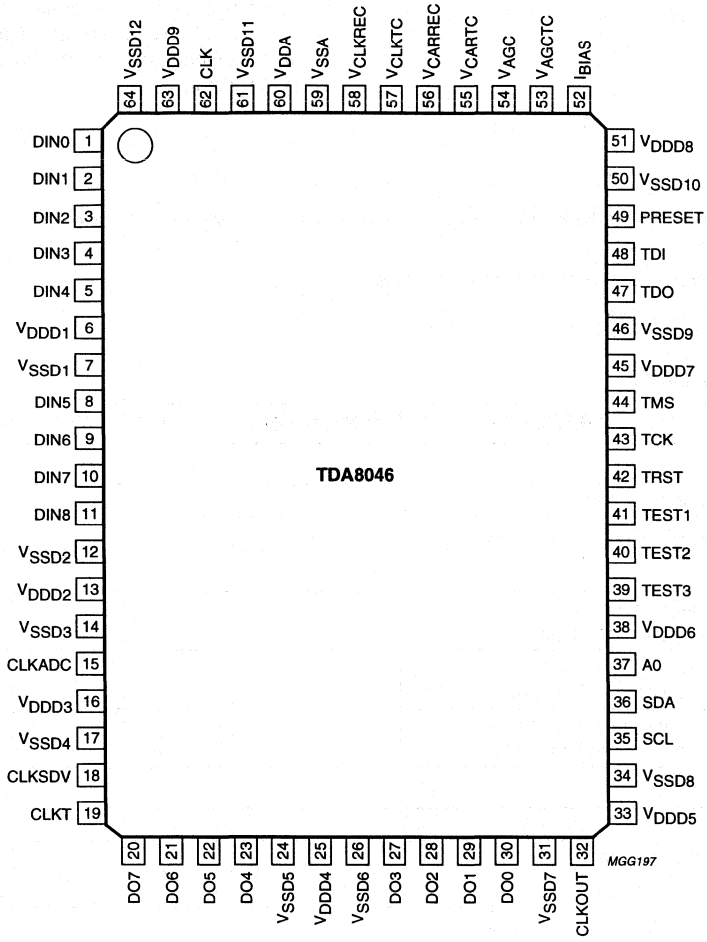


Fig.2 Pin configuration.

DC coupled vertical deflection circuit TDA8351

FEATURES

- Few external components
- Highly efficient fully DC-coupled vertical output bridge circuit
- Vertical flyback switch
- Guard circuit
- Protection against:
  - short-circuit of the output pins (7 and 4)
  - short-circuit of the output pins to V_P
- Temperature (thermal) protection
- High EMC immunity because of common mode inputs
- A guard signal in zoom mode.

GENERAL DESCRIPTION

The TDA8351 is a power circuit for use in 90° and 110° colour deflection systems for field frequencies of 50 to 120 Hz. The circuit provides a DC driven vertical deflection output circuit, operating as a highly efficient class G system.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DC supply						
V_P	supply voltage		9	–	25	V
I_q	quiescent supply current		–	30	–	mA
Vertical circuit						
$I_{O(p-p)}$	output current (peak-to-peak value)		–	–	3	A
$I_{diff(p-p)}$	differential input current (peak-to-peak value)		–	600	–	μA
$V_{diff(p-p)}$	differential input voltage (peak-to-peak value)		–	1.5	1.8	V
Flyback switch						
I_M	peak output current		–	–	±1.5	A
V_{FB}	flyback supply voltage		–	–	50	V
		note 1	–	–	60	V
Thermal data (in accordance with IEC 747-1)						
T_{stg}	storage temperature		–55	–	+150	°C
T_{amb}	operating ambient temperature		–25	–	+75	°C
T_{vj}	virtual junction temperature		–	–	150	°C

Note

1. A flyback supply voltage of >50 V up to 60 V is allowed in application. A 220 nF capacitor in series with a 22 Ω resistor (dependent on I_O and the inductance of the coil) has to be connected between pin 7 and ground. The decoupling capacitor of V_{FB} has to be connected between pin 6 and pin 3. This supply voltage line must have a resistance of 33 Ω.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8351	SIL9P	plastic single-in-line power package; 9 leads	SOT131-2

BLOCK DIAGRAM

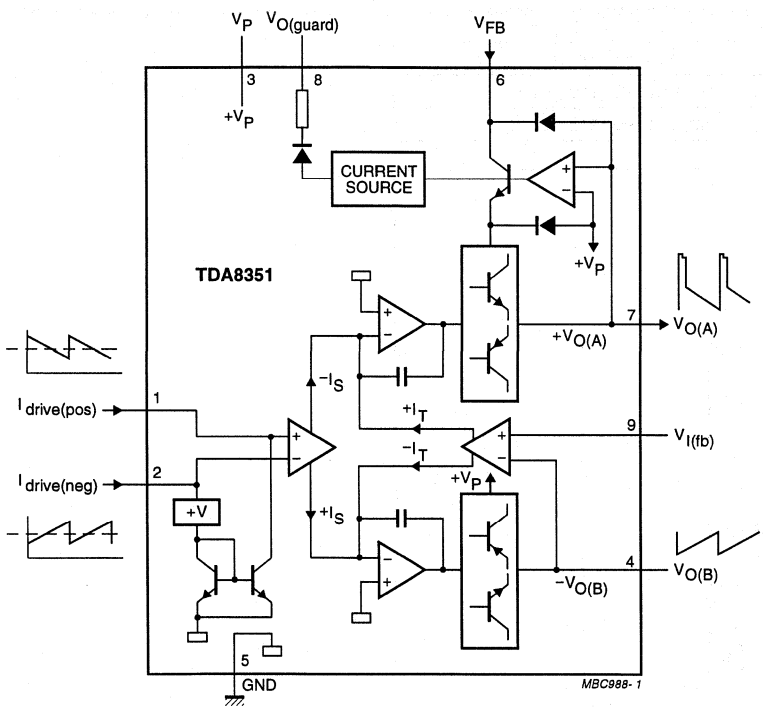
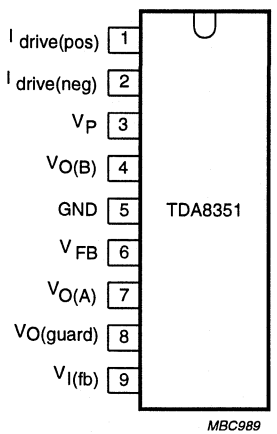


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$I_{drive(pos)}$	1	input power-stage (positive); includes $I_{I(sb)}$ signal bias
$I_{drive(neg)}$	2	input power-stage (negative); includes $I_{I(sb)}$ signal bias
V_P	3	operating supply voltage
$V_{O(B)}$	4	output voltage B
GND	5	ground
V_{FB}	6	input flyback supply voltage
$V_{O(A)}$	7	output voltage A
$V_{O(guard)}$	8	guard output voltage
$V_{I(fb)}$	9	input feedback voltage



Metal block connected to substrate pin 5.
Metal on back.

Fig.2 Pin configuration.

Octuple 6-bit DAC with I²C-bus

TDA8444

GENERAL DESCRIPTION

The TDA8444 comprises eight digital-to-analogue converters (DACs) each controlled via the two-wire I²C-bus. The DACs are individually programmed using a 6-bit word to select an output from one of 64 voltage steps. The maximum output voltage of all DACs is set by the input V_{max} and the resolution is approximately $V_{max}/64$.

At power-on all DAC outputs are set to their lowest value. The I²C-bus slave receiver has a 7-bit address of which 3 bits are programmable via pins A0, A1 and A2.

Features

- Eight discrete DACs
- I²C-bus slave receiver
- 16-pin DIL package.

QUICK REFERENCE DATA

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage		V_P	10.8	12.0	13.2	V
Supply current	no loads; $V_{max} = V_P$; all data = 00	I_{CC}	8	12	15	mA
Total power dissipation	no loads; $V_{max} = V_P$; all data = 00	P_{tot}	–	150	–	mW
Effective range of V_{max} input	V_P = 12 V	V_{max}	1	–	10.5	V
DAC output voltage range		V_O	0.1	–	V_P–0.5	V
Step value of 1 LSB	$V_{max} = V_P$; I_O = –2 mA	V_{LSB}	70	160	250	mV

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38); SOT38-1; 1996 July 23.

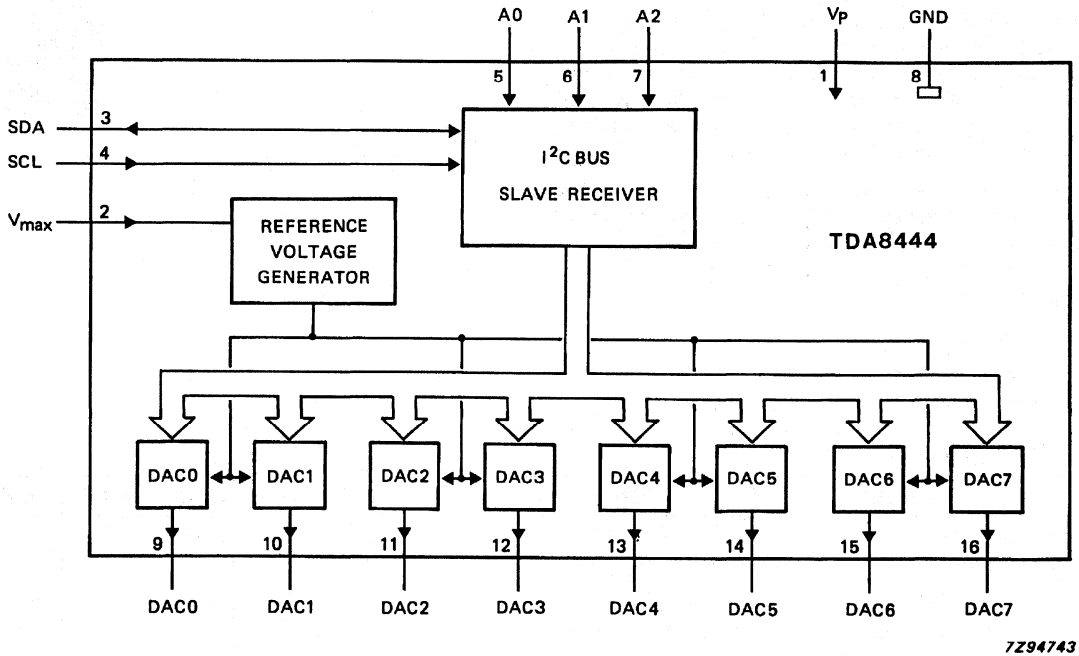


Fig.1 Block diagram.

PINNING

PIN	SYMBOL	DESCRIPTION
1	V_P	positive supply voltage
2	V_{max}	control input for DAC maximum output voltage
3	SDA	I²C-bus serial data input/output
4	SCL	I²C-bus serial data clock
5	A0	programmable address bits for I²C-bus slave receiver
6	A1	
7	A2	
8	GND	ground
9-16	DAC0-7	analogue voltage outputs

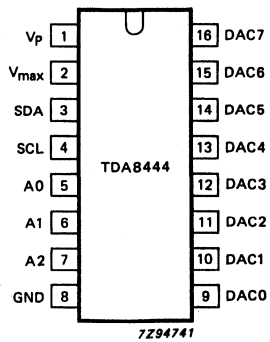


Fig.2 Pinning diagram

FUNCTIONAL DESCRIPTION

I²C-bus

The TDA8444 I2C-bus interface is a receive-only slave. Data is accepted from the I2C-bus in the following format:

S	0 1 0 0 A2 A1 A0 0	A	I3 I2 I1 I0 SD SC SB SA	A	X X D5 D4 D3 D2 D1 D0	A	P
	<----- address byte ---->		<----- instruction byte ---->		<----- first data byte ---->		

Where:

S = start condition
P = stop condition
A = acknowledge
X = don't care
A2, A1, A0 = programmable address bits
I3, I2, I1, I0 = instruction bits
SD, SC, SB, SA = subaddress bits
D5, D4, D3, D2, D1, D0 = data bits

Fig.3 Data format.

Address byte

Valid addresses are 40, 42, 44, 46, 48, 4A, 4C, 4E (hexadec), depending on the programming of bits A2, A1 and A0. With these addresses, up to eight TDA8444 ICs can be operated independently from one I²C-bus. No other addresses are acknowledged by the TDA8444.

Instruction and data bytes

Valid instructions are 00 to 0F and F0 to FF (hexadec); the TDA8444 will not respond to other instruction values.

Instructions 00 to 0F cause auto-incrementing of the subaddress (bits SD to SA) when more than one data byte is sent within one transmission. With auto-incrementing, the first data byte is written into the DAC addressed by bits SD to SA and then the subaddress is automatically incremented by one position for the next data byte in the series.

Auto-incrementation does not occur with instructions F0 to FF. Other than auto-incrementation there is no difference between instructions 00 to 0F and F0 to FF. When only one data byte per transmission is present, the DAC addressed by the subaddress will always receive the data.

Valid subaddresses (bits SD to SA) are 0 to 7 (hexadec) relating numerically to DAC0 to DAC7. When the auto-incrementing function is used, the subaddress will sequence through all possible values (0 to F, 0 to F, etc.).

I²C-bus

Input SCL (pin 3) and input/output SDA (pin 4) conform to I²C-bus specifications. Pins 3 and 4 are protected against positive voltage pulses by internal zener diodes connected to the ground plane and therefore the normal bus line voltage should not exceed 5.5 V.

The address inputs A0, A1, A2 are programmed by a connection to GND for An = 0 or to V_P for An = 1. If the inputs are left floating, An = 1 will result.

Input V_{max}

Input V_{max} (pin 2) provides a means of compressing the output voltage swing of the DACs. The maximum DAC output voltage is restricted to approximately V_{max} while the 6-bit resolution is maintained, so giving a finer voltage resolution of smaller output swings.

Digital-to-analogue converters

Each DAC comprises a 6-bit data latch, current switches and an output driver. Current sources with values weighted by 2^0 up to 2^5 are switched according to the data input so that the sum of the selected currents gives the required analogue voltage from the output driver. The range of the output voltage is approximately 0.5 to 10.5 V when $V_{max} = V_P$.

The DAC outputs are protected against short-circuits to V_P and GND.

To avoid the possibility of oscillations, capacitive loading at the DAC outputs should not exceed 2 nF.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Supply voltage	$V_P = V_1$	−0.5	18	V
Supply current (source)	$I_P = I_1$	−	−10	mA
	$I_P = I_I$	−	40	mA
I2C-bus line voltage	$V_{3,4}$	−0.5	5.9	V
Input voltage	V_I	−0.5	$V_P + 0.5$	V
Output voltage	V_O	−0.5	$V_P + 0.5$	V
Maximum current on any pin (except pins 1 and 8)	$\pm I_{max}$	−	10	mA
Total power dissipation	P_{tot}	−	500	mW
Operating ambient temperature range	T_{amb}	−20	+70	°C
Storage temperature range	T_{stg}	−55	+150	°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	75	K/W

CHARACTERISTICS

All voltages are with respect to GND; T_{amb} = 25 °C; V_P = 12 V unless otherwise specified

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage		V_P	10.8	12.0	13.2	V
Voltage level for power-on reset		V_1	1	–	4.8	V
Supply current	no loads; $V_{max} = V_P$; all data = 00	$I_P = I_1$	8	12	15	mA
Total power dissipation	no loads; $V_{max} = V_P$; all data = 00	P_{tot}	–	150	–	mW
Effective range of V_{max} input (pin 2)	V_P = 12 V	$V_{max} = V_2$	1.0	–	10.5	V
Pin 2 current	V_2 = 1 V	I_2	–	–	–10	µA
	V_2 = VP	I_2	–	–	10	µA
SDA, SCL inputs (pins 3 and 4)						
Input voltage range		V_I	0	–	5.5	V
Input voltage LOW		V_{IL}	–	–	1.5	V
Input voltage HIGH		V_{IH}	3.0	–	–	V
Input current LOW	$V_{3;4}$ = 0.3 V	I_{IL}	–	–	–10	µA
Input current HIGH	$V_{3;4}$ = 6 V	I_{IH}	–	–	±10	µA
SDA output (pin 3)						
Output voltage LOW	I_3 = 3 mA	V_{OL}	–	–	0.4	V
Sink current		I_{OL}	3	8	–	mA
Address inputs (pins 5 to 7)						
Input voltage range		V_I	0		5	V
Input voltage LOW		V_{IL}	–	–	1	V
Input voltage HIGH		V_{IH}	2.1	–	–	V
Input current LOW		I_{IL}	–	–7	–12	µA
Input current HIGH		I_{IH}	–	–	1	µA

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
DAC outputs (pins 9 to 16)						
Output voltage range		V_O	0.1	–	$V_P - 0.5$	V
Minimum output voltage	data = 00; I_O = –2 mA	VOmin	0.1	0.4	0.8	V
Maximum output voltage	data = 3F; I_O = –2 mA					
at Vmax = VP		V_{Omax}	10	10.5	11.5	V
at 1 < Vmax < 10.5 V		V_{Omax}		see note 1		V
Output sink current	V = V_P; data = 1F	I_O	2	8	15	mA
Output source current	V = 0 V; data = 1F	I_O	–2	–	–6	mA
Output impedance	data = 1F; -2 < I_O < +2 mA	Z_O	–	4	50	Ω
Step value of 1 LSB	$V_{max} = V_P$; I_O = -2 mA	V_{LSB}	70	160	250	mV
Deviation from linearity	I_O = -2 mA; N ≠ 32		0	–	50	mV
Deviation from linearity	I_O = -2 mA; N = 32		0	–	70	mV

Note to the Characteristics

1. $V_O = 0.95\ V_{max} + V_{Omin}$.

APPLICATION INFORMATION

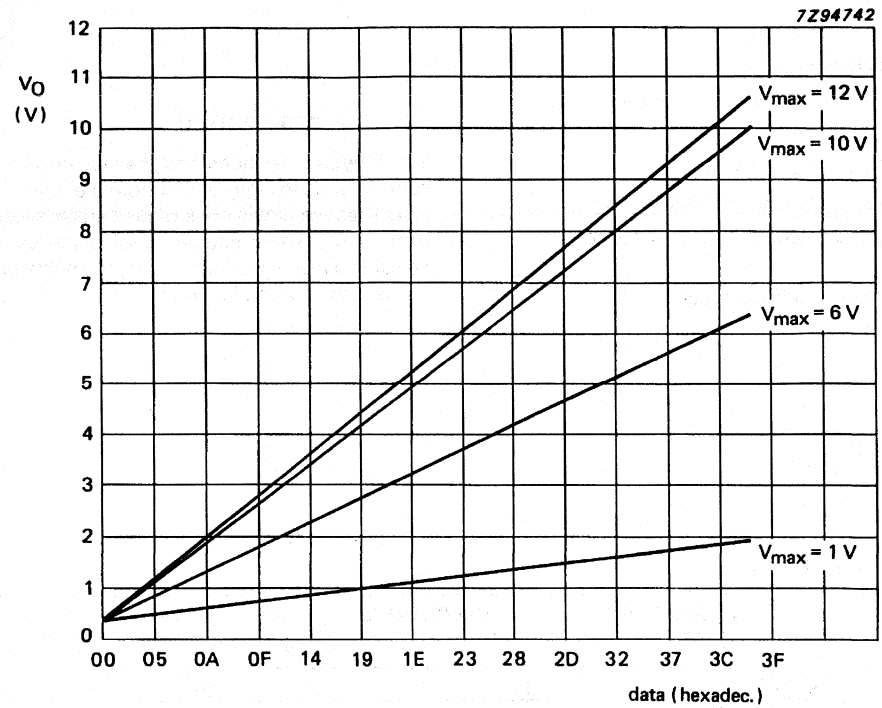


Fig.4 Graph showing output voltage as a function of the input data value for V_{max} values of 1, 6, 10 and 12 V; V_P = 12 V.

4 × 4 video switch matrix TDA8540

FEATURES

- I²C-bus or non-I²C-bus mode (controlled by DC voltages)
- S-VHS or CVBS processing
- 3-state switches for all channels
- Selectable gain for the video channels
- sub-address facility
- Slave receiver in the I²C mode
- Auxiliary logic outputs for audio switching
- System expansion possible up to 7 devices (28 sources)
- Static short-circuit proof outputs
- ESD protection.

APPLICATIONS

- Colour Television (CTV) receivers
- Peritelevision sets
- Satellite receivers.

GENERAL DESCRIPTION

The TDA8540 has been designed for switching between composite video signals, therefore the minimum of four input lines are provided as requested for switching between two S-VHS sources. Each of the four outputs can be set to a high impedance state, to enable parallel connection of several devices.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		7.2	–	8.8	V
I_{CC}	supply current		–	20	30	mA
I_{SO}	isolation 'OFF' state	at f = 5 MHz	60	80	–	dB
B	3 dB bandwidth		12	–	–	MHz
α_{ct}	crosstalk attenuation between channels		60	70	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8540	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
TDA8540T	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

BLOCK DIAGRAM

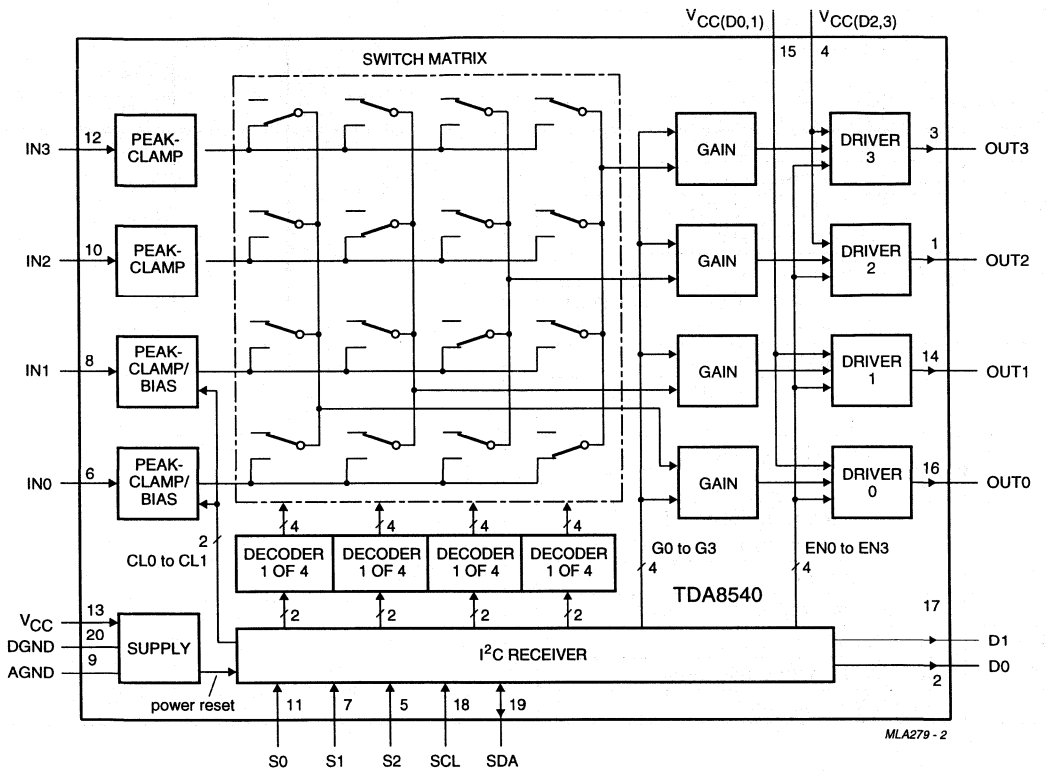


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
OUT2	1	video output 2
D0	2	control output 0
OUT3	3	video output 3
$V_{CC(D2,3)}$	4	driver supply voltage; for drivers 2 and 3
S2	5	sub-address input 2
IN0	6	video input 0 (CVBS or chrominance signal)
S1	7	sub-address input 1
IN1	8	video input 1 (CVBS or chrominance signal)
AGND	9	analog ground
IN2	10	video input 2 (CVBS or luminance signal)
S0	11	sub-address input 0
IN3	12	video input 3 (CVBS or luminance signal)
V_{CC}	13	general supply voltage
OUT1	14	video output 1
$V_{CC(D0,1)}$	15	driver supply voltage; for drivers 0 and 1
OUT0	16	video output 0
D1	17	control output 1
SCL	18	serial clock input
SDA	19	serial data input/output
DGND	20	digital ground

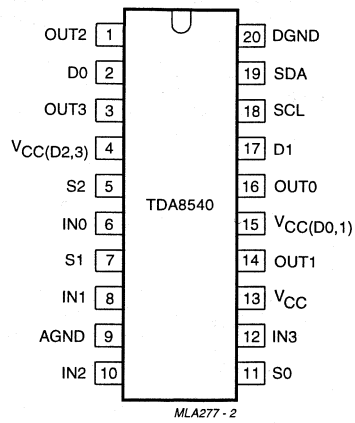


Fig.2 Pinning configuration.

FUNCTIONAL DESCRIPTION

The TDA8540 is controlled via a bidirectional I²C-bus. 3 bits of the I²C address can be selected via the address pin, thus providing a facility for parallel connection of 7 devices.

Control options via the I²C-bus:

- The input signals can be clamped at their negative peak (top sync).
- The gain factor of the outputs can be selected between 1× or 2×.
- Each of the four outputs can individually be connected to one of the four inputs.
- Each output can individually be set in a high impedance state.
- Two binary output data lines can be controlled for switching accompanying sound signals.

The SDA and SCL pins (pins 19 and 18) can be connected to the I²C-bus or to DC switching voltage sources. Address inputs S0 to S2 (pins 11, 7 and 5) are used to select sub-addresses or switching to the non-I²C mode. Inputs S0 to S2 can be connected to the supply voltage (HIGH) or the ground (LOW). In this way no peripheral components are required for selection.

Table 1 I²C-bus sub-addressing

S2	S1	S0	SUB-ADDRESS		
			A2	A1	A0
L	L	L	0	0	0
L	L	H	0	0	1
L	H	L	0	1	0
L	H	H	0	1	1
H	L	L	1	0	0
H	L	H	1	0	1
H	H	L	1	1	0
H	H	H	non I²C addressable		

I²C-bus control

After power-up the outputs are initialized in the high impedance state, and D0 and D1 are at a LOW level.

Detailed description of the I²C-bus specification, with applications, is given in brochure *"The I²C-bus and how to use it"*. This brochure may be ordered using the code 9398 393 40011.

The TDA8540 is a **slave receiver** and the protocol is given in Table 2.

Table 2 The TDA8540 protocol

SEQUENCE									
S[1]	SLV[2]	A[3]	SUB	A[3]	DATA	A[3]	DATA	A[3]	P[4]

Notes

1. S = START condition.
2. Data transmission to the TDA8540 starts with the slave address (SLV).
3. A = acknowledge bit, generated by TDA8540.
4. P = STOP condition.

Table 3 Data transmission to the TDA8540 begins with SLV

A6 MSB	A5	A4	A3	A2	A1	A0	R/$\overline{W}$ LSB
1	0	0	1	A2[1]	A1[1]	A0[1]	0[2]

Notes

1. A2 to A0: pin programmable slave address bits.
2. R/$\overline{W}$ = 0; write only.

After the SLV, a second byte, SUB, is required for selecting the functions, as shown in Table 4.

Table 4 The second byte: SUB

7 MSB	6	5	4	3	2	1	0 LSB
0	0	0	0	0	0	RS1	RS0

Options for SUB:

If SUB = 00H: access to switch control (SW1)

If SUB = 01H: access to gain/clamp/data control (GCO)

If SUB = 02H: access to output enable control (OEN).

Remarks:

If more than one data byte is sent, the SUB byte will be automatically incremented.

If more than 3 data bytes are sent, the internal counter will roll over and the device will then rewrite the first register.

Data Bytes

SWI (SUB = 00H): selects which input is connected to the different outputs, as shown in Table 5.

Table 5 SWI (SUB = 00H) selection of inputs connected to outputs

7 MSB	6	5	4	3	2	1	0 LSB
S31	S30	S21	S20	S11	S10	S01	S00

Table 6 Selection of inputs

OUTPUT	Sj1 AND Sj0[1]			
	00	01	10	11
OUTj	IN0	IN1	IN2	IN3

Note

1. For j = 0 to 3.
   Example: if S21 = 0 and S20 = 1, then OUT2 is connected to IN1.

GCO (SUB = 01H):

- Selects the gain of each output.
- Selects the clamp action or mean value on inputs 0 and 1.
- Determines the value of the auxiliary outputs D1 and D0.

Table 7 GCO byte

7 MSB	6	5	4	3	2	1	0 LSB
G3[1]	G2[1]	G1[1]	G0[1]	CL1[2]	CL0[2]	D1[3]	D0[3]

Notes

1. For j = 0 to 3: if Gj = 0 (1), then output j has a gain of 2 (1).
2. If CL0 (CL1) = 0, then input signal on IN0 (IN1) is clamped.
3. For j = 0 or 1: if Dj = 0 (1), then logical output j is LOW (HIGH).

OEN (SUB = 02H): selects, for each output, if the output is active or high impedance, see Table 8.

Table 8 OEN (SUB = 02H) determines which output is active or high impedance

7 MSB	6	5	4	3	2	1	0 LSB
X(1)	X(1)	X(1)	X(1)	EN3(2)	EN2(2)	EN1(2)	EN0(2)

Notes

1. X = don't care.
2. For j = 0 to 3: if ENj = 0 (1), then OUT j is high impedance (active).

After a power-on reset:

- The outputs are set to a high impedance state; the outputs are connected to IN0; the gains are set at two and inputs IN0 and IN1 are clamped.
- Programming of the device is necessary because the outputs are in high impedance state.

Non-I²C-bus control

If the S0, S1 and S2 pins are all connected to V_{CC} the device will enter the non-I²C-bus mode.

After a power-on reset:

- Gain is set at two for all outputs.
- All inputs are clamped.
- All outputs are active.
- The matrix position is given by the SDA and SCL voltage level.

Table 9 Non-I²C-bus control

OUTPUT	SCL AND SDA			
	00	01	10	11
OUT3	IN3	IN2	IN1	IN0
OUT2	IN2	IN3	IN0	IN1
OUT1	IN1	IN0	IN3	IN2
OUT0	IN0	IN1	IN2	IN3

SCL and SDA act as normal input pins:

SCL interchanges (OUT3 and OUT2) with (OUT1 and OUT0).

SDA interchanges OUT3 with OUT2 and OUT1 with OUT0.

Remark: For use with chrominance signals, the clamp action must be overruled by external bias.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage (pin 13)		−0.3	+9.1	V
P_{tot}	total power dissipation		–	750	mW
$V_{CC(D0,1)}$, $V_{CC(D2,3)}$	driver supply voltage		−0.3	+13.8	V
IN0 to IN3	video input voltage		−0.3	+7.2	V
OUT0 to OUT3	video output voltage		−0.3	+7.2	V
D0, D1	control output voltage		−0.3	+7.2	V
SDA, SDL	I^2C input/output voltage		−0.3	+8.8	V
S0 to S2	sub-address input voltage		−0.3	+8.8	V
T_{stg}	IC storage temperature		−55	+125	°C
T_j	junction temperature		–	+150	°C
V_{es}	electrostatic handling	HBM; note 1	−1500	+1500	V
		MM; note 2	−200	+200	V

Notes

1. Human Body Model (HBM): in accordance with UZW-BO/FQ-A302.
2. Machine Model (MM): in accordance with UZW-BO/FQ-B302 (stress reference pins: AGND and DGND short-circuited and V_{CC}).

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	SOT146-1	60 (typ.)	K/W
	SOT163-1	85 (typ.)	K/W

OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
General						
V_{CC}	supply voltage (pin 13)		7.2	–	8.8	V
T_{amb}	operating ambient temperature		0	–	70	°C
Video inputs (pins 6, 8, 10 and 12)						
C_I	external capacitor		–	100	–	nF
$V_{I(p\text{-}p)}$	C signal amplitude (peak-to-peak value)	note 1	–	–	1	V
$V_{I(p\text{-}p)}$	CVBS or Y-signal amplitude (peak-to-peak value)	note 2	–	–	1.5	V
Video drivers (pins 4 and 15)						
R_D	external collector resistor	note 3	–	25	–	Ω
C_D	external decoupling capacitor	note 4	–	22	–	µF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Sub-address S0, S1 and S2 (pins 5, 7 and 11)						
V_{IH}	HIGH level input voltage		4	–	V_{CC}	V
V_{IL}	LOW level input voltage		0	–	1	V

Notes

1. Only for pins 6 and 8 when clamp action is not selected for these pins.
2. On all the video input pins, when non-I²C-bus control mode is selected or when clamp action is selected on pins 6 and 8 (by I²C-bus control).
3. Connected between V_{CC} and pin 4 or pin 15.
4. Connected between AGND and pin 4 or pin 15.

CHARACTERISTICS

V_{CC} = 8 V; T_{amb} = 25 °C; gain condition, clamp condition and OFF state are controlled by the I²C-bus; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
I_{CC}	supply current	without load	–	20	30	mA
		OFF state	–	12	–	mA
Video inputs: IN0 to IN3 when the clamp is active (see Figs 3 and 4)						
I_{LI}	input leakage current	V_I = 3 V	–	0.4	1	µA
V_{clamp}	input clamping voltage	I_I = 5 µA	–	2.2	–	V
I_{clamp}	input clamping current	V_I = 0 V	1.2	–	–	mA
Video inputs: IN0 and IN2 when the clamp is not active (see Fig.3)						
V_{bias}	DC input bias level	I_I = 0	–	2.9	–	V
R_I	input resistance		–	10	–	kΩ
Video outputs: OUT0 to OUT3 (see Fig.5)						
Z_O	output impedance	OFF state	100	–	–	kΩ
R_O	output resistance		–	5	–	Ω
ISO	isolation	OFF state; f = 5 MHz	60	–	–	dB
V_O	output top sync level; (Y or CVBS)		0.4	0.7	1	V
V_{bias}	output mean value for chrominance signals	G = 2; load = 150 Ω	1.5	1.9	2.2	V
		G = 1; without load	1	1.3	1.6	V
G_v	voltage gain	G = 1; f = 1 MHz	−1	0	+1	dB
		G = 2; f = 1 MHz	5	6	7	dB
G_{diff}	differential gain	note 1	–	0.5	3	%
φ_{diff}	differential phase	note 1	–	0.6	–	deg
NL	non linearity	note 2	–	0.5	2	%
α_{ct}	crosstalk attenuation between channels	note 3	60	70	–	dB
SVRR	supply voltage rejection	note 4	36	55	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ΔG	maximum gain variation	100 kHz < f < 5 MHz	–	0.5	–	dB
		100 kHz < f < 8.5 MHz	–	1	–	dB
		100 kHz < f < 12 MHz	–	3	–	dB
α_{ct}	crosstalk attenuation of I²C-bus signals		60	–	–	dB
Auxiliary outputs D0 and D1 (open collector)						
I_{OH}	HIGH level output current	V_{OH} = 5.5 V	–	–	10	μA
V_{OL}	LOW level output voltage	I_{OL} = 4 mA	–	–	0.4	V
I²C-bus inputs SCL and SDA						
I_{IH}	HIGH level input current	V_{IH} = 3.0 V	–	–	10	μA
I_{IL}	LOW level input current	V_{IL} = 1.5 V	−10	–	–	μA
C_i	input capacitance		–	–	10	pF
I²C-bus output SDA						
V_{OL}	LOW level output voltage	I_{OL} = 3 mA	–	–	0.4	V
Sub-address S0, S1 and S2						
I_{IH}	HIGH level input current	$V_{IH} = V_{CC}$	–	–	10	μA
I_{IL}	LOW level input current	V_{IL} = 0 V	–	–	10	μA

Notes

1. Gain set at 2; R_L = 150 Ω; test signal D2 from CCIR 330.
2. Gain set at 2; R_L = 150 Ω; test signal D1 from CCIR 17.
3. Measured from any selected input to output; f = 5 MHz; R_L = 150 Ω; gain set at 2; V_I = 1.5 V (peak-to-peak value). This measurement requires an optimized board.
4. Supply voltage ripple rejection: $20 \log \frac{V_{ripple\ (supply)}}{V_{ripple\ (on\ output)}}$;
   measured at f = 1 kHz with $V_{ripple\ (supply\ max)}$ = 100 mV (peak-to-peak value).
   The supply voltage rejection ratio is >36 dB at f_{max} = 100 kHz.

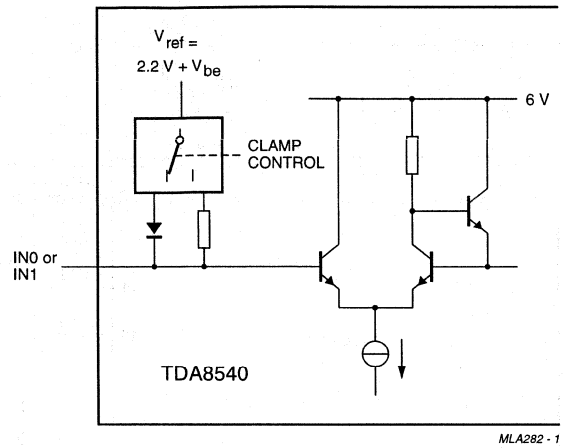


Fig.3 IN0 and IN1 inputs.

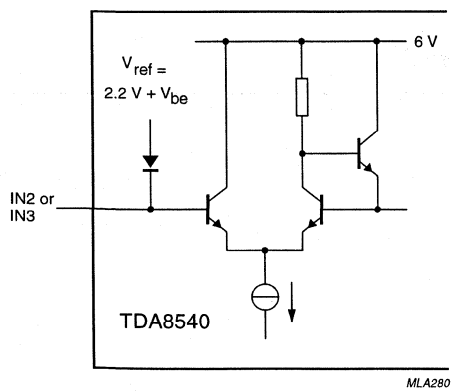


Fig.4 IN2 and IN3 inputs.

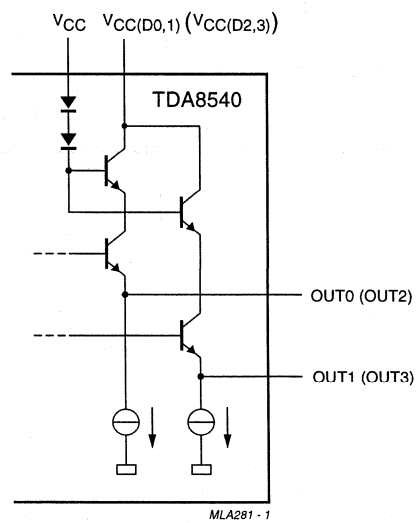
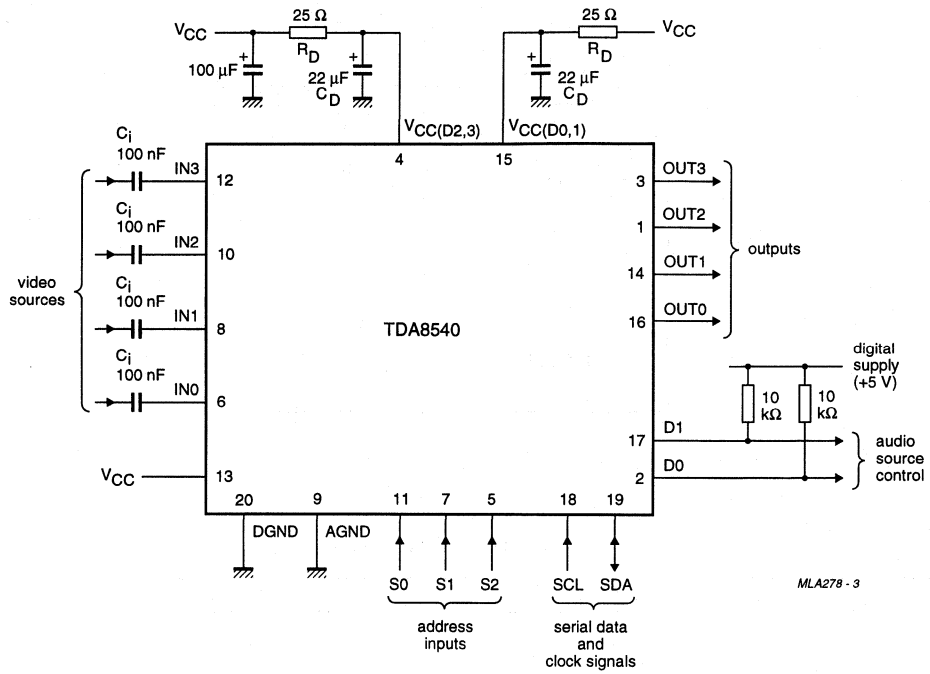


Fig.5 Driver output stage.

APPLICATION INFORMATION



V_{CC} = analog supply (+8 V).

Fig.6 Application diagram.

2 × 1 W BTL audio amplifier TDA8542

FEATURES

- Flexibility in use
- Few external components
- Low saturation voltage of output stage
- Gain can be fixed with external resistors
- Standby mode controlled by CMOS compatible levels
- Low standby current
- No switch-on/switch-off plops
- High supply voltage ripple rejection
- Protected against electrostatic discharge
- Outputs short-circuit safe to ground, V_{CC} and across the load
- Thermally protected.

GENERAL DESCRIPTION

The TDA8542(T) is a two channel audio power amplifier for an output power of 2 × 1 W with an 8 Ω load at a 5 V supply. The circuit contains two BTL amplifiers with a complementary PNP-NPN output stage and standby/mute logic. The TDA8542T comes in a 16 pin SO package and the TDA8542 in a 16 pin DIP package.

APPLICATIONS

- Portable consumer products
- Personal computers
- Motor-driver (servo).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		2.2	5	18	V
I_q	quiescent current	V_{CC} = 5 V	–	15	22	mA
I_{stb}	standby current		–	–	10	μA
P_o	output power	THD = 10%; R_L = 8 Ω; V_{CC} = 5 V	1	–	–	W
THD	total harmonic distortion	P_o = 0.5 W	–	0.15	–	%
SVRR	supply voltage ripple rejection		50	–	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8542T	SO16L	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1
TDA8541	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1

BLOCK DIAGRAM

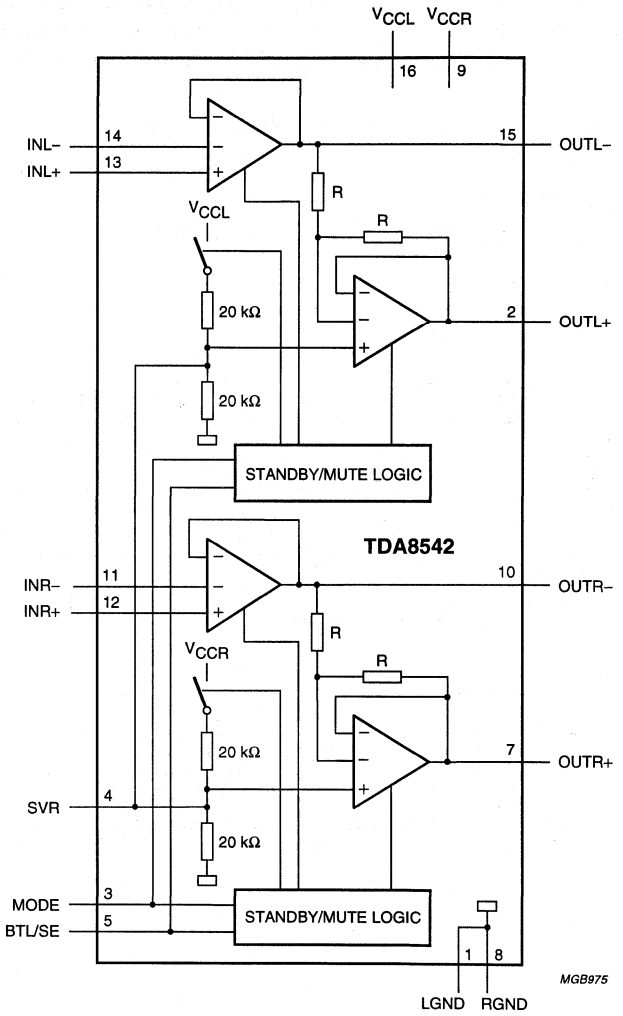


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
LGND	1	ground, left channel
OUTL+	2	positive loudspeaker terminal, left channel
MODE	3	operating mode select (standby, mute, operating)
SVR	4	half supply voltage, decoupling ripple rejection
BTL/SE	5	BTL loudspeaker or SE headphone operation
n.c.	6	not connected
OUTR+	7	positive loudspeaker terminal, right channel
RGND	8	ground, right channel
V_{CCR}	9	supply voltage, right channel
OUTR–	10	negative loudspeaker terminal, right channel
INR–	11	negative input, right channel
INR+	12	positive input, right channel
INL+	13	positive input, left channel
INL–	14	negative input, left channel
OUTL–	15	negative loudspeaker terminal, left channel
V_{CCL}	16	supply voltage, left channel

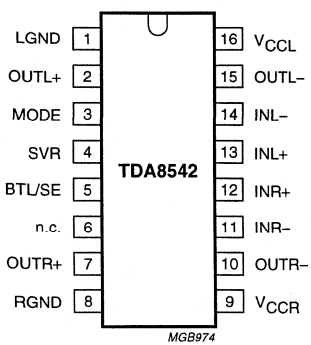


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA8542(T) is a 2 × 1 W BTL audio power amplifier capable of delivering 2 × 1 W output power to an 8 Ω load at THD = 10% using a 5 V power supply. Using the MODE pin the device can be switched to standby and mute condition. The device is protected by an internal thermal shutdown protection mechanism. The gain can be set within a range from 6 dB to 30 dB by external feedback resistors.

Power amplifier

The power amplifier is a Bridge Tied Load (BTL) amplifier with a complementary PNP-NPN output stage. The voltage loss on the positive supply line is the saturation voltage of a PNP power transistor, on the negative side the saturation voltage of a NPN power transistor. The total voltage loss is <1 V and with a 5 V supply voltage and an 8 Ω loudspeaker an output power of 1 W can be delivered.

Mode select pin

The device is in the standby mode (with a very low current consumption) if the voltage at the MODE pin is >(V_{CC} – 0.5 V), or if this pin is floating. At a MODE voltage level of less than 0.5 V the amplifier is fully operational. In the range between 1.5 V and V_{CC} – 1.5 V the amplifier is in mute condition. The mute condition is useful to suppress plop noise at the output caused by charging of the input capacitor.

Headphone connection

A headphone can be connected to the amplifier using two coupling capacitors for each channel. The common GND pin of the headphone is connected to the ground of the amplifier (see Fig.4). In this case the BTL/SE pin must be either on a logic HIGH level or not connected at all.

The two coupling capacitors can be omitted if it is allowed to connect the common GND pin of the headphone jack not to ground, but to a voltage level of $\frac{1}{2}V_{CC}$. See Fig.5 for the application diagram. In this case the BTL/SE pin must be either on a logic LOW level or connected to ground. If the BTL/SE pin is on a LOW level, the power amplifier for the positive loudspeaker terminal is always in mute condition.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage	operating	−0.3	18	V
V_I	input voltage		−0.3	V_{CC} + 0.3	V
I_{ORM}	repetitive peak output current		–	1	A
T_{stg}	storage temperature	non-operating	−55	150	°C
T_{amb}	operating ambient temperature		−40	85	°C
V_{psc}	AC and DC short-circuit safe voltage		–	10	V
P_{tot}	total power dissipation	SO16	–	1.2	W
		DIP16	–	2.2	W

QUALITY SPECIFICATION

In accordance with *"SNW-FQ-611-E"*. The number of the quality specification can be found in the *"Quality Reference Handbook"*. The handbook can be ordered using the code 9397 750 00192.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air:		
	TDA8542T (SO16L)	100	K/W
	TDA8542 (DIP16)	55	K/W

DC CHARACTERISTICS

V_{CC} = 5 V; T_{amb} = 25 °C; R_L = 8 Ω; V_{MODE} = 0 V; measured in test circuit Fig.3; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	operating	2.2	5	18	V
I_q	quiescent current	$R_L = \infty$; note 1	–	15	22	mA
I_{stb}	standby current	$V_{MODE} = V_{CC}$	–	–	10	μA
V_O	DC output voltage	note 2	–	2.2	–	V
$\lvert V_{OUT+} - V_{OUT-} \rvert$	differential output voltage offset		–	–	50	mV
I_{IN+}, I_{IN-}	input bias current		–	–	500	nA
V_{MODE}	input voltage mode select	operating	0	–	0.5	V
		mute	1.5	–	V_{CC} – 1.5	V
		standby	V_{CC} – 0.5	–	V_{CC}	V
I_{MODE}	input current mode select	$0 < V_{MODE} < V_{CC}$	–	–	20	μA
V_{BS}	input voltage BTL/SE pin	single ended	0	–	0.6	V
		BTL	2	–	V_{CC}	V
I_{BS}	input current BTL/SE pin	V_{BS} = 0	–	–	100	μA

Notes

1. With a load connected at the outputs the quiescent current will increase, the maximum of this increase being equal to the DC output offset voltage divided by R_L.
2. The DC output voltage with respect to ground is approximately 0.5 × V_{CC}.

AC CHARACTERISTICS

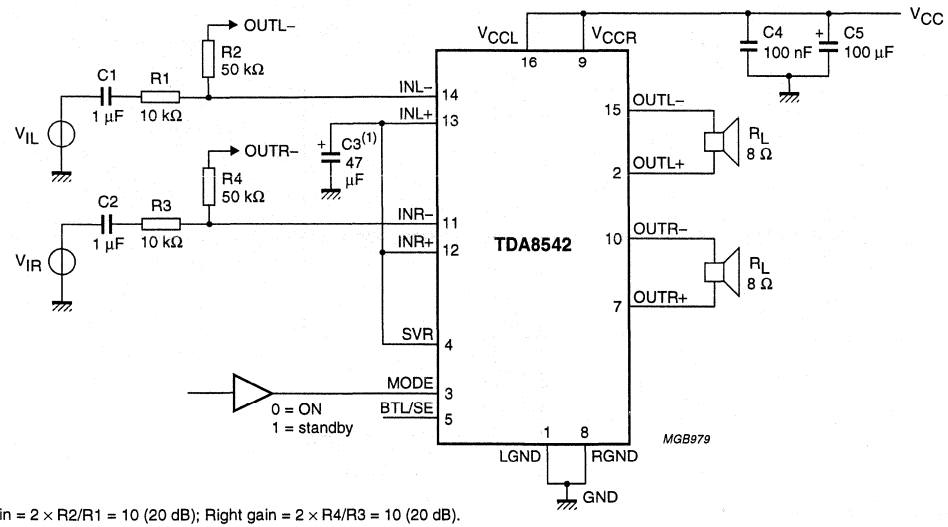
V_{CC} = 5 V; T_{amb} = 25 °C; R_L = 8 Ω; f = 1 kHz; V_{MODE} = 0 V; measured in test circuit Fig.3; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_o	output power	THD = 10%	1	1.2	–	W
		THD = 0.5%	0.6	0.9	–	W
THD	total harmonic distortion	P_o = 0.5 W	–	0.15	0.3	%
G_v	closed loop voltage gain	note 1	6	–	30	dB
Z_i	differential input impedance		–	100	–	kΩ
V_{no}	noise output voltage	note 2	–	–	100	μV
SVRR	supply voltage ripple rejection	note 3	50	–	–	dB
		note 4	40	–	–	dB
V_o	output voltage in mute condition	note 5	–	–	200	μV
α_{cs}	channel separation		40	–	–	dB

Notes

1. Gain of the amplifier is 2 × R2/R1 in test circuit of Fig.3.
2. The noise output voltage is measured at the output in a frequency range from 20 Hz to 20 kHz (unweighted), with a source impedance of R_S = 0 Ω at the input.
3. Supply voltage ripple rejection is measured at the output, with a source impedance of R_S = 0 Ω at the input. The ripple voltage is a sine wave with a frequency of 1 kHz and an amplitude of 100 mV (RMS), which is applied to the positive supply rail.
4. Supply voltage ripple rejection is measured at the output, with a source impedance of R_S = 0 Ω at the input. The ripple voltage is a sine wave with a frequency between 100 Hz and 20 kHz and an amplitude of 100 mV (RMS), which is applied to the positive supply rail.
5. Output voltage in mute position is measured with a 1 V (RMS) input voltage in a bandwidth of 20 kHz, so including noise.

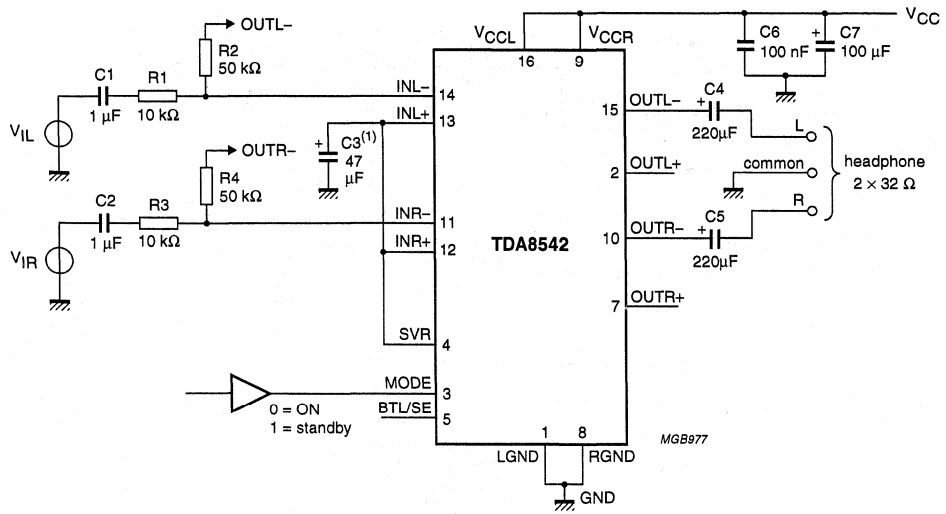
TEST AND APPLICATION INFORMATION



Left gain = 2 × R2/R1 = 10 (20 dB); Right gain = 2 × R4/R3 = 10 (20 dB).

(1) Reducing the value of C3 results in a decrease in performance of SVRR at low frequencies.

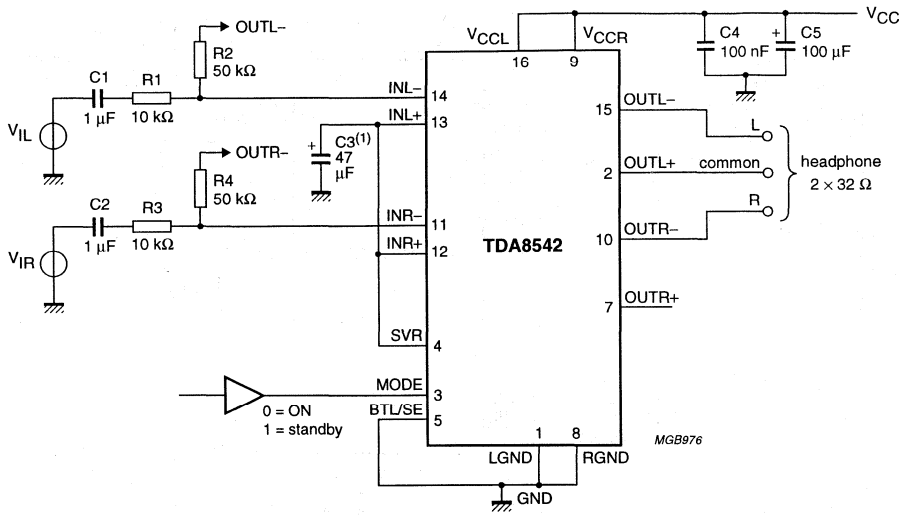
Fig.3 BTL application and test circuit.



Left gain = R2/R1 = 5; Right gain = R4/R3 = 5.

(1) Reducing the value of C3 results in a decrease in performance of SVRR at low frequencies.

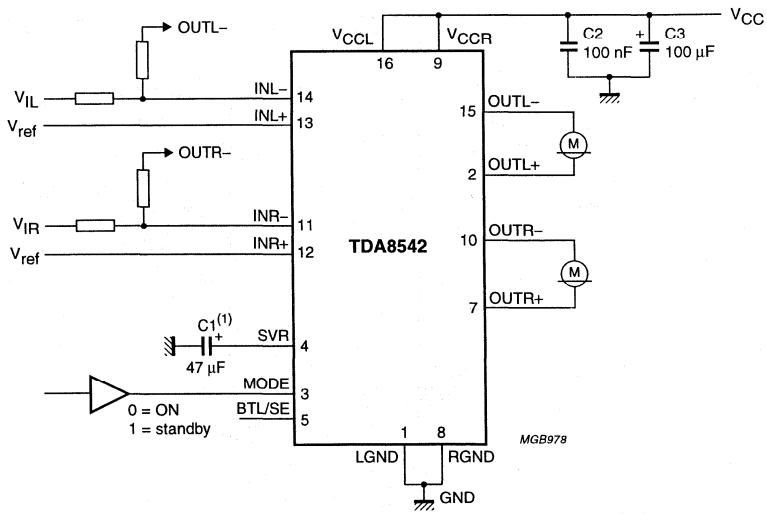
Fig.4 Single-ended headphone application.



Left gain = R2/R1 = 5; Right gain = R4/R3 = 5.

(1) Reducing the value of C3 results in a decrease in performance of SVRR at low frequencies.

Fig.5 Headphone application without coupling capacitors.



(1) Reducing the value of C1 results in a decrease in performance of SVRR at low frequencies.

Fig.6 Motor drive application.

Low-voltage stereo headphone amplifier TDA8559

FEATURES

- Operating voltage from 1.8 to 30 V
- Very low quiescent current
- Low distortion
- Few external components
- Differential inputs
- Usable as a mono amplifier in bridge-tied load (BTL) or stereo single-ended (SE)
- Single-ended mode without loudspeaker capacitor
- Mute and standby mode
- Short-circuit proof to ground, to supply voltage (<18 V) and across load
- No switch on or switch off clicks
- ESD protected on all pins.

APPLICATIONS

- Portable telephones
- Walk-man's
- Portable audio
- Mains fed equipment.

GENERAL DESCRIPTION

The TDA8559 is a stereo amplifier that operates over a wide supply voltage range from 1.8 to 30 V and consumes a very low quiescent current. This makes it suitable for battery fed applications (2 × 1.5 V cells). Because of an internal voltage buffer, this device can be used with or without a capacitor connected in series with the load. It can be applied as a headphone amplifier, but also as a mono amplifier with a small speaker (25 W), or as a line driver in mains applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	operating supply voltage		1.8	3	30	V
$I_{q(tot)}$	total quiescent current		–	2.75	4	mA
I_{stb}	standby supply current		–	–	10	μA
Stereo application						
P_o	output power	THD = 10%	30	35	–	mW
THD	total harmonic distortion	P_o = 20 mW; f_i = 1 kHz	–	0.05	0.1	%
		P_o = 20 mW; f_i = 10 kHz	–	0.1	–	%
G_v	voltage gain		25	26	27	dB
f_{ss}	small signal roll-off frequency	−1 dB	–	750	–	kHz
BTL application						
P_o	output power	THD = 10%	125	140	–	mW
THD	total harmonic distortion	P_o = 20 mW; f_i = 1 kHz	–	0.075	0.15	%
		P_o = 20 mW; f_i = 10 kHz	–	0.2	–	%
G_v	voltage gain		31	32	33	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8559	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1
TDA8559T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

BLOCK DIAGRAM

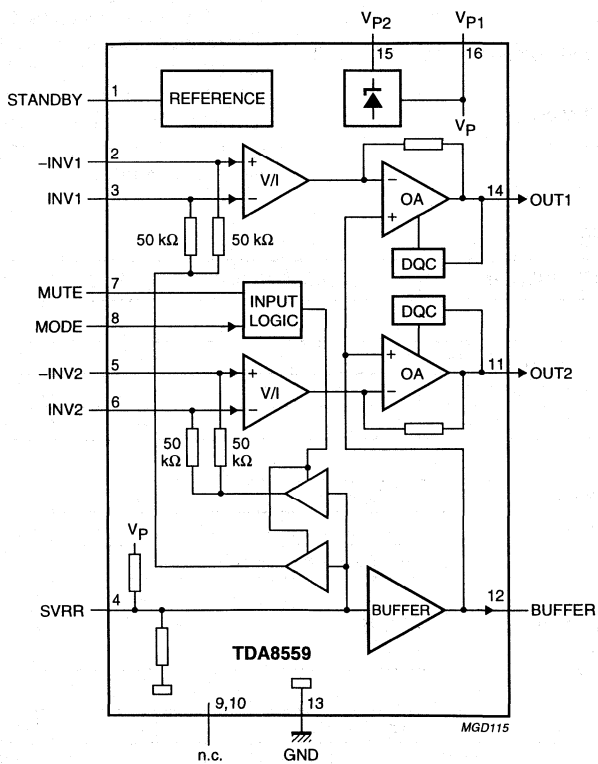


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
STANDBY	1	standby select
–INV1	2	non-inverting input 1
INV1	3	inverting input 1
SVRR	4	supply voltage ripple rejection
–INV2	5	non-inverting input 2
INV2	6	inverting input 2
MUTE	7	mute select
MODE	8	input mode select
n.c.	9	not connected
n.c.	10	not connected
OUT2	11	output 2
BUFFER	12	buffer output ($0.5V_P$)
GND	13	ground
OUT1	14	output 1
V_{P2}	15	high supply voltage
V_{P1}	16	low supply voltage

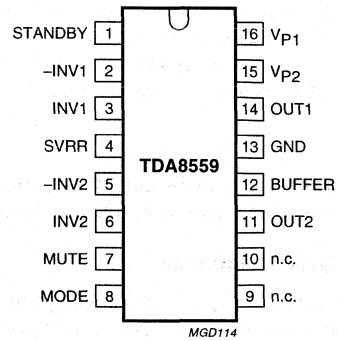


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA8559 contains two amplifiers with differential inputs, a $0.5V_P$ output buffer and a high supply voltage stabiliser. Each amplifier consist of a voltage-to-current converter (V/I), an output amplifier and its dynamic quiescent controller. The gain of each amplifier is internally fixed at 26 dB (= 20 ×). The $0.5V_P$ output can be used as a replacement for the single-ended capacitors. The two amplifiers can also be used as a mono amplifier in a bridge-tied load (BTL) configuration thereby resulting in more output power.

With three mode select pins, the device can be switched into the following modes;

1. Standby mode ($I_P < 10$ μA)
2. Mute mode
3. Operation mode, with two input selections (the input source is directly connected or connected via a coupling capacitor at the input).

The ripple rejection in the stereo application with a single-ended capacitor can be improved by connecting a capacitor between the $0.5V_P$ capacitor pin and ground.

The device is fully protected against short-circuiting of the output pins to ground, to the low supply voltage pin and across the load.

V/I converters

The V/I converters have a transconduction of 400 μS. The inputs are completely symmetrical and the two amplifiers can be used in opposite phase. The mute mode causes the V/I converters to block the input signal. The input mode pin selects two applications in which the V/I converters can be used.

The first application (input mode pin floating) is used with a supply voltage below 6 V. The input DC level is at ground level (the unused input pin connected to ground) and no input coupling capacitors are necessary. The maximum converter output current is sufficient to obtain an output swing of 3 V (peak).

In the second application with a supply voltage greater than 6 V (input mode pin high), the input mode pin is connected to V_P. In this configuration (input DC level = $0.5V_P$ + 0.6 V) the input source must be coupled with a capacitor and the two unused input pins must be connected via a capacitor to ground, to improve noise performance. This application has a higher quiescent current, because the maximum output current of the V/I converter is higher to obtain an output voltage swing of 9 V (peak).

Output amplifiers

The output amplifiers have a transresistance of 50 kΩ, a bandwidth of approximately 750 kHz and a maximum output current of 150 mA. The mid-tap output voltage equals the voltage applied at the non-inverting pin of the output amplifier. This pin is connected to the output of the $0.5V_P$ buffer. This reduces the distortion when the load is connected between an output amplifier and the buffer (because feedback is applied over the load).

Buffer

The buffer delivers $0.5V_P$ to the output with a maximum output (sink and source) current of 300 mA (peak).

Dynamic quiescent controller

The Dynamic Quiescent Current controller (DQC) gives the advantage of low quiescent current and low distortion. When there are high frequencies in the output signal, the DQC will increase the quiescent current of its own output amplifier. This will reduce the cross-over distortion that normally occurs at high frequencies and low quiescent current. The DQC gives two output currents that are linear with the amplitude and the frequency of the output signal of its own output amplifier. These currents control the quiescent current.

Stabilizer

The TDA8559 has a voltage supply range from 1.8 to 30 V. This range is divided over two supply voltage pins. Pin 16 is 1.8 to 18 V (breakdown voltage of the process); this pin is preferred for supply voltages less than 18 V. Pin 15 is used for applications where V_P is approximately 6 to 30 V. The stabilizer output is internally connected to the supply voltage pin 16 and in the range from 6 to 18 V to pin 15. The voltage drop to pin 16 is 1 V. In the range from 18 to 30 V the stabilizer output voltage (to pin 16) is approximately 17 V.

Input logic

The mute pin (pin 7) selects the mute mode of the V/I converters. Low (TTL/CMOS) level is mute. A voltage between 0.5 V (low level) and 1.5 V (high level) causes a soft mute to operate (no plops). When pin 7 is floating or greater than 1.5 V it is in the operating condition.

The input mode pin must be connected to V_P when the supply voltage is greater than 6 V. The input mode logic raises the tail current of the V/I converters and enables the two buffers to bias the inputs of the V/I converters.

Reference

This circuit supplies all currents needed in this device. With the standby mode pin 1 (TTL/CMOS), it is possible to switch to the standby mode and reduce the total quiescent current to below 10 μA.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{P2(max)}$	maximum supply voltage (pin 15)		–	30	V
$V_{P1(max)}$	maximum supply voltage (pin 16)		–	18	V
$V_{i(max)}$	maximum input voltage		–	18	V
I_{ORM}	peak output current	repetitive	–	150	mA
P_{tot}	total power dissipation	SO16	–	1.19	W
		DIP16	–	2.4	W
T_{amb}	operating ambient temperature		−40	+150	°C
T_{stg}	storage temperature		−55	+150	°C
T_{vj}	virtual junction temperature		–	150	°C
t_{sc}	short-circuiting time		–	1	hour

QUALITY SPECIFICATION

Quality in accordance with *"UZW-FQ-611"*, if this type is used as an audio amplifier. The number of the quality specification can be found in the *"Quality Reference handbook"*. The handbook can be ordered using the code 9397 750 00192.

THERMAL CHARACTERISTICS

SYMBOL	DESCRIPTION	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	DIP16	52	K/W
	SO16	105	K/W

CHARACTERISTICS

V_P = 3 V; T_{amb} = 25 °C; f_i = 1 kHz; unless otherwise specified).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DC characteristics						
V_P	operating supply voltage	note 1	1.8	3	30	V
$I_{q(tot)}$	total quiescent current	open load	–	2.75	4	mA
I_{stb}	standby supply current	open load	–	–	10	µA
V_1	standby mode voltage	standby	0	–	0.5	V
		operating	1.5	–	18	V
V_7	mute mode voltage	mute	0	–	0.5	V
		operating	1.5	–	18	V
I_{bias}	input bias current		–	100	300	nA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Single-ended stereo application (R_L = 32 Ω)						
P_o	output power	THD = 10%	30	35	–	mW
THD	total harmonic distortion	P_o = 20 mW; f_i = 1 kHz; note 2	–	0.05	0.1	%
		P_o = 20 mW; f_i = 10 kHz; note 2	–	0.1	–	%
G_v	voltage gain		25	26	27	dB
f_{ss}	small signal roll-off frequency	–1 dB	–	750	–	kHz
α_{cs}	channel separation	R_s = 5 kΩ	40	–	–	dB
$\lvert\Delta G_v\rvert$	channel unbalance		–	–	1	dB
V_{no}	noise output voltage	note 3	–	75	90	μV
$V_{no(mute)}$	noise output voltage in mute	note 3	–	35	45	μV
$V_{o(mute)}$	output voltage in mute	note 4	–	–	45	μV
V_{mt}	mid-tap voltage		1.4	1.5	1.6	V
Z_i	input impedance		75	100	125	kΩ
V_{os}	DC output offset voltage	note 5	–	–	100	mV
SVRR	supply voltage ripple rejection	note 6	45	–	–	dB
BTL application (R_L = 25 Ω)						
P_o	output power	THD = 10%	125	140	–	mW
THD	total harmonic distortion	P_o = 20 mW; f_i = 1 kHz; note 2	–	0.075	0.15	%
		P_o = 20 mW; f_i = 10 kHz; note 2	–	0.2	–	%
G_v	voltage gain		31	32	33	dB
f_{ss}	small signal roll-off frequency	–1 dB	–	750	–	kHz
V_{no}	noise output voltage	note 3	–	100	120	μV
$V_{no(mute)}$	noise output voltage in mute	note 3	–	50	60	μV
$V_{o(mute)}$	output voltage in mute	note 4	–	–	60	μV
V_{os}	DC output offset voltage	note 7	–	–	150	mv
SVRR	supply voltage ripple rejection	note 6	44	–	–	dB
Z_i	input impedance		39	50	61	kΩ
Line driver application (R_L = 1 kΩ)						
V_o	line output voltage		0.1	–	2.9	V

Note

1. The supply voltage range at pin V_{P1} is from 1.8 to 18 V. Pin V_{P2} is used for the voltage range from 6 to 30 V.
2. Measured with low-pass filter 30 kHz.
3. Noise output voltage measured with a bandwidth of 20 Hz to 20 kHz, unweighted. R_s = 5 kΩ
4. RMS output voltage in mute is measured with V_i = 200 mV (RMS); f = 1 kHz.
5. DC output offset voltage is measured between the signal output and the $0.5V_P$ output.
6. The ripple rejection is measured with a ripple voltage of 200 mV (RMS) applied to the positive supply rail (R_s = 0 kΩ).
7. DC output offset voltage is measured between the two signal outputs.

TEST AND APPLICATION INFORMATION

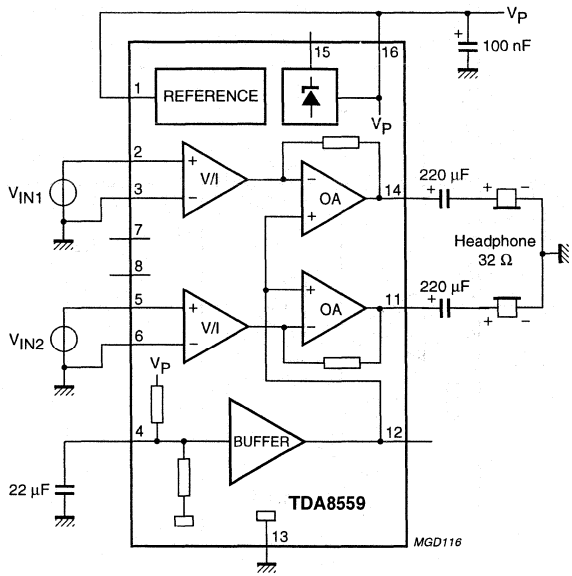


Fig.3 Single-ended with loudspeaker capacitor.

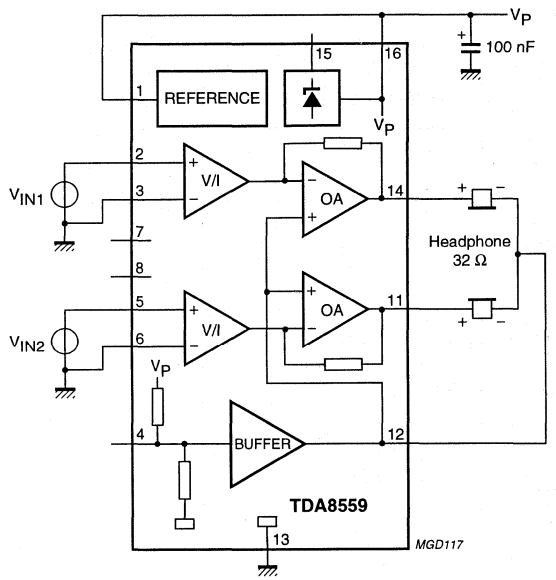


Fig.4 Single-ended with buffer.

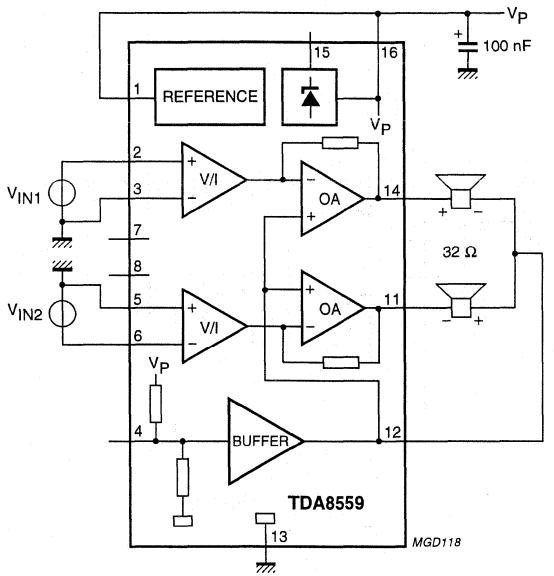


Fig.5 Improved single-ended with buffer.

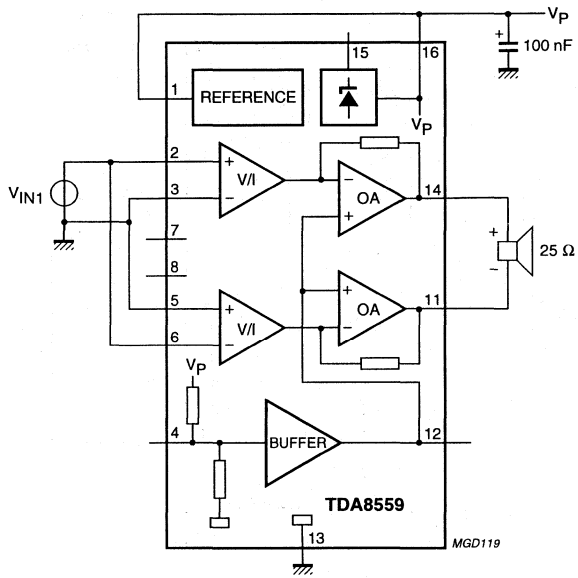


Fig.6 BTL amplifier.

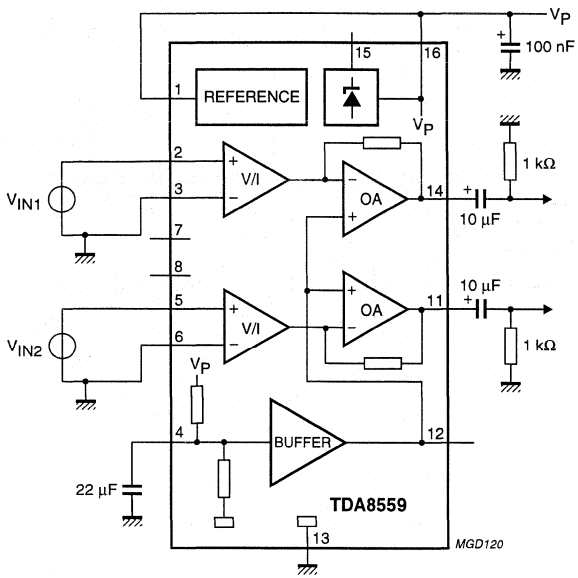


Fig.7 Line driver application 1.8 to 6 V.

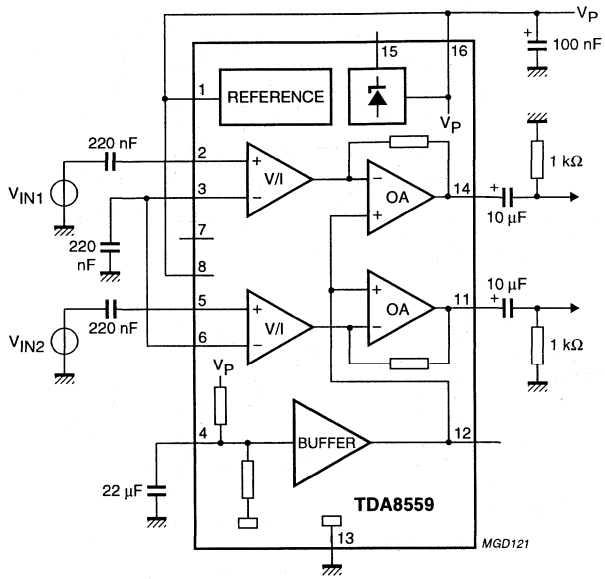


Fig.8 Line driver application V_P = 6 to 18 V.

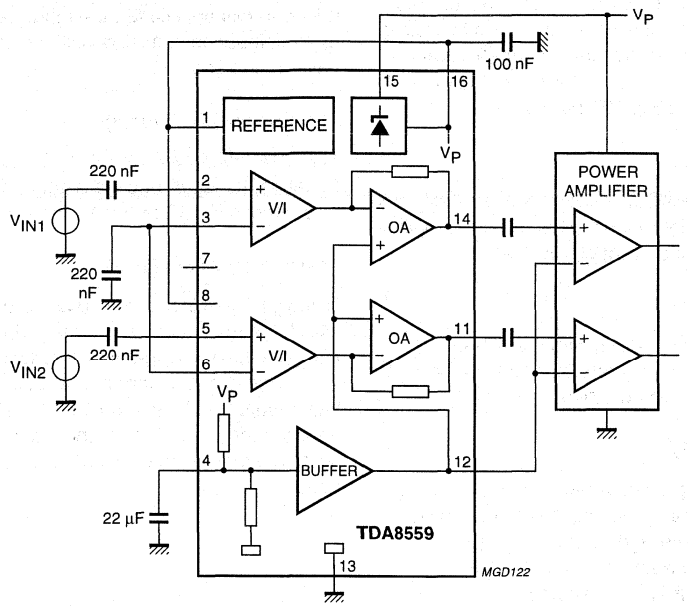


Fig.9 Line driver application V_P = 6 to 30 V.

Application notes

GENERAL

For applications where V_P has a maximum voltage of 6 V (input mode low), the input pins need a DC path to ground, see Fig.10 and Fig.11 for applications where V_P has a voltage range of 6 to 18 V (input mode high) the input DC level is $0.5V_P + 0.6$ V, see Fig.12 and Fig.13.

APPLICATION 1 (see Fig.3)

This is the basic headphone application with four external components. In this configuration the headphone amplifier can deliver a peak output current of 100 mA.

APPLICATION 2 (see Fig.4)

The advantage of this application, with respect to Application 1, is that it has only one external component and maintains the same performance.

APPLICATION 3 (see Fig.5)

This application is an improved version of application 2. The difference is connecting the two loads in opposite phase. This lowers the average current through the single-ended buffer. A headphone cannot be used because it is necessary that the load has floating terminals.

APPLICATION 4 (see Fig.6)

This configuration delivers four times the output power of the single-ended application with the same load conditions. The disadvantage is that the load must have floating terminals consequently a stereo headphone application is not possible.

APPLICATION 5 (see Fig.7)

The TDA8559 has a virtual rail-to-rail output voltage and is also usable in a low voltage environment such as a line driver. In this application the input needs a DC path to ground; input configurations illustrated in Fig.10 or Fig.11 have to be used.

APPLICATION 6 (see Fig.8)

The TDA8559 has a virtual rail-to-rail output voltage. Because the input mode is high, input configurations illustrated in Fig.12 or Fig.13 have to be used.

APPLICATION 7 (see Fig.9)

Using pin V_{P2} it is possible to use the headphone amplifier above the maximum 18 V supply voltage of pin V_{P1}. The internal supply voltage will be reduced to approximately 17 V. This is convenient in applications where there is a higher supply voltage than 18 V but do not need an output voltage swing that reaches the higher supply voltage; input configurations illustrated in Fig.12 or Fig.13 have to be used.

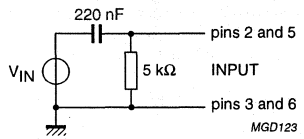


Fig.10 Input configuration; with input capacitor and $V_P < 6$ V.

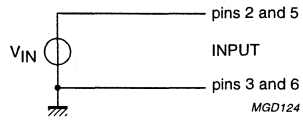


Fig.11 Input configuration; without input capacitor and $V_P < 6$ V.

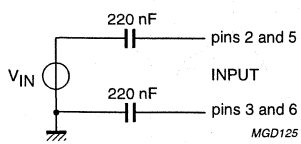


Fig.12 Input configuration; at $V_P > 6$ V.

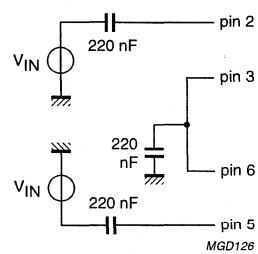
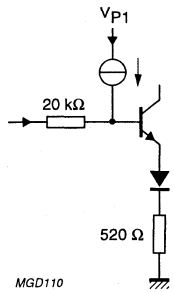
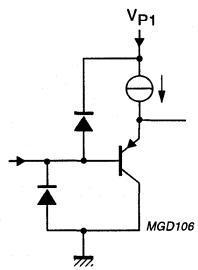
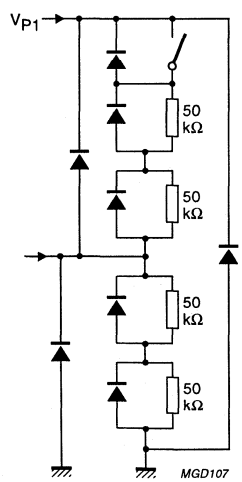
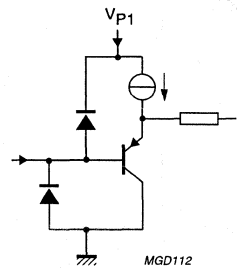
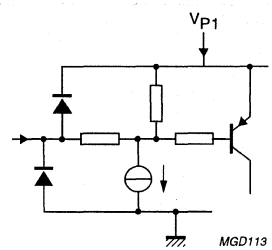
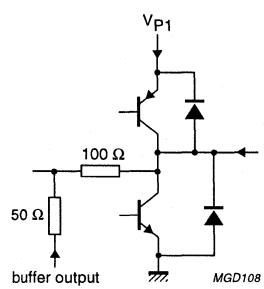
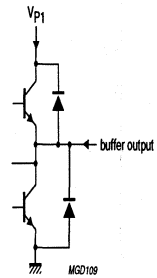
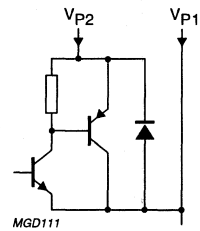


Fig.13 Input configuration; at $V_P > 6$ V (combined negative inputs).

INTERNAL PIN CONFIGURATION

SYMBOL	PIN	EQUIVALENT CIRCUIT
STANDBY	1	
–INV1, INV1, –INV2 and INV2	2, 3, 5 and 6	
SVRR	4	

SYMBOL	PIN	EQUIVALENT CIRCUIT
MUTE	7	
MODE	8	
OUT2 and OUT1	11 and 14	

SYMBOL	PIN	EQUIVALENT CIRCUIT
BUFFER	12	
V_{P2} and V_{P1}	15 and 16	

6-bit high-speed dual Analog-to-Digital Converter (ADC)

TDA8705A

FEATURES

- 2 times 6-bit resolution
- Sampling rate up to 80 MHz
- High signal-to-noise ratio over a large analog input frequency range (5.5 effective bits at 20 MHz full-scale input at f_{clk} = 80 MHz)
- TTL output
- Two separated inputs (AC-coupling)
- TTL compatible digital inputs
- Low-level AC clock input signal allowed
- Internal reference voltage regulator (external reference regulation possible)
- Power dissipation only 250 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- No sample-and-hold circuit required.

APPLICATIONS

High-speed analog-to-digital conversion for:

- DBS (Digital Broadcast Satellite)
- QPSK (Quadrature Phase Shift Keying) demodulation
- Video.

GENERAL DESCRIPTION

The TDA8705A is a 6-bit high-speed dual analog-to-digital converter (ADC) for satellite video and other applications. It converts the two analog input signals into two 6-bit binary-coded digital words at a maximum sampling rate of 80 MHz. All digital inputs and outputs are TTL compatible, although a low-level sine wave clock input signal is allowed.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current		20	27	32	mA
I_{CCD}	digital supply current		10	14	18	mA
I_{CCO}	output stages supply current		10	14	18	mA
ILE	DC integral linear error		–	±0.25	±0.5	LSB
DLE	DC differential linearity error		–	±0.25	±0.5	LSB
AILE	AC integral linearity error	note 1	–	±0.5	±1.0	LSB
$f_{clk(max)}$	maximum clock frequency		80	–	–	MHz
P_{tot}	total power dissipation		–	250	–	mW

Note

1. Full-scale sine wave (f_i = 20 MHz; f_{clk} = 80 MHz).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8705AT	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1

6-bit high-speed dual Analog-to-Digital Converter (ADC)

TDA8705A

BLOCK DIAGRAM

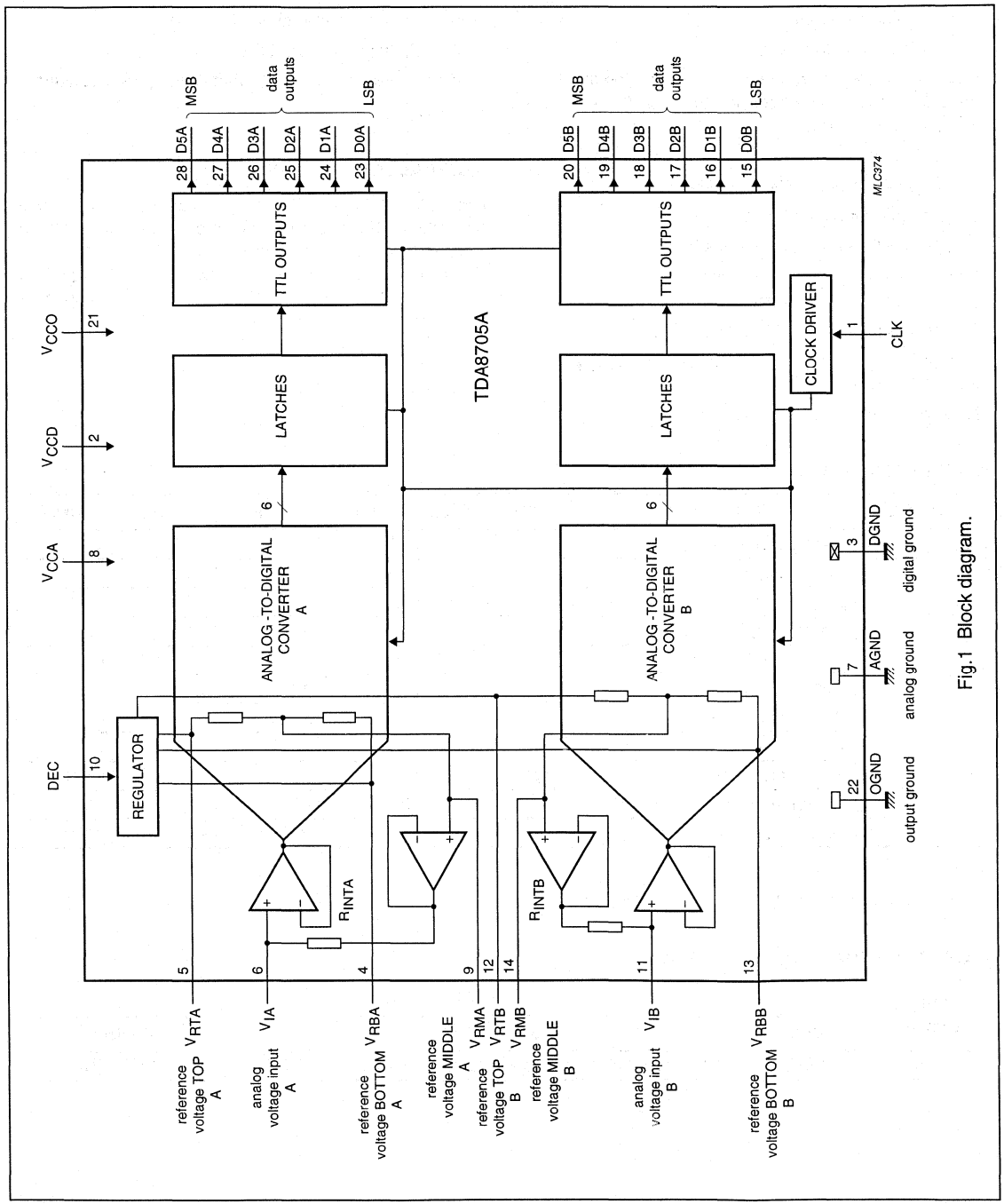


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
CLK	1	clock input
V_{CCD}	2	digital supply voltage (+5 V)
DGND	3	digital ground
V_{RBA}	4	reference voltage BOTTOM for ADC A (decoupling)
V_{RTA}	5	reference voltage TOP for ADC A (decoupling)
V_{IA}	6	analog input voltage for ADC A
AGND	7	analog ground
V_{CCA}	8	analog supply voltage (+5 V)
V_{RMA}	9	reference voltage MIDDLE for ADC A (decoupling)
DEC	10	decoupling input
V_{IB}	11	analog input voltage for ADC B
V_{RTB}	12	reference voltage TOP for ADC B (decoupling)
V_{RBB}	13	reference voltage BOTTOM for ADC B (decoupling)
V_{RMB}	14	reference voltage MIDDLE for ADC B (decoupling)
D0B	15	data output; bit 0 (LSB), ADC B
D1B	16	data output; bit 1, ADC B
D2B	17	data output; bit 2, ADC B
D3B	18	data output; bit 3, ADC B
D4B	19	data output; bit 4, ADC B
D5B	20	data output; bit 5 (MSB), ADC B
V_{CCO}	21	supply voltage for output stages (+5 V)
OGND	22	output ground
D0A	23	data output; bit 0 (LSB), ADC A
D1A	24	data output; bit 1, ADC A
D2A	25	data output; bit 2, ADC A
D3A	26	data output; bit 3, ADC A
D4A	27	data output; bit 4, ADC A
D5A	28	data output; bit 5 (MSB), ADC A

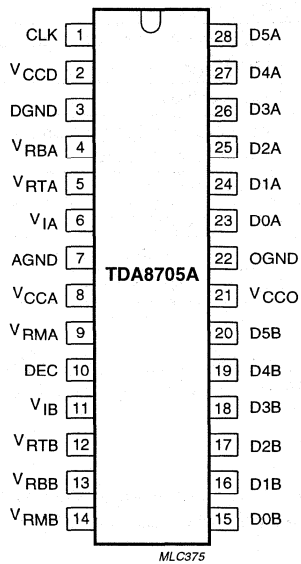


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage	note 1	−0.3	+7.0	V
V_{CCD}	digital supply voltage	note 1	−0.3	+7.0	V
V_{CCO}	output stages supply voltage	note 1	−0.3	+7.0	V
ΔV_{CC}	supply voltage differences between V_{CCA} and V_{CCD}		−1.0	+1.0	V
ΔV_{CC}	supply voltage differences between V_{CCO} and V_{CCD}		−1.0	+1.0	V
ΔV_{CC}	supply voltage differences between V_{CCA} and V_{CCO}		−1.0	+1.0	V
V_I	input voltage	referenced to AGND	−0.3	+7.0	V
$V_{clk(p-p)}$	AC input voltage for switching (peak-to-peak value)	referenced to DGND	−	V_{CCD}	V
I_O	output current		−	10	mA
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C
T_j	junction temperature		−	+150	°C

Note

1. The supply voltages V_{CCA}, V_{CCO} and V_{CCD} may have any value between −0.3 V and +7 V provided the difference between V_{CCA}, V_{CCO} and V_{CCD} is between −1 V and +1 V.

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air	70	K/W

CHARACTERISTICS

$V_{CCA} = V_8$ to $V_7 = 4.75$ to 5.25 V; $V_{CCD} = V_2$ to $V_3 = 4.75$ to 5.25 V; $V_{CCO} = V_{21}$ to $V_{22} = 4.75$ to 5.25 V; AGND, OGND and DGND shorted together; V_{CCA} to $V_{CCD} = -0.25$ to +0.25 V; V_{CCO} to $V_{CCD} = -0.25$ to +0.25 V; V_{CCA} to $V_{CCO} = -0.25$ to +0.25 V; $T_{amb} = 0$ to +70 °C; typical values measured at $V_{CCA} = V_{CCD} = V_{CCO} = 5$ V and $T_{amb} = 25$ °C; $C_L = 15$ pF; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current		20	27	32	mA
I_{CCD}	digital supply current		10	14	18	mA
I_{CCO}	output stages supply current		10	14	18	mA
Inputs						
CLOCK INPUT CLK; REFERENCED TO DGND; note 1						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	$V_{clk} = 0.4$ V	–1	–	+1	μA
I_{IH}	HIGH level input current	$V_{clk} = 2.7$ V	–	–	20	μA
Z_I	input impedance	$f_{clk} = 80$ MHz	–	2	–	kΩ
C_I	input capacitance	$f_{clk} = 80$ MHz	–	2	–	pF
V_I ANALOG INPUT VOLTAGE FOR A AND B; REFERENCED TO AGND						
R_I	DC parallel input resistance		20	–	–	kΩ
C_I	parallel input capacitance	$f_i = 20$ MHz	–	1.5	–	pF
α_{CT}	crosstalk between V_{IA} and V_{IB}	$f_i = 20$ MHz	40	–	–	dB
Reference voltages for the resistor ladder (A and B); see Table 1						
V_{RB}	reference voltage BOTTOM		1.9	2.0	2.1	V
V_{RT}	reference voltage TOP		2.8	2.9	3.0	V
V_{diff}	differential reference voltage $V_{RT} - V_{RB}$		0.85	0.90	0.95	V
I_{ref}	reference current		–	2	–	mA
R_{LAD}	resistor ladder		–	450	–	Ω
TC_{RLAD}	temperature coefficient of the resistor ladder		–	3280	–	ppm
V_{osB}	offset voltage BOTTOM	note 2	–	200	–	mV
V_{osT}	offset voltage TOP	note 2	–	200	–	mV
$V_{i(p-p)}$	input voltage amplitude (peak-to-peak value)		0.45	0.50	0.55	V
Outputs (A and B)						
DIGITAL OUTPUTS D5 TO D0 (REFERENCED TO DGND)						
V_{OL}	LOW level output voltage	$I_O = 1$ mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	$I_O = -1$ mA	2.4	–	V_{CCD}	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Switching characteristics						
CLOCK INPUT CLK; note 1; see Fig.3						
$f_{clk(max)}$	maximum clock frequency		80	–	–	MHz
t_{CPH}	clock pulse width HIGH		5.5	–	–	ns
t_{CPL}	clock pulse width LOW		5.5	–	–	ns
Analog signal processing						
LINEARITY						
ILE	DC integral linearity error		–	±0.25	±0.5	LSB
DLE	DC differential linearity error		–	±0.25	±0.5	LSB
AILE	AC integral linearity error	note 3	–	±0.5	±1.0	LSB
OFE	offset error between A and B	f_i = 10 MHz; f_{clk} = 40 MHz; note 4	±1	–	±2	LSB
GE	gain error between A and B	f_i = 10 MHz; f_{clk} = 40 MHz; note 4	±1	–	±2	LSB
MID	middle scale output code (A and B)		31	–	32	
BANDWIDTH; f_{clk} = 80 MHz						
B	–0.5 dB analog bandwidth	full-scale sine wave; note 5	–	50	–	MHz
t_{STLH}	analog input settling time LOW-to-HIGH	full-scale square wave; Fig.4; note 6	–	8	–	ns
t_{STHL}	analog input settling time HIGH-to-LOW	full-scale square wave; Fig.4; note 6	–	5	–	ns
HARMONICS; f_{clk} = 40 MHz; see Fig.5						
h_1	fundamental harmonics (full scale)	f_i = 20 MHz	–	–	0	dB
h_{all}	harmonics (full scale); all components	f_i = 20 MHz				
	second harmonics		–	–45	–	dB
	third harmonics		–	–41	–	dB
THD	total harmonic distortion	f_i = 20 MHz	–	–39	–34	dB
SIGNAL-TO-NOISE RATIO; note 7; see Fig.5						
S/N	signal-to-noise ratio (full scale)	without harmonics; f_{clk} = 80 MHz; f_i = 20 MHz	33	36	–	dB
EFFECTIVE BITS; note 7; see Fig.5						
EB	effective bits	f_{clk} = 80 MHz				
		f_i = 10 MHz	–	5.7	–	bits
		f_i = 20 MHz	–	5.5	–	bits
		f_i = 30 MHz	–	5.1	–	bits

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
TWO-TONE; note 8						
TTIR	two-tone intermodulation rejection	f_{clk} = 80 MHz	–	48	–	dB
BIT ERROR RATE						
BER	bit error rate	f_{clk} = 80 MHz; f_i = 20 MHz; V_i = ±16 LSB at code 32	–	10^{-12}	–	times/ samples
Timing (f_{clk} = 80 MHz; C_L = 15 pF); note 9; see Fig.3						
t_{ds}	sampling delay time		–	–	2	ns
t_h	output hold time		5	–	–	ns
t_d	output delay time		–	–	11	ns

Notes

1. In addition to a good layout of the digital and analog ground, it is recommended that the rise and fall times of the clock must not be less than 1 ns.
2. Analog input voltages producing code 00 up to and including 3F:
   a) V_{osB} (voltage offset BOTTOM) is the difference between the analog input which produces data equal to 00 and the reference voltage BOTTOM (V_{RB}) at T_{amb} = 25 °C.
   b) V_{osT} (voltage offset TOP) is the difference between V_{RT} (reference voltage TOP) and the analog input which produces data outputs equal to 3F at T_{amb} = 25 °C.
3. Full-scale sine wave (f_i = 20 MHz; f_{clk} = 80 MHz).
4. The Offset Error (OFE) and Gain Error (GE) are determined by taking results from a simultaneous acquisition on both ADCs of a sine wave greater than full-scale. The occurrences of code 0 and 63 are used to calculate the OFE (mid-scale-to-mid-scale) and the GE (amplitude difference) between the two converters A and B.
5. The –0.5 dB analog bandwidth is determined by the 0.5 dB reduction in the reconstructed output, the input being a full-scale sine wave. It is determined with a beat frequency method; no glitches occurrence.
6. The analog input settling time is the minimum time required for the input signal to be stabilized after a sharp full-scale input (square-wave signal) in order to sample the signal and obtain correct output data.
7. Effective bits are obtained via a Fast Fourier Transform (FFT) treatment taking 8K acquisition points per period. The calculation takes into account all harmonics and noise up to half of the clock frequency (NYQUIST frequency). Conversion to signal-to-noise ratio: S/N = EB × 6.02 + 1.76 dB.
8. Intermodulation measured relative to either tone with analog input frequencies of 20.0 MHz and 20.1 MHz. The two input signals have the same amplitude and the total amplitude of both signals provides full scale to the converter.
9. Output data acquisition: the output data is available after the maximum delay time of t_d.

Table 1 Output coding and input voltage (typical values; referenced to AGND)

STEP	$V_{I(p-p)}$ A or B (V)	BINARY OUTPUT BITS					
		D5	D4	D3	D2	D1	D0
Underflow	<2.2	0	0	0	0	0	0
0	2.2	0	0	0	0	0	0
1	2.208	0	0	0	0	0	1
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
62	2.692	1	1	1	1	1	0
63	2.7	1	1	1	1	1	1
Overflow	>2.7	1	1	1	1	1	1

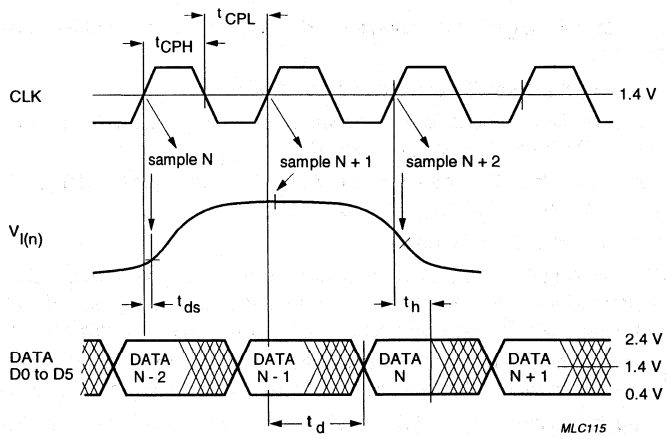


Fig.3 Timing diagram for data output.

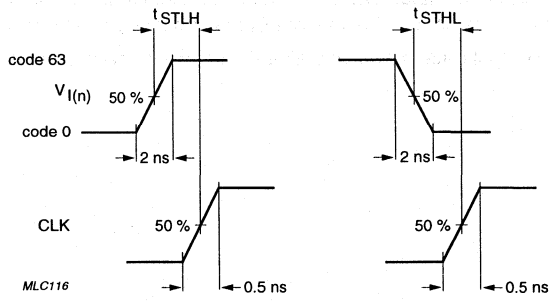
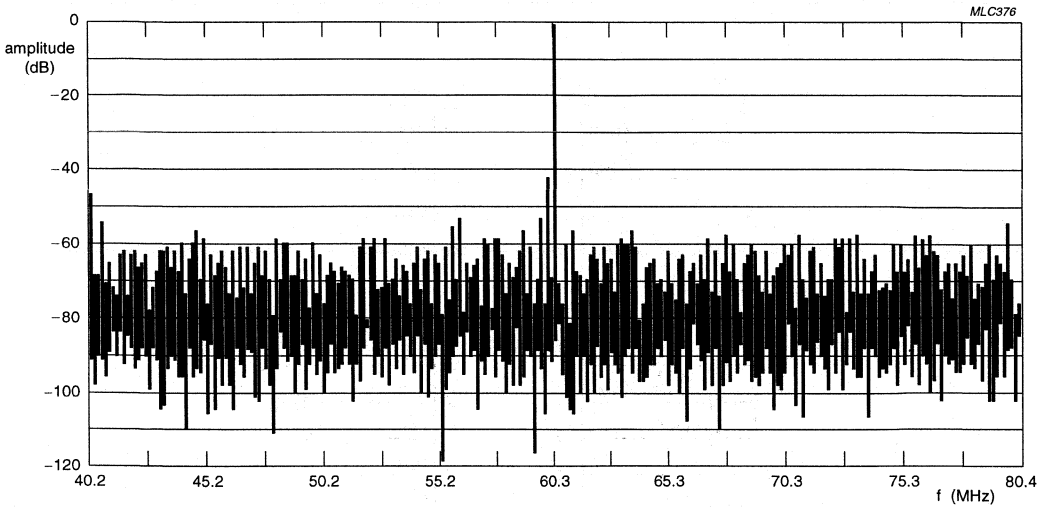


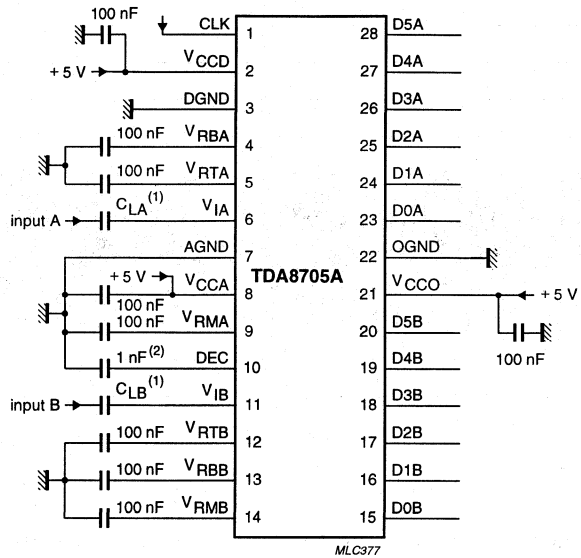
Fig.4 Analog input settling-time diagram.



Effective bits: 5.54; THD = −39.89 dB;
Harmonic levels (dB): 2nd = −46.51; 3rd = −41.21; 4th = −80.65; 5th = −60.16; 6th = −54.51.

Fig.5 Typical Fast Fourier Transform (f_{clk} = 80 MHz; f_i = 20 MHz).

APPLICATION INFORMATION



The analog and digital supplies should be separated and decoupled.

$V_{RT(n)}$, $V_{RM(n)}$ and $V_{RB(n)}$ and DEC inputs are decoupled to AGND.

(1) In the event of AC-coupling, C_{LA} and C_{LB} values are chosen in accordance with the classical low frequencies cut-off formulae

$$f_{CL} = \frac{1}{2 \times \pi \times R_i \times C_L}$$ where input resistance R_i is the value measured under DC conditions.

In the event of DC-coupling, C_{LA} and C_{LB} capacitors are omitted. The DC biassing and AC modulation signal directly applied to inputs (pin 6 and 11), must be in the range of $V_{RT(n)} - V_{RB(n)}$.

(2) When pin 10 (DEC) is short-circuited to AGND, an external regulator can be connected to $V_{RT(n)}$ and $V_{RB(n)}$.

Fig.6 Application diagram.

Triple RGB 6-bit video analog-to-digital interface

TDA8707

FEATURES

- Triple analog-to-digital converter (ADC)
- 6-bit resolution
- Sampling rate up to 35 MHz
- Power dissipation of 335 mW (typical)
- Internal clamping function
- TTL compatible digital inputs
- –40 to +85 °C operating temperature
- CMOS digital outputs.

APPLICATIONS

- High-speed analog-to-digital conversion for video signals
- VGA signal treatment.

DESCRIPTION

The TDA8707 is a CMOS triple 6-bit video low-power analog-to-digital converter (ADC) for RGB signals. It converts the analog inputs into 6-bit binary coded digital words at a sampling rate of 35 MHz. All analog signal inputs are clamped.

Analog-to-digital converter

The TDA8707 implements 3 independent 6-bit analog-to-digital converters in CMOS process. These converters use a full-flash approach.

Clamping feature

An internal clamping circuit is provided in each of the 3 analog channels. The analog pins INR, ING and INB are switched, through series capacitors, to on-chip clamping levels during an active pulse on the clamp input CLP. Clamping level in the R, G and B channels is Code 0.

Input buffers

Internal buffers are provided to drive the analog-to-digital converter inputs. Their ratio can be adjusted externally at 1.5 or 2.0 with select input SLT.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
I_{DDA}	analog supply current		–	60	80	mA
I_{DDD}	digital supply current	f_{clk} = 35 MHz	–	5	8	mA
INL	integral non-linearity	f_{clk} = 35 MHz; ramp input; T_{amb} = 25 °C	–	±0.35	±0.6	LSB
DNL	differential non-linearity	f_{clk} = 35 MHz; ramp input; T_{amb} = 25 °C	–	±0.35	±0.6	LSB
EB	effective bits	note 1	–	5.3	–	bits
f_{clk}	maximum clock conversion rate		35	–	–	MHz
P_{tot}	total power dissipation	f_{clk} = 35 MHz; note 2	–	335	485	mW

Notes

1. The number of effective bits is measured with a clock frequency of 35 MHz. This value is given for a 4.43 MHz frequency on the R, G and B channels.
2. The external resistor (value 15 kΩ) between V_{DDA} and CLREF, fixing internal static currents, influences P_{tot}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8707H	QFP44	plastic quad flat package; 44 leads; lead length 1.3 mm; body 10 × 10 × 1.75 mm	SOT307-2

BLOCK DIAGRAM

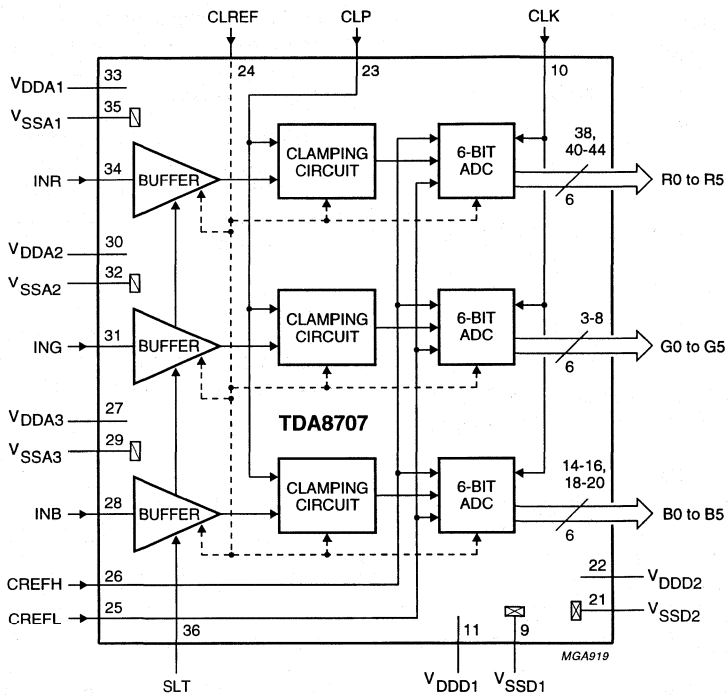


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
n.c.	2	not connected
G0	3	GREEN data output; bit 0 (LSB)
G1	4	GREEN data output; bit 1
G2	5	GREEN data output; bit 2
G3	6	GREEN data output; bit 3
G4	7	GREEN data output; bit 4
G5	8	GREEN data output; bit 5 (MSB)
V_{SSD1}	9	digital supply ground 1
CLK	10	clock input
V_{DDD1}	11	digital supply voltage 1
n.c.	12	not connected
n.c.	13	not connected
B0	14	BLUE data output; bit 0 (LSB)
B1	15	BLUE data output; bit 1
B2	16	BLUE data output; bit 2
n.c.	17	not connected
B3	18	BLUE data output; bit 3
B4	19	BLUE data output; bit 4
B5	20	BLUE data output; bit 5 (MSB)
V_{SSD2}	21	digital supply ground 2
V_{DDD2}	22	digital supply voltage 2

SYMBOL	PIN	DESCRIPTION
CLP	23	clamping input
CLREF	24	ADCs current reference level input
CREFL	25	converter reference LOW level input
CREFH	26	converter reference HIGH level input
V_{DDA3}	27	analog supply voltage 3
INB	28	BLUE analog input
V_{SSA3}	29	analog supply ground 3
V_{DDA2}	30	analog supply voltage 2
ING	31	GREEN analog input
V_{SSA2}	32	analog supply ground 2
V_{DDA1}	33	analog supply voltage 1
INR	34	RED analog input
V_{SSA1}	35	analog supply ground 1
SLT	36	select input buffer ratio
n.c.	37	not connected
R0	38	RED data output; bit 0 (LSB)
n.c.	39	not connected
R1	40	RED data output; bit 1
R2	41	RED data output; bit 2
R3	42	RED data output; bit 3
R4	43	RED data output; bit 4
R5	44	RED data output; bit 5 (MSB)

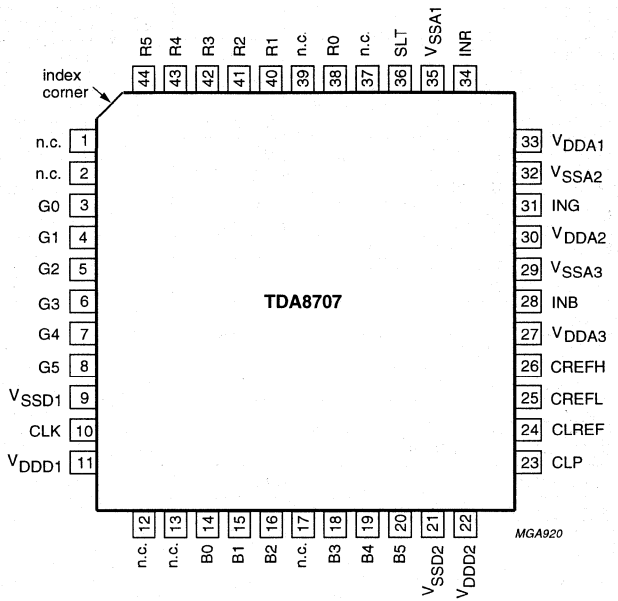


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage (pins 27, 30 and 33)		−0.3	+6.5	V
V_{DDD}	digital supply voltage (pins 11 and 22)		−0.3	+6.5	V
ΔV_{DD}	supply voltage difference between V_{DDA} and V_{DDD}		−0.5	+0.5	V
V_I	input voltage (pins 28, 31 and 34)	referenced to V_{SSA}	−	V_{DDA}	V
$V_{i(p-p)}$	AC input voltage for switching (pins 10 and 23; peak-to-peak value)	referenced to V_{SSD}	−	V_{DDD}	V
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		−40	+85	°C
T_j	junction temperature		−	+125	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air	75	K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS (see Tables 1 and 2)

$V_{DDA} = V_{DDD} = 4.5$ to 5.5 V; V_{SSA} and V_{SSD} short-circuited together; $V_{DDA} - V_{DDD} = -0.5$ to +0.5 V; $T_{amb} = -40$ to +85 °C; SLT = 0 V; CREFH = 2 V, CREFL = 0.5 V, $C_L = 15$ pF; typical values measured at $V_{DDA} = V_{DDD} = 5$ V; $V_{SSA} = V_{SSD} = 0$ V and $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDA}	analog supply voltage	note 1	4.5	5.0	5.5	V
V_{DDD}	digital supply voltage	note 1	4.5	5.0	5.5	V
I_{DDA}	analog supply current	note 1	–	60	80	mA
I_{DDD}	digital supply current	$f_{clk} = 35$ MHz	–	5	8	mA
Inputs						
DIGITAL INPUTS (CLK: PIN 10 AND CLP: PIN 23)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DDD}	V
I_{LI}	input leakage current		−10	–	+10	μA
C_I	input capacitance		–	7	–	pF
CLAMP AND REFERENCES (CLREF: PIN 24, CREFL: PIN 25 AND CREFH: PIN 26)						
A_{CL}	clamping accuracy		–	±0.5	–	LSB
I_{CL}	input clamping current		−200	–	+400	μA
C_{CL}	external series clamping capacitor		10	22	–	nF
R_{CLREF}	external resistor on CLREF pin for current reference of converter	note 2	12	15	–	kΩ
V_{REFH}	converter reference voltage HIGH level applied to CREFH pin	referenced to V_{SSA}	1.5	2.0	2.5	V
V_{REFL}	converter reference voltage LOW level applied to CREFL pin	referenced to V_{SSA}	0.25	0.5	0.75	V
ΔREF	reference voltage difference between V_{REFH} and V_{REFL}	note 3	–	1.5	–	V
Z_{CREF}	internal ladder impedance between pins CREFH and CREFL		–	300	–	Ω
ANALOG INPUTS (INR: PIN 34, ING: PIN 31 AND INB: PIN 28)						
$V_{I(p-p)}$	full-range input voltage (peak-to-peak value)	SLT = logic 0; gain = 1.5; note 4	–	1.0	–	V
		SLT = logic 1; gain = 2.0; note 4	–	0.75	–	V
I_I	input current	clamp off	–	5	100	nA
C_I	input capacitance		–	7	15	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
INPUT ISOLATION						
α_{ct}	crosstalk between INR, ING and INB		–	–	–40	dB
Outputs (R0 to R5: pins 38 and 40 to 44; G0 to G5: pins 3 to 8; B0 to B5: pins 14 to 16 and 18 to 20)						
V_{OL}	LOW level output voltage		0	–	0.5	V
V_{OH}	HIGH level output voltage		4.0	–	V_{DDD}	V
Switching characteristics						
CLOCK INPUT CLK (see Fig.3)						
$f_{clk(max)}$	maximum clock frequency		35	–	–	MHz
t_{CPH}	clock pulse width HIGH		10	–	–	ns
t_{CPL}	clock pulse width LOW		12	–	–	ns
Analog signal processing (50% clock duty cycle) f_{clk} = 35 MHz						
LINEARITY						
INL	integral non-linearity	ramp input; T_{amb} = 25 °C	–	±0.35	±0.6	LSB
DNL	differential non-linearity	ramp input; T_{amb} = 25 °C	–	±0.35	±0.6	LSB
BANDWIDTH (see Fig.5 and note 7)						
B	–3 dB analog bandwidth		–	9	–	MHz
t_{STLH}	analog input settling time LOW-to-HIGH	full scale square wave	–	13	16	ns
t_{STHL}	analog input settling time HIGH-to-LOW	full scale square wave	–	11	14	ns
HARMONICS; note 6						
f_1	fundamental harmonic		–	–	0	dB
f_{all}	harmonics, all components		–	–37	–	dB
EFFECTIVE BITS						
EB	effective bits	f_i = 4.43 MHz	–	5.3	–	bits
DIFFERENTIAL GAIN; note 5						
G_{diff}	differential gain	PAL modulated ramp	–	3	–	%
DIFFERENTIAL PHASE; note 5						
φ_{diff}	differential phase	PAL modulated ramp	–	2	–	deg
Timing (see Figs 3 and 4)						
t_{dS}	sampling delay time		–	3	–	ns
t_h	output hold time		6	–	–	ns
t_d	output delay time	note 8	–	–	16	ns
t_r	clock rise time		3	5	–	ns
t_f	clock fall time		3	5	–	ns
t_{CLP}	active clamping duration		3	4	–	µs

Notes to the characteristics

1. V_{DDA} and V_{DDD} should be supplied from the same power supply and decoupled separately.
2. The analog supply current is directly proportional to the series resistance between V_{DDA} and CLREF.
3. CREFH and CREFL are connected respectively to the top and bottom reference ladders of the 3 analog-to-digital converters.
4. $V_{I(p-p)} = (V_{REFL} - V_{REFH})$/buffer gain factor. See Table for gain factor selection. When clamping at code 0 is used, active video signal amplitude V_{ACT} should be: $V_{ACT} = \frac{(V_{REFH} - V_{REFL})}{\text{buffer gain factor}}$
5. Measurement carried out using video analyser VM700A, where the video analog signal is reconstructed through a digital-to-analog converter.
6. $V_{I(p-p)} = \Delta REF$ with $f_i = 4.43$ MHz.
7. The analog input settling time is the minimum time required for the input signal to be stabilized after a sharp full-scale input (square-wave signal) in order to sample the signal and obtain correct output data.
8. Output data acquisition: output data is available after the maximum delay time of t_d.

Table 1 Typical output coding (V_{REFH} = 2 V; V_{REFL} = 0.5 V referenced to V_{SSA}, SLT = logic 0; buffer ratio = 1.5; T_{amb} = 25°C)

STEP	$V_{I(p-p)}$	BINARY OUTPUT BITS					
		D5	D4	D3	D2	D1	D0
–	$<0.333 = \frac{V_{REFL}}{1.5}$	0	0	0	0	0	0
0	0.349	0	0	0	0	0	0
1	0.364	0	0	0	0	0	1
.	.	.		.	.	.	.
62	1.317	1	1	1	1	1	0
63	1.333	1	1	1	1	1	1
–	$>1.333 = \frac{V_{REFH}}{1.5}$	1	1	1	1	1	1

Table 2 Mode selection

SLT	BUFFER RATIO	TYPICAL $V_{I(p-p)}$ FULL SCALE
0	1.5	$\frac{V_{REFH} - V_{REFL}}{1.5}$
1	2.0	$\frac{V_{REFH} - V_{REFL}}{2.0}$

TIMING DIAGRAMS

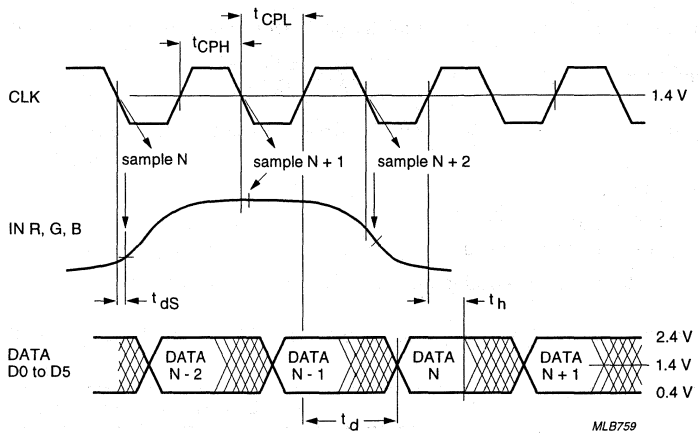


Fig.3 Input timing.

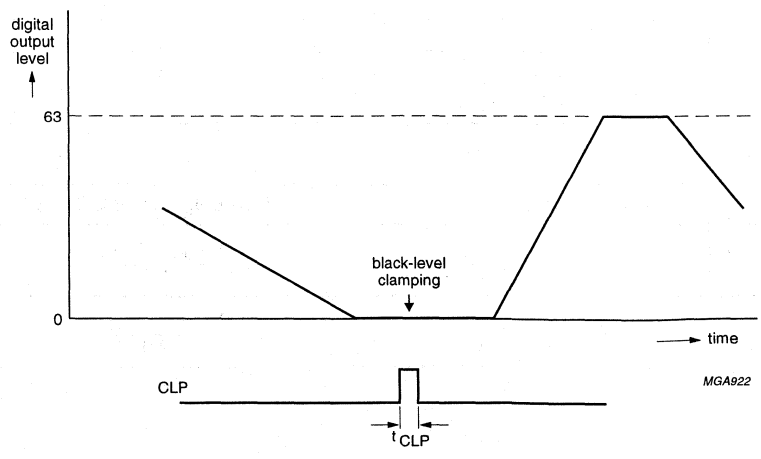


Fig.4 Clamp timing.

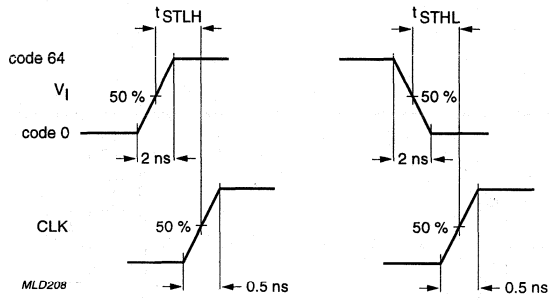
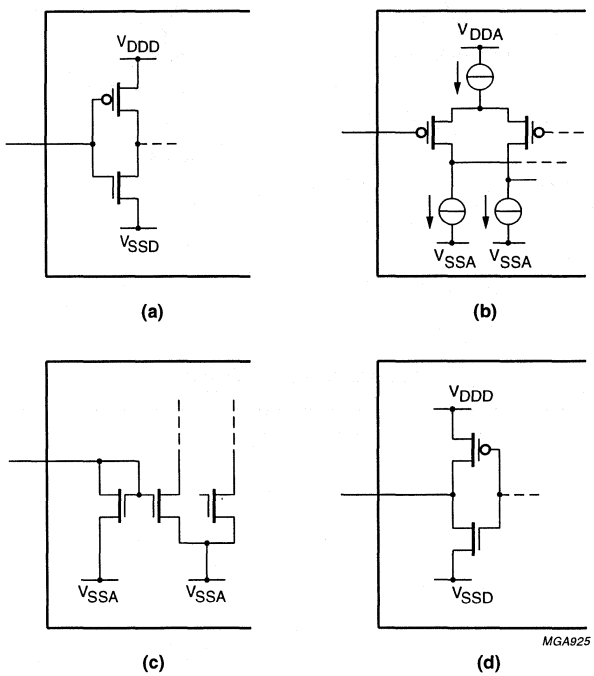


Fig.5 Analog input settling-time diagram.

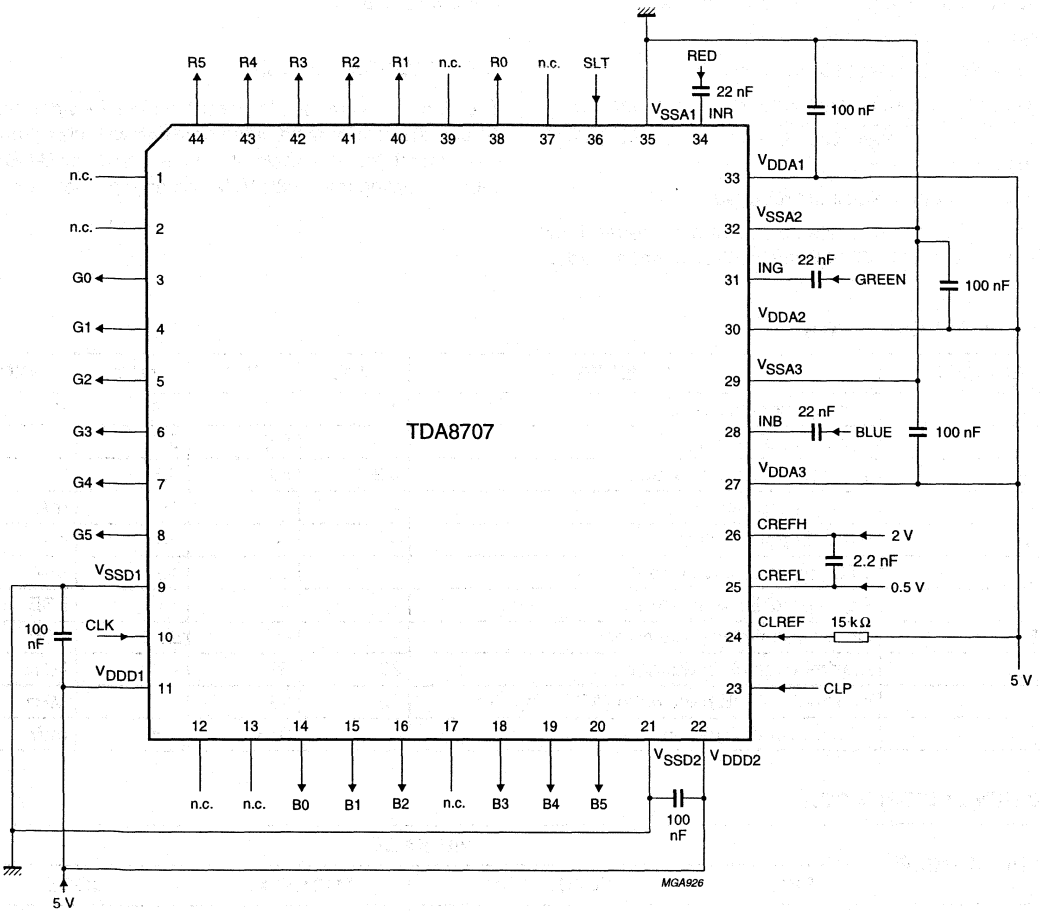
INTERNAL CIRCUITRY



(a) Digital inputs; pins 10, 23 and 36.
(b) Analog inputs; pins 28, 31 and 34.
(c) Current reference; pin 24.
(d) Digital outputs; pins 3 to 8, 14 to 16, 18 to 20 and 40 to 44.

Fig.6 Internal circuitry.

APPLICATION INFORMATION



Analog and digital supplies should be separated and decoupled.

Supplies are not connected internally; also applicable to grounds.

The internal reference currents are set by the series resistor between pin V_{DDA} and CLREF. The resistor value should be in the range of 12 kΩ and 15 kΩ.

It is recommended, if possible, to connect pins 1, 2, 12, 13, 17, 37 and 39 to V_{SSD}.

Fig.7 Application diagram.

Video analog input interface TDA8708A

FEATURES

- 8-bit resolution
- Sampling rate up to 32 MHz
- Binary or two's complement 3-state TTL outputs
- TTL-compatible digital inputs and outputs
- Internal reference voltage regulator
- Power dissipation of 365 mW (typical)
- Input selector circuit (one out of three video inputs)
- Clamp and Automatic Gain Control (AGC) functions for CVBS and Y signals
- No sample-and-hold circuit required.
- The TDA8708A has white peak control in modes 1 and 2 whereas the TDA8708B has control in mode 1 only.

APPLICATIONS

- Video signal decoding
- Scrambled TV (encoding and decoding)
- Digital picture processing
- Frame grabbing.

GENERAL DESCRIPTION

The TDA8708A is an analog input interface for video signal processing. It includes a video amplifier with clamp and gain control, an 8-bit analog-to-digital converter (ADC) with a sampling rate of 32 MHz and an input selector.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage	4.5	5.0	5.5	V
V_{CCD}	digital supply voltage	4.5	5.0	5.5	V
V_{CCO}	TTL output supply voltage	4.2	5.0	5.5	V
I_{CCA}	analog supply current	–	37	45	mA
I_{CCD}	digital supply current	–	24	30	mA
I_{CCO}	TTL output supply current	–	12	16	mA
ILE	DC integral linearity error	–	–	±1	LSB
DLE	DC differential linearity error	–	–	±0.5	LSB
$f_{clk(max)}$	maximum clock frequency	30	32	–	MHz
B	maximum –3 dB bandwidth (AGC amplifier)	12	18	–	MHz
P_{tot}	total power dissipation	–	365	500	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8708A	28	DIP	plastic	SOT117-1
TDA8708AT	28	SO28L	plastic	SOT136-1

BLOCK DIAGRAM

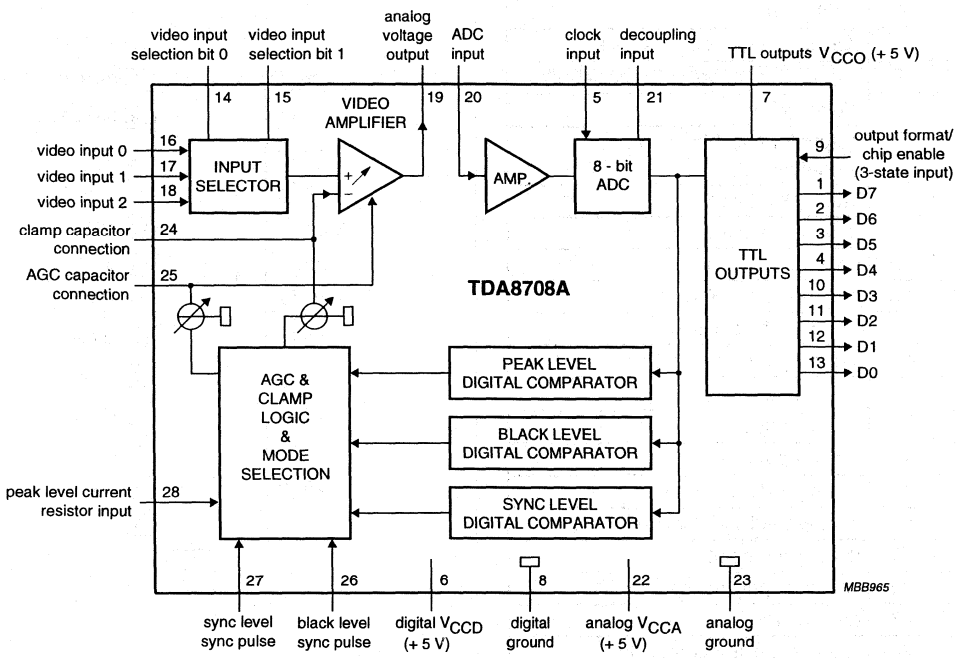


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
D7	1	data output; bit 7 (MSB)
D6	2	data output; bit 6
D5	3	data output; bit 5
D4	4	data output; bit 4
CLK	5	clock input
V_{CCD}	6	digital supply voltage (+5 V)
V_{CCO}	7	TTL outputs supply voltage (+5 V)
DGND	8	digital ground
OF	9	output format/chip enable (3-state input)
D3	10	data output; bit 3
D2	11	data output; bit 2
D1	12	data output; bit 1
D0	13	data output; bit 0 (LSB)
I0	14	video input selection bit 0
I1	15	video input selection bit 1
VIN0	16	video input 0
VIN1	17	video input 1
VIN2	18	video input 2
ANOUT	19	analog voltage output
ADCIN	20	analog-to-digital converter input
DEC	21	decoupling input
V_{CCA}	22	analog supply voltage (+5 V)
AGND	23	analog ground
CLAMP	24	clamp capacitor connection
AGC	25	AGC capacitor connection
GATE B	26	black level synchronization pulse
GATE A	27	sync level synchronization pulse
RPEAK	28	peak level current resistor input

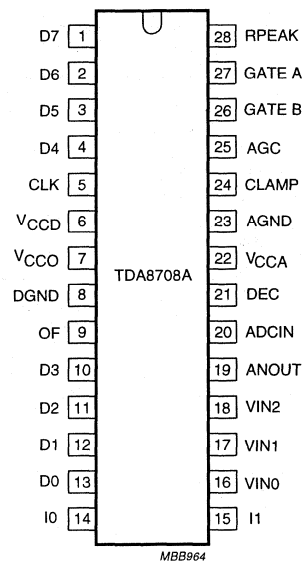


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA8708A provides a simple interface for decoding video signals.

The TDA8708A operates in configuration mode 1 (see Fig.4) when the video signals are weak (i.e. when the gain of the AGC amplifier has not yet reached its optimum value). This enables a fast recovery of the synchronization pulses in the decoder circuit. When the pulses at the GATE A and GATE B inputs become distinct (GATE A and GATE B pulses are synchronization pulses occurring during the sync period and rear porch respectively) the TDA8708A automatically switches to configuration mode 2 (see Fig.5).

When the TDA8708A is in configuration mode 1, the gain of the AGC amplifier will be roughly adjusted (sync level to a digital output level of 0 and the peak level to a digital output level of 255).

In configuration mode 2 the digital output of the ADC is compared to internal digital reference levels. The resultant outputs control the charge or discharge current of a capacitor connected to the AGC pin. The voltage across this capacitor controls the gain of the video amplifier. This is the gain control loop.

The sync level comparator is active during a positive-going pulse at the GATE A input. This means that the sync pulse of the composite video signal is used as an amplitude reference. The bottom of the sync pulse is adjusted to obtain a digital output of logic 0 at the converter output. As the black level is at digital level 64, the sync pulse will have a digital amplitude of 64 LSBs.

The peak-white control loop is always active. If the video signal tends to exceed the digital code of 248, the gain will be limited to avoid any over-range of the converter.

The use of nominal signals will prevent the output from exceeding a digital code of 213 and the peak-white control loop will be non-active.

The clamp level control is accomplished by using the same techniques as used for the gain control. The black-level digital comparator is active during a positive-going pulse at the GATE B input. The clamp capacitor will be charged or discharged to adjust the digital output to code 64.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage	−0.3	+7.0	V
V_{CCD}	digital supply voltage	−0.3	+7.0	V
V_{CCO}	output supply voltage	−0.3	+7.0	V
ΔV_{CC}	supply voltage difference between V_{CCA} and V_{CCD}	−1.0	+1.0	V
	supply voltage difference between V_{CCO} and V_{CCD}	−1.0	+1.0	V
	supply voltage difference between V_{CCA} and V_{CCO}	−1.0	+1.0	V
V_I	input voltage	−0.3	V_{CCA}	V
I_O	output current	0	+10	mA
T_{stg}	storage temperature	−55	+150	°C
T_{amb}	operating ambient temperature	0	+70	°C
T_j	junction temperature	0	+125	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	SOT117-1	55	K/W
	SOT136-1	70	K/W

CHARACTERISTICS

$V_{CCA} = V_{22}$ to V_{23} = 4.5 to 5.5 V; $V_{CCD} = V_6$ to V_8 = 4.5 to 5.5 V; $V_{CCO} = V_7$ to V_8 = 4.2 to 5.5 V; AGND and DGND shorted together; V_{CCA} to V_{CCD} = −0.5 to +0.5 V; V_{CCO} to V_{CCD} = −0.5 to +0.5 V; V_{CCA} to V_{CCO} = −0.5 to +0.5 V; T_{amb} = 0 to +70 °C; typical readings taken at $V_{CCA} = V_{CCD} = V_{CCO}$ = 5 V and T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
V_{CCO}	TTL output supply voltage		4.2	5.0	5.5	V
I_{CCA}	analog supply current		–	37	45	mA
I_{CCD}	digital supply current		–	24	30	mA
I_{CCO}	TTL output supply current	TTL load (see Fig.8)	–	12	16	mA
Video amplifier inputs						
VIN(0 TO 2) INPUTS						
$V_{I(p-p)}$	input voltage (peak-to-peak value)	AGC load with external capacitor; note 1	0.6	–	1.5	V
$\|Z_i\|$	input impedance	f_i = 6 MHz	10	20	–	kΩ
C_I	input capacitance	f_i = 6 MHz	–	1	–	pF
I0 AND I1 TTL INPUTS (SEE TABLE 1)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_I = 0.4 V	−400	–	–	µA
I_{IH}	HIGH level input current	V_I = 2.7 V	–	–	20	µA
GATE A AND GATE B TTL INPUTS (SEE FIGS 4 AND 5)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_I = 0.4 V	−400	–	–	µA
I_{IH}	HIGH level input current	V_I = 2.7 V	–	–	20	µA
t_W	pulse width	see Fig.5	2	–	–	µs
RPEAK INPUT (PIN 28)						
$I_{28(min)}$	minimum peak level current	R_{28} = 0 Ω	–	80	150	µA
AGC INPUT (PIN 25)						
$V_{25(min)}$	AGC voltage for minimum gain		–	2.8	–	V
$V_{25(max)}$	AGC voltage for maximum gain		–	4.0	–	V
	AGC output current		see Table 2			
CLAMP INPUT (PIN 24)						
V_{24}	clamp voltage for code 128 output		–	3.5	–	V
I_{24}	clamp output current		see Table 3			

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Video amplifier outputs						
ANOUT OUTPUT (PIN 19)						
$V_{19(p-p)}$	AC output voltage (peak-to-peak value)	V_{VIN} = 1.33 V (p-p); V_{25} = 3.6 V	–	1.33	–	V
I_{19}	internal current source	$R_L = \infty$	2.0	2.5	–	mA
$I_{O(p-p)}$	output current driven by the load	V_{ANOUT} = 1.33 V (p-p); note 2	–	–	1.0	mA
V_{19}	DC output voltage for black level	note 3	–	V_{CCA} – 2.24	–	V
Z_{19}	output impedance		–	20	–	Ω
Video amplifier dynamic characteristics						
α_{ct}	crosstalk between VIN inputs	V_{CCA} = 4.75 to 5.25 V	–	–50	–45	dB
G_{diff}	differential gain	V_{VIN} = 1.33 V (p-p); V_{25} = 3.6 V	–	2	–	%
φ_{diff}	differential phase	V_{VIN} = 1.33 V (p-p); V_{25} = 3.6 V	–	0.8	–	deg
B	–3 dB bandwidth		12	–	–	MHz
S/N	signal-to-noise ratio	note 4	60	–	–	dB
SVRR1	supply voltage ripple rejection	note 5	–	45	–	dB
ΔG	gain range	see Fig.10	–4.5	–	+6.0	dB
G_{stab}	gain stability as a function of supply voltage and temperature	see Fig.10	–	–	5	%
Analog-to-digital converter inputs						
CLK INPUT (PIN 5)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_{clk} = 0.4 V	–400	–	–	μA
I_{IH}	HIGH level input current	V_{clk} = 2.7 V	–	–	100	μA
$\|Z_i\|$	input impedance	f_{clk}= 10 MHz	–	4	–	kΩ
C_I	input capacitance	f_{clk} = 10 MHz	–	4.5	–	pF
OF INPUT (3-STATE; SEE TABLE 4)						
V_{IL}	LOW level input voltage		0	–	0.2	V
V_{IH}	HIGH level input voltage		2.6	–	V_{CCD}	V
V_9	input voltage in high impedance state		–	1.15	–	V
I_{IL}	LOW level input current		–370	–300	–	μA
I_{IH}	HIGH level input current		–	300	450	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ADCIN INPUT (PIN 20; SEE TABLE 5)						
V_{20}	input voltage	digital output = 00	–	V_{CCA} – 2.42	–	V
V_{20}	input voltage	digital output = 255	–	V_{CCA} – 1.41	–	V
$V_{20(p-p)}$	input voltage amplitude (peak-to-peak value)		–	1.0	–	V
I_{20}	input current		–	1.0	10	μA
$\|Z_i\|$	input impedance	f_i = 6 MHz	–	50	–	MΩ
C_I	input capacitance	f_i = 6 MHz	–	1	–	pF
Analog-to-digital converter outputs						
DIGITAL OUTPUTS D0 TO D7						
V_{OL}	LOW level output voltage	I_{OL} = 2 mA	0	–	0.6	V
V_{OH}	HIGH level output voltage	I_{OL} = –0.4 mA	2.4	–	V_{CCD}	V
I_{OZ}	output current in 3-state mode	0.4 V < V_O < V_{CCD}	–20	–	+20	μA
Switching characteristics						
$f_{clk(max)}$	maximum clock input frequency	see Fig.6; note 6	30	32	–	MHz
Analog signal processing (f_{clk} = 32 MHz; see Fig.8)						
G_{diff}	differential gain	V_{20} = 1.0 V (p-p); see Fig.3; note 7	–	2	–	%
φ_{diff}	differential phase	see Fig.3; note 7	–	2	–	deg
f_1	fundamental harmonics (full-scale)	f_i = 4.43 MHz; note 7	–	–	0	dB
f_{all}	harmonics (full-scale); all components	f_i = 4.43 MHz; note 7	–	–55	–	dB
SVRR2	supply voltage ripple rejection	note 8	–	1	5	%/V
Transfer function (see Fig.8)						
ILE	DC integral linearity error		–	–	±1	LSB
DLE	DC differential linearity error		–	–	±0.5	LSB
ILE	AC integral linearity error	note 9	–	–	±2	LSB
Timing (f_{clk} = 32 MHz; see Figs 6, 7 and 8)						
DIGITAL OUTPUTS (C_L = 15 pF; I_{OL} = 2 mA; R_L = 2 kΩ)						
t_{ds}	sampling delay time		–	2	–	ns
t_h	output hold time		6	8	–	ns
t_d	output delay time		–	16	20	ns
t_{dEZ}	3-state delay time; output enable		–	19	25	ns
t_{dDZ}	3-state delay time; output disable		–	14	20	ns

Notes

1. 0 dB is obtained at the AGC amplifier when applying $V_{i(p-p)}$ = 1.33 V.
2. The output current at pin 19 should not exceed 1 mA. The load impedance R_L should be referenced to V_{CCA} and defined as:
   a) AC impedance ≥1 kΩ and the DC impedance >2.7 kΩ.
   b) The load impedance should be coupled directly to the output of the amplifier so that the DC voltage supplied by the clamp is not disturbed.
3. Control mode 2 is selected.
4. Signal-to-noise ratio measured with 5 MHz bandwidth:

   $$\frac{S}{N} = 20 \log \frac{V_{ANOUTC(p-p)}}{V_{ANOUTY\ (RMS\ noise)}} \text{ at } B = 5 \text{ MHz.}$$

5. The voltage ratio is expressed as:

   $$SVRR1 = 20 \log \frac{\Delta V_{CCA}}{V_{CCA}} \times \frac{G}{\Delta G}$$ for V_I = 1 V (p-p), gain at 100 kHz = 1 and 1 V supply variation.

6. It is recommended that the rise and fall times of the clock are ≥2 ns. In addition, a 'good layout' for the digital and analog grounds is recommended.
7. These measurements are realized on analog signals after a digital-to-analog conversion (TDA8702 is used).
8. The supply voltage rejection is the relative variation of the analog signal (full-scale signal at input) for 1 V of supply variation:

   $$SVRR2 = \frac{\Delta (V_{I(00)} - V_{I(FF)}) + (V_{I(00)} - V_{I(FF)})}{\Delta V_{CCA}}$$

9. Full-scale sine wave (f_i = 4.4 MHz; f_{clk} = 27 MHz).

Table 1 Video input selection (CVBS).

I1	I0	SELECTED INPUT
0	0	VIN0
0	1	VIN1
1	0	VIN2
1	1	VIN2

Table 2 AGC output current.

GATE A	GATE B	DIGITAL OUTPUT	I_{AGC}	MODE(2)
1	1	output < 255	−2.5 µA	1
		output > 255	I_{AGCM}	1
0	X(1)	output < 248	0 µA	2
		output > 248	I_{AGCM}	2
1	0	output < 0	+2.5 µA	2
		0 < output < 248	−2.5 µA	2
		output > 248	I_{AGCM}	2

Note

1. X = don't care.
2. Mode 2 can only be initialized with successive pulses on GATE A and GATE B (see Fig.5).

Table 3 CLAMP output current.

GATE A	GATE B	DIGITAL OUTPUT	I_{CLAMP}	MODE
1	1	output < 0	I_{CLAMPM}	1
		output > 0	−2.5 µA	1
X(1)	0	X(1)	0 µA	2
0	1	output < 64	+50 µA	2
		64 < output	−50 µA	2

Note

1. X = don't care.

Table 4 OF input coding.

OF	D0 TO D7
0	active, two's complement
1	high impedance
open circuit(1)	active, binary

Note

1. Use C ≥ 10 pF to DGND.

Table 5 Output coding and input voltage (typical values).

STEP	V_{ADCIN}	BINARY OUTPUTS								TWO'S COMPLEMENT							
		D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Underflow	–	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0	V_{CCA} − 2.41 V	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	–	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1
.	–	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	–	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
254	–	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0
255	V_{CCA} − 1.41 V	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
Overflow	–	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1

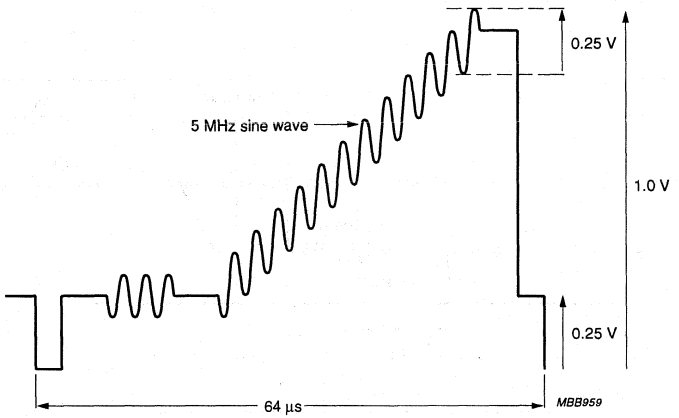


Fig.3 Test signal on the ADCIN pin for differential gain and phase measurements.

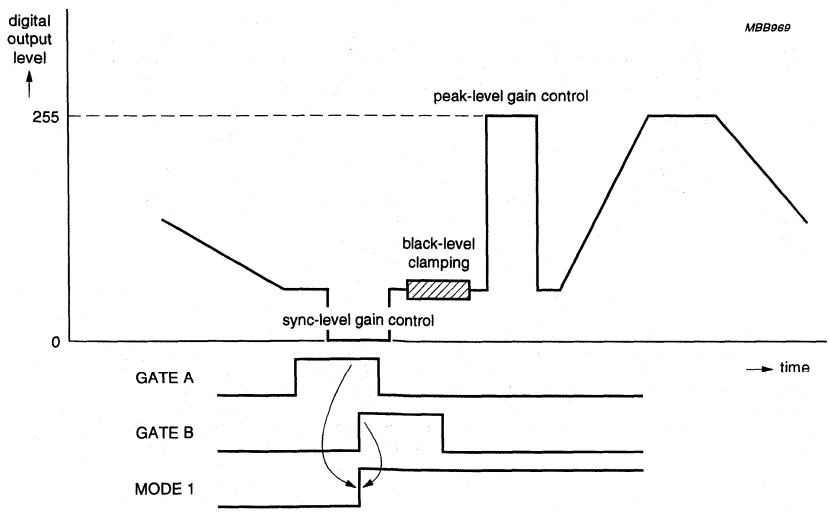


Fig.4 Control mode 1.

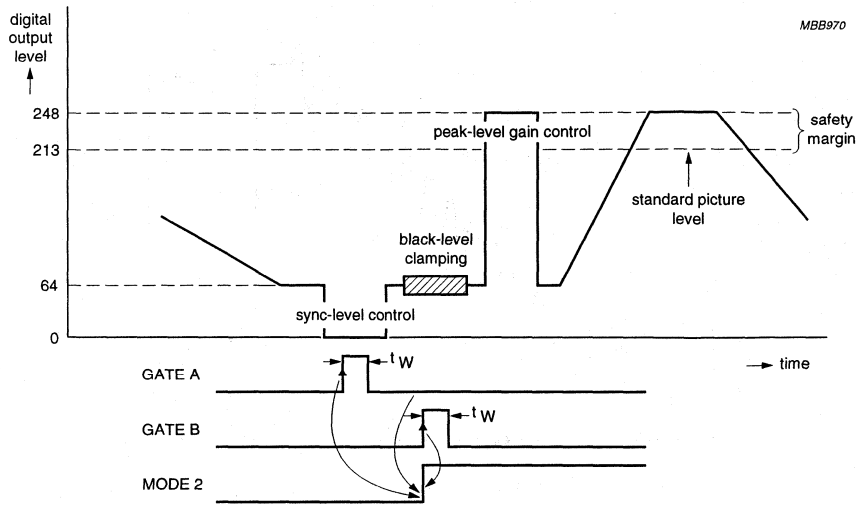


Fig.5 Control mode 2.

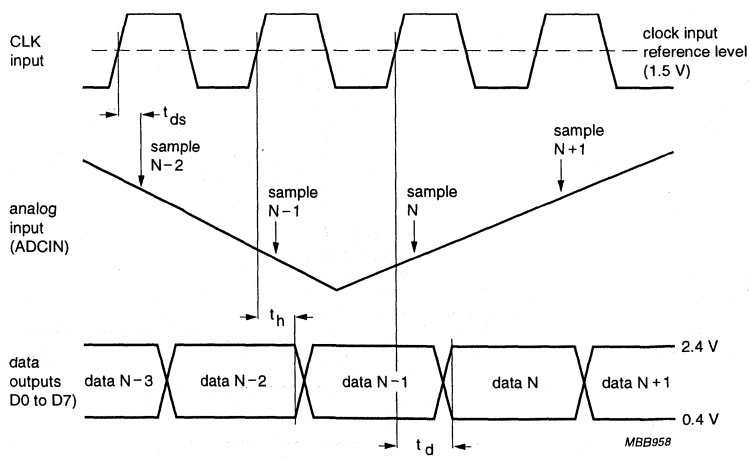


Fig.6 Timing diagram for data output.

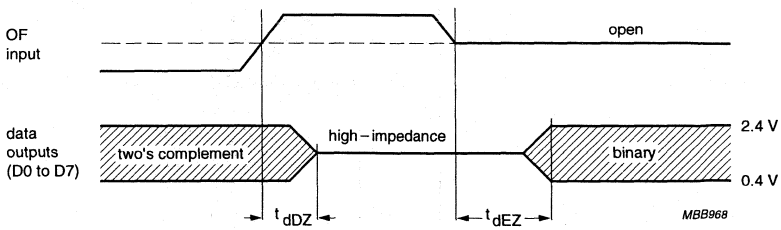


Fig.7 Output format timing diagram.

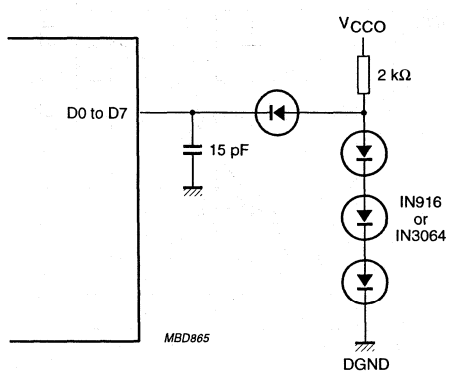


Fig.8 Load circuit for timing measurement; data outputs (OF = LOW or open-circuit).

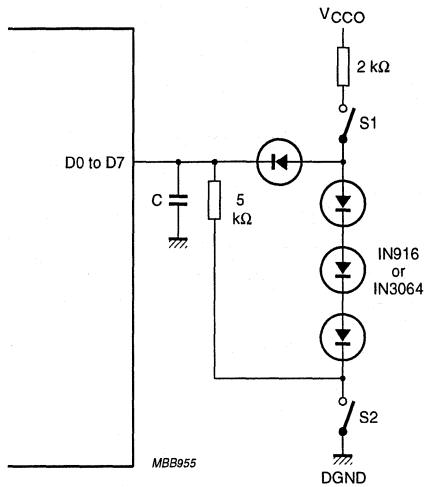
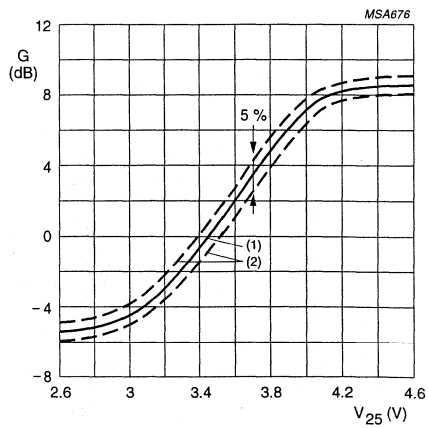


Fig.9 Load circuit for timing measurement; 3-state outputs (OF: f_i = 1 MHz; V_{OF} = 3 V).



(1) Typical value (V_{CCA} = V_{CCD} = 5 V; T_{amb} = 25 °C).
(2) Minimum and maximum values (temperature and supply).

Fig.10 Gain control curve.

INTERNAL PIN CIRCUITRY

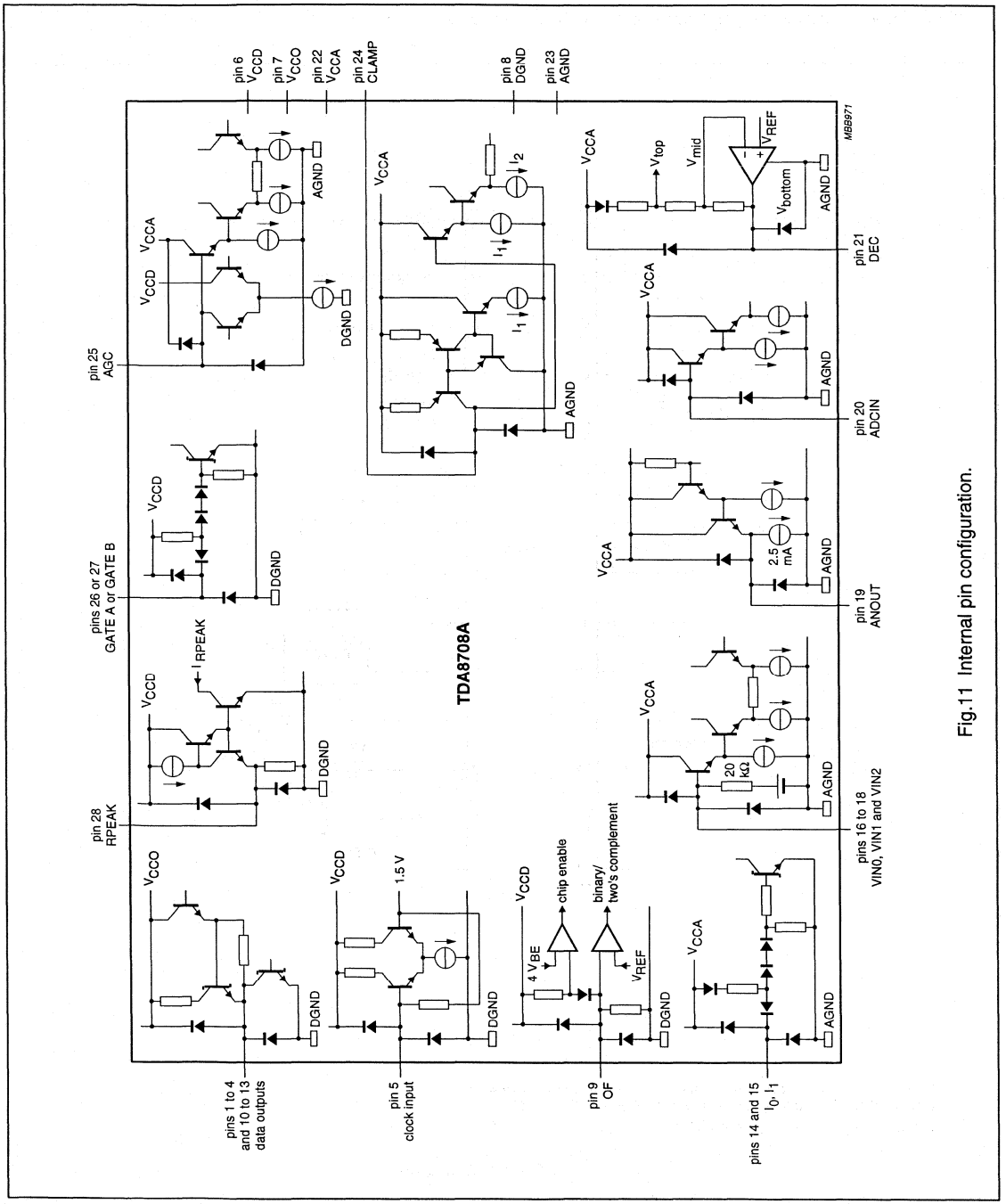
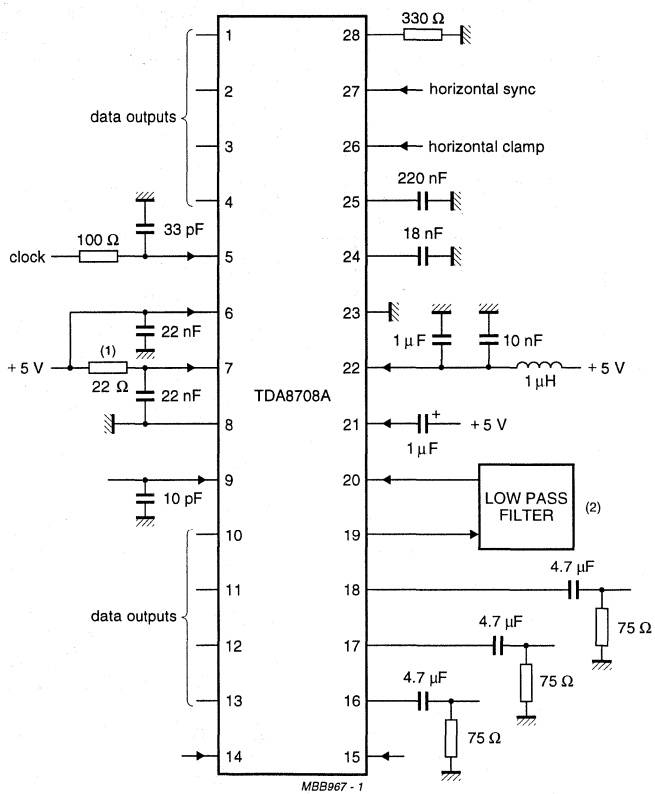


Fig.11 Internal pin configuration.

APPLICATION INFORMATION

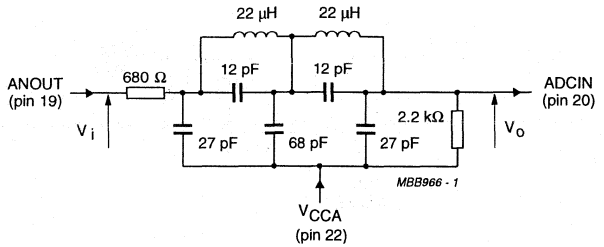
Additional information can be found in the laboratory report *"FBL/AN9308"*.



(1) It is recommended to decouple V_{CCO} through a 22 Ω resistor especially when the output data of TDA8708A interfaces with a capacitive CMOS load device.

(2) See Figs 13 and 15 for examples of the low-pass filters.

Fig.12 Application diagram.



This filter can be adapted to various applications with respect to performance requirements. An input and output impedance of at least 680 Ω and 2.2 kΩ must in any event be applied.

Fig.13 Example of a low-pass filter for CVBS and Y signals.

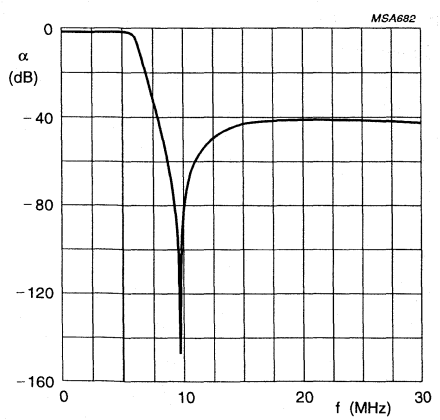
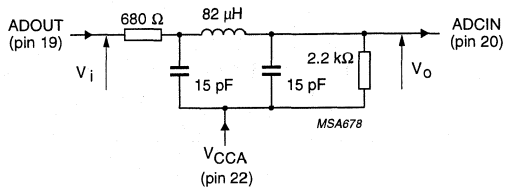


Fig.14 Frequency response for filter shown in Fig.13.

Characteristics of Fig. 13

- Order 5; adapted CHEBYSHEV
- Ripple $\rho \leq 0.4$ dB
- f = 6.5 MHz at −3 dB
- f_{notch} = 9.75 MHz.



This filter can be adapted to various applications with respect to performance requirements. An input and output impedance of at least 680 Ω and 2.2 kΩ must in any event be applied.

Fig.15 Example of an economical low-pass filter for CVBS and Y signals.

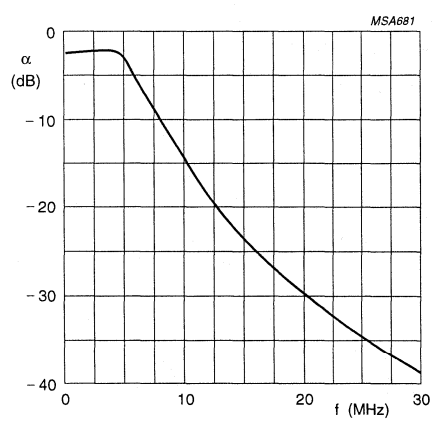


Fig.16 Frequency response for filter shown in Fig.15.

Characteristics of Fig. 15

- Order 5; adapted CHEBYSHEV
- Ripple $\rho \leq 0.4$ dB
- f = 6.5 MHz at –3 dB.

Video analog input interface TDA8708B

FEATURES

- 8-bit resolution
- Sampling rate up to 32 MHz
- Binary or two's complement 3-state TTL outputs
- TTL-compatible digital inputs and outputs
- Internal reference voltage regulator
- Power dissipation of 365 mW (typical)
- Input selector circuit (one out of three video inputs)
- Clamp and Automatic Gain Control (AGC) functions for CVBS and Y signals
- No sample-and-hold circuit required
- The TDA8708B has no white peak control in mode 2 whereas the TDA8708A has control in modes 1 and 2.
- In-range output (not TTL levels).

APPLICATIONS

- Video signal decoding
- Scrambled TV (encoding and decoding)
- Digital picture processing
- Frame grabbing.

GENERAL DESCRIPTION

The TDA8708B is an analog input interface for video signal processing. It includes a video amplifier with clamp and gain control, an 8-bit analog-to-digital converter (ADC) with a sampling rate of 32 MHz and an input selector.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage	4.5	5.0	5.5	V
V_{CCD}	digital supply voltage	4.5	5.0	5.5	V
V_{CCO}	TTL output supply voltage	4.2	5.0	5.5	V
I_{CCA}	analog supply current	–	37	45	mA
I_{CCD}	digital supply current	–	24	30	mA
I_{CCO}	TTL output supply current	–	12	16	mA
ILE	DC integral linearity error	–	–	±1	LSB
DLE	DC differential linearity error	–	–	±0.5	LSB
$f_{clk(max)}$	maximum clock frequency	30	32	–	MHz
B	maximum –3 dB bandwidth (AGC amplifier)	12	18	–	MHz
P_{tot}	total power dissipation	–	365	500	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8708B	28	DIP	plastic	SOT117-1
TDA8708BT	28	SO28L	plastic	SOT136-1

BLOCK DIAGRAM

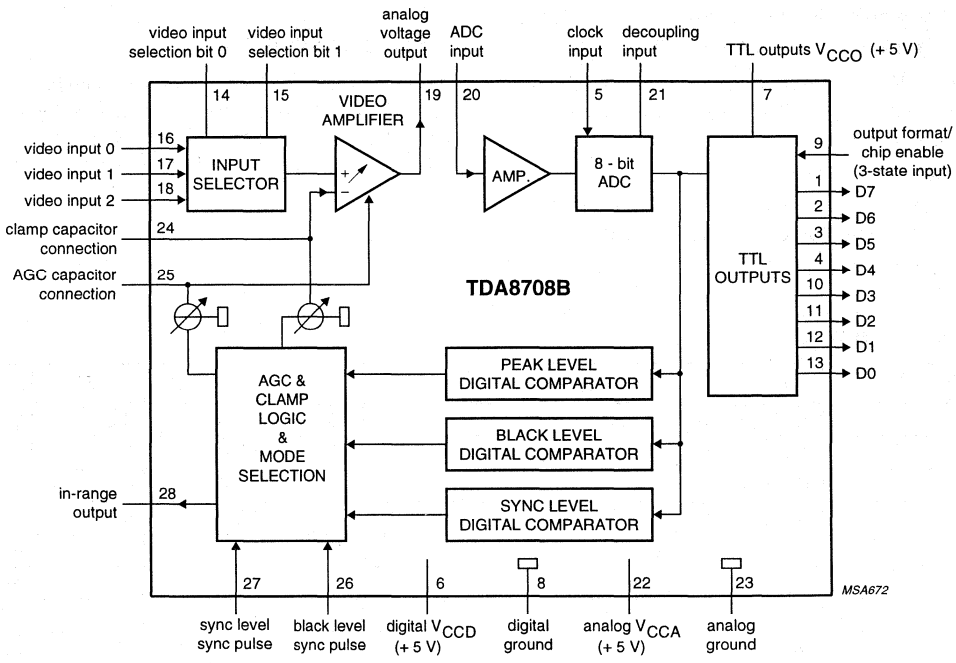


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
D7	1	data output; bit 7 (MSB)
D6	2	data output; bit 6
D5	3	data output; bit 5
D4	4	data output; bit 4
CLK	5	clock input
V_{CCD}	6	digital supply voltage (+5 V)
V_{CCO}	7	TTL outputs supply voltage (+5 V)
DGND	8	digital ground
OF	9	output format/chip enable (3-state input)
D3	10	data output; bit 3
D2	11	data output; bit 2
D1	12	data output; bit 1
D0	13	data output; bit 0 (LSB)
I0	14	video input selection bit 0
I1	15	video input selection bit 1
VIN0	16	video input 0
VIN1	17	video input 1
VIN2	18	video input 2
ANOUT	19	analog voltage output
ADCIN	20	analog-to-digital converter input
DEC	21	decoupling input
V_{CCA}	22	analog supply voltage (+5 V)
AGND	23	analog ground
CLAMP	24	clamp capacitor connection
AGC	25	AGC capacitor connection
GATE B	26	black level synchronization pulse
GATE A	27	sync level synchronization pulse
IR	28	in-range output

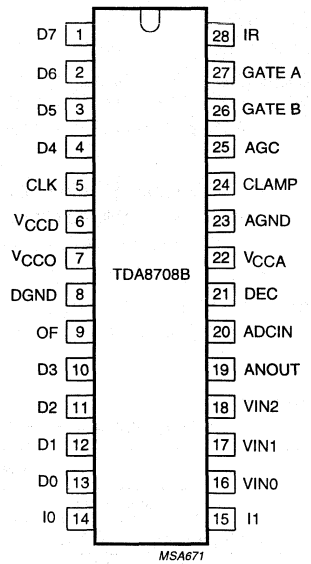


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA8708B provides a simple interface for decoding video signals.

The TDA8708B operates in configuration mode 1 (see Fig.4) when the video signals are weak (i.e. when the gain of the AGC amplifier has not yet reached its optimum value). This enables a fast recovery of the synchronization pulses in the decoder circuit. When the pulses at the GATE A and GATE B inputs become distinct (GATE A and GATE B pulses are synchronization pulses occurring during the sync period and rear porch respectively) the TDA8708B automatically switches to configuration mode 2 (see Fig.5).

When the TDA8708B is in configuration mode 1, the gain of the AGC amplifier will be roughly adjusted (sync level to a digital output level of 0 and the peak level to a digital output level of 255).

In configuration mode 2 the digital output of the ADC is compared to internal digital reference levels. The voltage across the capacitor connected to the AGC pin controls the gain of the video amplifier. This is the gain control loop.

The sync level comparator is active during a positive-going pulse at the GATE A input. This means that the sync pulse of the composite video signal is used as an amplitude reference. The bottom of the sync pulse is adjusted to obtain a digital output of logic 0 at the converter output. As the black level is at digital level 64, the sync pulse will have a digital amplitude of 64 LSBs.

The use of nominal signals will prevent the output from exceeding a digital code of 213.

The clamp level control is accomplished by using the same techniques as used for the gain control. The black-level digital comparator is active during a positive-going pulse at the GATE B input. The clamp capacitor will be charged or discharged to adjust the digital output to code 64.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage	−0.3	+7.0	V
V_{CCD}	digital supply voltage	−0.3	+7.0	V
V_{CCO}	TTL output supply voltage	−0.3	+7.0	V
ΔV_{CC}	supply voltage difference between V_{CCA} and V_{CCD}	−1.0	+1.0	V
	supply voltage difference between V_{CCO} and V_{CCD}	−1.0	+1.0	V
	supply voltage difference between V_{CCA} and V_{CCO}	−1.0	+1.0	V
V_I	input voltage	−0.3	V_{CCA}	V
I_O	output current	0	+10	mA
T_{stg}	storage temperature	−55	+150	°C
T_{amb}	operating ambient temperature	0	+70	°C
T_j	junction temperature	0	+125	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	SOT117-1	55	K/W
	SOT136-1	70	K/W

CHARACTERISTICS

$V_{CCA} = V_{22}$ to $V_{23} = 4.5$ to 5.5 V; $V_{CCD} = V_6$ to $V_8 = 4.5$ to 5.5 V; $V_{CCO} = V_7$ to $V_8 = 4.2$ to 5.5 V; AGND and DGND shorted together; V_{CCA} to $V_{CCD} = -0.5$ to +0.5 V; V_{CCO} to $V_{CCD} = -0.5$ to +0.5 V; V_{CCA} to $V_{CCO} = -0.5$ to +0.5 V; $T_{amb} = 0$ to +70 °C; typical readings taken at $V_{CCA} = V_{CCD} = V_{CCO} = 5$ V and $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
V_{CCO}	TTL output supply voltage		4.2	5.0	5.5	V
I_{CCA}	analog supply current		–	37	45	mA
I_{CCD}	digital supply current		–	24	30	mA
I_{CCO}	TTL output supply current	TTL load (see Fig.8)	–	12	16	mA
Video amplifier inputs						
VIN0 TO VIN2 INPUTS						
$V_{I(p-p)}$	input voltage (peak-to-peak value)	AGC load with external capacitor; note 1	0.6	–	1.5	V
$\|Z_i\|$	input impedance	$f_i = 6$ MHz	10	20	–	kΩ
C_I	input capacitance	$f_i = 6$ MHz	–	1	–	pF
I0 AND I1 TTL INPUTS (SEE TABLE 1)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	$V_I = 0.4$ V	–400	–	–	µA
I_{IH}	HIGH level input current	$V_I = 2.7$ V	–	–	20	µA
GATE A AND GATE B TTL INPUTS (SEE FIGS 4 AND 5)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	$V_I = 0.4$ V	–400	–	–	µA
I_{IH}	HIGH level input current	$V_I = 2.7$ V	–	–	20	µA
t_W	pulse width	see Fig.5	2	–	–	µs
AGC INPUT (PIN 25)						
$V_{25(min)}$	AGC voltage for minimum gain		–	2.8	–	V
$V_{25(max)}$	AGC voltage for maximum gain		–	4.0	–	V
	AGC output current		see Table 2			
CLAMP INPUT (PIN 24)						
V_{24}	clamp voltage for code 128 output		–	3.5	–	V
I_{24}	clamp output current		see Table 3			

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Video amplifier outputs						
ANOUT OUTPUT (PIN 19)						
$V_{19(p-p)}$	AC output voltage (peak-to-peak value)	V_{VIN} = 1.33 V (p-p); V_{25} = 3.6 V	–	1.33	–	V
I_{19}	internal current source	$R_L = \infty$	2.0	2.5	–	mA
$I_{O(p-p)}$	output current driven by the load	V_{ANOUT} = 1.33 V (p-p); note 2	–	–	1.0	mA
V_{19}	DC output voltage for black level	note 3	–	V_{CCA} – 2.24	–	V
Z_{19}	output impedance		–	20	–	Ω
Video amplifier dynamic characteristics						
α_{ct}	crosstalk between VIN inputs	V_{CCA} = 4.75 to 5.25 V	–	–50	–45	dB
G_{diff}	differential gain	V_{VIN} = 1.33 V (p-p); V_{25} = 3.6 V	–	2	–	%
φ_{diff}	differential phase	V_{VIN} = 1.33 V (p-p); V_{25} = 3.6 V	–	0.8	–	deg
B	–3 dB bandwidth		12	–	–	MHz
S/N	signal-to-noise ratio	note 4	60	–	–	dB
SVRR1	supply voltage ripple rejection	note 5	–	45	–	dB
ΔG	gain range	see Fig.10	–4.5	–	+6.0	dB
G_{stab}	gain stability as a function of supply voltage and temperature	see Fig.10	–	–	5	%
Analog-to-digital converter inputs						
CLK INPUT (PIN 5)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_{clk} = 0.4 V	–400	–	–	μA
I_{IH}	HIGH level input current	V_{clk} = 2.7 V	–	–	100	μA
$\lvert Z_i \rvert$	input impedance	f_{clk} = 10 MHz	–	4	–	kΩ
C_I	input capacitance	f_{clk} = 10 MHz	–	4.5	–	pF
OF INPUT (3-STATE; SEE TABLE 4)						
V_{IL}	LOW level input voltage		0	–	0.2	V
V_{IH}	HIGH level input voltage		2.6	–	V_{CCD}	V
V_9	input voltage in high impedance state		–	1.15	–	V
I_{IL}	LOW level input current		–370	–300	–	μA
I_{IH}	HIGH level input current		–	300	450	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ADCIN INPUT (PIN 20; SEE TABLE 5)						
V_{20}	input voltage	digital output = 00	–	V_{CCA} – 2.42	–	V
V_{20}	input voltage	digital output = 255	–	V_{CCA} – 1.41	–	V
$V_{20(p-p)}$	input voltage amplitude (peak-to-peak value)		–	1.0	–	V
I_{20}	input current		–	1.0	10	μA
$\|Z_i\|$	input impedance	f_i = 6 MHz	–	50	–	MΩ
C_I	input capacitance	f_i = 6 MHz	–	1	–	pF
Analog-to-digital converter outputs						
IR OUTPUT (PIN 28)						
V_{OL}	LOW level output voltage		–	–	1.7	V
V_{OH}	HIGH level output voltage		1.9	–	–	V
I_O	output current		–500	–	–	μA
DIGITAL OUTPUTS D0 TO D7						
V_{OL}	LOW level output voltage	I_{OL} = 2 mA	0	–	0.6	V
V_{OH}	HIGH level output voltage	I_{OL} = –0.4 mA	2.4	–	V_{CCD}	V
I_{OZ}	output current in 3-state mode	0.4 V < V_O < V_{CCD}	–20	–	+20	μA
Switching characteristics						
$f_{clk(max)}$	maximum clock input frequency	see Fig.6; note 6	30	32	–	MHz
Analog signal processing (f_{clk} = 32 MHz; see Fig.8)						
G_{diff}	differential gain	V_{20} = 1.0 V (p-p); see Fig.7; note 7	–	2	–	%
φ_{diff}	differential phase	see Fig.7; note 7	–	2	–	deg
f_1	fundamental harmonics (full-scale)	f_i = 4.43 MHz; note 7	–	–	0	dB
f_{all}	harmonics (full-scale); all components	f_i = 4.43 MHz; note 7	–	–55	–	dB
SVRR2	supply voltage ripple rejection	note 8	–	1	5	%/V
Transfer function (see Fig.8)						
ILE	DC integral linearity error		–	–	±1	LSB
DLE	DC differential linearity error		–	–	±0.5	LSB
ILE	AC integral linearity error	note 9	–	–	±2	LSB
Timing (f_{clk} = 32 MHz; see Figs 6, 7 and 8)						
DIGITAL OUTPUTS (C_L = 15 pF; I_{OL} = 2 mA; R_L = 2 kΩ)						
t_{ds}	sampling delay time		–	2	–	ns
t_h	output hold time		6	8	–	ns
t_d	output delay time		–	16	20	ns
t_{dEZ}	3-state delay time; output enable		–	19	25	ns
t_{dDZ}	3-state delay time; output disable		–	14	20	ns

Notes to the "Characteristics"

1. 0 dB is obtained at the AGC amplifier when applying $V_{i(p-p)}$ = 1.33 V.
2. The output current at pin 19 should not exceed 1 mA. The load impedance R_L should be referenced to V_{CCA} and defined as:
   a) AC impedance ≥1 kΩ and the DC impedance >2.7 kΩ.
   b) The load impedance should be coupled directly to the output of the amplifier so that the DC voltage supplied by the clamp is not disturbed.
3. Control mode 2 is selected.
4. Signal-to-noise ratio measured with 5 MHz bandwidth:

   $$\frac{S}{N} = 20 \log \frac{V_{ANOUTC\,(p-p)}}{V_{ANOUTY\,(RMS\ noise)}}$$ at B = 5 MHz.

5. The voltage ratio is expressed as:

   $$SVRR1 = 20 \log \frac{\Delta V_{CCA}}{V_{CCA}} \times \frac{G}{\Delta G}$$ for V_I = 1 V (p-p), gain at 100 kHz = 1 and 1 V supply variation.

6. It is recommended that the rise and fall times of the clock are ≥2 ns. In addition, a 'good layout' for the digital and analog grounds is recommended.
7. These measurements are realized on analog signals after a digital-to-analog conversion (TDA8702 is used).
8. The supply voltage rejection is the relative variation of the analog signal (full-scale signal at input) for 1 V of supply variation:

   $$SVRR2 = \frac{\Delta (V_{I(00)} - V_{I(FF)}) + (V_{I(00)} - V_{I(FF)})}{\Delta V_{CCA}}$$

9. Full-scale sine wave (f_i = 4.4 MHz; f_{clk} = 27 MHz).

Table 1 Video input selection (CVBS).

I1	I0	SELECTED INPUT
0	0	VIN0
0	1	VIN1
1	0	VIN2
1	1	VIN2

Table 2 AGC output current.

GATE A	GATE B	DIGITAL OUTPUT	I_{AGC}	MODE(2)
1	1	output < 255	−2.5 μA	1
		output > 255	130 μA	1
0	X(1)	–	0 μA	2
1	0	output < 0	+2.5 μA	2
		output > 0	−2.5 μA	2

Notes

1. X = don't care.
2. Mode 2 can only be initialized with successive pulses on GATE A and GATE B (see Fig.5).

Table 3 CLAMP output current.

GATE A	GATE B	DIGITAL OUTPUT	I_{CLAMP}	MODE
1	1	output < 0	130 μA	1
		output > 0	−2.5 μA	1
X(1)	0	X	0 μA	2
0	1	output < 64	+50 μA	2
		64 < output	−50 μA	2

Note

1. X = don't care.

Table 4 OF input coding.

OF	D0 TO D7
0	active, two's complement
1	high impedance
open circuit(1)	active, binary

Note

1. Use C ≥ 10 pF to DGND.

Table 5 Output coding and input voltage (typical values).

STEP	V_{ADCIN}	BINARY OUTPUTS								TWO'S COMPLEMENT							
		D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Underflow	–	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0	V_{CCA} − 2.41 V	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	–	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1
.	–	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	–	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
254	–	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0
255	V_{CCA} − 1.41 V	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
Overflow	–	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1

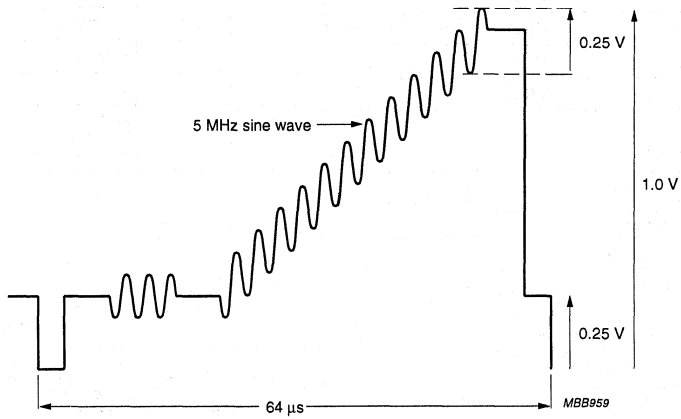


Fig.3 Test signal on the ADCIN pin for differential gain and phase measurements.

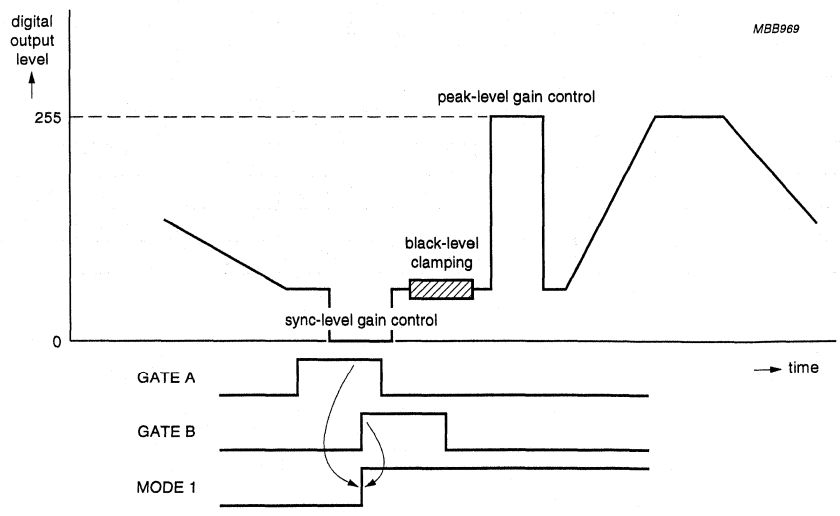


Fig.4 Control mode 1.

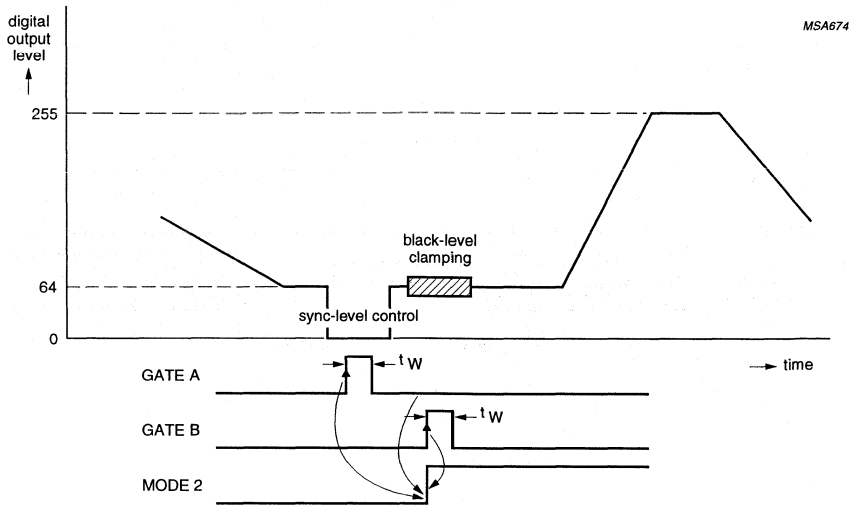


Fig.5 Control mode 2.

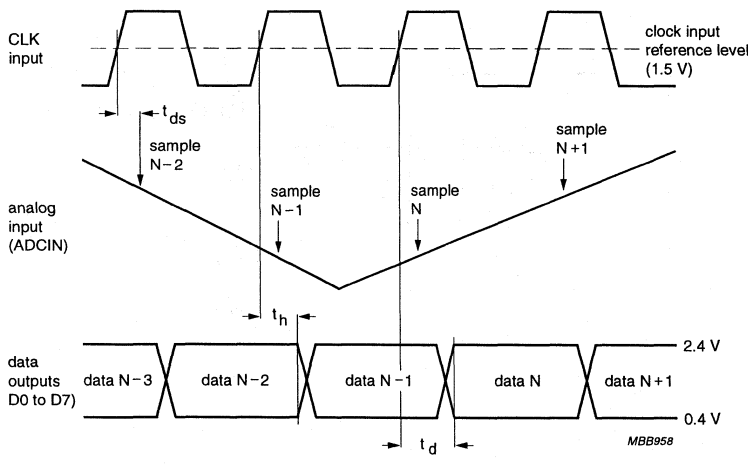


Fig.6 Timing diagram for data output.

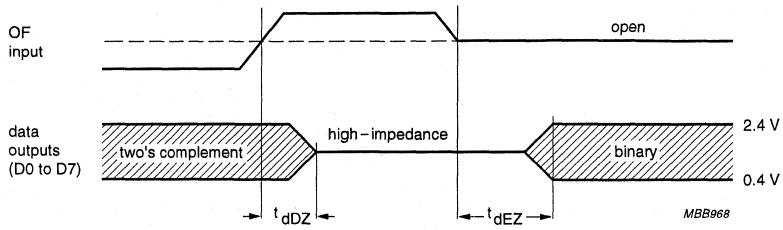


Fig.7 Output format timing diagram.

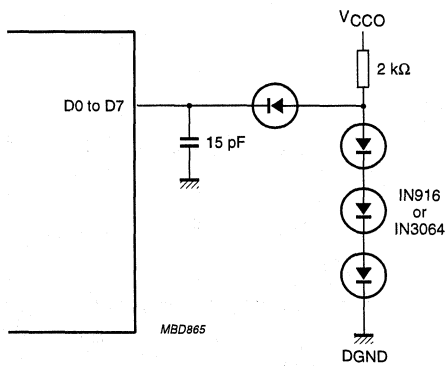


Fig.8 Load circuit for timing measurement; data outputs (OF = LOW or open-circuit).

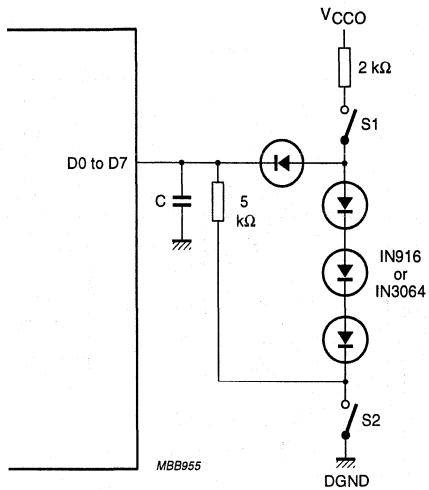
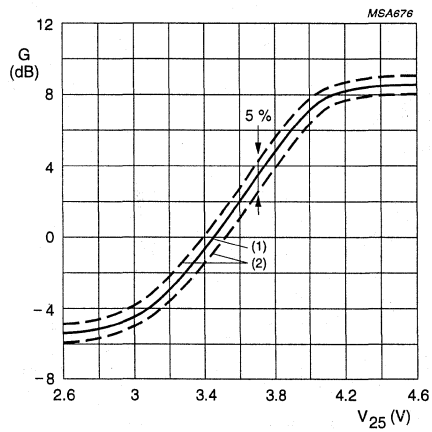


Fig.9 Load circuit for timing measurement; 3-state outputs (OF: f_i = 1 MHz; V_{OF} = 3 V).



(1) Typical value (V_{CCA} = V_{CCD} = 5 V; T_{amb} = 25 °C).
(2) Minimum and maximum values (temperature and supply).

Fig.10 Gain control curve.

INTERNAL PIN CIRCUITRY

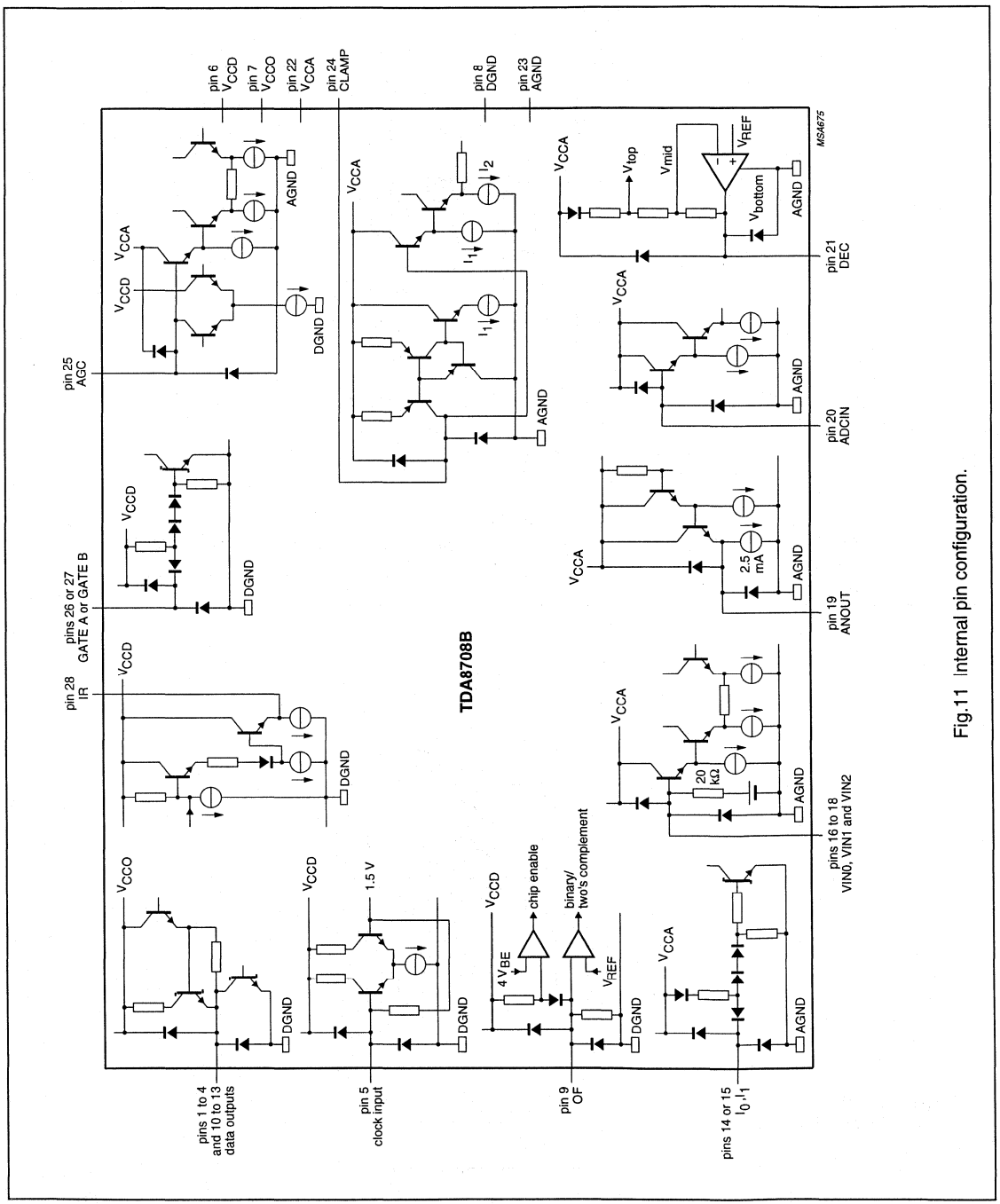
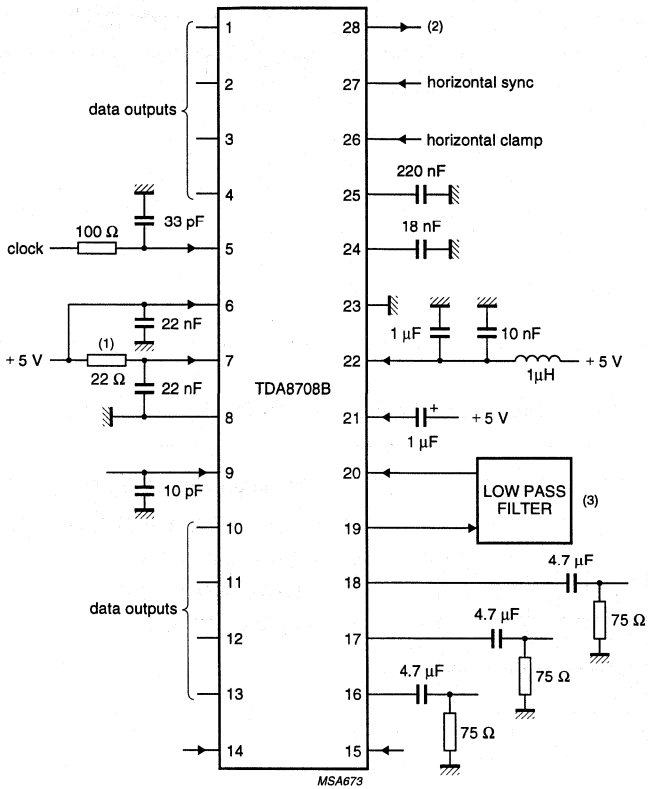


Fig.11 Internal pin configuration.

APPLICATION INFORMATION

Additional information can be found in the laboratory report of TDA8708A *"FBL/AN9308"*.

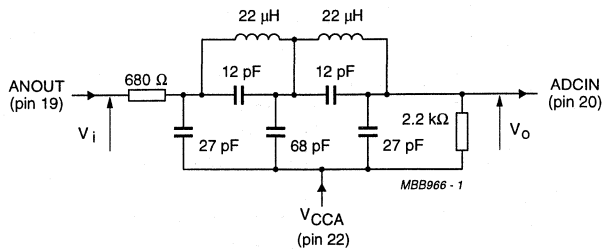


(1) It is recommended to decouple V_{CCO} through a 22 Ω resistor especially when the output data of TDA8708B interfaces with a capacitive CMOS load device.

(2) When IR is not used, it must be connected to ground via a 47 pF capacitor.

(3) See Figs 13 and 15 for examples of the low-pass filters.

Fig.12 Application diagram.



This filter can be adapted to various applications with respect to performance requirements. An input and output impedance of at least 680 Ω and 2.2 kΩ must in any event be applied.

Fig.13 Example of a low-pass filter for CVBS and Y signals.

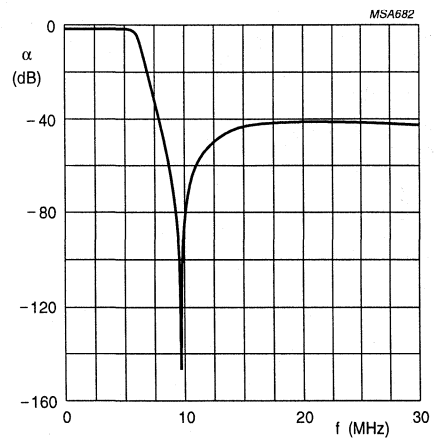
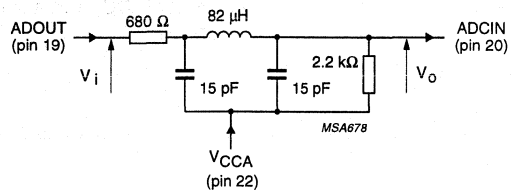


Fig.14 Frequency response for filter shown in Fig.13.

Characteristics of Fig.14

- Order 5; adapted CHEBYSHEV
- Ripple $\rho \leq 0.4$ dB
- f = 6.5 MHz at −3 dB
- f_{notch} = 9.75 MHz.



This filter can be adapted to various applications with respect to performance requirements. An input and output impedance of at least 680 Ω and 2.2 kΩ must in any event be applied.

Fig.15 Example of an economical low-pass filter for CVBS and Y signals.

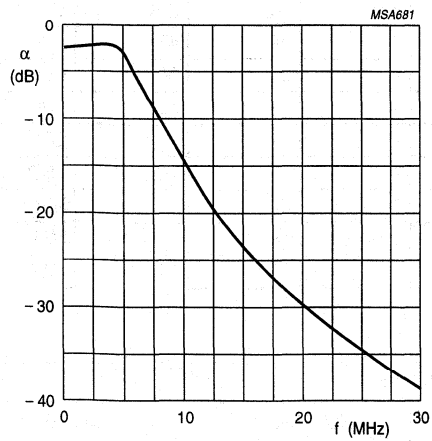


Fig.16 Frequency response for filter shown in Fig.15.

Characteristics of Fig.16

- Order 5; adapted CHEBYSHEV
- Ripple $\rho \leq 0.4$ dB
- f = 6.5 MHz at −3 dB.

Video analog input interface TDA8709A

FEATURES

- 8-bit resolution
- Sampling rate up to 32 MHz
- TTL-compatible digital inputs and outputs
- Internal reference voltage regulator
- Low-level AC clock inputs and outputs
- Clamp function with selection for '16' or '128'
- No sample-and-hold circuit required
- Three selectable video inputs.

APPLICATIONS

- Video signal processing
- Digital picture processing
- Frame grabbing.
- Colour difference signals (U, V)
- R, G, B signals
- Chrominance signal (C).

GENERAL DESCRIPTION

The TDA8709A is an analog input interface for video signal processing. It includes a an input selector (one out-of-three video signals), video amplifier with clamp and external gain control, an 8-bit analog-to-digital converter (ADC) with a sampling rate of 32 MHz and an input selector.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage	4.5	5.0	5.5	V
V_{CCD}	digital supply voltage	4.5	5.0	5.5	V
V_{CCO}	TTL output supply voltage	4.2	5.0	5.5	V
I_{CCA}	analog supply current	–	40	47	mA
I_{CCD}	digital supply current	–	24	30	mA
I_{CCO}	TTL output supply current	–	12	16	mA
ILE	DC integral linearity error	–	–	±1	LSB
DLE	DC differential linearity error	–	–	±0.5	LSB
$f_{clk(max)}$	maximum clock frequency	30	32	–	MHz
B	maximum –3 dB bandwidth (preamplifier)	12	18	–	MHz
P_{tot}	total power dissipation	–	380	512	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8709A	28	DIP	plastic	SOT117-1
TDA8709AT	28	SO28L	plastic	SOT136-1

BLOCK DIAGRAM

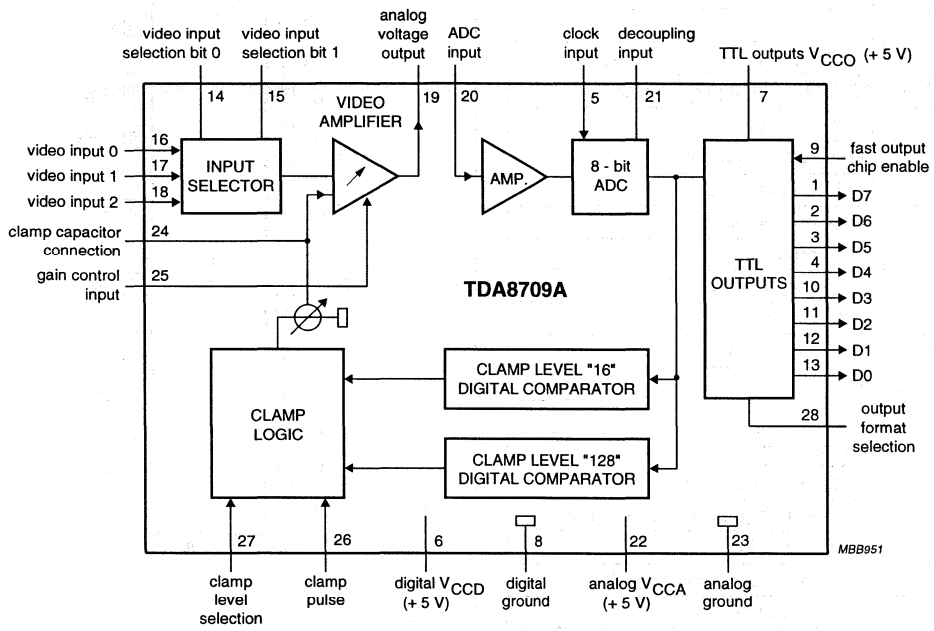


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
D7	1	data output; bit 7 (MSB)
D6	2	data output; bit 6
D5	3	data output; bit 5
D4	4	data output; bit 4
CLK	5	clock input
V_{CCD}	6	digital supply voltage (+5 V)
V_{CCO}	7	TTL outputs supply voltage (+5 V)
DGND	8	digital ground
FOEN	9	fast output chip enable
D3	10	data output; bit 3
D2	11	data output; bit 2
D1	12	data output; bit 1
D0	13	data output; bit 0 (LSB)
I0	14	video input selection bit 0
I1	15	video input selection bit 1
VIN0	16	video input 0
VIN1	17	video input 1
VIN2	18	video input 2
ANOUT	19	analog voltage output
ADCIN	20	analog-to-digital converter input
DEC	21	decoupling input
V_{CCA}	22	analog supply voltage (+5 V)
AGND	23	analog ground
CLAMP	24	clamp capacitor connection
GAIN	25	gain control input
CLP	26	clamping pulse
CLS	27	clamping level selection input
OFS	28	output format selection

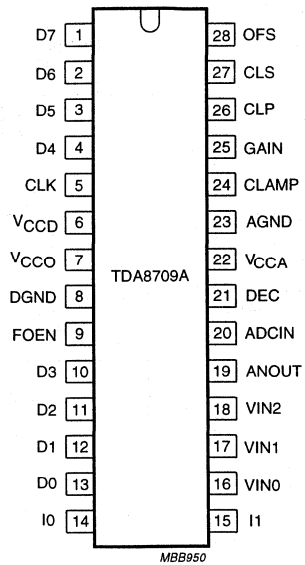


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

TDA8709A is an 8-bit ADC with internal clamping and a preamplifier with adjustable gain.

The clamping value is switched via pin 27 between digital 16 (for R, G, B signals) and digital 128 (for chrominance or colour difference signals). While clamping pulse at pin 27 is logic 1, the device will adjust the clamping level to the chosen value. The output format can be selected between binary and two's complement at pin 28.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage	−0.3	+7.0	V
V_{CCD}	digital supply voltage	−0.3	+7.0	V
V_{CCO}	TTL output supply voltage	−0.3	+7.0	V
ΔV_{CC}	supply voltage difference between V_{CCA} and V_{CCD}	−0.5	+0.5	V
	supply voltage difference between V_{CCO} and V_{CCD}	−0.5	+0.5	V
	supply voltage difference between V_{CCA} and V_{CCO}	−1.0	+1.0	V
V_I	input voltage	−0.3	+7.0	V
I_O	output current	–	+10	mA
T_{stg}	storage temperature	−55	+150	°C
T_{amb}	operating ambient temperature	0	+70	°C
T_j	junction temperature	0	+125	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	SOT117-1	55	K/W
	SOT136-1	70	K/W

CHARACTERISTICS

$V_{CCA} = V_{22}$ to V_{23} = 4.5 to 5.5 V; $V_{CCD} = V_6$ to V_8 = 4.5 to 5.5 V; $V_{CCO} = V_7$ to V_8 = 4.2 to 5.5 V; AGND and DGND shorted together; V_{CCA} to V_{CCD} = −0.5 to +0.5 V; V_{CCO} to V_{CCD} = −0.5 to +0.5 V; V_{CCA} to V_{CCO} = −0.5 to +0.5 V; T_{amb} = 0 to +70 °C; typical readings taken at $V_{CCA} = V_{CCD} = V_{CCO}$ = 5 V and T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
V_{CCO}	TTL output supply voltage		4.2	5.0	5.5	V
I_{CCA}	analog supply current		–	40	47	mA
I_{CCD}	digital supply current		–	24	30	mA
I_{CCO}	TTL output supply current	TTL load (see Fig.7)	–	12	16	mA
Preamplifier inputs						
VIN0 TO VIN2 INPUTS						
$V_{I(p-p)}$	input voltage (peak-to-peak value)	note 1	0.6	–	1.5	V
$\|Z_i\|$	input impedance	f_i = 6 MHz	10	20	–	kΩ
C_I	input capacitance	f_i = 6 MHz	–	1	–	pF
I0 AND I1 TTL INPUTS (SEE TABLE 1)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_I = 0.4 V	−400	–	–	µA
I_{IH}	HIGH level input current	V_I = 2.7 V	–	–	20	µA
CLS, OFS AND CLP TTL INPUTS (SEE FIG.5)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_I = 0.4 V	−400	–	–	µA
I_{IH}	HIGH level input current	V_I = 2.7 V	–	–	20	µA
t_{CLP}	clamp pulse width		2	–	–	µs
GAIN INPUT (PIN 25)						
$V_{25(min)}$	input voltage for minimum gain	see Fig.9	–	1.8	–	V
$V_{25(max)}$	input voltage for maximum gain	see Fig.9	–	3.8	–	V
I_I	input current		–	1.0	–	µA
CLAMP INPUT (PIN 24)						
V_{24}	clamp voltage for code 128 output		–	3.5	–	V
I_{24}	clamp output current		see Table 2			

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Video amplifier outputs						
ANOUT OUTPUT (PIN 19)						
$V_{19(p-p)}$	AC output voltage (peak-to-peak value)	V_{OF} = 1.33 V (p-p); V_{25} = 3.0 V	–	1.33	–	V
I_{19}	internal current source	$R_L = \infty$	2.0	2.5	–	mA
$I_{O(p-p)}$	output current driven by the load	V_{ANOUT} = 1.33 V (p-p); note 2	–	–	1.0	mA
V_{19}	DC output voltage for black level	CLS = logic 1	–	V_{CCA} – 2.02	–	V
V_{19}	DC output voltage for black level	CLS = logic 0	–	V_{CCA} – 2.6	–	V
Z_{19}	output impedance		–	20	–	Ω
Preamplifier dynamic characteristics						
α_{ct}	crosstalk between VIN inputs	V_{CCA} = 4.75 to 5.25 V; note 3	–	–50	–45	dB
G_{diff}	differential gain	V_{VIN} = 1.33 V (p-p); V_{25} = 3.0 V	–	2	–	%
φ_{diff}	differential phase	V_{VIN} = 1.33 V (p-p); V_{25} = 3.0 V	–	0.8	–	deg
B	–3 dB bandwidth		12	–	–	MHz
S/N	signal-to-noise ratio	note 4	60	–	–	dB
SVRR1	supply voltage ripple rejection	note 5	–	45	–	dB
ΔG	gain range	see Fig.9	–4.5	–	+6.0	dB
G_{stab}	gain stability as a function of supply voltage and temperature	see Fig.9	–	–	5	%
Analog-to-digital converter inputs						
CLK INPUT (PIN 5)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_{clk} = 0.4 V	–400	–	–	μA
I_{IH}	HIGH level input current	V_{clk} = 2.7 V	–	–	100	μA
$\|Z_i\|$	input impedance	f_{clk} = 10 MHz	–	4	–	kΩ
C_I	input capacitance	f_{clk} = 10 MHz	–	4.5	–	pF
FOEN INPUT (SEE TABLE 3)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_9 = 0.4 V	–400	–	–	μA
I_{IH}	HIGH level input current	V_9 = 2.7 V	–	–	20	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ADCIN INPUT (PIN 20; SEE TABLE 4)						
V_{20}	input voltage	digital output = 00	–	V_{CCA} – 2.52	–	V
V_{20}	input voltage	digital output = 255	–	V_{CCA} – 1.52	–	V
$V_{20(p-p)}$	input voltage amplitude (peak-to-peak value)		–	1.0	–	V
I_{20}	input current		–	1.0	10	μA
$\|Z_i\|$	input impedance	f_i = 6 MHz	–	50	–	MΩ
C_I	input capacitance	f_i = 6 MHz	–	1	–	pF
Analog-to-digital converter outputs						
DIGITAL OUTPUTS D0 TO D7						
V_{OL}	LOW level output voltage	I_{OL} = 2 mA	0	–	0.6	V
V_{OH}	HIGH level output voltage	I_{OL} = –0.4 mA	2.4	–	V_{CCD}	V
I_{OZ}	output current in 3-state mode	0.4 V < V_O < V_{CCD}	–20	–	+20	μA
Switching characteristics						
$f_{clk(max)}$	maximum clock input frequency	see Fig.5; note 6	30	32	–	MHz
Analog signal processing (f_{clk} = 32 MHz; see Fig.7)						
G_{diff}	differential gain	V_{20} = 1.0 V (p-p); see Fig.6; note 7	–	2	–	%
φ_{diff}	differential phase	see Fig.6; note 7	–	2	–	deg
f_1	fundamental harmonics (full-scale)	f_i = 4.43 MHz; note 7	–	–	0	dB
f_{all}	harmonics (full-scale); all components	f_i = 4.43 MHz; note 7	–	–55	–	dB
SVRR2	supply voltage ripple rejection	note 8	–	1	5	%/V
Transfer function						
ILE	DC integral linearity error		–	–	±1	LSB
DLE	DC differential linearity error		–	–	±0.5	LSB
ILE	AC integral linearity error	note 9	–	–	±2	LSB
Timing (f_{clk} = 32 MHz; see Figs 5, 6 and 7)						
DIGITAL OUTPUTS (C_L = 15 pF; I_{OL} = 2 mA; R_L = 2 kΩ)						
t_{ds}	sampling delay time		–	2	–	ns
t_h	output hold time		–	8	–	ns
t_d	output delay time		–	16	20	ns
t_{dEZ}	3-state delay time; output enable		–	16	25	ns
t_{dDZ}	3-state delay time; output disable		–	12	25	ns

Notes to the "Characteristics"

1. 0 dB is obtained at the AGC amplifier when applying $V_{i(p-p)}$ = 1.33 V.
2. The output current at pin 19 should not exceed 1 mA. The load impedance R_L should be referenced to V_{CCA} and defined as:
   a) AC impedance ≥1 kΩ and the DC impedance >2.7 kΩ.
   b) The load impedance should be coupled directly to the output of the amplifier so that the DC voltage supplied by the clamp is not disturbed.
3. Input signals with the same amplitude. Gain is adjusted to obtain ANOUT = 1.33 V (p-p).
4. Signal-to-noise ratio measured with 5 MHz bandwidth:

   $$\frac{S}{N} = 20 \log \frac{V_{ANOUT\,(p-p)}}{V_{ANOUT\,(RMS\ noise)}} \text{ at } B = 5 \text{ MHz}.$$

5. The voltage ratio is expressed as:

   $$SVRR1 = 20 \log \frac{\Delta V_{CCA}}{V_{CCA}} \times \frac{G}{\Delta G}$$ for V_I = 1 V (p-p), gain at 100 kHz = 1 and 1 V supply variation.

6. It is recommended that the rise and fall times of the clock are ≥2 ns. In addition, a 'good layout' for the digital and analog grounds is recommended.
7. These measurements are realized on analog signals after a digital-to-analog conversion (TDA8702 is used).
8. The supply voltage rejection is the relative variation of the analog signal (full-scale signal at input) for 1 V of supply variation:

   $$SVRR2 = \frac{\Delta (V_{I\,(00)} - V_{I\,(FF)}) + (V_{I\,(00)} - V_{I\,(FF)})}{\Delta V_{CCA}}$$

9. Full-scale sine wave (f_i = 4.4 MHz; f_{clk} = 27 MHz).

Table 1 Video input selection (CVBS).

I1	I0	SELECTED INPUT
0	0	VIN0
0	1	VIN1
1	0	VIN2
1	1	VIN1

Table 2 CLAMP output current.

CLS	CLP	DIGITAL OUTPUT	I_{CLAMP}
1	1	output < 128	+50 μA
		output > 128	−50 μA
X[1]	0	X	0 μA
0	1	output < 16	+50 μA
		16 < output	−50 μA

Note

1. X = don't care.

Table 3 FOEN input coding.

FOEN	D0 TO D7
0	active, two's complement
1	high impedance

Table 4 Output coding and input voltage (typical values).

STEP	V_{ADCIN}	BINARY OUTPUTS								TWO'S COMPLEMENT							
		D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Underflow	–	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0	V_{CCA} − 2.52 V	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	–	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1
.	–	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	–	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
254	–	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0
255	V_{CCA} − 1.52 V	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
Overflow	–	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1

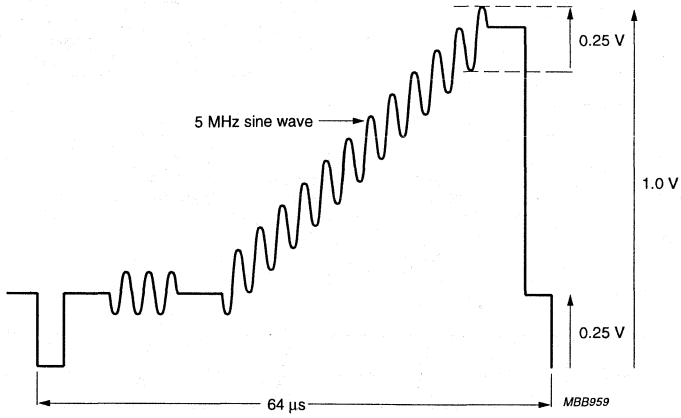


Fig.3 Test signal on the ADCIN pin for differential gain and phase measurements.

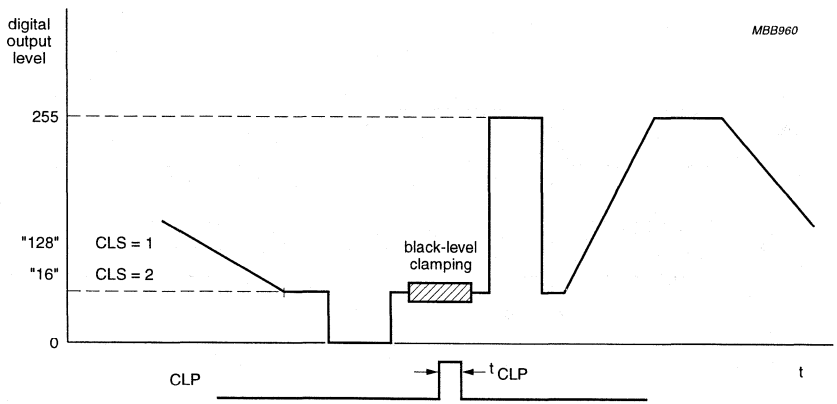


Fig.4 Control mode selection.

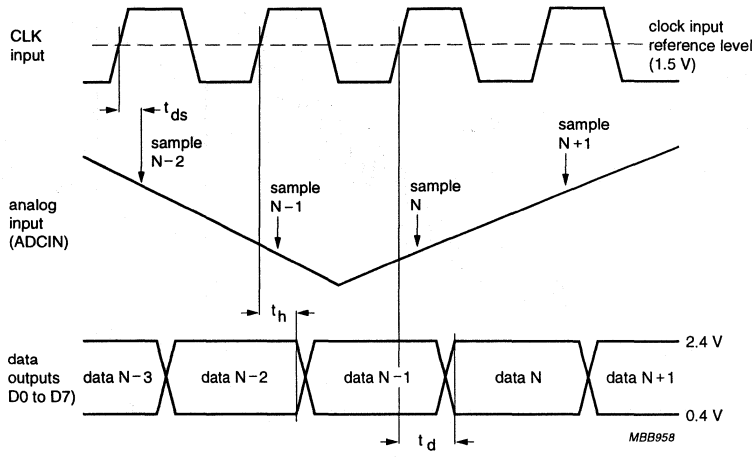


Fig.5 Timing diagram.

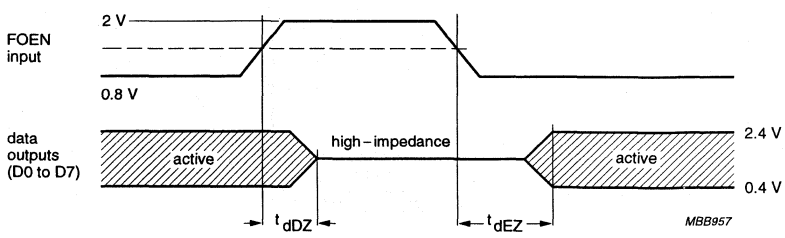


Fig.6 Output format timing diagram.

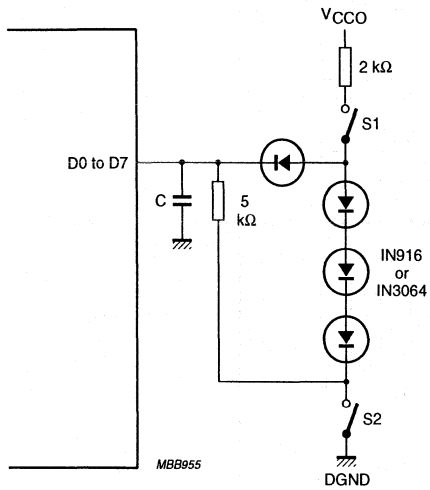


Fig.7 Load circuit for timing measurement; data outputs (FOEN = LOW).

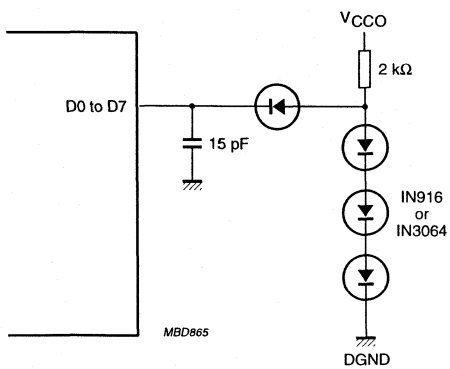
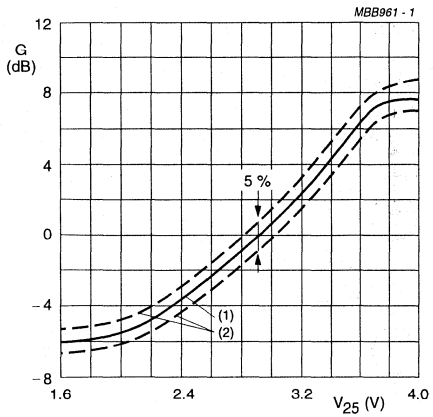


Fig.8 Load circuit for timing measurement; 3-state outputs (FOEN: f_i = 1 MHz; V_{FOEN} = 3 V).



(1) Typical value ($V_{CCA} = V_{CCD} = 5$ V; $T_{amb} = 25$ °C).
(2) Minimum and maximum values (temperature and supply).

Fig.9 Typical gain control curve as a function of gain voltage.

INTERNAL PIN CIRCUITRY

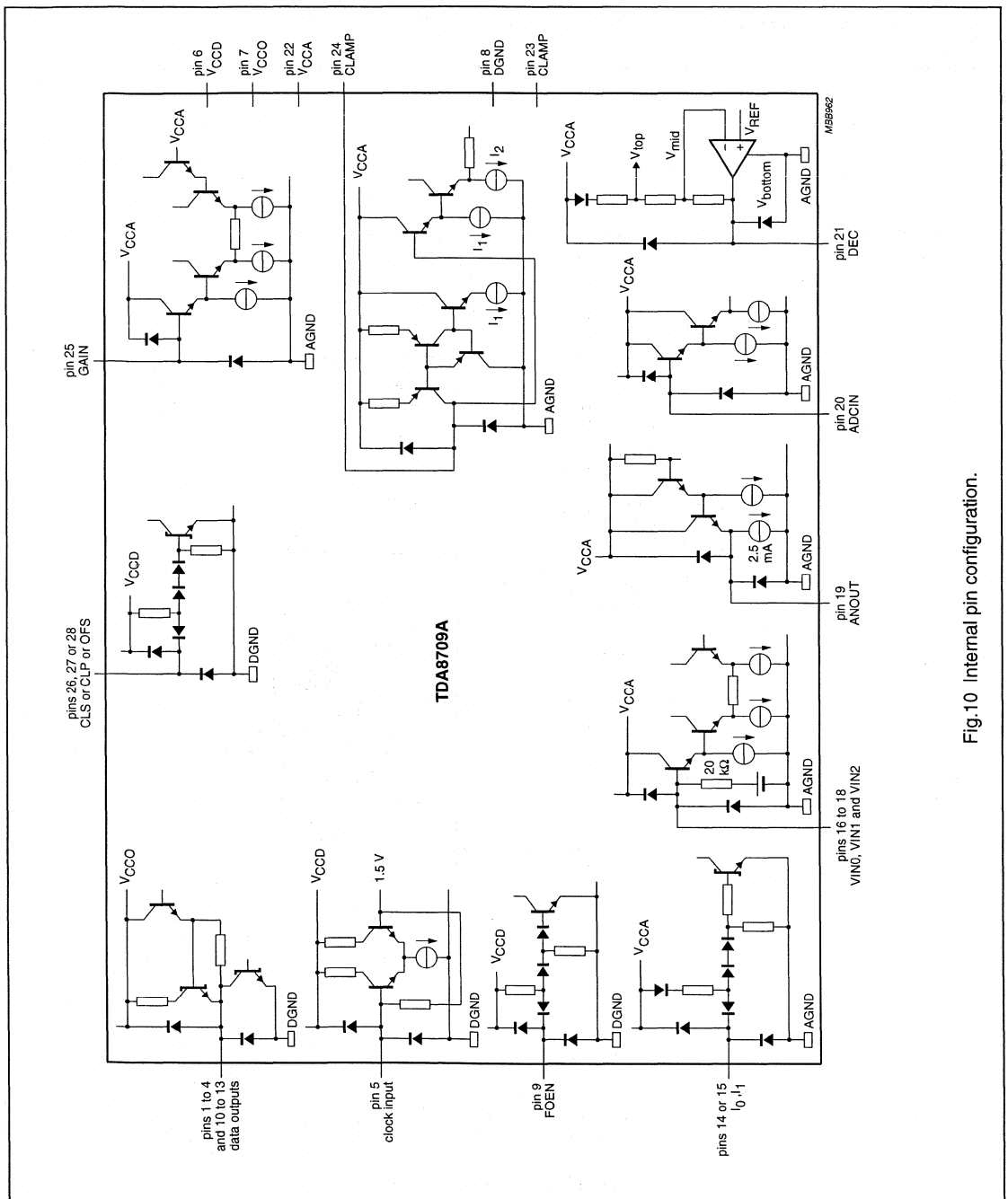
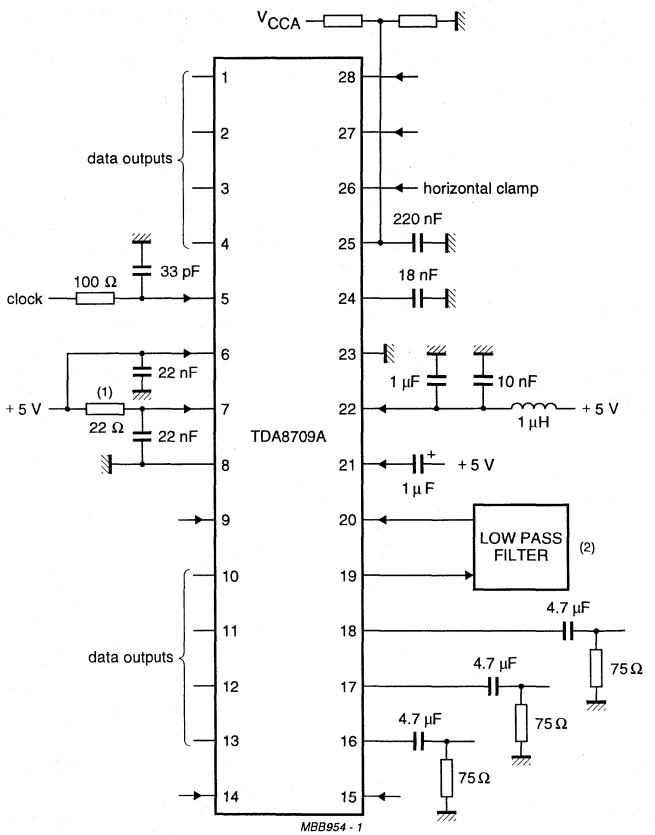


Fig.10 Internal pin configuration.

APPLICATION INFORMATION

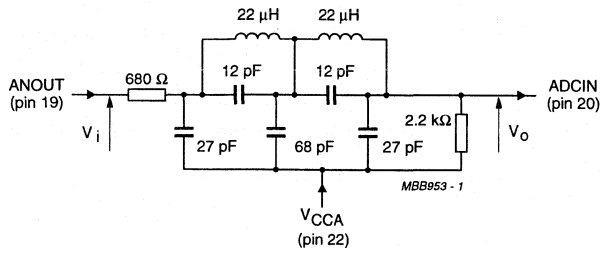
Additional information can be found in the laboratory report of TDA8708A *"FBL/AN9308"*.



(1) It is recommended to decouple V_{CCO} through a 22 Ω resistor especially when the output data of TDA8709A interfaces with a capacitive CMOS load device.

(2) See Figs 12, 14, 16 and 18 for examples of the low-pass filters.

Fig.11 Application diagram.



This filter can be adapted to various applications with respect to performance requirements. An input and output impedance of at least 680 Ω and 2.2 kΩ must in any event be applied.

Fig.12 Example of a low-pass filter for RGB and C signals.

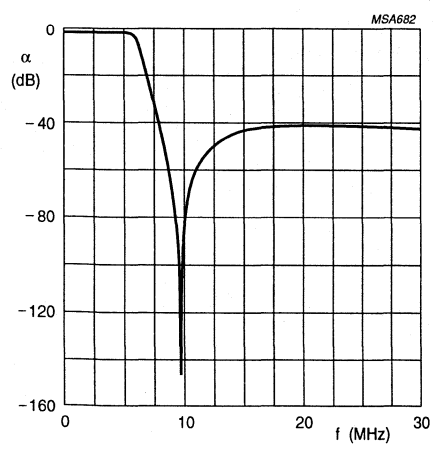
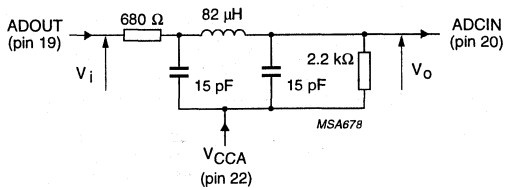


Fig.13 Frequency response for filter shown in Fig.12.

Characteristics of Fig.13

- Order 5; adapted CHEBYSHEV
- Ripple $\rho \leq 0.4$ dB
- f = 6.5 MHz at −3 dB
- f_{notch} = 9.65 MHz.



This filter can be adapted to various applications with respect to performance requirements. An input and output impedance of at least 680 Ω and 2.2 kΩ must in any event be applied.

Fig.14 Example of an economical low-pass filter for RGB and C signals.

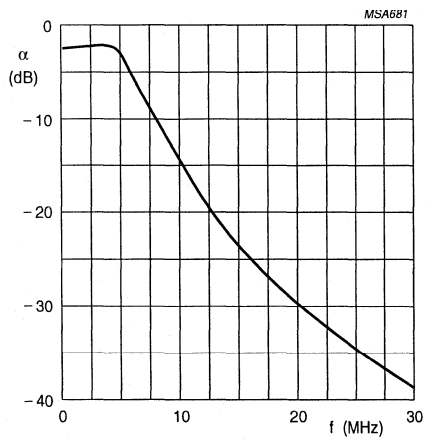
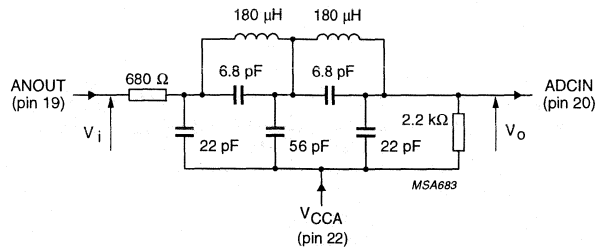


Fig.15 Frequency response for filter shown in Fig.14.

Characteristics of Fig.15

- Order 3; adapted CHEBYSHEV
- Ripple $\rho \leq 0.4$ dB
- f = 6.5 MHz at −3 dB.



This filter can be adapted to various applications with respect to performance requirements. An input and output impedance of at least 680 Ω and 2.2 kΩ must in any event be applied.

Fig.16 Example of a low-pass filter for U and V signals.

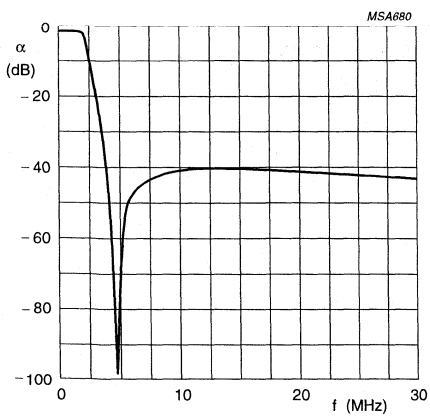
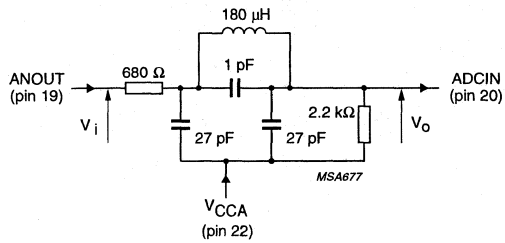


Fig.17 Frequency response for filter shown in Fig.16.

Characteristics of Fig.17

- Order 5; adapted CHEBYSHEV
- Ripple $\rho \leq 0.4$ dB
- f = 2.3 MHz at −3 dB
- f_{notch} = 4.5 MHz.



This filter can be adapted to various applications with respect to performance requirements. An input and output impedance of at least 680 Ω and 2.2 kΩ must in any event be applied.

Fig.18 Example of an economical low-pass filter for U and V signals.

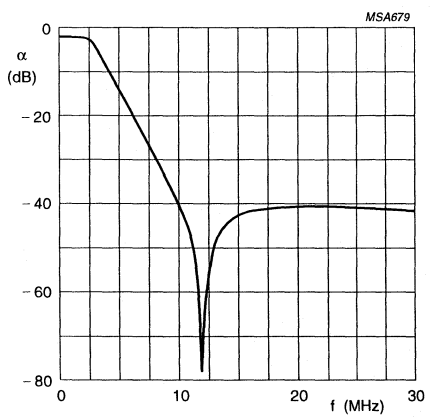


Fig.19 Frequency response for filter shown in Fig.18.

Characteristics of Fig.19

- Order 3; adapted CHEBYSHEV
- Ripple $\rho \leq 0.3$ dB
- f = 2.8 MHz at –3 dB
- f_{notch} = 11.9 MHz.

YC 8-bit low-power analog-to-digital video interface

TDA8758

FEATURES

- Two 8-bit ADCs:
  - one Luminance or CVBS channel
  - one Chrominance channel
- Sampling rate up to 32 MHz
- Binary or two's complement 3-state TTL outputs for each channel
- Internal reference voltage regulator
- TTL-compatible digital inputs and outputs
- Power dissipation of 530 mW (typical)
- Input selector circuit (five selectable video inputs for CVBS or YC processing)
- Peak white enable input
- Clamp and Automatic Gain Control (AGC) functions for Y/CVBS channel (clamping on code 64 and Peak White level control at code 255)
- Clamp function for C channel (code 128)
- No sample-and-hold circuit required.

APPLICATIONS

- Video signal decoding
- Digital picture processing
- Frame grabbing
- Multimedia with the Philips Desktop Video chip set (and especially SAA7196 multistandard decoder and scaler).

GENERAL DESCRIPTION

The TDA8758 is an 8-bit video high-speed low-power analog-to-digital conversion (ADC) interface for YC and CVBS signal processing. It converts 1-of-3 CVBS input signals or 1-of-2 YC input signals into binary or two's complement words at a sampling rate of 32 MHz.
All analog signal inputs are digitally clamped and an ADC interface is provided on the Y/CVBS channel. A fast precharge on clamp and AGC is provided for start-up.
All digital inputs and outputs are TTL compatible.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current		–	59	70	mA
I_{CCD}	digital supply current		–	28	40	mA
I_{CCO}	output supply current	C_L = 15 pF	–	19	28	mA
ILE	DC integral linearity error		–	±0.75	±1.5	LSB
DLE	DC differential linearity error		–	±0.4	±1.0	LSB
EB	effective bits (from video input to digital outputs)	f_{clk} = 32 MHz; f_i = 4.43 MHz	–	7.1	–	bits
$f_{clk(max)}$	maximum clock frequency		30	32	–	MHz
B	maximum –3 dB bandwidth (input preamplifier)	full-scale; 0 dB gain	–	15	–	MHz
α_{ct}	crosstalk between Y and C channels and each video input		–	–63	–55	dB
P_{tot}	total power dissipation		–	530	724	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8758G	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

BLOCK DIAGRAM

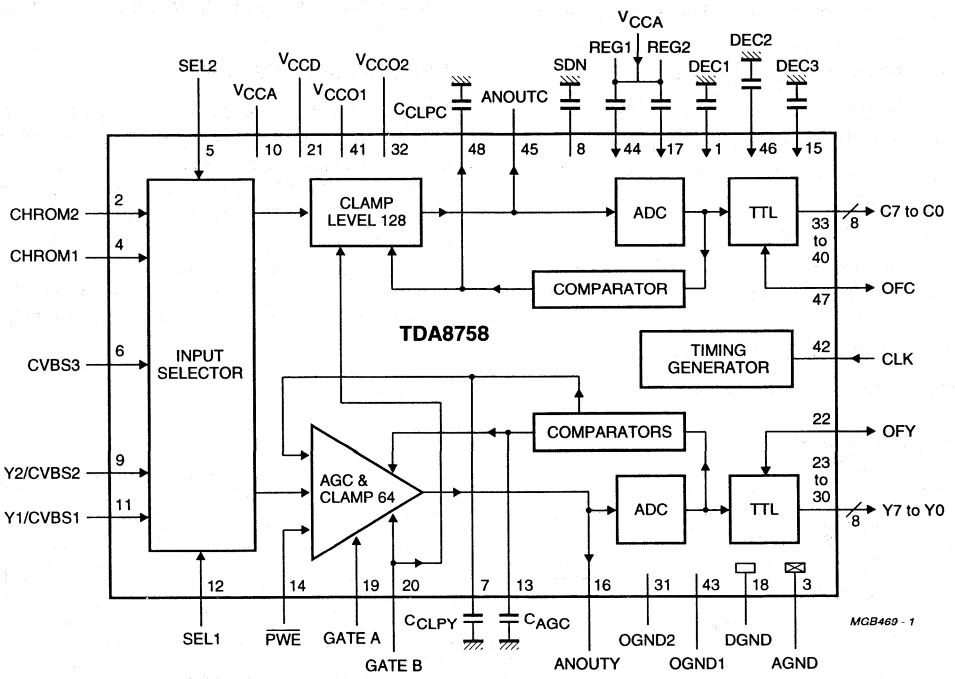


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
DEC1	1	decoupling input 1
CHROM2	2	chrominance analog voltage input 2
AGND	3	analog ground
CHROM1	4	chrominance analog voltage input 1
SEL2	5	selection control input 2
CVBS3	6	luminance analog voltage input 3
C_{CLPY}	7	Y channel clamping capacitor
SDN	8	stabilizer decoupling node
Y2/CVBS2	9	luminance analog voltage input 2
V_{CCA}	10	analog supply voltage (+5 V)
Y1/CVBS1	11	luminance analog voltage input 1
SEL1	12	selection control input 1
C_{AGC}	13	AGC capacitor
$\overline{PWE}$	14	peak white enable input (active LOW)
DEC3	15	decoupling input 3
ANOUTY	16	analog output for Y channel
REG2	17	decoupling input 2 (internal stabilization loop decoupling)
DGND	18	digital ground
GATE A	19	AGC control input
GATE B	20	clamp control input
V_{CCD}	21	digital supply voltage (+5 V)
OFY	22	Y channel output format/chip enable (3-state input)
Y7	23	Y channel data output; bit 7 (MSB)
Y6	24	Y channel data output; bit 6
Y5	25	Y channel data output; bit 5
Y4	26	Y channel data output; bit 4
Y3	27	Y channel data output; bit 3
Y2	28	Y channel data output; bit 2
Y1	29	Y channel data output; bit 1
Y0	30	Y channel data output; bit 0 (LSB)
OGND2	31	output ground 2
V_{CCO2}	32	output supply voltage 2 (+5 V)
C7	33	C channel data output; bit 7 (MSB)
C6	34	C channel data output; bit 6
C5	35	C channel data output; bit 5
C4	36	C channel data output; bit 4
C3	37	C channel data output; bit 3
C2	38	C channel data output; bit 2
C1	39	C channel data output; bit 1
C0	40	C channel data output; bit 0 (LSB)

SYMBOL	PIN	DESCRIPTION
V_{CCO1}	41	output supply voltage 1 (+5 V)
CLK	42	clock input
OGND1	43	output ground 1
REG1	44	decoupling input 1 (internal stabilization loop decoupling)
ANOUTC	45	analog output for C channel
DEC2	46	decoupling input 2
OFC	47	C channel output format/chip enable (3-state input)
C_{CLPC}	48	C channel clamping capacitor

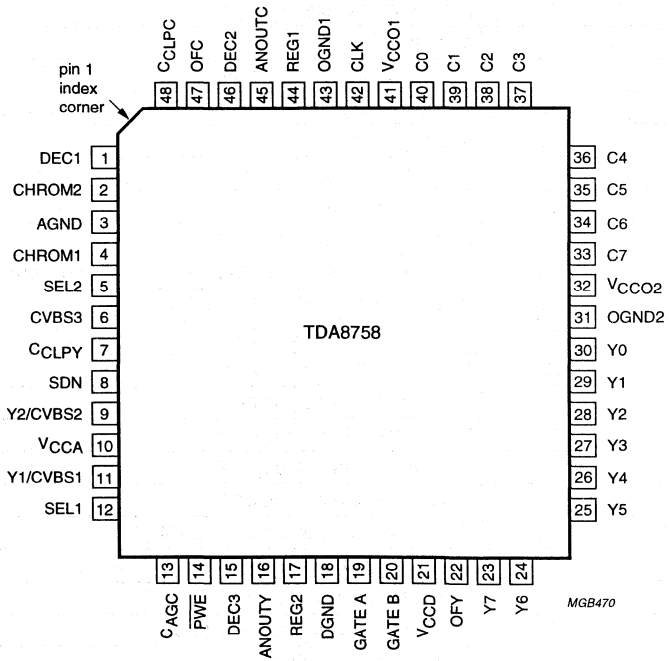


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA8758 provides a simple interface between CVBS or Y/C analog signals and a digital colour decoder.

Video inputs selection

The input selector allows a choice from different video sources, and has one of the following configurations:

A: Two Y/C and one CVBS signals

B: One Y/C and two CVBS signals

C: Three CVBS signals (only the Y channel is used).

The wiring of the five video inputs (pins 2, 4, 6, 9 and 11) and the control of the two selection inputs (pins 5 and 12) will depend on the available video sources.

- In configuration A, connect as follows:
  - Y1 to pin 11
  - C1 to pin 4
  - Y2 to pin 9
  - C2 to pin 2
  - CVBS3 to pin 6.

  Keep SEL2 (pin 5) LOW and select Y1/C1 or Y2/C2 by switching SEL1 (pin 12).

  CVBS3 is selected with SEL1 and SEL2 HIGH.
- In configuration B, replace Y1 (or Y2) by a CVBS input (no more C1 or C2). The selection mode is the same.
- In configuration C, connect as follows:
  - CVBS1 to pin 11
  - CVBS2 to pin 9
  - CVBS3 to pin 6.

  Use both SEL1 and SEL2 to select inputs.

Remark: the video inputs selection is a static selection.

Synchronization pulses

GATE A and GATE B pulses are synchronization pulses occurring during the sync period and rear porch respectively. They should be distinct.

On the Y channel, the digital output of the ADC is compared to internal digital reference levels. The resultant outputs control the charge or discharge current of a capacitor connected to the C_{AGC} pin. The voltage across this capacitor controls the gain of the video amplifier. This is the control loop.

The sync level comparator is active during a positive-going pulse at the GATE A input. This means that sync pulse of the composite video signal is used as an amplitude reference. The bottom of the sync pulse is adjusted to obtain a digital output of logic 1 at the converter Y output. As the black level is digital level 64, the sync pulse will have a digital amplitude of 64 LSBs.

The Peak White control loop is active when the selection pin $\overline{PWE}$ is LOW. Then, if the Y video signal exceeds the digital code of 255, it will be limited to avoid any over-range of the converter.

The clamp level control is accomplished by using the same techniques as used for the gain control. On both Y and C channels, the black level digital comparators are active during a positive-going pulse at the GATE B input. On the Y channel, the clamping capacitor connected to the C_{CLPY} pin will be charged or discharged to adjust the digital output to code 64. On the C channel, the clamping capacitor connected to the C_{CLPC} pin will be charged or discharged to adjust the digital output to code 128.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage		−0.3	+7.0	V
V_{CCD}	digital supply voltage		−0.3	+7.0	V
V_{CCO}	output supply voltage		−0.3	+7.0	V
ΔV_{CC}	supply voltage difference between V_{CCA} and V_{CCD}		−1.0	+1.0	V
	supply voltage difference between V_{CCO} and V_{CCD}		−1.0	+1.0	V
	supply voltage difference between V_{CCA} and V_{CCO}		−1.0	+1.0	V
V_I	input voltage	referenced to AGND	−	5.0	V
$V_{clk(p-p)}$	AC input voltage for switching (peak-to-peak value)	referenced to DGND	−	V_{CCO}	V
I_O	output current		−	+6	mA
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C
T_j	junction temperature		−	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	72	K/W

CHARACTERISTICS

$V_{CCA} = V_{10}$ to V_3 = 4.75 to 5.25 V; $V_{CCD} = V_{21}$ to V_{18} = 4.75 to 5.25 V; $V_{CCO1} = V_{41}$ to V_{43} = 4.75 to 5.25 V; $V_{CCO2} = V_{32}$ to V_{31} = 4.75 to 5.25 V; AGND and DGND shorted together; V_{CCA} to V_{CCD} = −0.25 to +0.25 V; V_{CCO} to V_{CCD} = −0.25 to +0.25 V; V_{CCA} to V_{CCO} = −0.25 to +0.25 V; T_{amb} = 0 to +70 °C; typical values measured at $V_{CCA} = V_{CCD} = V_{CCO}$ = 5 V and T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current		−	59	70	mA
I_{CCD}	digital supply current		−	28	40	mA
I_{CCOtot}	total output supply current	C_L = 15 pF	−	19	28	mA
Video amplifier inputs						
Y1/CVBS1, Y2/CVBS2, CVBS3, CHROM1 AND CHROM2 INPUTS						
$V_{I(p-p)}$	input voltage (peak-to-peak value)	AGC load with external capacitor; note 1				
	Y channel		0.7	−	1.4	V
	C channel		−	1.0	−	V
$\|Z_i\|$	input impedance	f_i = 6 MHz	−	25	−	kΩ
C_I	input capacitance	f_i = 6 MHz	−	2	−	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SEL1 AND SEL2 TTL INPUTS; see Table 1						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_I = 0.4 V	–400	–	–	μA
I_{IH}	HIGH level input current	V_I = 2.7 V	–	–	20	μA
GATE A AND GATE B TTL INPUTS; see Figs 5 and 6						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_I = 0.4 V	–400	–	–	μA
I_{IH}	HIGH level input current	V_I = 2.7 V	–	–	20	μA
AGC INPUT (PIN 13); see Fig.8						
$V_{13(min)}$	AGC voltage for minimum gain at –3 dB		–	3.3	–	V
$V_{13(max)}$	AGC voltage for maximum gain at +3 dB		–	3.75	–	V
I_{12}	AGC output current		see Table 2			
C-CHANNEL CLAMP INPUT (PIN 48)						
V_{48}	CLAMP voltage for code 128 output		–	3.45	–	V
I_{48}	CLAMP output current		see Table 3			
Y-CHANNEL CLAMP INPUT (PIN 7)						
V_7	CLAMP voltage for code 64 output		–	3.70	–	V
I_7	CLAMP output current		see Table 3			
Video amplifier dynamic characteristics						
α_{ct}	crosstalk between video inputs (pins 2, 4, 6, 9 and 11)	V_{CCA} = 4.75 to 5.25 V	–	–63	–55	dB
B	–3 dB bandwidth		–	15	–	MHz
ΔG	gain range		–3	–	+3	dB
G_{stab}	gain stability as a function of:					
	supply voltage	f_i = 4.43 MHz	–	–	0.5	%
	supply voltage and temperature		–	–	6	%
Analog-to-digital converter inputs						
CLK INPUT (PIN 42)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_{clk} = 0.4 V	–400	–	–	μA
I_{IH}	HIGH level input current	V_{clk} = 2.7 V	–	–	20	μA
C_I	input capacitance	f_{clk} = 32 MHz	–	2	–	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
OFY AND OFC INPUTS; 3-STATE; see Table 4						
V_{IL}	LOW level input voltage		0	–	0.2	V
V_{IH}	HIGH level input voltage		2.6	–	V_{CCD}	V
V_I	input voltage in high impedance state		–	1.15	–	V
I_{IL}	LOW level input current		–370	–300	–	µA
I_{IH}	HIGH level input current		–	500	700	µA
Analog-to-digital converter outputs						
ANOUTY AND ANOUTC OUTPUTS (PINS 16 AND 45); see Table 5						
V_{ANOUT}	output voltage	digital output = 00	–	2.6	–	V
V_{ANOUT}	output voltage	digital output = 255	–	3.6	–	V
$V_{ANOUT(p-p)}$	output voltage amplitude (peak-to-peak value)		–	1.0	–	V
DIGITAL OUTPUTS Y0 TO Y7, C0 TO C7						
V_{OL}	LOW level output voltage	I_{OL} = 2 mA	0	–	0.6	V
V_{OH}	HIGH level output voltage	I_{OL} = –0.4 mA	2.4	–	V_{CCD}	V
Switching characteristics; see Fig.9						
$f_{clk(max)}$	CLK input maximum frequency	note 2	30	32	–	MHz
t_{CPH}	clock pulse width HIGH		12	–	–	ns
t_{CPL}	clock pulse with LOW		12	–	–	ns
Analog signal processing from video input to digital output on both channels; 0 dB gain (f_{clk} = 32 MHz)						
INL	DC integral non-linearity		–	±0.75	±1.5	LSB
DNL	DC differential non-linearity		–	±0.4	±1.0	LSB
AINL	AC integral non linearity	f_i = 4.43 MHz	–	±1.5	–	LSB
ADNL	AC differential non-linearity	f_i = 4.43 MHz	–	±0.5	–	LSB
THD	total harmonic distortion	note 3	–	–52	–	dB
EB	effective bits	f_i = 4.43 MHz; note 4	–	7.1	–	bits
G_{diff}	differential gain	$V_{16,45}$ = 1.0 V (p-p); see Fig.4; PAL modulated ramp; note 5	–	1.5	3.0	%
φ_{diff}	differential phase	see Fig.5; PAL modulated ramp; note 5	–	0.6	1.5	deg
SVRR2	supply voltage ripple rejection	note 6	–	–	5	%/V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing (f_{clk} = 32 MHz); see Fig.9						
DIGITAL OUTPUTS (C_L = 15 pF)						
t_{ds}	sampling delay time		–	2	–	ns
t_h	output hold time		10	–	–	ns
t_d	output delay time		–	15	18	ns
t_W	clamp pulse width	see Figs 6 and 7	2	3	–	µs
3-state output delay times; see Fig.10						
t_{dZH}	enable HIGH		–	12	14	ns
t_{dZL}	enable LOW		–	10	12	ns
t_{dHZ}	disable HIGH		–	58	62	ns
t_{dLZ}	disable LOW		–	70	74	ns

Notes

1. 0 dB is obtained at the AGC amplifier when applying $V_{I(p\text{-}p)}$ = 1.0 V on Y channel.
2. It is recommended that the rise and fall times of the clock are ≥1 ns. In addition, a 'good layout' for the digital and analog grounds is recommended.
3. THD (total harmonic distortion) is obtained with the addition of the first five harmonics:

$$THD = 20 \log \frac{F}{\sqrt{(2nd)^2 + (3rd)^2 + (4th)^2 + (5th)^2 + (6th)^2}}$$

   a) F being the fundamental harmonic referenced at 0 dB for a full-scale sine wave input.
4. Effective bits are obtained via a Fast Fourier Transform (FFT) treatment taking 8 K acquisition points per equivalent fundamental period. The calculation takes into account all harmonics and noise up to half of the clock frequency (NYQUIST frequency). Conversion to signal-to-noise ratio: S/N = EB × 6.02 + 1.76 dB.
5. Measurement carried out using video analyser VM700A, where video analog signal is reconstructed through a digital-to-analog converter.
6. The supply voltage ripple rejection is the relative variation of the analog signal (full-scale signal at input) for 0.5 V of supply variation:

$$SVRR2 = \frac{\Delta (V_{I(00)} - V_{I(FF)}) \times (V_{I(00)} - V_{I(FF)})}{\Delta V_{CCA}}$$

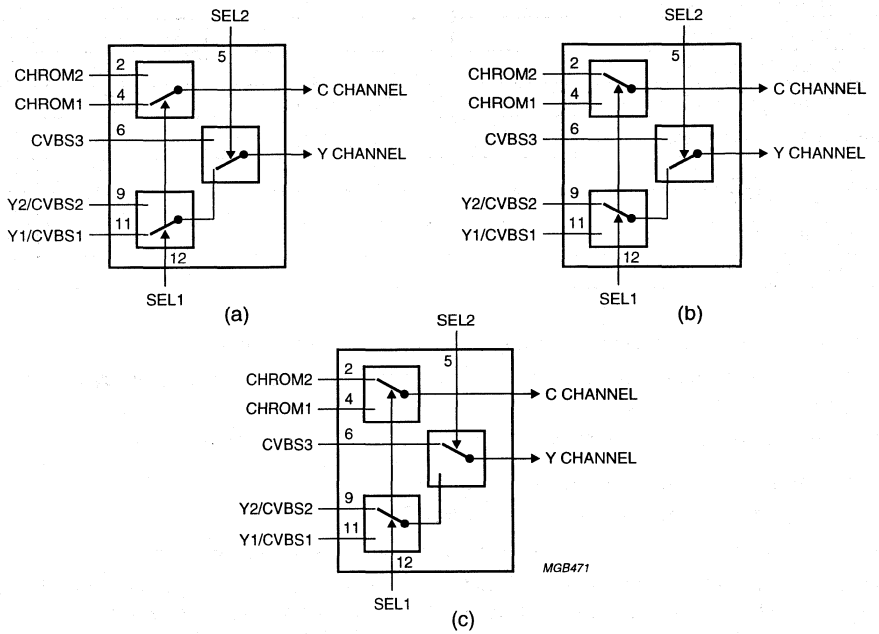


Fig.3 Video inputs selector.

Table 1 Video input selection

SEL1	SEL2	Y-CHANNEL	C-CHANNEL	FIGURE 3
0	X[1]	Y1/CVBS1	CHROM1	(a)
1	0	Y2/CVBS2	CHROM2	(b)
1	1	CVBS3	CHROM2	(c)

Note

1. X = don't care.

Table 2 AGC output current

$\overline{PWE}$	GATE A	DIGITAL OUTPUT	I_{AGC}
0	0	output < 255	0 μA
		output > 255	+540 μA
0	1	output < 0	+8 μA
		0 < output < 255	−8 μA
		output > 255	+540 μA
1	0	X[1]	0 μA
1	1	output < 0	+8 μA
		0 < output < 255	−8 μA

Note

1. X = don't care.

Table 3 CLAMP output current

CLAMP	GATE B	DIGITAL OUTPUT	I_{CLAMP}
C	1	output < 128	+54 μA
		output > 128	−54 μA
X[1]	0	X[1]	0 μA
Y	1	output < 64	+54 μA
		64 < output	−54 μA

Note

1. X = don't care.

Table 4 OFY and OFC input coding

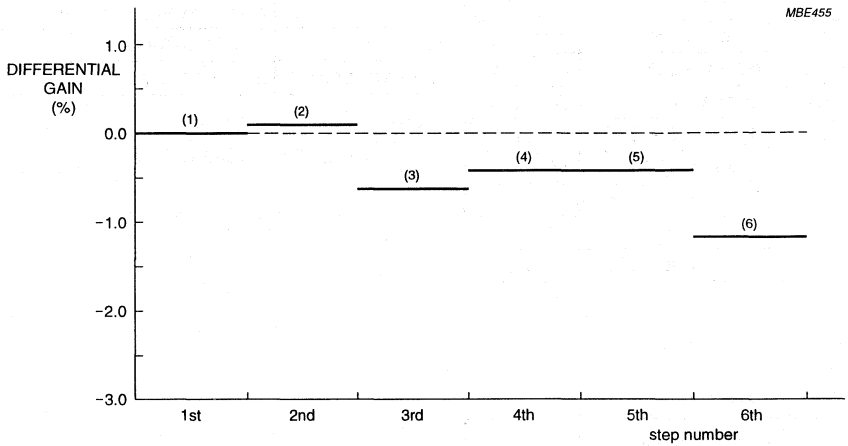
OFY (or OFC)	Y0 to Y7 (or C0 TO C7)
0	active, twos complement
1	high impedance
open circuit[1]	active, binary

Note

1. Use C ≥ 10 pF to DGND.

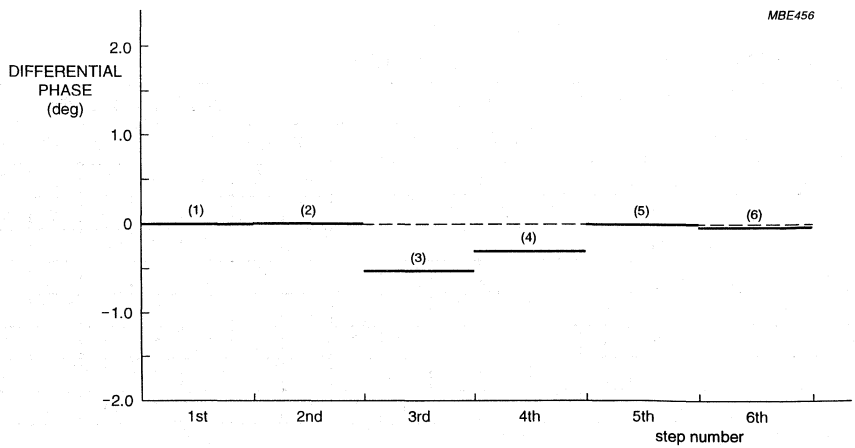
Table 5 Output coding and ANOUTY (or ANOUTC) voltage (typical values)

STEP	V_I	BINARY OUTPUTS								TWOS COMPLIMENT							
		D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Underflow	–	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0	2.6	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	–	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1
.	–	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	–	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
254	–	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0
255	3.6	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
Overflow	–	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1



(1) = 0.00; (2) = 0.09; (3) = −0.63; (4) = −0.45; (5) = −0.45; (6) = −1.23.
Differential gain = max. (2) − min. (6) = 1.32%.

Fig.4 Typical differential gain result on VM700A.



(1) = 0.00; (2) = 0.03; (3) = −0.53; (4) = −0.32; (5) = 0.01; (6) = −0.08.
Differential phase = max. (2) − min. (3) = 0.56 deg.

Fig.5 Typical differential phase result on VM700A.

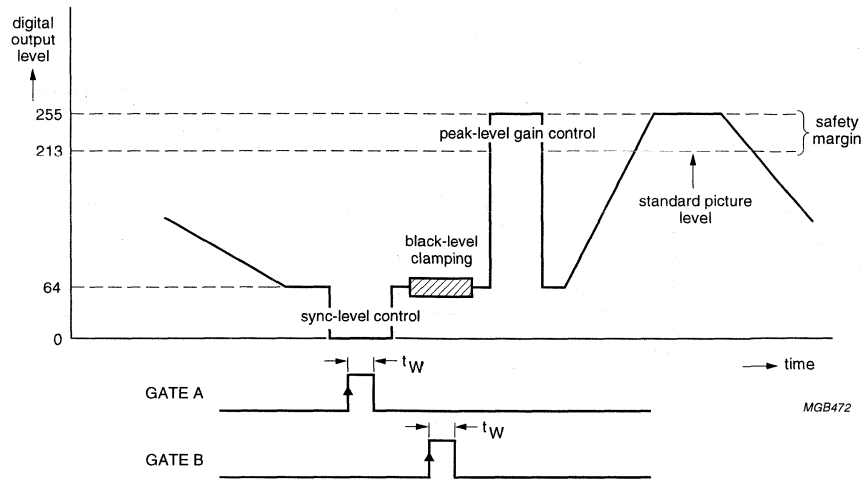


Fig.6 Control mode Y channel.

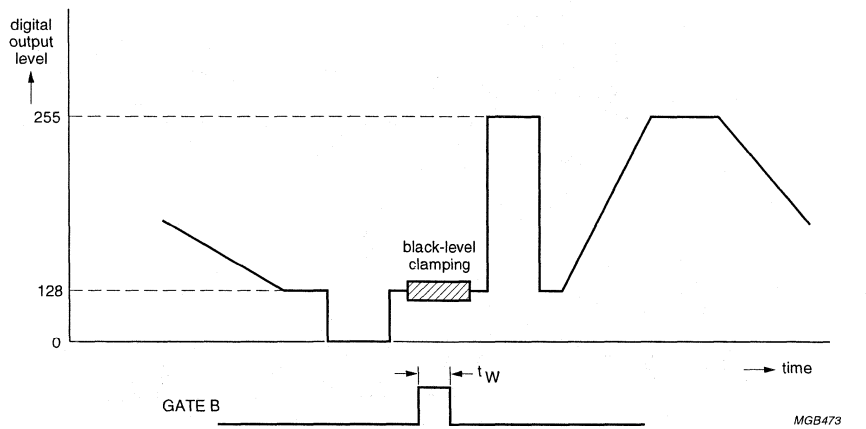
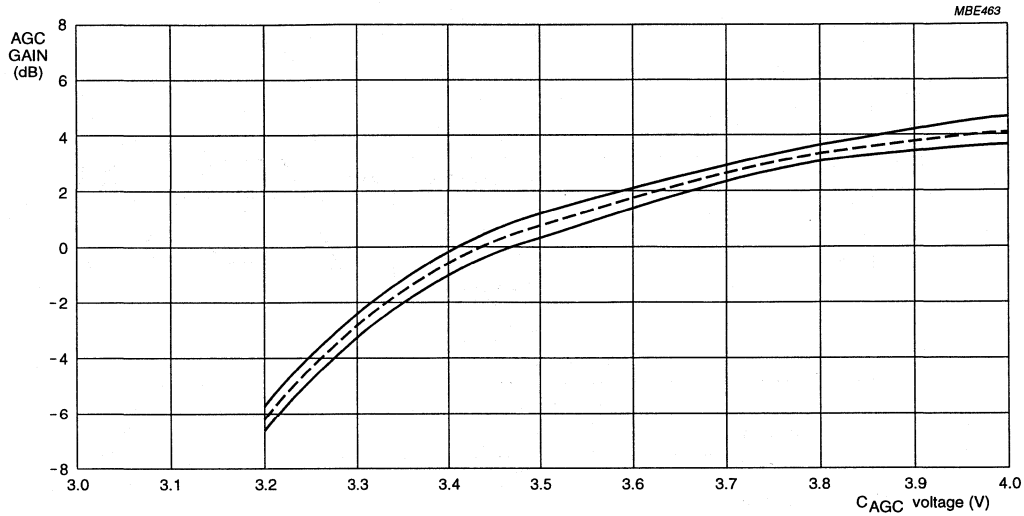


Fig.7 Control mode C-channel.



Dotted line: Typical curve (T_{amb} = 25 °C; V_{CC} = 5 V).
Full line: Maximum envelope (T_{amb} = 0 to 70 °C; V_{CC} = 4.75 to 5.25 V).

Fig.8 AGC behaviour as a function temperature and supply voltage for ANOUTY output; f_i = 4.43 MHz, V_i = 0 dB.

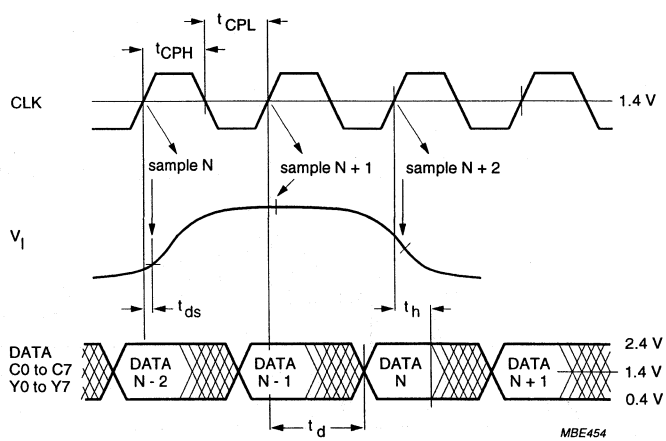
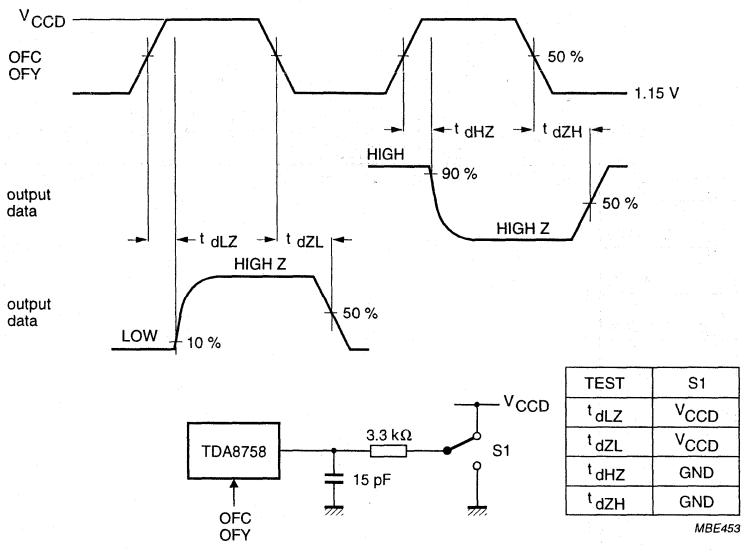


Fig.9 Timing diagram.

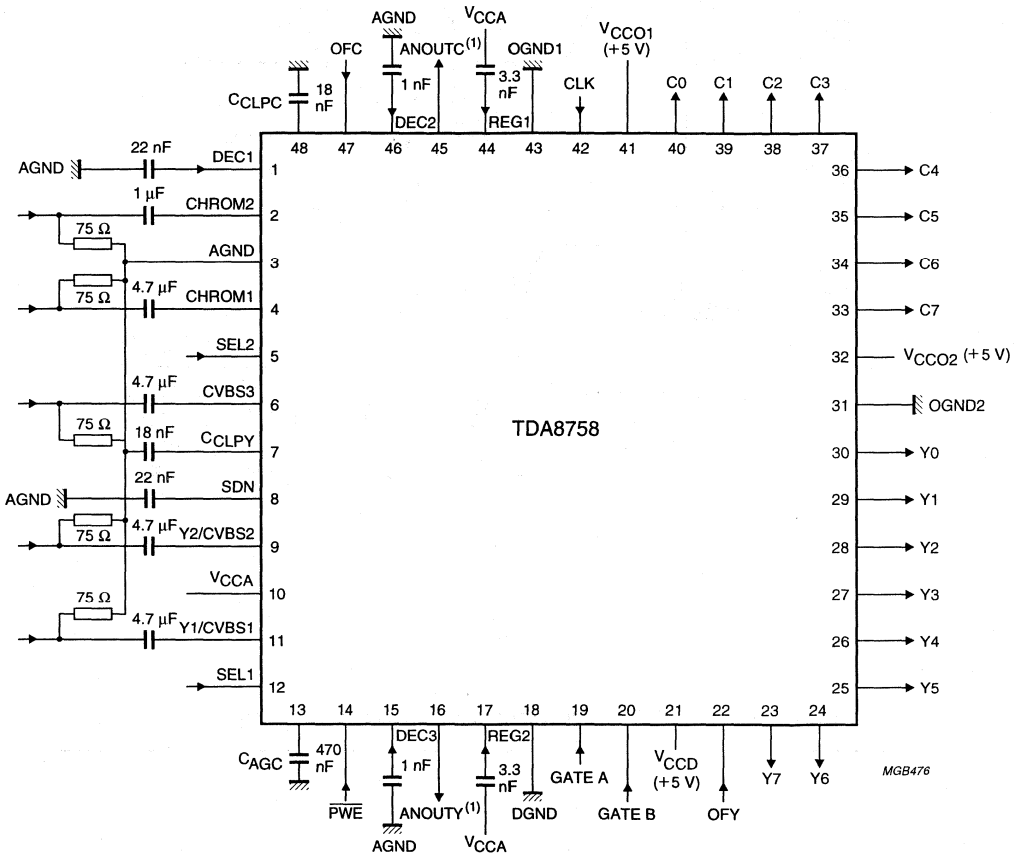


TEST	S1
t_{dLZ}	V_{CCD}
t_{dZL}	V_{CCD}
t_{dHZ}	GND
t_{dZH}	GND

$f_{OFC} = f_{OFY} = 100$ kHz.

Fig.10 Timing diagram and test conditions of 3-state output delay time.

APPLICATION INFORMATION



(1) It is recommended that pin 16 and pin 45 are not loaded in order to avoid any distortion.

Fig.11 Application diagram.

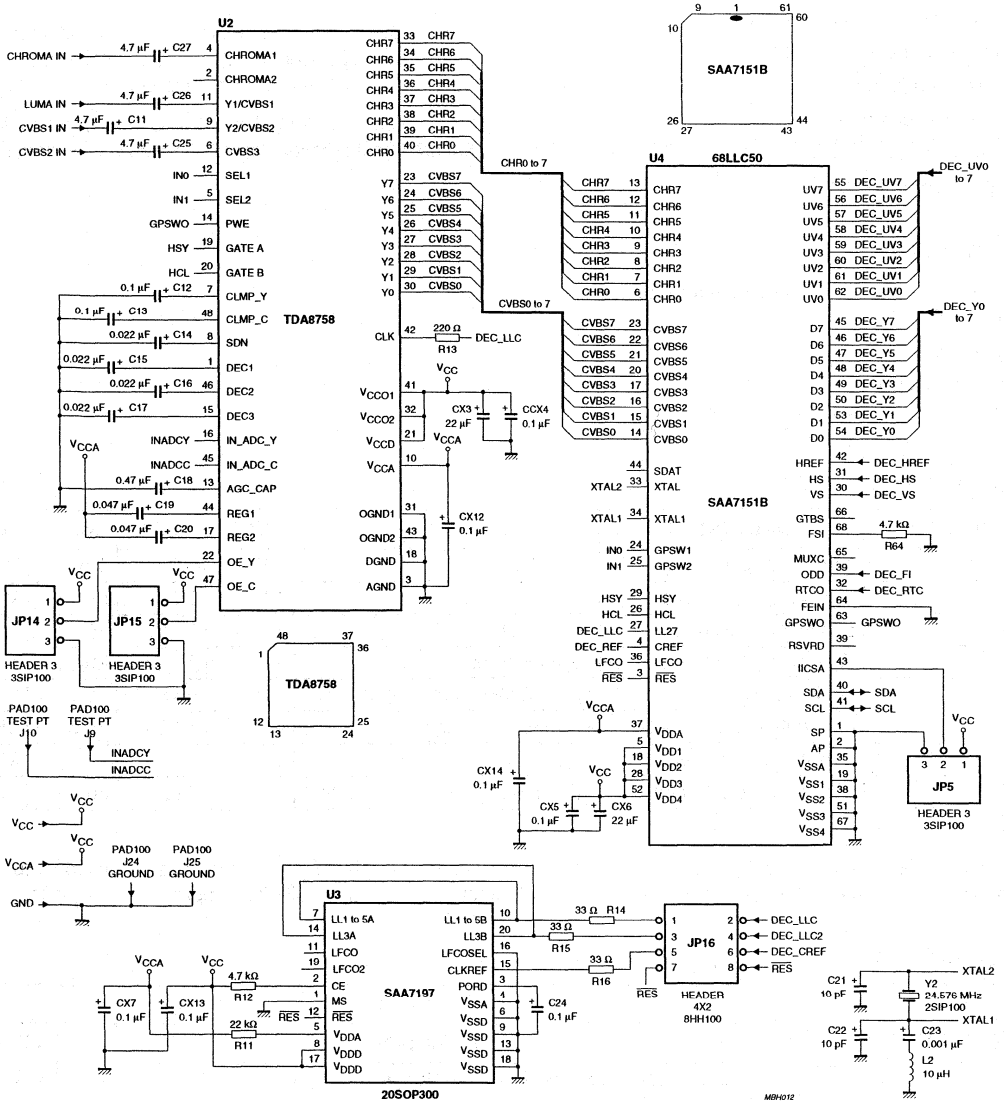


Fig.12 Example of system application (DPC71 evaluation board).

Triple 8-bit video Digital-to-Analog Converter (DAC)

TDA8771A

FEATURES

- 8-bit resolution
- Sampling rate up to 35 MHz
- Internal reference voltage regulator
- No deglitching circuit required
- Large output voltage range
- 1 kΩ output load
- Power dissipation only 200 mW
- Single 5 V power supply
- 44-pin QFP package.

APPLICATIONS

- General purpose high-speed digital-to-analog conversion
- Digital TV
- Graphic display
- Desktop video processing.

GENERAL DESCRIPTION

The TDA8771A is a triple 8-bit video Digital-to-Analog Converter (DAC). It converts the digital input signals into analog voltage outputs at a maximum conversion rate of 35 MHz.

The DACs are based on resistor-string architecture with integrated output buffers. The output voltage range is determined by a built-in reference source.

The device is fabricated in a 5 V, CMOS process that ensures high functionality with low power dissipation.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
I_{DDA}	analog supply current	R_L = 1 kΩ; note 1	10	33	45	mA
I_{DDD}	digital supply current	f_{clk} = 35 MHz	–	7	20	mA
INL	integral non-linearity	f_{clk} = 35 MHz; ramp input	–	±0.5	±1	LSB
DNL	differential non-linearity	f_{clk} = 35 MHz; ramp input	–	±0.25	±0.5	LSB
$f_{clk(max)}$	maximum clock frequency		35	–	–	MHz
P_{tot}	total power dissipation	R_L = 1 kΩ; f_{clk} = 35 MHz; note 1	45	200	360	mW

Note

1. Minimum and maximum data of current and power consumption are measured in worse case conditions: for minimum data, all digital inputs are at logic level 0 while for maximum data, all digital inputs are at logic level 1.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8771AH	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2

BLOCK DIAGRAM

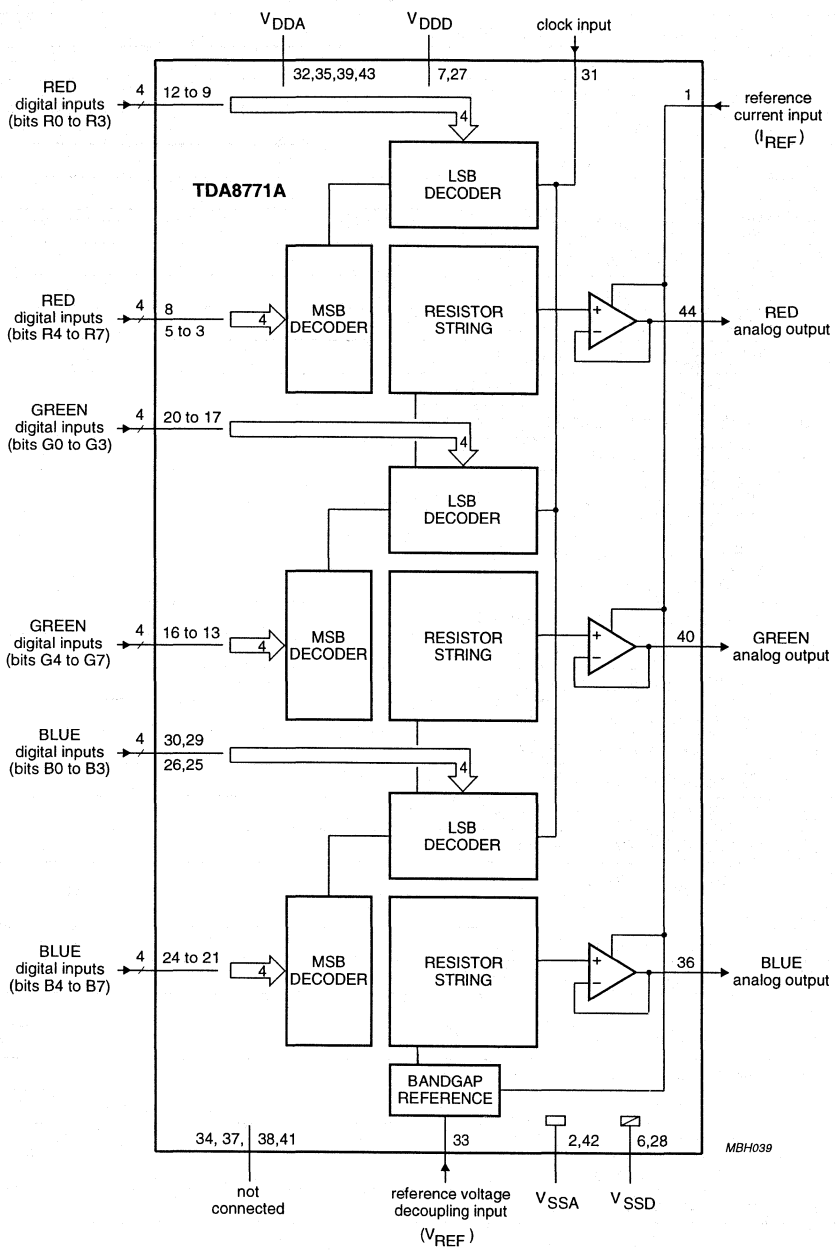


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
I_{REF}	1	reference current input for output buffers
V_{SSA1}	2	analog supply ground 1
R7	3	RED digital input data; bit 7 (MSB)
R6	4	RED digital input data; bit 6
R5	5	RED digital input data; bit 5
V_{SSD1}	6	digital supply ground 1
V_{DDD1}	7	digital supply voltage 1
R4	8	RED digital input data; bit 4
R3	9	RED digital input data; bit 3
R2	10	RED digital input data; bit 2
R1	11	RED digital input data; bit 1
R0	12	RED digital input data; bit 0 (LSB)
G7	13	GREEN digital input data; bit 7 (MSB)
G6	14	GREEN digital input data; bit 6
G5	15	GREEN digital input data; bit 5
G4	16	GREEN digital input data; bit 4
G3	17	GREEN digital input data; bit 3
G2	18	GREEN digital input data; bit 2
G1	19	GREEN digital input data; bit 1
G0	20	GREEN digital input data; bit 0 (LSB)
B7	21	BLUE digital input data; bit 7 (MSB)
B6	22	BLUE digital input data; bit 6
B5	23	BLUE digital input data; bit 5
B4	24	BLUE digital input data; bit 4
B3	25	BLUE digital input data; bit 3
B2	26	BLUE digital input data; bit 2
V_{DDD2}	27	digital supply voltage 2
V_{SSD2}	28	digital supply ground 2
B1	29	BLUE digital input data; bit 1
B0	30	BLUE digital input data; bit 0 (LSB)
CLK	31	clock input
V_{DDA1}	32	analog supply voltage 1
V_{REF}	33	decoupling input for reference voltage
n.c.	34	not connected
V_{DDA2}	35	analog supply voltage 2
OUTB	36	BLUE analog output
n.c.	37	not connected
n.c.	38	not connected
V_{DDA3}	39	analog supply voltage 3
OUTG	40	GREEN analog output

SYMBOL	PIN	DESCRIPTION
n.c.	41	not connected
V_{SSA2}	42	analog supply ground 2
V_{DDA4}	43	analog supply voltage 4
OUTR	44	RED analog output

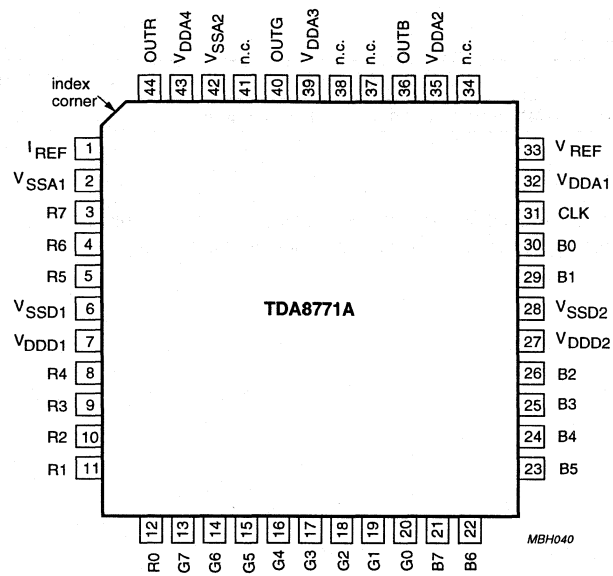


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage	−0.5	+6.5	V
V_{DDD}	digital supply voltage	−0.5	+6.5	V
ΔV_{DD}	supply voltage difference between V_{DDA} and V_{DDD}	−1.0	+1.0	V
T_{stg}	storage temperature	−55	+150	°C
T_{amb}	operating ambient temperature	0	+70	°C
T_j	junction temperature	–	+125	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	75	K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS

$V_{DDA} = V_{DDD} = 4.5$ to 5.5 V; V_{SSA} and V_{SSD} shorted together; $V_{DDA} - V_{DDD} = -0.5$ to +0.5 V; $T_{amb} = 0$ to 70 °C; typical values measured at $V_{DDA} = V_{DDD} = 5$ V and $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
I_{DDA}	analog supply current	$R_L = 1$ kΩ; note 1	10	33	45	mA
I_{DDD}	digital supply current	$f_{clk} = 35$ MHz	–	7	20	mA
Inputs						
CLOCK INPUT (PIN 31)						
V_{IL}	LOW level input voltage		0	–	1.2	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DDD}	V
R, G, B DIGITAL INPUTS (PINS 12 TO 8, 5 TO 3, 20 TO 13, 30, 29 AND 26 TO 21)						
V_{IL}	LOW level input voltage		0	–	1.2	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DDD}	V
I_{REF} REFERENCE CURRENT INPUT FOR OUTPUT BUFFERS (PIN 1)						
I_I	input current		–	0.6	0.7	mA
Timing; see Fig.3						
$f_{clk(max)}$	maximum clock frequency		35	–	–	MHz
t_{CPH}	clock pulse width HIGH		8	–	–	ns
t_{CPL}	clock pulse width LOW		8	–	–	ns
t_r	clock rise time		–	–	5	ns
t_f	clock fall time		–	–	6	ns
$t_{SU;DAT}$	input data set-up time		4	–	–	ns
$t_{HD;DAT}$	input data hold time		4	–	–	ns
Voltage reference (pin 33, referenced to V_{SSA})						
V_{REF}	output reference voltage		1.180	1.242	1.305	V
Outputs						
OUTB, OUTR, OUTG ANALOG OUTPUTS (PINS 36, 44 AND 40, REFERENCED TO V_{SSA}) FOR 1 kΩ LOAD; see Table 1						
FSR	full-scale output voltage range		2.80	2.95	3.10	V
V_{os}	offset of analog voltage output		–	0.25	–	V
V_{Omax}	maximum output voltage	data inputs = logic 1; note 2	2.95	3.20	3.45	V
V_{Omin}	minimum output voltage	data inputs = logic 0; note 2	0.05	0.25	0.45	V
THD	total harmonic distortion	$f_i = 4.43$ MHz; $f_{clk} = 35$ MHz	–	–44	–	dB
Z_L	output load impedance		0.9	1.0	1.1	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Transfer function (f_{clk} = 35 MHz)						
INL	integral non-linearity	ramp input	–	0.5	±1	LSB
DNL	differential non-linearity	ramp input	–	0.25	±0.5	LSB
α_{ct}	crosstalk DAC to DAC		–50	–	–	dB
	DAC to DAC matching		–	1.0	2.0	%
Switching characteristics (for 1 kΩ output load); see Fig.4						
t_d	input to 50% output delay time	full-scale change	–	12	–	ns
t_{s1}	settling time	10% to 90% of full-scale change	–	15	–	ns
t_{s2}	settling time	to ±1 LSB	–	50	–	ns
Output transients (glitches)						
V_g	area for 1 LSB change		–	1	–	LSB·ns

Notes

1. Minimum and maximum data of current and power consumption are measured in worse case conditions: for minimum data, all digital inputs are at logic level 0 while for maximum data, all digital inputs are at logic level 1.
2. V_O is directly proportional to V_{REF}.

Table 1 Input coding and DAC output voltages (typical values)

BINARY INPUT DATA (SYNC = BLANK = 0)	CODE	DAC OUTPUT VOLTAGES (V) OUTB, OUTR, OUTG R_L = 1 kΩ
0000 0000	0	0.262
0000 0001	1	0.273
....	.	.
1000 0000	128	1.731
....	.	.
1111 1110	254	3.188
1111 1111	255	3.200

TIMING

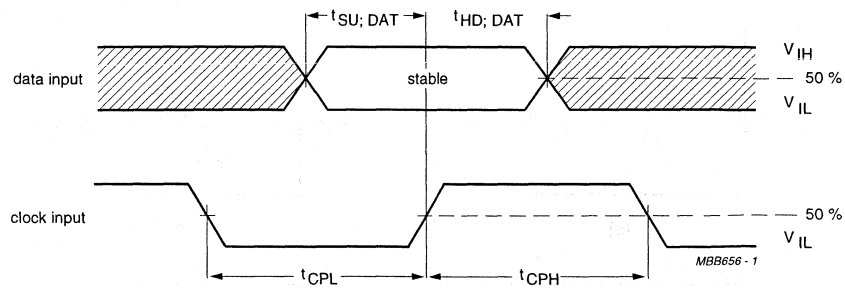


Fig.3 Input timing.

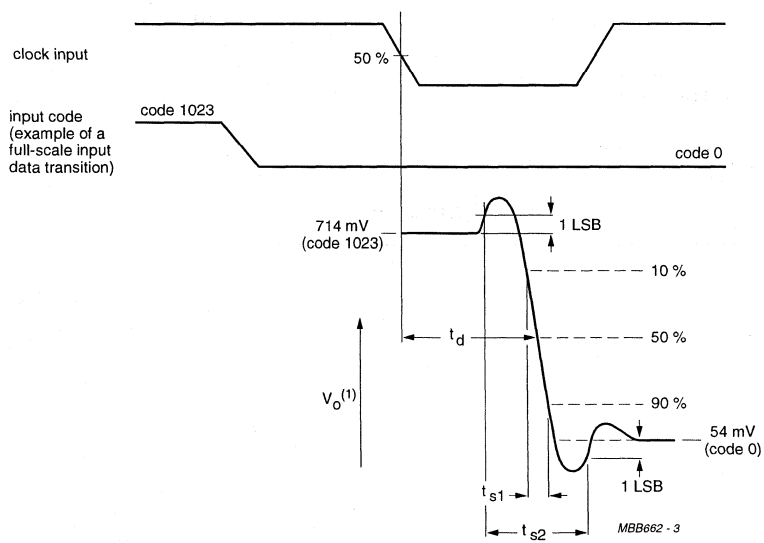
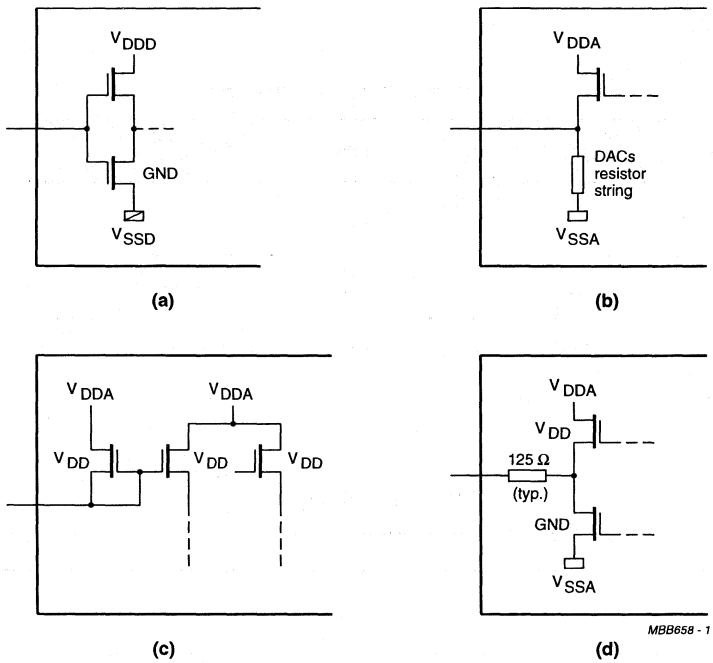


Fig.4 Switching timing.

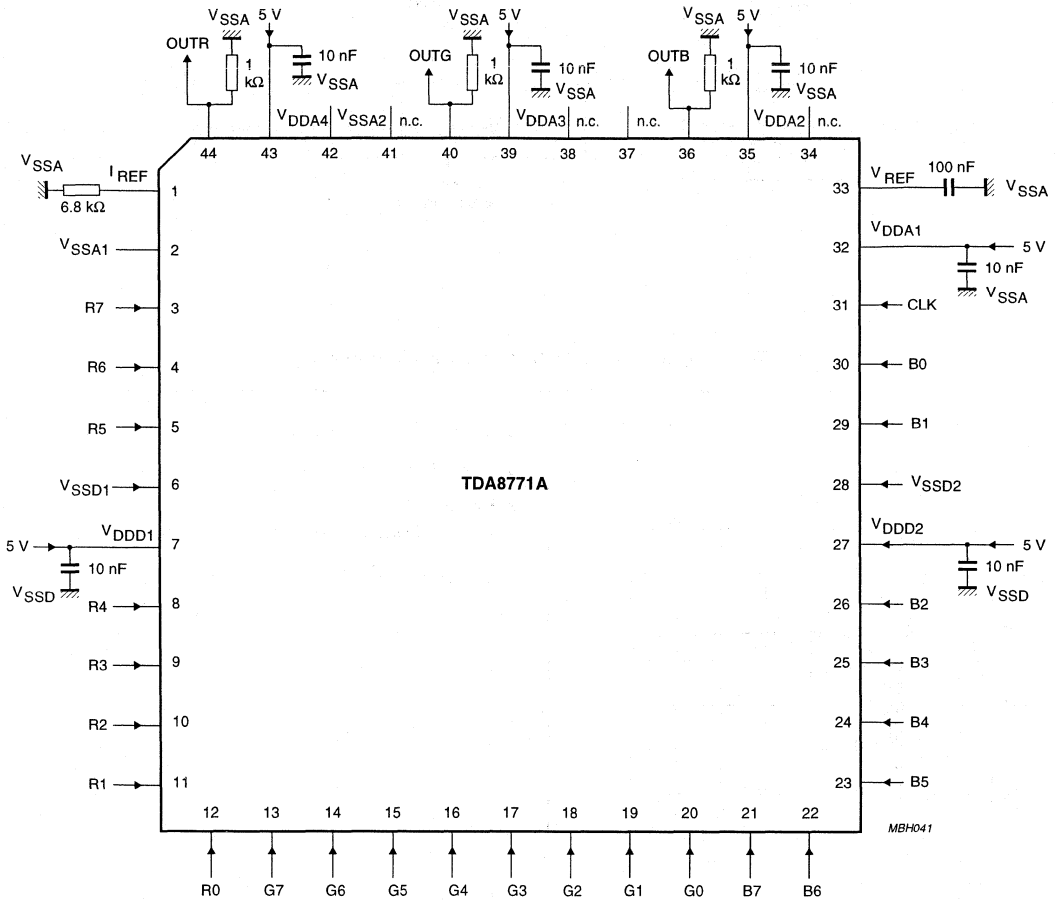
INTERNAL CIRCUITRY



(a) Digital inputs; pins 3 to 5, 8 to 26 and 29 to 31.
(b) V_{REF}; pin 33.
(c) I_{REF}; pin 1.
(d) OUTR, G, B; pins 44, 40 and 36.

Fig.5 Internal circuitry.

APPLICATION INFORMATION



Analog and digital supplies should be separated and decoupled.
Supplies are not connected internally.
All ground pins must be connected. One ground plane is preferred although it depends on application.
See Figs 7 and 9 for example of anti-aliasing filter.

Fig.6 Application diagram.

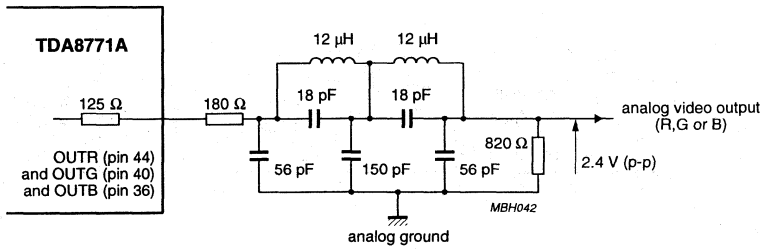


Fig.7 Example of anti-aliasing filter for 2.4 V output swing.

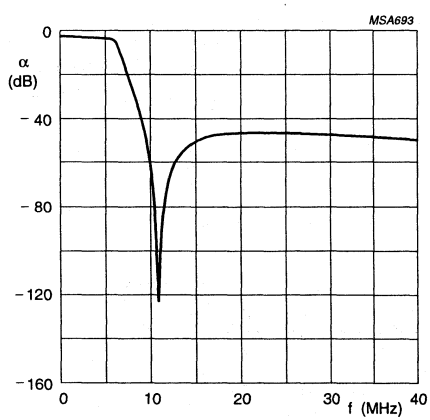


Fig.8 Frequency response for filter shown in Fig.7.

Characteristics of Fig.8

- Order 5; adapted CHEBYSHEV
- Ripple $\rho \geq 0.7$ dB
- f at –3 dB = 6.2 MHz
- f_{NOTCH} = 10.8 MHz.

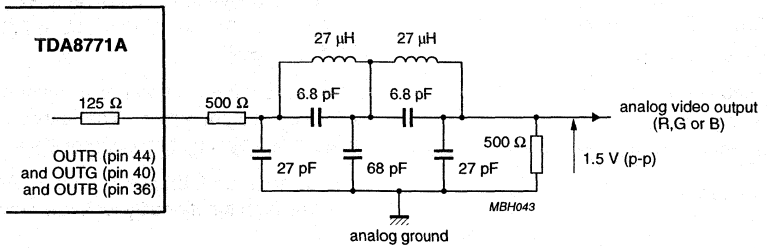


Fig.9 Example of anti-aliasing filter for 1.5 V output swing.

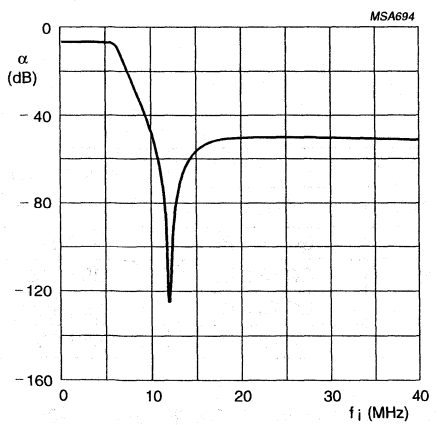


Fig.10 Frequency response for filter shown in Fig.9.

Characteristics of Fig.10

- Order 5; adapted CHEBYSHEV
- Ripple $\rho \geq 0.25$ dB
- f at −3 dB = 5.6 MHz
- f_{NOTCH} = 11.7 MHz.

Triple 8-bit video digital-to-analog converter

TDA8772; TDA8772A

FEATURES

- 8-bit resolution
- Sampling rate up to
  35 MHz for TDA8772H/3, TDA8772AH/3
  85 MHz for TDA8772H/8, TDA8772AH/8
- Internal reference voltage regulator
- No deglitching circuit required
- $\overline{\text{SYNC}}$, $\overline{\text{BLANK}}$ control inputs
- 3 independent clock inputs (one per DAC)
- 1 V output voltage range
- 75 Ω output load
- TDA8772A has $\overline{\text{BLANK}}$ control input on the GREEN channel only while TDA8772 has it on the 3 channels
- Single 5 V power supply
- 44-pin QFP package.

APPLICATIONS

- General purpose high-speed digital-to-analog conversion
- Digital TV
- Graphic display
- Desktop video processing.

GENERAL DESCRIPTION

The TDA8772, TDA8772A are triple 8-bit video digital-to-analog converters (DACs). They convert the digital input signals into analog voltage outputs at a maximum conversion rate of 35 MHz (TDA8772H/3, TDA8772AH/3) and 85 MHz (TDA8772H/8, TDA8772AH/8).

The DACs are based on resistor-string architecture with integrated output buffers. The output voltage range is determined by a built-in reference source.

The devices are fabricated in a 5 V CMOS process that ensures high functionality with low power dissipation.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE				SAMPLING FREQUENCY
	PINS	PIN POSITION	MATERIAL	CODE	
TDA8772H/3[1]	44	QFP44	plastic	SOT307B	35 MHz
TDA8772AH/3[1]	44	QFP44	plastic	SOT307B	35 MHz
TDA8772H/8[1]	44	QFP44	plastic	SOT307B	85 MHz
TDA8772AH/8[1]	44	QFP44	plastic	SOT307B	85 MHz

Note

1. Plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm; (SOT307B); SOT307-2; 1996 Oct 29.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
I_{DDA}	analog supply current	R_L = 75 Ω; note 1	40	65	100	mA
I_{DDD}	digital supply current					
	TDA8772H/3, TDA8772AH/3		–	7	16	mA
	TDA8772H/8, TDA8772AH/8		–	16	27	mA
INL	integral non-linearity2	f_{clk} = 35 MHz; ramp input	–	±0.5	±1	LSB
		f_{clk} = 85 MHz; ramp input	–	±0.75	±1.2	LSB
DNL	differential non-linearity	f_{clk} = 35 MHz; ramp input	–	±0.25	±0.5	LSB
		f_{clk} = 85 MHz; ramp input	-	±0.5	±0.75	LSB
$f_{clk(max)}$	maximum clock frequency					
	TDA8772H/3, TDA8772AH/3		35	–	–	MHz
	TDA8772H/8, TDA8772AH/8		85	–	–	MHz
P_{tot}	total power dissipation	note 1				
	TDA8772H/3, TDA8772AH/3	R_L = 75 Ω; f_{clk} = 35 MHz	180	360	640	mW
	TDA8772H/8, TDA8772AH/8	R_L = 75 Ω; f_{clk} = 85 MHz	180	405	700	mW

Note

1. Minimum and maximum data of current and power consumption are measured in worse case conditions: for minimum data, all digital inputs are at logic level 0 while for maximum data, all digital inputs are at logic level 1.

BLOCK DIAGRAMS

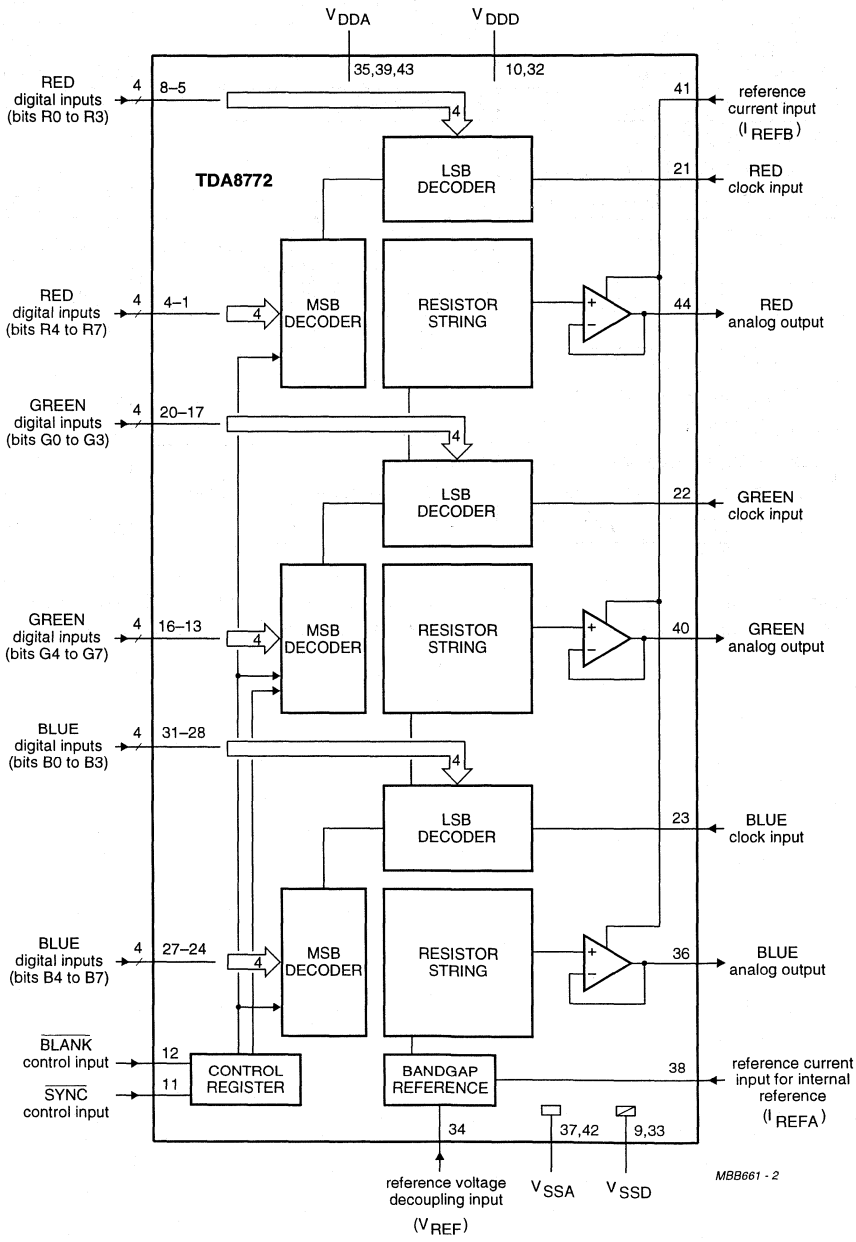


Fig.1 Block diagram for TDA8772.

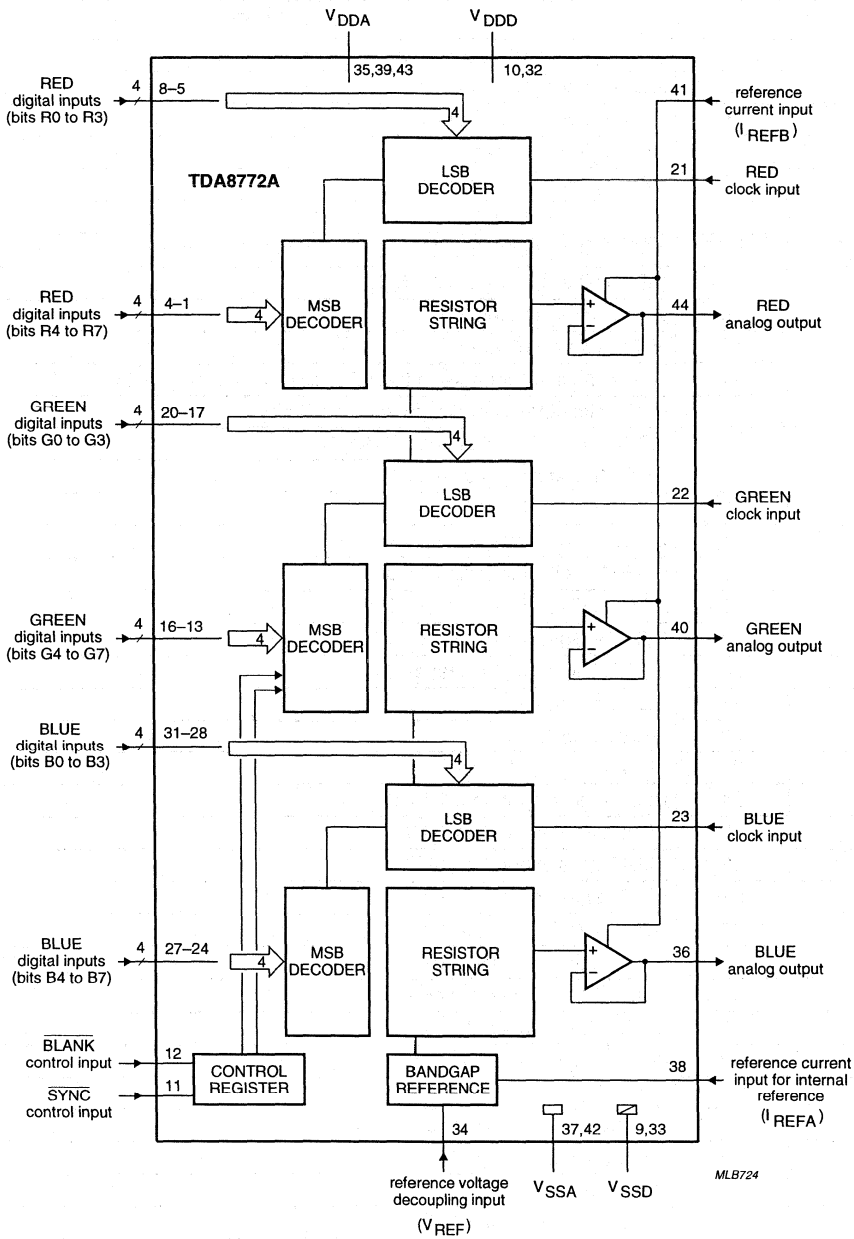


Fig.2 Block diagram for TDA8772A.

PINNING

SYMBOL	PIN	DESCRIPTION
R7	1	RED digital input data; bit 7 (MSB)
R6	2	RED digital input data; bit 6
R5	3	RED digital input data; bit 5
R4	4	RED digital input data; bit 4
R3	5	RED digital input data; bit 3
R2	6	RED digital input data; bit 2
R1	7	RED digital input data; bit 1
R0	8	RED digital input data; bit 0 (LSB)
V_{SSD1}	9	digital supply ground 1
V_{DDD1}	10	digital supply voltage 1
$\overline{SYNC}$	11	composite sync control input; for GREEN channel only (active LOW)
$\overline{BLANK}$	12	composite blank control input (active LOW)
G7	13	GREEN digital input data; bit 7 (MSB)
G6	14	GREEN digital input data; bit 6
G5	15	GREEN digital input data; bit 5
G4	16	GREEN digital input data; bit 4
G3	17	GREEN digital input data; bit 3
G2	18	GREEN digital input data; bit 2
G1	19	GREEN digital input data; bit 1
G0	20	GREEN digital input data; bit 0 (LSB)
CLKR	21	RED clock input
CLKG	22	GREEN clock input
CLKB	23	BLUE clock input
B7	24	BLUE digital input data; bit 7 (MSB)
B6	25	BLUE digital input data; bit 6
B5	26	BLUE digital input data; bit 5
B4	27	BLUE digital input data; bit 4
B3	28	BLUE digital input data; bit 3
B2	29	BLUE digital input data; bit 2
B1	30	BLUE digital input data; bit 1
B0	31	BLUE digital input data; bit 0 (LSB)
V_{DDD2}	32	digital supply voltage 2
V_{SSD2}	33	digital supply ground 2
V_{REF}	34	decoupling input for reference voltage
V_{DDA1}	35	analog supply voltage 1
OUTB	36	BLUE analog output
V_{SSA1}	37	analog supply ground 1
I_{REFA}	38	reference current input for internal reference
V_{DDA2}	39	analog supply voltage 2
OUTG	40	GREEN analog output

SYMBOL	PIN	DESCRIPTION
I_{REFB}	41	reference current input for output buffers
V_{SSA2}	42	analog supply ground 2
V_{DDA3}	43	analog supply voltage 3
OUTR	44	RED analog output

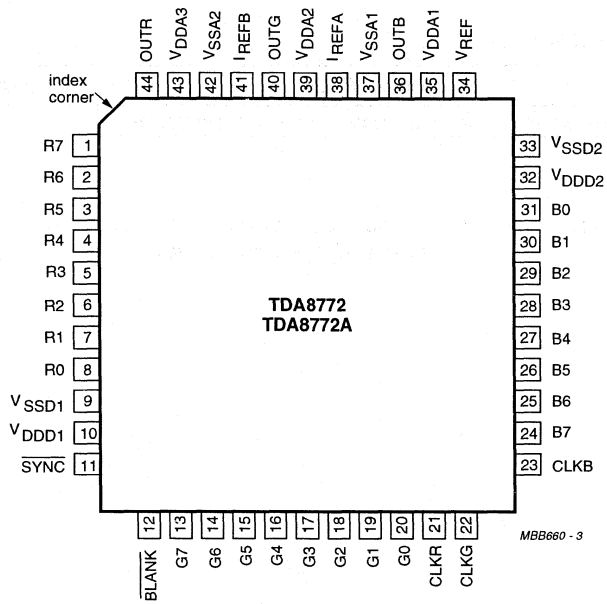


Fig.3 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage	−0.5	+6.5	V
V_{DDD}	digital supply voltage	−0.5	+6.5	V
ΔV_{DD}	supply voltage difference between V_{DDA} and V_{DDD}	−1.0	+1.0	V
T_{stg}	storage temperature	−55	+150	°C
T_{amb}	operating ambient temperature	0	+70	°C
T_j	junction temperature	−	+125	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	75	K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS

TDA8772H/3, TDA8772AH/3 operating at 35 MHz and TDA8772H/8, TDA8772AH/8 operating at 85 MHz unless otherwise specified.

$V_{DDA} = V_{DDD} = 4.5$ V to 5.5 V; V_{SSA} and V_{SSD} shorted together; $V_{DDA} - V_{DDD} = -0.5$ V to +0.5 V; $T_{amb} = 0$ to +70 °C; typical values measured at $V_{DDA} = V_{DDD} = 5$ V and $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
I_{DDA}	analog supply current	$R_L = 75\ \Omega$; note 1	40	65	100	mA
I_{DDD}	digital supply current					
	TDA8772H/3, TDA8772AH/3		–	7	16	mA
	TDA8772H/8, TDA8772AH/8		–	16	27	mA
Inputs						
CLOCK INPUTS (PINS 21, 22 AND 23)						
V_{IL}	LOW level input voltage		$V_{SSD} - 0.5$	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	$V_{DDD} + 0.5$	V
$\overline{BLANK}$, $\overline{SYNC}$ INPUTS (PINS 12 AND 11; ACTIVE LOW)						
V_{IL}	LOW level input voltage		$V_{SSD} - 0.5$	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	$V_{DDD} + 0.5$	V
R, G, B DIGITAL INPUTS (PINS 1 TO 8, 13 TO 20 AND 24 TO 31)						
V_{IL}	LOW level input voltage		$V_{SSD} - 0.5$	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	$V_{DDD} + 0.5$	V
I_{REFA} INTERNAL REFERENCE SUPPLY CURRENT (PIN 38)						
I_I	input current		–	0.17	0.25	mA
I_{REFB} OUTPUT BUFFER SUPPLY CURRENT (PIN 41)						
I_I	input current		–	0.5	0.7	mA
Timing ($C_L = 25$ pF; $R_L = 75\ \Omega$); see Fig.4						
$f_{clk(max)}$	maximum clock frequency					
	TDA8772H/3, TDA8772AH/3		35	–	–	MHz
	TDA8772H/8, TDA8772AH/8		85	–	–	MHz
t_{CPH}	clock pulse width HIGH		5	–	–	ns
t_{CPL}	clock pulse width LOW		5	–	–	ns
t_r	clock rise time					
	TDA8772H/3, TDA8772AH/3		–	–	5	ns
	TDA8772H/8, TDA8772AH/8		–	–	3	ns
t_f	clock fall time					
	TDA8772H/3, TDA8772AH/3		–	–	5	ns
	TDA8772H/8, TDA8772AH/8		–	–	3	ns
$t_{SU;DAT}$	input data set-up time		4	–	–	ns
$t_{HD;DAT}$	input data hold time		2.5	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Voltage reference (pin 34, referenced to V_{SSA})						
V_{REF}	output reference voltage		1.180	1.242	1.305	V
Outputs						
OUTB, OUTR, OUTG ANALOG OUTPUTS (PINS 36, 44 AND 40, REFERENCED TO V_{SSA}) FOR 75 Ω LOAD; see Tables 1 and 2						
FSR	full-scale output voltage range		0.9	1.0	1.1	V
V_{os}	offset of analog voltage output		0.75	0.83	0.95	V
V_{OUTmax}	maximum output voltage	data inputs = logic 1; note 2	1.65	1.83	2.05	V
V_{OUTmin}	minimum output voltage	data inputs = logic 0; note 2	0.75	0.83	0.95	V
THD	total harmonic distortion	f_i = 4.43 MHz; f_{clk} = 35 MHz	–	–45	–	dB
		f_i = 4.43 MHz; f_{clk} = 85 MHz	–	–43	–	dB
Z_L	output load impedance		60	75	90	Ω
Transfer function						
INL	integral non-linearity	f_{clk} = 35 MHz; ramp input	–	±0.5	±1	LSB
		f_{clk} = 85 MHz; ramp input	–	±0.75	±1.2	LSB
DNL	differential non-linearity	f_{clk} = 35 MHz; ramp input	–	±0.25	±0.5	LSB
		f_{clk} = 85 MHz; ramp input	-	±0.5	±0.75	LSB
α_{CT}	crosstalk DAC to DAC		–45	–	–	dB
	DAC to DAC matching		–	1.0	2.0	%
Switching characteristics (for 75 Ω output load); see Fig.5						
t_d	input to 50% output delay time	full-scale change	–	10	–	ns
t_{s1}	settling time	10% to 90% full-scale change	–	6	–	ns
t_{s2}	settling time	to ±1 LSB	–	30	–	ns
Output transients (glitches)						
V_g	area for 1 LSB change		–	1	–	LSB.ns

Notes

1. Minimum and maximum data of current and power consumption are measured in worse case conditions: for minimum data, all digital inputs are at logic level 0 while for maximum data, all digital inputs are at logic level 1.
2. V_{OUT} is directly proportional to V_{REF}.

Table 1 Input coding and DAC output voltages (typical values)

BINARY INPUT DATA (SYNC = BLANK = 0)	CODE	DAC OUTPUT VOLTAGES (V) OUTB, OUTR, OUTG R_L = 75 Ω
0000 0000	0	0.830
0000 0001	1	0.834
....	.	.
1000 0000	128	1.330
....	.	.
1111 1110	254	1.826
1111 1111	255	1.830

Table 2 Input coding and DAC output voltages (typical values)

BINARY INPUT DATA	$\overline{\text{SYNC}}$ (PIN 11)	$\overline{\text{BLANK}}$ (PIN 12)	DAC OUTPUT VOLTAGES (V)		
			OUTG (PIN 40)	OUTR/B (PINS 44, 46) TDA8772	OUTR/B (PINS 44, 46) TDA8772A
....	x	1	see Table 1	see Table 1	see Table 1
....	1	0	0.830	0.830	
....	0	0	0.440		

TIMING

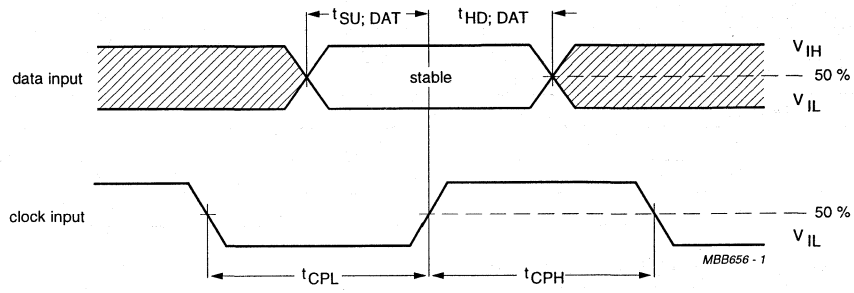


Fig.4 Input timing.

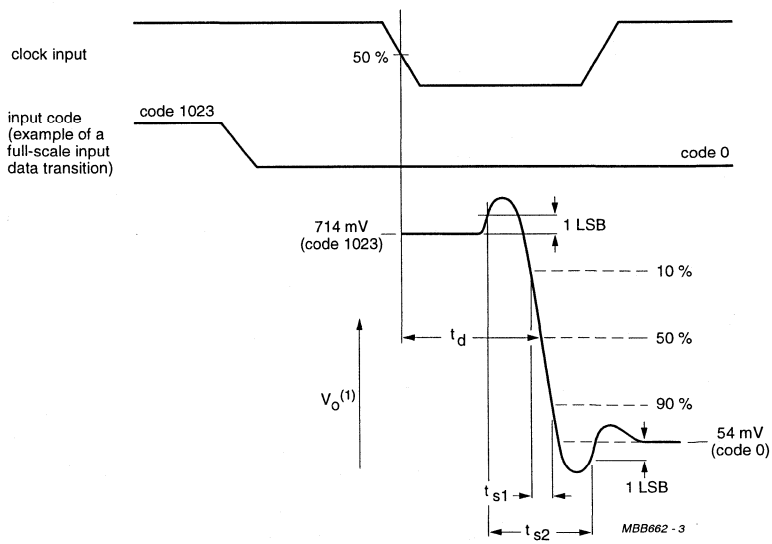
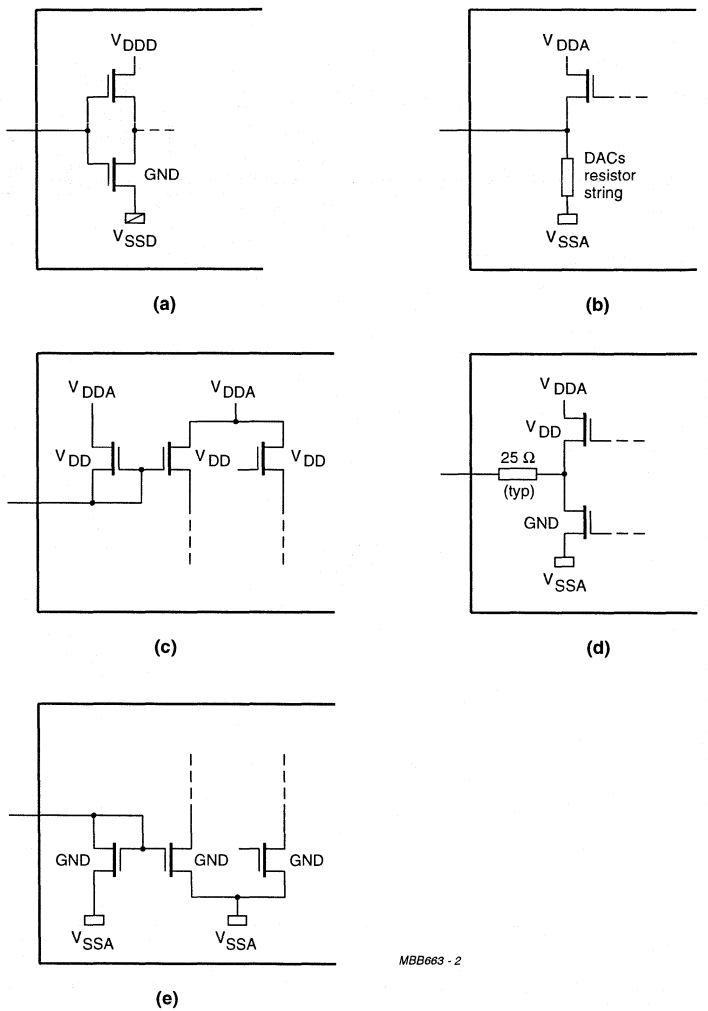


Fig.5 Switching timing.

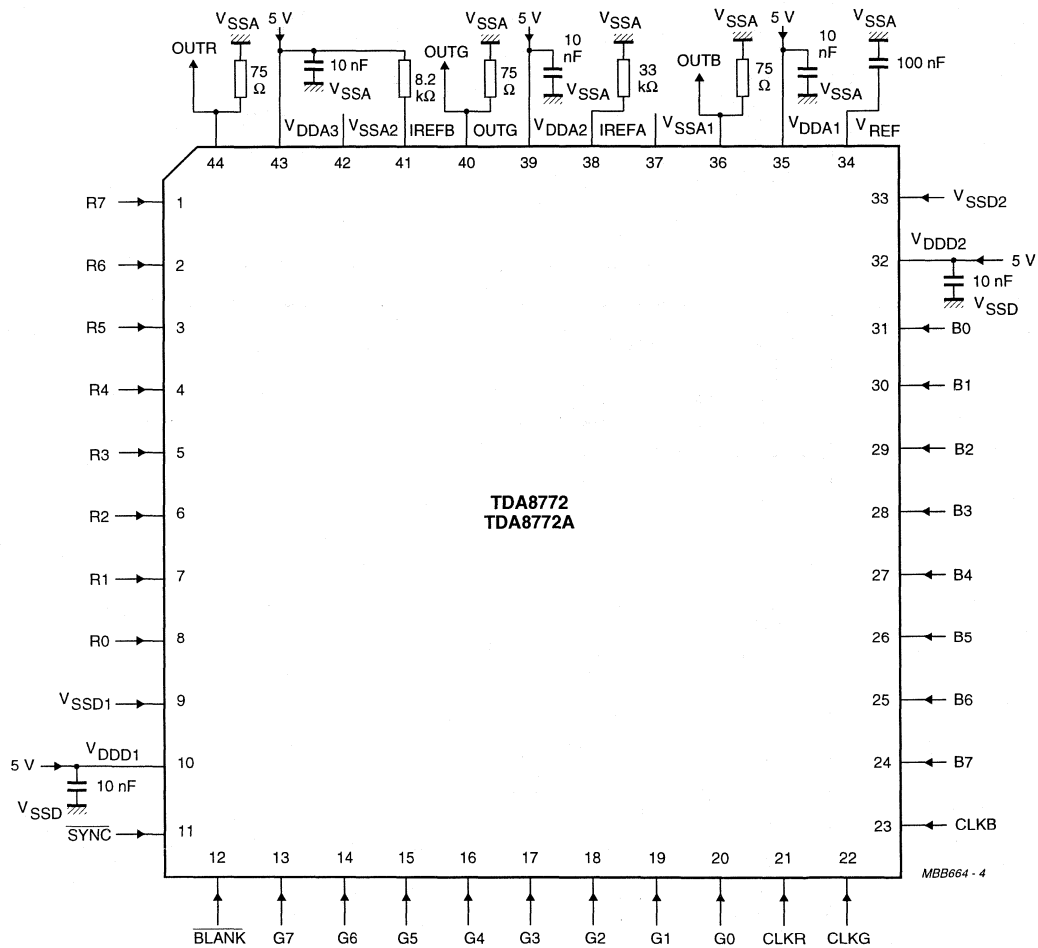
INTERNAL CIRCUITRY



(a) Digital inputs; pins 1 to 8 and 11 to 31.
(b) VREF; pin 34.
(c) IREFA; pin 38.
(d) OUTR, G, B; pins 44, 40 and 36.
(e) IREFB; pin 41.

Fig.6 Internal circuitry.

APPLICATION INFORMATION



Analog and digital supplies should be separated and decoupled.
Supplies are not connected internally.
All ground pins must be connected. One ground plane is preferred although it depends on the application.
See Fig.8 for example of anti-aliasing filter.

Fig.7 Application diagram.

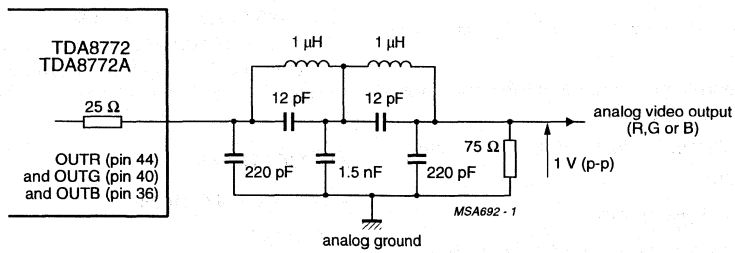


Fig.8 Example of anti-aliasing filter for 1 V output swing.

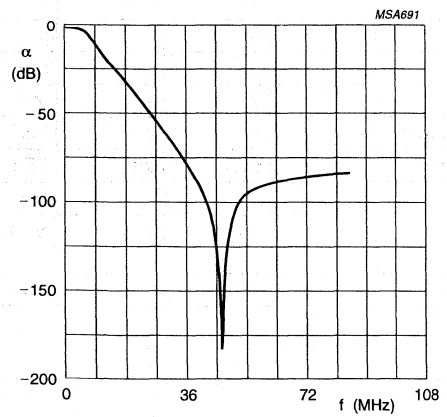


Fig.9 Frequency response for filter shown in Fig.8.

Characteristics of Fig.9

- Order 5; adapted CHEBYSHEV
- Ripple $\rho \geq 0.6$ dB
- f at −3 dB = 6.5 MHz
- f_{NOTCH} = 46 MHz.

8-bit high-speed analog-to-digital converter with gain and offset controls

TDA8785

FEATURES

- 8-bit analog-to-digital converter (ADC)
- 8-bit digital-to-analog converter (DAC)
- Sampling rate up to 30 Msps for both ADC and DAC
- Binary or two's complement 3-state TTL outputs
- TTL compatible inputs and outputs
- 100 MHz variable gain amplifier (0 to 20 dB) externally controlled
- All analog inputs and outputs are differential (can also be used in single-ended format)
- Analog input signal from 0.1 to 1.0 V (p-p) differential
- Offset amplifier with:
  - slow offset control (±250 mV)
  - fast offset control (±500 mV) eventually driven by internal DAC
- ADC output code of 8 (typ.) when analog input signal and offset correction inputs are 0 V
- Gain, slow offset control inputs and DAC output swing of 1.5 V (p-p) range (2.75 ±0.75 V)
- 2.75 V reference voltage
- Internal references for ADC and DAC.

GENERAL DESCRIPTION

The TDA8785 is an 8-bit analog-to-digital converter with gain and offset controls for the input signal. An internal 8-bit DAC provides digital adjustment of the different input offsets.

APPLICATIONS

- CCD type of systems
- Scanner
- Copier
- Video acquisition.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA1}	analog supply voltage 1		4.75	5.0	5.25	V
V_{CCA2}	analog supply voltage 2		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	TTL output supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current		–	80	–	mA
I_{CCD}	digital supply current		–	30	–	mA
I_{CCO}	TTL output supply current		–	9	–	mA
INL	integral non-linearity	0 to 20 dB gain; ramp input	–	±0.7	tbf	LSB
DNL	differential non-linearity	0 to 20 dB gain; ramp input	–	±0.4	tbf	LSB
$f_{clk(max)}$	maximum clock frequency	ADC and DAC	30	–	–	MHz
B	controlled gain amplifier bandwidth		–	100	–	MHz
P_{tot}	total power dissipation		–	600	–	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8785H	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2

8-bit high-speed analog-to-digital converter with gain and offset controls

TDA8785

BLOCK DIAGRAM

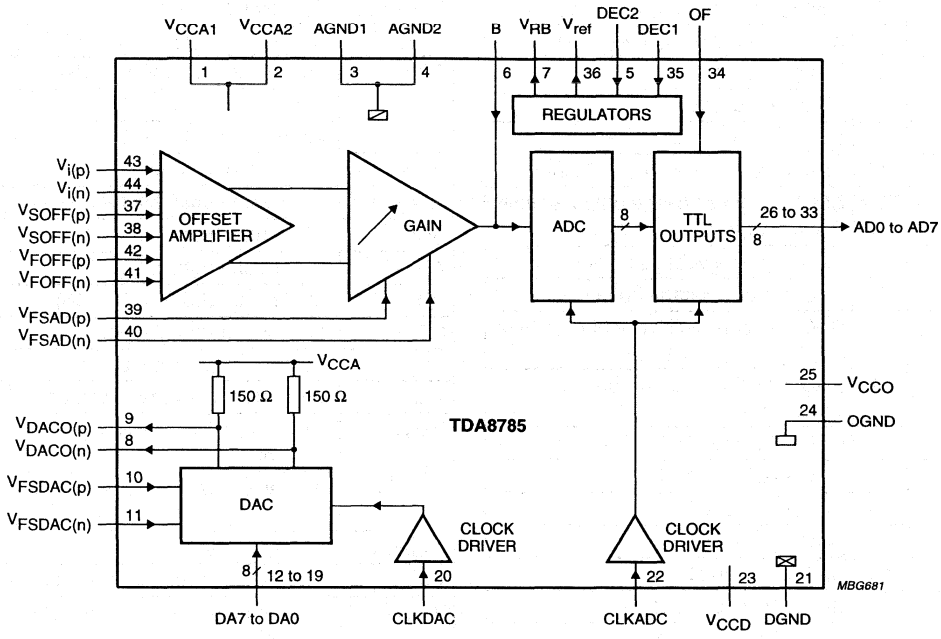


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{CCA1}	1	analog supply voltage 1 (+5 V)
V_{CCA2}	2	analog supply voltage 2 (+5 V)
AGND1	3	analog ground 1
AGND2	4	analog ground 2
DEC2	5	decoupling input 2
B	6	bandwidth adjustment node input
V_{RB}	7	ADC reference voltage output bottom (decoupling)
$V_{DACO(n)}$	8	DAC negative voltage output
$V_{DACO(p)}$	9	DAC positive voltage output
$V_{FSDAC(p)}$	10	DAC full-scale positive control voltage input
$V_{FSDAC(n)}$	11	DAC full-scale negative control voltage input
DA7	12	DAC TTL input; bit 7 (MSB)
DA6	13	DAC TTL input; bit 6
DA5	14	DAC TTL input; bit 5
DA4	15	DAC TTL input; bit 4
DA3	16	DAC TTL input; bit 3
DA2	17	DAC TTL input; bit 2
DA1	18	DAC TTL input; bit 1
DA0	19	DAC TTL input; bit 0 (LSB)
CLKDAC	20	DAC clock input
DGND	21	digital ground
CLKADC	22	ADC clock input
V_{CCD}	23	digital supply voltage (+5 V)

SYMBOL	PIN	DESCRIPTION
OGND	24	output ground
V_{CCO}	25	output supply voltage (+5 V)
AD0	26	output data; bit 0 (LSB)
AD1	27	output data; bit 1
AD2	28	output data; bit 2
AD3	29	output data; bit 3
AD4	30	output data; bit 4
AD5	31	output data; bit 5
AD6	32	output data; bit 6
AD7	33	output data; bit 7 (MSB)
OF	34	output format input
DEC1	35	decoupling input 1
V_{ref}	36	reference voltage output (2.75 V)
$V_{SOFF(p)}$	37	slow offset amplifier positive voltage input
$V_{SOFF(n)}$	38	slow offset amplifier negative voltage input
$V_{FSAD(p)}$	39	gain control positive voltage input
$V_{FSAD(n)}$	40	gain control negative voltage input
$V_{FOFF(n)}$	41	fast offset amplifier negative voltage input
$V_{FOFF(p)}$	42	fast offset amplifier positive voltage input
$V_{i(p)}$	43	analog positive voltage input
$V_{i(n)}$	44	analog negative voltage input

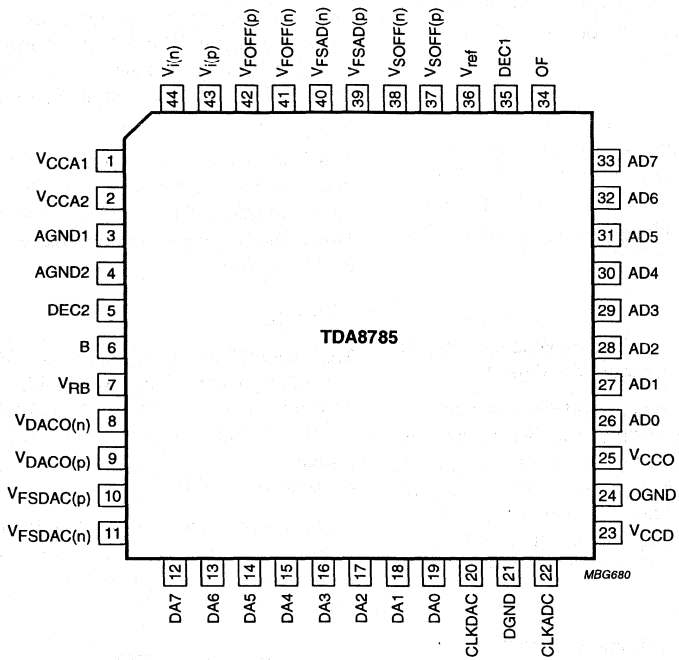


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA8785 is composed of an 8-bit ADC (30 Msps), a wide-band gain amplifier, an input offset amplifier and an 8-bit dynamic adjustment DAC.

Input signal

Two input pins are provided to apply a differential input signal with a wide range (100 to 1000 mV differential). It is also possible to apply a single signal by setting a DC voltage on one of the differential pins and supplying the signal to the other.

Controlled gain amplifier

The gain amplifier is used to adjust the wide input signal range to the fixed ADC input range of 1 V (p-p).

A large gain of 20 dB can be achieved with low-noise behaviour and a large bandwidth of 100 MHz to correctly amplify square type signals with step edges. Using pin 6, it is possible to reduce the internal bandwidth of the gain amplifier via an external capacitor and thus improve its noise behaviour. The gain amplifier is controlled via an external differential voltage (single input can also be applied).

Input offset amplifier and adjustment DAC

The Input offset amplifier contains two different control inputs (which can also be single):

- Slow offset control, for slow variation characteristics (e.g. temperature, supply voltage, etc.)
- Fast offset control, for correction related to the clock rate.

Slow offset control is carried out by an external voltage while fast offset control is digitally carried out via the internal 8-bit DAC with external connections of the respective pins $V_{DACO(n)}$, $V_{DACO(p)}$, $V_{FOFF(n)}$ and $V_{FOFF(p)}$.

The internal 8-bit DAC operates at the ADC clock rate to allow dynamic corrections on the input signal chain based on the signal processing information carried out after the digital conversion. The output voltage amplitude of the DAC can be controlled via a different input voltage (which can also be single) in a range of ±25% with a 150 Ω DAC output load.

The DAC can also be used for the gain or the slow offset control with some external DC voltage adaptations and can be considered as a separate function of the ADC chain. The DAC can be used independently, for example as a video DAC.

8-bit ADC

The 8-bit ADC converts a signal of 1 V (p-p) from the controlled gain amplifier into an 8-bit coded digital word at a maximum rate of 30 Msps. Its reference voltage is supplied by the general voltage regulator. The output data format can either be binary, two's complement or 3-state by selecting pin OF.

When all the differential inputs on the offset amplifier ($V_{SOFF(p)}$, $V_{SOFF(n)}$, $V_{FOFF(n)}$, $V_{FOFF(p)}$, $V_{i(p)}$ and $V_{i(n)}$) are at 0 V (equivalent to both inputs short-circuited), the output code of the ADC is code 8.

Internal voltage regulator

An internal voltage regulator provides all the references for the different blocks. A stable 2.75 V voltage reference output is provided for use in the application environment. One application is to connect all the slow control inputs ($V_{FSDAC(p)}$, $V_{FSDAC(n)}$, $V_{SOFF(p)}$, $V_{SOFF(n)}$, $V_{FSAD(p)}$ and $V_{FSAD(n)}$) to this reference, either to their two differential inputs to get the nominal settings or to one of the differential inputs to have easy single-input control.

All these control inputs have the same control range.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage		−0.3	+7.0	V
V_{CCD}	digital supply voltage		−0.3	+7.0	V
V_{CCO}	output supply voltage		−0.3	+7.0	V
ΔV_{CC}	supply voltage difference between				
	V_{CCA} and V_{CCD}		−1.0	+1.0	V
	V_{CCD} and V_{CCO}		−1.0	+1.0	V
	V_{CCA} and V_{CCO}		−1.0	+1.0	V
V_I	input voltage	referenced to AGND	−0.3	+7.0	V
$V_{clk(p-p)}$	clock input voltage for switching (peak-to-peak value)	referenced to DGND	−	V_{CCD}	V
I_O	output current		−	6	mA
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		0	70	°C
T_j	junction temperature		−	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	75	K/W

CHARACTERISTICS

$V_{CCA1} = V_{CCA2} = V_{CCD} = V_{CCO}$ = 4.75 to 5.25 V; AGND, DGND and OGND short-circuited together; V_{CCA} to $V_{CCD} = V_{CCD}$ to $V_{CCO} = V_{CCA}$ to V_{CCO} = –0.25 to +0.25 V; T_{amb} = 0 to 70 °C; typical values measured at $V_{CCA} = V_{CCD} = V_{CCO}$ = 5 V and T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CCA1}	analog supply voltage 1		4.75	5.0	5.25	V
V_{CCA2}	analog supply voltage 2		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	TTL output supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current		–	80	–	mA
I_{CCD}	digital supply current		–	30	–	mA
I_{CCO}	TTL output supply current		–	9	–	mA
Reference voltages (pins V_{ref} and V_{RB})						
V_{ref}	output reference voltage		2.60	2.75	2.90	V
V_{line}	line regulation voltage	V_{CCA} = 4.75 to 5.25 V	–	4	–	mV
I_{LO}	output load current		–1	–	–	mA
V_{RB}	reference voltage output bottom (decoupling)		–	V_{CCA} – 2.5	–	V
V_{osB}	offset voltage bottom	code 0 – V_{RB}	–	250	–	mV
ΔV_{ADC}	ADC reference voltage difference	between code 0 and 255	–	1	–	V
Analog inputs (pins $V_{I(p)}$ and $V_{I(n)}$); see Table 1						
$V_{i(p-p)}$	differential input voltage $V_{i(p)} - V_{i(n)}$ (peak-to-peak value)	0 dB gain	–	1000	–	mV
		20 dB gain	–	100	–	mV
V_I	DC input voltage		–	3.0	–	V
I_i	input current		–	10	–	µA
Z_i	input impedance		–	20	–	kΩ
C_i	input capacitance		–	1	–	pF
Fast amplifier inputs (pins $V_{FOFF(p)}$ and $V_{FOFF(n)}$); DC parameters						
$V_{FOFF(p)}$	input voltage	0 dB gain	–	500	–	mV
		20 dB gain	–	50	–	mV
$V_{FOFF(n)}$	input voltage	0 dB gain	–	500	–	mV
		20 dB gain	–	50	–	mV
V_I	DC input voltage		–	V_{CCA} – 0.25	–	V
I_i	input current		–	10	–	µA
Z_i	input impedance		–	20	–	kΩ
C_i	input capacitance		–	1	–	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Slow offset amplifier inputs (pins $V_{SOFF(p)}$ and $V_{SOFF(n)}$) gain amplifier at 0 dB; note 1						
V_{os}	offset voltage at ADC input	$V_{SOFF(p)}$ = 2 V; $V_{SOFF(n)}$ = 2.75 V	–	–0.25	–	V
		$V_{SOFF(p)}$ = 2.75 V; $V_{SOFF(n)}$ = 2.75 V	–	0	–	V
		$V_{SOFF(p)}$ = 3.5 V; $V_{SOFF(n)}$ = 2.75 V	–	+0.25	–	V
I_i	input current		–	10	–	µA
Offset reference code; T_{amb} = 25 °C						
OFSRE	offset reference (ADC output code)	$V_{i(p)} = V_{i(n)}$; $V_{FOFF(p)} = V_{FOFF(n)}$; $V_{SOFF(p)} = V_{SOFF(n)}$; amplifier gain set at 0 dB	–	8	–	code
OFSER	offset reference error on code 8		tbf	0	tbf	code
Gain control inputs (pins $V_{FSAD(p)}$ and $V_{FSAD(n)}$); see Fig.7						
$G_{v(min)}$	minimum voltage gain	$V_{FSAD(p)}$ = 2 V; $V_{FSAD(n)}$ = 2.75 V	–	–	0	dB
$G_{v(max)}$	maximum voltage gain	$V_{FSAD(p)}$ = 3.5 V; $V_{FSAD(n)}$ = 2.75 V	20	–	–	dB
I_i	input current		–	10	–	µA
DAC full-scale control inputs (pins $V_{FSDAC(p)}$ and $V_{FSDAC(n)}$) 150 Ω output load on pins $V_{DACO(p)}$ and $V_{DACO(n)}$; see Table 3						
$V_{DACO(n)}$	DAC output voltage (pin 8)	code 0 at DAC inputs	–	V_{CCA}	–	V
		code 255 at DAC inputs; $V_{FSDAC(p)}$ = 2 V; $V_{FSDAC(n)}$ = 2.75 V	–	V_{CCA} – 0.4	–	V
		code 255 at DAC inputs; $V_{FSDAC(p)}$ = 2.75 V; $V_{FSDAC(n)}$ = 2.75 V	–	V_{CCA} – 0.5	–	V
		code 255 at DAC inputs; $V_{FSDAC(p)}$ = 3.5 V; $V_{FSDAC(n)}$ = 2.75 V	–	V_{CCA} – 0.6	–	V
I_i	input current		–	2	–	µA
Bandwidth adjustment node input (pin B); see Fig.6						
Z_i	input impedance		–	500	–	Ω
8-bit DAC; f_{clk} = 30 MHz, ramp input; T_{amb} = 25 °C						
Z_o	output impedance		–	150	–	Ω
INL	integral non-linearity		–	±0.4	tbf	LSB
DNL	differential non-linearity		–	±0.4	tbf	LSB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital inputs (pins CLKDAC, CLKADC and DA7 to DA0)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_{clk} = 0.4 V	–400	–	–	µA
I_{IH}	HIGH level input current	V_{clk} = 2.7 V	–	–	100	µA
Z_i	input impedance	f_{clk} = 10 MHz	–	4	–	kΩ
C_i	input capacitance	f_{clk} = 10 MHz	–	4.5	–	pF
ADC output format (pin OF); see Table 2						
V_{IL}	LOW level input voltage		0	–	0.2	V
V_{IH}	HIGH level input voltage		2.6	–	V_{CCD}	V
V_I	input voltage in high impedance state		–	1.15	–	V
I_{IL}	LOW level input current	V_{clk} = 0.4 V	–370	–300	–	µA
I_{IH}	HIGH level input current	V_{clk} = 2.7 V	–	300	450	µA
ADC digital outputs						
V_{OL}	LOW level output voltage	I_{OL} = 2 mA	0	–	0.6	V
V_{OH}	HIGH level output voltage	I_{OH} = –0.4 mA	2.4	–	V_{CCO}	V
ADC and DAC switching; see Fig.4						
$f_{clk(max)}$	maximum clock frequency	note 2	30	–	–	MHz
t_{CPH}	clock pulse width HIGH		12	–	–	ns
t_{CPL}	clock pulse width LOW		12	–	–	ns
Analog processing; note 3						
INL	integral non-linearity	ramp input (full scale); 0 to 20 dB gain	–	±0.7	tbf	LSB
DNL	differential non-linearity	ramp input (full scale); 0 to 20 dB gain		±0.4	tbf	LSB
S/N	signal-to-noise ratio (without harmonics)	f_i = 4.43 MHz				
		0 dB gain	–	47	–	dB
		10 dB gain	–	45	–	dB
		20 dB gain	–	43	–	dB
B	bandwidth	–3 dB	–	100	–	MHz
t_S	settling time	note 4	–	2	–	code

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing						
ADC DIGITAL OUTPUTS (C_L = 15 pF)						
t_{ds}	sampling delay time		–	1.5	–	ns
t_h	output hold time		7	–	–	ns
t_d	output delay time		–	–	16	ns
DAC OUTPUTS (PINS $V_{DACO(p)}$ AND $V_{DACO(n)}$)						
$t_{SU;\ DAT}$	data set-up time	note 5	−0.3	–	–	ns
$t_{HD;\ DAT}$	data hold time	note 5	–	–	2	ns
t_S	DAC settling time (1% accuracy)	R_L = 150 Ω; C_L = 15 pF	–	8	–	ns
3-STATE OUTPUT DELAY TIMES (see Fig.5)						
t_{dZH}	enable HIGH		–	12	14	ns
t_{dZL}	enable LOW		–	10	12	ns
t_{dHZ}	disable HIGH		–	58	62	ns
t_{dLZ}	disable LOW		–	70	74	ns

Notes

1. V_{os} is proportional to the amplifier gain. For instance, V_{os} at 20 dB is the one indicated at 0 dB multiplied by 10.
2. It is recommended that the rise and fall times of the clock are >1 ns. In addition a good layout for the digital and analog grounds is recommended.
3. Analog processing from signal inputs or fast offset amplifier inputs to ADC digital output; f_{clk} = 30 MHz; no external filtering on pin 6 (B).
4. Settling time is the number of code variations at the ADC output, after one clock period settling. A full-scale jump is applied at the DAC inputs, with the DAC output (square signal) connected to the fast offset amplifier input. ADC and DAC clock signals (CLKADC and CLKDAC) are in phase.
5. The data set-up time ($t_{SU;\ DAT}$) is the minimum period preceding the rising edge of the clock, that the input data must be stable in order to be correctly registered. A negative set-up time indicates that the data may be initiated after the rising edge and still be recognized. The data set hold time ($t_{HD;\ DAT}$) is the minimum period following the rising edge of the clock, that the input data must be stable in order to be correctly registered. A negative hold time indicates that the data may be released prior to the rising edge and still be recognized.

Table 1 Output coding and input voltage (typical values; referenced to AGND, $V_{i(p)} - V_{i(n)}$ = 1 V (p-p), 0 dB gain, no offset correction

STEP	$V_{i(p)} - V_{i(n)}$	BINARY OUTPUT BITS								TWO'S COMPLEMENT OUTPUT BITS							
		D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Underflow	<–0.032	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0	–0.032	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	–	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1
.	–	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
8	0	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0
.	–	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
254	–	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0
255	0.968	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
Overflow	>0.968	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1

Table 2 OF input coding

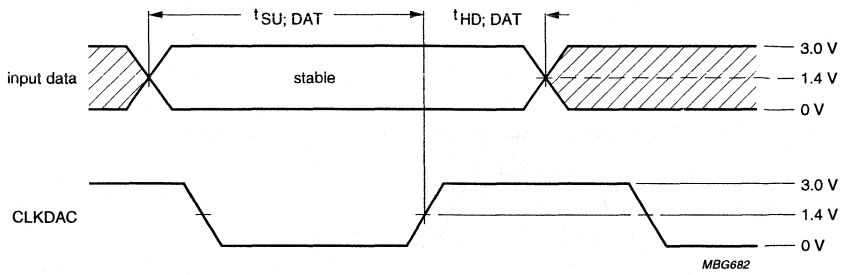
OF	AD0 to AD7
0	active, two's complement
1	high impedance
open circuit(1)	active, binary

Note

1. Use C ≥ 10 pF to DGND.

Table 3 Input coding and DAC output voltages (typical values; referenced to V_{CCA} regardless of the offset voltage); $V_{FSDAC(p)} = V_{FSDAC(n)}$

CODE	BINARY INPUT DATA								DAC OUTPUT VOLTAGES (V)			
	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	Z_L = 10 kΩ		Z_L = 150 Ω	
									$V_{DACO(p)}$	$V_{DACO(n)}$	$V_{DACO(p)}$	$V_{DACO(n)}$
0	0	0	0	0	0	0	0	0	–1.0	0	–0.5	0
1	0	0	0	0	0	0	0	1	–	–	–	–
.	.	.	.	.	.	.	.	.	.	.	.	.
128	1	0	0	0	0	0	0	0	–0.5	–0.5	–0.25	–0.25
.	.	.	.	.	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0	–	–	–	–
255	1	1	1	1	1	1	1	1	0	–1.0	0	–0.5



The shaded areas indicate when the input data may change and be correctly registered. Data input update must be completed within 0.3 ns, after the first rising edge of the clock ($t_{SU;\,DAT}$ is negative; −0.3 ns). Data must be held at least 2 ns after the rising edge ($t_{HD;\,DAT}$ = +2 ns).

Fig.3 Data set-up and hold times (DAC).

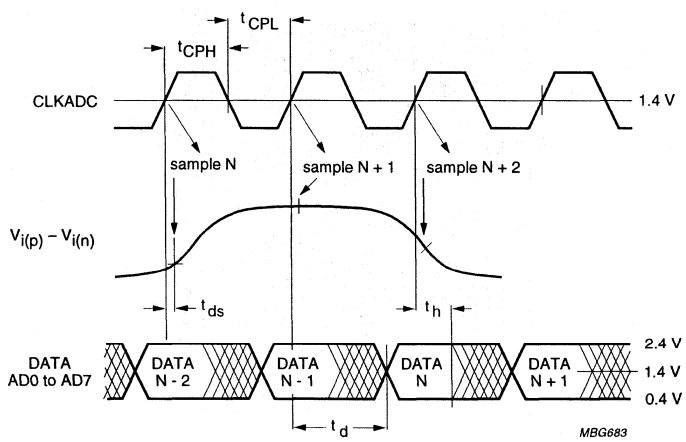
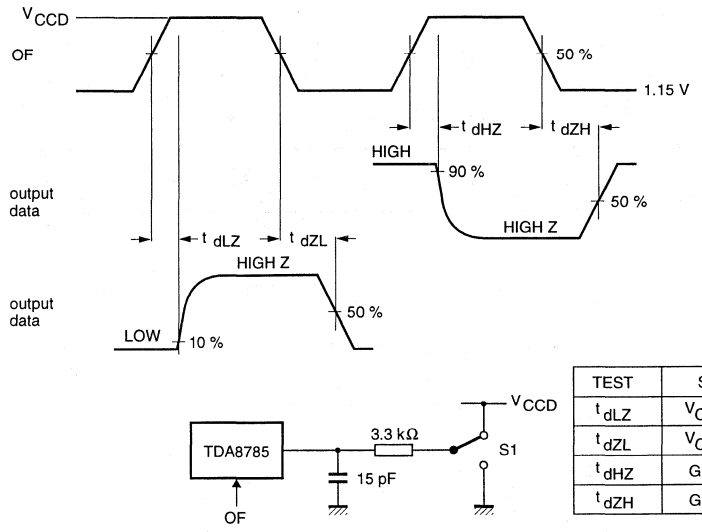


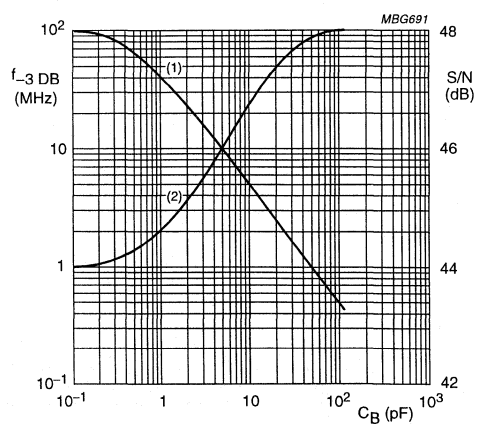
Fig.4 Timing diagram



TEST	S1
t_{dLZ}	V_{CCD}
t_{dZL}	V_{CCD}
t_{dHZ}	GND
t_{dZH}	GND

f_{OF} = 100 kHz.

Fig.5 Timing diagram and test conditions of 3-state output delay time.



(1) $f_{-3\ dB}$.
(2) Signal-to-noise ratio.
The controlled gain amplifier is set at 20 dB gain.

Fig.6 Gain amplifier bandwidth and acquisition chain S/N ratio as a function of the external capacitance on pin 6.

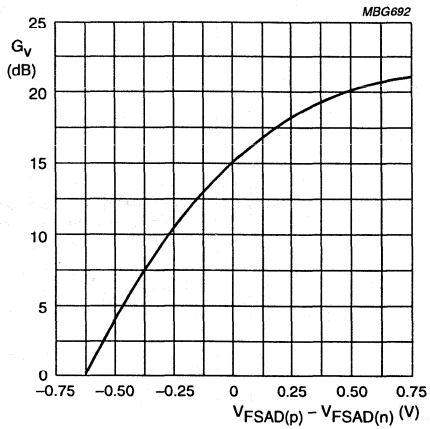


Fig.7 Typical amplifier gain (G_v) as a function of the differential input voltage; $V_{FSAD(p)} - V_{FSAD(n)}$.

INTERNAL PIN CONFIGURATIONS

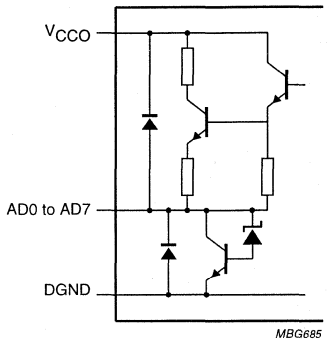


Fig.8 TTL data outputs.

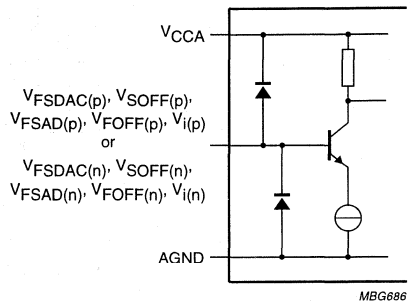


Fig.9 Analog inputs.

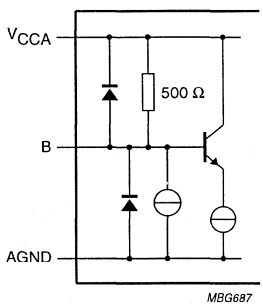


Fig.10 Bandwidth input (B).

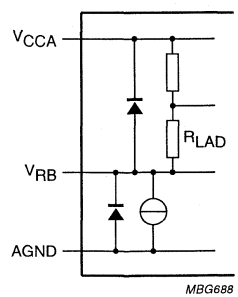


Fig.11 V_{RB}.

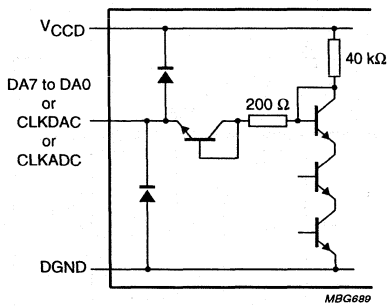


Fig.12 DAC inputs.

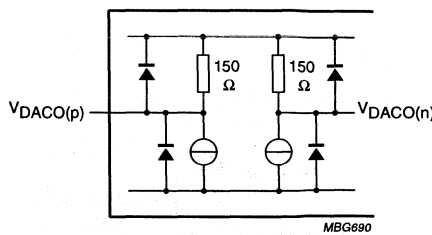


Fig.13 DAC outputs.

APPLICATION INFORMATION

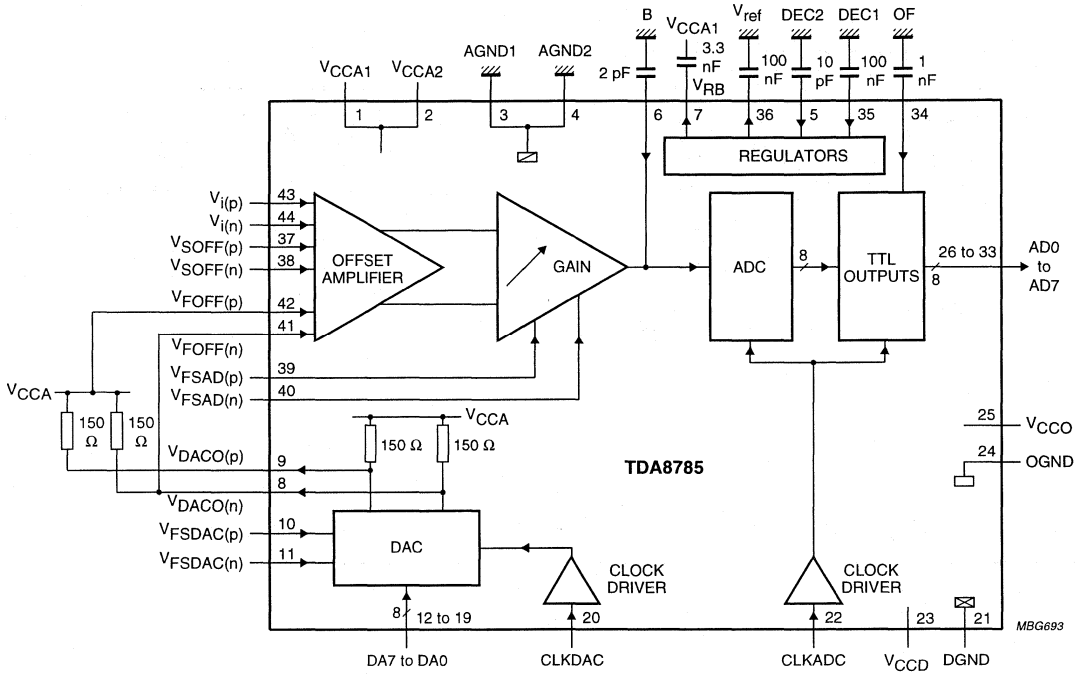


Fig.14 Application diagram.

10-bit analog-to-digital interface for CCD cameras

TDA8786; TDA8786A

FEATURES

- Correlated double sampling (CDS), AGC, soft clipper, pre- blanking, 10-bit ADC and reference regulator included
- Fully programmable via a 3-wire serial interface
- Sampling frequency up to 18 MHz
- AGC gain from 3.5 dB to 33.5 dB (in 0.1 dB steps)
- Programmable soft clipper for white compression (starting at 40% of the input signal)
- Standby mode available for each block for power saving applications
- 6 dB fixed gain analog output for analog iris control
- 8-bit and 10-bit DAC included for analog settings
- Low power consumption of only 400 mW (typ.)
- 5 V operation and 2.5 to 5 V operation for the digital outputs
- Active control pulse: TDA8786 = HIGH; TDA8786A = LOW
- TTL compatible inputs, TTL and CMOS compatible outputs.

GENERAL DESCRIPTION

The TDA8786; TDA8786A is a 10-bit analog-to-digital interface for CCD cameras. The device includes a correlated double sampling circuit, AGC, a soft clipper circuit and a low power 10-bit analog-to-digital converter (ADC) together with its reference voltage regulator.

The AGC and soft clipper circuits are controlled by on-chip DACs via a serial interface.

A 10-bit DAC controls the ADC input clamp level.

A pre-blanking function is also included.

An additional DAC is provided for additional system controls; its output voltage range is 1 V (p-p) which is available at pin OFD.

APPLICATIONS

- CCD camera systems.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.5	4.75	5.5	V
V_{CCD}	digital supply voltage		4.5	4.75	5.5	V
V_{CCO}	digital outputs supply voltage		2.5	2.6	5.5	V
I_{CCA}	analog supply current		–	67	–	mA
I_{CCD}	digital supply current		–	15	–	mA
I_{CCO}	digital outputs supply current	f_{CLK} = 18 MHz; C_L = 20 pF; ramp input	–	1	–	mA
ADC_{res}	ADC resolution		–	10	–	bits
$V_{iCDS(p-p)}$	CDS input voltage (peak-to-peak value)		–	400	1200	mV
G_{CDS}	CDS output amplifier gain		–	6	–	dB
$f_{ss(max)}$	maximum clock frequency		18	–	–	MHz
AGC_{dyn}	AGC dynamic range		–	30	–	dB
P_{tot}	total power consumption		–	400	–	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8786	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
TDA8786A			

BLOCK DIAGRAM

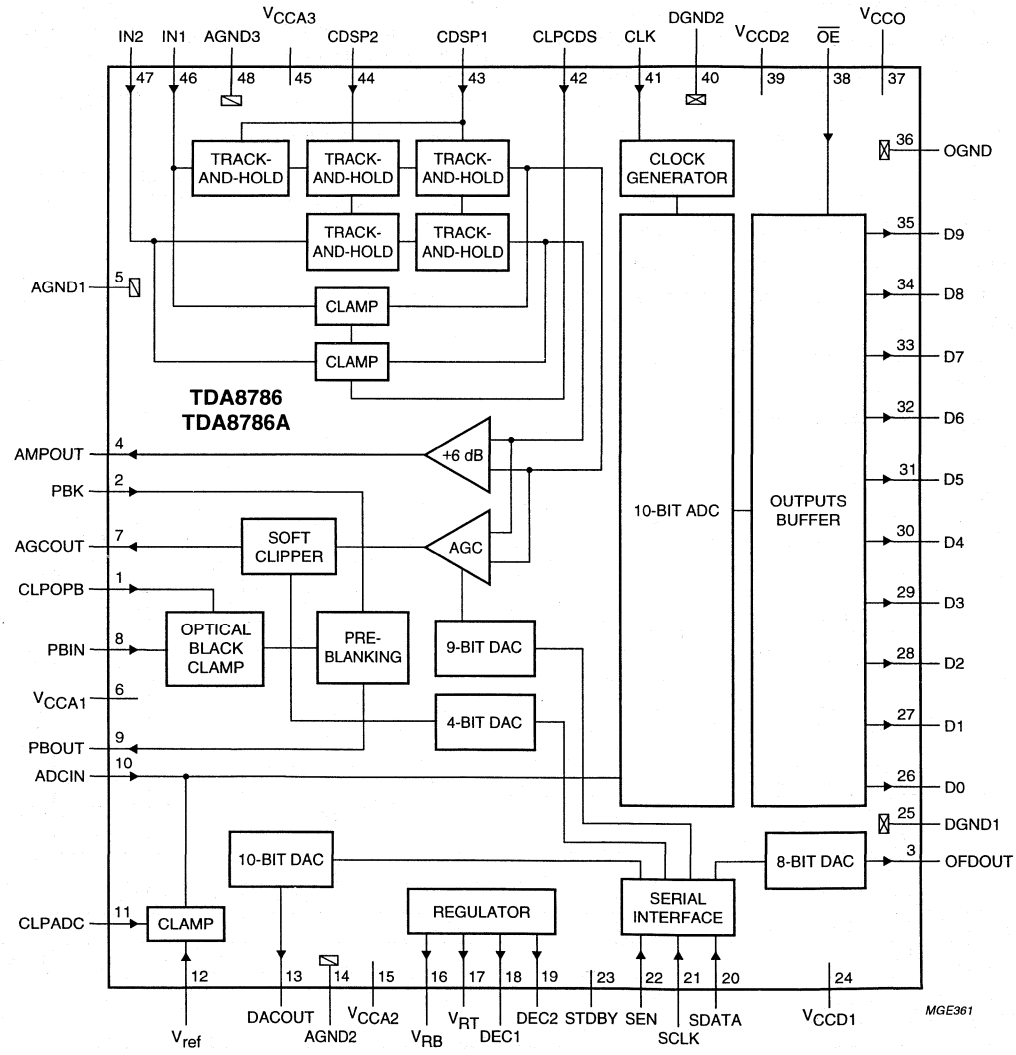


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
CLPOPB	1	optical black clamp control pulse input (active HIGH for TDA8786, active LOW for TDA8786A)
PBK	2	pre-blanking control pulse input; if PBK is HIGH (LOW) the signal is replaced by the optical black level for TDA8786 (TDA8786A)
OFDOUT	3	analog output of the additional 8-bit control DAC (controlled via the serial interface)
AMPOUT	4	CDS amplifier output (fixed gain = +6 dB)
AGND1	5	analog ground 1
V_{CCA1}	6	analog supply voltage 1
AGCOUT	7	AGC and soft clipper amplifier signal output
PBIN	8	optical black clamp and pre-blanking block signal input (from AGCOUT via a capacitor)
PBOUT	9	optical black clamp and pre-blanking block signal output
ADCIN	10	ADC analog signal input (from PBOUT or AGCOUT via a capacitor)
CLPADC	11	clamp control input for ADC analog input signal clamp (active HIGH for TDA8786 and active LOW for TDA8786A)
V_{ref}	12	ADC input clamp reference voltage (normally connected to pin VRB or DACOUT)
DACOUT	13	DAC output for ADC clamp level
AGND2	14	analog ground 2
V_{CCA2}	15	analog supply voltage 2
V_{RB}	16	ADC reference voltage (BOTTOM) code 0
V_{RT}	17	ADC reference voltage (TOP) code 1023
DEC1	18	decoupling 1 (decoupled to ground via a capacitor)
DEC2	19	decoupling 2 (decoupled to ground via a capacitor)
SDATA	20	serial data input for the 4 control DACs (9-bit DAC for AGC gain, 4-bit DAC for soft clipper; additional 8-bit DAC for OFD output voltage; 10-bit DAC for ADC clamp level and the standby mode per block; see Table 1)
SCLK	21	serial clock input for the control DACs and their serial interface; see Table 1
SEN	22	enable input for the serial interface shift register (active when SEN = logic 0); see Table 1
STDBY	23	standby control pin (active HIGH); all the output bits are logic 0 when standby is enabled
V_{CCD1}	24	digital supply voltage 1
DGND1	25	digital ground 1
D0	26	ADC digital output 0 (LSB)
D1	27	ADC digital output 1
D2	28	ADC digital output 2
D3	29	ADC digital output 3
D4	30	ADC digital output 4
D5	31	ADC digital output 5
D6	32	ADC digital output 6
D7	33	ADC digital output 7
D8	34	ADC digital output 8
D9	35	ADC digital output 9 (MSB)
OGND	36	digital output ground

SYMBOL	PIN	DESCRIPTION
V_{CCO}	37	digital output supply voltage
$\overline{OE}$	38	output enable (LOW: digital outputs active; HIGH: digital outputs high impedance)
V_{CCD2}	39	digital supply voltage 2
DGND2	40	digital ground 2
CLK	41	ADC clock input
CLPCDS	42	CDS clamp control input (active HIGH for TDA8786; active LOW for TDA8786A)
CDSP1	43	CDS control pulse input 1 (active HIGH for TDA8786; active LOW for TDA8786A)
CDSP2	44	CDS control pulse input 2 (active HIGH for TDA8786; active LOW for TDA8786A)
V_{CCA3}	45	analog supply voltage 3
IN1	46	input signal 1 from CCD (usually black channel)
IN2	47	input signal 2 from CCD (usually video channel)
AGND3	48	analog ground 3

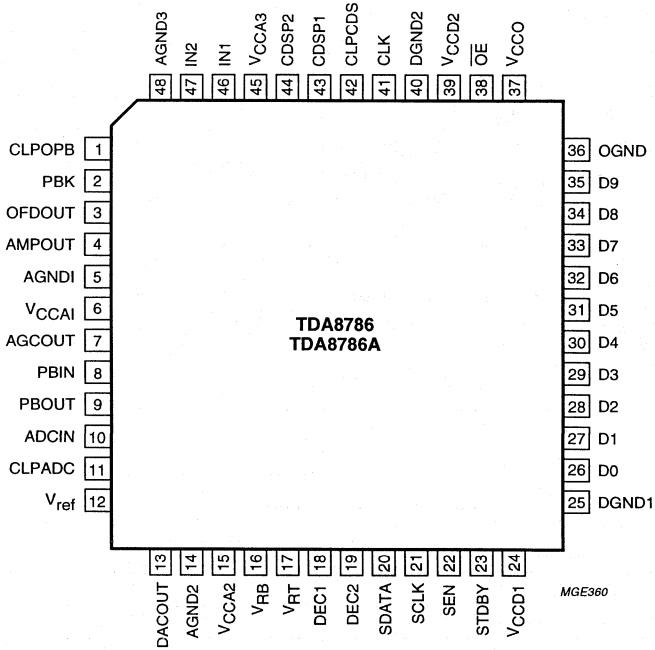


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage	note 1	−0.3	+7.0	V
V_{CCD}	digital supply voltage	note 1	−0.3	+7.0	V
V_{CCO}	output stages supply voltage	note 1	−0.3	+7.0	V
ΔV_{CC}	supply voltage difference				
	between V_{CCA} and V_{CCD}		−1.0	+1.0	V
	between V_{CCA} and V_{CCO}		−1.0	+4.0	V
	between V_{CCD} and V_{CCO}		−1.0	+4.0	V
V_i	input voltage	referenced to V_{SSA}	−0.3	+7.0	V
$V_{clk(p-p)}$	AC input voltage for switching (peak-to peak-value)	referenced to V_{SSD}	−	V_{CCD}	V
I_o	output current		−	10	mA
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		−20	+75	°C
T_j	junction temperature		−	150	°C

Note

1. The supply voltages V_{CCA}, V_{CCD} and V_{CCO} may have any value between −0.3 and +7.0 V provided that the supply voltage difference ΔV_{CC} remains as indicated.

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air	76 (typ.)	K/W

CHARACTERISTICS

$V_{CCA} = V_{CCD} = 4.75$ V; $V_{CCO} = 2.6$ V; $f_{CLK} = 18$ Msps; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CCA}	analog supply voltage		4.5	4.75	5.5	V
V_{CCD}	digital supply voltage		4.5	4.75	5.5	V
V_{CCO}	supply voltage output		2.5	2.6	5.5	V
I_{CCA}	analog supply current		–	67	–	mA
I_{CCD}	digital supply current		–	15	–	mA
I_{CCO}	supply current output	$C_L = 20$ pF on all data outputs; ramp input	–	1	–	mA
Digital inputs						
CLOCK INPUT: CLK (REFERENCED TO DGND)						
V_{IL}	LOW level input voltage		0	–	0.6	V
V_{IH}	HIGH level input voltage		2.2	–	V_{CCD}	V
I_{IL}	LOW level input current	$V_{CLK} = 0.6$ V	–1	–	+1	µA
I_{IH}	HIGH level input current	$V_{CLK} = 2.2$ V	–	–	20	µA
Z_I	input impedance	$f_{CLK} = 18$ MHz	–	2	–	kΩ
C_I	input capacitance	$f_{CLK} = 18$ MHz	–	2	–	pF
INPUTS: CDSP1 AND CDSP2						
V_{IL}	LOW level input voltage		0	–	0.6	V
V_{IH}	HIGH level input voltage		2.2	–	V_{CCD}	V
I_{IL}	LOW level input current	$V_{IL} = 0.6$ V	–	–100	–	µA
I_{IH}	HIGH level input current	$V_{IH} = 2.2$ V	–	0	–	µA
INPUTS: SEN, STDBY, CLPCDS, CLPOPB, PBK AND CLPADC						
V_{IL}	LOW level input voltage		0	–	0.6	V
V_{IH}	HIGH level input voltage		2.2	–	V_{CCD}	V
I_i	input current		–2	–	+2	µA
Correlated double sampling; CDS						
$V_{iCDS(p-p)}$	CDS input amplitude (peak-to-peak value)		–	400	1200	mV
$I_{IN1,IN2}$	input current pins 46 and 47		–2	–	+2	µA
$t_{CDS(min)}$	CDS control pulses minimum active time (HIGH for TDA8786, LOW for TDA8786A)	$f_{iCDS1,2} = f_{CLK(pix)}$	12	–	–	ns
φ	CDSP1 phase with respect to CDSP2 phase		–	180	–	deg

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Amplifier outputs						
G_{AMPOUT}	output amplifier gain		–	6	–	dB
Z_{AMPOUT}	output amplifier impedance		–	300	–	Ω
V_{AGCOUT}	AGC output amplifier dynamic voltage level		–	1800	–	mV
Z_{AGCOUT}	AGC output amplifier output impedance		–	–	100	Ω
Z_{OPB}	optical black clamp and blanking block output impedance		–	–	100	Ω
I_{PBIN}	input current pin 8		–2	–	+2	μA
G_{AGCmin}	minimum gain of AGC circuit	AGC DAC input code = 00 (9-bit control)	–	3.5	–	dB
G_{AGCmax}	maximum gain of AGC circuit	AGC DAC input code = ≥319 (9-bit control)	–	33.5	–	dB
$V_{inflex(p-p)}$	voltage at soft clipper inflexion point (peak-to-peak value)	soft clipper 4-bit control DAC input code = 00	–	0.9	–	V
		soft clipper 4-bit control DAC input code = 15	–	2.5	–	V
CR_{sc}	soft clipper compression ratio	$V_{i(sc)} < V_{inflex}$	–	1.0	–	
		$V_{i(sc)} > V_{inflex}$	–	0.66	–	
Analog-to-digital converter; ADC						
$f_{CLK(max)}$	maximum clock frequency		18	–	–	MHz
t_{CPH}	clock pulse width HIGH		15	–	–	ns
t_{CPL}	clock pulse width LOW		15	–	–	ns
SR_{CLK}	clock input slew rate (rising and falling edge)	10% to 90%	0.5	–	–	V/ns
$V_{iADC(p-p)}$	ADC input voltage level (peak-to-peak value)		–	1.8	–	V
V_{RB}	ADC reference voltage output code 0		–	1.4	–	V
V_{RT}	ADC reference voltage output code 1023		–	3.2	–	V
I_{ADCIN}	input current pin 10		–2	–	+2	μA
ILE	integral linearity error	f_{CLK} = 18 Msps; ramp input	–	±1.3	±2.0	LSB
DLE	differential linearity error	f_{CLK} = 18 Msps; ramp input	–	±0.5	±0.9	LSB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital-to-analog converters						
OFD DAC						
$V_{OFD(p-p)}$	additional 8-bit control DAC (OFD) output voltage (peak-to-peak value)		–	1.0	–	V
$V_{OFD(0)}$	DC output voltage for code 0		–	2.4	–	V
$V_{OFD(255)}$	DC output voltage for code 255		–	3.4	–	V
Z_{OFD}	additional 8-bit control DAC (OFD) output impedance		–	2000	–	Ω
ADC CLAMP CONTROL DAC (see Fig.5)						
$V_{DACOUT(p-p)}$	ADC clamp 10-bit control DAC output voltage (peak-to-peak value)		–	0.9	–	V
V_{DACOUT}	DC output voltage	code 0	–	1.4	–	V
		code 1023	–	2.3	–	V
Z_{DACOUT}	ADC clamp control DAC output impedance		–	–	250	Ω
Digital outputs (f_{clk} = 18 MHz; C_L = 20 pF)						
V_{OH}	HIGH level output voltage	I_o = –1 mA	V_{DDO} – 0.5	–	V_{DDO}	V
V_{OL}	LOW level output voltage	I_o = 1 mA	0	–	0.5	V
I_{OZ}	output current in 3-state mode	0.5 V < V_o < V_{DDO}	–20		+20	μA
t_h	output hold time		5	–	–	ns
t_d	output delay	V_{DDO} = 4.75 V	–	12	15	ns
		V_{DDO} = 3.15 V	–	17	20	ns
		V_{DDO} = 2.7 V	–	21	24	ns
Serial interface						
f_{SCLK}	maximum frequency of serial interface		5	–	–	MHz

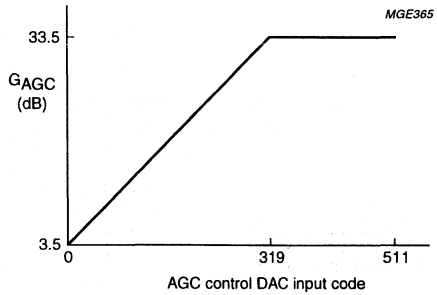
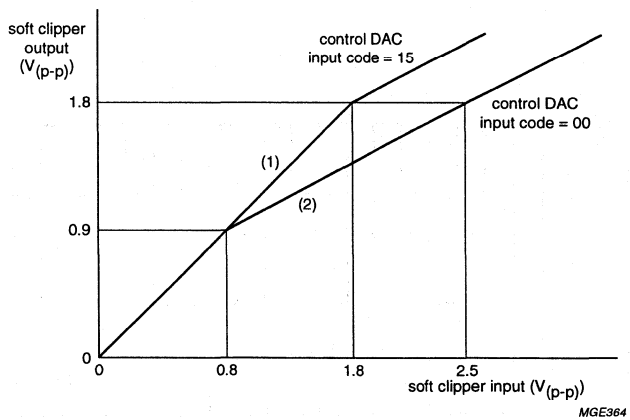


Fig.3 AGC gain as a function of DAC input code.



(1) $\frac{V_o}{V_i} = 1$

(2) $\frac{V_o}{V_i} = 0.66$

Fig.4 Soft clipper output voltage as a function of soft clipper input voltage.

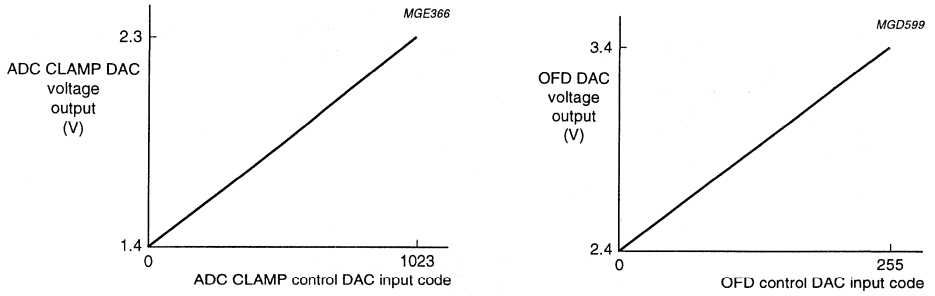


Fig.5 DAC voltage output as a function of DAC input code.

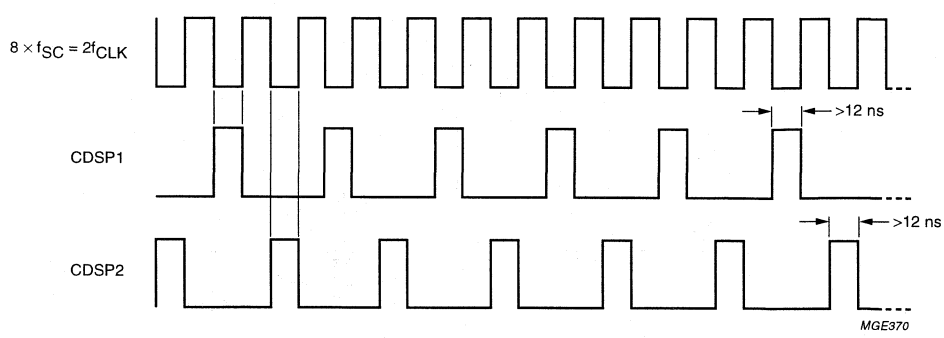


Fig.6 CCD high-band control signal timing (TDA8786).

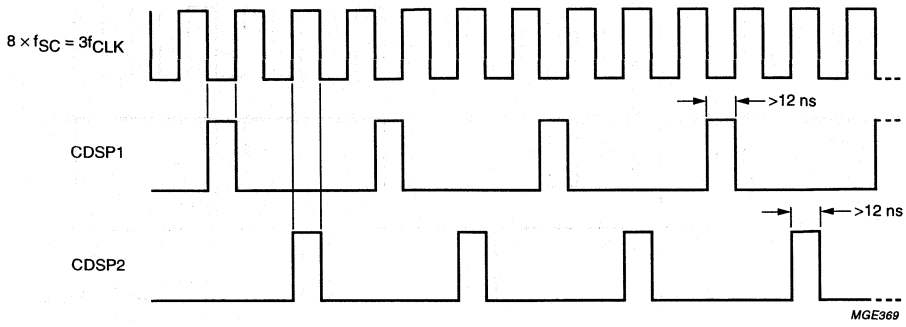


Fig.7 CCD normal-band control signal timing (TDA8786).

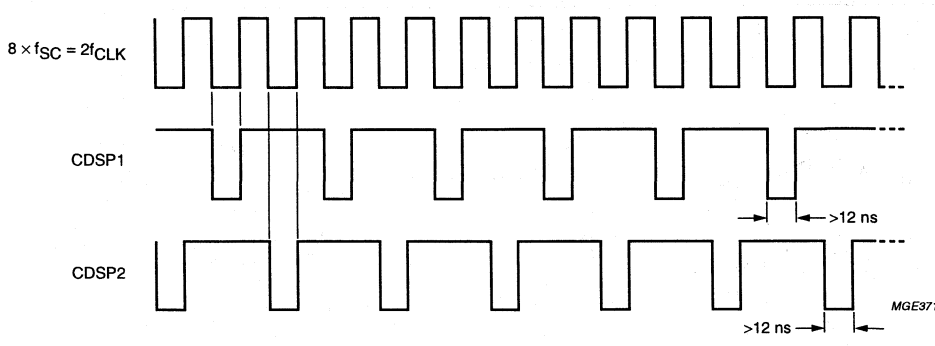


Fig.8 CCD high-band control signal timing (TDA8786A).

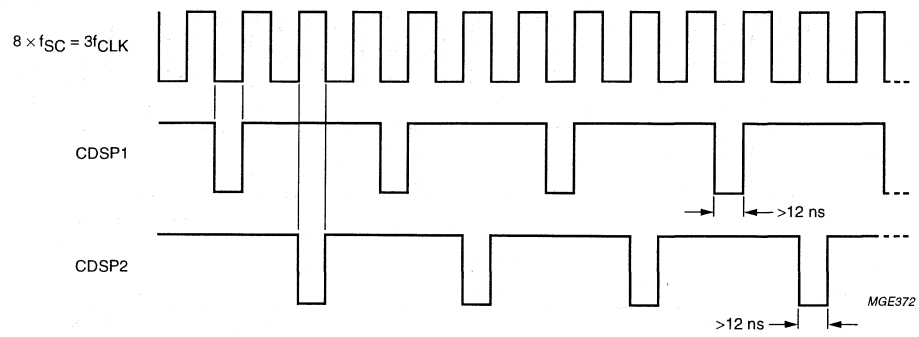


Fig.9 CCD normal-band control signal timing (TDA8786A).

ADC clamping

When CLPADC is HIGH (TDA8786); (LOW for TDA8786A) the ADC input is clamped to voltage level V_{ref}. V_{ref} should normally be connected to V_{RB} (ADC output code 0 pin) or to DACOUT (10-bit DAC output). The DAC is controlled via the serial interface, its output covers the lower half of the ADC input range.

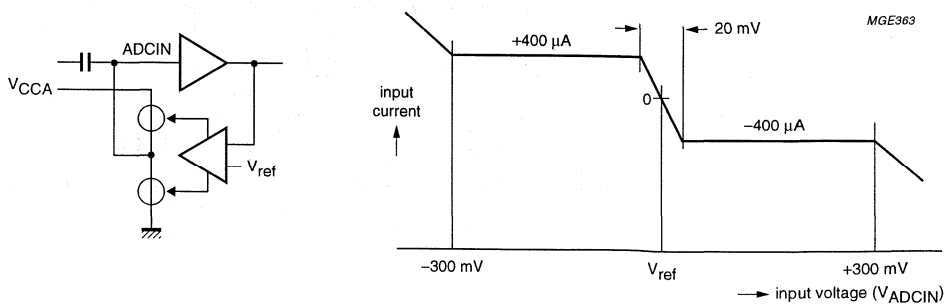


Fig.10 Clamping circuit and current waveform.

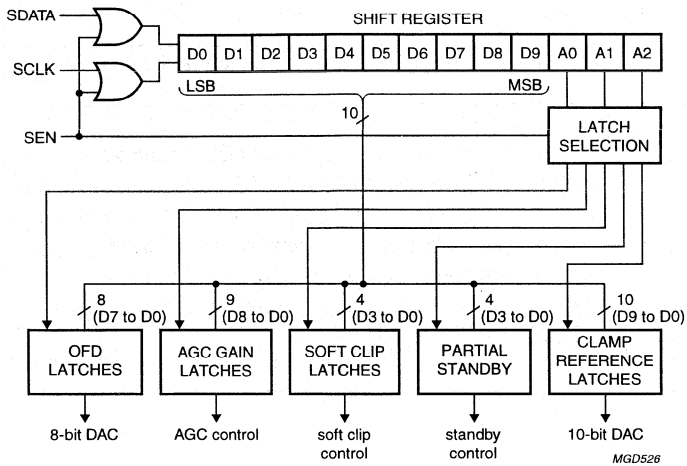
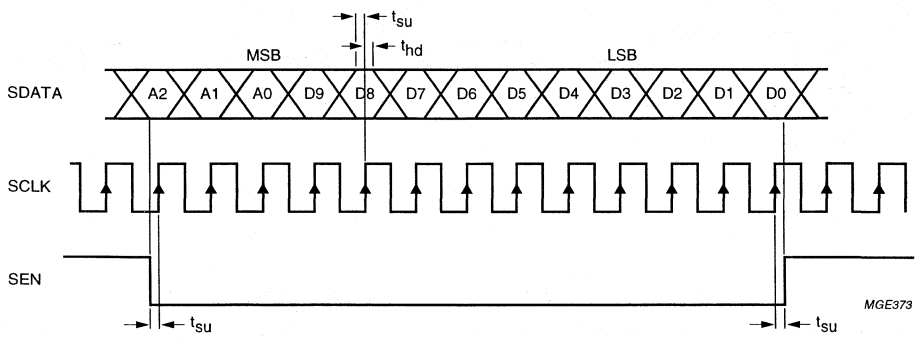


Fig.11 Serial interface block diagram.



t_{su} = 4 ns (min.); t_{hd} = 4 ns (min.).

Fig.12 Loading sequence of control DACs input data via the serial interface.

Table 1 Serial interface programming

ADDRESS BITS			DATA BITS D9 to D0
A2	A1	A0	
0	0	0	OFD output control (D7 to D0).
0	0	1	Soft clipper control. Only the 4 LSBs (D3 to D0) are used. Bits D9 to D4 should be set to logic 0.
0	1	0	AGC gain control (D8 to D0).
0	1	1	Partial standby controls for power consumption optimization. Only the 4 LSBs (D3 to D0) are used. Bits D9 to D4 should be set to logic 0: D0 = 1: CDS + AGC + soft clipper block in standby; $I_{CCA} + I_{CCD}$ = 38 mA D1 = 1: optical black clamp + blanking block in standby; $I_{CCA} + I_{CCD}$ = 75 mA D2 = 1: OFD DAC in standby; $I_{CCA} + I_{CCD}$ = 80.5 mA D3 = 1: 6 dB amplifier (output on AMPOUT pin) in standby; $I_{CCA} + I_{CCD}$ = 81 mA.
1	0	0	Clamp reference DAC (D9 to D0).

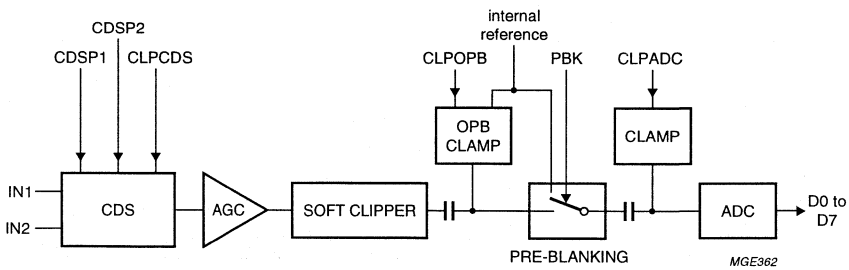
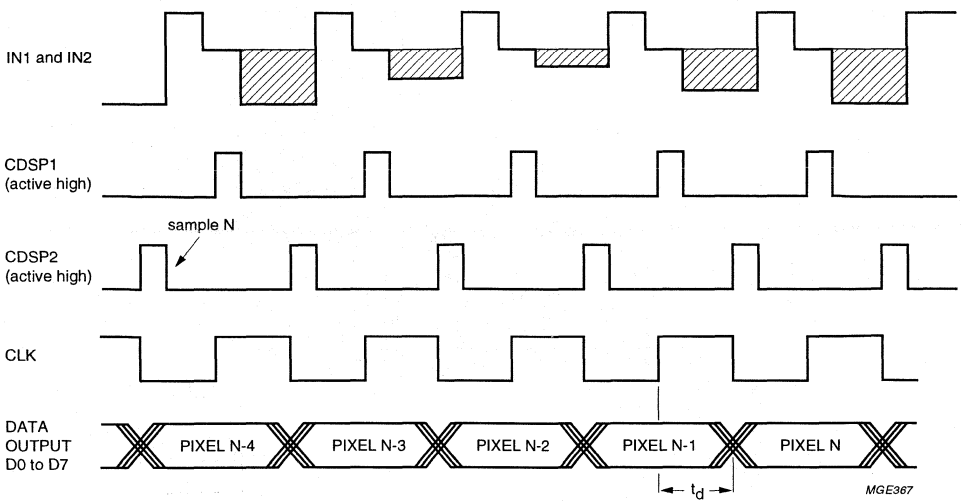


Fig.13 CDS, CLAMP and pre-blanking signal path for Figs 14. and 15



The hatched areas represent active video.

Fig.14 Pixel frequency timing diagram.

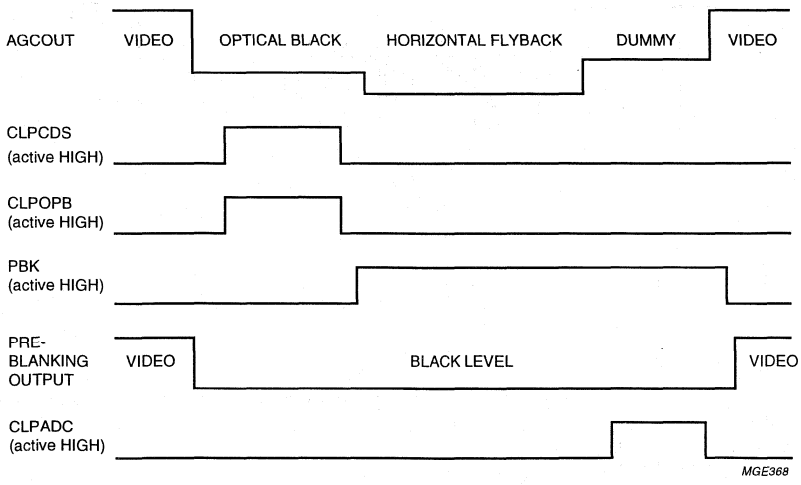
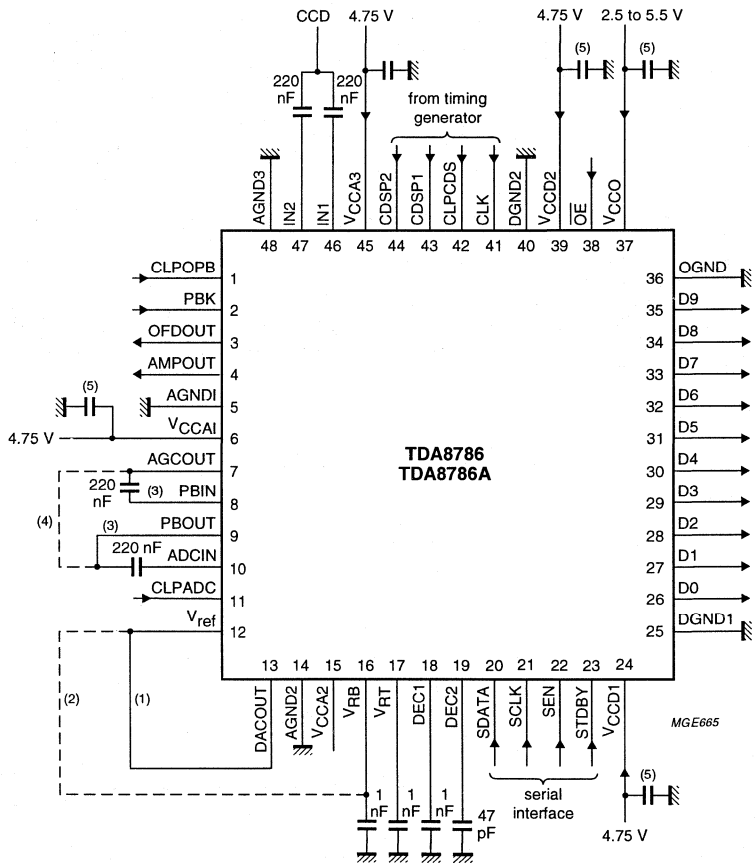


Fig.15 Line frequency timing diagram.

APPLICATION INFORMATION



Depending on application [(1) or (2) and (3) or (4)] the following connections must be made;

(1) The clamp level of the signal input at ADCIN can be tuned from code 00 to code 511 in 0.5LSB step of ADC via the serial interface.

(2) The clamp level of the signal input at ADCIN is at code 00 of the ADC.

(3) The optical black clamp and preblanking blocks are used.

(4) The optical black clamp and preblanking blocks are not used.

(5) All supply pins must be decoupled with 100 nF capacitors as close as possible to the device.

Fig.16 Application diagram.

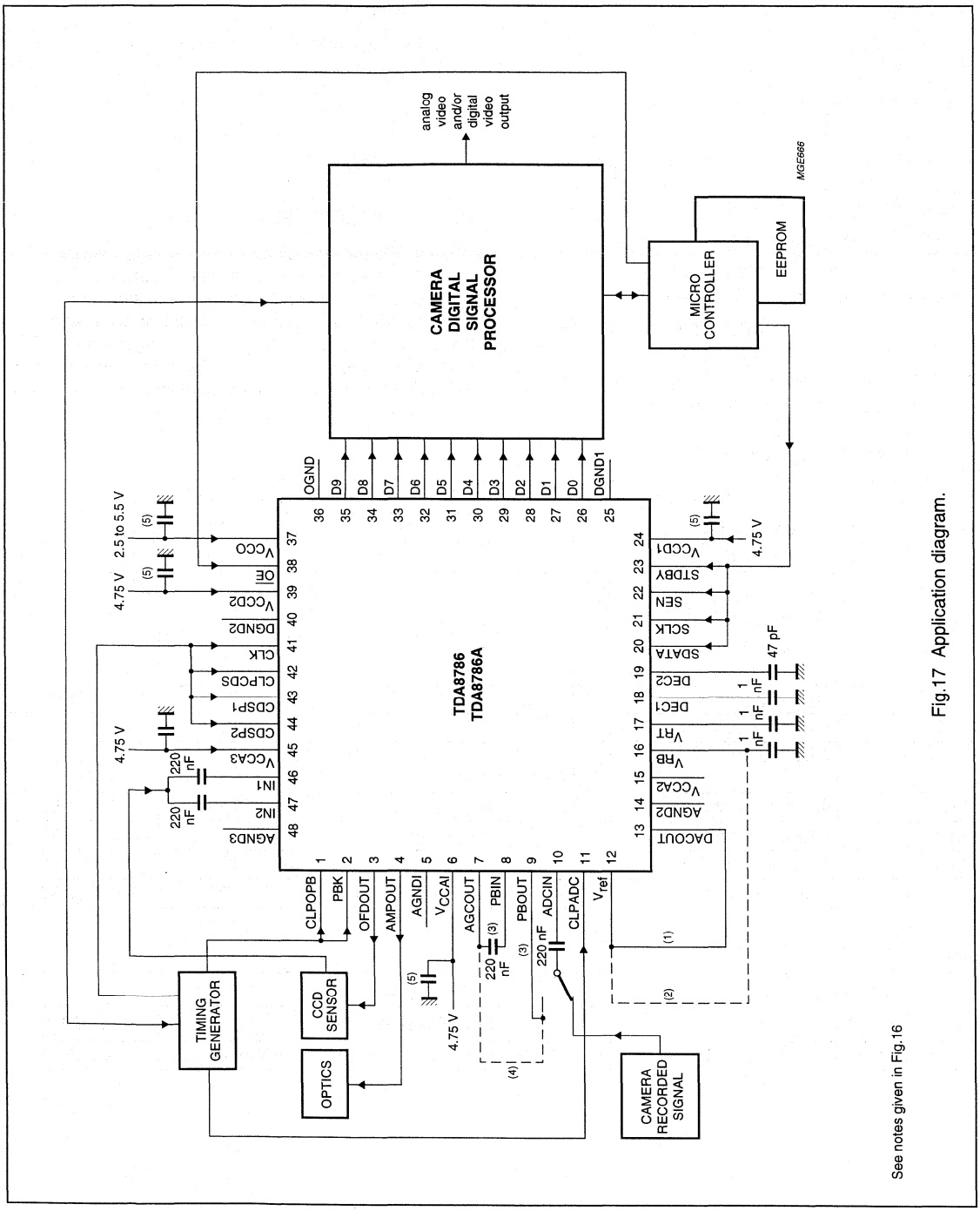


Fig.17 Application diagram.

8-bit, 40 Msps 2.7 to 5.5 V universal analog-to-digital converter

TDA8790

FEATURES

- 8-bit resolution
- Operation between 2.7 and 5.5 V
- Sampling rate up to 40 MHz
- DC sampling allowed
- High signal-to-noise ratio over a large analog input frequency range (7.3 effective bits at 4.43 MHz full-scale input at f_{clk} = 40 MHz)
- CMOS/TTL compatible digital inputs and outputs
- External reference voltage regulator
- Power dissipation only 30 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- Sleep mode (4 mW)
- No sample-and-hold circuit required.

APPLICATIONS

High-speed analog-to-digital conversion for:

- Video data digitizing
- Camera
- Camcorder
- Radio communication.

GENERAL DESCRIPTION

The TDA8790 is an 8-bit universal analog-to-digital converter (ADC) for video and general purpose applications. It converts the analog input signal from 2.7 to 5.5 V into 8-bit binary-coded digital words at a maximum sampling rate of 40 MHz. All digital inputs and outputs are CMOS/TTL compatible. A sleep mode allows reduction of the device power consumption down to 4 mW.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage		2.7	3.3	5.5	V
V_{DDD}	digital supply voltage		2.7	3.3	5.5	V
V_{DDO}	output stages supply voltage		2.5	3.3	5.5	V
ΔV_{DD}	supply voltage difference					
	$V_{DDA} - V_{DDD}$		−0.2	–	+0.2	V
	$V_{DDD} - V_{DDO}$		−0.2	–	+2.25	V
I_{DDA}	analog supply current		–	4	6	mA
I_{DDD}	digital supply current		–	5	8	mA
I_{DDO}	output stages supply current	f_{clk} = 40 MHz; C_L = 20 pF; ramp input	–	1	2	mA
INL	integral non-linearity	f_{clk} = 40 MHz; ramp input	–	±0.5	±0.75	LSB
DNL	differential non-linearity	f_{clk} = 40 MHz; ramp input	–	±0.25	±0.5	LSB
$f_{clk(max)}$	maximum clock frequency		40	–	–	MHz
P_{tot}	total power dissipation	$V_{DDA} = V_{DDD} = V_{DDO}$ = 3.3 V	–	30	53	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8790M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

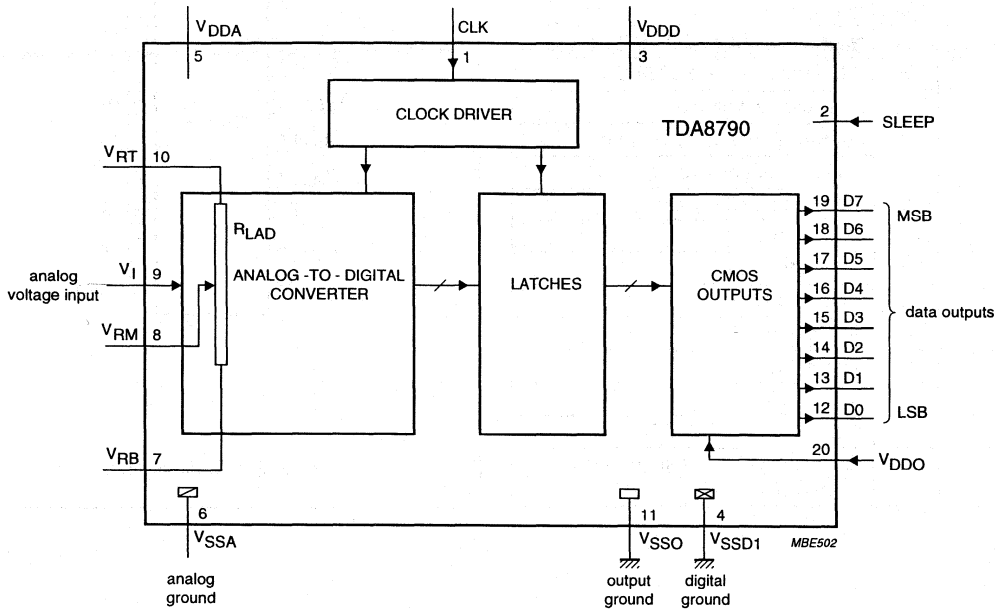


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
CLK	1	clock input
SLEEP	2	sleep mode input
V_{DDD}	3	digital supply voltage (2.7 to 5.5 V)
V_{SSD}	4	digital ground
V_{DDA}	5	analog supply voltage (2.7 to 5.5 V)
V_{SSA}	6	analog ground
V_{RB}	7	reference voltage BOTTOM input
V_{RM}	8	reference voltage MIDDLE
V_I	9	analog input voltage
V_{RT}	10	reference voltage TOP input
V_{SSO}	11	digital output ground
D0	12	data output; bit 0 (LSB)
D1	13	data output; bit 1
D2	14	data output; bit 2
D3	15	data output; bit 3
D4	16	data output; bit 4
D5	17	data output; bit 5
D6	18	data output; bit 6
D7	19	data output; bit 7 (MSB)
V_{DDO}	20	positive supply voltage for output stage (2.7 to 5.5 V)

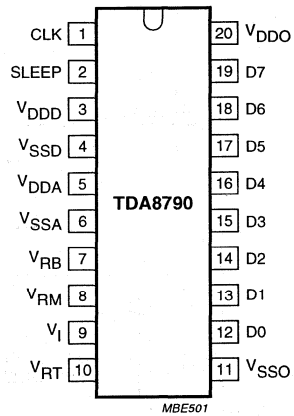


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage	note 1	−0.3	+7.0	V
V_{DDD}	digital supply voltage	note 1	−0.3	+7.0	V
V_{DDO}	output stages supply voltage	note 1	−0.3	+7.0	V
ΔV_{DD}	supply voltage difference				
	$V_{DDA} - V_{DDD}$		−1.0	+4.0	V
	$V_{DDA} - V_{DDO}$		−1.0	+4.0	V
	$V_{DDD} - V_{DDO}$		−1.0	+4.0	V
V_I	input voltage	referenced to V_{SSA}	−0.3	+7.0	V
$V_{clk(p-p)}$	AC input voltage for switching (peak-to-peak value)	referenced to V_{SSD}	−	V_{DDD}	V
I_O	output current		−	10	mA
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		−20	+75	°C
T_j	junction temperature		−	+150	°C

Note

1. The supply voltages V_{DDA}, V_{DDD} and V_{DDO} may have any value between −0.3 V and +7.0 V provided that the supply voltage ΔV_{DD} remains as indicated.

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air	120	K/W

CHARACTERISTICS

V_{DDA} = V_5 to V_6 = 3.3 V; V_{DDD} = V_3 to V_4 = 3.3 V; V_{DDO} = V_{20} to V_{11} = 3.3 V; V_{SSA}, V_{SSD} and V_{SSO} shorted together; $V_{i(p-p)}$ = 1.84 V; C_L = 20 pF; T_{amb} = 0 to +70 °C; typical values measured at T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDA}	analog supply voltage		2.7	3.3	5.5	V
V_{DDD}	digital supply voltage		2.7	3.3	5.5	V
V_{DDO}	output stages supply voltage		2.5	3.3	5.5	V
ΔV_{DD}	supply voltage difference					
	$V_{DDA} - V_{DDD}$		−0.2	−	+0.2	V
	$V_{DDD} - V_{DDO}$		−0.2	−	+2.25	V
I_{DDA}	analog supply current		−	4	6	mA
I_{DDD}	digital supply current		−	5	8	mA
I_{DDO}	output stages supply current	f_{clk} = 40 MHz; ramp input; C_L = 20 pF	−	1	2	mA
Inputs						
CLOCK INPUT CLK (REFERENCED TO V_{SSD}); see note 1						
V_{IL}	LOW level input voltage		0	−	$0.3V_{DDD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DDD}$	−	V_{DDD}	V
		$V_{DDD} \leq 3.6$ V	$0.6V_{DDD}$	−	V_{DDD}	V
I_{IL}	LOW level input current	V_{clk} = $0.3V_{DDD}$	−1	0	+1	µA
I_{IH}	HIGH level input current	V_{clk} = $0.7V_{DDD}$	−	−	5	µA
Z_I	input impedance	f_{clk} = 40 MHz	−	4	−	kΩ
C_I	input capacitance	f_{clk} = 40 MHz	−	3	−	pF
INPUT SLEEP (REFERENCED TO V_{SSD}); see Table 2						
V_{IL}	LOW level input voltage		0	−	$0.3V_{DDD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DDD}$	−	V_{DDD}	V
		$V_{DDD} \leq 3.6$ V	$0.6V_{DDD}$	−	V_{DDD}	V
I_{IL}	LOW level input current	V_{IL} = $0.3V_{DDD}$	−1	−	−	µA
I_{IH}	HIGH level input current	V_{IH} = $0.7V_{DDD}$	−	−	+1	µA
V_I (ANALOG INPUT VOLTAGE REFERENCED TO V_{SSA})						
I_{IL}	LOW level input current	$V_I = V_{RB}$	−	0	−	µA
I_{IH}	HIGH level input current	$V_I = V_{RT}$	−	9	−	µA
Z_I	input impedance	f_i = 1 MHz	−	20	−	kΩ
C_I	input capacitance	f_i = 1 MHz	−	2	−	pF
Reference voltages for the resistor ladder; see Table 1						
V_{RB}	reference voltage BOTTOM		1.1	1.2	−	V
V_{RT}	reference voltage TOP	$V_{TOP} \leq V_{DDA}$	2.7	3.3	V_{DDA}	V
V_{diff}	differential reference voltage $V_{RT} - V_{RB}$		1.5	2.1	2.7	V
I_{ref}	reference current		−	0.95	−	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
R_{LAD}	resistor ladder		–	2.2	–	kΩ
TC_{RLAD}	temperature coefficient of the resistor ladder		–	1860	–	ppm
			–	4092	–	mΩ/K
V_{osB}	offset voltage BOTTOM	note 2	–	170	–	mV
V_{osT}	offset voltage TOP	note 2	–	170	–	mV
$V_{i(p-p)}$	analog input voltage (peak-to-peak value)	note 3	1.4	1.76	2.4	V
Outputs						
DIGITAL OUTPUTS D7 TO D0 (REFERENCED TO V_{SSD})						
V_{OL}	LOW level output voltage	I_O = 1 mA	0	–	0.5	V
V_{OH}	HIGH level output voltage	I_O = −1 mA	V_{DDO} − 0.5	–	V_{DDO}	V
I_{OZ}	output current in 3-state mode	0.4 V < V_O < V_{DDO}	−20	–	+20	µA
Switching characteristics						
CLOCK INPUT CLK; see Fig.4; note 1						
$f_{clk(max)}$	maximum clock frequency		40	–	–	MHz
t_{CPH}	clock pulse width HIGH		9	–	–	ns
t_{CPL}	clock pulse width LOW		9	–	–	ns
Analog signal processing						
LINEARITY						
INL	integral non-linearity	f_{clk} = 40 MHz; ramp input; see Fig.6	–	±0.5	±0.75	LSB
DNL	differential non-linearity	f_{clk} = 40 MHz; ramp input; see Fig.7	–	±0.25	±0.5	LSB
BANDWIDTH (f_{clk} = 40 MHz)						
B	analog bandwidth	full-scale sine wave; note 4	–	10	–	MHz
		75% full-scale sine wave; note 4	–	13	–	MHz
		50% full-scale sine wave; note 4	–	20	–	MHz
		small signal at mid scale; V_i = ±10 LSB at code 128; note 4	–	350	–	MHz
INPUT SET RESPONSE (f_{clk} = 40 MHz; see Fig.8; note 5)						
t_{STLH}	analog input settling time LOW-to-HIGH	full-scale square wave	–	3	5	ns
t_{STHL}	analog input settling time HIGH-to-LOW	full-scale square wave	–	3	5	ns
HARMONICS; (f_{clk} = 40 MHz; see Fig.9; note 6)						
THD	total harmonic distortion	f_i = 4.43 MHz	–	−50	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SIGNAL-TO-NOISE RATIO; see Fig.9; note 6						
S/N	signal-to-noise ratio (full scale)	without harmonics; f_{clk} = 40 MHz; f_i = 4.43 MHz	–	47	–	dB
EFFECTIVE BITS; see Fig.9; note 6						
EB	effective bits	f_{clk} = 40 MHz				
		f_i = 300 kHz	–	7.8	–	bits
		f_i = 4.43 MHz	–	7.3	–	bits
DIFFERENTIAL GAIN; see note 7						
G_{diff}	differential gain	f_{clk} = 40 MHz; PAL modulated ramp	–	1.5	–	%
DIFFERENTIAL PHASE; see note 7						
φ_{diff}	differential phase	f_{clk} = 40 MHz; PAL modulated ramp	–	0.25	–	deg
Timing (f_{clk} = 40 MHz; C_L = 20 pF); see Fig.4; note 8						
t_{ds}	sampling delay time		–	–	5	ns
t_h	output hold time		5	–	–	ns
t_d	output delay time	V_{DDO} = 4.75 V	8	12	15	ns
		V_{DDO} = 3.15 V	8	17	20	ns
		V_{DDO} = 2.7 V	8	18	21	ns
3-state sleep mode delay times; see Fig.5						
t_{dZH}	enable HIGH		–	14	18	ns
t_{dZL}	enable LOW		–	16	20	ns
t_{dHZ}	disable HIGH		–	16	20	ns
t_{dLZ}	disable LOW		–	14	18	ns

Notes

1. In addition to a good layout of the digital and analog ground, it is recommended that the rise and fall times of the clock must not be less than 1 ns.
2. Analog input voltages producing code 0 up to and including 256:
   a) V_{osB} (voltage offset BOTTOM) is the difference between the analog input which produces data equal to 00 and the reference voltage BOTTOM (V_{RB}) at T_{amb} = 25 °C.
   b) V_{osT} (voltage offset TOP) is the difference between V_{RT} (reference voltage TOP) and the analog input which produces data outputs equal to 256 at T_{amb} = 25 °C.

3. In order to ensure the optimum linearity performance of such converter architecture the lower and upper extremities of the converter reference resistor ladder (corresponding to output codes 0 and 255 respectively) are connected to pins V_{RB} and V_{RT} via offset resistors R_{OB} and R_{OT} as shown in Fig.3.

   a) The current flowing into the resistor ladder is $I_L = \frac{V_{RT} - V_{RB}}{R_{OB} + R_L + R_{OT}}$ and the full-scale input range at the converter, to cover code 0 to code 255, is $V_i = R_L \times I_L = \frac{R_L}{R_{OB} + R_L + R_{OT}} \times (V_{RT} - V_{RB}) = 0.838 \times (V_{RT} - V_{RB})$

   b) Since R_L, R_{OB} and R_{OT} have similar behaviour with respect to process and temperature variation, the ratio $\frac{R_L}{R_{OB} + R_L + R_{OT}}$ will be kept reasonably constant from part to part. Consequently variation of the output codes at a given input voltage depends mainly on the difference $V_{RT} - V_{RB}$ and its variation with temperature and supply voltage. When several ADCs are connected in parallel and fed with the same reference source, the matching between each of them is then optimized.

4. The analog bandwidth is defined as the maximum input sine wave frequency which can be applied to the device. No glitches greater than 2 LSBs, nor any significant attenuation is observed in the reconstructed signal.
5. The analog input settling time is the minimum time required for the input signal to be stabilized after a sharp full-scale input (square-wave signal) in order to sample the signal and obtain correct output data.
6. Effective bits are obtained via a Fast Fourier Transform (FFT) treatment taking 8 K acquisition points per equivalent fundamental period. The calculation takes into account all harmonics and noise up to half of the clock frequency (NYQUIST frequency). Conversion to signal-to-noise ratio: S/N = EB × 6.02 + 1.76 dB.
7. Measurement carried out using video analyser VM700A, where video analog signal is reconstructed through a DAC.
8. Output data acquisition: the output data is available after the maximum delay time of t_d.

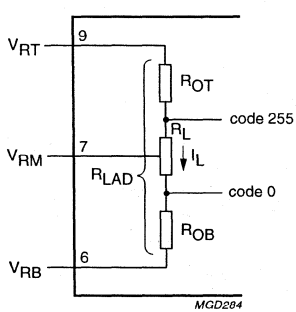


Fig.3 Explanation of note 3.

Table 1 Output coding and input voltage (typical values; referenced to V_{SSA})

STEP	$V_{I(p-p)}$ (V)	BINARY OUTPUT BITS							
		D7	D6	D5	D4	D3	D2	D1	D0
Underflow	<1.37	0	0	0	0	0	0	0	0
0	1.37	0	0	0	0	0	0	0	0
1	.	0	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
254	.	1	1	1	1	1	1	1	0
255	3.13	1	1	1	1	1	1	1	1
Overflow	>3.13	1	1	1	1	1	1	1	1

Table 2 Sleep mode selection

SLEEP	D7 TO D0	$I_{DDA} + I_{DDD}$ (typ.)
1	high impedance	1.2 mA
0	active	9 mA

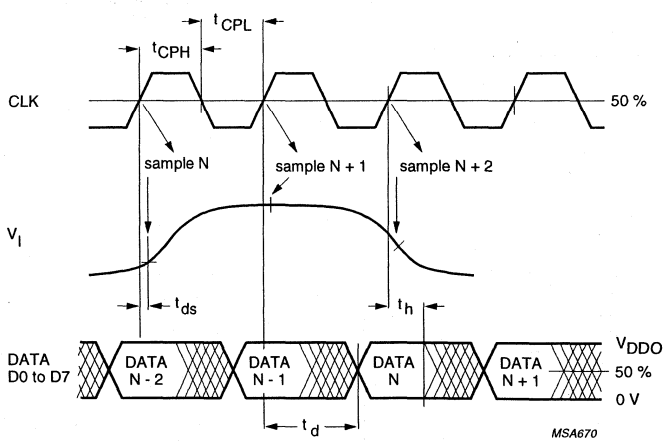
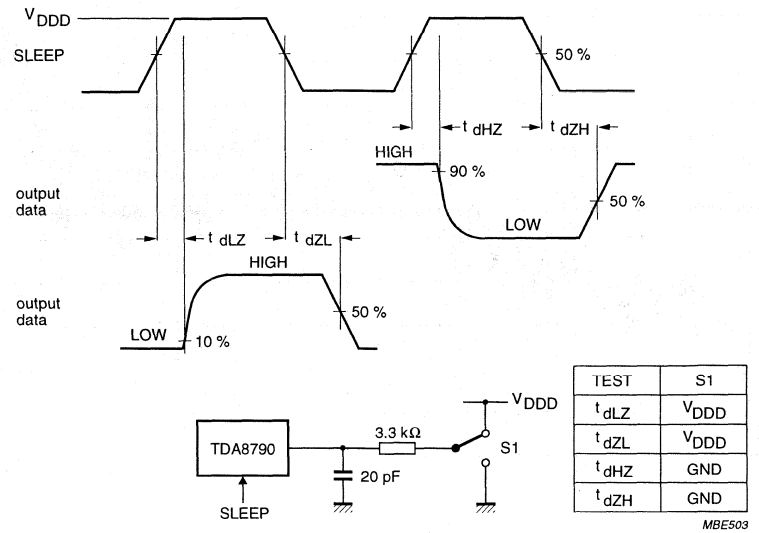


Fig.4 Timing diagram.



TEST	S1
t_{dLZ}	V_{DDD}
t_{dZL}	V_{DDD}
t_{dHZ}	GND
t_{dZH}	GND

f_{SLEEP} = 100 kHz.

Fig.5 Timing diagram and test conditions of 3-state output delay time.

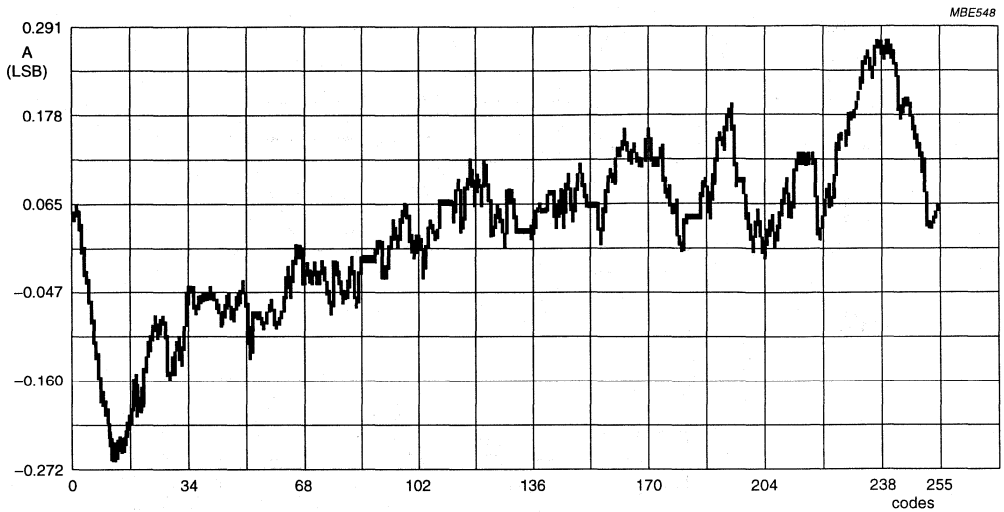


Fig.6 Typical integral non-linearity (INL) performance.

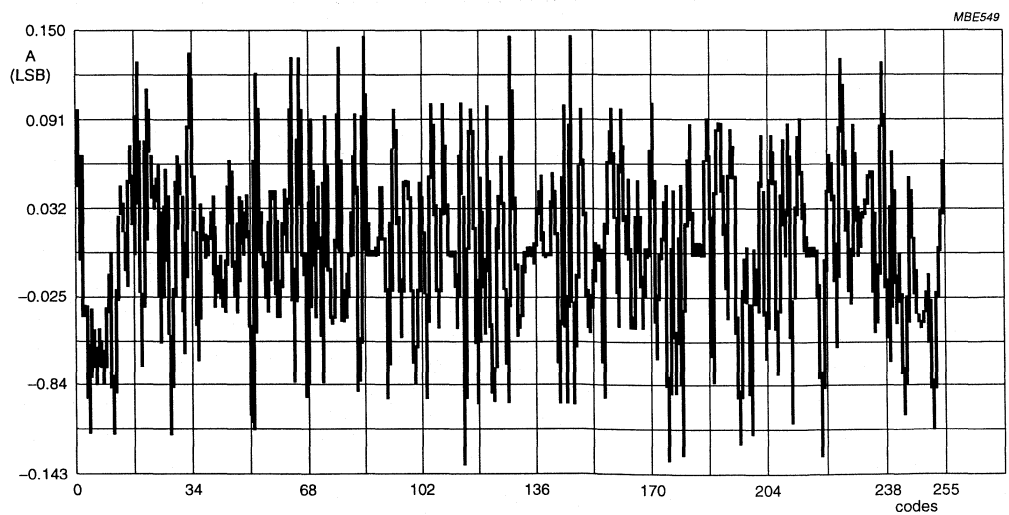


Fig.7 Typical differential non-linearity (DNL) performance.

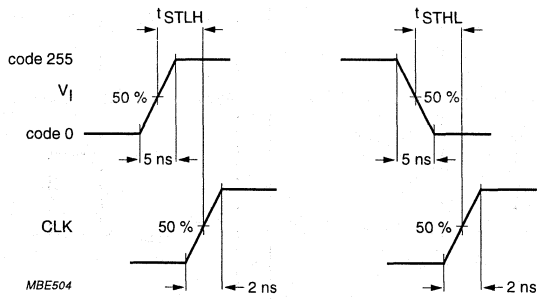
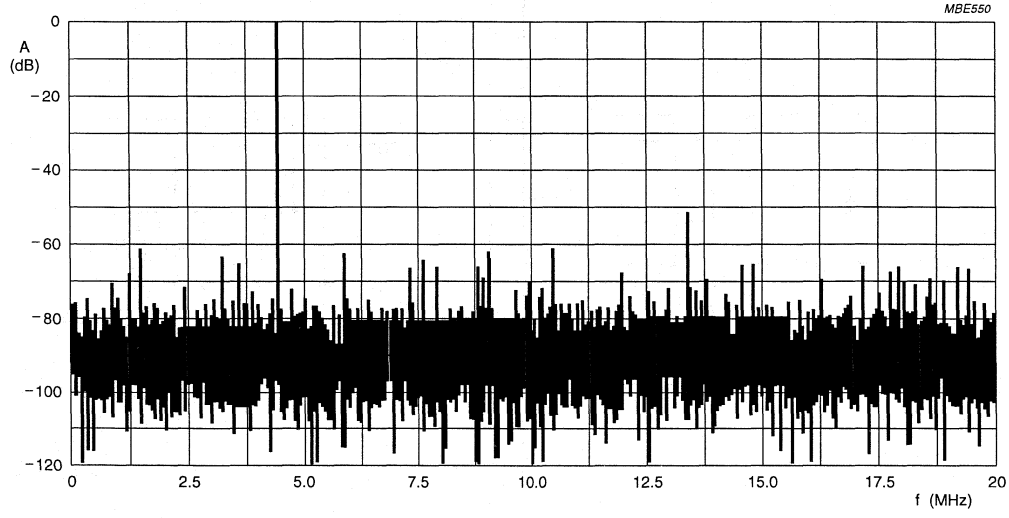


Fig.8 Analog input settling-time diagram.



Effective bits: 7.32; THD = 51.08 dB.
Harmonic levels (dB): 2nd = −68.99; 3rd = −51.62; 4th = −66.05; 5th = −63.23; 6th = −72.79.

Fig.9 Typical Fast Fourier Transform (f_{clk} = 40 MHz; f_i = 4.43 MHz).

INTERNAL PIN CONFIGURATIONS

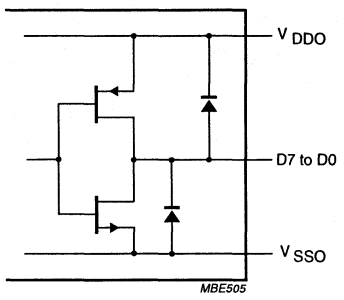


Fig.10 CMOS data outputs.

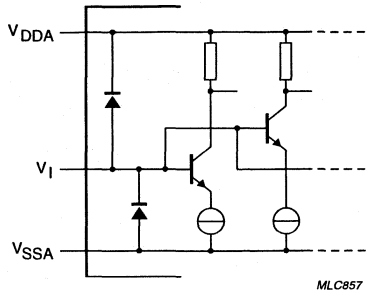


Fig.11 Analog inputs.

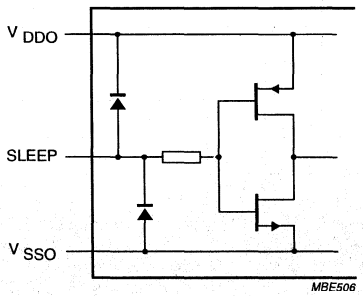


Fig.12 SLEEP 3-state input.

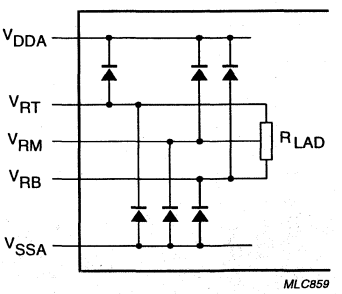


Fig.13 V_{RB}, V_{RM} and V_{RT}.

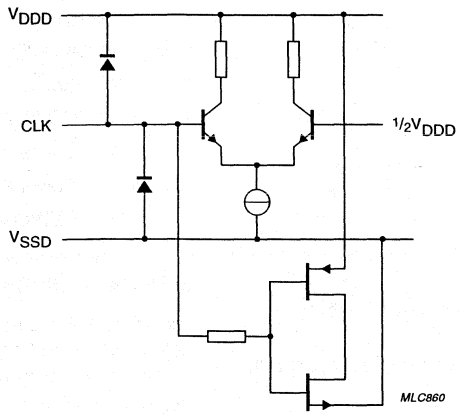
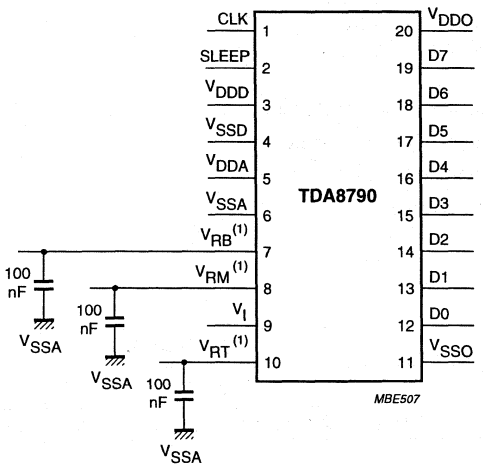


Fig.14 CLK input.

APPLICATION INFORMATION



The analog and digital supplies should be separated and decoupled.

The external voltage generator must be built such that a good supply voltage ripple rejection is achieved with respect to the LSB value. Eventually, the reference ladder voltages can be derived from a well regulated V_{DDA} supply through a resistor bridge and a decoupled capacitor.

(1) V_{RB}, V_{RM} and V_{RT} are decoupled to V_{SSA}.

Fig.15 Application diagram.

Multistandard vision and sound-IF PLL with DVB-IF processing

TDA9819

FEATURES

- 5 V supply voltage
- Applicable for IF frequencies of 38.9 MHz and 45.75 MHz
- Two switched VIF inputs, gain controlled wide band VIF-amplifier (AC-coupled)
- True synchronous demodulation with active carrier regeneration (very linear demodulation, good intermodulation figures, reduced harmonics and excellent pulse response)
- VCO frequency switchable between TV (M or BG/L) IF-picture carrier and Digital Video Broadcast (DVB) frequency
- Separate video amplifier for sound trap buffering with high video bandwidth
- VIF AGC detector for gain control, operating as peak sync detector for M and B/G and peak white detector for L; controlled reaction time for L
- Tuner AGC with adjustable takeover point (TOP)
- AFC detector without extra reference circuit
- SIF input for single reference QSS mode (PLL controlled); SIF AGC detector for gain controlled SIF amplifier; single reference QSS mixer able to operate in high performance single reference QSS mode
- AC-coupled limiter amplifier for sound intercarrier signal
- Alignment-free FM-PLL demodulator with high linearity
- AM demodulator without extra reference circuit
- Stabilizer circuit for ripple rejection and to achieve constant output signals.

DVB functions

- Gain controlled IF-amplifier
- Mixer for DVB-IF
- VCO for QAM carrier recovery
- External VCO control for DVB
- Internal and external AGC for DVB
- DVB output level adjust via AGC adjust
- High level DVB operational output amplifier.

GENERAL DESCRIPTION

The TDA9819 is an integrated circuit for multistandard vision and sound-IF signal processing with single reference PLL demodulator combined with the signal stages for DVB-IF processing.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9819	SDIP32	plastic shrink dual in-line package; 32 leads (400 mil)	SOT232-1

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC02 OR DATA SHEET

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		4.5	5.0	5.5	V
I_P	supply current		81	100	121	mA
$V_{i\ VIF(rms)}$	vision IF input signal voltage sensitivity (RMS value)	−1 dB video at output	–	60	100	μV
$V_{o\ CVBS(p-p)}$	CVBS output signal voltage (peak-to-peak value)		1.7	2.0	2.3	V
B (M, BG/L)	−3 dB video bandwidth on pin 10	M, B/G and L standard; $C_L < 20$ pF; $R_L > 1$ kΩ; AC load	7	8	–	MHz
S/N (W)	weighted signal-to-noise ratio for video		56	60	–	dB
$\alpha_{1.1}$	intermodulation attenuation at 'blue'	f = 1.1 MHz	58	64	–	dB
$\alpha_{3.3}$	intermodulation attenuation at 'blue'	f = 3.3 MHz	58	64	–	dB
α_H	suppression of harmonics in video signal		35	40	–	dB
$V_{i\ SIF(rms)}$	sound-IF input signal voltage sensitivity (RMS value)	−3 dB at intercarrier output	–	70	100	μV
$V_{o(rms)}$	audio output signal voltage for FM (RMS value)	M and B/G standard; 25 kHz frequency deviation	–	0.5	–	V
	audio output signal voltage for AM (RMS value)	L standard; 54% modulation	–	0.5	–	V
THD	total harmonic distortion					
	FM	25 kHz frequency deviation	–	0.15	0.5	%
	AM	54% modulation	–	0.5	1.0	%
S/N (W)	weighted signal-to-noise ratio					
	FM	25 kHz frequency deviation	–	60	–	dB
	AM	54% modulation	47	53	–	dB

BLOCK DIAGRAM

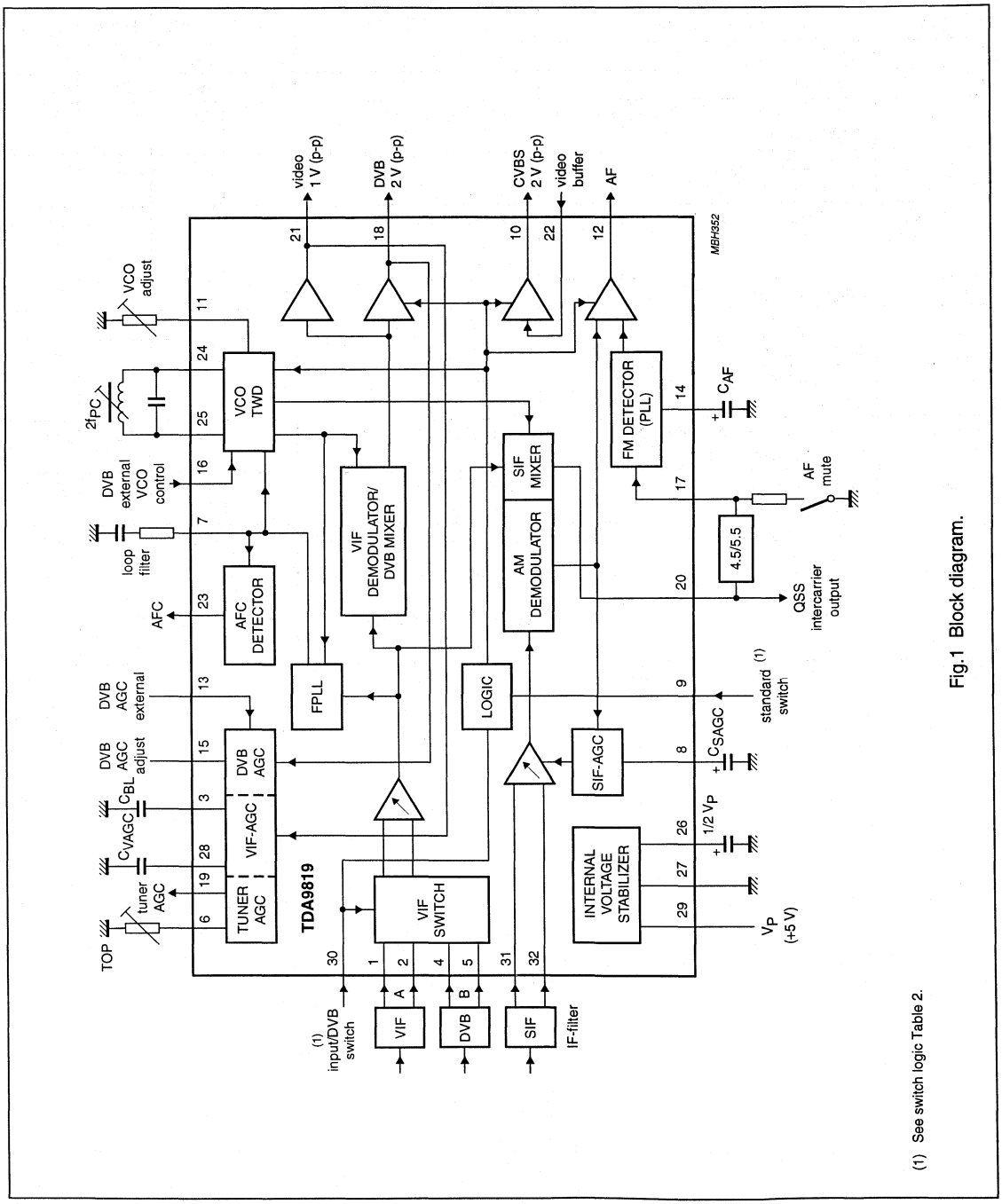


Fig.1 Block diagram.

(1) See switch logic Table 2.

PINNING

SYMBOL	PIN	DESCRIPTION
$V_{i\ VIF1}$	1	VIF differential input signal voltage 1
$V_{i\ VIF2}$	2	VIF differential input signal voltage 2
C_{BL}	3	black level detector
$V_{i\ VIF3}$	4	VIF differential input signal voltage 3
$V_{i\ VIF4}$	5	VIF differential input signal voltage 4
TADJ	6	tuner AGC takeover adjust (TOP)
T_{PLL}	7	PLL loop filter
C_{SAGC}	8	SIF AGC capacitor
STD	9	standard switch input
$V_{o\ CVBS}$	10	2 V CVBS output signal voltage
VCOADJ	11	VCO adjust BG/L/M
$V_{o\ AF}$	12	audio voltage frequency output
$V_{AGC(ext)}$	13	external AGC voltage (DVB)
C_{AF}	14	AF decoupling capacitor
AGCADJ	15	AGC adjust (DVB)
$V_{VCO(ext)}$	16	external VCO control voltage (DVB)
$V_{i\ FM}$	17	sound intercarrier input
DVB	18	DVB output
TAGC	19	tuner AGC output
$V_{o\ QSS}$	20	single reference QSS output voltage
$V_{o(vid)}$	21	composite video output voltage
$V_{i(vid)}$	22	video buffer input voltage
AFC	23	AFC output
VCO1	24	VCO1 reference circuit for $2f_{PC}$
VCO2	25	VCO2 reference circuit for $2f_{PC}$
C_{ref}	26	$\frac{1}{2}V_P$ reference capacitor
GND	27	ground
C_{VAGC}	28	VIF AGC capacitor
V_P	29	supply voltage (+5 V)
INSWI	30	VIF input switch
$V_{i\ SIF1}$	31	SIF differential input signal voltage 1
$V_{i\ SIF2}$	32	SIF differential input signal voltage 2

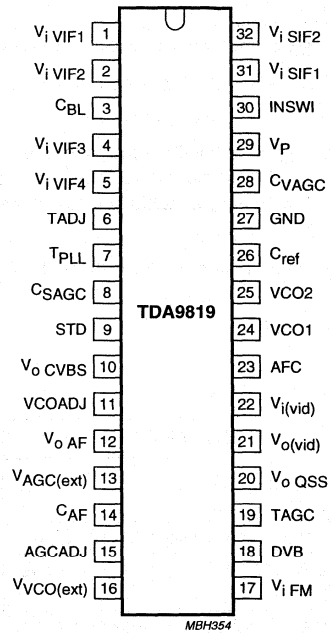


Fig.2 Pin configuration.

I²C-bus controlled BTSC stereo/SAP decoder TDA9850

FEATURES

- Quasi alignment-free application due to automatic adjustment of channel separation via I²C-bus
- Dbx noise reduction circuit
- Dbx decoded stereo, Second Audio Program (SAP) or mono selectable at the AF outputs
- Additional SAP output without dbx, including de-emphasis
- High integration level with automatically tuned integrated filters
- Input level adjustment I²C-bus controlled
- Alignment-free SAP processing
- Stereo pilot PLL circuit with ceramic resonator, automatic adjustment procedure for stereo channel separation, two pilot thresholds selectable via I²C-bus
- Automatic pilot cancellation
- Composite input noise detector with I²C-bus selectable thresholds for stereo and SAP off
- I²C-bus transceiver.

GENERAL DESCRIPTION

The TDA9850 is a bipolar-integrated BTSC stereo/SAP decoder (I²C-bus controlled) for application in TV sets, VCRs and multimedia.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		8.5	9	9.5	V
I_{CC}	supply current		–	58	75	mA
$V_{comp(rms)}$	input signal voltage (RMS value)	100% modulation L + R; f_i = 300 Hz	–	250	–	mV
$V_{oR(rms)}$; $V_{oL(rms)}$	output signal voltage (RMS value)	100% modulation L + R; f_i = 300 Hz	–	500	–	mV
G_{LA}	input level adjustment control		–3.5	–	+4.0	dB
α_{cs}	stereo channel separation	f_L = 300 Hz; f_R = 3 kHz	25	35	–	dB
$THD_{L,R}$	total harmonic distortion L + R	f_i = 1 kHz	–	0.2	–	%
S/N	signal-to-noise ratio	500 mV (RMS) mono output signal				
		CCIR noise weighting filter (peak value)	–	60	–	dB
		DIN noise weighting filter (RMS value)	–	73	–	dBA

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9850	SDIP32	plastic shrink dual in-line package; 32 leads (400 mil)	SOT232-1
TDA9850T	SO32	plastic small outline package; 32 leads; body width 7.5 mm	SOT287-1

License information

A license is required for the use of this product. For further information, please contact:

COMPANY	BRANCH	ADDRESS
THAT Corporation	Licensing Operations	734 Forest St. Marlborough, MA 01752 USA Tel.: (508) 229-2500 Fax: (508) 229-2590
	Tokyo Office	405 Palm House, 1-20-2 Honmachi Shibuya-ku, Tokyo 151 Japan Tel.: (03) 3378-0915 Fax: (03) 3374-5191

BLOCK DIAGRAM

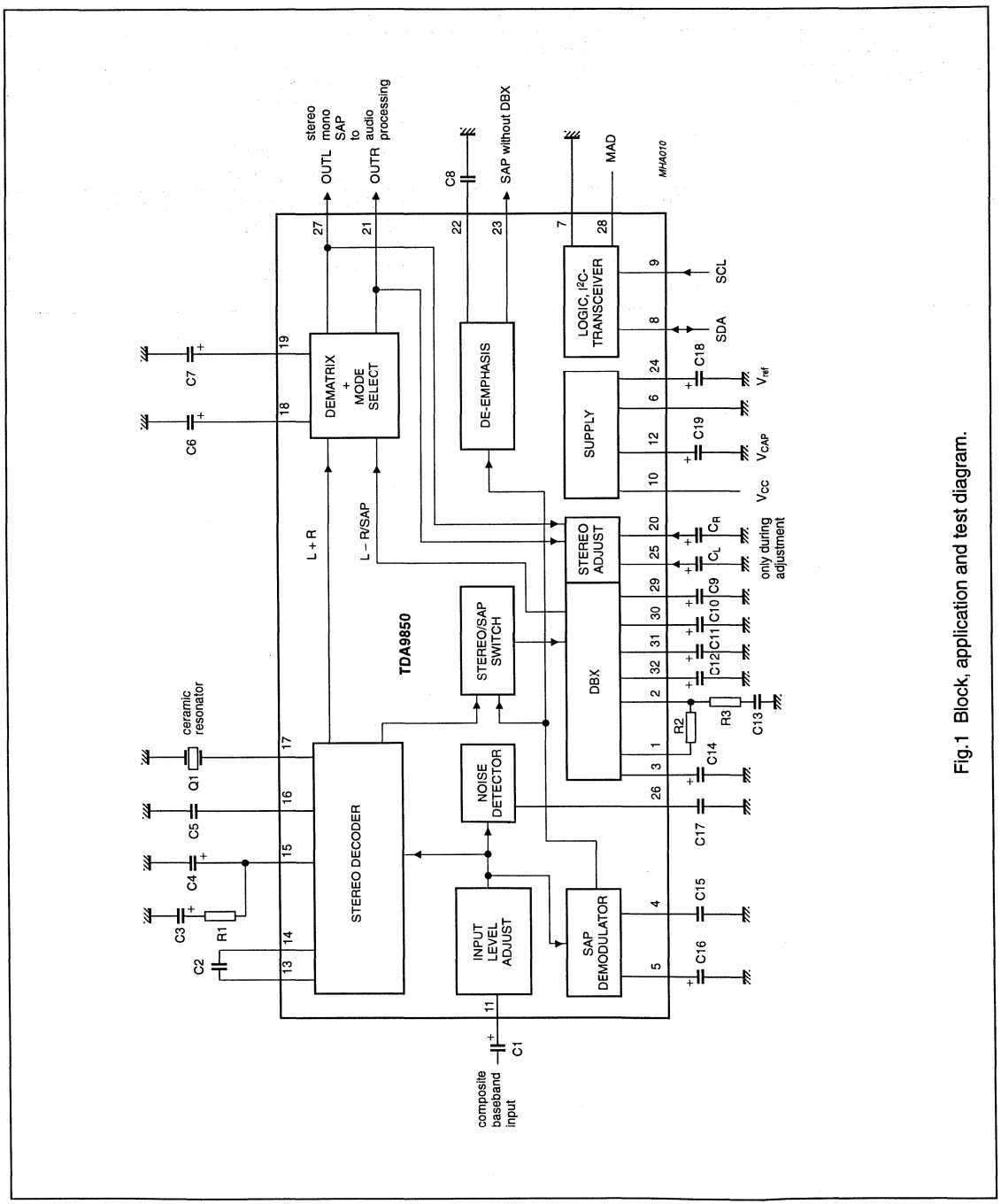


Fig.1 Block, application and test diagram.

COMPONENT LIST

Electrolytic capacitors ±20%; foil capacitors ±10%; resistors ±5%; unless otherwise specified; see Fig.1.

COMPONENT	VALUE	TYPE	REMARK
C1	10 µF	electrolytic	63 V
C2	470 nF	foil	
C3	4.7 µF	electrolytic	63 V
C4	220 nF	foil	
C5	10 µF	electrolytic	63 V; $I_{leak} < 1.5$ µA
C6	4.7 µF	electrolytic	63 V
C7	4.7 µF	electrolytic	63 V
C8	15 nF	foil	
C9	10 µF	electrolytic	63 V ±10%
C10	10 µF	electrolytic	63 V ±10%
C11	1 µF	electrolytic	63 V
C12	1 µF	electrolytic	63 V
C13	47 nF	foil	±5%
C14	10 µF	electrolytic	63 V
C15	100 nF	foil	
C16	4.7 µF	electrolytic	63 V
C17	100 nF	foil	
C18	100 µF	electrolytic	16 V
C19	100 µF	electrolytic	16 V
CR	2.2 µF	electrolytic	63 V
CL	2.2 µF	electrolytic	63 V
R1	2.2 kΩ		
R2	8.2 kΩ		±2%
R3	160 Ω		±2%
Q1		CSB503F58	radial leads
		CSB503JF958	alternative as SMD

PINNING

SYMBOL	PIN	DESCRIPTION
VEO	1	variable emphasis output for dbx
VEI	2	variable emphasis input for dbx
C_{NR}	3	capacitor noise reduction for dbx
C_M	4	capacitor mute for SAP
C_{DEC}	5	capacitor DC-decoupling for SAP
AGND	6	analog ground
DGND	7	digital ground
SDA	8	serial data input/output
SCL	9	serial clock input
V_{CC}	10	supply voltage (+9 V)
COMP	11	composite input signal
V_{CAP}	12	capacitor for electronic filtering of supply
C_{P1}	13	capacitor for pilot detector
C_{P2}	14	capacitor for pilot detector
C_{PH}	15	capacitor for phase detector
C_{ADJ}	16	capacitor for filter adjustment
CER	17	ceramic resonator
C_{MO}	18	capacitor DC-decoupling mono
C_{SS}	19	capacitor DC-decoupling stereo/SAP
C_R	20	adjustment capacitor, right channel
OUTR	21	output, right channel
C_{SDE}	22	capacitor SAP de-emphasis
SAP	23	SAP output
V_{ref}	24	reference voltage 0.5 × (V_{CC} – 1.5 V)
C_L	25	adjustment capacitor, left channel
C_{ND}	26	noise detector capacitor
OUTL	27	output, left channel
MAD	28	programmable address bit
C_{TW}	29	capacitor timing wideband for dbx
C_{TS}	30	capacitor timing spectral for dbx
C_W	31	capacitor wideband for dbx
C_S	32	capacitor spectral for dbx

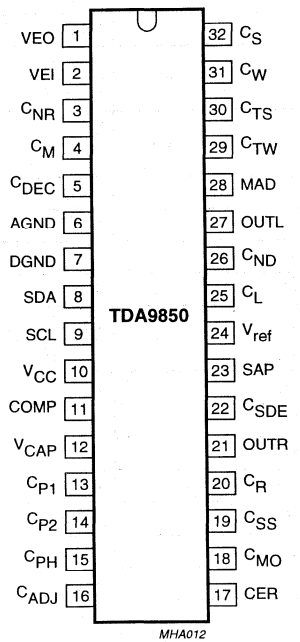


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Input level adjustment

The composite input signal is fed to the input level adjustment stage. The control range is from −3.5 to +4.0 dB in steps of 0.5 dB. The subaddress control 4 of Tables 5 and 6 and the level adjust setting of Table 10 allows an optimum signal adjustment during the set alignment. The maximum input signal voltage is 2 V (RMS).

Stereo decoder

The output signal of the level adjustment stage is coupled to a low-pass filter which suppresses the baseband noise above 125 kHz. The composite signal is then fed into a pilot detector/pilot cancellation circuit and into the MPX demodulator. The main L + R signal passes a 75 μs fixed de-emphasis filter and is fed into the dematrix circuit. The decoded sub-signal L − R is sent to the stereo/SAP switch. To generate the pilot signal the stereo demodulator uses a PLL circuit including a ceramic resonator. The stereo channel separation is adjusted by an automatic procedure to be performed during set production. For a detailed description see Section "Adjustment procedure". The stereo identification can be read by the I²C-bus (see Table 2). Two different pilot thresholds (data STS = 1; STS = 0) can be selected via the I²C-bus (see Table 14).

SAP demodulator

The composite signal is fed from the output of the input level adjustment stage to the SAP demodulator circuit through a $5f_H$ band-pass filter. The demodulator level is automatically controlled. The SAP demodulator includes an internal field strength detector that mutes the SAP output in the event of insufficient signal conditions. The SAP identification signal can be read by the I²C-bus (see Table 2).

Noise detector

The composite input noise increases with decreasing antenna signal. This makes it necessary to switch stereo or SAP off at certain thresholds. These thresholds can be set via the I²C-bus. With ST0 to ST3 (see Table 6) the stereo threshold can be selected and with SP0 to SP3 the SAP threshold. A hysteresis can be achieved via software by making the threshold dependent of the identification bits STP and SAPP (see Table 2).

Mode selection

The stereo/SAP switch feeds either the L − R signal or the SAP demodulator output signal via the internal dbx noise reduction circuit to the dematrix/switching circuit. Table 8 shows the different switch modes provided at the output pins OUTR and OUTL.

dbx decoder

The dbx circuit includes all blocks required for the noise reduction system in accordance with the BTSC system specification. The output signal is fed through a 73 μs fixed de-emphasis circuit to the dematrix block.

SAP output

Independent of the stereo/SAP switch, the SAP signal is also available at pin SAP. At SAP, the SAP signal is not dbx decoded. The capacitor at SDE provides a recommended de-emphasis (150 μs) at SAP.

Integrated filters

The filter functions necessary for stereo and SAP demodulation and part of the dbx filter circuits are provided on-chip using transconductor circuits. The required filter accuracy is attained by an automatic filter alignment circuit.

Adjustment procedure

Composite input level adjustment

Feed in from FM demodulator the composite signal with 100% modulation (25 kHz deviation) L + R; f_i = 300 Hz. Set input level control via I²C-bus monitoring OUTL or OUTR (500 mV ±20 mV). Store the setting in a non-volatile memory.

Automatic adjustment procedure

- Connect 2.2 µF capacitors from ACR and ACL to ground.
- Composite input signal L = 300 Hz, R = 3.1 kHz, 14% modulation for each channel.
- Mode selection setting bits: STEREO = 1, SAP = 0 (see Table 8).
- Start adjustment by transmission ADJ = 1 in register ALI3. The decoder will align itself.
- After 1 second minimum stop alignment by transmitting ADJ = 0 in register ALI3 read the alignment data by an I²C-bus read operation from ALR1 and ALR2 (see Chapter "I²C-bus protocol") and store it in a non-volatile memory. The alignment procedure overwrites the previous data stored in ALI1 and ALI2.
- The capacitors from ACR and ACL may be disconnected after alignment.

Manual adjustment

Manual adjustment is necessary when no dual tone generator is available (e.g. for service).

- Spectral and wideband data have to be set to 10000 (middle position for adjustment range)
- Composite input L = 300 Hz; 14% modulation
- Adjust channel separation by varying wideband data
- Composite input L = 3 kHz; 14% modulation
- Adjust channel separation by varying spectral data
- Iterative spectral/wideband operation for optimum adjustment
- Store data in non-volatile memory.

After every power-on, the alignment data and the input level adjustment data must be loaded from the non-volatile memory.

Timing current for release rate

Due to possible internal and external spreading, the timing current can be adjusted via I²C-bus, see Table 9, as recommended by dbx.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		0	10	V
V_{VCAP}	voltage of V_{CAP} to GND		0	V_{CC}	V
V_{VEO}	voltage of VEO to GND		0	$\frac{1}{2}V_{CC}$	V
V_{SDA}	voltage of SDA to GND		0	8.5	V
V_{SCL}	voltage of SCL to GND		0	8.5	V
V_n	voltage of all other pins to GND	$V_{CC} \geq 8.5$ V	0	8.5	V
		$V_{CC} < 8.5$ V	0	V_{CC}	V
T_{amb}	operating ambient temperature	$T_j < 125$ °C	−20	+70	°C
T_{stg}	storage temperature		−65	+150	°C
V_{es}	electrostatic handling	HBM; note 1			

Note

1. Human Body Model (HBM): C = 100 pF; R = 1.5 kΩ; V = 2 kV; charge device model: C = 200 pF; R = 0 Ω; V = 300 V.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	SOT232-1	55	K/W
	SOT287-1	68	K/W

REQUIREMENTS FOR THE COMPOSITE INPUT SIGNAL TO ENSURE CORRECT SYSTEM PERFORMANCE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$COMP_{L+R(rms)}$	composite input level for 100% modulation L + R (25 kHz deviation); RMS value; f_i = 300 Hz	measured at COMP	162	250	363	mV
ΔCOMP	composite input level spreading under operating conditions	T_{amb} = –20 to +70 °C; aging; power supply influence	–0.5	–	+0.5	dB
Z_{source}	source impedance	note 1	–	low-ohmic	5	kΩ
f_{lf}	low frequency roll-off	25 kHz deviation L + R; –2 dB	–	–	5	Hz
f_{hf}	high frequency roll-off	25 kHz deviation L + R; –2 dB	100	–	–	kHz
$THD_{L,R}$	total harmonic distortion L + R	f_i = 1 kHz; 25 kHz deviation	–	–	0.5	%
		f_i = 1 kHz; 125 kHz deviation; note 2	–	–	1.5	%
S/N	signal-to-noise ratio L + R/noise	CCIR 468-2 weighted quasi peak; L + R; 25 kHz deviation; f_i = 1 kHz; 75 μs de-emphasis				
	critical picture modulation; note 3		44	–	–	dB
	with sync only		54	–	–	dB
α_{SB}	side band suppression mono into unmodulated SAP carrier; SAP carrier/side band	mono signal: 25 kHz deviation, f_i = 1 kHz; side band: SAP carrier frequency ±1 kHz	40	–	–	dB
α_{SP}	spectral spurious attenuation L + R/spurious	50 Hz to 100 kHz; mainly n × f_H; no de-emphasis; L + R; 25 kHz deviation, f = 1 kHz as reference				
	n = 1, 4, 5, 6		35	–	–	dB
	n = 2, 3		26	–	–	dB

Notes

1. Low-ohmic preferred, otherwise the signal loss and spreading at COMP, caused by Z_O and the composite input impedance (see Chapter "Characteristics"; row head "Input level adjustment control") must be taken into account.
2. In order to prevent clipping at over-modulation (maximum deviation in the BTSC system for 100% modulation is 73 kHz).
3. For example colour bar or flat field white; 100% video modulation.

CHARACTERISTICS

All voltages are measured relative to GND; V_{CC} = 9 V; R_s = 600 Ω; R_L = 10 kΩ; AC-coupled; C_L = 2.5 nF; f_i = 1 kHz; T_{amb} = +25 °C; see Fig.1; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CC}	supply voltage		8.5	9	9.5	V
$V_{ripple(p-p)}$	allowed supply voltage ripple (peak-to-peak value)	f_i = 50 Hz to 100 kHz	–	–	100	mV
I_{CC}	supply current		–	58	75	mA
V_{ref}	internal reference voltage at pin V_{ref}		–	3.7	–	V
α_{ct}	crosstalk between bus inputs and signal outputs	notes 1 and 2	–	110	–	dB
Input level adjustment control						
G_{LA}	input level adjustment control		–3.5	–	+4.0	dB
G_{step}	step resolution		–	0.5	–	dB
$V_{i(rms)}$	maximum input voltage level (RMS value)		2	–	–	V
Z_i	input impedance		29.5	35	40.5	kΩ
Stereo decoder						
MPX_{L+R}	input voltage level for 100% modulation L + R; 25 kHz deviation (RMS value)	input level adjusted via I²C-bus (L + R; f_i = 300 Hz); monitoring OUTL or OUTR	–	250	–	mV
MPX_{L-R}	input voltage level for 100% modulation L – R; 50 kHz deviation (peak value)		–	707	–	mV
$MPX_{(max)}$	maximum headroom for L + R, L, R	f_{mod} < 15 kHz; THD < 15%	9	–	–	dB
MPX_{pilot}	nominal stereo pilot voltage level (RMS value)		–	50	–	mV
$ST_{on(rms)}$	pilot threshold voltage stereo on (RMS value)	data STS = 1	–	–	35	mV
		data STS = 0	–	–	30	mV
$ST_{off(rms)}$	pilot threshold voltage stereo off (RMS value)	data STS = 1	15	–	–	mV
		data STS = 0	10	–	–	mV
Hys	hysteresis		–	2.5	–	dB
OUT_{L+R}	output voltage level for 100% modulation L + R at OUTL, OUTR	input level adjusted via I²C-bus (L + R; f_i = 300 Hz); monitoring OUTL or OUTR	480	500	520	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
α_{cs}	stereo channel separation L/R	aligned with dual tone 14% modulation for each channel; see Section "Adjustment procedure"				
		f_L = 300 Hz; f_R = 3 kHz	25	35	–	dB
		f_L = 300 Hz; f_R = 8 kHz	20	30	–	dB
		f_L = 300 Hz; f_R = 10 kHz	15	25	–	dB
$f_{L, R}$	L, R frequency response	14% modulation; f_{ref} = 300 Hz L or R				
		f_i = 50 Hz to 10 kHz	–3	–	–	dB
		f_i = 12 kHz	–	–3	–	dB
$THD_{L,R}$	total harmonic distortion L, R	modulation L or R 1% to 100%; f_i = 1 kHz	–	0.2	1.0	%
S/N	signal-to-noise ratio	mono mode; CCIR 468-2 weighted; quasi peak; 500 mV output signal	50	60	–	dB
Stereo decoder, oscillator (VCXO); note 3						
f_o	nominal VCXO output frequency ($32f_H$)	with nominal ceramic resonator	–	503.5	–	kHz
f_{of}	spread of free-running frequency	with nominal ceramic resonator	500.0	–	507.0	kHz
Δf_H	capture range frequency (nominal pilot)		±190	±265	–	Hz
SAP demodulator; note 4						
$SAP_{i(rms)}$	nominal SAP carrier input voltage level (RMS value)	15 kHz frequency deviation of intercarrier	–	150	–	mV
$SAP_{on(rms)}$	threshold voltage SAP on (RMS value)		–	–	68	mV
$SAP_{off(rms)}$	threshold voltage SAP off (RMS value)		28	–	–	mV
SAP_{hys}	hysteresis		–	2	–	dB
SAP_{LEV}	SAP output voltage level at OUTL, OUTR	mode selector in position SAP/SAP; f_{mod} = 300 Hz; 100% modulation	–	500	–	mV
f_{res}	frequency response	14% modulation; 50 Hz to 8 kHz; f_{ref} = 300 Hz	–3	–	–	dB
THD	total harmonic distortion	f_i = 1 kHz	–	0.5	2.0	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SAP output						
Z_o	output impedance		–	80	120	Ω
V_O	DC output voltage		–	$0.5V_{CC}$–1.5	–	V
R_L	output load resistance (AC-coupled)		5	–	–	kΩ
C_L	output load capacitance		–	–	2.5	nF
$V_{o(rms)}$	nominal output voltage (RMS value)	150 µs de-emphasis	see Fig.3			
Outputs OUTL and OUTR						
$V_{o(rms)}$	nominal output voltage (RMS value)	100% modulation	–	500	–	mV
$HEAD_o$	output headroom		9	–	–	dB
Z_o	output impedance		–	80	120	Ω
V_O	DC output voltage		$0.45V_{CC}$–1.5	$0.5V_{CC}$–1.5	$0.55V_{CC}$–1.5	V
R_L	output load resistance (AC-coupled)		5	–	–	kΩ
C_L	output load capacitance		–	–	2.5	nF
α_{ct}	crosstalk L, R into SAP	100% modulation; f_i = 1 kHz; L or R; mode selector switched to SAP/SAP	50	75	–	dB
	crosstalk SAP into L, R	100% modulation; f_i = 1 kHz; SAP; mode selector switched to stereo	50	70	–	dB
ΔV_{ST-SAP}	output voltage difference if switched from L, R to SAP	250 Hz to 6.3 kHz	–	–	3	dB
Dbx noise reduction circuit						
t_{adj}	stereo adjustment time	see Section "Adjustment procedure"	–	–	1	s
I_s	nominal timing current for nominal release rate of spectral RMS detector	I_s can be measured at pin C_{TS} via current meter connected to $\frac{1}{2}V_{CC}$ + 0.25 V	–	24	–	µA
ΔI_s	spread of timing current		–15	–	+15	%
$I_{s\ range}$	timing current range	7 steps via I²C-bus	–	±30	–	%
I_t	timing current for release rate of wideband RMS detector		–	$\frac{1}{3}I_s$	–	µA
Rel_{rate}	nominal RMS detector release rate	nominal timing current and external capacitor values				
	wideband		–	125	–	dB/s
	spectral		–	381	–	dB/s

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Noise detector						
f_0	noise band-pass centre frequency	composite input level 100 mV (RMS)	–	185	–	kHz
Q	quality factor		–	6	–	–
Ster1, SAP1	lowest noise threshold for stereo off respectively SAP off (RMS value; see Tables 11 and 12)	f_i = 185 kHz	17	24	34	mV
Ster16, SAP16	highest noise threshold for stereo off respectively SAP off (RMS value)	f_i = 185 kHz	210	290	400	mV
ΔSter, ΔSAP	noise threshold step width	f_i = 185 kHz	0	1.5	3	dB
Power-on reset; note 5						
$V_{RESET(STA)}$	start of reset voltage	increasing supply voltage	–	–	2.5	V
		decreasing supply voltage	4.2	5	5.8	V
$V_{RESET(END)}$	end of reset voltage	increasing supply voltage	5.2	6	6.8	V
Digital part (I²C-bus pins); note 6						
V_{IH}	HIGH level input voltage		3	–	8.5	V
V_{IL}	LOW level input voltage		–0.3	–	+1.5	V
I_{IH}	HIGH level input current		–10	–	+10	μA
I_{IL}	LOW level input current		–10	–	+10	μA
V_{OL}	LOW level output voltage	I_{IL} = 3 mA	–	–	0.4	V

Notes to the characteristics

1. Crosstalk: $20 \log \frac{V_{bus(p-p)}}{V_{o(rms)}}$
2. The transmission contains:
   a) Total initialization with MAD and SAD for volume and 11 DATA words, see also definition of characteristics
   b) Clock frequency = 50 kHz
   c) Repetition burst rate = 400 Hz
   d) Maximum bus signal amplitude = 5 V (p-p).
3. The oscillator is designed to operate together with MURATA resonator CSB503F58 or CSB503JF958 as SMD. Change of the resonator supplier is possible, but the resonator specification must be close to the specified ones.
4. The internal SAP carrier level is determined by the composite input level and the level adjustment gain.
5. When reset is active the SMU-bit (SAP mute) and the LMU-bit (OUTL, OUTR mute) is set and the I²C-bus receiver is in the reset position.
6. The AC characteristics are in accordance with the I²C-bus specification for standard mode (clock frequency maximum 100 kHz). A higher frequency, up to 280 kHz, can be used if all clock and data times are interpolated between standard mode (100 kHz) and fast mode (400 kHz) in accordance with the I²C-bus specification. Information about the I²C-bus can be found in brochure *"I²C-bus and how to use it"* (order number 9398 393 40011).

I²C-BUS PROTOCOL

I²C-bus format to read (slave transmits data)

S	SLAVE ADDRESS	R/$\overline{W}$	A	DATA	MA	DATA	P

Table 1 Explanation of I²C-bus format to read (slave transmits data)

NAME	DESCRIPTION
S	START condition; generated by the master
Standard SLAVE ADDRESS (MAD)	1011011 pin MAD not connected
Pin programmable SLAVE ADDRESS	1011010 pin MAD connected to ground
R/$\overline{W}$	1 (read); generated by the master
A	acknowledge; generated by the slave
DATA	slave transmits an 8-bit data word
MA	acknowledge; generated by the master
P	STOP condition; generated by the master

Table 2 Definition of the transmitted bytes after read condition

FUNCTION	BYTE	MSB							LSB
		D7	D6	D5	D4	D3	D2	D1	D0
Alignment read 1	ALR1	Y	SAPP	STP	A14	A13	A12	A11	A10
Alignment read 2	ALR2	Y	SAPP	STP	A24	A23	A22	A21	A20

Table 3 Function of the bits in Table 2

BITS	FUNCTION
STP	stereo pilot identification (stereo received = 1)
SAPP	SAP pilot identification (SAP received = 1)
A1X to A2X	stereo alignment read data
A1X	for wideband expander
A2X	for spectral expander
Y	indefinite

The master generates an acknowledge when it has received the first data word, ALR1, then the slave transmits the next data word ALR2. The master next generates an acknowledge, then slave begins transmitting the first data word ALR1, and so on until the master generates no acknowledge and transmits a STOP condition.

I²C-bus format to write (slave receives data)

S	SLAVE ADDRESS	R/$\overline{W}$	A	SUBADDRESS	A	DATA	A	P

Table 4 Explanation of I²C-bus format to write (slave receives data)

NAME	DESCRIPTION
S	START condition
Standard SLAVE ADDRESS (MAD)	101 101 1 pin MAD not connected
Pin programmable SLAVE ADDRESS	101 101 0 pin MAD connected to ground
R/$\overline{W}$	0 (write)
A	acknowledge; generated by the slave
SUBADDRESS (SAD)	see Table 5
DATA	see Table 6
P	STOP condition

If more than 1 byte of DATA is transmitted, then auto-increment is performed, starting from the transmitted subaddress and auto-increment of subaddress in accordance with the order of Table 5 is performed.

Table 5 Subaddress second byte after MAD

FUNCTION	REGISTER	MSB							LSB
		D7	D6	D5	D4	D3	D2	D1	D0
Control 1	CON1	0	0	0	0	0	1	0	0
Control 2	CON2	0	0	0	0	0	1	0	1
Control 3	CON3	0	0	0	0	0	1	1	0
Control 4	CON4	0	0	0	0	0	1	1	1
Alignment 1	ALI1	0	0	0	0	1	0	0	0
Alignment 2	ALI2	0	0	0	0	1	0	0	1
Alignment 3	ALI3	0	0	0	0	1	0	1	0

Table 6 Definition of third byte, third byte after MAD and SAD

FUNCTION	REGISTER	MSB							LSB
		D7	D6	D5	D4	D3	D2	D1	D0
Control 1	CON1	0	0	0	0	ST3	ST2	ST1	ST0
Control 2	CON2	0	0	0	0	SP3	SP2	SP1	SP0
Control 3	CON3	SAP	STEREO	0	SMU	LMU	0	0	0
Control 4	CON4	0	0	0	0	L3	L2	L1	L0
Alignment 1	ALI1	0	0	0	A14	A13	A12	A11	A10
Alignment 2	ALI2	STS	0	0	A24	A23	A22	A21	A20
Alignment 3	ALI3	ADJ	0	0	0	0	TC2	TC1	TC0

Table 7 Function of the bits in Table 6

BITS	FUNCTION
ST0 to ST3	noise threshold for stereo
SP0 to SP3	noise threshold for SAP
STEREO, SAP	mode selection
LMU	mute control OUTL and OUTR
SMU	mute control SAP
L0 to L3	input level adjustment
ADJ	stereo adjustment on/off
A1X to A2X	stereo alignment data
A1X	for wideband expander
A2X	for spectral expander
TC0 to TC2	timing current alignment data
STS	stereo level switch

Table 8 Mode selection

FUNCTION MODE AT		DATA TRANSMISSION STATUS INTERNAL SWITCH, READABLE BITS: STP, SAPP	SETTING BITS	
OUTL	OUTR		STEREO	SAP
SAP	SAP	SAP received	1	1
Mute	mute	no SAP received	1	1
Left	right	STEREO received	1	0
Mono	mono	no STEREO received	1	0
Mono	SAP	SAP received	0	1
Mono	mute	no SAP received	0	1
Mono	mono	independent	0	0

Table 9 Timing current setting

FUNCTION I_S RANGE	DATA		
	TC2	TC1	TC0
+30%	1	0	0
+20%	1	0	1
+10%	1	1	1
Nominal	0	1	1
−10%	0	1	0
−20%	0	0	1
−30%	0	0	0

Table 10 Level adjust setting

G_L (dB)	DATA			
	L3	L2	L1	L0
+4.0	1	1	1	1
+3.5	1	1	1	0
+3.0	1	1	0	1
+2.5	1	1	0	0
+2.0	1	0	1	1
+1.5	1	0	1	0
+1.0	1	0	0	1
+0.5	1	0	0	0
0.0	0	1	1	1
−0.5	0	1	1	0
−1.0	0	1	0	1
−1.5	0	1	0	0
−2.0	0	0	1	1
−2.5	0	0	1	0
−3.0	0	0	0	1
−3.5	0	0	0	0

Table 11 Stereo noise threshold (Ster)

THRESHOLD	DATA			
	ST3	ST2	ST1	ST0
Ster1	0	0	0	0
Ster2	0	0	0	1
Ster3	0	0	1	0
Ster4	0	0	1	1
Ster5	0	1	0	0
Ster6	0	1	0	1
Ster7	0	1	1	0
Ster8	0	1	1	1
Ster9	1	0	0	0
Ster10	1	0	0	1
Ster11	1	0	1	0
Ster12	1	0	1	1
Ster13	1	1	0	0
Ster14	1	1	0	1
Ster15	1	1	1	0
Ster16	1	1	1	1

Table 12 SAP noise threshold (SAP)

THRESHOLD	DATA			
	SP3	SP2	SP1	SP0
SAP1	0	0	0	0
SAP2	0	0	0	1
SAP3	0	0	1	0
SAP4	0	0	1	1
SAP5	0	1	0	0
SAP6	0	1	0	1
SAP7	0	1	1	0
SAP8	0	1	1	1
SAP9	1	0	0	0
SAP10	1	0	0	1
SAP11	1	0	1	0
SAP12	1	0	1	1
SAP13	1	1	0	0
SAP14	1	1	0	1
SAP15	1	1	1	0
SAP16	1	1	1	1

Table 13 ADJ bit setting

FUNCTION	DATA
Stereo decoder operation mode	0
Auto adjustment of channel separation	1

Table 14 STS bit setting (pilot threshold stereo on)

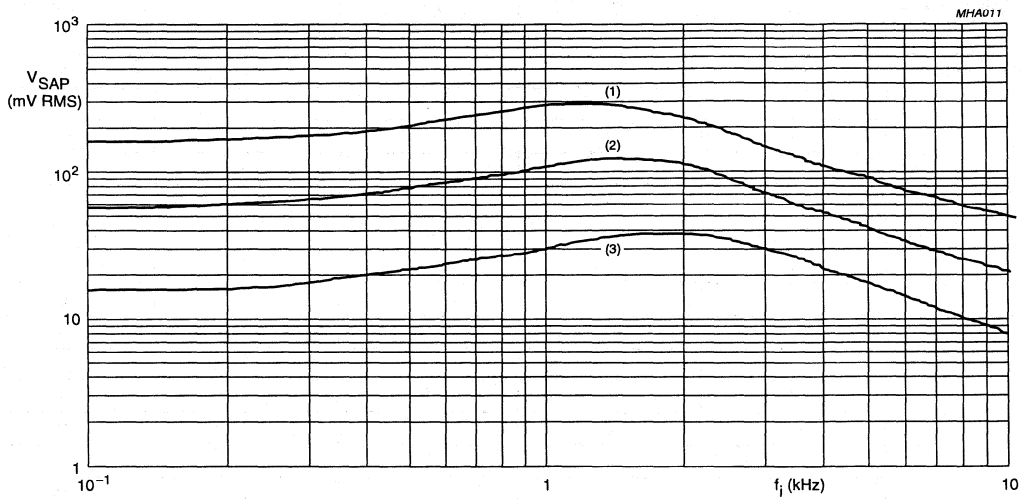
FUNCTION	DATA
$ST_{on} \leq 35$ mV	1
$ST_{on} \leq 30$ mV	0

Table 15 Mute setting

FUNCTION	DATA LMU	FUNCTION	DATA SMU
Forced mute at OUTR, OUTL	1	forced mute at SAP	1
No forced mute at OUTR, OUTL	0	no forced mute at SAP	0

Table 16 Alignment data for expander in read register ALR1 and ALR2 and in write register ALI1 and ALI2

FUNCTION	DATA				
	D4 AX4	D3 AX3	D2 AX2	D1 AX1	D0 AX0
Gain increase	1	1	1	1	1
	1	1	1	1	0
	1	1	1	0	1
	1	1	1	0	0
	1	1	0	1	1
	1	1	0	1	0
	1	1	0	0	1
	1	1	0	0	0
	1	0	1	1	1
	1	0	1	1	0
	1	0	1	0	1
	1	0	1	0	0
	1	0	0	1	1
	1	0	0	1	0
	1	0	0	0	1
Nominal gain	1	0	0	0	0
	0	1	1	1	1
Gain decrease	0	1	1	1	0
	0	1	1	0	1
	0	1	1	0	0
	0	1	0	1	1
	0	1	0	1	0
	0	1	0	0	1
	0	1	0	0	0
	0	0	1	1	1
	0	0	1	1	0
	0	0	1	0	1
	0	0	1	0	0
	0	0	0	1	1
	0	0	0	1	0
	0	0	0	0	1
	0	0	0	0	0



150 µs de-emphasis.
(1) 100% modulation.
(2) 14% modulation.
(3) 1% modulation.

Fig.3 Voltage at SAP output.

INTERNAL PIN CONFIGURATIONS

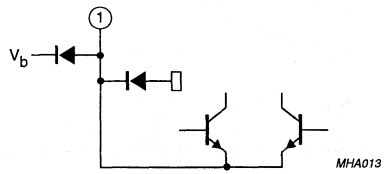


Fig.4 Pin 1; VEO.

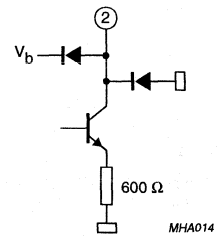


Fig.5 Pin 2; VEI.

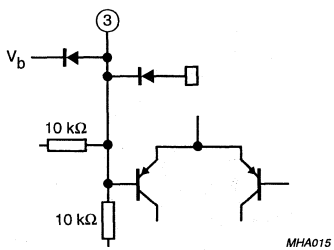


Fig.6 Pin 3; C_{NR}.

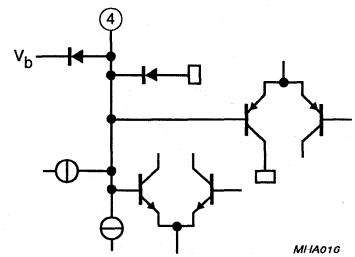


Fig.7 Pin 4; C_M.

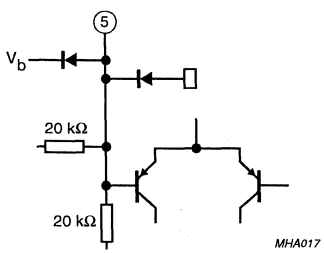


Fig.8 Pin 5; C_{DEC}.

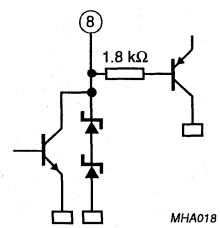


Fig.9 Pin 8; SDA.

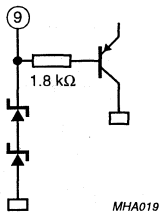


Fig.10 Pin 9; SCL.

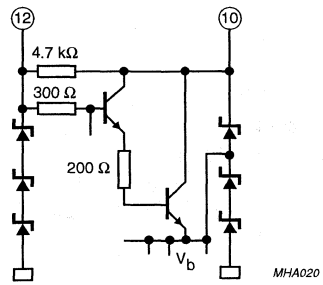


Fig.11 Pin 10; V_{CC} and pin 12; V_{CAP}.

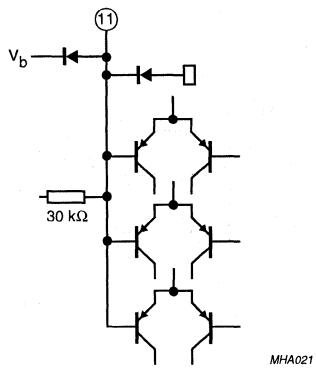


Fig.12 Pin 11; COMP.

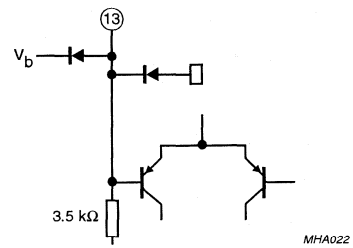


Fig.13 Pin 13; C_{P1}.

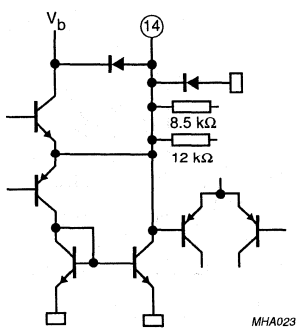


Fig.14 Pin 14; C_{P2}.

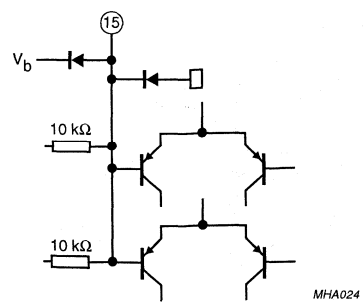


Fig.15 Pin 15; C_{PH}.

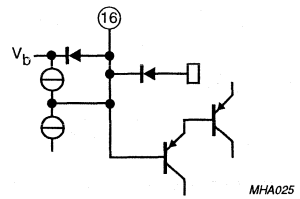


Fig.16 Pin 16; C_{ADJ}.

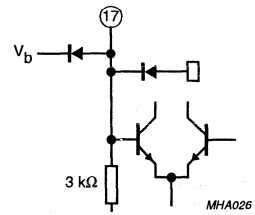


Fig.17 Pin 17; CER.

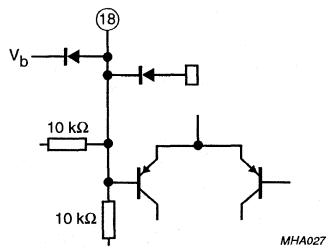


Fig.18 Pin 18; C_{MO} and pin 19; C_{SS}.

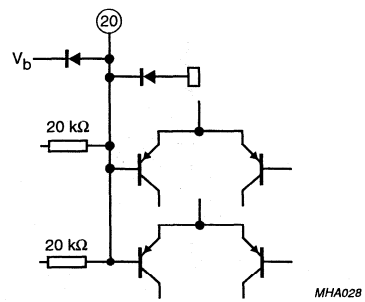


Fig.19 Pin 20; C_R and pin 25; C_L.

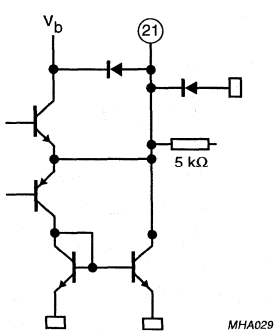


Fig.20 Pin 21; OUTR and pin 27 OUTL.

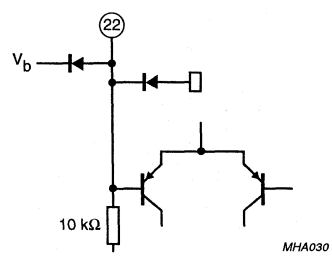


Fig.21 Pin 22; C_{SDE}.

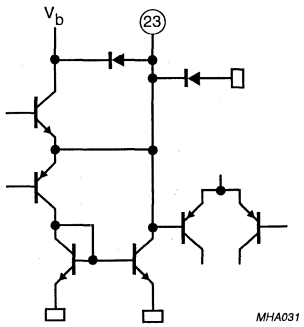


Fig.22 Pin 23; SAP.

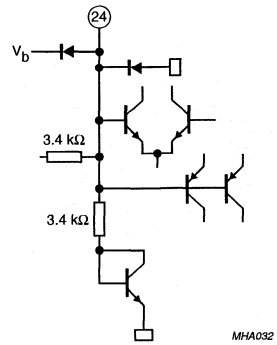


Fig.23 Pin 24; V_{ref}.

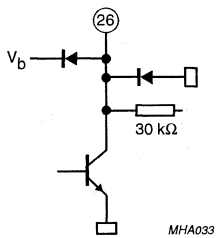


Fig.24 Pin 26; C_{ND}.

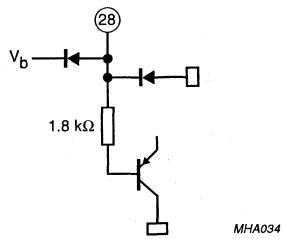


Fig.25 Pin 28; MAD.

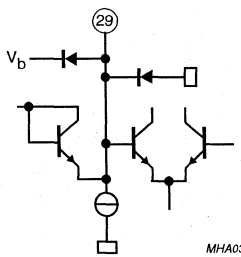


Fig.26 Pin 29; C_{TW} and pin 30; C_{TS}.

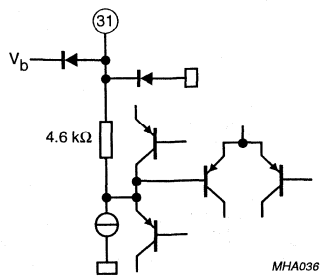


Fig.27 Pin 31; C_W and pin 32; C_S.

I²C-bus controlled BTSC stereo/SAP decoder and audio processor

TDA9852

FEATURES

- Quasi alignment-free application due to automatic adjustment of channel separation via I²C-bus
- High integration level with automatically tuned integrated filters
- Input level adjustment I²C-bus controlled
- Alignment-free SAP processing
- dbx noise reduction circuit
- Power supply
- I²C-bus transceiver.

Stereo decoder

- Stereo pilot PLL circuit with ceramic resonator, automatic adjustment procedure for stereo channel separation, two pilot thresholds selectable via I²C-bus.

Audio processor

- Selector for internal and external signals (line in)
- Automatic volume level control (control range +6 to −15 dB)
- Interface for external noise reduction circuits
- Volume control (control range +16 to −71 dB)
- Special loudness characteristic automatically controlled in combination with volume setting (control range 28 dB)
- Audio signal zero crossing detection between any volume step switching
- Mute control at audio signal zero crossing
- Mute control via I²C-bus.

GENERAL DESCRIPTION

The TDA9852 is a bipolar-integrated BTSC stereo decoder with hi-fi audio processor (I²C-bus controlled) for application in TV sets, VCRs and multimedia.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9852	SDIP42	plastic shrink dual in-line package; 42 leads (600 mil)	SOT270-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		8.0	8.5	9.0	V
I_{CC}	supply current		–	75	95	mA
$V_{comp(rms)}$	input signal voltage (RMS value)	100% modulation L + R; f_i = 300 Hz	–	250	–	mV
$V_{oR,L(rms)}$	output signal voltage (RMS value)	100% modulation L + R; f_i = 300 Hz	–	500	–	mV
G_{LA}	input level adjustment control		–3.5	–	+4.0	dB
α_{cs}	stereo channel separation	f_L = 300 Hz; f_R = 3 kHz	25	35	–	dB
$THD_{L,R}$	total harmonic distortion L + R	f_i = 1 kHz	–	0.2	–	%
$V_{I, O(rms)}$	signal handling (RMS value)	THD < 0.5%	2	–	–	V
AVL	control range		–15	–	+6	dB
G_C	volume control range		–71	–	+16	dB
L_B	maximum loudness boost	f_i = 40 Hz	–	17	–	dB
S/N	signal-to-noise ratio	line out (mono); V_o = 0.5 V (RMS)				
		CCIR noise weighting filter (peak value)	–	60	–	dB
		DIN noise weighting filter (RMS value)	–	73	–	dBA
S/N	signal-to-noise ratio	audio section; V_o = 2 V (RMS); gain = 0 dB				
		CCIR noise weighting filter (peak value)	–	94	–	dB
		DIN noise weighting filter (RMS value)	–	107	–	dBA

BLOCK DIAGRAM

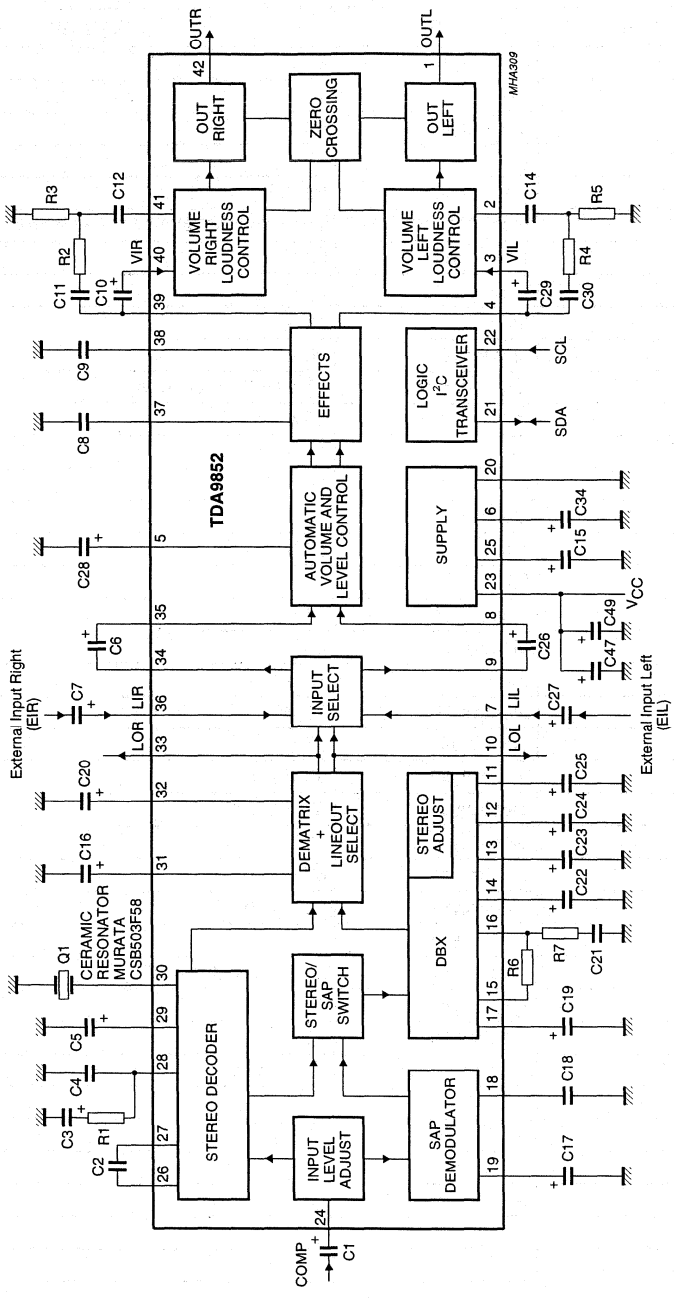


Fig.1 Block diagram.

Component list

Electrolytic capacitors ±20%; foil or ceramic capacitors ±10%; resistors ±5%; unless otherwise specified; see Fig.1.

COMPONENT	VALUE	TYPE	REMARK
C1	10 µF	electrolytic	63 V
C2	470 nF	foil	
C3	4.7 µF	electrolytic	63 V
C4	220 nF	foil	
C5	10 µF	electrolytic	63 V; I_{leak} < 1.5 µA
C6	2.2 µF	electrolytic	16 V
C7	2.2 µF	electrolytic	63 V
C8	15 nF	foil	±5%
C9	15 nF	foil	±5%
C10	2.2 µF	electrolytic	16 V
C11	8.2 nF	foil or ceramic	±5% SMD 2220/1206
C12	150 nF	foil	±5%
C14	150 nF	foil	±5%
C15	100 µF	electrolytic	16 V
C16	4.7 µF	electrolytic	63 V
C17	4.7 µF	electrolytic	63 V
C18	100 nF	foil	
C19	10 µF	electrolytic	63 V
C20	4.7 µF	electrolytic	63 V
C21	47 nF	foil	±5%
C22	1 µF	electrolytic	63 V
C23	1 µF	electrolytic	63 V
C24	10 µF	electrolytic	63 V ±10%
C25	10 µF	electrolytic	63 V ±10%
C26	2.2 µF	electrolytic	16 V
C27	2.2 µF	electrolytic	63 V
C28	4.7 µF	electrolytic	63 V ±10%
C29	2.2 µF	electrolytic	16 V
C30	8.2 nF	foil or ceramic	±5% SMD 2220/1206
C34	100 µF	electrolytic	16 V
C47	220 µF	electrolytic	25 V
C49	100 nF	foil or ceramic	SMD 1206
R1	2.2 kΩ	–	
R2	20 kΩ	–	
R3	2.2 kΩ	–	
R4	20 kΩ	–	
R5	2.2 kΩ	–	
R6	8.2 kΩ	–	±2%

COMPONENT	VALUE	TYPE	REMARK
R7	160 Ω	–	±2%
Q1		CSB503F58	radial leads
		CSB503JF958	alternative as SMD

PINNING

SYMBOL	PIN	DESCRIPTION
OUTL	1	output, left channel
LDL	2	input loudness, left channel
VIL	3	input volume, left channel
EOL	4	output effects, left channel
C_{AV}	5	automatic volume control capacitor
V_{ref}	6	reference voltage $0.5V_{CC}$
LIL	7	input line control, left channel
AVL	8	input automatic volume control, left channel
SOL	9	output selector, left channel
LOL	10	output line control, left channel
C_{TW}	11	capacitor timing wideband for dbx
C_{TS}	12	capacitor timing spectral for dbx
C_W	13	capacitor wideband for dbx
C_S	14	capacitor spectral for dbx
VEO	15	variable emphasis output for dbx
VEI	16	variable emphasis input for dbx
C_{NR}	17	capacitor noise reduction for dbx
C_M	18	capacitor mute for SAP
C_{DEC}	19	capacitor DC-decoupling for SAP
GND	20	ground
SDA	21	serial data input/output
SCL	22	serial clock input
V_{CC}	23	supply voltage
COMP	24	composite input signal
V_{CAP}	25	capacitor for electronic filtering of supply
C_{P1}	26	capacitor for pilot detector
C_{P2}	27	capacitor for pilot detector
C_{PH}	28	capacitor for phase detector
C_{ADJ}	29	capacitor for filter adjustment
CER	30	ceramic resonator
C_{MO}	31	capacitor DC-decoupling mono
C_{SS}	32	capacitor DC-decoupling stereo/SAP
LOR	33	output line control, right channel
SOR	34	output selector, right channel

SYMBOL	PIN	DESCRIPTION
AVR	35	input automatic volume control, right channel
LIR	36	input line control, right channel
C_{PS2}	37	capacitor 2 pseudo function
C_{PS1}	38	capacitor 1 pseudo function
EOR	39	output effects, right channel
VIR	40	input volume, right channel
LDR	41	input loudness, right channel
OUTR	42	output, right channel

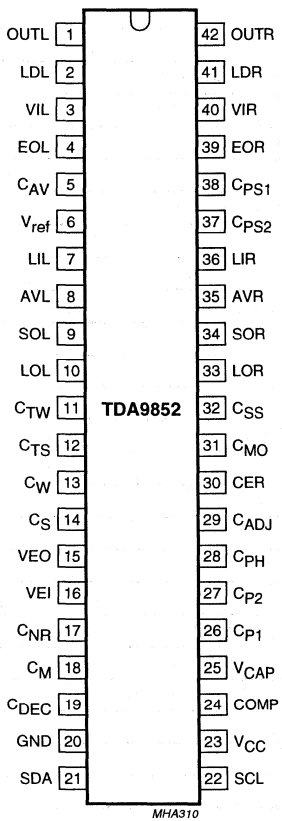


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Stereo decoder

INPUT LEVEL ADJUSTMENT

The composite input signal is fed to the input level adjustment stage. The control range is from −3.5 to +4.0 dB in steps of 0.5 dB. The subaddress control 3 of Tables 5 and 6 and the level adjust setting of Table 21 allows an optimum signal adjustment during the set alignment. The maximum input signal voltage is 2 V (RMS).

STEREO DECODER

The output signal of the level adjustment stage is coupled to a low-pass filter which suppresses the baseband noise above 125 kHz. The composite signal is then fed into a pilot detector/pilot cancellation circuit and into the MPX demodulator. The main L + R signal passes a 75 µs fixed de-emphasis filter and is fed into the dematrix circuit. The decoded sub-signal L − R is sent to the stereo/SAP switch. To generate the pilot signal the stereo demodulator uses a PLL circuit including a ceramic resonator. The stereo channel separation is adjusted by an automatic procedure to be performed during set production. For a detailed description see Section "Adjustment procedure". The stereo identification can be read by the I²C-bus (see Table 2). Two different pilot thresholds (data STS = 1; STS = 0) can be selected via the I²C-bus (see Table 19).

SAP DEMODULATOR

The composite signal is fed from the output of the input level adjustment stage to the SAP demodulator circuit through a $5f_H$ (f_H = horizontal frequency) band-pass filter. The demodulator level is automatically controlled. The SAP demodulator includes internal noise and field strength detectors that mute the SAP output in the event of

insufficient signal conditions. The SAP identification signal can be read by the I²C-bus (see Table 2).

SWITCH

The stereo/SAP switch feeds either the L – R signal or the SAP demodulator output signal via the internal dbx noise reduction circuit to the dematrix/switching circuit. Table 12 shows the different switch modes provided at the output pins LOR and LOL.

dbx DECODER

The circuit includes all blocks required for the noise reduction system in accordance with the BTSC system specification. The output signal is fed through a 73 µs fixed de-emphasis circuit to the dematrix block.

INTEGRATED FILTERS

The filter functions necessary for stereo and SAP demodulation and part of the dbx filter circuits are provided on-chip using transconductor circuits. The required filter accuracy is attained by an automatic filter alignment circuit.

Audio processor

SELECTOR

The selector allows selecting either the internal line out signals LOR or LOL (dematrix output) or the external line in signals LIR and LIL and combines the left and right signals in several modes (see Tables 5 and 6 for subaddress and Table 11 for data). The input signal capability of the line inputs (LIR/LIL) is 2 V (RMS). The output of the selector is AC-coupled to the automatic volume level control circuit via pins SOR/SOL and AVR/AVL to avoid offset voltages.

AUTOMATIC VOLUME LEVEL CONTROL

The automatic volume level stage controls its output voltage to a constant level of typically 200 mV (RMS) from an input voltage range of 0.1 to 1.1 V (RMS). The circuit adjusts variations in modulation during broadcasting and due to changes in the programme material. The function can be switched **off**. To avoid audible 'plops' during the permanent operation of the AVL circuit a soft blending scheme has been applied between the different gain stages. A capacitor (4.7 µF) at pin C_{AV} determines the attack and decay time constants. In addition the ratio of attack and decay time can be changed via I²C-bus (see Table 15). At power **on**, the discharged 4.7 µF capacitor at C_{AV} must be loaded by the internal decay current. If AVL is chosen, this would result in an attenuated AVL gain for about 10 seconds after power **on**. This can be speeded up by choosing via I²C-bus an increased charge current (about 10 times higher) for about the first 2 seconds after power **on** (see Table 6, CCD bit in control 1 and Table 18).

EFFECTS

The audio processor section offers the following mode selections: linear stereo, pseudo stereo, spatial stereo and forced mono.The spatial mode provides an antiphase crosstalk of 30% or 52% (switchable via I²C-bus; see Table 10).

VOLUME/LOUDNESS

The volume control range is from +16 dB to –71 dB in steps of 1 dB and ends with a mute step (see Table 8). Balance control is achieved by the independent volume control of each channel. The volume control blocks operate in combination with the loudness control. The filter is linear when maximum gain for volume control is selected. The filter characteristic changes automatically over a range of 28 dB down to a setting of –12 dB. At –12 dB volume control the maximum loudness boost is obtained. The filter characteristic is determined by external components. The proposed application provides a maximum boost of 17 dB for bass and 4.5 dB for treble. The loudness may be switched **on** or **off** via I²C-bus control (see Table 9). The left and right volume control stages include two independent zero crossing detectors. A change in volume is automatically activated but not executed. The execution is enabled at the next zero crossing of the signal. If a new volume step is activated before the previous one has been processed, the previous value will be executed first, and then the new value will be activated. If no zero crossing occurs the next volume transmission will enforce the last activated volume setting.

The zero crossing is realized between adjoining steps and between any steps, but not from any step to mute. In this case the GMU bit is needed to use. In case only one channel has to be muted, two steps are necessary. The first step is a transmission of any step to –71 dB and the second step is the –71 dB step to mute mode. The step of –71 dB to mute mode has no zero crossing but this is not relevant.

MUTE

The mute function can be activated independently with last step of volume control at the left or right output. By setting the general mute bit GMU via the I²C-bus all outputs are

muted. All channels include an independent zero cross detector. The zero crossing mute feature can be selected via bit TZCM:

TZCM = 0: forced mute with direct execution

TZCM = 1: execution in time with signal zero crossing.

In the zero cross mode a change in the GMU polarity is activated but not executed. The execution is enabled at the next zero crossing of the signal. To avoid a large delay of mute switching, when very low frequencies are processed, or the output signal amplitude is lower than the DC offset voltage, the following I²C-bus transmissions are needed:

a first transmission for mute execution

a second transmission about 100 ms later, which must switch the zero crossing mode to forced mute (TZCM = 0)

a third transmission to reactivate the zero crossing mode (TZCM = 1). This transmission can take place immediately, but must follow before the next mute execution.

Adjustment procedure

COMPOSITE INPUT LEVEL ADJUSTMENT

Feed in from FM demodulator the composite signal with 100% modulation (25 kHz deviation) L + R; f_i = 300 Hz. Set input level control via I²C-bus monitoring line out (500 mV ±20 mV). Store the setting in a non-volatile memory.

AUTOMATIC ADJUSTMENT PROCEDURE

- Capacitors of external inputs LIL and LIR must be grounded at EIL and EIR
- Composite input signal L = 300 Hz, R = 3.1 kHz, 14% modulation for each channel; volume gain +16 dB via I²C-bus
- Effects, AVL, loudness **off**.
- Line out setting bits: STEREO = 1, SAP = 0 (see Table 12)
- Selector setting SC0, SC1, SC2 = 0, 0, 0 (see Table 11)
- Start adjustment by transmission ADJ = 1 in register ALI3; the decoder will align itself
- After 1 second minimum stop alignment by transmitting ADJ = 0 in register ALI3 read the alignment data by an I²C-bus read operation from ALR1 and ALR2 (see Chapter "I²C-bus protocol") and store it in a non-volatile memory; the alignment procedure overwrites the previous data stored in ALI1 and ALI2
- Disconnect the capacitors of external inputs from ground.

MANUAL ADJUSTMENT

Manual adjustment is necessary when no dual tone generator is available (e.g. for service).

- Spectral and wideband data have to be set to 10000 (middle position for adjustment range)
- Composite input L = 300 Hz; 14% modulation
- Adjust channel separation by varying wideband data
- Composite input L = 3 kHz; 14% modulation
- Adjust channel separation by varying spectral data
- Iterative spectral/wideband operation for optimum adjustment
- Store data in non-volatile memory.

TIMING CURRENT FOR RELEASE RATE

Due to possible internal and external spreading, the timing current can be adjusted via I²C-bus, see Table 20, as recommended by dbx.

Requirements for the composite input signal to ensure correct system performance

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$COMP_{L+R(rms)}$	composite input level for 100% modulation L + R (25 kHz deviation); RMS value; f_i = 300 Hz	measured at COMP	162	250	363	mV
ΔCOMP	composite input level spreading under operating conditions	T_{amb} = −20 to +70 °C; aging; power supply influence	−0.5	–	+0.5	dB
Z_o	output impedance	note 1	–	low-ohmic	5	kΩ
f_{lf}	low frequency roll-off	25 kHz deviation L + R; −2 dB	–	–	5	Hz
f_{hf}	high frequency roll-off	25 kHz deviation L + R; −2 dB	100	–	–	kHz
$THD_{L,R}$	total harmonic distortion L + R	f_i = 1 kHz; 25 kHz deviation	–	–	0.5	%
		f_i = 1 kHz; 125 kHz deviation; note 2	–	–	1.5	%
S/N	signal-to-noise ratio L + R/noise	CCIR 468-2 weighted quasi peak; L + R; 25 kHz deviation; f_i = 1 kHz; 75 μs de-emphasis				
		critical picture modulation; note 3	44	–	–	dB
		with sync only	54	–	–	dB
α_{SB}	side band suppression mono into unmodulated SAP carrier; SAP carrier/side band	mono signal: 25 kHz deviation, f_i = 1 kHz; side band: SAP carrier frequency ±1 kHz	46	–	–	dB
α_{SP}	spectral spurious attenuation L + R/spurious	50 Hz to 100 kHz; mainly n × f_H; no de-emphasis; L + R; 25 kHz deviation, f = 1 kHz as reference				
		n = 1, 5	35	–	–	dB
		n = 4, 6	40	–	–	dB
		n = 2, 3	26	–	–	dB

Notes

1. Low-ohmic preferred, otherwise the signal loss and spreading at COMP, caused by Z_O and the composite input impedance (see Chapter "Characteristics", Section "Input level adjustment control") must be taken into account.
2. In order to prevent clipping at over-modulation (maximum deviation in the BTSC system for 100% modulation is 73 kHz).
3. For example colour bar or flat field white; 100% video modulation.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	0	9.5	V
V_n	voltage of all other pins to pin V_{CC}	0	V_{CC}	V
T_{amb}	operating ambient temperature	−20	+70	°C
T_{stg}	storage temperature	−65	+150	°C
V_{es}	electrostatic handling; note 1			

Note

1. Human body model: C = 100 pF; R = 1.5 kΩ; V = 2 kV; Charge device model: C = 200 pF; R = 0 Ω; V = 300 V.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	43	K/W

CHARACTERISTICS

All voltages are measured relative to GND; V_{CC} = 8.5 V; R_s = 600 Ω; R_L = 10 kΩ; C_L = 2.5 nF; AC-coupled; f_i = 1 kHz; T_{amb} = 25 °C; gain control G_v = 0 dB; balance in mid position; loudness **off**; see Fig.1; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
General						
V_{CC}	supply voltage		8.0	8.5	9.0	V
I_{CC}	supply current		–	75	95	mA
V_{ref}	internal reference voltage at pin V_{ref}		–	4.25	–	V
Input level adjustment control						
G_{LA}	input level adjustment control		−3.5	–	+4.0	dB
G_{step}	step resolution		–	0.5	–	dB
$V_{i(rms)}$	maximum input voltage level (RMS value)		2	–	–	V
Z_i	input impedance		29.5	35	40.5	kΩ
Stereo decoder						
$MPX_{L+R(rms)}$	input voltage level for 100% modulation L + R; 25 kHz deviation (RMS value)	input level adjusted via I²C-bus (L + R; f_i = 300 Hz); monitoring LINE OUT	–	250	–	mV
MPX_{L-R}	input voltage level for 100% modulation L − R; 50 kHz deviation (peak value)		–	707	–	mV
$MPX_{(max)}$	maximum headroom for L + R, L, R	f_{mod} < 15 kHz; THD < 15%	9	–	–	dB
$MPX_{pilot(rms)}$	nominal stereo pilot voltage level (RMS value)		–	50	–	mV
$ST_{on(rms)}$	pilot threshold voltage stereo **on** (RMS value)	data STS = 1	–	–	35	mV
		data STS = 0	–	–	30	mV
$ST_{off(rms)}$	pilot threshold voltage stereo **off** (RMS value)	data STS = 1	15	–	–	mV
		data STS = 0	10	–	–	mV
Hys	hysteresis		–	2.5	–	dB
OUT_{L+R}	output voltage level for 100% modulation L + R at LINE OUT	input level adjusted via I²C-bus (L + R; f_i = 300 Hz); monitoring LINE OUT	480	500	520	mV
α_{cs}	stereo channel separation L/R at LINE OUT	aligned with dual tone 14% modulation for each channel; see Section "Adjustment procedure" in Chapter "Functional description"				
		f_L = 300 Hz; f_R = 3 kHz	25	35	–	dB
		f_L = 300 Hz; f_R = 8 kHz	20	30	–	dB
		f_L = 300 Hz; f_R = 10 kHz	15	25	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$f_{L,R}$	L, R frequency response	14% modulation; f_{ref} = 300 Hz L or R				
		f_i = 50 Hz to 10 kHz	–3	–	–	dB
		f_i = 12 kHz	–	–3	–	dB
$THD_{L,R}$	total harmonic distortion L, R at LINE OUT	modulation L or R 1% to 100%; f_i = 1 kHz	–	0.2	1.0	%
S/N	signal-to-noise ratio	mono mode; CCIR 468-2 weighted; quasi peak; 500 mV output signal	50	60	–	dB
Stereo decoder, oscillator (VCXO); note 1						
f_o	nominal VCXO output frequency ($32f_H$)	with nominal ceramic resonator	–	503.5	–	kHz
f_{of}	spread of free-running frequency	with nominal ceramic resonator	500.0	–	507.0	kHz
Δf_H	capture range frequency (nominal pilot)		±190	±265	–	Hz
SAP demodulator; note 2						
$SAP_{i(rms)}$	nominal SAP carrier input voltage level (RMS value)	15 kHz frequency deviation of intercarrier	–	150	–	mV
$SAP_{on(rms)}$	threshold voltage SAP **on** (RMS value)		–	–	85	mV
$SAP_{off(rms)}$	threshold voltage SAP **off** (RMS value)		35	–	–	mV
SAP_{hys}	hysteresis		–	2	–	dB
SAP_{LEV}	SAP output voltage level at LINE OUT	mode selector in position SAP/SAP; f_{mod} = 300 Hz; 100% modulation	–	500	–	mV
f_{res}	frequency response	14% modulation; 50 Hz to 8 kHz; f_{ref} = 300 Hz	–3	–	–	dB
THD	total harmonic distortion	f_i = 1 kHz	–	0.5	2.0	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
LINE OUT at pins LOL and LOR						
$V_{o(rms)}$	nominal output voltage (RMS value)	100% modulation	–	500	–	mV
$HEAD_o$	output headroom		9	–	–	dB
Z_o	output impedance		–	80	120	Ω
V_O	DC output voltage		$0.45V_{CC}$	$0.5V_{CC}$	$0.55V_{CC}$	V
R_L	output load resistance		5	–	–	kΩ
C_L	output load capacitance		–	–	2.5	nF
α_{ct}	crosstalk L, R into SAP	100% modulation; f_i = 1 kHz; L or R; mode selector switched to SAP/SAP	50	75	–	dB
	crosstalk SAP into L, R	100% modulation; f_i = 1 kHz; SAP; mode selector switched to stereo	50	70	–	dB
ΔV_{ST-SAP}	output voltage difference if switched from L, R to SAP	250 Hz to 6.3 kHz	–	–	3	dB
dbx noise reduction circuit						
t_{adj}	stereo adjustment time	see Section "Adjustment procedure" in Chapter "Functional description"	–	–	1	s
I_s	nominal timing current for nominal release rate of spectral RMS detector	I_s can be measured at pin C_{TS} via current meter connected to $\frac{1}{2}V_{CC}$ + 1 V	–	24	–	µA
ΔI_s	spread of timing current		−15	–	+15	%
$I_{s\ range}$	timing current range	7 steps via I²C-bus	–	±30	–	%
I_t	timing current for release rate of wideband RMS detector		–	$\frac{1}{3}I_s$	–	µA
Rel_{rate}	nominal RMS detector release rate	nominal timing current and external capacitor values				
		wideband	–	125	–	dB/s
		spectral	–	381	–	dB/s

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Circuit section from pins LIL and LIR to pins OUTL and OUTR; note 3						
B	roll-off frequencies	C_6, C_7, C_{10}, C_{26}, C_{27} and C_{29} = 2.2 µF; $Z_i = Z_{i\,min}$				
		low frequency (–3 dB)	–	–	20	Hz
		high frequency (–0.5 dB)	20	–	–	kHz
THD	total harmonic distortion	V_i = 1000 mV; G_v = 0 dB; AVL **on**	–	0.2	0.5	%
		V_i = 2000 mV; G_v = 0 dB; AVL **on**	–	0.2	0.5	%
		V_i = 1000 mV; G_v = 0 dB; AVL **off**	–	0.02	–	%
		V_i = 2000 mV; G_v = 0 dB; AVL **off**	–	0.02	–	%
RR	ripple rejection	$V_{r\,(rms)}$ < 200 mV; f_i = 100 Hz	47	50	–	dB
α_{ct}	crosstalk between bus inputs and signal outputs	notes 4 and 5	–	110	–	dB
V_{no}	noise output voltage	CCIR 468-2 weighted; quasi peak; AVL **off**; loudness **off**; G_v = 0 dB	–	40	80	µV
		measured in dBA; AVL **off**; loudness **off**; G_v = 0 dB	–	8	–	µV
α_{cs}	channel separation	V_i = 1 V; f_i = 1 kHz	75	–	–	dB
		V_i = 1 V; f_i = 12.5 kHz	75	–	–	dB
Effect controls						
α_{spat1}	anti-phase crosstalk by spatial effect		–	52	–	%
α_{spat2}			–	30	–	%
φ	phase shift by pseudo-stereo	see Fig.3	–	–	–	–

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Automatic volume level control (AVL)						
Z_i	input impedance		8.8	11.0	13.2	kΩ
$V_{i(rms)}$	maximum input voltage (RMS value)	THD < 0.2%	2	tbf	–	V
G_v	gain, maximum boost		5	6	7	dB
	maximum attenuation		14	15	16	dB
G_{step}	equivalent step width between the input stages (soft switching system)		–	1.5	–	dB
$V_{iop(rms)}$	input level at maximum boost (RMS value)		–	0.1	–	V
	input level at maximum attenuation (RMS value)		–	1.125	–	V
$V_{o(rms)}$	output level in AVL operation (RMS value)	see Fig.4	160	200	250	mV
$V_{DC\ OFF}$	DC offset between different gain steps	voltage at pin C_{AV} 6.50 to 6.33 V or 6.33 to 6.11 V or 6.11 to 5.33 V or 5.33 to 2.60 V; note 6	–	–	6	mV
R_{att}	discharge resistors for attack time constant	AT1 = 0; AT2 = 0; note 7	340	420	520	Ω
		AT1 = 1; AT2 = 0; note 7	590	730	910	Ω
		AT1 = 0; AT2 = 1; note 7	0.96	1.2	1.5	kΩ
		AT1 = 1; AT2 = 1; note 7	1.7	2.1	2.6	kΩ
I_{dec}	charge current for decay time	normal mode; CCD = 0; note 8	1.6	2.0	2.4	µA
		power-on speed-up; CCD = 1; note 8	–	tbf	–	µA
Selector from pins LOL, LOR, LIL and LIR to pins SOL and SOR						
Z_i	input impedance		16	20	24	kΩ
α_s	input isolation of one selected source to the other input	V_i = 1 V; f_i = 1 kHz	86	96	–	dB
		V_i = 1 V; f_i = 12.5 kHz	80	96	–	dB
$V_{i(rms)}$	maximum input voltage (RMS value)	THD < 0.5%	2	2.3	–	V
$V_{DC\ OFF}$	DC offset voltage at selector output by selection of any inputs		–	–	25	mV
Z_o	output impedance		–	80	120	Ω
R_L	output load resistance		5	–	–	kΩ
C_L	output load capacitance		0	–	2.5	nF
G_v	voltage gain, selector		–	0	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Audio control part; input pins VIL and VIR to pins OUTX and OUTS						
Z_i	volume input impedance		8.0	10.0	12.0	kΩ
Z_o	output impedance		–	80	120	Ω
R_L	output load resistance		5	–	–	kΩ
C_L	output load capacitance		0	–	2.5	nF
$V_{i(rms)}$	maximum input voltage (RMS value)	THD < 0.5%	2.0	2.15	–	V
V_{no}	noise output voltage	CCIR 468-2 weighted; quasi peak				
		G_v = 16 dB	–	110	220	μV
		G_v = 0 dB	–	33	50	μV
		mute position	–	10	–	μV
G_c	total continuous control range	maximum boost	–	16	–	dB
		maximum attenuation	–	71	–	dB
G_{step}	step resolution		–	1	–	dB
	step error between adjoining step		–	–	0.5	dB
ΔG_a	attenuator set error	G_v = +16 to –50 dB	–	–	2	dB
		G_v = –51 to –71 dB	–	–	3	dB
ΔG_L	gain tracking error	G_v = +16 to –50 dB	–	–	2	dB
α_m	mute attenuation		80	–	–	dB
$V_{DC\ OFF}$	DC step offset between any adjacent step	G_v = +16 to 0 dB	–	0.2	10.0	mV
		G_v = 0 to –71 dB	–	–	5	mV
	DC step offset between any step to mute	G_v = +16 to +1 dB	–	2	15	mV
		G_v = 0 to –71 dB	–	1	10	mV
Loudness control part						
L_B	maximum loudness boost	loudness **on**; referred to loudness **off**; boost is determined by external components; see Fig.5				
		f_i = 40 Hz	–	17	–	dB
		f_i = 10 kHz	–	4.5	–	dB
L_G	loudness control range		–12	–	+16	
Muting at power supply drop for OUTR and OUTS						
$V_{CC-DROP}$	supply drop for mute active		–	V_{CAP} – 0.7	–	V
Power-on reset; note 9						
$V_{RESET(STA)}$	start of reset voltage	increasing supply voltage	–	–	2.5	V
		decreasing supply voltage	4.2	5	5.8	V
$V_{RESET(END)}$	end of reset voltage	increasing supply voltage	5.2	6	6.8	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital part (I²C-bus pins); note 10						
V_{IH}	HIGH level input voltage		3	–	V_{CC}	V
V_{IL}	LOW level input voltage		−0.3	–	+1.5	V
I_{IH}	HIGH level input current		−10	–	+10	μA
I_{IL}	LOW level input current		−10	–	+10	μA
V_{OL}	LOW level output voltage	I_{IL} = 3 mA	–	–	+0.4	V

Notes to the characteristics

1. The oscillator is designed to operate together with MURATA resonator CSB503F58. Change of the resonator supplier is possible, but the resonator specification must be close to CSB503F58.
2. The internal SAP carrier level is determined by the composite input level and the level adjustment gain.
3. Frequency range 20 Hz to 20 kHz; select in to input line control; effects: linear stereo.
4. Crosstalk: $20 \log \frac{V_{bus(p-p)}}{V_{o(rms)}}$
5. The transmission contains:
   a) Total initialization with MAD and SAD for volume and 11 DATA words, see also definition of characteristics
   b) Clock frequency = 50 kHz
   c) Repetition burst rate = 400 Hz
   d) Maximum bus signal amplitude = 5 V (p-p).
6. The listed pin voltage corresponds with typical gain steps of +6 dB, +3 dB, 0 dB, −6 dB and −15 dB.
7. Attack time constant = $C_{AV} \times R_{att}$.
8. Decay time = $\frac{C_{AV} \times 0.76\ V \left(10^{\frac{-G_1}{20}} - 10^{\frac{-G_2}{20}} \right)}{I_{dec}}$

   Example: C_{AV} = 4.7 μF; I_{dec} = 2 μA; G_1 = −9 dB; G_2 = +6 dB → decay time results in 4.14 s.
9. When reset is active the GMU-bit (general mute) and the LMU-bit (LINE OUT mute) is set and the I²C-bus receiver is in the reset position.
10. The AC characteristics are in accordance with the I²C-bus specification. The maximum clock frequency is 100 kHz. Information about the I²C-bus can be found in the brochure *"The I²C-bus and how to use it"* (order number 9398 393 40011).

I²C-BUS PROTOCOL

I²C-bus format to read (slave transmits data)

S	SLAVE ADDRESS	R/$\overline{W}$	A	DATA	MA	DATA	P

Table 1 Explanation of I²C-bus format to read (slave transmits data)

NAME	DESCRIPTION
S	START condition; generated by the master
Standard SLAVE ADDRESS (MAD)	101 101 1
R/$\overline{W}$	1 (read); generated by the master
A	acknowledge; generated by the slave
DATA	slave transmits an 8-bit data word
MA	acknowledge; generated by the master
P	STOP condition; generated by the master

Table 2 Definition of the transmitted bytes after read condition

FUNCTION	BYTE	MSB							LSB
		D7	D6	D5	D4	D3	D2	D1	D0
Alignment read 1	ALR1	Y	SAPP	STP	A14	A13	A12	A11	A10
Alignment read 2	ALR2	Y	SAPP	STP	A24	A23	A22	A21	A20

Table 3 Function of the bits in Table 2

BITS	FUNCTION
STP	stereo pilot identification (stereo received = 1)
SAPP	SAP pilot identification (SAP received = 1)
A1X to A2X	stereo alignment read data
A1X	for wideband expander
A2X	for spectral expander
Y	indefinite

The master generates an acknowledge when it has received the first data word ALR1, then the slave transmits the next data word ALR2. Afterwards the master generates an acknowledge, then the slave begins transmitting the first data word ALR1 etc. until the master generates no acknowledge and transmits a STOP condition.

I²C-bus format to write (slave receives data)

S	SLAVE ADDRESS	R/$\overline{W}$	A	SUBADDRESS	A	DATA	A	P

Table 4 Explanation of I²C-bus format to write (slave receives data)

NAME	DESCRIPTION
S	START condition
Standard SLAVE ADDRESS (MAD)	101 101 1
R/$\overline{W}$	0 (write)
A	acknowledge; generated by the slave
SUBADDRESS (SAD)	see Table 5
DATA	see Table 6
P	STOP condition

If more than 1 byte of DATA is transmitted, then auto-increment is performed, starting from the transmitted subaddress and auto-increment of subaddress in accordance with the order of Table 5 is performed.

Table 5 Subaddress second byte after MAD

FUNCTION	REGISTER	MSB							LSB
		D7	D6	D5	D4	D3	D2	D1	D0
Volume right	VR	0	0	0	0	0	0	0	0
Volume left	VL	0	0	0	0	0	0	0	1
Control 1 (note 1)	CON1	0	0	0	0	0	1	0	1
Control 2	CON2	0	0	0	0	0	1	1	0
Control 3	CON3	0	0	0	0	0	1	1	1
Alignment 1	ALI1	0	0	0	0	1	0	0	0
Alignment 2	ALI2	0	0	0	0	1	0	0	1
Alignment 3	ALI3	0	0	0	0	1	0	1	0

Note

1. In auto-increment mode it is necessary to insert 3 dummy data words between volume left and control 1.

Table 6 Definition of third byte, third byte after MAD and SAD

FUNCTION	REGISTER	MSB							LSB
		D7	D6	D5	D4	D3	D2	D1	D0
Volume right	VR	0	VR6	VR5	VR4	VR3	VR2	VR1	VR0
Volume left	VL	0	VL6	VL5	VL4	VL3	VL2	VL1	VL0
Control 1	CON1	GMU	AVLON	LOFF	CCD	0	SC2	SC1	SC0
Control 2	CON2	SAP	STEREO	TZCM	1	LMU	EF2	EF1	EF0
Control 3	CON3	0	0	0	0	L3	L2	L1	L0
Alignment 1	ALI1	0	0	0	A14	A13	A12	A11	A10
Alignment 2	ALI2	STS	0	0	A24	A23	A22	A21	A20
Alignment 3	ALI3	ADJ	AT1	AT2	0	1	TC2	TC1	TC0

Table 7 Function of the bits in Table 6

BITS	FUNCTION
VR0 to VR6	volume control right
VL0 to VL6	volume control left
GMU	mute control for all outputs (generate mute)
AVLON	AVL **on/off**
CCD	increased AVL decay current **on/off**
LOFF	switch loudness **on/off**
SC0 to SC2	selection between line in and line out
STEREO, SAP	mode selection for line out
TZCM	zero cross mode in mute operation (right and left output stage)
LMU	mute control for line out
EF0 to EF2	selection between mono, stereo linear, spatial stereo and pseudo mode
L0 to L3	input level adjustment
ADJ	stereo adjustment **on/off**
A1X to A2X	stereo alignment data
A1X	for wideband expander
A2X	for spectral expander
AT1 and AT2	attack time at AVL
TC0 to TC2	timing current alignment data
STS	stereo level switch

Table 8 Volume setting

FUNCTION G_v (dB)	DATA						
	V6	V5	V4	V3	V2	V1	V0
16	1	1	1	1	1	1	1
15	1	1	1	1	1	1	0
14	1	1	1	1	1	0	1
13	1	1	1	1	1	0	0
12	1	1	1	1	0	1	1
11	1	1	1	1	0	1	0
10	1	1	1	1	0	0	1
9	1	1	1	1	0	0	0
8	1	1	1	0	1	1	1
7	1	1	1	0	1	1	0
6	1	1	1	0	1	0	1
5	1	1	1	0	1	0	0
4	1	1	1	0	0	1	1
3	1	1	1	0	0	1	0
2	1	1	1	0	0	0	1
1	1	1	1	0	0	0	0

FUNCTION G_v (dB)	DATA						
	V6	V5	V4	V3	V2	V1	V0
0	1	1	0	1	1	1	1
–1	1	1	0	1	1	1	0
–2	1	1	0	1	1	0	1
–3	1	1	0	1	1	0	0
–4	1	1	0	1	0	1	1
–5	1	1	0	1	0	1	0
–6	1	1	0	1	0	0	1
–7	1	1	0	1	0	0	0
–8	1	1	0	0	1	1	1
–9	1	1	0	0	1	1	0
–10	1	1	0	0	1	0	1
–11	1	1	0	0	1	0	0
–12	1	1	0	0	0	1	1
–13	1	1	0	0	0	1	0
–14	1	1	0	0	0	0	1
–15	1	1	0	0	0	0	0
–16	1	0	1	1	1	1	1
–17	1	0	1	1	1	1	0
–18	1	0	1	1	1	0	1
–19	1	0	1	1	1	0	0
–20	1	0	1	1	0	1	1
–21	1	0	1	1	0	1	0
–22	1	0	1	1	0	0	1
–23	1	0	1	1	0	0	0
–24	1	0	1	0	1	1	1
–25	1	0	1	0	1	1	0
–26	1	0	1	0	1	0	1
–27	1	0	1	0	1	0	0
–28	1	0	1	0	0	1	1
–29	1	0	1	0	0	1	0
–30	1	0	1	0	0	0	1
–31	1	0	1	0	0	0	0
–32	1	0	0	1	1	1	1
–33	1	0	0	1	1	1	0
–34	1	0	0	1	1	0	1
–35	1	0	0	1	1	0	0
–36	1	0	0	1	0	1	1
–37	1	0	0	1	0	1	0
–38	1	0	0	1	0	0	1

FUNCTION G_v (dB)	DATA						
	V6	V5	V4	V3	V2	V1	V0
–39	1	0	0	1	0	0	0
–40	1	0	0	0	1	1	1
–41	1	0	0	0	1	1	0
–42	1	0	0	0	1	0	1
–43	1	0	0	0	1	0	0
–44	1	0	0	0	0	1	1
–45	1	0	0	0	0	1	0
–46	1	0	0	0	0	0	1
–47	1	0	0	0	0	0	0
–48	0	1	1	1	1	1	1
–49	0	1	1	1	1	1	0
–50	0	1	1	1	1	0	1
–51	0	1	1	1	1	0	0
–52	0	1	1	1	0	1	1
–53	0	1	1	1	0	1	0
–54	0	1	1	1	0	0	1
–55	0	1	1	1	0	0	0
–56	0	1	1	0	1	1	1
–57	0	1	1	0	1	1	0
–58	0	1	1	0	1	0	1
–59	0	1	1	0	1	0	0
–60	0	1	1	0	0	1	1
–61	0	1	1	0	0	1	0
–62	0	1	1	0	0	0	1
–63	0	1	1	0	0	0	0
–64	0	1	0	1	1	1	1
–65	0	1	0	1	1	1	0
–66	0	1	0	1	1	0	1
–67	0	1	0	1	1	0	0
–68	0	1	0	1	0	1	1
–69	0	1	0	1	0	1	0
–70	0	1	0	1	0	0	1
–71	0	1	0	1	0	0	0
Mute	0	1	0	0	1	1	1

Table 9 Loudness setting

CHARACTERISTIC	DATA LOFF
With loudness	0
Linear	1

Table 10 Effects setting

FUNCTION	DATA		
	EF2	EF1	EF0
Stereo linear **on**	0	0	0
Pseudo **on**	0	0	1
Spatial stereo; 30% anti-phase crosstalk	0	1	0
Spatial stereo; 50% anti-phase crosstalk	0	1	1
Forced mono	1	1	1

Table 11 Selector setting

FUNCTION(1)	DATA		
	SC2	SC1	SC0
Inputs LOR and LOL	0	0	0
Inputs LOR and LOR	0	0	1
Inputs LOL and LOL	0	1	0
Inputs LOL and LOR	0	1	1
Inputs LIR and LIL	1	0	0
Inputs LIR and LIR	1	0	1
Inputs LIL and LIL	1	1	0
Inputs LIL and LIR	1	1	1

Note

1. Input connected to outputs SOR and SOL.

Table 12 Switch setting at line out

LINE OUT SIGNALS AT		DATA TRANSMISSION STATUS INTERNAL SWITCH, READABLE BITS: STP, SAPP	SETTING BITS	
LOL	LOR		STEREO	SAP
SAP	SAP	SAP received	1	1
Mute	mute	no SAP received	1	1
Left	right	STEREO received	1	0
Mono	mono	no STEREO received	1	0
Mono	SAP	SAP received	0	1
Mono	mute	no SAP received	0	1
Mono	mono	independent	0	0

Table 13 Zero cross detection setting

FUNCTION	DATA TZCM
Direct mute control	0
Mute control delayed until the next zero crossing	1

Table 14 Mute setting

FUNCTION	DATA GMU	FUNCTION	DATA LMU
Forced mute at OUTR, OUTL and OUTS	1	forced mute at LOR and LOL	1
Audio processor controlled outputs	0	stereo processor controlled outputs	0

Table 15 AVL attack time

FUNCTION	DATA	
	AT1	AT2
R_{att} = 420 Ω	0	0
R_{att} = 730 Ω	1	0
R_{att} = 1200 Ω	0	1
R_{att} = 2100 Ω	1	1

Table 16 ADJ bit setting

FUNCTION	DATA
Stereo decoder operation mode	0
Auto adjustment of channel separation	1

Table 17 AVLON bit setting

FUNCTION	DATA
Automatic volume control **off**	0
Automatic volume control **on**	1

Table 18 CCD bit setting

FUNCTION	DATA
Load current for normal AVL decay time	0
Increased load current	1

Table 19 STS bit setting (pilot threshold stereo **on**)

FUNCTION	DATA
$ST_{on} \leq 35$ mV	1
$ST_{on} \leq 30$ mV	0

Table 20 Timing current setting

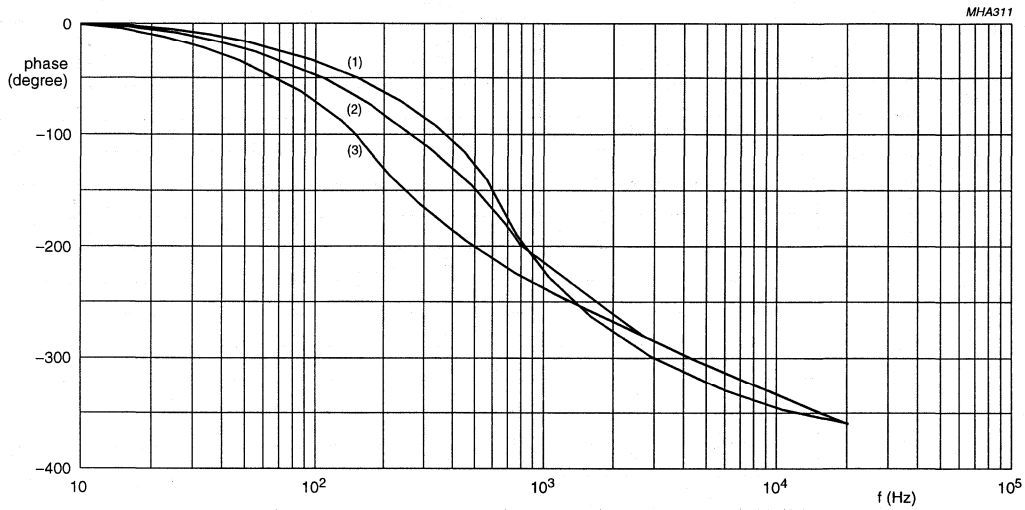
FUNCTION I_S RANGE	DATA		
	TC2	TC1	TC0
+30%	1	0	0
+20%	1	0	1
+10%	1	1	0
Nominal	0	1	1
−10%	0	1	0
−20%	0	0	1
−30%	0	0	0

Table 21 Level adjust setting

G_L (dB)	DATA			
	L3	L2	L1	L0
+4.0	1	1	1	1
+3.5	1	1	1	0
+3.0	1	1	0	1
+2.5	1	1	0	0
+2.0	1	0	1	1
+1.5	1	0	1	0
+1.0	1	0	0	1
+0.5	1	0	0	0
0.0	0	1	1	1
−0.5	0	1	1	0
−1.0	0	1	0	1
−1.5	0	1	0	0
−2.0	0	0	1	1
−2.5	0	0	1	0
−3.0	0	0	0	1
−3.5	0	0	0	0

Table 22 Alignment data for expander in read register ALR1 and ALR2 and in write register ALI1 and ALI2

FUNCTION	DATA				
	D4 AX4	D3 AX3	D2 AX2	D1 AX1	D0 AX0
Gain increase	1	1	1	1	1
	1	1	1	1	0
	1	1	1	0	1
	1	1	1	0	0
	1	1	0	1	1
	1	1	0	1	0
	1	1	0	0	1
	1	1	0	0	0
	1	0	1	1	1
	1	0	1	1	0
	1	0	1	0	1
	1	0	1	0	0
	1	0	0	1	1
	1	0	0	1	0
	1	0	0	0	1
Nominal gain	1	0	0	0	0
	0	1	1	1	1
Gain decrease	0	1	1	1	0
	0	1	1	0	1
	0	1	1	0	0
	0	1	0	1	1
	0	1	0	1	0
	0	1	0	0	1
	0	1	0	0	0
	0	0	1	1	1
	0	0	1	1	0
	0	0	1	0	1
	0	0	1	0	0
	0	0	0	1	1
	0	0	0	1	0
	0	0	0	0	1
	0	0	0	0	0

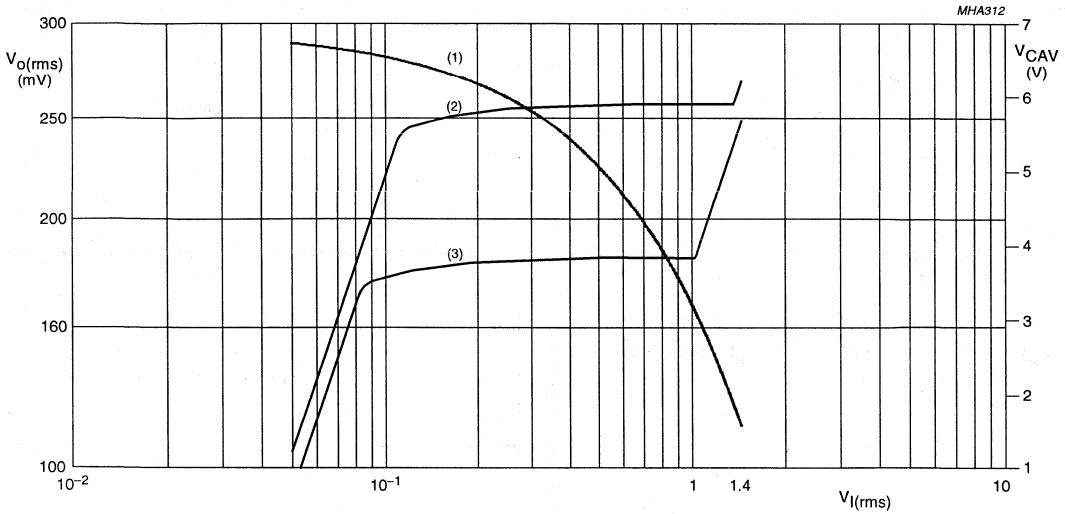


(1) see Table 23.
(2) see Table 23.
(3) see Table 23.

Fig.3 Pseudo (phase in degrees) as a function of frequency (left output).

Table 23 Explanation of curves in Fig.3

CURVE	CAPACITANCE AT PIN 38 (nF)	CAPACITANCE AT PIN 37 (nF)	EFFECT
1	15	15	normal
2	5.6	47	intensified
3	5.6	68	more intensified



(1) V_{CAV} AVL measured at pin EOL/EOR.

(2) $V_{o\ max(rms)}$ Y_1 axis output level in AVL operation with typically 200 mV.

(3) $V_{o\ min(rms)}$ Y_2 axis V_{CAV} DC voltage at pin C_{AV} corresponds with typical gain steps in range of +6 to −15 dB.

Fig.4 Automatic level control diagram.

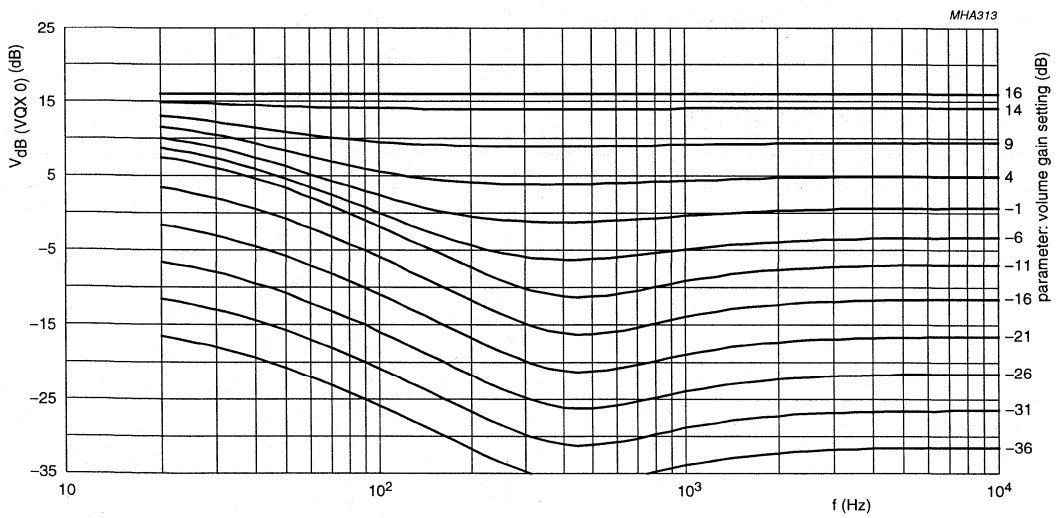


Fig.5 Volume control with loudness (including low roll-off frequency).

INTERNAL PIN CONFIGURATIONS

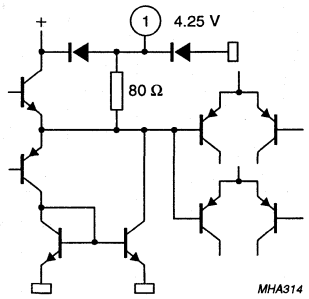


Fig.6 Pin 1: OUTL; pin 9: SOL; pin 34: SOR; pin 42; OUTR.

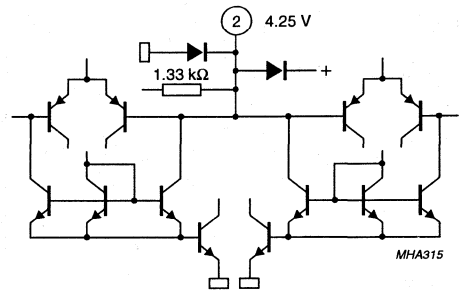


Fig.7 Pin 2: LDL; pin 41: LDR.

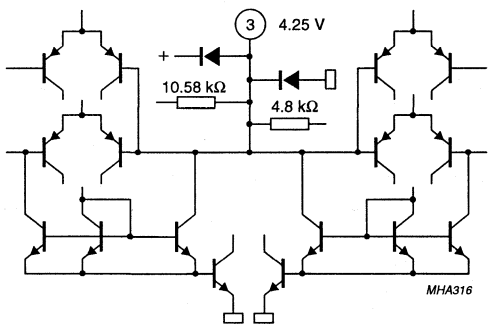


Fig.8 Pin 3: VIL; pin 40: VIR.

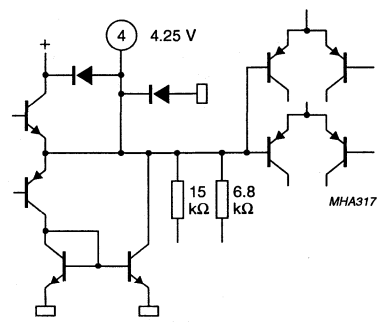


Fig.9 Pin 4: EOL; pin 39: EOR.

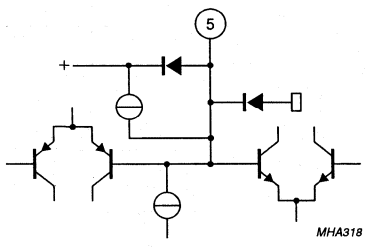


Fig.10 Pin 5: C_{AV}.

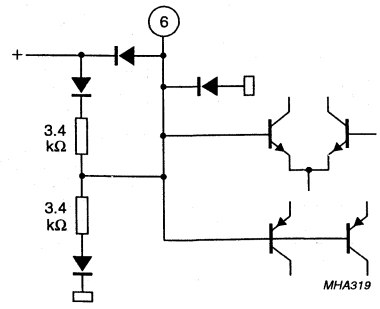


Fig.11 Pin 6: V_{ref}.

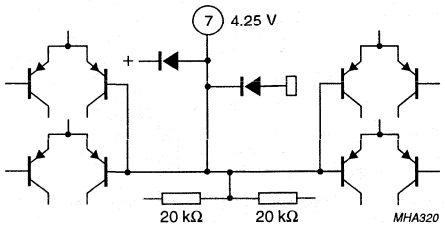


Fig.12 Pin 7: LIL; pin 36: LIR.

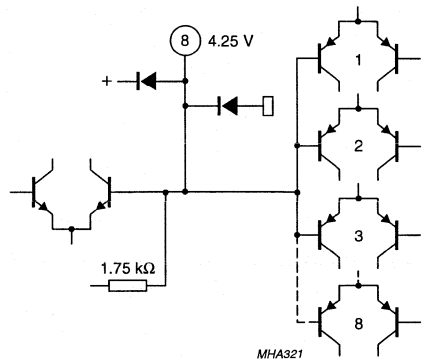


Fig.13 Pin 8: AVL pin 35: AVR.

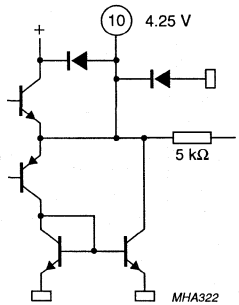


Fig.14 Pin 10: LOL; pin 33: LOR.

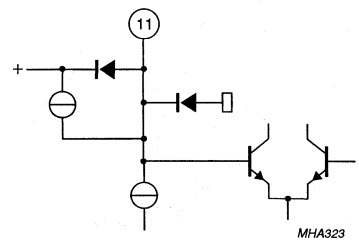


Fig.15 Pin 11: C_{TW}; pin 12: C_{TS}.

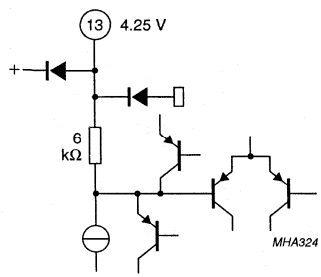


Fig.16 Pin 13: C_W; pin 14: C_S.

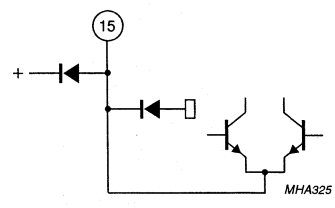


Fig.17 Pin 15: VEO.

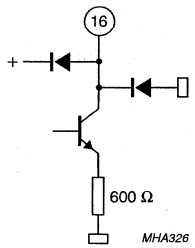


Fig.18 Pin 16: VEI.

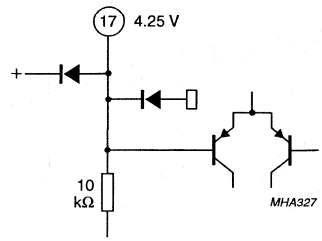


Fig.19 Pin 17: C_{NR}.

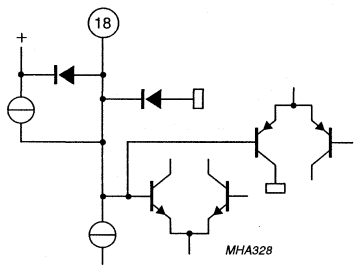


Fig.20 Pin 18: C_M.

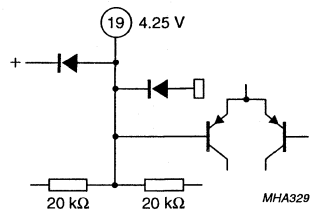


Fig.21 Pin 19: C_{DEC}.

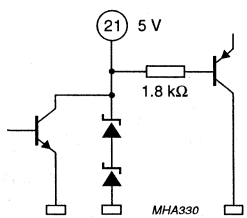


Fig.22 Pin 21: SDA.

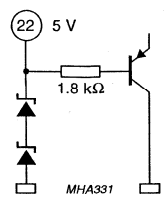


Fig.23 Pin 22: SCL.

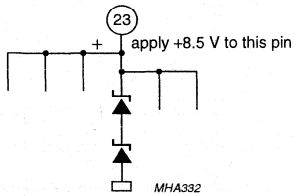


Fig.24 Pin 23: V_{CC}.

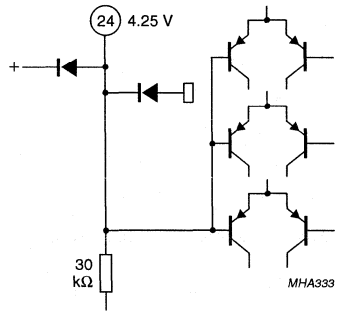


Fig.25 Pin 24: COMP.

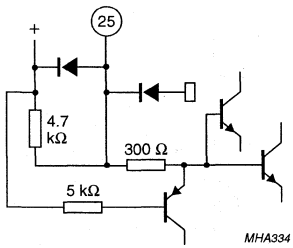


Fig.26 Pin 25: V_{CAP}.

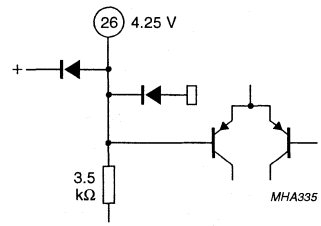


Fig.27 Pin 26: C_{P1}.

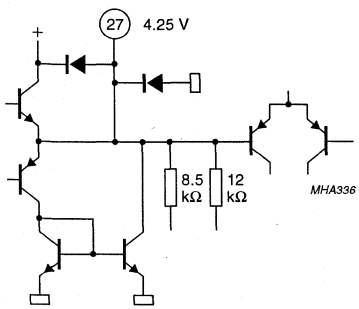


Fig.28 Pin 27: C_{P2}.

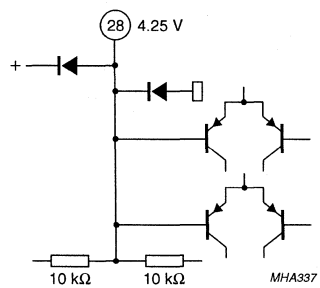


Fig.29 Pin 28: C_{PH}.

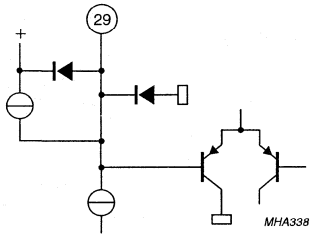


Fig.30 Pin 29: C_{ADJ}.

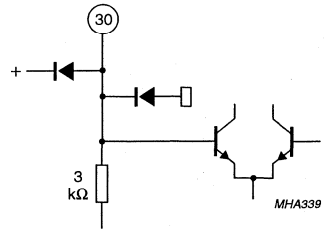


Fig.31 Pin 30: CER.

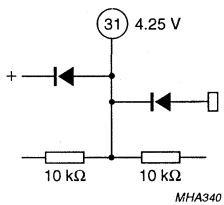


Fig.32 Pin 31: C_{MO}; pin 32: C_{SS}.

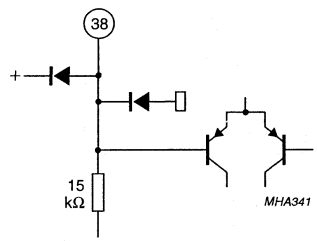


Fig.33 Pin 38: C_{PS1}; pin 37: C_{PS2}.

I²C-bus controlled BTSC stereo / SAP decoder and audio processor

TDA9855

FEATURES

- Quasi alignment-free BTSC stereo decoder due to auto adjustment of channel separation via I²C-bus
- High integration level with automatically tuned integrated filters
- Input level adjustment I²C-bus controlled
- Alignment-free SAP processing
- dbx noise reduction circuit
- Audio processor
  - Selector for internal and external signals (line in)
  - Automatic volume level control
  - Subwoofer or surround output with separate volume control
  - Volume control
  - Special loudness characteristic automatically controlled in combination with volume setting
  - Bass and treble control
  - Audio signal zero crossing detection between any volume step switching
- Mute control at audio signal zero crossing
- I²C-bus transceiver.

GENERAL DESCRIPTION

The TDA9855 is a bipolar-integrated BTSC stereo / SAP decoder with hi-fi audio processor (I²C-bus controlled) for application in TV sets.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA9855	52	SHDIL	plastic	SOT247-1
TDA9855WP	68	PLCC	plastic	SOT188-2

A license is required for the use of this product. For further information, please contact

THAT Corporation
Licensing Operations
734 Forest St.
Marlborough, MA 01752
USA

Tel: (508) 229-2500
Fax: (508) 229-2590

THAT Corporation
Tokyo Office
405 Palm House, 1-20-2 Honmachi
Shibuya-ku, Tokyo 151
Japan

Tel: (03) 3378-0915
Fax: (03) 3374-5191

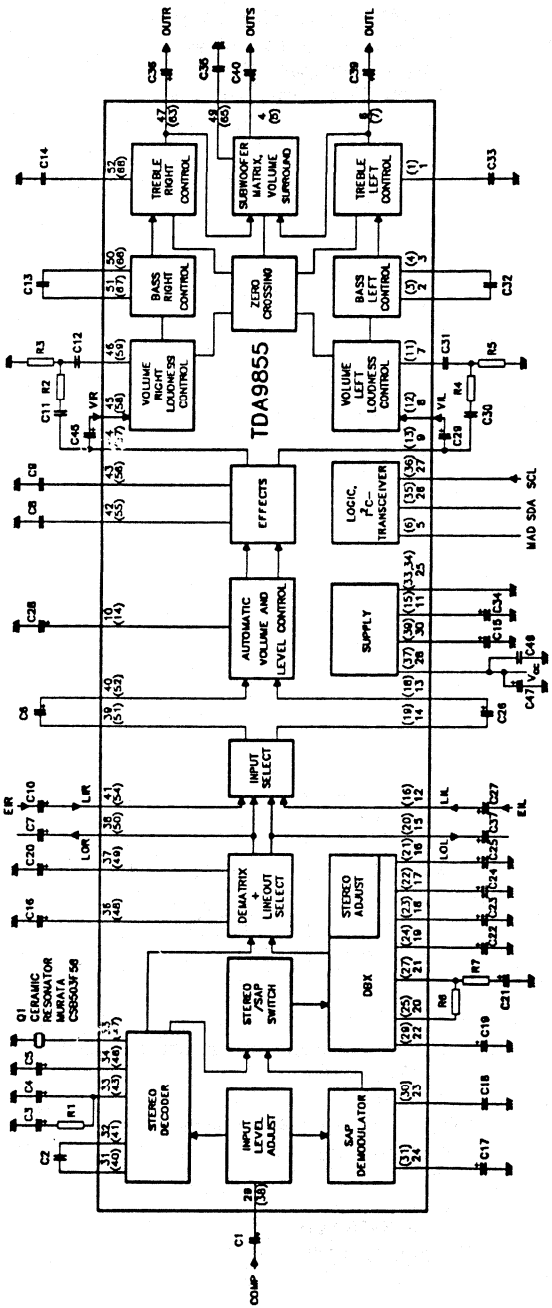


Fig.1 Block, application and test diagram (PLCC pinning in parenthesis).

COMPONENT LIST

elco ±20%; foil or ceramic ±10%; resistors ±5% unless otherwise specified.

COMPONENT	VALUE	TYPE	REMARK
C1	10 µF	elco	63 V
C2	470 nF	foil	
C3	4.7 µF	elco	63 V
C4	220 nF	foil	
C5	10 µF	elco	63 V; I_{leak} < 1.5 µA
C6	2.2 µF	elco	16 V
C7	4.7 µF	elco	16 V
C8	15 nF	foil	±5%
C9	15 nF	foil	±5%
C10	2.2 µF	elco	63 V
C11	8.2 nF	foil or ceramic	±5% SMD 2220/1206
C12	150 nF	foil	±5%
C13	33 nF	foil	±5%
C14	5.6 nF	foil or ceramic	±5% SMD 2220/1206
C15	100 µF	elco	16 V
C16	4.7 µF	elco	63 V
C17	4.7 µF	elco	63 V
C18	100 nF	foil	
C19	10 µF	elco	63
C20	4.7 µF	elco	63
C21	47 nF	foil	±5%
C22	1 µF	elco	63 V
C23	1 µF	elco	63 V
C24	10 µF	elco	63 V ±10%
C25	10 µF	elco	63 V ±10%
C26	2.2 µF	elco	16 V
C27	2.2 µF	elco	63 V
C28	4.7 µF	elco	63 V ±10%
C29	2.2 µF	elco	16 V
C30	8.2 nF	foil or ceramic	±5% SMD 2220/1206
C31	150 nF	foil	±5%
C32	33 nF	foil	±5%
C33	5.6 nF	foil or ceramic	±5% SMD 2220/1206
C34	100 µF	elco	16 V
C35	150 nF	foil	±5%
C36	4.7 µF	elco	16 V
C37	4.7 µF	elco	16 V
C39	4.7 µF	elco	16 V
C40	4.7 µF	elco	16 V
C45	2.2 µF	elco	16 V
C47	220 µF	elco	25 V
C49	100 nF	foil or ceramic	SMD 1206

COMPONENT	VALUE	REMARK
R1	2.2 kΩ	
R2	20 kΩ	
R3	2.2 kΩ	
R4	20 kΩ	
R5	2.2 kΩ	
R6	8.2 kΩ	±2%
R7	160 Ω	±2%
Q1	503.5 kHz	MURATA CSB503F58

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		8.0	8.5	9.0	V
I_{CC}	supply current		50	75	95	mA
V_{comp}	input signal (RMS value)	100% modulation L + R; f = 300 Hz	–	250	–	mV
V_{LOR}, V_{LOL}	output signal (RMS value)		–	500	–	mV
G_{LA}	input level adjustment control range		–3.5	–	+4.0	dB
α_{st}	stereo channel separation	f_L = 300 Hz; f_R = 3 kHz	25	35	–	dB
$THD_{L,R}$	total harmonic distortion	f = 1 kHz	–	0.2	–	%
$V_{I,O}$	signal handling (RMS value)	THD < 0.5%	2	–	–	V
AVL	control range		–15	–	+6	dB
G_c	volume control range		–71	–	+16	dB
L_B	maximum loudness boost	f = 40 Hz	–	17	–	dB
G_b	bass control range	f = 40 Hz	–12	–	+16.5	dB
G_t	treble control range	f = 15 kHz	–12	–	+12	dB
G_v	subwoofer control range	f = 40 Hz	–14	–	+14	dB
S/N	signal-to-noise ratio	line out (mono); Vo = 0.5 V (RMS)				
	CCIR noise weighting filter (peak value)		–	60	–	dB
	DIN noise weighting filter (RMS value)		–	73	–	dBA
S/N	signal-to-noise ratio	audio section; Vo = 2 V (RMS); gain = 0 dB				
	CCIR noise weighting filter (peak value)		–	94	–	dB
	DIN noise weighting filter (RMS value)		–	107	–	dBA

PINNING

SYMBOL	SOT188	SOT247	DESCRIPTION
TL	1	1	treble control capacitor, left channel
n.c.	2	–	not connected
B1L	3	2	bass control capacitor, left channel
B2L	4	3	bass control capacitor, left channel
OUTS	5	4	output subwoofer or output surround sound
MAD	6	5	programmable address bit (module address)
OUTL	7	6	output, left channel
n.c.	8 to 10	–	not connected
LDL	11	7	input loudness, left channel
VIL	12	8	input volume control, left channel
EOL	13	9	output effects, left channel
CAV	14	10	automatic volume control capacitor
V_{REF}	15	11	reference voltage $0.5V_{CC}$
LIL	16	12	line input, left channel
n.c.	17	–	not connected
AVL	18	13	input automatic volume control, left channel
SOL	19	14	output selector, left channel
LOL	20	15	line output, left channel
TW	21	16	capacitor timing wideband for dbx
TS	22	17	capacitor timing spect for dbx
CW	23	18	capacitor wideband f x
CS	24	19	capacitor spectral for dbx
VEO	25	20	variable emphasis out for dbx
n.c.	26	–	not connected
VEI	27	21	variable emphasis in for dbx
n.c.	28	–	not connected
CNR	29	22	capacitor noise reduction for dbx
CM	30	23	capacitor mute for SAP
CD	31	24	capacitor DC decoupling for SAP
n.c.	32	–	not connected
GND	33	–	analog ground
GND	34	–	digital ground
GND	–	25	common ground
SDA	35	26	serial data input/output
SCL	36	27	serial clock input
Vcc	37	28	supply voltage
COMP	38	29	input composite signal
VCAP	39	30	capacitor for electronic filtering of supply
CP1	40	31	capacitor for pilot detector
CP2	41	32	capacitor for pilot detector
n.c.	42	–	not connected
CPH	43	33	capacitor for phase detector
n.c.	44, 45	–	not connected

SYMBOL	SOT188	SOT247	DESCRIPTION
CA	46	34	capacitor for filter adjust
CER	47	35	ceramic resonator
CMO	48	36	capacitor DC decoupling mono
CSS	49	37	capacitor DC decoupling stereo/SAP
LOR	50	38	line output, right channel
SOR	51	39	output selector, right channel
AVR	52	40	input automatic volume control, right channel
n.c.	53	–	not connected
LIR	54	41	line input, right channel
PS2	55	42	capacitor 2 pseudo function
PS1	56	43	capacitor 1 pseudo function
EOR	57	44	output effects, right channel
VIR	58	45	input volume control, right channel
LDR	59	46	input loudness, right channel
n.c.	60 to 62	–	not connected
OUTR	63	47	output, right channel
n.c.	64	48	not connected
SW	65	49	filter capacitor for subwoofer
B2R	66	50	bass control capacitor, right channel
B1R	67	51	bass control capacitor, right channel
TR	68	52	treble control capacitor

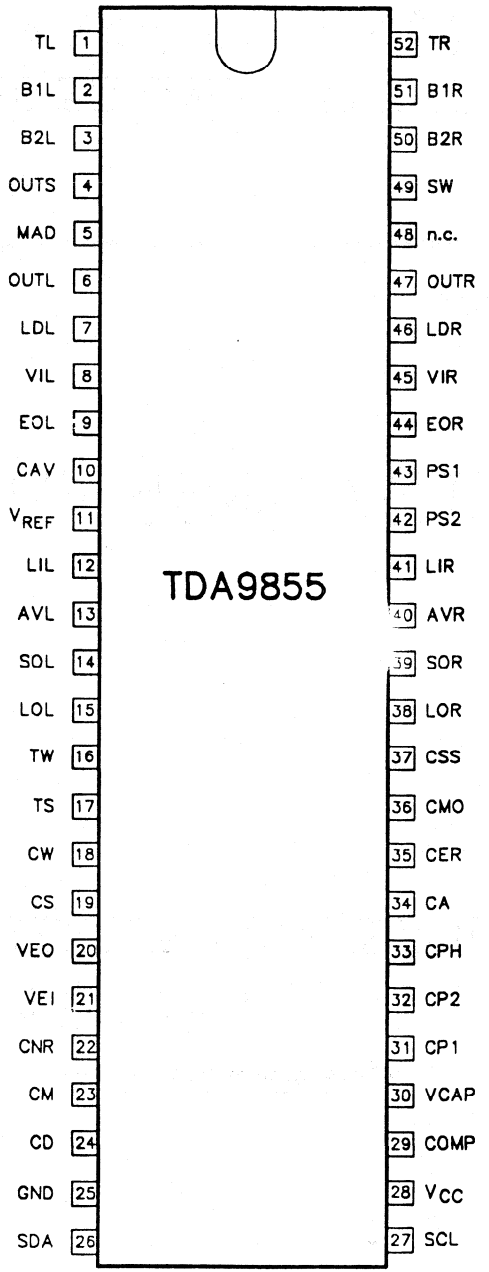


Fig.2 Pin configuration for SHRDIL-version.

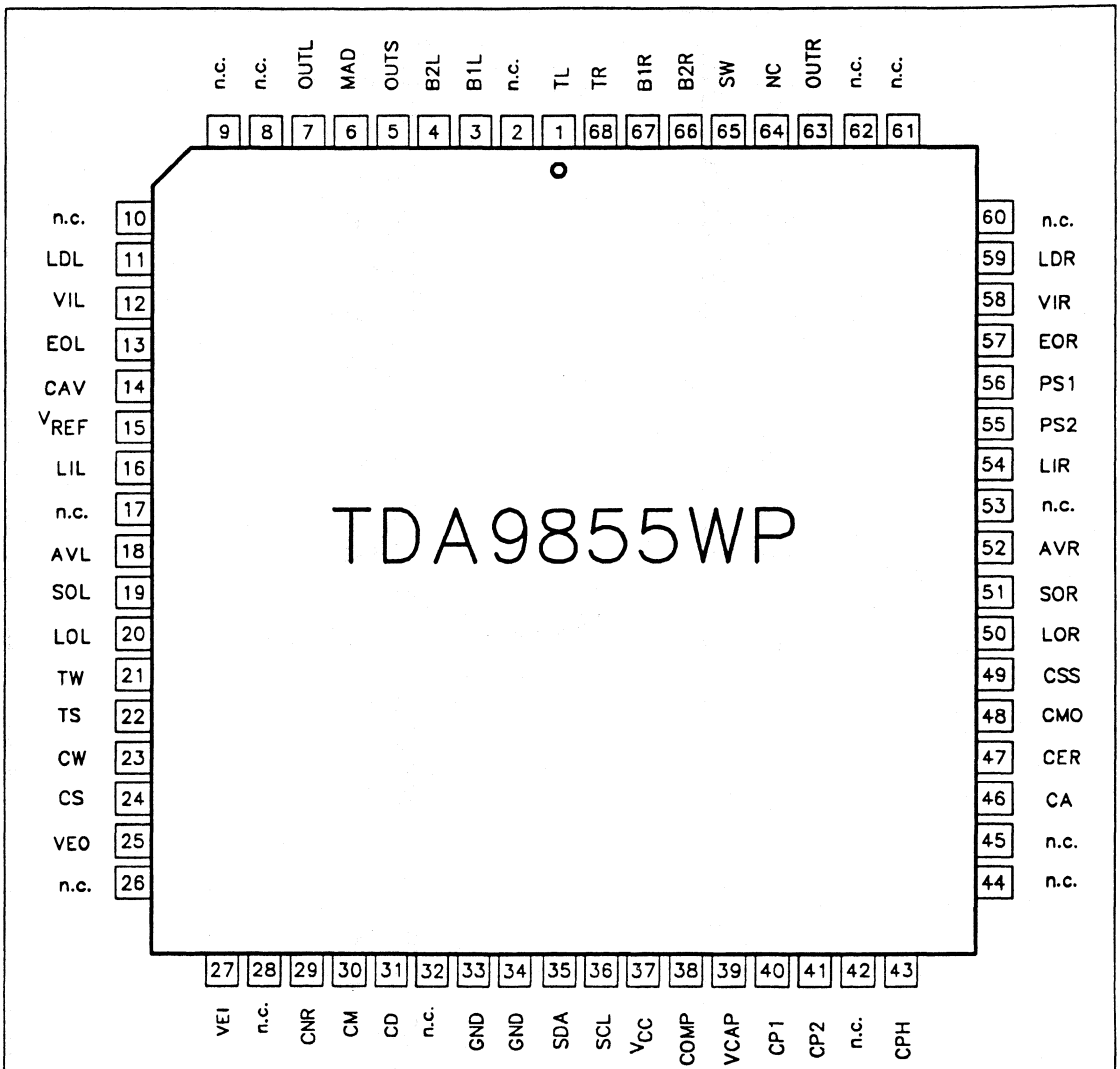


Fig.3 Pin configuration for PLCC-version.

FUNCTIONAL DESCRIPTION

Decoder

Input level adjustment

The composite input signal is fed to the input level adjustment stage. In order to compensate tolerances of the FM demodulator which supplied the composite input signal, the TDA9855 provides an input level adjustment stage. The control range is between –3.5 dB and +4.0 dB in steps of 0.5 dB. The subaddress control 3 of Tables 2 and 3 and the level adjust setting of Table 16 allows an optimal signal adjustment during the set alignment in the production line. This value has to be stored in a none volatile memory. The maximum input signal voltage is 2 V (RMS).

Stereo decoder

The output signal of the level adjustment stage is coupled to a low-pass filter which suppresses the baseband noise above 125 kHz. The composite signal is then fed into a pilot detector/pilot cancellation circuit and into the MPX demodulator. The main L + R signal passes a 75 µs fixed de-emphasis filter and is fed into the dematrix circuit. The decoded subsignal L – R is sent to the stereo/SAP switch. To generate the pilot signal the stereo demodulator uses a PLL circuit including a ceramic resonator. The stereo channel separation can be adjusted by an automatic procedure or manually. A detailed description of this alignment is provided in the ADJUSTMENT PROCEDURE. The stereo identification can be read by the I²C-bus (see Table 1). Two different pilot thresholds can be selected via I²C-bus (see Table 18).

SAP demodulator

The composite signal is fed from the output of the input level adjustment stage to the SAP demodulator circuit through a $5f_H$ band-pass filter. The demodulator level is automatically controlled. The SAP demodulator includes internal noise and field strength detectors that mute the SAP output in case of insufficient signal conditions. The SAP identification signal can be read by the I²C-bus (see Table 1).

Switch

The stereo/SAP switch feeds either the L – R signal or the SAP demodulator output signal via the internal dbx noise reduction circuit to the dematrix/line out select circuit. Table 15 shows the different switch modes provided at the output pins LOR and LOL.

dbx decoder

The dbx circuit includes all blocks required for the noise reduction system according to the BTSC system specification. The output signal is fed through a 73 µs fixed de-emphasis circuit to the dematrix block.

Integrated filters

The filter functions necessary for stereo and SAP demodulation and part of the dbx filter circuits are provided on chip using transconductor circuits. The required filter accuracy is attained by an automatic filter alignment circuit.

Audio processor

Selector

The selector allows selecting either the internal line out signals LOR or LOL (dematrix out) or the external line in signals LIR and LIL and combines the left and right signals in several modes (see Table 8). The input signal capability of the line inputs (LIR/LIL) is 2 V (RMS). The output of the selector is AC coupled to the automatic volume level control circuit via pins SOR/SOL and AVR/AVL to avoid offset voltages.

Automatic volume level control

The automatic volume level stage controls its output voltage to a constant level of typically 200 mV (RMS) from an input voltage range between 0.1 and 1.1 V (RMS). The circuit adjusts variations in modulation during broadcasting and due to changes in the programme material. The function can be switched off. To avoid audible 'plops' during the permanent operation of the AVL circuit a soft blending scheme has been applied between the different gain stages. A capacitor at pin CAV determines the attack and decay time constants. In addition the ratio of attack and decay time can be changed via I²C-bus (see notes 3 and 4 of the CHARACTERISTICS).

Effects

The audio processor section offers the following mode selections: linear stereo, pseudo stereo, spatial stereo and forced mono. The spatial mode provides an antiphase crosstalk of 30% or 52% (switchable via I²C-bus; see Table 13).

Volume/loudness

The volume control range is between +16 dB and –71 dB in steps of 1 dB and ends with a mute step (see Table 4). Balance control is achieved by the independent volume control of each channel. The volume control blocks operate in combination with the loudness control. The filter is linear when maximum gain for volume control is selected. The filter characteristic changes automatically over a range of 28 dB down to a setting of –12 dB. At –12 dB volume control the maximum loudness boost is obtained. The filter characteristic is

determined by external components. The proposed application provides a maximum boost of 17 dB for bass and 4.5 dB for treble. The loudness may be switched on or off via the I²C-bus control (see Table 10). The left and right volume control stages include two independent zero crossing detectors. In the zero cross mode a change in volume is automatically activated but not executed. The execution is enabled at the next zero crossing of the signal. If a new volume step is activated before the previous one has been processed, the previous value will be executed first, and then the new value will be activated. If no zero crossing occurs the next volume transmission will enforce the last activated volume setting. The zero crossing mode is realized between adjoining steps and between any steps, but not from any step to mute. In this case the GMU bit is needed to use. In case of need to mute only one channel, two steps are necessary. The first step is a transmission from any steps to –71 dB and the second is –71 dB step to mute. The step of –71 dB to mute has no zero crossing but it is not relevant. This procedure has to be provided by software.

Bass control

A single external 33 nF capacitor for each channel in combination with a linear operational amplifier and internal resistors provides a bass control range of +16.5 dB to –12 dB in steps of 1.5 dB at low frequencies (40 Hz). Internally the basic step width is 3 dB, with intermediate steps are obtained by a toggle function that provides additional an 1.5 dB boost or attenuation (see Table 5). Please note that both loudness and bass control together result in a maximum bass boost of 34.5 dB for low volume steps.

Treble control

The adjustable range of the treble control stage is between –12 dB and +12 dB in steps of 3 dB. The filter characteristic is determined by an external 5.6 nF capacitor for each channel. The logic circuitry is arranged in a way that the same data words (HEX 06 to 16) can be used for both tone controls if a bass control range from –12 dB to +12 dB and a treble control range from –12 dB to +12 dB with 3 dB steps are used (see Tables 5 and 6).

Subwoofer; surround sound control

The subwoofer or the surround mode can be activated with the control bit SUR (see Table 3). A low bit provides an output signal (L + R)/2 in subwoofer mode, a high bit selects surround mode and provides an output signal (L – R)/2. The signal is fed through a volume control stage with a range between +14 dB and –14 dB in 2 dB steps on top of the main channel control to the output pin OUTS. The last setting is the mute position (see Table 7). The capacitor C35 at pin SW provides a 230 Hz low-pass filter in subwoofer mode. In surround mode this capacitor should be disconnected. If balance is not in mid position the selected left and right output levels will be combined.

Mute

The mute function can be activated independently with the last step of volume or subwoofer/surround control at the left, right or center output. By setting the general mute bit GMU via the I²C-bus all audio part outputs are muted. All channels include an independent zero cross detector. The zero crossing mute feature can be selected via bit TZCM:
TZCM = 0:
forced mute with direct execution,
TZCM = 1:
execution in time with signal zero crossing.
In the zero cross mode a change of the GMU bit is activated but not executed. The execution is enabled at the next zero crossing of the signal. To avoid a large delay of mute switching, when very low frequencies are processed, or the output signal amplitude is lower than the DC offset voltage, the following I²C-bus transmissions are needed:
- a first transmission for mute execution
- a second transmission about 100 ms later, which must switch the zero crossing mode to forced mute (TZCM = 0)
- a third transmission to reactivate the zero crossing mode (TZCM = 1). This transmission can take place immediately, but must follow before the next mute execution.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		0	9.5	V
T_{amb}	operating ambient temperature		−20	+70	°C
T_{stg}	storage temperature		−65	+150	°C
V_{es}	electrostatic handling	note 1			
V_n	voltage at all other pins to pin GND		0	V_{CC}	V

Note to the limiting values

1. Human body model: C = 100 pF; R = 1.5 kΩ; V = 2 kV; charge device model: C = 200 pF; R = 0 Ω; V = 300 V.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j-a}$	from junction to ambient in free air	
	SOT247AH	43 K/W
	SOT188CG	38 K/W

Requirements for the composite input signal to ensure proper system performance.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$COMP_{L+R}$	composite input level for 100% modulation L + R (25 kHz deviation), RMS, f = 300 Hz	measured at COMP	162	250	363	mV
ΔCOMP	composite input level spreading under operating conditions	T_{amb} = −20 to +70 °C; aging; power supply influence	−0.5	−	+0.5	dB
Z_O	output impedance	note 1	−	low-ohmic	5	kΩ
$f_{-2\ dB}$	roll-off frequencies (25 kHz deviation L + R)	low frequency (−2 dB)	−	−	5	Hz
		high frequency (−2 dB)	100	−	−	kHz
THD	total harmonic distortion L + R; f = 1 kHz	25 kHz deviation	−	−	0.5	%
		125 kHz deviation; note 2	−	−	1.5	%
S/N	signal-to-noise ratio L + R/noise	CCIR 468-2 weighted quasi peak; L + R; 25 kHz deviation; f = 1 kHz; 75 μs de-emphasis				
		critical picture modulation	44	−	−	dB
		with sync only	54	−	−	dB
α_{SB}	side band suppression mono into unmodulated SAP carrier; SAP carrier/side band	mono signal: 25 kHz deviation, f = 1 kHz; side band: SAP carrier frequency ±1 kHz	46	−	−	dB
α_{SP}	spectral spurious attenuation L + R/spurious	50 Hz to 100 kHz; mainly n x f_H; no de-emphasis; L + R: 25 kHz deviation, f = 1 kHz	40	−	−	dB

Notes to the requirements

1. Low-ohmic preferred, otherwise the signal loss and spreading at COMP, caused by Z_O and the composite input impedance (see input level adjustment control) must be taken into account.
2. In order to prevent clipping at overmodulation (maximum deviation in the BTSC system for 100% modulation is 73 kHz).

CHARACTERISTICS

All voltages are measured relative to GND; V_{CC} = 8.5 V, source resistance ≤ 600 Ω, output load R_L ≥ 10 kΩ, C_L ≤ 2.5 nF, AC coupled; f = 1 kHz; T_{amb} = +25 °C; volume gain control G_c = 0 dB; bass linear; treble linear; loudness off; AVL off; effects linear; composite input signal according to BTSC standard; see block diagram unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		8.0	8.5	9.0	V
I_{CC}	supply current		50	75	95	mA
V_{DC}	DC voltage at signal handling pins		–	$V_{CC}/2$	–	V
DECODER SECTION						
Input level adjustment control						
G_{LA}	input level adjustment control	maximum gain	–	4.0	–	dB
		maximum attenuation	–	–3.5	–	dB
G_{step}	step resolution		–	0.5	–	dB
$V_{i(RMS)}$	maximum input level		2	–	–	V
Z_i	input impedance		29.5	35	40.5	kΩ
Stereo decoder						
MPX_{L+R}	input level for 100% modulation L + R (25 kHz deviation) (RMS value)	input level adjusted via I²C-bus (L + R; f = 300 Hz); monitoring LINE OUT	–	250	–	mV
MPX_{L-R}	input level for 100% modulation L – R (50 kHz deviation) (peak value)		–	707	–	mV
MPX_{max}	headroom for L + R, L, R	f_{mod} < 15 kHz; THD < 15% for 75 µs equivalent input modulation	9	–	–	dB
MPX_{pilot}	nominal stereo pilot level (RMS value)		–	50	–	mV
ST_{ON}	pilot threshold STEREO ON (RMS value)	data STS = 1	–	–	35	mV
		data STS = 0	–	–	30	mV
ST_{OFF}	pilot threshold STEREO OFF (RMS value)	data STS = 1	15	–	–	mV
		data STS = 0	10	–	–	mV
Hyst	hysteresis		–	2.5	–	dB
Out_{L+R}	output level for 100% modulation L + R at LINE OUT	input level adjusted via I²C-bus (L + R; f = 300 Hz); monitoring LINE OUT	480	500	520	mV
α_{ST}	stereo channel separation L/R at LINE OUT	aligned with dual tone 14% modulation; alignment at f_L = 300 Hz; f_R = 3.1 kHz				
		f_L = 300 Hz; f_R = 3 kHz	25	35	–	dB
		f_L = 300 Hz; f_R = 8 kHz	20	30	–	dB
		f_L = 300 Hz; f_R = 10 kHz	15	25	–	dB
$L,R_{(f)}$	L, R frequency response	14% modulation; $f_{reference}$ = 300 Hz L or R				
		50 Hz to 11 kHz	–3	–	–	dB
		12 kHz	–	–3	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$THD_{L,R}$	total harmonic distortion L, R at LINE OUT	modulation L or R 1% to 100%; f = 1 kHz	–	0.2	1.0	%
S/N	S/N CCIR 468-2 weighted; quasi peak; V_O = 500 mV (RMS)	LINE OUT in position MONO	50	60	–	dB
Stereo decoder, oscillator (VCXO)						
f_o	nominal VCXO frequency ($32f_H$)	with nominal ceramic resonator	–	503.5	–	kHz
f_{of}	spread of free running frequency		500.0	–	507.0	kHz
Remark: The oscillator is designed to work together with MURATA resonator CSB503F58 for TDA9855. Change of the resonator supplier is possible, but the resonator specification must be close to CSB503F58 for TDA9855.						
Δf_H	capture range (nominal pilot)		±190	±265	–	Hz
SAP demodulator						
Remark: The internal SAP carrier level is determined by the composite input level and the level adjust gain.						
SAP_{IN}	nominal SAP carrier input level (RMS value)	15 kHz frequency deviation of intercarrier	–	150	–	mV
SAP_{ON}	pilot threshold SAP ON (RMS value)		–	–	85	mV
SAP_{OFF}	pilot threshold SAP OFF (RMS value)		35	–	–	mV
SAP_{HYS}	hysteresis		–	2	–	dB
SAP_{LEV}	SAP output level at LINE OUT (RMS value)	LINE OUT (LOL, LOR) in position SAP / SAP; f_{mod} = 300 Hz; 100% modulation	–	500	–	mV
F_{res}	frequency response	14% modulation; 50 [illegible] to 8 kHz; $f_{reference}$ = 300 Hz	–3	–	–	dB
THD	total harmonic distortion	1 kHz	–	0.5	2.0	%
LINE OUT (at pins LOL, LOR)						
V_o	nominal output voltage (RMS value)	100% modulation	–	500	–	mV
Headr	output headroom		9	–	–	dB
Z_o	output impedance		–	80	120	Ω
Out_{DC}	DC output voltage		0.45Vcc	0.5Vcc	0.55Vcc	V
R_L	output load resistance (AC)		5	–	–	kΩ
C_L	output load capacitance		–	–	2.5	nF
$\alpha_{ST\text{-}SAP}$	idle crosstalk L, R into SAP	100% modulation; f = 1 kHz; L or R; LINE OUT switched to SAP / SAP	50	–	–	dB
$\alpha_{SAP\text{-}ST}$	idle crosstalk SAP into L, R	100% modulation; f = 1 kHz; SAP; LINE OUT switched to stereo	50	–	–	dB
$\Delta V_{ST\text{-}SAP}$	output voltage difference if switched from L, R to SAP	250 Hz to 6.3 kHz	–	–	3	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dbx noise reduction circuit						
t_{adj}	stereo adjust time	see adjustment procedure	–	–	1	s
I_s	nominal timing current for nominal release rate of spectral RMS detector	I_s can be measured at pin 17 (pin 22) via current meter connected to $V_{CC}/2 + 1$ V	–	24	–	µA
ΔI_s	spread of timing current		–	–	15	%
$I_{s\ range}$	timing current adjustment range	7 steps via I²C-bus	–	±30	–	%
I_t	timing current for release rate of wideband RMS detector		–	$I_s/3$	–	µA
Rel_{rate}	nominal RMS detector release rate	nominal timing current and external capacitor values				
	wideband		–	125	–	dB/s
	spectral		–	381	–	dB/s
AUDIO PART Circuit section from pins LIL, LIR to pins OUTL, OUTR, OUTS Select in to input line control						
B	roll-off frequencies	C_6, C_7, C_{10}, C_{26}, C_{27}, C_{29} = 2.2 µF; $Z_i = Z_{i\ min}$				
		low frequency (–3 dB)	–	–	20	Hz
		high frequency (–0.5 dB)	20	–	–	kHz
THD	total harmonic distortion	V_i = 1 V (RMS); G_c = 0 dB; AVL on	–	0.2	0.5	%
		V_i = 2 V (RMS); G_c = 0 dB; AVL on	–	0.2	0.5	%
		V_i = 1 V (RMS); G_c = 0 dB; AVL off	–	0.05	–	%
		V_i = 2 V (RMS); G_c = 0 dB; AVL off	–	0.02	–	%
RR	power supply ripple rejection	$V_{r(RMS)}$ < 200 mV; f = 100 Hz	47	50	–	dB
α_B	crosstalk (20 log $V_{bus(p-p)}$ / $V_{o(RMS)}$) between bus inputs and signal outputs	note 1	–	110	–	dB
V_{no}	noise output voltage	CCIR 468-2 weighted; quasi peak	–	40	80	µV
		measured in dBA	–	8	–	µV
α_{cs}	channel separation	V_i = 1 V; f = 1 kHz	75	–	–	dB
		V_i = 1 V; f = 12.5 kHz	75	–	–	dB
Selector (from pins LOL, LOR, LIL, LIR to pins SOL, SOR)						
Z_i	input impedance		16	20	24	kΩ
α_s	input isolation of one selected source to the other input	f = 1 kHz; V_i = 1 V	86	96	–	dB
		f = 12.5 kHz; V_i = 1 V	80	96	–	dB
$V_{i(RMS)}$	maximum input voltage	THD < 0.5%	2	2.3	–	V
$V_{DC\ OFF}$	DC offset voltage at selector out by selection of any inputs		–	–	25	mV
Z_o	output impedance		–	80	120	Ω
R_L	output load resistance (AC)		5	–	–	kΩ
C_L	output load capacitance		–	–	2.5	nF
G_c	voltage gain, selector		–	0	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Automatic volume level control (AVL)						
Z_i	input impedance		8.8	11.0	13.2	kΩ
$V_{i(RMS)}$	maximum input voltage	THD < 0.2%	2	–	–	V
G_v	gain, maximum boost		5	6	7	dB
	maximum attenuation		14	15	16	dB
G_{step}	equivalent step width between the input stages (soft switching system)		–	1.5	–	dB
$V_{i(RMS)}$	input level at maximum boost	see Fig.4	–	0.1	–	V
	input level at maximum attenuation		–	1.125	–	V
$V_{o(RMS)}$	output level in AVL operation range		160	200	250	mV
$V_{DC\ OFF}$	DC offset between different gain steps	note 2; voltage at pin CAV				
		6.50 V to 6.33 V	–	–	6	mV
		6.33 V to 6.11 V	–	–	6	mV
		6.11 V to 5.33 V	–	–	6	mV
		5.33 V to 2.60 V	–	–	6	mV
R_{att}	discharge resistors for attack time constant	note 3;				
		AT1 = 0; AT2 = 0	340	420	520	Ω
		AT1 = 1; AT2 = 0	590	730	910	Ω
		AT1 = 0; AT2 = 1	0.96	1.2	1.5	kΩ
		AT1 = 1; AT2 = 1	1.7	2.1	2.6	kΩ
I_{dec}	charge current for decay time	note 4	1.6	2.0	2.4	µA
Effect controls						
α_{spat1}	anti-phase crosstalk by spatial effect		–	52	–	%
α_{spat2}			–	30	–	%
φ	phase shift by pseudo-stereo	see Fig.5	–	–	–	–
Volume tone control part (input pins VIL, VIR to pins OUTX, to pin OUTS)						
Z_i	input impedance volume input		8.0	10.0	12.0	kΩ
Z_o	output impedance		–	80	120	Ω
R_L	output load resistance (AC)		5	–	–	kΩ
C_L	output load capacitance		–	–	2.5	nF
$V_{i(RMS)}$	maximum input voltage	THD < 0.5%	2.0	2.15	–	V
V_{no}	noise output voltage	CCIR 468-2 weighted; quasi peak				
		G_c = 16 dB	–	110	220	µV
		G_c = 0 dB	–	33	50	µV
		mute position	–	10	–	µV
G_c	total continuous control range					
	maximum boost		–	16	–	dB
	maximum attenuation		–	71	–	dB
G_{step}	step resolution		–	1	–	dB
	step error between any adjoining step		–	–	0.5	dB
ΔG_a	attenuator set error	G_c = +16 to –50 dB	–	–	2	dB
		G_c = –51 to –71 dB	–	–	3	dB
ΔG_t	gain tracking error	G_c = +16 to –50 dB	–	–	2	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
α_m	mute attenuation		80	–	–	dB
$V_{DC\ OFF}$	DC step offset between any adjacent step	G_c = +16 to 0 dB	–	0.2	10.0	mV
		G_c = 0 to –71 dB	–	–	5	mV
	DC step offset between any step to mute	G_c = +16 to +1 dB	–	2	15	mV
		G_c = 0 to –71 dB	–	1	10	mV
Loudness control part						
L_B	maximum loudness boost	loudness on; referred to loudness off; boost is determined by external components; see Fig.6;				
		f = 40 Hz	–	17	–	dB
		f = 10 kHz	–	4.5	–	dB
Bass control (see Fig.7)						
G_b	bass control maximum boost	f = 40 Hz	15.5	16.5	17.5	dB
	maximum attenuation	f = 40 Hz	11	12	13	dB
G_{step}	step resolution	f = 40 Hz	–	1.5	–	dB
	step error between any adjoining step		–	–	0.5	dB
$V_{DC\ OFF}$	DC step offset between any adjacent step		–	–	15	mV
Treble control (see Fig.8)						
G_t	treble control maximum boost	f = 15 kHz	11	12	13	dB
	maximum attenuation	f = 15 kHz	11	12	13	dB
	maximum boost	f > 15 kHz	–	–	15	dB
G_{step}	step resolution	f = 15 kHz	–	3	–	dB
	step error between any adjoining step		–	–	0.5	dB
$V_{DC\ OFF}$	DC step offset between any adjacent step		–	–	10	mV
Subwoofer or surround control						
G_s	subwoofer control	f = 40 Hz				
	maximum boost		12	14	16	dB
	maximum attenuation		12	14	16	dB
G_{step}	step resolution		–	2	–	dB
α_m	mute attenuation		60	–	–	dB
$V_{DC\ OFF}$	DC step offset between any adjacent step	G_s = 0 to +14 dB	–	–	10	mV
		G_s = 0 to –14 dB	–	–	5	mV
	DC step offset between any step to mute	G_s = +2 to +14 dB without input offset (pin SW connected to V_{REF})	–	–	15	mV
		G_s = +2 to +14 dB inclusive offset from OUTR, OUTL	–	–	50	mV
		G_s = 0 to –14 dB	–	–	10	mV
R_F	internal resistor for low-pass filter with external capacitor at pin SW		4	5	6	kΩ
L + R_{REJ}	common mode rejection in surround sound at pin OUTS	mono signal at VIL/VIR; f = 1 kHz; V_i = 1 V; balance = 0 dB	26	36	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Muting at power supply drop for OUTL, OUTR, OUTS						
$V_{CC-DROP}$	supply drop for mute active		–	V_{CAP} – 0.7	–	V
Power on reset						
When reset is active the GMU-bit (general mute) and the LMU-bit (LINEOUT - mute) is set and the I²C-bus receiver is in reset position						
V_{CC}	start of reset	increasing supply voltage	–	–	2.5	V
	end of reset		5.2	6	6.8	V
	start of reset	decreasing supply voltage	4.2	5	5.8	V
Digital part (I²C-bus pins; note 5)						
V_{IH}	HIGH level input voltage		3	–	V_{CC}	V
V_{IL}	LOW level input voltage		–0.3	–	+1.5	V
I_{IH}	HIGH level input current		–10	–	+10	μA
I_{IL}	LOW level input current		–10	–	+10	μA
V_{OL}	LOW level output voltage	I_L = 3 mA	–	–	0.4	V

Notes to the characteristics

1. The transmission contains:
   - total initialization with MAD and SAD for volume and 11 DATA words, see also definition of characteristics
   - clock frequency = 50 kHz
   - repetition burst rate = 400 Hz
   - maximum bus signal amplitude = 5 V_{p-p}.
2. The listed pin voltage corresponds with typical gain steps of +6 dB, +3 dB, 0 dB, –6 dB, –15 dB.
3. Attack time constant = $C_{AV} \times R_{att}$.
4. Decay time = $$\frac{C_{AV} \times 0.76\ V \left(10^{-\frac{G_{v1}}{20}} - 10^{-\frac{G_{v2}}{20}}\right)}{I_{dec}}$$
   Example: C_{AV} = 4.7 μF; I_{dec} = 2 μA; G_{v1} = –9 dB; G_{v2} = +6 dB → decay time result: 4.14 s.
5. The AC characteristics are in accordance with the I²C-bus specification. Full specification of I²C-bus will be supplied on request. The maximum clock frequency is 100 kHz.

ADJUSTMENT PROCEDURE

Composite input level adjustment. Feed in from FM demodulator the composite signal with 100% modulation (25 kHz deviation) L + R, f = 300 Hz. Set input level control via I²C-bus monitoring line out (500 mV ± 20 mV). Store the setting in a none volatile memory. Adjustment of spectral and wideband expander via stereo channel separation adjust.

Automatic adjustment procedure

- Capacitors of external inputs EIL, EIR must be grounded
- Composite input signal L = 300 Hz, R = 3.1 kHz, 14% modulation for each channel; volume gain +16 dB via I²C-bus. To avoid anoing sound level set GMU bit to '1' during adjustment procedure
- Effects, AVL, loudness off
- Selector setting SC0, SC1, SC2 = 0, 0, 0 (see Table 8)
- Line out setting bits: STEREO = 1, SAP = 0 (see Table 15)
- Start adjustment by transmission ADJ = 1 in register ALI3. The decoder will align itself
- After 1 s, stop alignment by transmitting ADJ = 0 in register ALI3 read the alignment data by an I²C-bus read operation from ALR1 and ALR2 (see I²C-bus protocol) and store it in a none volatile memory. The alignment procedure overwrites the previous data stored in ALI1 and ALI2
- Disconnect the capacitors of external inputs from ground.

Manual adjust

Manual adjust is necessary when no dual tone generator is available (e.g. for service).

- Spectral and wideband data have to be set to 10000 (middle position for adjustment range)
- Composite input L = 300 Hz, 14% modulation
- Adjust channel separation by varying wideband data
- Composite input L = 3 kHz, 14% modulation
- Adjust channel separation by varying spectral data
- Iterative spectral/wideband operation for optimal adjust
- Store data in none volatile memory.

After every POWER ON, the alignment data and the input level adjustment data must be loaded from the none volatile memory.

Timing current for release rate

Due to possible internal and external spreading, the timing current can be adjusted via I²C-bus, see Table 19, as recommended by dbx.

I²C-BUS PROTOCOL

I²C-bus format to read (slave transmits data)

S	SLAVE ADDRESS	R/W	A	DATA	MA	DATA	P

Where:

S	=	start condition, generated by the master
standard SLAVE ADDRESS	=	101 101 1 pin MAD not connected
pin programmable SLAVE ADDRESS	=	101 101 0 pin MAD connected to ground
R/W	=	1 (read), generated by the master
A	=	acknowledge, generated by the slave
DATA	=	slave transmits an 8-bit data word
MA	=	acknowledge, generated by the master
P	-	stop condition, generated by the master

Table 1 Definition of the transmitted bytes after read condition.

FUNCTION	BYTE	MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
Alignment read 1	ALR1	Y	SAPP	STP	A14	A13	A12	A11	A10
Alignment read 2	ALR2	Y	SAPP	STP	A24	A23	A22	A21	A20

Function of the bits:

STP	stereo pilot identification (stereo received = 1)
SAPP	SAP pilot identification (SAP received = 1)
A1x to A2x	stereo alignment read data
A1x	for wideband expander
A2x	for spectral expander
Y	indefinite

The master generates an acknowledge when it has received the first data word, ALR1, then the slave transmits the next data word ALR2. The master next generates an acknowledge, then the slave begins transmitting the first data word ALR1, and so on until the master generates no acknowledge and transmitts condition P.

I²C-bus format to write (slave receives data)

S	SLAVE ADDRESS	R/W	A	SUBADDRESS	A	DATA	A	P

Where:

S	=	start condition
standard SLAVE ADDRESS	=	101 101 1 pin MAD not connected
pin programmable SLAVE ADDRESS	=	101 101 0 pin MAD connected to ground
R/W	=	0 (write)
A	=	acknowledge, generated by the slave
SUBADDRESS (SAD)	=	see Table 2
DATA	=	see Table 3
P	=	stop condition

If more than 1 byte of DATA is transmitted, then auto-increment is performed, starting from the transmitted subaddress and auto-increment of subaddress according to the order of Table 2 is performed.

Subaddress

Table 2 Second byte after slave address.

FUNCTION	REGISTER	MSB D7	D6	D5	D4	D3	D2	D1	LSB D0	HEX
volume right	VR	0	0	0	0	0	0	0	0	00
volume left	VL	0	0	0	0	0	0	0	1	01
bass	BA	0	0	0	0	0	0	1	0	02
treble	TR	0	0	0	0	0	0	1	1	03
subwoofer	SW	0	0	0	0	0	1	0	0	04
control 1	CON1	0	0	0	0	0	1	0	1	05
control 2	CON2	0	0	0	0	0	1	1	0	06
control 3	CON3	0	0	0	0	0	1	1	1	07
alignment 1	ALI1	0	0	0	0	1	0	0	0	08
alignment 2	ALI2	0	0	0	0	1	0	0	1	09
alignment 3	ALI3	0	0	0	0	1	0	1	0	0A

Definition of third byte

Table 3 Third byte after slave address.

FUNCTION	REGISTER	MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
volume right	VR	0	VR6	VR5	VR4	VR3	VR2	VR1	VR0
volume left	VL	0	VL6	VL5	VL4	VL3	VL2	VL1	VL0
bass	BA	0	0	0	BA4	BA3	BA2	BA1	BA0
treble	TR	0	0	0	TR4	TR3	TR2	TR1	0
subwoofer	SW	0	0	SW5	SW4	SW3	SW2	0	0
control 1	CON1	GMU	AVLON	LOFF	0	SUR	SC2	SC1	SC0
control 2	CON2	SAP	STEREO	TZCM	VZCM	LMU	EF2	EF1	EF0
control 3	CON3	0	0	0	0	L3	L2	L1	L0
alignment 1	ALI1	0	0	0	A14	A13	A12	A11	A10
alignment 2	ALI2	STS	0	0	A24	A23	A22	A21	A20
alignment 3	ALI3	ADJ	AT1	AT2	0	1	TC2	TC1	TC0

Function of the bits:

VR0 to VR6	volume control right
VL0 to VL6	volume control left
BA0 to BA4	bass control
TR1 to TR3	treble control
SW2 to SW5	subwoofer, surround control
GMU	mute control for all outputs (general mute)
AVLON	AVL on/off
LOFF	switch loudness on/off
SUR	surround/subwoofer SUR = 1 → (L – R)/2; SUR = 0 → (L + R)/2
SC0 to SC2	selection between line in and line out
STEREO, SAP	mode selection for line out
TZCM	zero cross mode in mute operation (treble and subwoofer/surround output stage)
VZCM	zero cross mode in volume operation
LMU	mute control for line out
EF0 to EF2	selection between mono, stereo linear, spatial stereo and pseudo mode
L0 to L3	input level adjust
ADJ	stereo adjust on/off
A1X	stereo alignment data for wideband expander
A2X	stereo alignment data for spectral expander
AT1, AT2	attack time at AVL
TC0 to TC2	timing current alignment data
STS	stereo level switch

Table 4 Volume setting in register VR and VL.

G_c (dB)	DATA							HEX
	D6 V6	D5 V5	D4 V4	D3 V3	D2 V2	D1 V1	D0 V0	
16	1	1	1	1	1	1	1	7F
15	1	1	1	1	1	1	0	7E
14	1	1	1	1	1	0	1	7D
13	1	1	1	1	1	0	0	7C
12	1	1	1	1	0	1	1	7B
11	1	1	1	1	0	1	0	7A
10	1	1	1	1	0	0	1	79
9	1	1	1	1	0	0	0	78
8	1	1	1	0	1	1	1	77
7	1	1	1	0	1	1	0	76
6	1	1	1	0	1	0	1	75
5	1	1	1	0	1	0	0	74
4	1	1	1	0	0	1	1	73
3	1	1	1	0	0	1	0	72
2	1	1	1	0	0	0	1	71
1	1	1	1	0	0	0	0	70
0	1	1	0	1	1	1	1	6F
−1	1	1	0	1	1	1	0	6E
−2	1	1	0	1	1	0	1	6D
−3	1	1	0	1	1	0	0	6C
−4	1	1	0	1	0	1	1	6B
−5	1	1	0	1	0	1	0	6A
−6	1	1	0	1	0	0	1	69
−7	1	1	0	1	0	0	0	68
−8	1	1	0	0	1	1	1	67
−9	1	1	0	0	1	1	0	66
−10	1	1	0	0	1	0	1	65
−11	1	1	0	0	1	0	0	64
−12	1	1	0	0	0	1	1	63
−13	1	1	0	0	0	1	0	62
−14	1	1	0	0	0	0	1	61
−15	1	1	0	0	0	0	0	60
−16	1	0	1	1	1	1	1	5F
−17	1	0	1	1	1	1	0	5E
−18	1	0	1	1	1	0	1	5D
−19	1	0	1	1	1	0	0	5C
−20	1	0	1	1	0	1	1	5B
−21	1	0	1	1	0	1	0	5A
−22	1	0	1	1	0	0	1	59
−23	1	0	1	1	0	0	0	58
−24	1	0	1	0	1	1	1	57
−25	1	0	1	0	1	1	0	56
−26	1	0	1	0	1	0	1	55
−27	1	0	1	0	1	0	0	54
−28	1	0	1	0	0	1	1	53
−29	1	0	1	0	0	1	0	52
−30	1	0	1	0	0	0	1	51
−31	1	0	1	0	0	0	0	50
−32	1	0	0	1	1	1	1	4F
−33	1	0	0	1	1	1	0	4E

G_c (dB)	DATA							HEX
	D6 V6	D5 V5	D4 V4	D3 V3	D2 V2	D1 V1	D0 V0	
−34	1	0	0	1	1	0	1	4D
−35	1	0	0	1	1	0	0	4C
−36	1	0	0	1	0	1	1	4B
−37	1	0	0	1	0	1	0	4A
−38	1	0	0	1	0	0	1	49
−39	1	0	0	1	0	0	0	48
−40	1	0	0	0	1	1	1	47
−41	1	0	0	0	1	1	0	46
−42	1	0	0	0	1	0	1	45
−43	1	0	0	0	1	0	0	44
−44	1	0	0	0	0	1	1	43
−45	1	0	0	0	0	1	0	42
−46	1	0	0	0	0	0	1	41
−47	1	0	0	0	0	0	0	40
−48	0	1	1	1	1	1	1	3F
−49	0	1	1	1	1	1	0	3E
−50	0	1	1	1	1	0	1	3D
−51	0	1	1	1	1	0	0	3C
−52	0	1	1	1	0	1	1	3B
−53	0	1	1	1	0	1	0	3A
−54	0	1	1	1	0	0	1	39
−55	0	1	1	1	0	0	0	38
−56	0	1	1	0	1	1	1	37
−57	0	1	1	0	1	1	0	36
−58	0	1	1	0	1	0	1	35
−59	0	1	1	0	1	0	0	34
−60	0	1	1	0	0	1	1	33
−61	0	1	1	0	0	1	0	32
−62	0	1	1	0	0	0	1	31
−63	0	1	1	0	0	0	0	30
−64	0	1	0	1	1	1	1	2F
−65	0	1	0	1	1	1	0	2E
−66	0	1	0	1	1	0	1	2D
−67	0	1	0	1	1	0	0	2C
−68	0	1	0	1	0	1	1	2B
−69	0	1	0	1	0	1	0	2A
−70	0	1	0	1	0	0	1	29
−71	0	1	0	1	0	0	0	28
mute	0	1	0	0	1	1	1	27

Table 5 Bass setting in register BA.

G_b (dB)	DATA D4 BA4	D3 BA3	D2 BA2	D1 BA1	D0 BA0	HEX
16.5	1	1	0	0	1	19
15	1	1	0	0	0	18
13.5	1	0	1	1	1	17
12	1	0	1	1	0	16
10.5	1	0	1	0	1	15
9	1	0	1	0	0	14
7.5	1	0	0	1	1	13
6	1	0	0	1	0	12
4.5	1	0	0	0	1	11
3	1	0	0	0	0	10
1.5	0	1	1	1	1	0F
0	0	1	1	1	0	0E
−1.5	0	1	1	0	1	0D
−3	0	1	1	0	0	0C
−4.5	0	1	0	1	1	0B
−6	0	1	0	1	0	0A
−7.5	0	1	0	0	1	09
−9	0	1	0	0	0	08
−10.5	0	0	1	1	1	07
−12	0	0	1	1	0	06

Table 6 Treble setting in register TR.

G_t (dB)	DATA D4 TR4	D3 TR3	D2 TR2	D1 TR1	HEX
12	1	0	1	1	16
9	1	0	1	0	14
6	1	0	0	1	12
3	1	0	0	0	10
0	0	1	1	1	0E
−3	0	1	1	0	0C
−6	0	1	0	1	0A
−9	0	1	0	0	08
−12	0	0	1	1	06

Table 7 Subwoofer/surround setting in register SW.

G_s (dB)	DATA D5 SW5	D4 SW4	D3 SW3	D2 SW2	HEX
14	1	1	1	1	3C
12	1	1	1	0	38
10	1	1	0	1	34
8	1	1	0	0	30
6	1	0	1	1	2C
4	1	0	1	0	28
2	1	0	0	1	24
0	1	0	0	0	20
−2	0	1	1	1	1C
−4	0	1	1	0	18
−6	0	1	0	1	14
−8	0	1	0	0	10
−10	0	0	1	1	0C
−12	0	0	1	0	08
−14	0	0	0	1	04
mute	0	0	0	0	00

Table 8 Selector setting in register CON1.

FUNCTION: input connected to output	SOR, SOL	DATA D2 SC2	D1 SC1	D0 SC0
input	LOR, LOL	0	0	0
input	LOR, LOR	0	0	1
input	LOL, LOL	0	1	0
input	LOL, LOR	0	1	1
input	LIR, LIL	1	0	0
input	LIR, LIR	1	0	1
input	LIL, LIL	1	1	0
input	LIL, LIR	1	1	1

Table 9 SUR bit setting in register CON1.

FUNCTION	DATA D3
surround sound	1
subwoofer	0

Table 10 LOFF bit setting in register CON1.

CHARACTERISTIC	DATA D5
with loudness	0
linear	1

Table 11 AVLON bit setting in register CON1.

FUNCTION	DATA D6
automatic volume control off	0
automatic volume control on	1

Table 12 Mute setting.

REGISTER CON1		REGISTER CON2	
FUNCTION	DATA D7 GMU	FUNCTION	DATA D3 LMU
forced mute at OUTR, OUTL, OUTS	1	forced mute at LOR, LOL	1
audio processor controlled outputs	0	stereo processor controlled outputs	0

Table 13 Effects setting in register CON2.

FUNCTION	DATA D2 EF2	D1 EF1	D0 EF0
stereo linear on	0	0	0
pseudo on	0	0	1
spatial stereo, 30% anti-phase crosstalk	0	1	0
spatial stereo, 50% anti-phase crosstalk	0	1	1
forced mono	1	1	1

Table 14 Zero cross detection setting in register CON2.

FUNCTION	DATA D5 TZCM	FUNCTION	DATA D4 VZCM
direct mute control	0	direct volume control	0
mute control delayed until the next zero crossing	1	volume control delayed until the next zero crossing	1

Table 15 Switch setting at line out.

FUNCTION		DATA	DATA	
line out signals at		transmission status	setting bits in register CON2	
LOL	LOR	internal switch readable bits in register ALR1, ALR2: D6 SAPP D5 STP	D7 SAP	D6 STEREO
SAP	SAP	SAP received	1	1
mute	mute	no SAP received	1	1
left	right	stereo received	0	1
mono	mono	no stereo received	0	1
mono	SAP	SAP received	1	0
mono	mute	no SAP received	1	0
mono	mono		0	0

Table 16 Level adjust setting in register CON3.

G_l (dB)	DATA D3 L3	D2 L2	D1 L1	D0 L0	HEX
+4	1	1	1	1	
+3.5	1	1	1	0	
+3	1	1	0	1	0D
+2.5	1	1	0	0	0C
+2	1	0	1	1	0B
+1.5	1	0	1	0	0A
+1	1	0	0	1	09
+0.5	1	0	0	0	08
0	0	1	1	1	07
−0.5	0	1	1	0	06
−1	0	1	0	1	05
−1.5	0	1	0	0	04
−2	0	0	1	1	03
−2.5	0	0	1	0	02
−3	0	0	0	1	01
−3.5	0	0	0	0	00

Table 17 Alignment data for expander in read register ALR1 and ALR2 and in write register ALI1 and ALI2.

FUNCTION	DATA				
	D4 AX4	D3 AX3	D2 AX2	D1 AX1	D0 AX0
gain increase	1	1	1	1	1
	1	1	1	1	0
	1	1	1	0	1
	1	1	1	0	0
	1	1	0	1	1
	1	1	0	1	0
	1	1	0	0	1
	1	1	0	0	0
	1	0	1	1	1
	1	0	1	1	0
	1	0	1	0	1
	1	0	1	0	0
	1	0	0	1	1
	1	0	0	1	0
	1	0	0	0	1
nominal gain	1	0	0	0	0
	0	1	1	1	1
gain decrease	0	1	1	1	0
	0	1	1	0	1
	0	1	1	0	0
	0	1	0	1	1
	0	1	0	1	0
	0	1	0	0	1
	0	1	0	0	0
	0	0	1	1	1
	0	0	1	1	0
	0	0	1	0	1
	0	0	1	0	0
	0	0	0	1	1
	0	0	0	1	0
	0	0	0	0	1
	0	0	0	0	0

Table 18 STS bit setting in register ALI2 (pilot threshold stereo on).

FUNCTION	DATA D7
STON ≤ 35 mV	1
STON ≤ 30 mV	0

Table 19 Timing current setting in register ALI3.

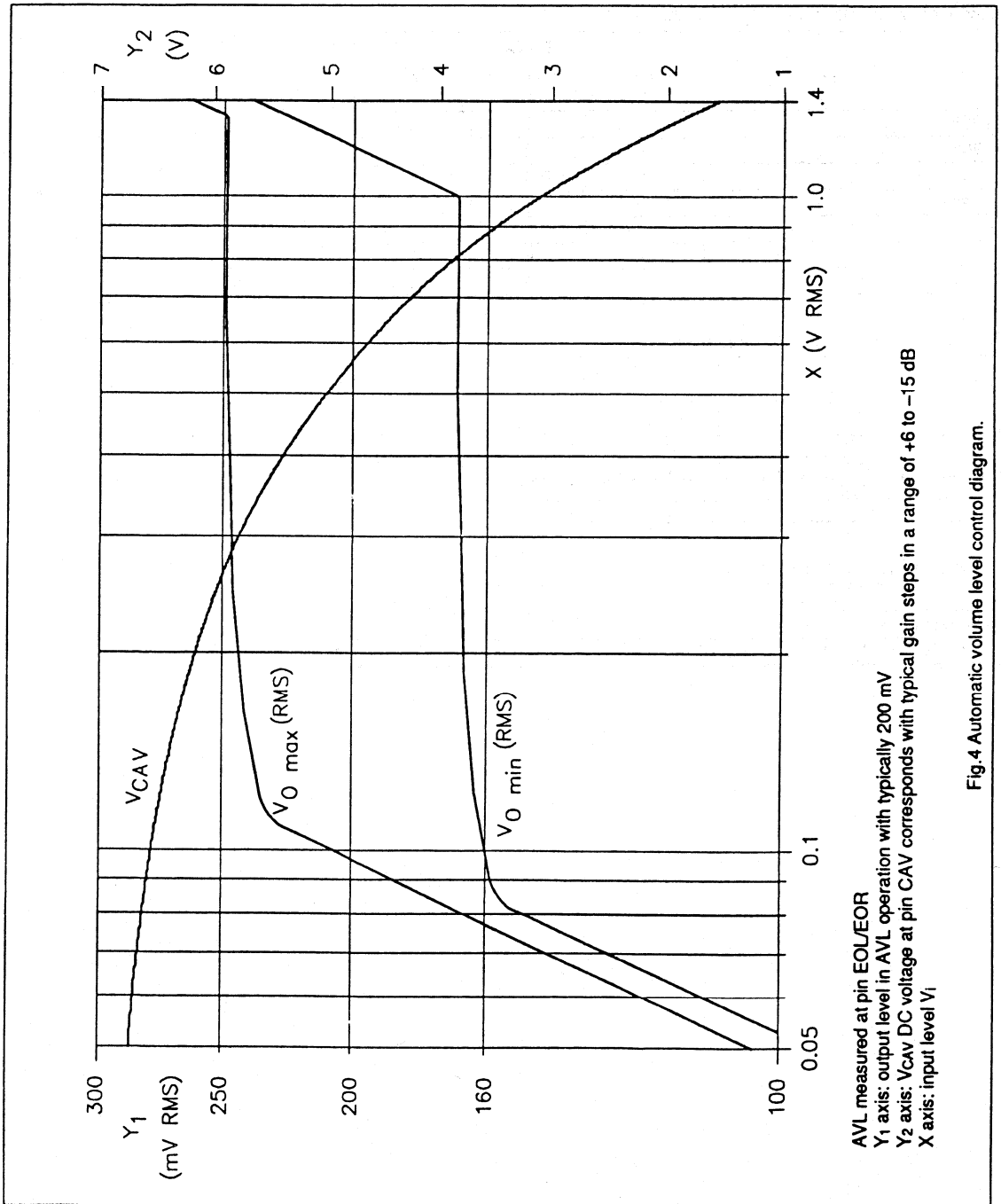
I_s range	DATA D2 TC2	D1 TC1	D0 TC0
+30%	1	0	0
+20%	1	0	1
+10%	1	1	0
nominal	0	1	1
−10%	0	1	0
−20%	0	0	1
−30%	0	0	0

Table 20 AVL attack time setting in register ALI3.

R_{att} (Ω)	DATA D6 AT1	D5 AT2
420	0	0
730	1	0
1200	0	1
2100	1	1

Table 21 ADJ bit setting in register ALI3.

FUNCTION	DATA D7
stereo decoder operation mode	0
auto adjustment of channel separation	1



AVL measured at pin EOL/EOR
Y_1 axis: output level in AVL operation with typically 200 mV
Y_2 axis: V_{CAV} DC voltage at pin CAV corresponds with typical gain steps in a range of +6 to −15 dB
X axis: input level V_I

Fig.4 Automatic volume level control diagram.

CURVE	CAPACITANCE AT PIN 43 (56) (nF)	CAPACITANCE AT PIN 42 (55) (nF)	EFFECT
1	15	15	normal
2	5.6	47	intensified
3	5.6	68	more intensified

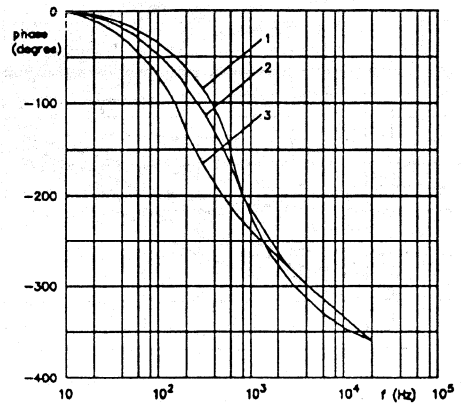


Fig.5 Pseudo (phase in degrees) as a function of frequency (left output).

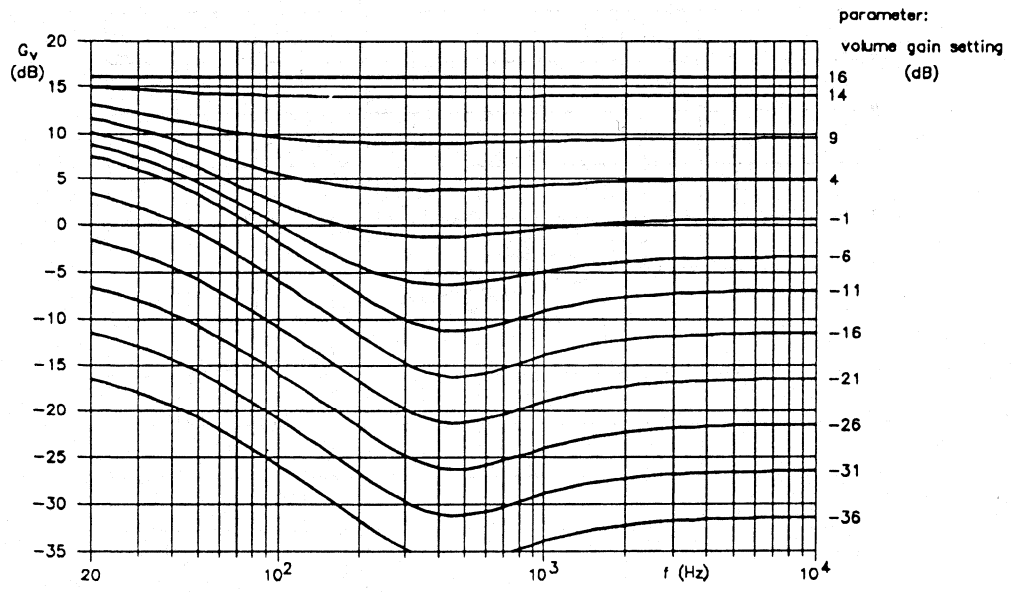


Fig.6 Volume control with loudness.

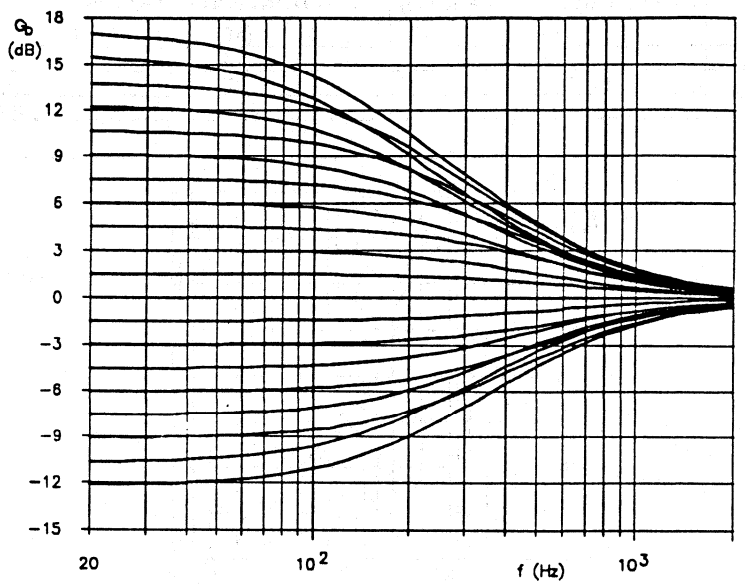


Fig.7 Bass control.

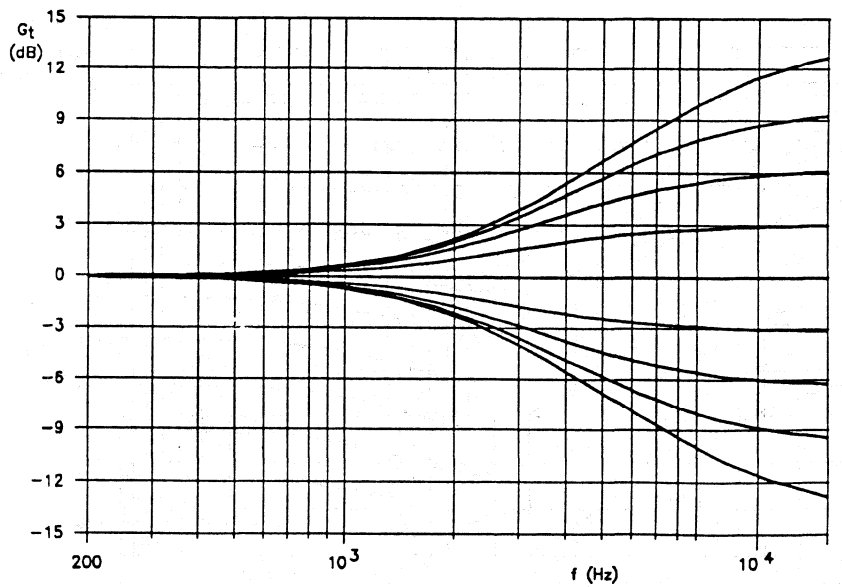


Fig.8 Treble control.

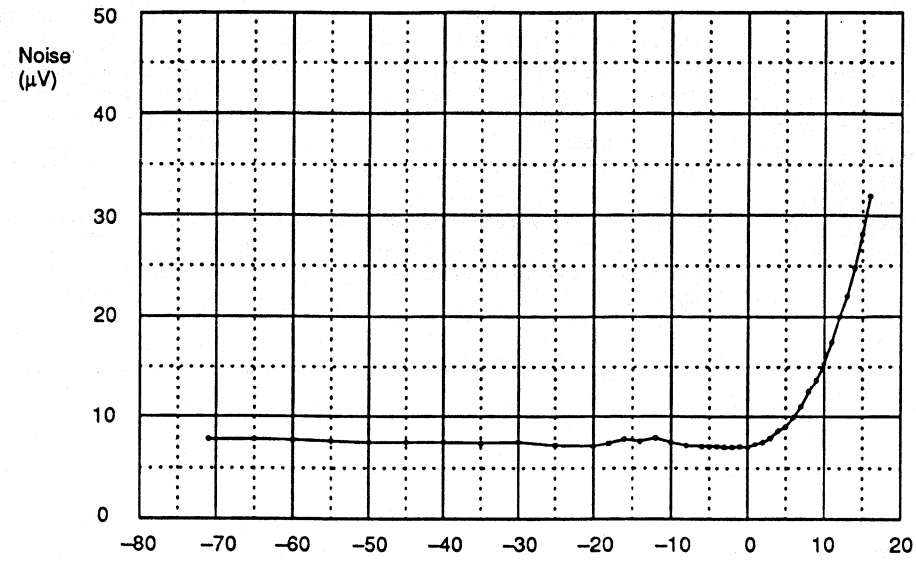


Fig.9 Noise as function of gain in dBA (RMS value).

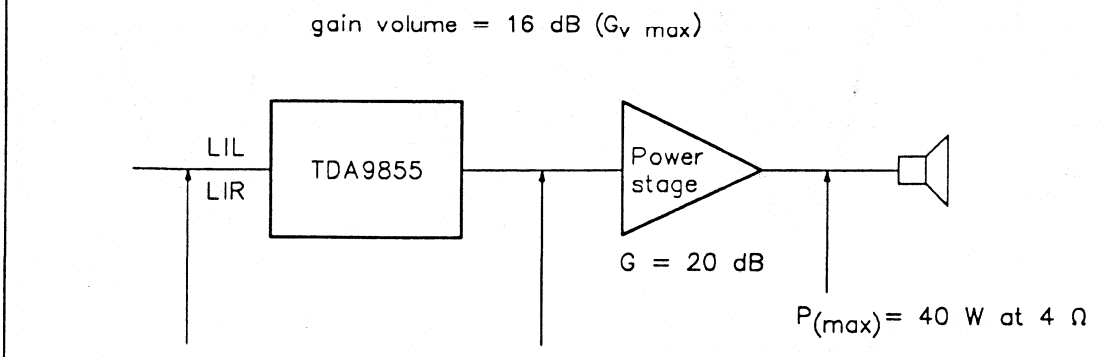


Fig.10 Level diagram.

APPLICATION HINTS

Selection of input signals by using the zero crossing mute mode

A selection between the internal signal path and the external input LIL/LIR produces a modulation click depending on the difference of the signal values at the time of switching. At t_1 the maximum possible difference between signals is 7 $V_{(p-p)}$ and gives a large click. Using the zero cross detector no modulation click is audible.

For example: The selection is enabled at t_1, the microcontroller sets the zero cross bit (TZCM = 1) and then the mute bit (GMU = 1) via the I²C-bus. The output signal follows the input A signal, until the next zero crossing occurs and then activates mute.
After a fixed delay time before t_2, the microcontroller has to send the forced mute mode (TZCM = 0) and the return to the zero crossing mode (TZCM = 1) to be sure that mute is enabled.

The output signal remains muted until the next signal zero crossing of input B occurs, and then follows that signal.
The delay time $t_2 - t_1$ is e. g. 40 ms. The zero cross function is working at the lowest frequency of 40 Hz.

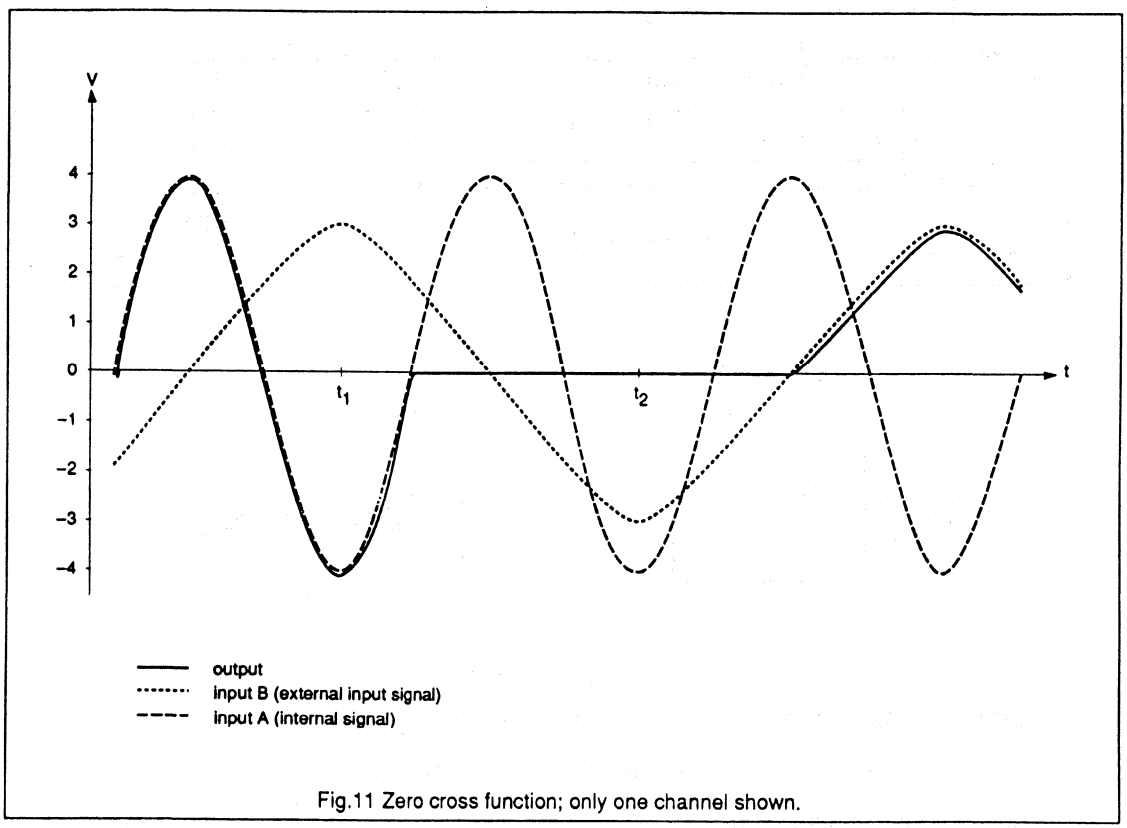


Fig.11 Zero cross function; only one channel shown.

Loudness filter calculation example

Fig.12 shows the basic loudness circuit with an external low-pass filter application. R_1 allows an attenuation range of 21 dB while the boost is determined by the gain stage V_1. Both result in a loudness control range of +16 dB to −12 dB.
Defining $f_{reference}$ as the frequency where the level does not change while switching loudness on/off. The external resistor R_3 for $f_{reference} \rightarrow \infty$ can be calculated as

$$R_3 = R_1 \frac{10^{G_v/20}}{1 - 10^{G_v/20}}$$

with G_v = −21 dB and R_1 = 33 kΩ results in R_3 = 3.2 kΩ.
For the low-pass filter characteristic the value of the external capacitor C_1 can be determined by setting a specific boost for a defined frequency and referring the gain to G_v at $f_{reference}$ as indicated above.

$$\left|\frac{1}{j\omega C_1}\right| = \frac{(R_1 + R_3) \times 10^{G_v/20} - R_3}{1 - 10^{G_v/20}}$$

For example: 3 dB boost at f = 1 kHz
$G_v = G_{v\,reference}$ + 3 dB = −18 dB;
f = 1 kHz and C_1 = 100 nF
If a loudness characteristic with additional high frequency boost is desired, an additional high-pass section has to be included in the external filter circuit as indicated in the block diagram. A filter configuration that provides AC coupling avoids offset voltage problems.
Fig.13 shows an example of the loudness circuit with bass and treble boost.

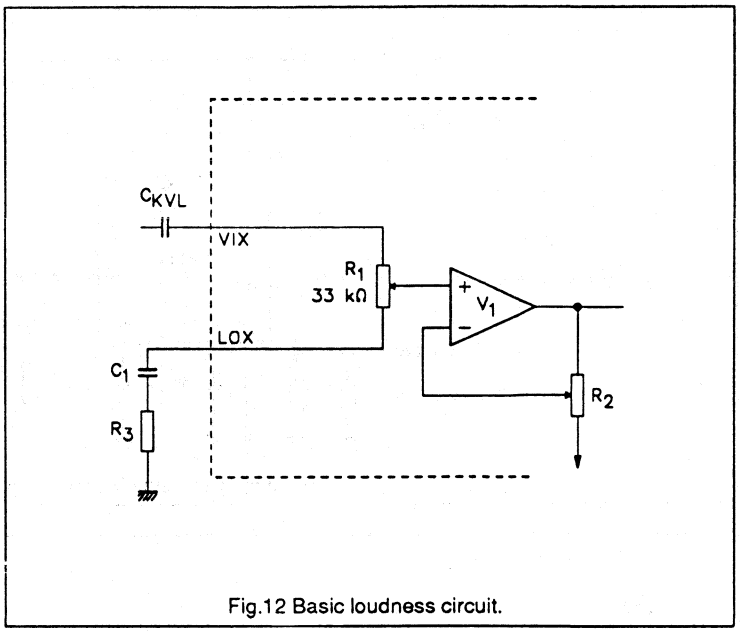


Fig.12 Basic loudness circuit.

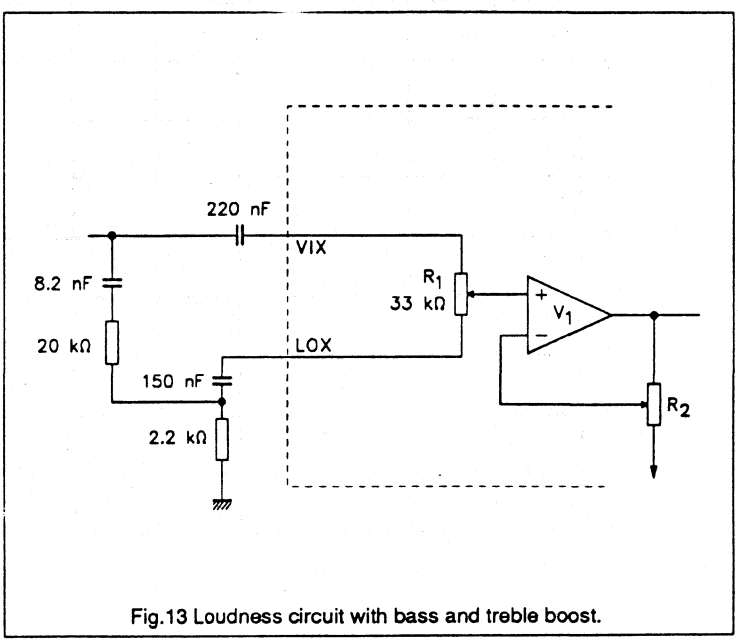


Fig.13 Loudness circuit with bass and treble boost.

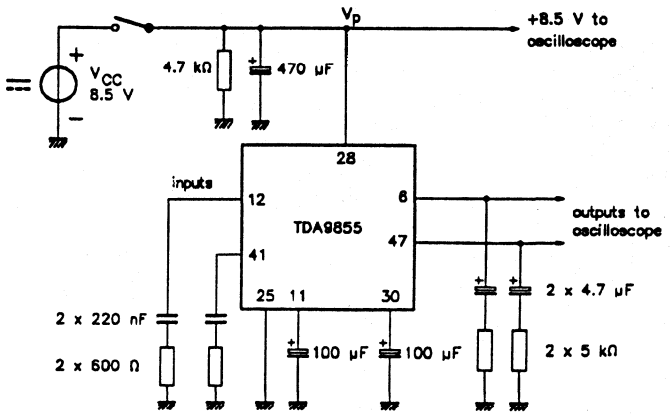


Fig.14 Turn-on/off power supply circuit diagram.

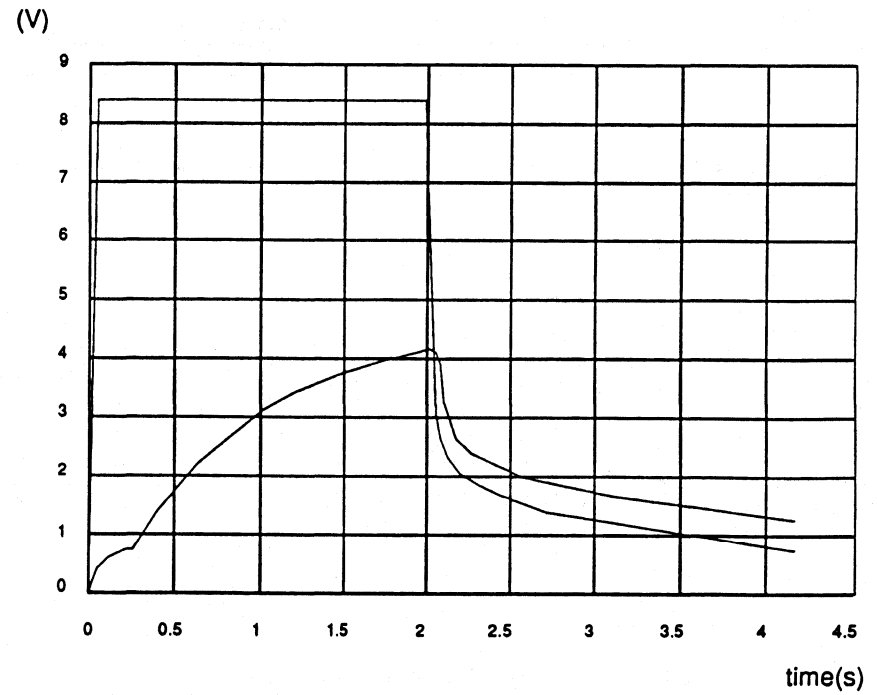
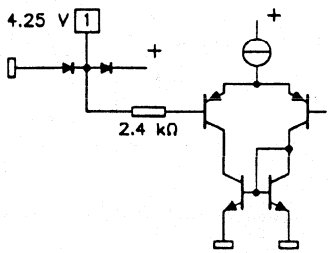
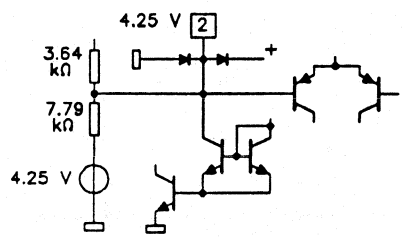


Fig.15 Turn-on/off behaviour.

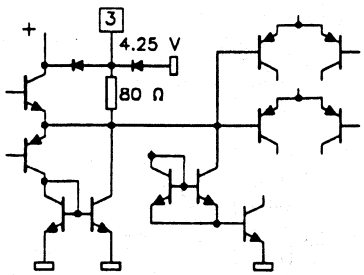
INTERNAL PIN CONFIGURATIONS (pin numbers for SHRDIL-version)



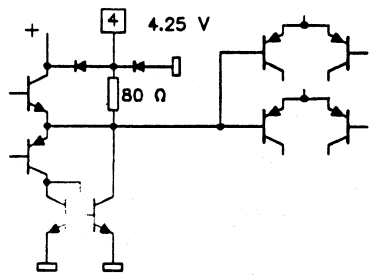
Pin 1: Treble control capacitor, left
Pin 52: Treble control capacitor, right



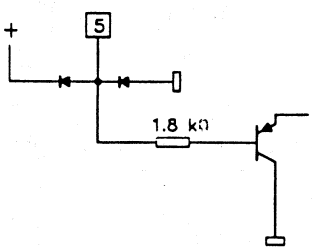
Pin 2: Bass control capacitor input, left
Pin 51: Bass control capacitor input, right



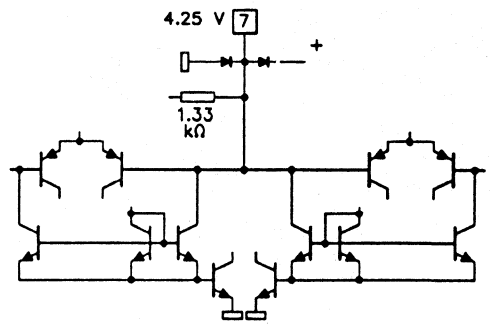
Pin 3: Bass control capacitor output, left
Pin 50: Bass control capacitor output, right



Pin 4: Output subwoofer
Pin 6: Output, left channel
Pin 14: Output selector, left channel
Pin 39: Output selector, right channel
Pin 47: Output, right channel

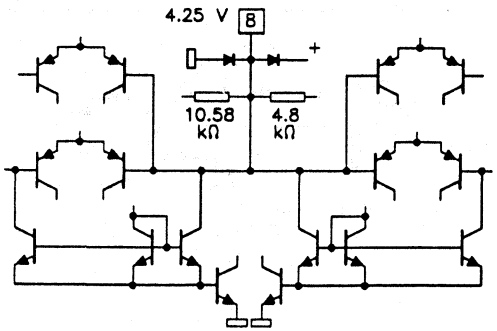


Pin 5: MAD (I²C–bus address switch)

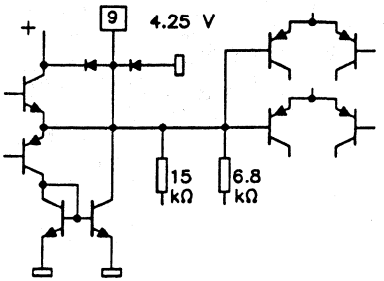


Pin 7: Input loudnes, left
Pin 46: Input loudness, right

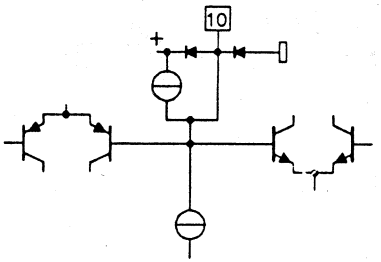
Fig.16 Internal circuits (continued in Fig.17).



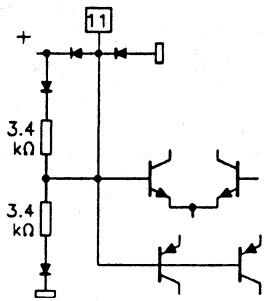
Pin 8: Input volume, left
Pin 45: Input volume, right



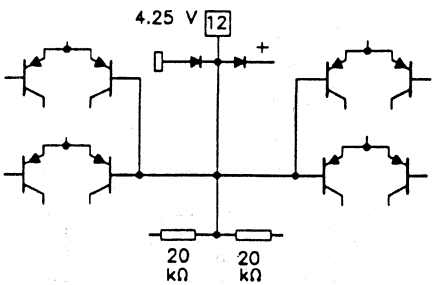
Pin 9: Output effects, left
Pin 44: Output effects, right



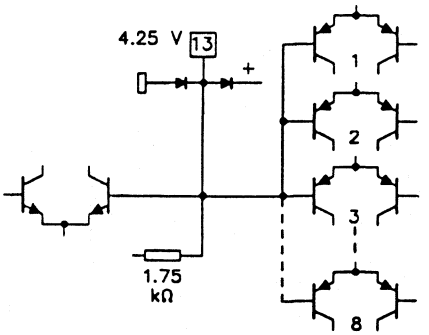
Pin 10: Automatic volume control capacitor



Pin 11: Reference voltage
$0.5 \times V_{CC}$

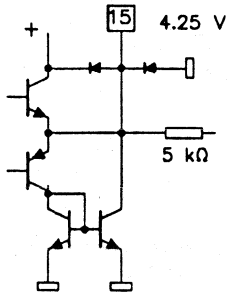


Pin 12: Line input, left
Pin 41: Line input, right

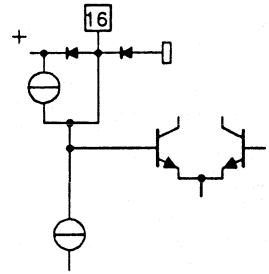


Pin 13: Input automatic volume control, left
Pin 40: Input automatic volume control, right

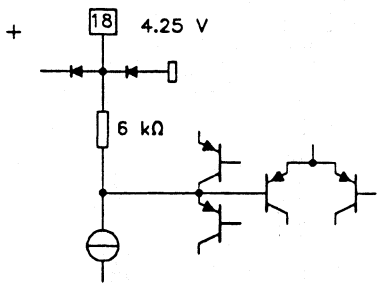
Fig.17 Internal circuits (continued from Fig.16).



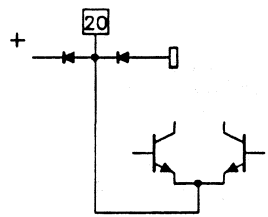
Pin 15: Line output, left
Pin 38: Line output, right



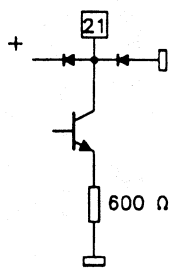
Pin 16: Timing capacitor wideband for DBX
Pin 17: Timing capacitor spectral for DBX



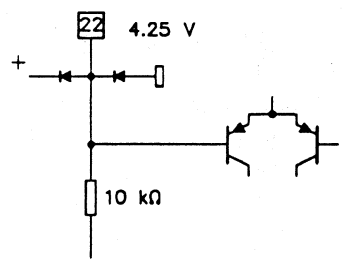
Pin 18: Capacitor wideband for DBX
Pin 19: Capacitor spectral for DBX



Pin 20: Variable emphasis out for DBX

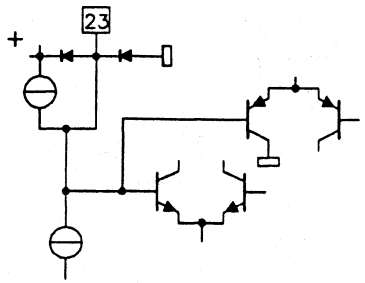


Pin 21: Variable emphasis in for DBX

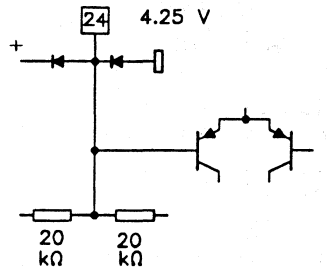


Pin 22: Capacitor noise reduction for DBX

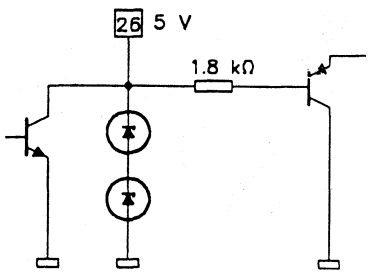
Fig.18 Internal circuits (continued from Fig.17).



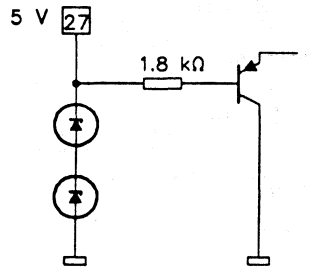
Pin 23: Capacitor mute for SAP



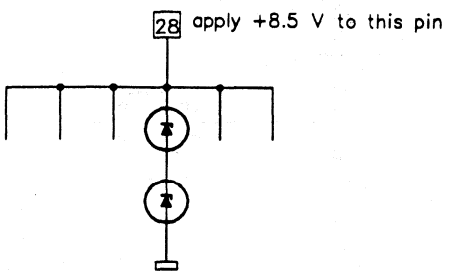
Pin 24: Capacitor DC decoupling for SAP



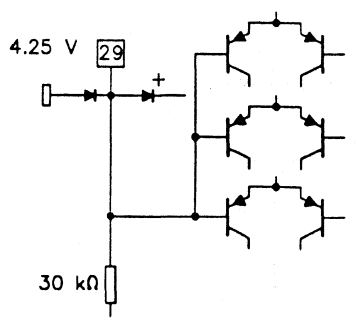
Pin 26: SDA (I²C–bus DATA input/output)



Pin 27: SCL (I²C–bus CLOCK)

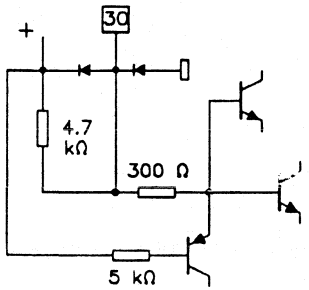


Pin 28: Supply voltage

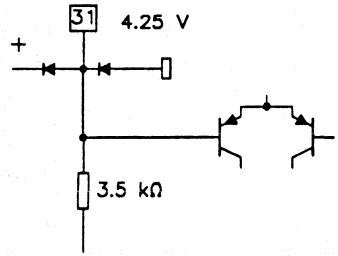


Pin 29: Input composite signal

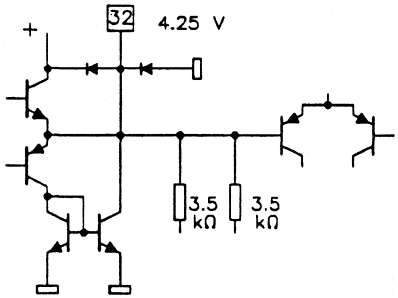
Fig.19 Internal circuits (continued from Fig.18).



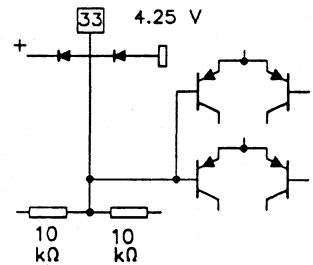
Pin 30: Smoothing capacitor for supply



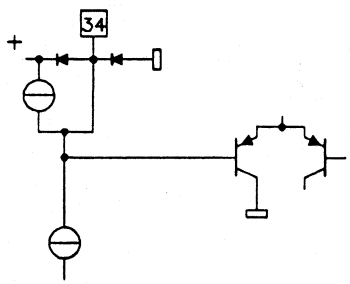
Pin 31: Capacitor for pilot detector



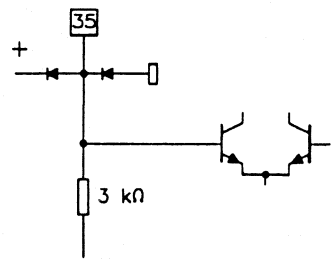
Pin 32: Capacitor for pilot detector



Pin 33: Capacitor for phase detector

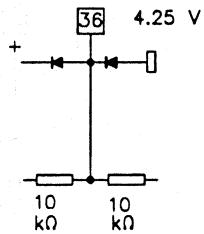


Pin 34: Capacitor for filter adjust

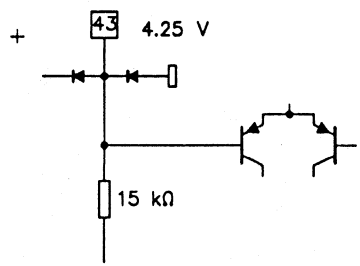


Pin 35: Ceramic resonator

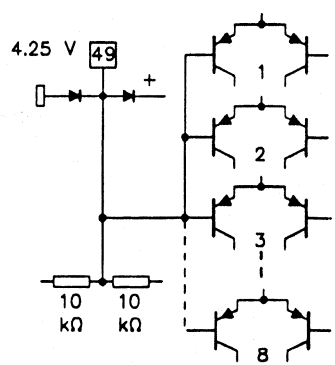
Fig.20 Internal circuits (continued from Fig.19).



Pin 36: Capacitor DC decoupling mono
Pin 37: Capacitor DC decoupling stereo/SAP



Pin 43: Capacitor 1 pseudo function
Pin 42: Capacitor 2 pseudo function



Pin 49: Capacitor subwoofer

Fig.21 Internal circuits (continued from Fig.20).

PLL stereo decoder (BTSC system) TEA5582

GENERAL DESCRIPTION

The TEA5582, a 20-pin integrated phase-locked loop (PLL) stereo decoder, is designed primarily for low cost stereo decoding in a low- to medium-line TV. The MUX input (pin 1) is a low impedance current input, the gain of the input amplifier is therefore determined by the external resistor R1 (see Fig.5). All characteristics are measured with R1 = 47 kΩ. The de-emphasis of (L, R) and (L-R) can be chosen by means of external capacitors and resistors. The supply voltage range of the device is from 7 V to 16 V.

Features

- Wide supply voltage range
- Automatic mono/stereo switching (pilot presence detector)
- LED driver for stereo indicator
- Smooth mono/stereo control
- Matrix and two amplifiers for left and right output signals
- A source selector to switch between the MUX signal and an external signal
- Mute circuit for 60 dB muting of the output level
- External de-emphasis control of (L, R) and (L – R)
- 6 dB fixed attenuation of (L – R) with respect to (L + R) prior to matrix
- All pins are protected against Electrostatic Discharge (ESD)

QUICK REFERENCE DATA

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage range		V_S	7.0	8.5	16	V
Total current consumption	without LED driver	I_{tot}	–	19	25	mA
Decoder						
Overall gain	mono; R1 = 47 kΩ	$G_o(V_o/V_i)$	4	5.8	7	dB
AF output voltage (RMS value)		$V_{14} = V_{15}$	–	245	–	mV
Total harmonic distortion	V_o = 600 mV	THD	–	0.3	–	%
Output channel unbalance		$\lvert V_{14}/V_{15} \rvert$	–	0.1	–	dB
Channel separation	L = 1; R = 0	α	24	28	–	dB
Source selector						
Suppression of MUX signal	$V_6 \geq 2$ V	α	80	90	–	dB
Suppression of external signal	$V_6 \leq 0.8$ V	α	56	60	–	dB
Output amplifiers						
Gain output amplifier						
MUX signal		G_v	6.7	7.2	7.7	dB
external signal		G_v	–0.5	0	+0.5	dB
AF output voltage (RMS value)		$V_{11} = V_{10}$	460	560	640	mV
Mute suppression	$V_7 \leq 0.8$ V					
MUX signal		α	56	60	–	dB
external signal		α	56	60	–	dB

PACKAGE OUTLINE

20-LEAD DIL; PLASTIC (SOT146); SOT146-1; 1996 November 18.

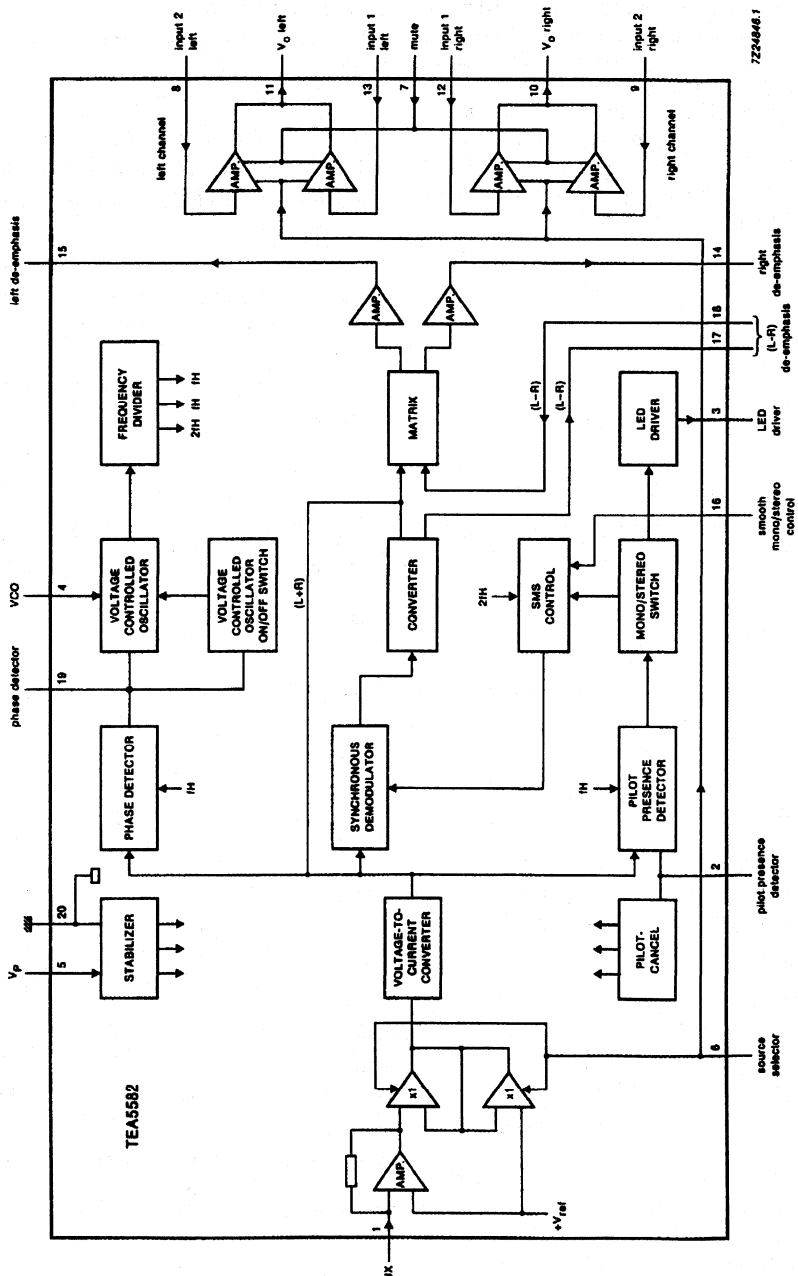


Fig.1 Block diagram.

PINNING

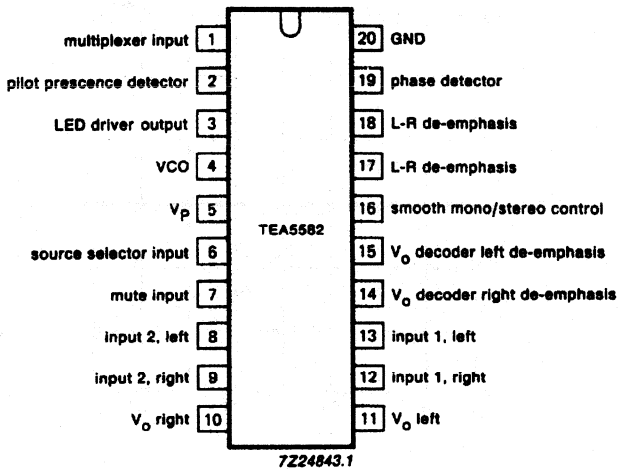


Fig.2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Supply voltage range (pin 5)	V_P	–	18	V
LED-driver current (peak value)	I_3	–	75	mA
Total power dissipation	P_{tot}	see Fig.3		
Storage temperature range	T_{stg}	−65	+150	°C
Operating ambient temperature range	T_{amb}	0	+70	°C
Electrostatic handling[1]	V_{es}	−2	+2	kV

Note

1. ESD withstand voltage is defined by MIL STD 883C (C = 100 pF; R = 1.5 kΩ).

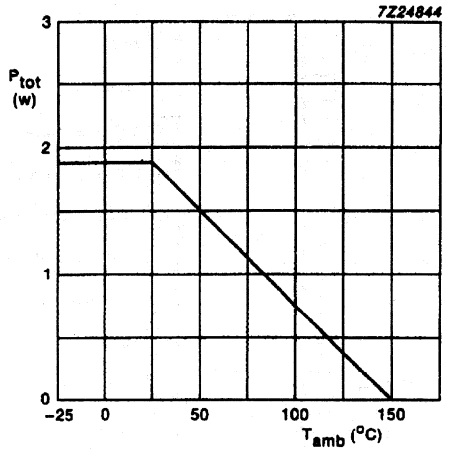


Fig.3 Power derating curve.

DC CHARACTERISTICS

All voltages are with respect to ground (pin 20); all currents are positive into the device; all parameters are measured in the test set-up (see Fig.5) at a nominal supply voltage of V_S = 8.5 V; T_{amb} = 25 °C unless otherwise specified.

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage		V_S	7.0	8.5	16	V
Total current consumption	without LED driver	I_{tot}	–	19	25	mA
Power dissipation		P_{tot}	–	160	–	mW
Voltage						
pin 1		V_1	–	2.1	–	V
pins 8, 9, 10, 11, 12 and 13		$V_8 - V_{13}$	–	4.2	–	V
DC output current						
pins 14 and 15		$-I_{14}, I_{15}$	1.1	1.4	1.8	mA
LED-driver current						
pin 3		I_3	–	–	20	mA
Switch "VCO-OFF"						
voltage	I_{19} = 50 µA	V_{19}	–	2	–	V
Switch "VCO-OFF"						
current		I_{19}	50	–	–	µA

AC CHARACTERISTICS

Measured in the test circuit of Fig.5; V_S = 8.5 V; T_{amb} = 25 °C.
AC conditions: (1) input signal (V_i) of 815 mV p-p for L = 1, R = 1 (mono) f_m = 1 kHz (= 80% modulation). (2) MUX input signal (V_i) of 1.2 V p-p for L = 1, R = 0 and no DBX; f_m = 1 kHz (stereo) and V_{pilot} = 200 mV p-p. (3) S1 open, unless specified (without L–R filter); voltage controlled oscillator (VCO) adjusted to 188.8 kHz at V_i = 0 V; values are measured with an external IF roll-off network (–2 dB at 31.5 kHz = $2f_H$) at the input (dashed components RS and CS in Fig.5).
All the above conditions apply unless otherwise specified.

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Overall performance (V_i to V_o)						
Input current (RMS value)		$I_{I(rms)}$	–	–	12	μA
Overall gain	mono; R1 = 47 kΩ	G_o (V_o/V_i)	4	5.8	7	dB
AF output voltage (mono) (RMS value)		$V_{11} = V_{10}$	460	560	640	mV
AF output voltage (mono) (RMS value)		$V_{15} = V_{14}$	–	245	–	mV
Total harmonic distortion	note 1	THD	–	0.3	0.5	%
Output voltage	THD = 1%	$V_{11} = V_{10}$	–	800	–	mV
Output channel unbalance		$\lvert V_{11}/V_{10} \rvert$	–	0.1	1	dB
Channel separation	L = 1; R = 0	α	24	28	–	dB
Signal-to-noise ratio	bandwidth 20 Hz to 16 kHz	S/N	–	76	–	dB
	bandwidth IEC 79 (curve Din A)	S/N	–	82	–	dB
Pilot presence detector	note 2					
Switching to:						
stereo		V_{pilot}	–	40	60	mV
mono		V_{pilot}	15	30	–	mV
hysteresis		ΔV_{pilot}	–	2.5	–	dB
Smooth mono/stereo control (pin 16)	see Fig.4					
Channel separation (α)						
Full stereo	$V_{16} \geq 1.25$ V	α	24	28	–	dB
Smooth operation	V_{16} = typ. 1 V	α	–	10	–	dB
Full mono	$V_{16} \leq 0.75$ V	α	–	–	1	dB

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Attenuation (L-R)			–	6	–	dB
Carrier and harmonic suppression at the output	note 3					
Pilot signal suppression	f_{pilot} = 15.734 kHz (1 fH)	αfH	32	36	–	dB
Subcarrier suppression f = 2 fH		α2fH	–	60	–	dB
VCO suppression f = 12fH		α12fH	–	75	–	dB
SAP signal suppression (Second Audio Programme) f = 5fH		α5fH	–	60	–	dB
Intermodulation suppression	note 4					
f_m = 8.367 kHz	spurious signal f_s = 1 kHz	α2	–	60	–	dB
f_m = 10.823 kHz	spurious signal f_s = 1 kHz	α3	–	70	–	dB
Ripple rejection	f = 120 Hz; V_{ripple} = 100 mV; mono	RR_{120}	–	50	–	dB
VCO						
R adjust (R5)	f_{OSC} = 188.808 kHz R7 = 10 kΩ 5% C6 = 820 pF 1%	R_{adj}	0	–	8	kΩ
Capture range	deviation from f_{OSC} centre frequency; V_{pilot} = 200 mV p-p	Δf/f	–	4.5	–	%
Temperature coefficient	uncompensated	TC	–	250 × 10^{-6}	–	K^{-1}
Output amplifiers						
Gain						
MUX signal		G_v	6.7	7.2	7.7	dB
external signal		G_v	–0.5	0	+0.5	dB
Input impedance		Z_i	–	50	–	kΩ
Output impedance		Z_o	–	10	–	Ω
External load impedance		Z_1	10	–	–	kΩ
External load capacitance		Z_1	–	–	1.5	nF
Mute suppression	$V_7 \leq 0.8$ V					
MUX signal		α	56	60	–	dB
external signal		α	56	60	–	dB

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
DC offset voltage at outputs	mute OFF-to-ON	ΔV	–	10	50	mV
	mute ON-to-OFF	ΔV	–	10	50	mV
Source selector (pin 6)						
Suppression of MUX signal	$V_6 \geq 2$ V	α	80	90	–	dB
Suppression of external signal	$V_6 \leq 0.8$ V	α	56	60	–	dB
Switching level	MUX selected					
voltage		V_{IL}	–	–	0.8	V
current	$V_I = 0.8$ V	I_{IL}	–	10	25	µA
Switching level	external selected					
voltage		V_{IH}	2	–	V_P	V
current	$V_I = V_P$	I_{IH}	–	0.1	1	µA
Muting circuit (pin 7)						
Input voltage	mute ON	V_{IL}	–	–	0.8	V
	mute OFF	V_{IH}	2	–	V_P	V
Input current	mute ON; $V_{IL} = 0.8$ V	$-I_{IL}$	–	10	25	µA
	mute OFF; $V_{IH} = V_P$	I_{IL}	–	0.1	1	µA

Notes

1. Guaranteed for mono, mono + pilot and stereo.
2. Adjustable.
3. S1 closed; reference: AF output voltage f = 1 kHz (mono).
4. Intermodulation suppression (Beat-Frequency Components (BFC)):

$$\alpha_2 = \frac{V_{o\,(signal)}\ (\text{at } 1\text{ kHz})}{V_{o\,(spurious)}\ (\text{at } 1\text{ kHz})};\ f_s = (2 \times 8.367\text{ kHz}) - fH$$

$$\alpha_3 = \frac{V_{o\,(signal)}\ (\text{at } 1\text{ kHz})}{V_{o\,(spurious)}\ (\text{at } 1\text{ kHz})};\ f_s = (3 \times 10.823\text{ kHz}) - 2fH$$

measured with 100% modulated input signal: L = R; pilot signal = 200 mV p-p; f_m = 8.367 or 10.823 kHz.

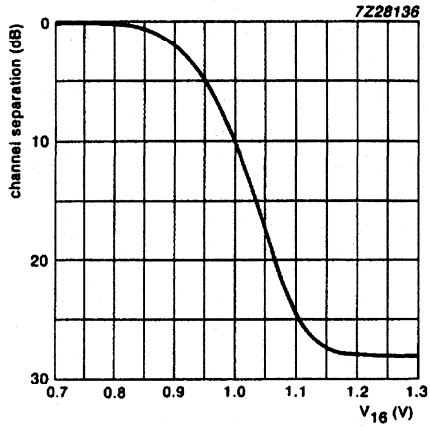


Fig.4 Smooth mono/stereo control.

Sound fader control circuit

TEA6300
TEA6300T

GENERAL DESCRIPTION

The Sound Fader Control circuit (SOFAC) is an I²C-bus controlled preamplifier for car radios.

Features

- Source selector for three stereo inputs
- Inputs and outputs for noise reduction circuits
- Volume and balance control; control range of 86 dB in steps of 2 dB
- Bass and treble control from + 15 dB (treble 12 dB) to −12 dB in steps of 3 dB
- Fader control from 0 dB to −30 dB in steps of 2 dB
- Fast muting
- Low noise suitable for DOLBY* B and C NR (noise reduction)
- Signal handling suitable for compact disc
- I²C-bus control for all functions
- ESD protected

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply voltage	7,0	8,5	13,2	V
$V_{i(rms)}$	Input sensitivity for full power at the output stage	–	50	–	mV
$V_{i(rms)}$	Input signal handling	–	1,65	–	V
f_r	Frequency response	35	–	20 000	Hz
α_{CS}	Channel separation; f = 250 Hz to 10 kHz	70	92	–	dB
THD	Total harmonic distortion	–	0,05	–	%
(S+N)/N	Signal plus noise-to-noise ratio	–	80	–	dB
T_{amb}	Operating ambient temperature range	−40	–	+ 85	°C

* Dolby is a registered trademark of Dolby Laboratories Licensing Corporation, San Francisco, California (U.S.A.).

PACKAGE OUTLINES

28-lead dual in-line; plastic (SOT117); SOT117-1; 1996 August 15.

28-lead mini-pack; plastic (SO28; SOT136A); SOT136-1; 1996 August 15.

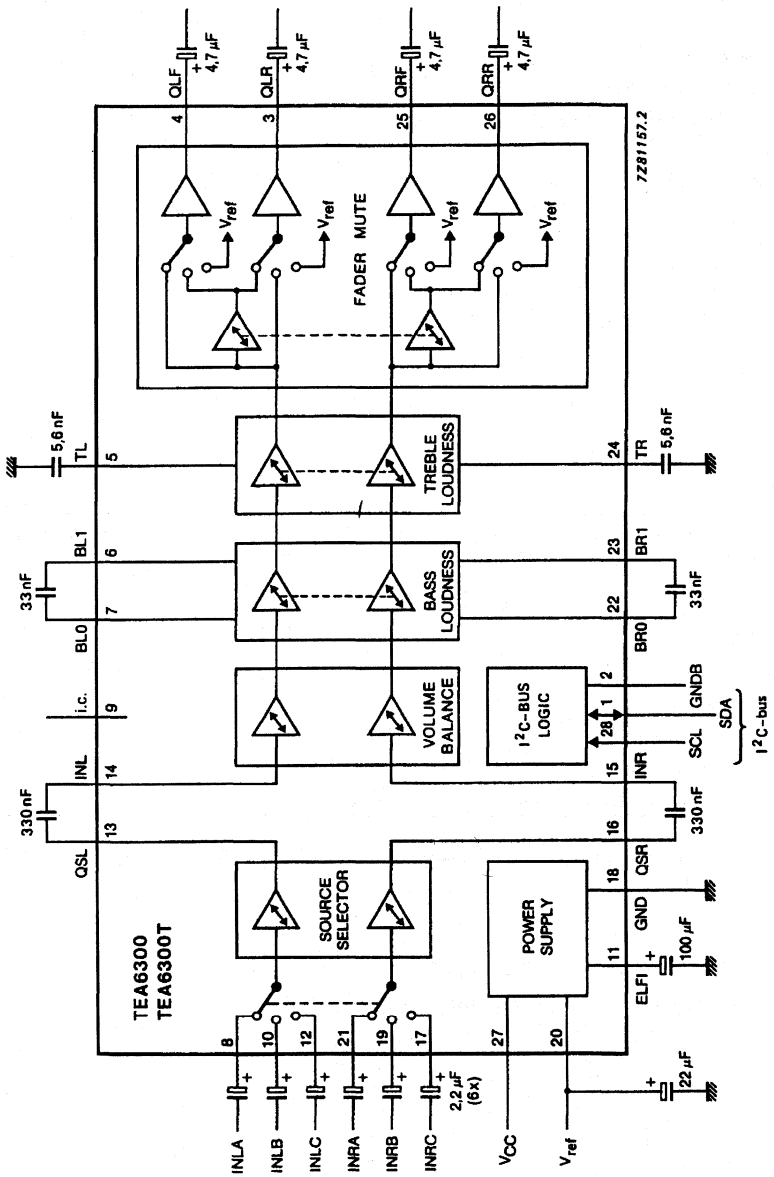


Fig.1 Block diagram.

PINNING

1	SDA	serial data input/output (I^2C-bus)
2	GNDB	ground for I^2C-bus terminals
3	QLR	output left rear
4	QLF	output left front
5	TL	treble control capacitor; left channel
6	BL1	bass control capacitor; left channel
7	BL0	bass control capacitor; left channel
8	INLA	input left source A
9	i.c.	internally connected
10	INLB	input left source B
11	ELFI	electronic filtering for supply
12	INLC	input left source C
13	QSL	output source selector left
14	INL	input left control part
15	INR	input right control part
16	QSR	output source selector right
17	INRC	input right source C
18	GND	ground
19	INRB	input right source B
20	V_{ref}	reference voltage (1/2 V_{CC})
21	INRA	input right source A
22	BRO	bass control capacitor; right channel
23	BR1	bass control capacitor; right channel
24	TR	treble control capacitor; right channel
25	QRF	output right front
26	QRR	output right rear
27	V_{CC}	supply voltage
28	SCL	serial clock input (I^2 C-bus)

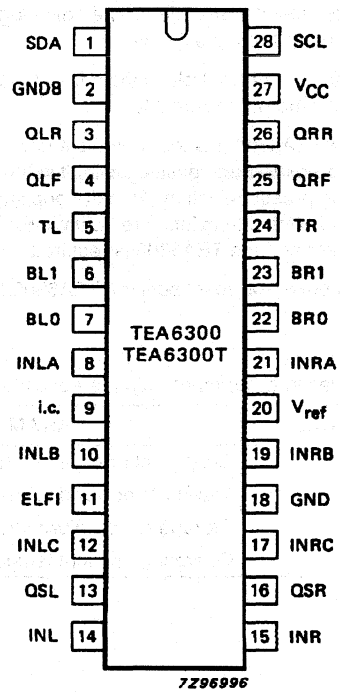


Fig.2 Pinning diagram.

FUNCTIONAL DESCRIPTION

The source selector selects three stereo channels –RF part (AM/FM), recorder and compact disc. As the outputs of the source selector and the inputs of the main control part are available, additional circuits such as compander and equalizer systems may be inserted into the signal path. The AC signal setting is performed by resistor chains in combination with multi-input operational amplifiers. The advantage of this principle is the combination of low noise, low distortion and a high dynamic range for the circuit.

The separate volume controls of the left and the right channel facilitate correct balance control. The range and balance control is software programmable.

Because the TEA6300 has four outputs a low-level fader is included. The fader control is independent of the volume control and an extra mute position is built in for the front, the rear or for all channels. The last function may be used for muting during preset selection. An extra pop suppression circuit is built in for pop-free switching on and off. As all switching and control functions are controllable via the two-wire I^2C-bus, no external interface between the microcomputer and the TEA6300 is required.

The on-chip power-on-reset sets the TEA6300 to the general mute mode.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	Supply voltage (pin 27-18)	–	16	V
P_{tot}	Maximum power dissipation	–	1	W
T_{stg}	Storage temperature range	–55	+150	°C
T_{amb}	Operating ambient temperature range	–40	+ 85	°C

CHARACTERISTICS

V_{CC} = 8,5 V; R_S = 600 Ω; R_L = 10 kΩ; f = 1 kHz; T_{amb} = 25 °C; test circuit Fig.10; unless otherwise specified

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply voltage	7,0	8,5	13,2	V
I_{CC}	Supply current	–	26	–	mA
I_{CC}	Supply current at 8,5 V	–	–	33	mA
I_{CC}	Supply current at 13,2 V	–	–	44	mA
	DC voltage				
V_{DC}	inputs, outputs and reference	0,45	0,5	0,55	V_{CC}
	Internal reference voltage (pin 20)				
V_{REF}	V_{ref} = 0,5 V_{CC}	–	4,25	–	V
	Maximum voltage gain				
G_v	bass and treble linear, fader off	19	20	21	dB
	Output voltage level				
$V_{o(rms)}$	for P_{max} at the output stage	–	500	–	mV
$V_{o(rms)}$	for start of clipping	–	1000	–	mV
	Input sensitivity				
$V_{i(rms)}$	at V_o = 500 mV	–	50	–	mV
	Frequency response				
	bass and treble linear; roll-off				
f_r	frequency –1 dB	35	–	20 000	Hz
	Channel separation				
	G_v = 0 dB; bass and treble linear;				
α_{CS}	frequency range 250 Hz to 10 kHz	70	92	–	dB
	Total harmonic distortion				
	frequency range 20 Hz to 12,5 kHz				
THD	V_i = 50 mV; G_v = 20 dB	–	0,1	0,3	%
THD	V_i = 500 mV; G_v = 0 dB	–	0,05	0,2	%
THD	V_i = 1,6 V; G_v = –10 dB	–	0,2	0,5	%
	Ripple rejection				
	$V_{r(rms)}$ < 200 mV; G_v = 0 dB;				
	bass and treble linear;				
RR_{100}	at f = 100 Hz	–	70	–	dB
RR_{range}	at f = 40 Hz to 12,5 kHz	–	60	–	dB

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
	Signal plus noise-to-noise ratio				
	bass and treble linear; notes 1 and 2				
	CCIR 468-2 weighted; quasi peak				
(S + N)/N	V_i = 50 mV; V_o = 46 mV; P_o = 50 mW	–	65	–	dB
(S + N)/N	V_i = 500 mV; V_o = 45 mV; P_o = 50 mW	–	67	–	dB
(S + N)/N	V_i = 50 mV; V_o = 200 mV; P_o = 1 W	65	70	–	dB
(S + N)/N	V_i = 500 mV; V_o = 200 mV; P_o = 1 W	65	78	–	dB
(S + N)/N	V_i = 50 mV; V_o = 500 mV; P_o = 6 W	–	70	–	dB
(S + N)/N	V_i = 500 mV; V_o = 500 mV; P_o = 6 W	–	85	–	dB
	Noise output power				
	mute position, only contribution of				
P_{no}	TEA6300; power amplifier for 25 W	–	–	10	nW
	Crosstalk (20 log $V_{bus(p-p)}/V_{o(rms)}$)				
	between bus inputs and signal outputs				
α_B	G_V = 0 dB; bass and treble linear	–	110	–	dB
Source selector					
Z_i	Input impedance	20	30	40	kΩ
Z_o	Output impedance	–	–	100	Ω
R_L	Output load resistance	10	–	–	kΩ
C_L	Output load capacity	0	–	200	pF
	Input isolation				
	not selected source; frequency range				
α_S	40 Hz to 12,5 kHz	–	80	–	dB
	Voltage gain				
G_v	$R_L \geq 10$ kΩ	–	0	–	dB
$V_{b\ int}/V_{ref}$	Internal bias voltage ratio	–	1	–	
	Maximum input voltage level (RMS value)				
$V_{i(rms)}$	THD < 0,5%	–	1,65	–	V
$V_{i(rms)}$	THD < 0,5%; V_{CC} = 7,5 V	–	1,5	–	V
	Total harmonic distortion				
THD	V_i = 500 mV; R_L = 10 kΩ	–	–	0,1	%
	Noise output voltage				
V_{no}	weighted CCIR 468-2, quasi peak	–	9	20	μV
	DC offset voltage				
V_o	between any inputs	–	–	10	mV

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Control part					
	Source selector disconnected, source resistance 600 Ω				
Z_i	Input impedance	35	50	65	kΩ
Z_o	Output impedance	–	100	150	Ω
R_L	Output load resistance	5	–	–	kΩ
C_L	Output load capacity	0	–	2500	pF
$V_{i(rms)}$	Maximum input voltage THD < 0,5%; G_v = –10 dB; bass and treble linear	–	2,0	–	V
	Noise output voltage weighted acc CCIR 468-2, quasi-peak, bass and treble linear, fader off				
V_{no}	G_v = 20 dB	–	110	220	μV
V_{no}	G_v = 0 dB	–	25	50	μV
V_{no}	G_v = –66 dB	–	19	38	μV
V_{no}	mute position	–	11	22	μV
Volume control					
G_c	Continuous control range	–	86	–	dB
	Step resolution	–	2	–	dB
ΔG_a	Attenuator set error (G_v = + 20 to –50 dB)	–	–	2	dB
ΔG_a	Attenuator set error (G_v = + 20 to –66 dB)	–	–	3	dB
ΔG_t	Gain tracking error balance in mid position, bass and treble linear	–	–	2	dB
α_m	Mute attenuation	72	90	–	dB
DC step offset					
	Between any adjoining step and any step to mute				
	G_v = 0 to –66 dB	–	0,2	10	mV
	G_v = 20 to 0 dB	–	2	15	mV
	In any treble and fader position				
	G_v = 0 to –66 dB	–	–	10	mV
	In any bass position				
	G_v = 0 to –66 dB	–	–	20	mV

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Bass control					
	Bass control range				
G_b	f = 40 Hz; maximum boost	14	15	16	dB
G_b	f = 40 Hz; maximum attenuation	11	12	13	dB
	Step resolution	–	3	–	dB
	Step error	–	–	0,5	dB
Treble control					
	Treble control range				
G_t	f = 15 kHz; maximum boost	11	12	13	dB
G_t	f = 15 kHz; maximum attenuation	11	12	13	dB
G_t	f > 15 kHz; maximum boost	–	–	15	dB
	Step resolution	–	3	–	dB
	Step error	–	–	0,5	dB
Fader control					
	Continuous attenuation				
G_f	fader control range	–	30	–	dB
	Step resolution	–	2	–	dB
	Attenuator set error	–	–	1,5	dB
α_m	Mute attenuation	74	84	–	dB
Digital part					
Bus terminals					
	Input voltage				
V_{IH}	HIGH	3	–	12	V
V_{IL}	LOW	−0,3	–	+ 1,5	V
	Input current				
I_{IH}	HIGH	−10	–	+10	μA
I_{IL}	LOW	−10	–	+10	μA
V_{OL}	Output voltage LOW; I_L = 3 mA	–	–	0,4	V
AC characteristics	In accordance with the I2C-bus specification				
Power-on-Reset					
	When RESET is active the GMU (general mute) bit is set and the I^2C-bus receiver is in RESET position				
	Increasing supply voltage				
V_{CC}	start of reset	–	–	2,5	V
V_{CC}	end of reset	5,2	6,0	6,8	V
V_{CC}	Decreasing supply voltage; start of reset	4,2	5,0	5,8	V

Notes to the characteristics

1. The indicated values for output power assume a 6 W power amplifier with 20 dB gain, connected to the output of the

circuit. Signal-to-noise ratios exclude noise contribution of the power amplifier.

2. Signal-to-noise ratios on a CCIR 468-2 average meter reading are 4,5 dB better than on CCIR 468-2 quasi peak.

I²C-BUS FORMAT

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA	A	P

S	=	start condition	SUBADDRESS	=	see Table 1
SLAVE ADDRESS	=	1000 0000	DATA	=	see Table 1
A	=	acknowledge, generated by the slave	P	=	STOP condition

If more than 1 byte of DATA is transmitted, then auto-increment of the subaddress is performed.

Table 1 I²C-bus; subaddress/data

FUNCTION	SUBADDRESS	DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
volume left	0 0 0 0 0 0 0 0	X	X	VL5	VL4	VL3	VL2	VL1	VL0
volume right	0 0 0 0 0 0 0 1	X	X	VR5	VR4	VR3	VR2	VR1	VR0
bass	0 0 0 0 0 0 1 0	X	X	X	X	BA3	BA2	BA1	BA0
treble	0 0 0 0 0 0 1 1	X	X	X	X	TR3	TR2	TR1	TR0
fader	0 0 0 0 0 1 0 0	X	X	MFN	FCH	FA3	FA2	FA1	FA0
switch	0 0 0 0 0 1 0 1	GMU	X	X	X	X	SCC	SCB	SCA

Function of the bits:

VL0 to VL5	volume control left
VR0 to VR5	volume control right
BA0 to BA3	bass control
TR0 to TR3	treble control
FA0 to FA3	fader control
FCH	select fader channel (front or rear)
MFN	mute control of the selected fader channel (front or rear)
SCA to SCC	source selector control
GMU	mute control (general mute) for the outputs QLF, QLR, QRF and QRR
X	don't care bits (logic 1 during testing)

Table 2 Bass setting

G_V	DATA			
DB	BA3	BA2	BA1	BA0
+15	1	1	1	1
+15	1	1	1	0
+15	1	1	0	1
+15	1	1	0	0
+12	1	0	1	1
+ 9	1	0	1	0
+ 6	1	0	0	1
+ 3	1	0	0	0
0	0	1	1	1
− 3	0	1	1	0
− 6	0	1	0	1
− 9	0	1	0	0
−12	0	0	1	1
−12	0	0	1	0
−12	0	0	0	1
−12	0	0	0	0

Table 3 Treble setting

G_V	DATA			
DB	TR3	TR2	TR1	TR0
+12	1	1	1	1
+12	1	1	1	0
+12	1	1	0	1
+12	1	1	0	0
+12	1	0	1	1
+ 9	1	0	1	0
+ 6	1	0	0	1
+ 3	1	0	0	0
0	0	1	1	1
− 3	0	1	1	0
− 6	0	1	0	1
− 9	0	1	0	0
−12	0	0	1	1
−12	0	0	1	0
−12	0	0	0	1
−12	0	0	0	0

Table 4 Volume setting LEFT

G_V	DATA					
DB	VL5	VL4	VL3	VL2	VL1	VL0
20	1	1	1	1	1	1
18	1	1	1	1	1	0
16	1	1	1	1	0	1
14	1	1	1	1	0	0
12	1	1	1	0	1	1
10	1	1	1	0	1	0
8	1	1	1	0	0	1
6	1	1	1	0	0	0
4	1	1	0	1	1	1
2	1	1	0	1	1	0
0	1	1	0	1	0	1
− 2	1	1	0	1	0	0
− 4	1	1	0	0	1	1
− 6	1	1	0	0	1	0
− 8	1	1	0	0	0	1
−10	1	1	0	0	0	0
−12	1	0	1	1	1	1
−14	1	0	1	1	1	0
−16	1	0	1	1	0	1
−18	1	0	1	1	0	0
−20	1	0	1	0	1	1
−22	1	0	1	0	1	0
−24	1	0	1	0	0	1
−26	1	0	1	0	0	0
−28	1	0	0	1	1	1

G_V	DATA					
DB	VL5	VL4	VL3	VL2	VL1	VL0
−30	1	0	0	1	1	0
−32	1	0	0	1	0	1
−34	1	0	0	1	0	0
−36	1	0	0	0	1	1
−38	1	0	0	0	1	0
−40	1	0	0	0	0	1
−42	1	0	0	0	0	0
−44	0	1	1	1	1	1
−46	0	1	1	1	1	0
−48	0	1	1	1	0	1
−50	0	1	1	1	0	0
−52	0	1	1	0	1	1
−54	0	1	1	0	1	0
−56	0	1	1	0	0	1
−58	0	1	1	0	0	0
−60	0	1	0	1	1	1
−62	0	1	0	1	1	0
−64	0	1	0	1	0	1
−66	0	1	0	1	0	0
mute left	0	1	0	0	1	1
mute left	0	1	0	0	1	0
.				.		
.				.		
.				.		
mute left	0	0	0	0	0	0

Table 5 Volume setting RIGHT

G_V	DATA					
DB	VR5	VR4	VR3	VR2	VR1	VR0
20	1	1	1	1	1	1
18	1	1	1	1	1	0
16	1	1	1	1	0	1
14	1	1	1	1	0	0
12	1	1	1	0	1	1
10	1	1	1	0	1	0
8	1	1	1	0	0	1
6	1	1	1	0	0	0
4	1	1	0	1	1	1
2	1	1	0	1	1	0
0	1	1	0	1	0	1
− 2	1	1	0	1	0	0
− 4	1	1	0	0	1	1
− 6	1	1	0	0	1	0
− 8	1	1	0	0	0	1
−10	1	1	0	0	0	0
−12	1	0	1	1	1	1
−14	1	0	1	1	1	0
−16	1	0	1	1	0	1
−18	1	0	1	1	0	0
−20	1	0	1	0	1	1
−22	1	0	1	0	1	0
−24	1	0	1	0	0	1
−26	1	0	1	0	0	0
−28	1	0	0	1	1	1

G_V	DATA					
DB	VR5	VR4	VR3	VR2	VR1	VR0
−30	1	0	0	1	1	0
−32	1	0	0	1	0	1
−34	1	0	0	1	0	0
−36	1	0	0	0	1	1
−38	1	0	0	0	1	0
−40	1	0	0	0	0	1
−42	1	0	0	0	0	0
−44	0	1	1	1	1	1
−46	0	1	1	1	1	0
−48	0	1	1	1	0	1
−50	0	1	1	1	0	0
−52	0	1	1	0	1	1
−54	0	1	1	0	1	0
−56	0	1	1	0	0	1
−58	0	1	1	0	0	0
−60	0	1	0	1	1	1
−62	0	1	0	1	1	0
−64	0	1	0	1	0	1
−66	0	1	0	1	0	0
mute right	0	1	0	0	1	1
mute right	0	1	0	0	1	0
.				.		
.				.		
.				.		
mute right	0	0	0	0	0	0

Table 6 Fader function

SETTING		DATA					
FRONT	REAR						
DB	DB	MFN	FCH	FA3	FA2	FA1	FA0
		fader off					
0	0	1	1	1	1	1	1
0	0	0	1	1	1	1	1
		fader front					
− 2	0	1	1	1	1	1	0
− 4	0	1	1	1	1	0	1
− 6	0	1	1	1	1	0	0
− 8	0	1	1	1	0	1	1
−10	0	1	1	1	0	1	0
−12	0	1	1	1	0	0	1
−14	0	1	1	1	0	0	0
−16	0	1	1	0	1	1	1
−18	0	1	1	0	1	1	0
−20	0	1	1	0	1	0	1
−22	0	1	1	0	1	0	0
−24	0	1	1	0	0	1	1
−26	0	1	1	0	0	1	0
−28	0	1	1	0	0	0	1
−30	0	1	1	0	0	0	0
		mute front					
−80	0	0	1	1	1	1	0
.	.			.			
.	.			.			
.	.			.			
−80	0	0	1	0	0	0	0

SETTING		DATA					
FRONT	REAR						
DB	DB	MFN	FCH	FA3	FA2	FA1	FA0
		fader off					
0	0	1	0	1	1	1	1
0	0	0	0	1	1	1	1
		fader rear					
0	− 2	1	0	1	1	1	0
0	− 4	1	0	1	1	0	1
0	− 6	1	0	1	1	0	0
0	− 8	1	0	1	0	1	1
0	−10	1	0	1	0	1	0
0	−12	1	0	1	0	0	1
0	−14	1	0	1	0	0	0
0	−16	1	0	0	1	1	1
0	−18	1	0	0	1	1	0
0	−20	1	0	0	1	0	1
0	−22	1	0	0	1	0	0
0	−24	1	0	0	0	1	1
0	−26	1	0	0	0	1	0
0	−28	1	0	0	0	0	1
0	−30	1	0	0	0	0	0
		mute rear					
0	−80	0	0	1	1	1	0
.	.			.			
.	.			.			
.	.			.			
0	−80	0	0	0	0	0	0

Table 7 Selected inputs

SELECTED INPUTS	DATA		
	SCC	SCB	SCA
data not allowed	1	1	1
data not allowed	1	1	0
data not allowed	1	0	1
INLC, INRC	1	0	0
data not allowed	0	1	1
INLB, INRB	0	1	0
INLA, INRA	0	0	1
data not allowed	0	0	0

Table 8 Mute control

MUTE CONTROL	DATA GMU	REMARKS
active	1	outputs QLF, QLR QRF and QRR are muted
passive	0	no general mute

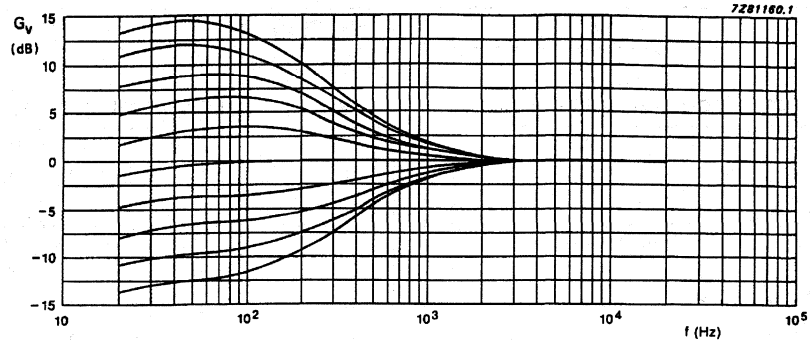


Fig.3 Bass control without T-pass filter.

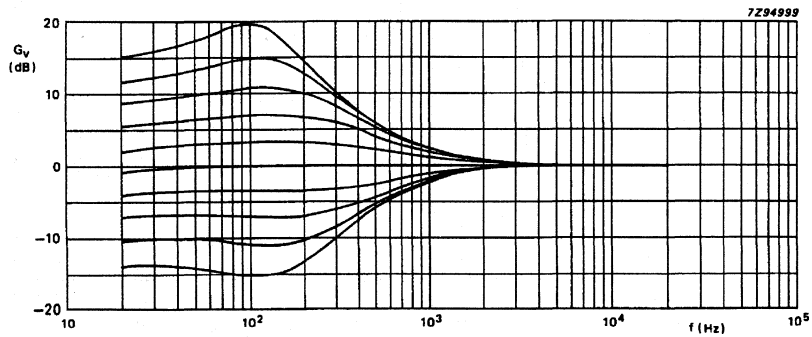
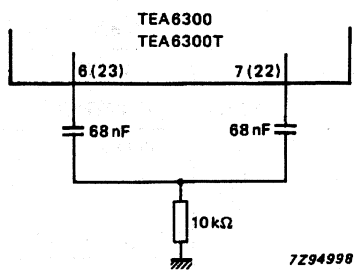


Fig.4 Bass control with T-pass filter.



Pin numbers in parentheses refer to the bass control, right channel.

Fig.5 T-pass filter.

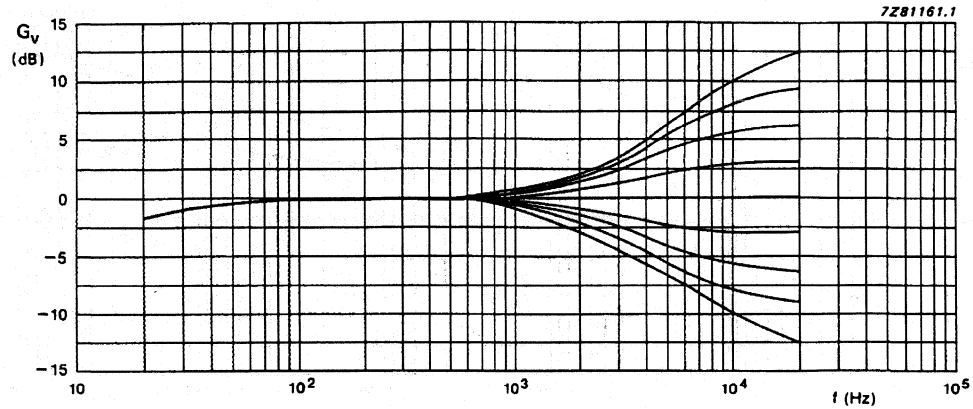


Fig.6 Treble control.

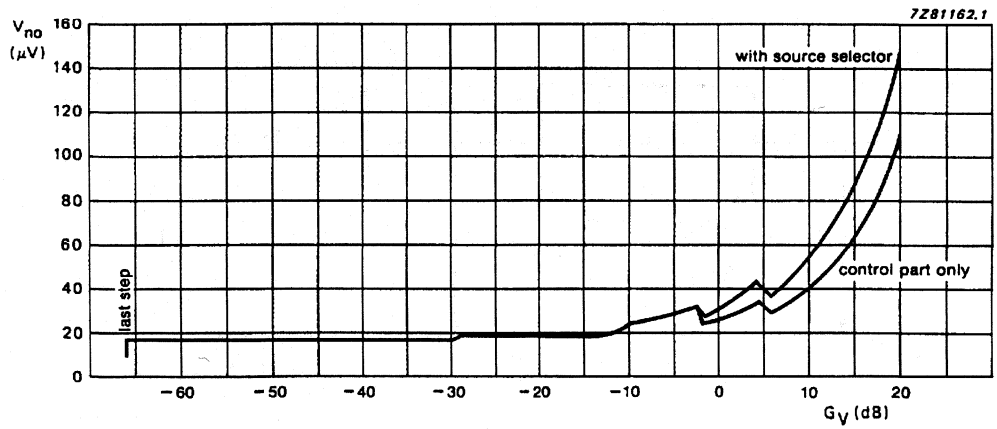


Fig.7 Output noise voltage (CCIR 468-2 weighted: quasi peak).

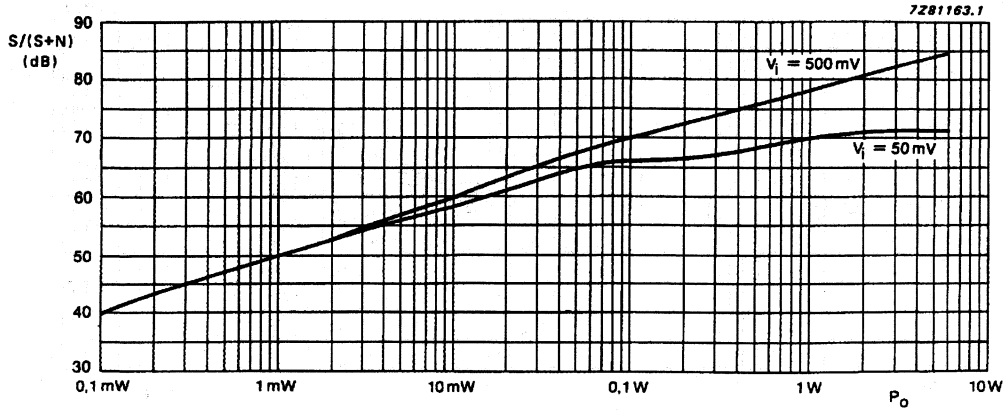


Fig.8 Signal-to-noise ratio (CCIT 468-2 weighted; quasi peak) with a 6 W power amplifier (gain 20 dB) without noise contribution of the power amplifier (see Fig.9).

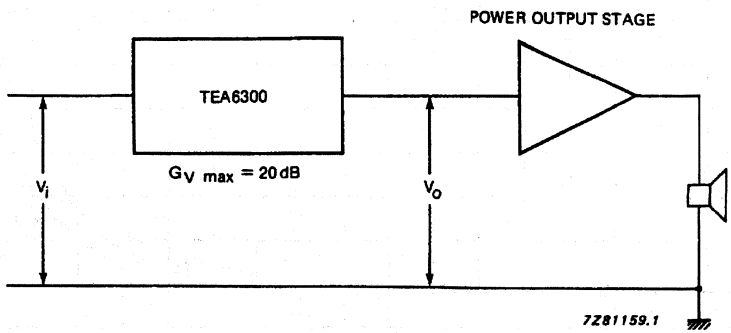


Fig.9 Recommended level diagram; $V_{i\,min}$ = 50 mV, V_o = 500 mV for P_{max}.

APPLICATION INFORMATION

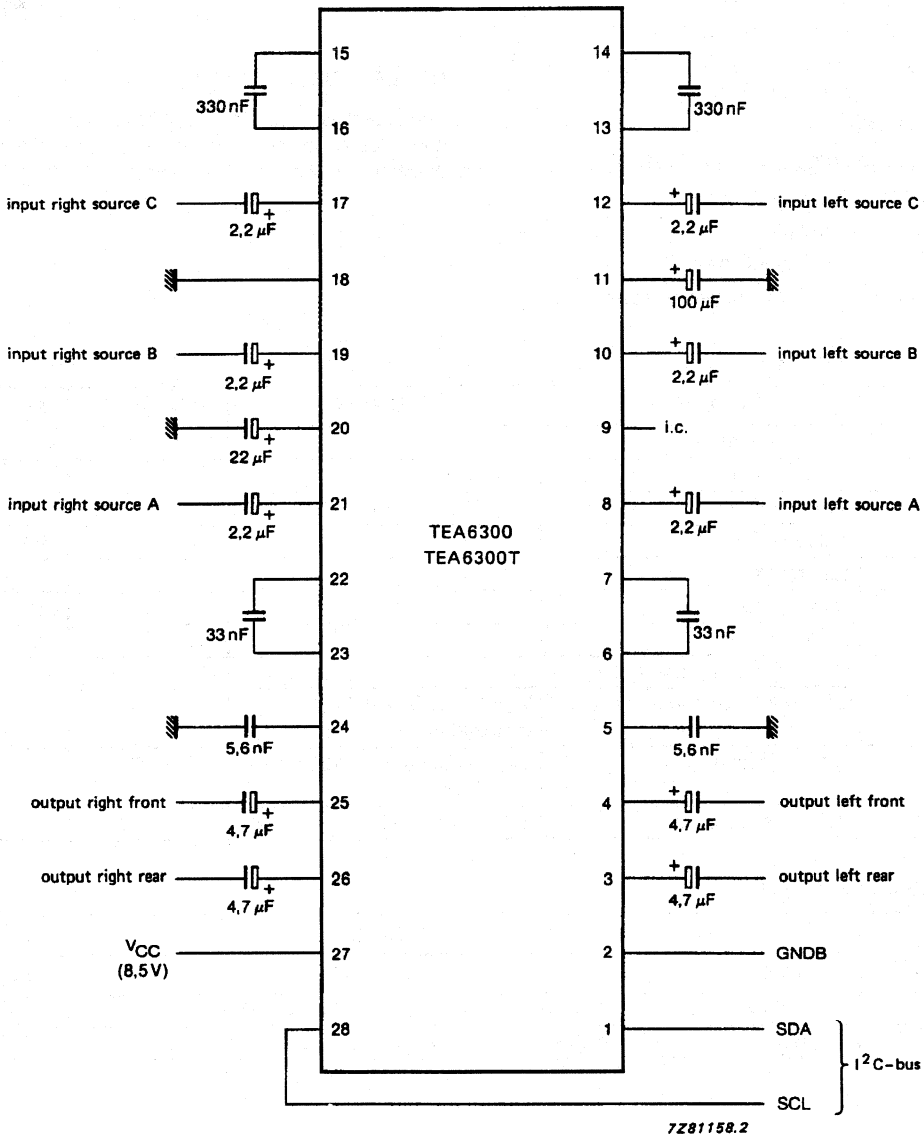


Fig.10 Test and application circuit.

Sound fader control circuit TEA6320

FEATURES

- Source selector for four stereo and one mono inputs
- Interface for noise reduction circuits
- Interface for external equalizer
- Volume, balance and fader control
- Special loudness characteristic automatically controlled in combination with volume setting
- Bass and treble control
- Mute control at audio signal zero crossing
- Fast mute control via I²C-bus
- Fast mute control via pin
- I²C-bus control for all functions
- Power supply with internal power-on reset.

GENERAL DESCRIPTION

The sound fader control circuit TEA6320 is an I²C-bus controlled stereo preamplifier for car radio hi-fi sound applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		7.5	8.5	9.5	V
I_{CC}	supply current	V_{CC} = 8.5 V	–	26	–	mA
$V_{o(rms)}$	maximum output voltage level	V_{CC} = 8.5 V; THD ≤ 0.1%	–	2000	–	mV
G_v	voltage gain		−86	–	+20	dB
$G_{step(vol)}$	step resolution (volume)		–	1	–	dB
G_{bass}	bass control		−15	–	+15	dB
G_{treble}	treble control		−12	–	+12	dB
$G_{step(treble)}$	step resolution (bass, treble)		–	1.5	–	dB
(S+N)/N	signal-plus-noise to noise ratio	V_O = 2.0 V; G_v = 0 dB; unweighted	–	105	–	dB
RR_{100}	ripple rejection	$V_{r(rms)}$ < 200 mV; f = 100 Hz; G_v = 0 dB	–	76	–	dB
α_{cs}	channel separation	250 Hz ≤ f ≤ 10 kHz; G_v = 0 dB	90	96	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA6320	SDIP32	plastic shrink dual in-line package; 32 leads (400 mil)	SOT232-1
TEA6320T	SO32	plastic small outline package; 32 leads; body width 7.5 mm	SOT287-1

BLOCK DIAGRAM

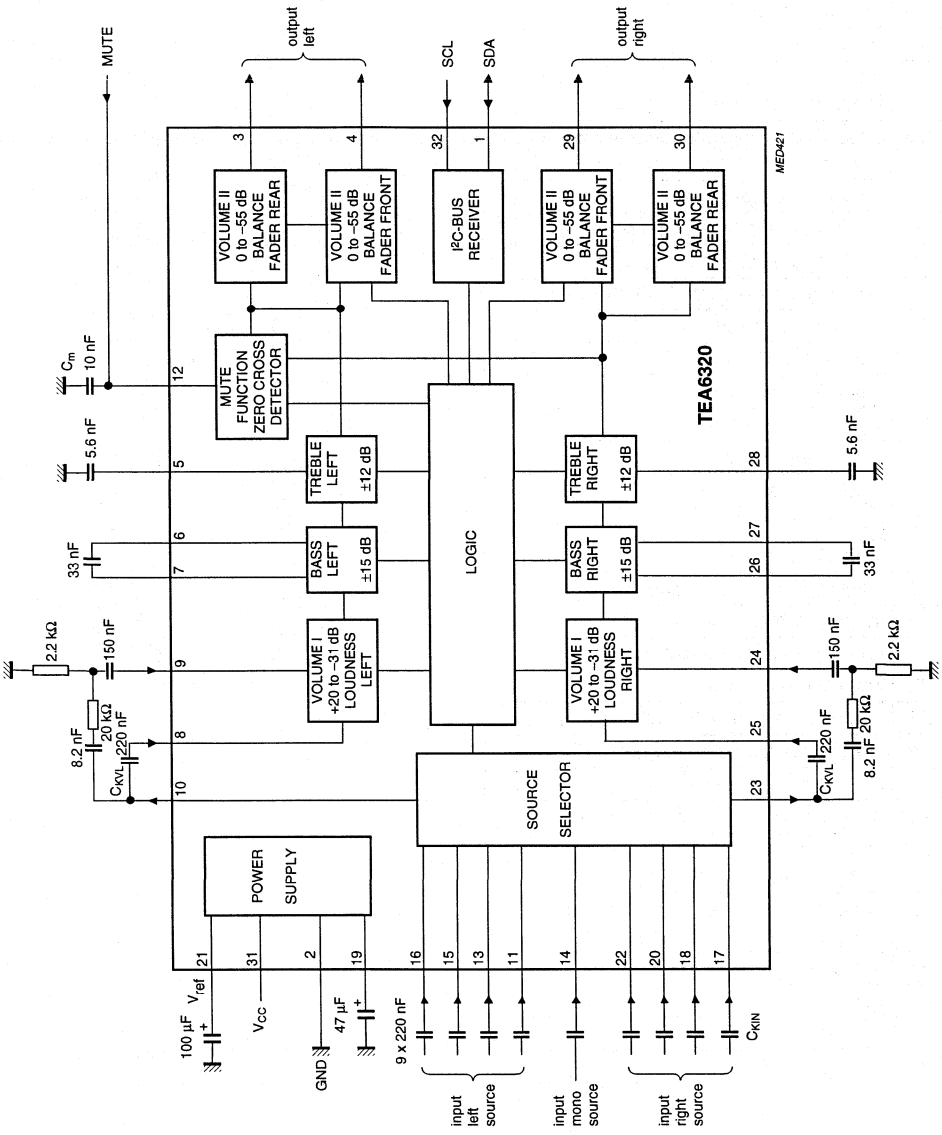


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SDA	1	serial data input/output
GND	2	ground
OUTLR	3	output left rear
OUTLF	4	output left front
TL	5	treble control capacitor left channel or input from an external equalizer
B2L	6	bass control capacitor left channel or output to an external equalizer
B1L	7	bass control capacitor, left channel
IVL	8	input volume I, left control part
ILL	9	input loudness, left control part
QSL	10	output source selector, left channel
IDL	11	input D left source
MUTE	12	mute control
ICL	13	input C left source
IMO	14	input mono source
IBL	15	input B left source
IAL	16	input A left source
IAR	17	input A right source
IBR	18	input B right source
CAP	19	electronic filtering for supply
ICR	20	input C right source
V_{ref}	21	reference voltage ($0.5V_{CC}$)
IDR	22	input D right source
QSR	23	output source selector right channel
ILR	24	input loudness right channel
IVR	25	input volume I, right control part
B1R	26	bass control capacitor right channel
B2R	27	bass control capacitor right channel or output to an external equalizer
TR	28	treble control capacitor right channel or input from an external equalizer
OUTRF	29	output right front
OUTRR	30	output right rear
V_{CC}	31	supply voltage
SCL	32	serial clock input

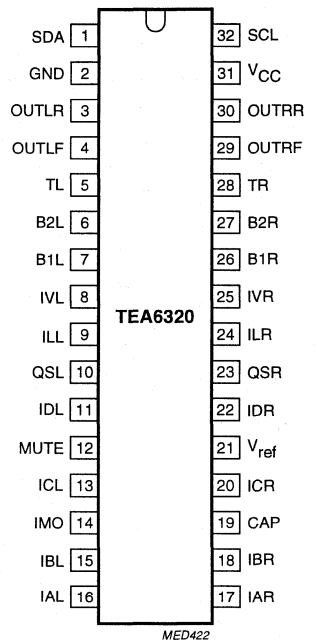


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The source selector selects one of 4 stereo inputs or the mono input. The maximum input signal voltage is $V_{i(rms)}$ = 2 V. The outputs of the source selector and the inputs of the following volume control parts are available at pins 8 and 10 for the left channel and pins 23 and 25 for the right channel. This offers the possibility of interfacing a noise reduction system.

The volume control function is split into two sections: volume I control block and volume II control block.

The control range of volume I is between +20 dB and −31 dB in steps of 1 dB. The volume II control range is between 0 dB and −55 dB in steps of 1 dB. Although the theoretical possible control range is 106 dB (+20 to −86 dB), in practice a range of 86 dB (+20 to −66 dB) is recommended. The gain/attenuation setting of the volume I control block is common for both channels.

The volume I control block operates in combination with the loudness control. The filter is linear when the maximum gain for the volume I control (+20 dB) is selected. The filter characteristic increases automatically over a range of 32 dB down to a setting of −12 dB. That means the maximum filter characteristic is obtained at −12 dB setting of volume I. Further reduction of the volume does not further influence the filter characteristic (see Fig.5). The maximum selected filter characteristic is determined by external components. The proposed application gives a maximum boost of 17 dB for bass and 4.5 dB for treble. The loudness may be switched on or off via I²C-bus control (see Table 7).

The volume I control block is followed by the bass control block. A single external capacitor of 33 nF for each channel in combination with internal resistors, provides the frequency response of the bass control (see Fig.3). The adjustable range is between −15 and +15 dB at 40 Hz.

Both loudness and bass control result in a maximum bass boost of 32 dB for low volume settings.

The treble control block offers a control range between −12 and +12 dB in steps of 1.5 dB at 15 kHz. The filter characteristic is determined by a single capacitor of 5.6 nF for each channel in combination with internal resistors (see Fig.4).

The basic step width of bass and treble control is 3 dB. The intermediate steps are obtained by switching 1.5 dB boost and 1.5 dB attenuation steps.

The bass and treble control functions can be switched off via I²C-bus. In this event the internal signal flow is disconnected. The connections B2L and B2R are outputs and TL and TR are inputs for inserting an external equalizer.

The last section of the circuit is the volume II block. The balance and fader functions are performed using the same control blocks. This is realized by 4 independently controllable attenuators, one for each output. The control range of these attenuators is 55 dB in steps of 1 dB with an additional mute step.

The circuit provides 3 mute modes:

1. Zero crossing mode mute via I²C-bus using 2 independent zero crossing detectors (ZCM, see Tables 2 and 9 and Fig.16).
2. Fast mute via MUTE pin (see Fig.10).
3. Fast mute via I²C-bus either by general mute (GMU, see Tables 2 and 9) or volume II block setting (see Table 4).

The mute function is performed immediately if ZCM is cleared (ZCM = 0). If the bit is set (ZCM = 1) the mute is activated after changing the GMU bit. The actual mute switching is delayed until the next zero crossing of the audio frequency signal. As the two audio channels (left and right) are independent, two comparators are built-in to control independent mute switches.

To avoid a large delay of mute switching when very low frequencies are processed, the maximum delay time is limited to typically 100 ms by an integrated timing circuit and an external capacitor (C_m = 10 nF, see Fig.10). This timing circuit is triggered by reception of a new data word for the switch function which includes the GMU bit. After a discharge and charge period of an external capacitor the muting switch follows the GMU bit if no zero crossing was detected during that time.

The mute function can also be controlled externally. If the mute pin is switched to ground all outputs are muted immediately (hardware mute). This mute request overwrites all mute controls via the I²C-bus for the time the pin is held LOW. The hardware mute position is not stored in the TEA6320.

For the turn on/off behaviour the following explanation is generally valid. To avoid AF output caused by the input signal coming from preceding stages, which produces output during drop of V_{CC}, the mute has to be set, before the V_{CC} will drop. This can be achieved by I²C-bus control or by grounding the MUTE pin.

For use where is no mute in the application before turn off, a supply voltage drop of more than $1 \times V_{BE}$ will result in a mute during the voltage drop.

The power supply should include a V_{CC} buffer capacitor, which provides a discharging time constant. If the input signal does not disappear after turn off the input will become audible after certain time. A 4.7 kΩ resistor discharges the V_{CC} buffer capacitor, because the internal current of the IC does not discharge it completely.

The hardware mute function is favourable for use in Radio Data System (RDS) applications. The zero crossing mute avoids modulation plops. This feature is an advantage for mute during changing presets and/or sources (e.g. traffic announcement during cassette playback).

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		0	10	V
V_n	voltage at all pins except pin 2 referenced to GND (pin 2)		0	V_{CC}	V
T_{amb}	operating ambient temperature		−40	+85	°C
T_{stg}	storage temperature		−65	+150	°C
V_{es}	electrostatic handling	note 1			

Note

1. Human body model: C = 100 pF; R = 1.5 kΩ; V ≥ 2 kV. Charge device model: C = 200 pF; R = 0 Ω; V ≥ 500 V.

CHARACTERISTICS

V_{CC} = 8.5 V; R_S = 600 Ω; R_L = 10 kΩ; C_L = 2.5 nF; AC coupled; f = 1 kHz; T_{amb} = 25 °C; gain control G_v = 0 dB; bass linear; treble linear; fader off; balance in mid position; loudness off; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		7.5	8.5	9.5	V
I_{CC}	supply current		–	26	33	mA
V_{DC}	internal DC voltage at inputs and outputs		3.83	4.25	4.68	V
V_{ref}	internal reference voltage at pin 21		–	4.25	–	V
$G_{v(max)}$	maximum voltage gain	R_S = 0 Ω; R_L = ∞	19	20	21	dB
$V_{o(rms)}$	output voltage level for					
	P_{max} at the power output stage	THD ≤ 0.5%; see Fig.11	–	2000	–	mV
	start of clipping	THD = 1%	2300	–	–	mV
		R_L = 2 kΩ; C_L = 10 nF; THD = 1%	2000	–	–	mV
$V_{i(rms)}$	input sensitivity	V_o = 2000 mV; G_v = 20 dB	–	200	–	mV
f_{ro}	roll-off frequency	C_{KIN} = 220 nF; C_{KVL} = 220 nF; $Z_i = Z_{i(min)}$				
		low frequency (–1 dB)	60	–	–	Hz
		low frequency (–3 dB)	30	–	–	Hz
		high frequency (–1 dB)	20000	–	–	Hz
		C_{KIN} = 470 nF; C_{KVL} = 100 nF; $Z_i = Z_{i(typ)}$ low frequency (–3 dB)	17	–	–	Hz
α_{cs}	channel separation	V_i = 2 V; frequency range 250 Hz to 10 kHz	90	96	–	dB
THD	total harmonic distortion	frequency range 20 Hz to 12.5 kHz				
		V_i = 100 mV; G_v = 20 dB	–	0.1	–	%
		V_i = 1 V; G_v = 0 dB	–	0.05	0.15	%
		V_i = 2 V; G_v = 0 dB	–	0.1	–	%
		V_i = 2 V; G_v = –10 dB	–	0.1	–	%
RR	ripple rejection	$V_{r(rms)}$ < 200 mV				
		f = 100 Hz	70	76	–	dB
		f = 40 Hz to 12.5 kHz	–	66	–	dB
(S+N)/N	signal-plus-noise to noise ratio	unweighted; 20 Hz to 20 kHz (RMS); V_o = 2.0 V; see Figs 6 and 7	–	105	–	dB
		CCIR468-2 weighted; quasi peak; V_o = 2.0 V				
		G_v = 0 dB	–	95	–	dB
		G_v = 12 dB	–	88	–	dB
		G_v = 20 dB	–	81	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$P_{no(rms)}$	noise output power (RMS value) only contribution of TEA6320; power amplifier for 6 W	mute position; note 1	–	–	10	nW
α_{ct}	crosstalk $\left(20 \log \frac{V_{bus(p-p)}}{V_{o(rms)}}\right)$ between bus inputs and signal outputs	note 2	–	110	–	dB
Source selector						
Z_i	input impedance		25	35	45	kΩ
α_S	input isolation of one selected source to any other input	f = 1 kHz	–	105	–	dB
		f = 12.5 kHz	–	95	–	dB
$V_{i(rms)}$	maximum input voltage (RMS value)	THD < 0.5%; V_{CC} = 8.5 V	–	2.15	–	V
		THD < 0.5%; V_{CC} = 7.5 V	–	1.8	–	V
V_{offset}	DC offset voltage at source selector output by selection of any inputs		–	–	10	mV
Z_o	output impedance		–	80	120	Ω
R_L	output load resistance		10	–	–	kΩ
C_L	output load capacity		0	–	2500	pF
G_v	voltage gain, source selector		–	0	–	dB
Control part (source selector disconnected; source resistance 600 Ω)						
Z_i	input impedance volume input		100	150	200	kΩ
	input impedance loudness input		25	33	40	kΩ
Z_o	output impedance		–	80	120	Ω
R_L	output load resistance		2	–	–	kΩ
C_L	output load capacity		0	–	10	nF
R_{DCL}	DC load resistance at output to ground		4.7	–	–	kΩ
$V_{i(rms)}$	maximum input voltage (RMS value)	THD < 0.5%	–	2.15	–	V
V_{no}	noise output voltage	CCIR468-2 weighted; quasi peak				
		G_v = 20 dB	–	110	220	μV
		G_v = 0 dB	–	33	50	μV
		G_v = –66 dB	–	13	22	μV
		mute position	–	10	–	μV
CR_{tot}	total continuous control range		–	106	–	dB
	recommended control range		–	86	–	dB
G_{step}	step resolution		–	1	–	dB
	step error between any adjoining step		–	–	0.5	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ΔG_a	attenuator set error	G_v = +20 to –50 dB	–	–	2	dB
		G_v = –51 to –66 dB	–	–	3	dB
ΔG_t	gain tracking error	G_v = +20 to –50 dB	–	–	2	dB
$MUTE_{att}$	mute attenuation	see Fig.10	100	110	–	dB
V_{offset}	DC step offset between any adjoining step	G_v = 0 to –66 dB	–	0.2	10	mV
		G_v = 20 to 0 dB	–	2	15	mV
	DC step offset between any step to mute	G_v = 0 to –66 dB	–	–	10	mV
Volume I control and loudness						
CR_{vol}	continuous volume control range		–	51	–	dB
G_v	voltage gain		–31	–	+20	dB
G_{step}	step resolution		–	1	–	dB
L_{Bmax}	maximum loudness boost	loudness on; referred to loudness off; boost is determined by external components				
		f = 40 Hz	–	17	–	dB
		f = 10 kHz	–	4.5	–	dB
Bass control						
G_{bass}	bass control, maximum boost	f = 40 Hz	14	15	16	dB
	maximum attenuation	f = 40 Hz	14	15	16	dB
G_{step}	step resolution (toggle switching)	f = 40 Hz	–	1.5	–	dB
	step error between any adjoining step	f = 40 Hz	–	–	0.5	dB
V_{offset}	DC step offset in any bass position		–	–	20	mV
Treble control						
G_{treble}	treble control, maximum boost	f = 15 kHz	11	12	13	dB
	maximum attenuation	f = 15 kHz	11	12	13	dB
	maximum boost	f > 15 kHz	–	–	15	dB
G_{step}	step resolution (toggle switching)	f = 15 kHz	–	1.5	–	dB
	step error between any adjoining step	f = 15 kHz	–	–	0.5	dB
V_{offset}	DC step offset in any treble position		–	–	10	mV
Volume II, balance and fader control						
CR	continuous attenuation fader and volume control range		53.5	55	56.5	dB
G_{step}	step resolution		–	1	2	dB
	attenuation set error		–	–	1.5	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Mute function (see Fig.10)						
HARDWARE MUTE						
V_{sw}	mute switch level ($2 \times V_{BE}$)		–	1.45	–	V
mute active						
V_{swLOW}	input level		–	–	1.0	V
I_i	input current	V_{swLOW} = 1 V	–300	–	–	µA
mute passive: level internally defined						
V_{swHIGH}	saturation voltage		–	–	V_{CC}	V
$t_{d(mute)}$	delay until mute passive		–	–	0.5	ms
ZERO CROSSING MUTE						
I_d	discharge current		0.3	0.6	1.2	µA
I_{ch}	charge current		–300	–150	–	µA
V_{swDEL}	delay switch level ($3 \times V_{BE}$)		–	2.2	–	V
t_d	delay time	C_m = 10 nF	–	100	–	ms
V_{wind}	window for audio signal zero crossing detection		–	30	40	mV
Muting at power supply drop						
V_{CCdrop}	supply drop for mute active		–	V_{19} – 0.7	–	V
Power-on reset (when reset is active the GMU-bit (general mute) is set and the I²C-bus receiver is in reset position)						
V_{CC}	increasing supply voltage start of reset		–	–	2.5	V
	end of reset		5.2	6.5	7.2	V
	decreasing supply voltage start of reset		4.2	5.5	6.2	V
Digital part (I²C-bus pins); note 3						
V_{iH}	HIGH level input voltage		3	–	9.5	V
V_{iL}	LOW level input voltage		–0.3	–	+1.5	V
I_{iH}	HIGH level input current		–10	–	+10	µA
I_{iL}	LOW level input current		–10	–	+10	µA
V_{oL}	LOW level output voltage	I_L = 3 mA	–	–	0.4	V

Notes to the characteristics

1. The indicated values for output power assume a 6 W power amplifier at 4 Ω with 20 dB gain and a fixed attenuator of 12 dB in front of it. Signal-to-noise ratios exclude noise contribution of the power amplifier.
2. The transmission contains: total initialization with MAD and subaddress for volume and 8 data words, see also definition of characteristics, clock frequency = 50 kHz, repetition burst rate = 400 Hz, maximum bus signal amplitude = 5 V (p-p).
3. The AC characteristics are in accordance with the I²C-bus specification. This specification, *"The I²C-bus and how to use it"*, can be ordered using the code 9398 393 40011.

I²C-BUS PROTOCOL

I²C-bus format

S(1)	SLAVE ADDRESS(2)	A(3)	SUBADDRESS(4)	A(3)	DATA(5)	A(3)	P(6)

Notes

1. S = START condition.
2. SLAVE ADDRESS (MAD) = 1000 0000.
3. A = acknowledge, generated by the slave.
4. SUBADDRESS (SAD), see Table 1.
5. DATA, see Table 1; if more than 1 byte of DATA is transmitted, then auto-increment of the significant subaddress is performed.
6. P = STOP condition.

Table 1 Second byte after MAD

FUNCTION	BIT	MSB							LSB
		7	6	5	4	3	2(1)	1(1)	0(1)
Volume/loudness	V	0	0	0	0	0	0	0	0
Fader front right	FFR	0	0	0	0	0	0	0	1
Fader front left	FFL	0	0	0	0	0	0	1	0
Fader rear right	FRR	0	0	0	0	0	0	1	1
Fader rear left	FRL	0	0	0	0	0	1	0	0
Bass	BA	0	0	0	0	0	1	0	1
Treble	TR	0	0	0	0	0	1	1	0
Switch	S	0	0	0	0	0	1	1	1

Note

1. Significant subaddress.

Table 2 Definition of third byte after MAD and SAD

FUNCTION	BIT	MSB							LSB
		7	6	5	4	3	2	1	0
Volume/loudness	V	ZCM[1]	LOFF[2]	V5[3]	V4[3]	V3[3]	V2[3]	V1[3]	V0[3]
Fader front right	FFR	X[4]	X[4]	FFR5[5]	FFR4[5]	FFR3[5]	FFR2[5]	FFR1[5]	FFR0[5]
Fader front left	FFL	X[4]	X[4]	FFL5[6]	FFL4[6]	FFL3[6]	FFL2[6]	FFL1[6]	FFL0[6]
Fader rear right	FRR	X[4]	X[4]	FRR5[7]	FRR4[7]	FRR3[7]	FRR2[7]	FRR1[7]	FRR0[7]
Fader rear left	FRL	X[4]	X[4]	FRL5[8]	FRL4[8]	FRL3[8]	FRL2[8]	FRL1[8]	FRL0[8]
Bass	BA	X[4]	X[4]	X[4]	BA4[9]	BA3[9]	BA2[9]	BA1[9]	BA0[9]
Treble	TR	X[4]	X[4]	X[4]	TR4[10]	TR3[10]	TR2[10]	TR1[10]	TR0[10]
Switch	S	GMU[11]	X[4]	X[4]	X[4]	X[4]	SC2[12]	SC1[12]	SC0[12]

Notes

1. Zero crossing mode.
2. Switch loudness on/off.
3. Volume control.
4. Don't care bits (logic 1 during testing).
5. Fader control front right.
6. Fader control front left.
7. Fader control rear right.
8. Fader control rear left.
9. Bass control.
10. Treble control.
11. Mute control for all outputs (general mute).
12. Source selector control.

Table 3 Volume I setting

G_v (dB)	DATA					
	V5	V4	V3	V2	V1	V0
Loudness on: the increment of the loudness characteristics is linear at every volume step in the range from +20 to −11 dB						
+20	1	1	1	1	1	1
+19	1	1	1	1	1	0
+18	1	1	1	1	0	1
+17	1	1	1	1	0	0
+16	1	1	1	0	1	1
+15	1	1	1	0	1	0
+14	1	1	1	0	0	1
+13	1	1	1	0	0	0
+12	1	1	0	1	1	1
+11	1	1	0	1	1	0
+10	1	1	0	1	0	1
+9	1	1	0	1	0	0
+8	1	1	0	0	1	1
+7	1	1	0	0	1	0
+6	1	1	0	0	0	1
+5	1	1	0	0	0	0
+4	1	0	1	1	1	1
+3	1	0	1	1	1	0
+2	1	0	1	1	0	1
+1	1	0	1	1	0	0
0	1	0	1	0	1	1
−1	1	0	1	0	1	0
−2	1	0	1	0	0	1
−3	1	0	1	0	0	0
−4	1	0	0	1	1	1
−5	1	0	0	1	1	0
−6	1	0	0	1	0	1
−7	1	0	0	1	0	0
−8	1	0	0	0	1	1
−9	1	0	0	0	1	0
−10	1	0	0	0	0	1
−11	1	0	0	0	0	0

G_v (dB)	DATA					
	V5	V4	V3	V2	V1	V0
Loudness characteristic is constant in a range from −11 dB to −31 dB						
−12	0	1	1	1	1	1
−13	0	1	1	1	1	0
−14	0	1	1	1	0	1
−15	0	1	1	1	0	0
−16	0	1	1	0	1	1
−17	0	1	1	0	1	0
−18	0	1	1	0	0	1
−19	0	1	1	0	0	0
−20	0	1	0	1	1	1
−21	0	1	0	1	1	0
−22	0	1	0	1	0	1
−23	0	1	0	1	0	0
−24	0	1	0	0	1	1
−25	0	1	0	0	1	0
−26	0	1	0	0	0	1
−27	0	1	0	0	0	0
−28	0	0	1	1	1	1
−29	0	0	1	1	1	0
−30	0	0	1	1	0	1
−31	0	0	1	1	0	0
Repetition of steps in a range from −28 dB to −31 dB						
−28	0	0	1	0	1	1
−29	0	0	1	0	1	0
−30	0	0	1	0	0	1
−31	0	0	1	0	0	0
−28	0	0	0	1	1	1
−29	0	0	0	1	1	0
−30	0	0	0	1	0	1
−31	0	0	0	1	0	0
−28	0	0	0	0	1	1
−29	0	0	0	0	1	0
−30	0	0	0	0	0	1
−31	0	0	0	0	0	0

Table 4 Volume II setting (fader and balance); note 1

G_v (dB)	DATA					
	FRR5	FRR4	FRR3	FRR2	FRR1	FRR0
	FRL5	FRL4	FRL3	FRL2	FRL1	FRL0
	FFL5	FFL4	FFL3	FFL2	FFL1	FFL0
	FFR5	FFR4	FFR3	FFR2	FFR1	FFR0
0	1	1	1	1	1	1
−1	1	1	1	1	1	0
−2	1	1	1	1	0	1
−3	1	1	1	1	0	0
−4	1	1	1	0	1	1
−5	1	1	1	0	1	0
−6	1	1	1	0	0	1
−7	1	1	1	0	0	0
−8	1	1	0	1	1	1
−9	1	1	0	1	1	0
−10	1	1	0	1	0	1
−11	1	1	0	1	0	0
−12	1	1	0	0	1	1
−13	1	1	0	0	1	0
−14	1	1	0	0	0	1
−15	1	1	0	0	0	0
−16	1	0	1	1	1	1
−17	1	0	1	1	1	0
−18	1	0	1	1	0	1
−19	1	0	1	1	0	0
−20	1	0	1	0	1	1
−21	1	0	1	0	1	0
−22	1	0	1	0	0	1
−23	1	0	1	0	0	0
−24	1	0	0	1	1	1
−25	1	0	0	1	1	0
−26	1	0	0	1	0	1
−27	1	0	0	1	0	0
−28	1	0	0	0	1	1
−29	1	0	0	0	1	0
−30	1	0	0	0	0	1
−31	1	0	0	0	0	0
−32	0	1	1	1	1	1
−33	0	1	1	1	1	0
−34	0	1	1	1	0	1

G_v (dB)	DATA					
	FRR5	FRR4	FRR3	FRR2	FRR1	FRR0
	FRL5	FRL4	FRL3	FRL2	FRL1	FRL0
	FFL5	FFL4	FFL3	FFL2	FFL1	FFL0
	FFR5	FFR4	FFR3	FFR2	FFR1	FFR0
–35	0	1	1	1	0	0
–36	0	1	1	0	1	1
–37	0	1	1	0	1	0
–38	0	1	1	0	0	1
–39	0	1	1	0	0	0
–40	0	1	0	1	1	1
–41	0	1	0	1	1	0
–42	0	1	0	1	0	1
–43	0	1	0	1	0	0
–44	0	1	0	0	1	1
–45	0	1	0	0	1	0
–46	0	1	0	0	0	1
–47	0	1	0	0	0	0
–48	0	0	1	1	1	1
–49	0	0	1	1	1	0
–50	0	0	1	1	0	1
–51	0	0	1	1	0	0
–52	0	0	1	0	1	1
–53	0	0	1	0	1	0
–54	0	0	1	0	0	1
–55	0	0	1	0	0	0
mute	0	0	0	1	1	1
mute	0	0	0	1	1	0
mute	0	0	0	1	0	1
mute	0	0	0	1	0	0
mute	0	0	0	0	1	1
mute	0	0	0	0	1	0
mute	0	0	0	0	0	1
mute	0	0	0	0	0	0

Note

1. For a particular range the data is always the same, only the subaddress changes.

Table 5 Bass setting

G_{bass} (dB)	DATA				
	BA4	BA3	BA2	BA1	BA0
+15.0	1	1	1	1	1
+13.5	1	1	1	1	0
+15.0	1	1	1	0	1
+13.5	1	1	1	0	0
+15.0	1	1	0	1	1
+13.5	1	1	0	1	0
+12.0	1	1	0	0	1
+10.5	1	1	0	0	0
+9.0	1	0	1	1	1
+7.5	1	0	1	1	0
+6.0	1	0	1	0	1
+4.5	1	0	1	0	0
+3.0	1	0	0	1	1
+1.5	1	0	0	1	0
0[1]	1	0	0	0	1
0[2]	1	0	0	0	0
−1.5	0	1	1	1	1
−3.0	0	1	1	1	0
−4.5	0	1	1	0	1
−6.0	0	1	1	0	0
−7.5	0	1	0	1	1
−9.0	0	1	0	1	0
−10.5	0	1	0	0	1
−12.0	0	1	0	0	0
−13.5	0	0	1	1	1
−15.0	0	0	1	1	0
−13.5	0	0	1	0	1
−15.0	0	0	1	0	0
note 3	0	0	0	1	1
note 3	0	0	0	1	0
note 3	0	0	0	0	1
notes 3 and 4	0	0	0	0	0

Notes

1. Recommended data word for step 0 dB.
2. Result of 1.5 dB boost and 1.5 dB attenuation.
3. The last four bass control data words mute the bass response.
4. The last bass control and treble control data words (00000) enable the external equalizer connection.

Table 6 Treble setting

G_{treble} (dB)	DATA				
	TR4	TR3	TR2	TR1	TR0
+12.0	1	1	1	1	1
+10.5	1	1	1	1	0
+12.0	1	1	1	0	1
+10.5	1	1	1	0	0
+12.0	1	1	0	1	1
+10.5	1	1	0	1	0
+12.0	1	1	0	0	1
+10.5	1	1	0	0	0
+9.0	1	0	1	1	1
+7.5	1	0	1	1	0
+6.0	1	0	1	0	1
+4.5	1	0	1	0	0
+3.0	1	0	0	1	1
+1.5	1	0	0	1	0
0[1]	1	0	0	0	1
0[2]	1	0	0	0	0
–1.5	0	1	1	1	1
–3.0	0	1	1	1	0
–4.5	0	1	1	0	1
–6.0	0	1	1	0	0
–7.5	0	1	0	1	1
–9.0	0	1	0	1	0
–10.5	0	1	0	0	1
–12.0	0	1	0	0	0
note 3	0	0	1	1	1
note 3	0	0	1	1	0
note 3	0	0	1	0	1
note 3	0	0	1	0	0
note 3	0	0	0	1	1
note 3	0	0	0	1	0
note 3	0	0	0	0	1
notes 3 and 4	0	0	0	0	0

Notes

1. Recommended data word for step 0 dB.
2. Result of 1.5 dB boost and 1.5 dB attenuation.
3. The last eight treble control data words select treble output.
4. The last treble control and bass control data words (00000) enable the external equalizer connection.

Table 7 Loudness setting

CHARACTERISTIC	DATA LOFF
With loudness	0
Linear	1

Table 8 Selected input

FUNCTION	DATA		
	SC2	SC1	SC0
Stereo inputs IAL and IAR	1	1	1
Stereo inputs IBL and IBR	1	1	0
Stereo inputs ICL and ICR	1	0	1
Stereo inputs IDL and IDR	1	0	0
Mono input IMO	0	X[1]	X[1]

Note

1. X = don't care bits (logic 1 during testing).

Table 9 Mute mode

FUNCTION	DATA	
	GMU	ZCM
Direct mute off	0	0
Mute off delayed until the next zero crossing	0	1
Direct mute	1	0
Mute delayed until the next zero crossing	1	1

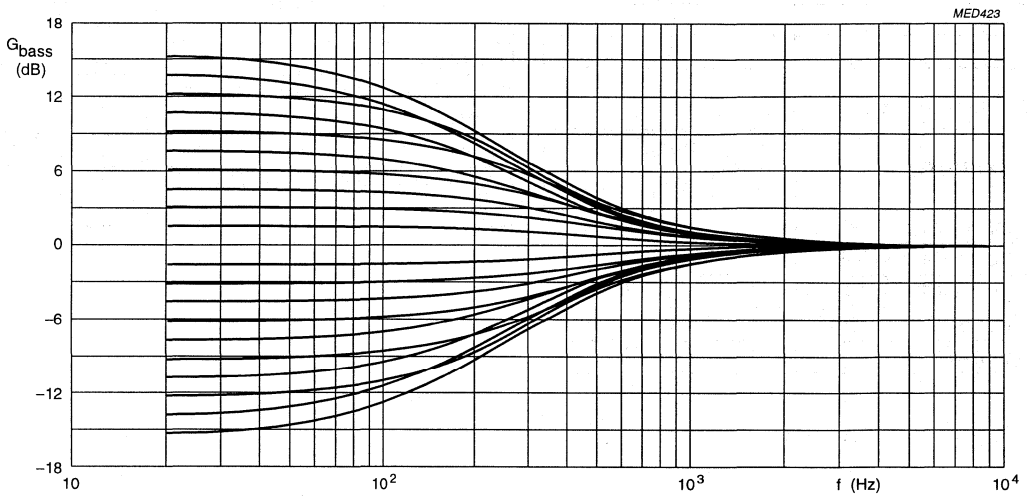


Fig.3 Bass control.

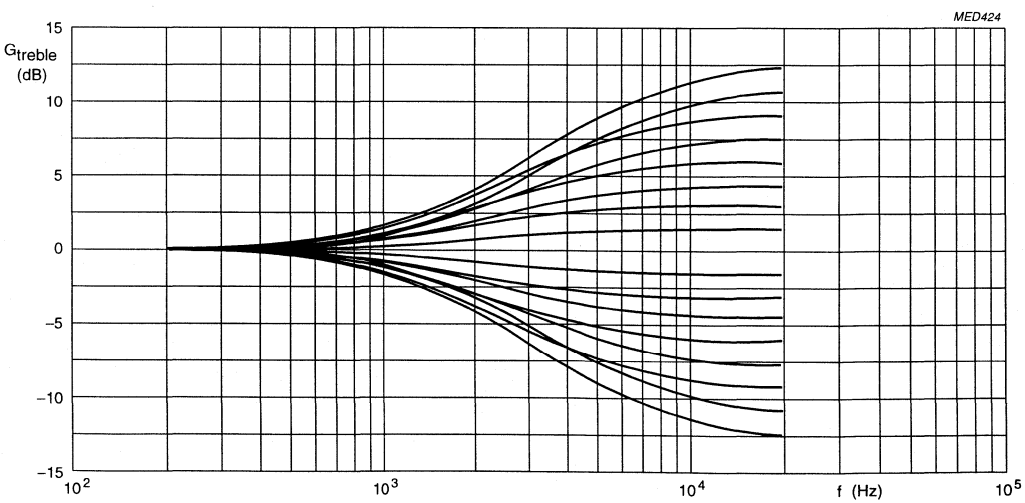


Fig.4 Treble control.

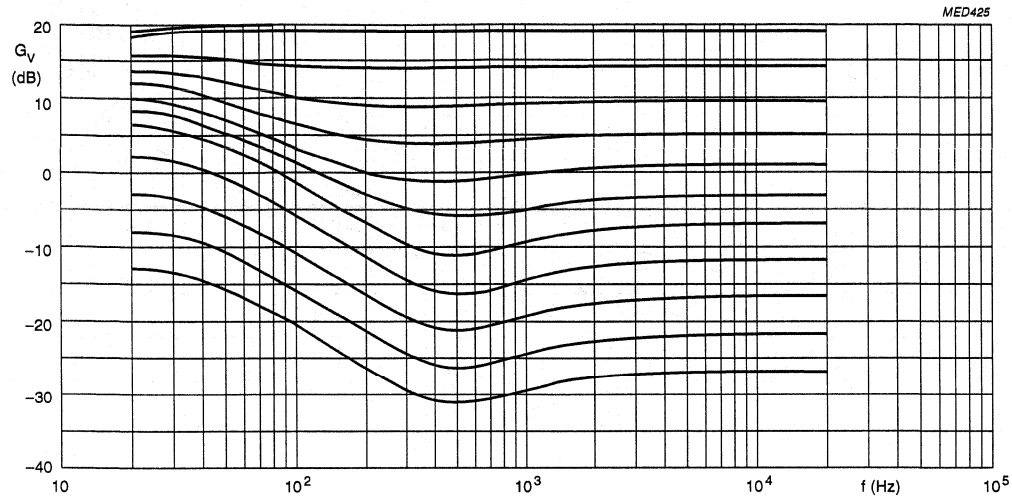
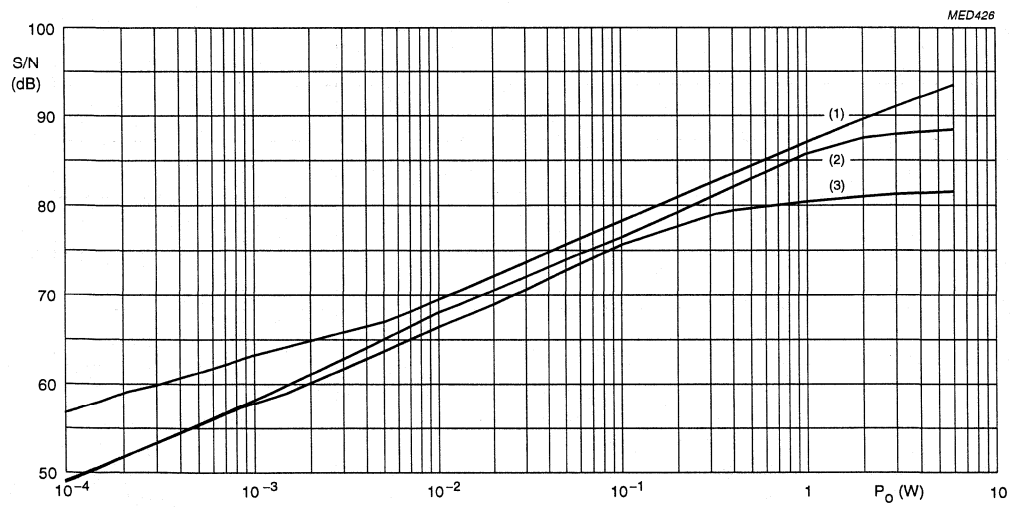
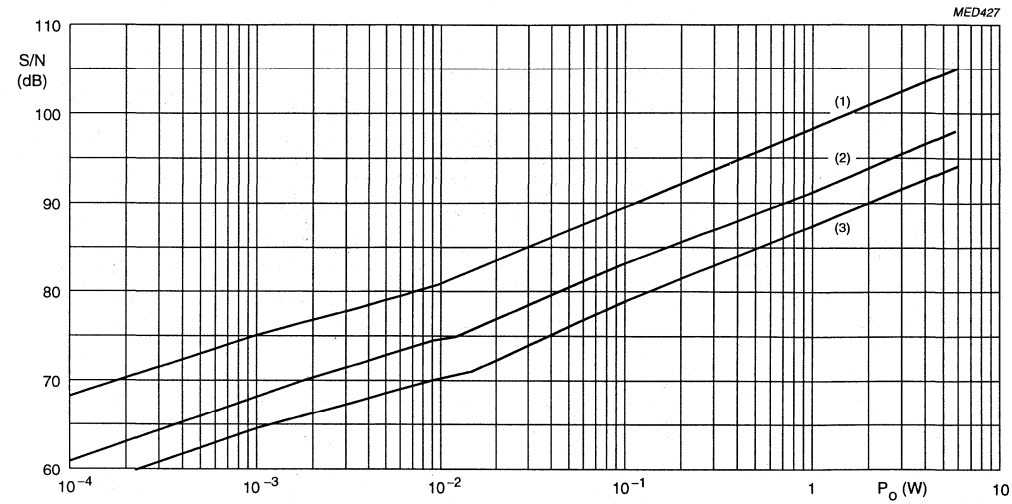


Fig.5 Volume control with loudness (including low roll-off frequency).



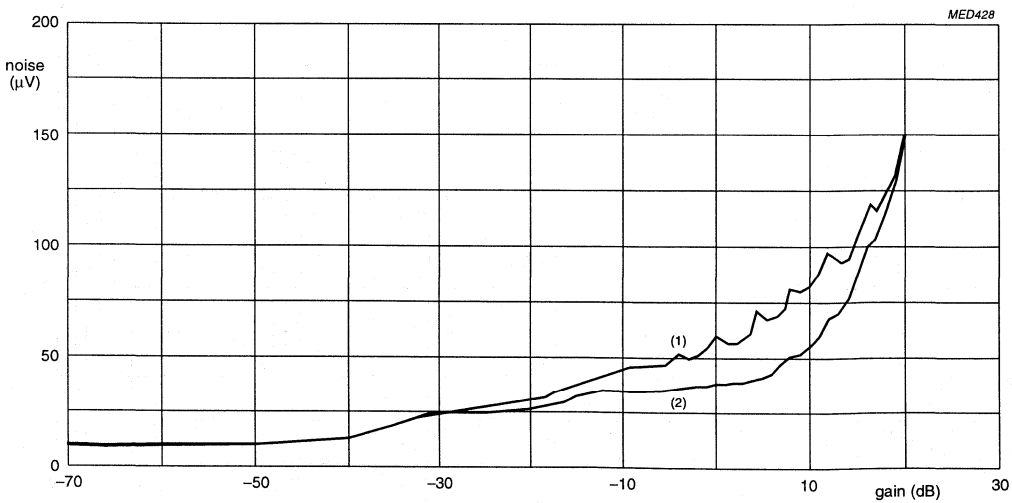
(1) V_i = 2.0 V.
(2) V_i = 0.5 V.
(3) V_i = 0.2 V.

Fig.6 Signal-to-noise ratio; noise weighted: CCIR468-2, quasi peak.



(1) Unweighted RMS.
(2) CCIR468-2 RMS.
(3) CCIR468-2 quasi peak.

Fig.7 Signal-to-noise ratio; V_i = 2 V; P_{max} = 6 W.



Stereo/mono inputs.
(1) Loudness on.
(2) Loudness off.

Fig.8 Noise output voltage; CCIR468-2, quasi peak.

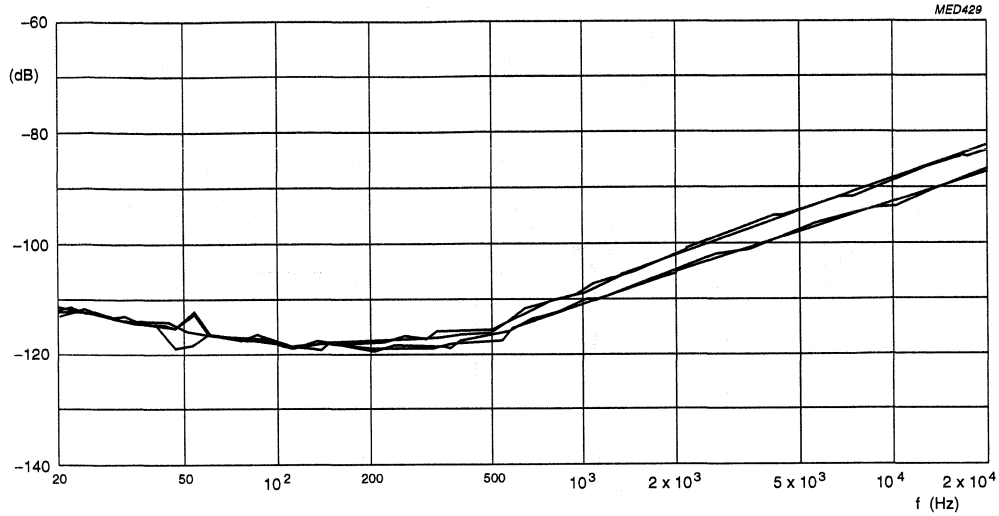
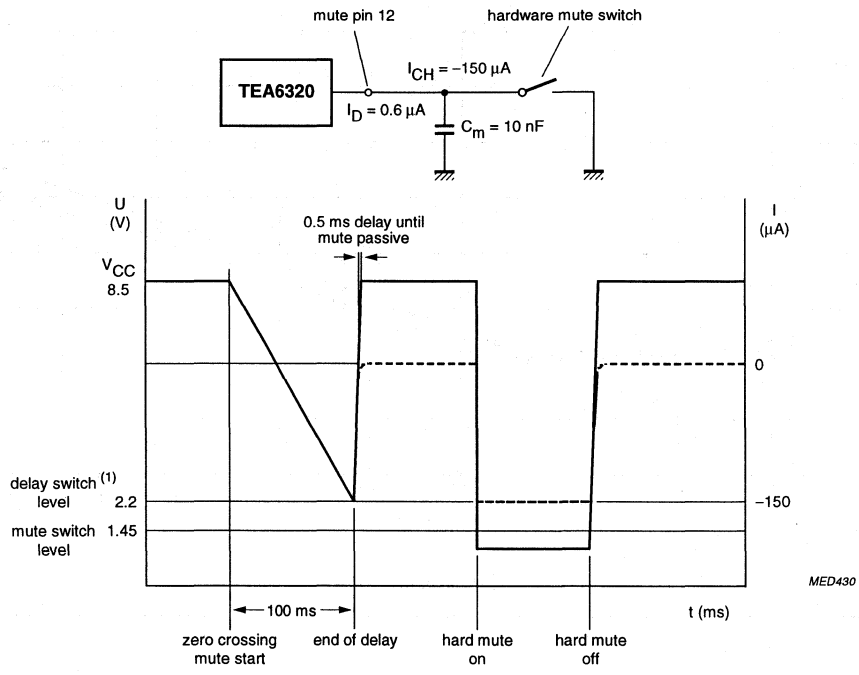

MED429
-60
(dB)
-80
-100
-120
-140
20
50
10 2
200
500
10 3
2 x 10 3
5 x 10 3
10 4
2 x 10 4
f (Hz)

Fig.9 Muting.

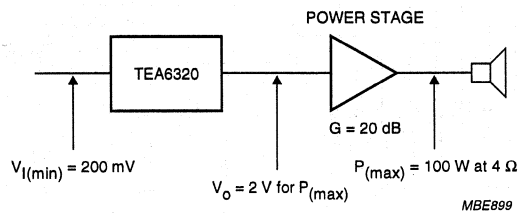


(1) Typically 2.2 V; referenced to $3 \times V_{BE}$.

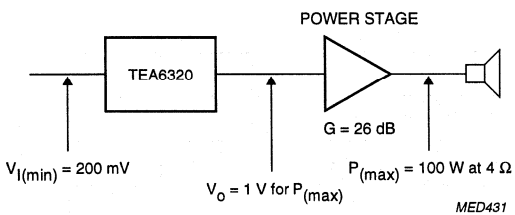
Fig.10 Mute function diagram.

If the 20 dB gain is not required for the maximum volume position, it will be an advantage to use the maximum boost gain and then increased attenuation in the last section, Volume II.

Therefore the loudness will be at the correct place and a lower noise and offset voltage will be achieved.



a.



b.

a. Gain volume I = 20 dB ($G_{v(max)}$); gain volume II = 0 dB; fader and balance range = 55 dB.
b. Gain volume I = 20 dB ($G_{v(max)}$); gain volume II = −6 dB global setting; fader and balance range now 49 dB, previously 55 dB.

Fig.11 Level diagram.

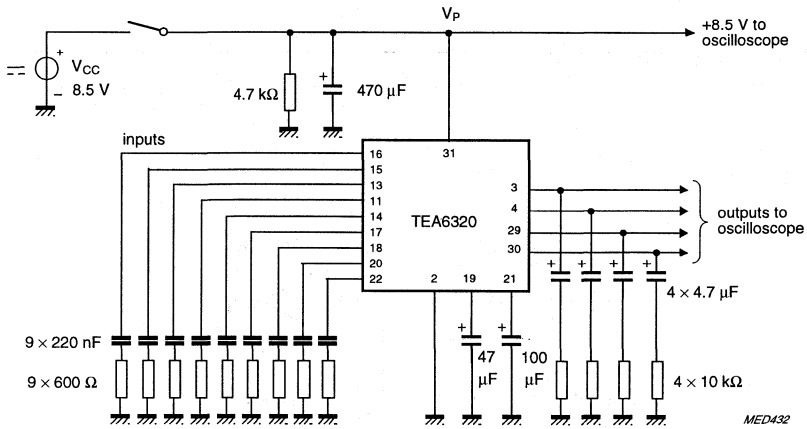
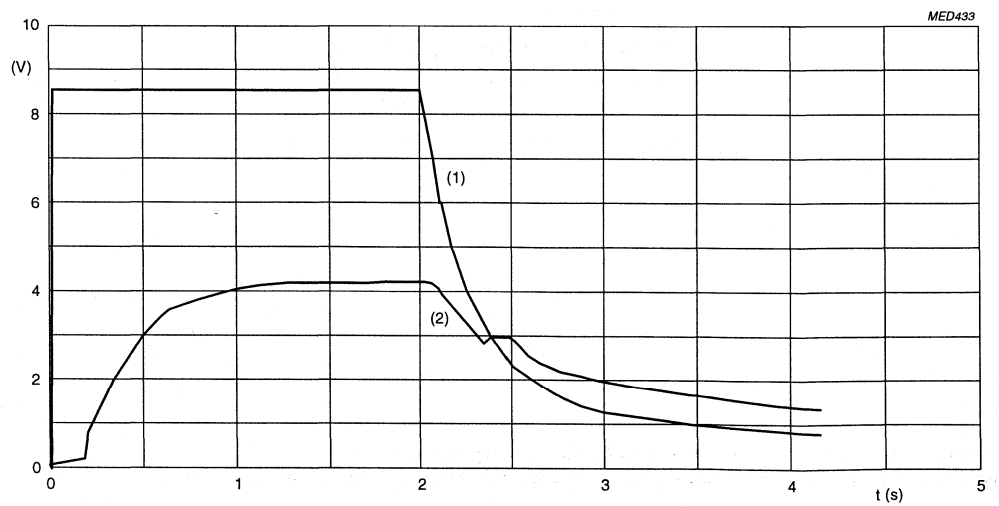


Fig.12 Turn-on/off power supply circuit diagram.



(1) V_{CC}.
(2) V_O.

Fig.13 Turn-on/off behaviour.

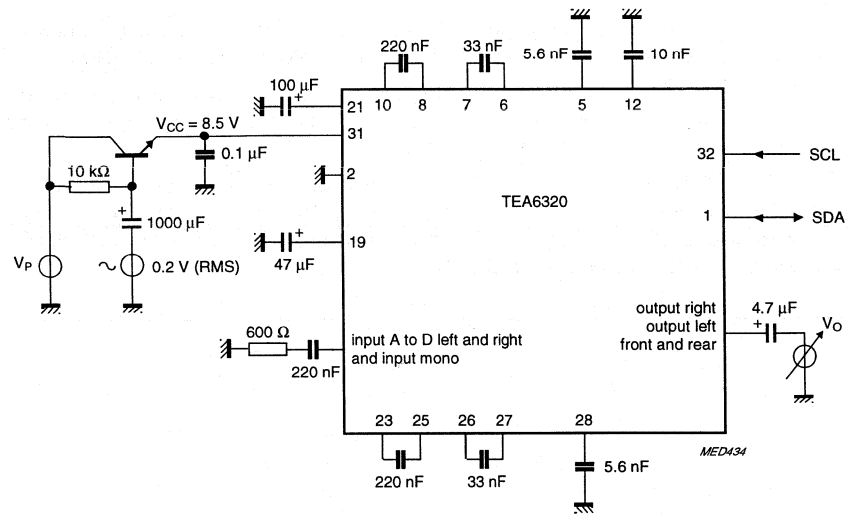


Fig.14 Test circuit for power supply ripple rejection (RR).

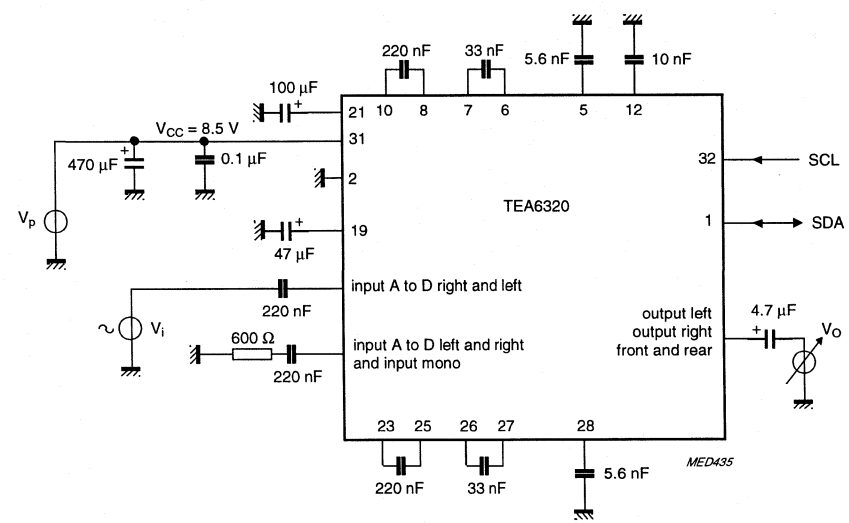


Fig.15 Test circuit for channel separation (α_{cs}).

Selection of input signals by using the zero crossing mute mode

A selection from input A (IAL) to input B (IBL) left sources produces a modulation click depending on the difference of the signal values at the time of switching.

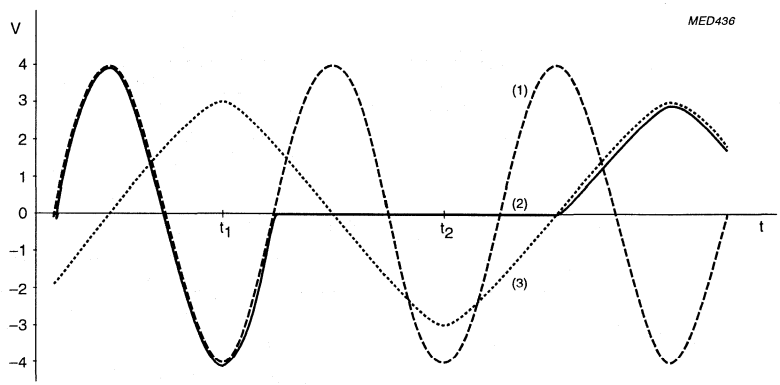
At t_1 the maximum possible difference between signals is 7 V(p-p) (see Fig. 16) and gives a large click. Using the cross detector no modulation click is audible.

For example: The selection is enabled at t_1, the microcontroller sets the zero cross bit (ZCM = 1) and then the mute bit (GMU = 1) via the I^2C-bus. The output signal follows the input A signal, until the next zero crossing occurs and then activates mute.

After a fixed delay time at t_2, the microcontroller sends the bits for input switching and mute inactive.

The output signal remains muted until the next signal zero crossing of input B (IBL) occurs, and then follows that signal.

The delay time $t_2 - t_1$ is e.g. 40 ms. Therefore the capacity C_m = 3.3 nF. The zero cross function is working at the lowest frequency of 40 Hz determined by the C_m capacitor.



(1) Input A (IAL).
(2) Output.
(3) Input B (IBL).

Fig.16 Zero cross function; only one channel shown.

Loudness filter calculation example

Figure 17 shows the basic loudness circuit with an external low-pass filter application. R1 allows an attenuation range of 21 dB while the boost is determined by the gain stage V_2. Both result in a loudness control range of +20 to −12 dB.

Defining f_{ref} as the frequency where the level does not change while switching loudness on/off. The external resistor R3 for $f_{ref} \rightarrow \infty$ can be calculated as:

$$R3 = R1\frac{10^{\frac{G_v}{20}}}{1 - 10^{\frac{G_v}{20}}}$$. With G_v = −21 dB and R1 = 33 kΩ,

R3 = 3.2 kΩ is generated.

For the low-pass filter characteristic the value of the external capacitor C1 can be determined by setting a specific boost for a defined frequency and referring the gain to G_v at f_{ref} as indicated above.

$$\left|\frac{1}{j(\omega C1)}\right| = \frac{(R1 + R3) \times 10^{\frac{G_v}{20}} - R3}{1 - 10^{\frac{G_v}{20}}}$$

For example: 3 dB boost at f = 1 kHz
$G_v = G_{v(ref)}$ + 3 dB = −18 dB; f = 1 kHz and C1 = 100 nF.

If a loudness characteristic with additional high frequency boost is desired, an additional high-pass section has to be included in the external filter circuit as indicated in the block diagram. A filter configuration that provides AC coupling avoids offset voltage problems.

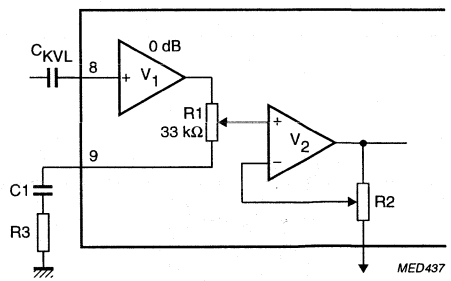


Fig.17 Basic loudness circuit.

INTERNAL PIN CONFIGURATIONS

Values shown in Figs 18 to 30 are typical DC values;
V_{CC} = 8.5 V.

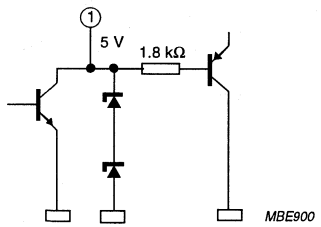


Fig.18 Pin 1: SDA (I²C-bus data).

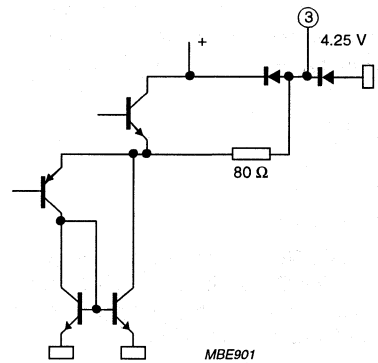


Fig.19 Pins 3, 4, 29, 30: output signals.

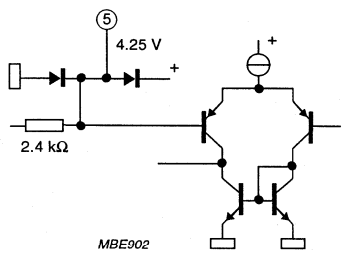


Fig.20 Pins 5 and 28: treble control capacitors.

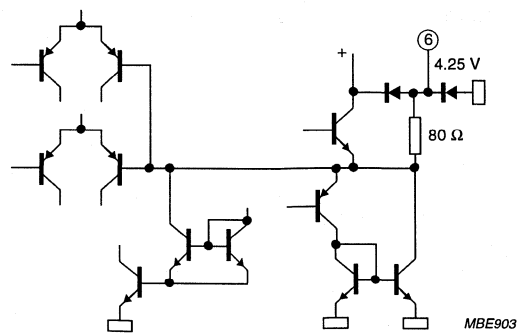


Fig.21 Pins 6 and 27: bass control capacitor outputs.

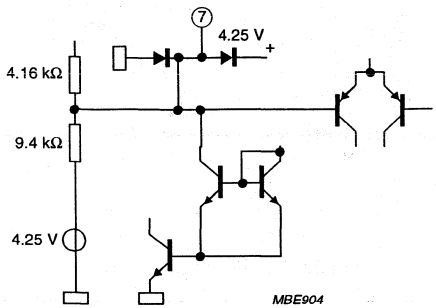


Fig.22 Pins 7 and 26: bass control capacitor inputs.

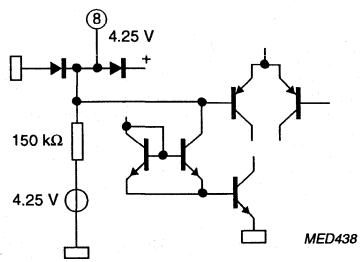


Fig.23 Pins 8 and 25: input volume 1, control part.

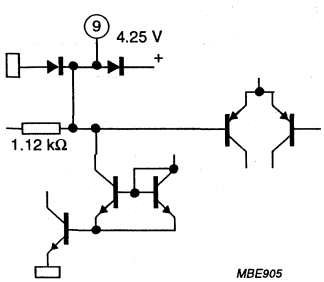


Fig.24 Pins 9 and 24: input loudness, control part.

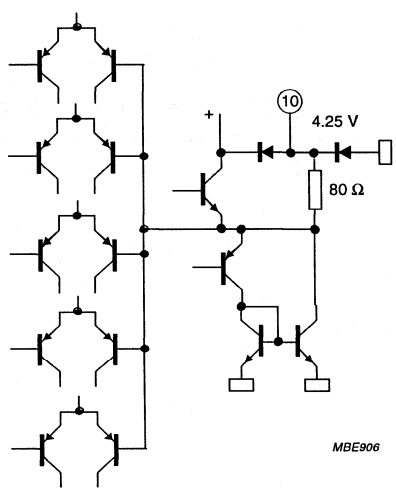


Fig.25 Pins 10 and 23: output source selector.

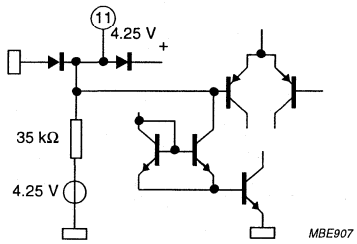


Fig.26 Pins 11, 13 to 18, 20, 22: inputs.

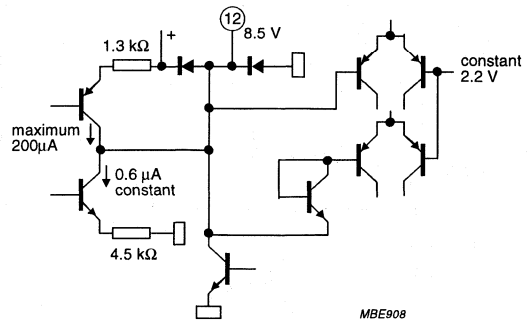


Fig.27 Pin 12: mute control.

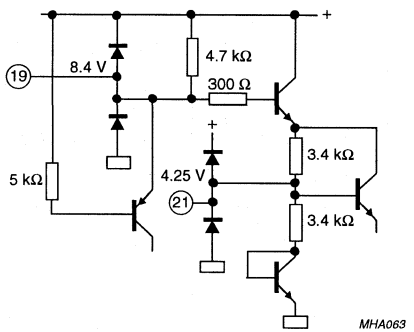


Fig.28 Pin 19: filtering for supply; pin 21: reference voltage.

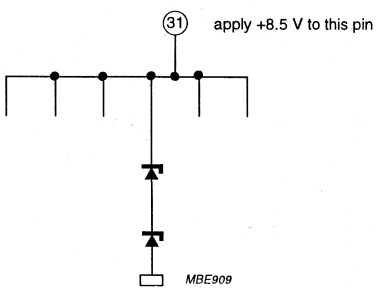


Fig.29 Pin 31: supply voltage.

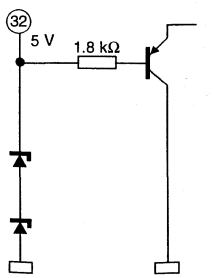


Fig.30 Pin 32: SCL (I^2C-bus clock).

Sound fader control circuit for car radios

TEA6330T

FEATURES

- Stereo/hi-fi processor for car radios performed with volume, balance, bass and treble controls
- Sound fader control (front/rear) down to –30 dB in steps of 2 dB
- Fast muting via bus or via setting the muting pin
- Suitable for external audio equalizers, can be looped-in controlled by the I²C-bus
- Power-on reset on chip sets the device into general mute position
- AC and DC short-circuit protected concerning neighbouring pins
- I²C-bus control for all functions.

GENERAL DESCRIPTION

This bipolar IC is an I²C-bus controlled sound/volume controller for car radios, in addition with fader function and the possibility of an external equalizer.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage	7	8.5	10	V
I_P	supply current	–	26	–	mA
V_i	maximum AF input signal (RMS value)	2	–	–	V
V_o	maximum AF output signal (RMS value)	1.1	–	–	V
ΔG_v	volume control range, separated	–66	–	+20	dB
	fader control range, separated	0	–	–30	dB
	bass control range	–12	–	+15	dB
	treble control range	–12	–	+12	dB
THD	total harmonic distortion	–	–	0.2	%
S/N(W)	weighted signal-to-noise ratio	–	67	–	dB
α_{CR}	crosstalk attenuation	–	90	–	dB
B	frequency response (–1 dB)	–	35 to 20000	–	Hz

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA6330T[1]	20	SO	plastic	SOT163A

Note

1. Plastic small outline package; 20 leads; body width 7.5 mm; (SOT163A); SOT163-1; 1996 August 02.

Sound fader control circuit for car radios

TEA6330T

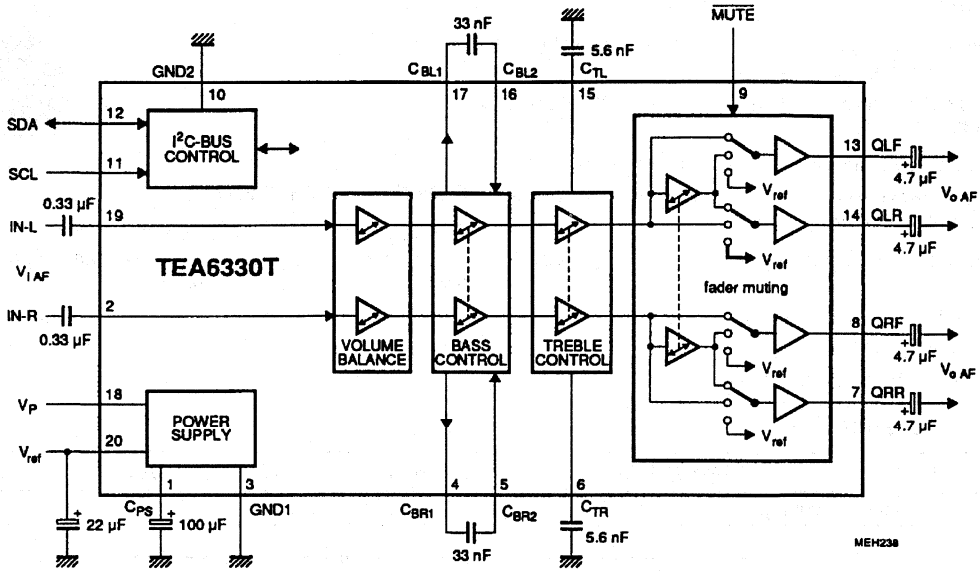


Fig.1 Block and test circuit.

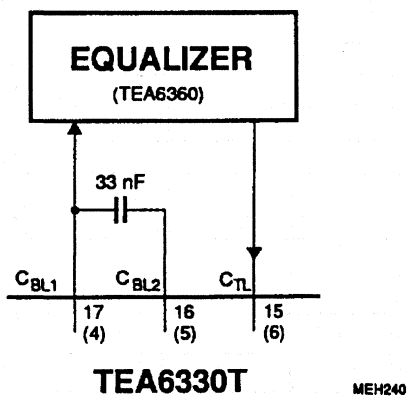


Fig.2 Connection of equalizer (Table 7). In application with equalizer circuit TEA6360 coupling capacitors are not necessary. Connectors for RIGHT in brackets.

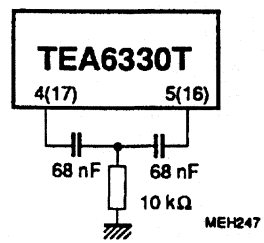


Fig.3 T-filter for enhanced bass control (Fig.5). Connectors for LEFT in brackets.

PINNING

SYMBOL	PIN	DESCRIPTION
C_{PS}	1	filtering capacitor for power supply
IN-R	2	audio input signal RIGHT
GND1	3	analog ground (0 V)
C_{BR1}	4	capacitor for bass control RIGHT and signal to equalizer
C_{BR2}	5	capacitor for bass control RIGHT
C_{TR}	6	capacitor for treble control RIGHT, input signal for equalizer RIGHT
QRR	7	right audio output signal of rear channel
QRF	8	right audio output signal of front channel
MUTE	9	input to set mute externally
GND2	10	digital ground (0 V) for bus control
SCL	11	clock signal of I^2C-bus
SDA	12	data signal of I^2C-bus
QLF	13	left audio output signal of front channel
QLR	14	left audio output signal of rear channel
C_{TL}	15	capacitor for treble control LEFT, input signal for equalizer LEFT
C_{BL2}	16	capacitor for bass control LEFT
C_{BL1}	17	capacitor for bass control LEFT and signal to equalizer
V_P	18	+8.5 V supply voltage
IN-L	19	audio input signal LEFT
V_{ref}	20	reference voltage output (V_P/2)

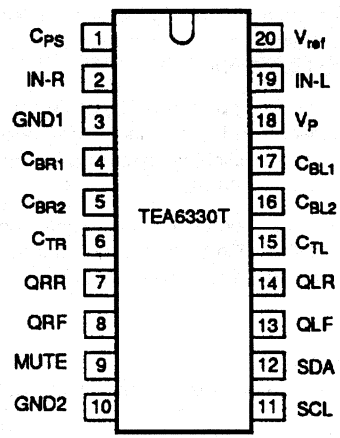


Fig.4 Pin configuration.

FUNCTIONAL DESCRIPTION

This bipolar IC is an I^2C-bus controlled sound/volume controller for car radios including fader function and the possibility of an external equalizer. The sound signal setting is performed by resistor chains in combination with multi-input operational amplifiers. The advantages of this principle are the combination of low noise, low distortion and a high dynamic range. The separated volume controls of the left and the right channel make the balance control possible. The value and the characteristic of the balance is controlled via the I^2C-bus.

The contour function is performed by setting an extra bass control and optional treble, depending on the actual volume position. Its switching points and its range are also controllable via the I^2C-bus.

An interface is assigned behind the volume control to loop-in an equalizer (Fig.2). In this case the treble control is switched off, and the bass control can be used to set the contour.

Low level control fader is included independent of the volume controls, because the TEA6330T has four driver outputs (for front and rear).

An extra mute position for the front, the rear or for all channels is built in. The last function may be used for muting during preset selection. No external interface is required between the microcomputer and this circuit, for all switching and controlling functions are controllable via the two-wire I^2C-bus.

The separate mute-pin allows to switch the fader into mute position without using the I^2C-bus.

The on chip power-on reset sets the TEA6330T into the general mute mode.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134). Ground pins 3 and 10 connected together.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 18)	0	10	V
P_{tot}	total power dissipation	0	700	mW
T_{stg}	storage temperature range	–55	150	°C
T_{amb}	operating ambient temperature range	–40	85	°C
V_{ESD}	electrostatic handling* for all pins	–	±300	V
	electrostatic handling** for all pins	–	±4000	V

* Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

** Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

CHARACTERISTICS

V_P = 8.5 V; load resistors at audio outputs 10 kΩ, f_i = 1 kHz (R_S = 600 Ω), bass and treble in linear position, fader in off position and T_{amb} = 25 °C; measurements taken in Fig.1 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 18)		7	8.5	10	V
I_P	supply current		–	26	–	mA
V_{ref}	reference voltage (pin 20)		0.45 V_P	0.5 V_P	0.55 V_P	V
V_O	DC voltage at output (pins 7, 8, 13, 14)		–	0.5 V_P	–	V
Measurements over all						
V_i	maximum AF input level for THD = 2 % at pins 2 and 19 (RMS value)	G_v = –66 to –6 dB and V_P = 8.1 V	2	–	–	V
V_o	maximum AF output level for THD = 2% at pins 7, 8, 13, 14 (RMS value)	G_v = –4 to +20 dB and V_P = 8.1 V	1.1	–	–	V
G_v	maximum gain by volume setting		19	20	21	dB
B	frequency response	–1 dB roll-off frequency	–	35 to 20000	–	Hz
α_{CR}	crosstalk attenuation	f = 250 to 10000 Hz; G_v = 0 dB	70	90	–	dB
THD	total harmonic distortion	f = 20 to 12500 Hz				
	$V_{i\,(RMS)}$ = 50 mV	G_v = +20 dB	–	0.1	0.3	%
	$V_{i\,(RMS)}$ = 500 mV	G_v = 0 dB	–	0.05	0.2	%
	$V_{i\,(RMS)}$ = 1.6 V	G_v = –10 dB	–	0.2	0.5	%
RR	ripple rejection for V_R < 200 mV RMS	G_v = 0 dB				
		f = 100 Hz	–	70	–	dB
		f = 40 Hz to 3 kHz	–	60	–	dB
		f = 3 to 12.5 kHz	–	50	–	dB
P_N	noise power at output of a 25 W powerstage with 26 dB gain (only contribution of TEA6330T)	mute position (V_9 = 0)	–	–	10	nW
α_{BUS}	crosstalk attenuation between SDA, SCL and signal output (20 log V_{BUS} (p-p)/V_o RMS)	G_v = 0 dB	–	110	–	dB
S/N(W)	weighted signal-to-noise ratio for	CCIR 468-2 quasi peak for 6 W power amplifier				
	V_i = 50 mV RMS	P_o = 50 mW	–	65	–	dB
	V_i = 500 mV RMS	P_o = 50 mW	–	67	–	dB
	V_i = 50 mV RMS	P_o = 1 W	65	72	–	dB
	V_i = 500 mV RMS	P_o = 1 W	71	78	–	dB
	V_i = 50 mV RMS	P_o = 6 W; Fig.9	–	72	–	dB
	V_i = 500 mV RMS	P_o = 6 W; Fig.9	–	86	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Audio frequency outputs QLF, QRF, QLR and QRR						
V_o	maximum output signal (RMS value)		1.1	–	–	V
R_o	output resistance (pins 7, 8, 13 and 14)		–	100	150	Ω
R_L	admissible output load resistor	to ground or V_{CC}	7.5	–	–	kΩ
C_L	admissible output load capacitor		–	–	2.5	nF
$V_{N(W)}$	weighted noise voltage at output	CCIR 468-2 ; Fig.8 quasi peak				
	for maximum gain	G_v = +20 dB	–	110	220	μV
	for 0 dB gain	G_v = 0 dB	–	25	50	μV
	for minimum gain	G_v = –66 dB	–	19	38	μV
	for mute position	(V_9 = 0)	–	11	22	μV
Volume control		R_G = 600Ω				
R_I	input resistance (pins 2 and 19)		35	50	65	kΩ
G_v	volume control range	Table 2	–66	–	+20	dB
ΔG_v	step width		–	2	-	dB
	gain set error	G_v = –50 to +20 dB	–	–	2	dB
		G_v = –66 to –50 dB	–	–	3	dB
	gain tracking error	balance in mid position	–	–	2	dB
α_{mute}	mute attenuation at volume mute	set mute-bits	76	90	–	dB
Bass control						
G_v	controllable bass range	Table 3; Fig.6				
	maximum boost	f = 40 Hz	14	15	16	dB
	maximum boost	f = 100 Hz	12	13	14	dB
	maximum attenuation	f = 40 Hz	11	12	13	dB
	maximum attenuation	f = 100 Hz	10	11	12	dB
ΔG_v	step width	f = 40 Hz	2.5	3	3.5	dB
Treble control						
G_v	controllable treble range	Table 4; Fig.7				
	maximum boost	f = 10 kHz	9	10	11	dB
	maximum boost	f = 15 kHz	11	12	13	dB
	maximum boost	f > 15 kHz	–	–	15	dB
	maximum attenuation	f = 10 kHz	9	10	11	dB
	maximum attenuation	f = 15 kHz	11	12	13	dB
ΔG_v	step width	f = 15 kHz	2.5	3	3.5	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Fader control						
G_v	fader control range	Table 5		0 to		
			–	–30	–	dB
	step width		1.5	2	2.5	dB
α_{MUTE}	mute attenuation	GMB-bit = 1; Table 6	74	84	–	dB
ΔV_o	DC offset output voltage (pins 7, 8, 13, 14)					
	between any adjoining volume step					
	and any step to mute	G_v = –66 to 0 dB	–	0.2	10	mV
		G_v = 0 to +20 dB	–	2	15	mV
	in any treble and fader position	G_v = –66 to 0 dB	–	–	10	mV
	in any bass position	G_v = –66 to 0 dB	–	–	10	mV
External mute (pin 9)						
V_9	input voltage for MUTE-ON (LOW)	fader is switched into				
		general mute position	0	–	1.5	V
	input voltage for MUTE-OFF (HIGH)	Tables 2 and 5	3	–	V_P	V
	input voltage for MUTE-OFF	pin 9 open-circuit	–	5	–	V
I_9	input current		–	–	±10	µA
I^2C-bus, SCL and SDA (pins 11 and 12)						
$V_{11, 12}$	input voltage HIGH-level		3	–	V_P	V
	input voltage LOW-level		0	–	1.5	V
$I_{11, 12}$	input current		–	–	±10	µA
V_{ACK}	output voltage at acknowledge (pin 12)	I_{12} = –3 mA	–	–	0.4	V
Power-on reset, when reset is active the GMU-bit (general mute) is set and the bus receiver is in reset position						
V_P	supply voltage for start of reset	increasing voltage	–	–	2.5	V
	supply voltage for end of reset	increasing voltage	5.2	6.0	6.8	V
	supply voltage for start of reset	decreasing voltage	4.2	5.0	5.8	V

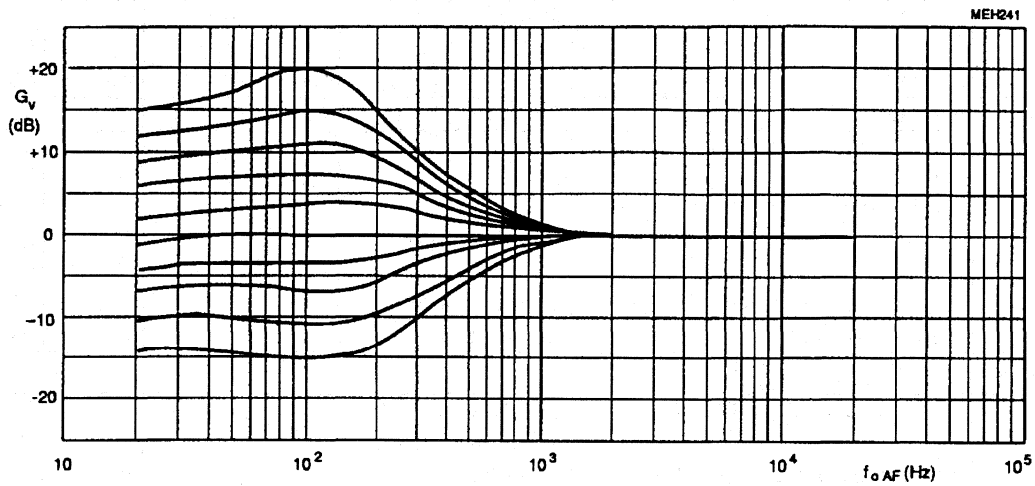


Fig.5 Bass control with enhanced control range (T-filter coupling, Fig.1).

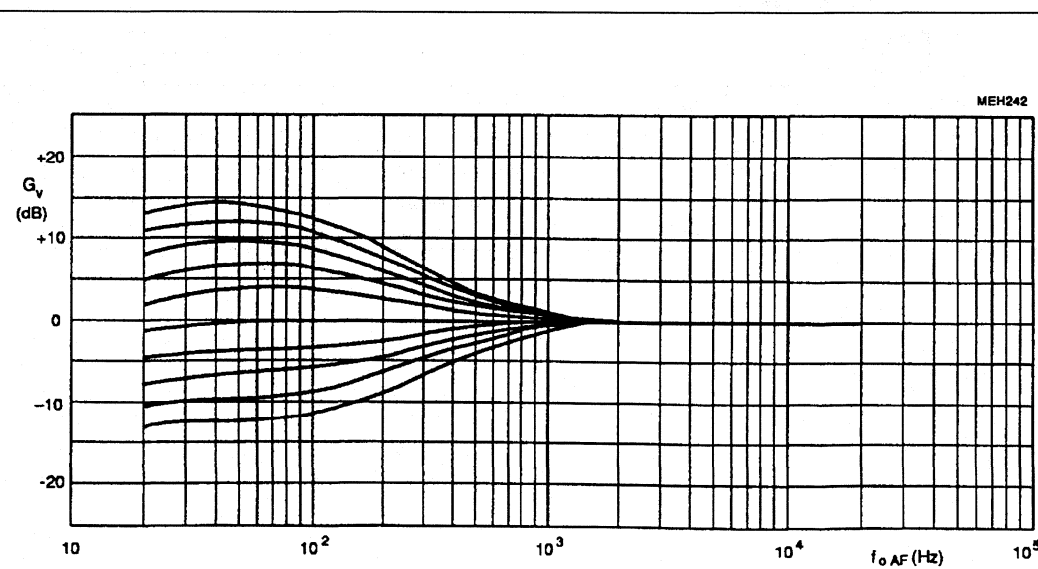


Fig.6 Bass control with normal control range (Fig.1).

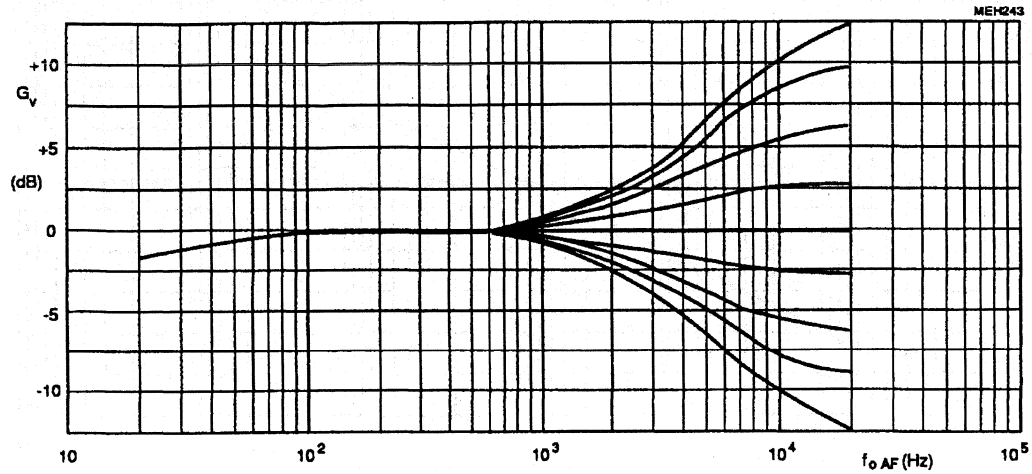


Fig.7 Treble control.

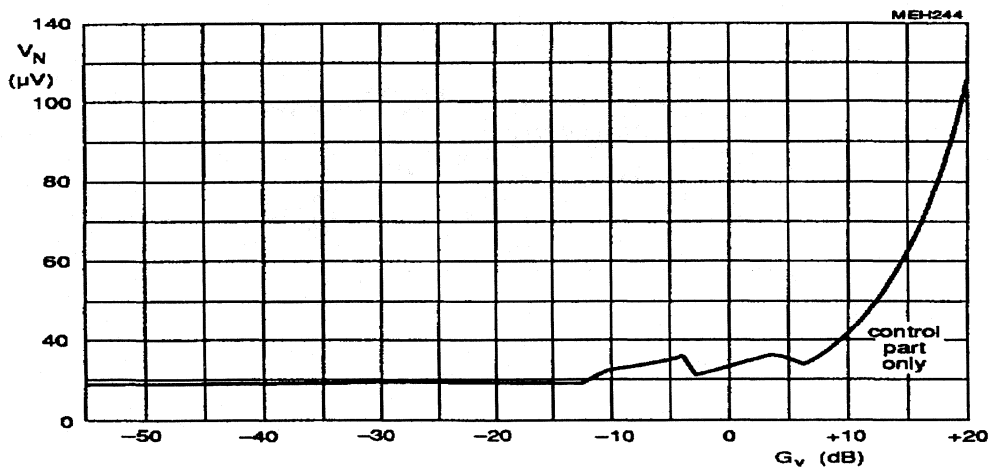


Fig.8 Noise voltage on outputs (CCIR 468-2 weighted, quasi-peak).

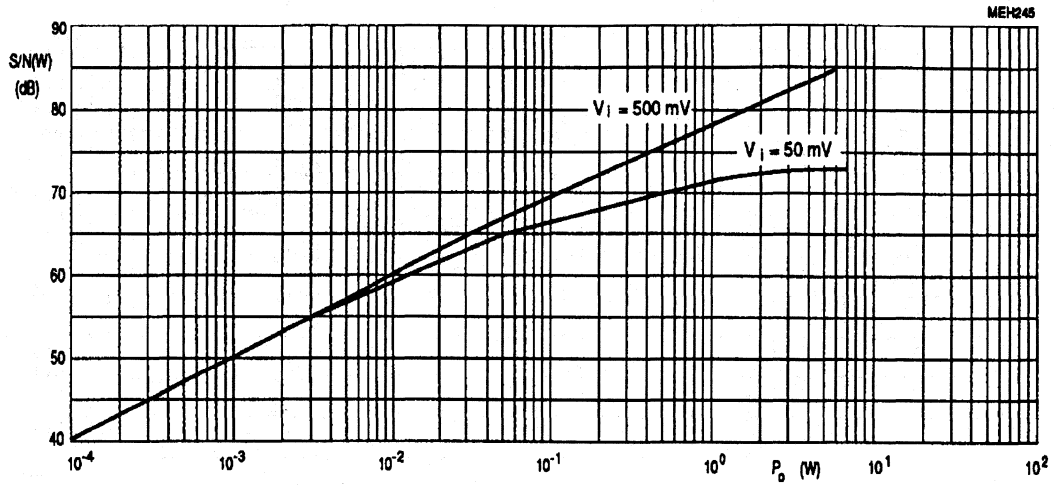


Fig.9 Signal-to-noise ratio (CCIR 468-2 weighted, quasi-peak) for TEA6330T with a 6 W power amplifier (20 dB gain, Fig.10). Measurements without noise contribution of the power amplifier.

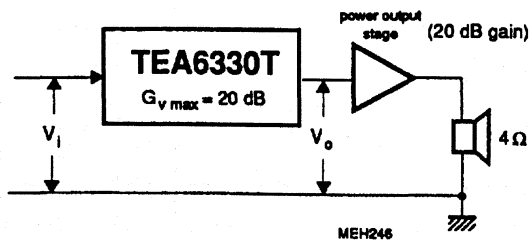


Fig.10 Signal-to-noise ratio measurement (Fig.9) with V_i = 50 mV RMS, V_o = 500 mV RMS for P_{max} = 6 W.

I²C-BUS PROTOCOL

I²C-bus format

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA	P

S	=	start condition
SLAVE ADDRESS	=	**1000 000X**
A	=	acknowledge, generated by the slave
SUBADDRESS	=	subaddress byte, Table 1
DATA	=	data byte, Table 1
P	=	stop condition
X	=	read/write control bit X = 0, order to write (the circuit is slave receiver only)

If more than 1 byte DATA are transmitted, then auto-increment of the subaddress is performed.

Byte organisation

Table 1 I²C-bus transmission

FUNCTION	SUBADDRESS BYTE								DATA BYTE							
									D7	D6	D5	D4	D3	D2	D1	D0
volume left	0	0	0	0	0	0	0	0	0	0	VL5	VL4	VL3	VL2	VL1	VL0
volume right	0	0	0	0	0	0	0	1	0	0	VR5	VR4	VR3	VR2	VR1	VR0
bass	0	0	0	0	0	0	1	0	0	0	0	0	BA3	BA2	BA1	BA0
treble	0	0	0	0	0	0	1	1	0	0	0	0	TR3	TR2	TR1	TR0
fader	0	0	0	0	0	1	0	0	0	0	MFN	FCH	FA3	FA2	FA1	FA0
audio switch	0	0	0	0	0	1	0	1	GMU	EQN	0	0	0	0	0	0

Function of the bits:

VL0	to	VL5	volume control of left channel (balance control)
VR0	to	VR5	volume control of right channel (balance control)
BA0	to	BA3	bass control of both channels
TRO	to	TR3	treble control of both channels
FA0	to	FA3	fader control front to rear
FCH			select fader channels front or rear
MFN			mute control of the selected channels front or rear
GMU			mute control, general mute
EQN			equalizer switchover (0 = equalizer-on)

Table 2(a) Volume setting LEFT

G_V	DATA					
DB	VL5	VL4	VL3	VL2	VL1	VL0
+20	1	1	1	1	1	1
+18	1	1	1	1	1	0
+16	1	1	1	1	0	1
+14	1	1	1	1	0	0
+12	1	1	1	0	1	1
+10	1	1	1	0	1	0
+8	1	1	1	0	0	1
+6	1	1	1	0	0	0
+4	1	1	0	1	1	1
+2	1	1	0	1	1	0
0	1	1	0	1	0	1
–2	1	1	0	1	0	0
–4	1	1	0	0	1	1
–6	1	1	0	0	1	0
–8	1	1	0	0	0	1
–10	1	1	0	0	0	0
–12	1	0	1	1	1	1
–14	1	0	1	1	1	0
–16	1	0	1	1	0	1
–18	1	0	1	1	0	0
–20	1	0	1	0	1	1
–22	1	0	1	0	1	0
–24	1	0	1	0	0	1
–26	1	0	1	0	0	0
–28	1	0	0	1	1	1
–30	1	0	0	1	1	0

G_V	DATA					
DB	VL5	VL4	VL3	VL2	VL1	VL0
–32	1	0	0	1	0	1
–34	1	0	0	1	0	0
–36	1	0	0	0	1	1
–38	1	0	0	0	1	0
–40	1	0	0	0	0	1
–42	1	0	0	0	0	0
–44	0	1	1	1	1	1
–46	0	1	1	1	1	0
–48	0	1	1	1	0	1
–50	0	1	1	1	0	0
–52	0	1	1	0	1	1
–54	0	1	1	0	1	0
–56	0	1	1	0	0	1
–58	0	1	1	0	0	0
–60	0	1	0	1	1	1
–62	0	1	0	1	1	0
–64	0	1	0	1	0	1
–66	0	1	0	1	0	0
mute left	0	1	0	0	1	1
mute left	0	1	0	0	1	0
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mute left	0	0	0	0	0	0

Table 2(b) Volume setting RIGHT

G_V	DATA					
DB	VR5	VR4	VR3	VR2	VR1	VL0
+20	1	1	1	1	1	1
+18	1	1	1	1	1	0
+16	1	1	1	1	0	1
+14	1	1	1	1	0	0
+12	1	1	1	0	1	1
+10	1	1	1	0	1	0
+8	1	1	1	0	0	1
+6	1	1	1	0	0	0
+4	1	1	0	1	1	1
+2	1	1	0	1	1	0
0	1	1	0	1	0	1
−2	1	1	0	1	0	0
−4	1	1	0	0	1	1
−6	1	1	0	0	1	0
−8	1	1	0	0	0	1
−10	1	1	0	0	0	0
−12	1	0	1	1	1	1
−14	1	0	1	1	1	0
−16	1	0	1	1	0	1
−18	1	0	1	1	0	0
−20	1	0	1	0	1	1
−22	1	0	1	0	1	0
−24	1	0	1	0	0	1
−26	1	0	1	0	0	0
−28	1	0	0	1	1	1
−30	1	0	0	1	1	0

G_V	DATA					
DB	VR5	VR4	VR3	VR2	VR1	VL0
−32	1	0	0	1	0	1
−34	1	0	0	1	0	0
−36	1	0	0	0	1	1
−38	1	0	0	0	1	0
−40	1	0	0	0	0	1
−42	1	0	0	0	0	0
−44	0	1	1	1	1	1
−46	0	1	1	1	1	0
−48	0	1	1	1	0	1
−50	0	1	1	1	0	0
−52	0	1	1	0	1	1
−54	0	1	1	0	1	0
−56	0	1	1	0	0	1
−58	0	1	1	0	0	0
−60	0	1	0	1	1	1
−62	0	1	0	1	1	0
−64	0	1	0	1	0	1
−66	0	1	0	1	0	0
mute right	0	1	0	0	1	1
mute right	0	1	0	0	1	0
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mute right	0	0	0	0	0	0

Table 3(a)
Bass setting with equalizer passive (EQN =1)

G_V	DATA			
DB	D3	D2	D1	D0
+15	1	1	1	1
+15	1	1	1	0
+15	1	1	0	1
+15	1	1	0	0
+12	1	0	1	1
+9	1	0	1	0
+6	1	0	0	1
+3	1	0	0	0
0	0	1	1	1
–3	0	1	1	0
–6	0	1	0	1
–9	0	1	0	0
–12	0	0	1	1
–12	0	0	1	0
–12	0	0	0	0

Table 3(b)
Bass setting with equalizer active (EQN = 0)

G_V	DATA			
DB	D3	D2	D1	D0
+15	1	1	1	1
+15	1	1	1	0
+15	1	1	0	1
+15	1	1	0	0
+12	1	0	1	1
+9	1	0	1	0
+6	1	0	0	1
+3	1	0	0	0
0	0	1	1	1
0	0	1	1	0
0	0	1	0	1
0	0	1	0	0
0	0	0	1	1
0	0	0	1	0
0	0	0	0	0

Table 4(a)
Treble setting with equalizer passive (EQN = 1)

G_V	DATA			
DB	D3	D2	D1	D0
+12	1	1	1	1
+12	1	1	1	0
+12	1	1	0	1
+12	1	1	0	0
+12	1	0	1	1
+9	1	0	1	0
+6	1	0	0	1
+3	1	0	0	0
0	0	1	1	1
–3	0	1	1	0
–6	0	1	0	1
–9	0	1	0	0
–12	0	0	1	1
–12	0	0	1	0
–12	0	0	0	0

Table 4(b)
Treble setting with equalizer active (EQN = 0)

G_V	DATA			
DB	D3	D2	D1	D0
0	1	1	1	1
0	1	1	1	0
0	1	1	0	1
0	1	1	0	0
0	1	0	1	1
0	1	0	1	0
0	1	0	0	1
0	1	0	0	0
0	0	1	1	1
0	0	1	1	0
0	0	1	0	1
0	0	1	0	0
0	0	0	1	1
0	0	0	1	0
0	0	0	0	0

Table 5(a) Fader function front

SETTING		DATA					
FRONT DB	REAR DB	MFN	FCH	FA3	FA2	FA1	FA0
		fader-off					
0	0	1	1	1	1	1	1
0	0	0	1	1	1	1	1
		fader-front					
–2	0	1	1	1	1	1	0
–4	0	1	1	1	1	0	1
–6	0	1	1	1	1	0	0
–8	0	1	1	1	0	1	1
–10	0	1	1	1	0	1	0
–12	0	1	1	1	0	0	1
–14	0	1	1	1	0	0	0
–16	0	1	1	0	1	1	1
–18	0	1	1	0	1	1	0
–20	0	1	1	0	1	0	1
–22	0	1	1	0	1	0	0
–24	0	1	1	0	0	1	1
–26	0	1	1	0	0	1	0
–28	0	1	1	0	0	0	1
–30	0	1	1	0	0	0	0
		mute front					
–84	0	0	1	1	1	1	0
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–84	0	0	1	0	0	0	0

Table 5(b) Fader function rear

SETTING		DATA					
FRONT DB	REAR DB	MFN	FCH	FA3	FA2	FA1	FA0
		fader-off					
0	0	1	0	1	1	1	1
0	0	0	0	1	1	1	1
		fader rear					
0	–2	1	0	1	1	1	0
0	–4	1	0	1	1	0	1
0	–6	1	0	1	1	0	0
0	–8	1	0	1	0	1	1
0	–10	1	0	1	0	1	0
0	–12	1	0	1	0	0	1
0	–14	1	0	1	0	0	0
0	–16	1	0	0	1	1	1
0	–18	1	0	0	1	1	0
0	–20	1	0	0	1	0	1
0	–22	1	0	0	1	0	0
0	–24	1	0	0	0	1	1
0	–26	1	0	0	0	1	0
0	–28	1	0	0	0	0	1
0	–30	1	0	0	0	0	0
		mute rear					
0	–84	0	0	1	1	1	0
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	---			---			---
	---			---			---
0	–84	0	0	0	0	0	0

Table 6 Mute control

MUTE CONTROL	DATA GMU-BIT	REMARKS
active	1	outputs QLF, QLR, QRF and QRR are muted
passive	0	no general mute

Table 7 Equalizer

EQUALIZER CONTROL	DATA EQN-BIT	REMARKS
active	0	signal outputs for equalizer are pins 4 and 17, inputs are pins 6 and 15; Tables 3(b) and 4(b)
passive	1	no general mute; Tables 3(a) and 4(a)

PACKAGE INFORMATION

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DIP 1818
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PLCC 1827
QFP 1830
SDIP 1836
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Soldering 1852

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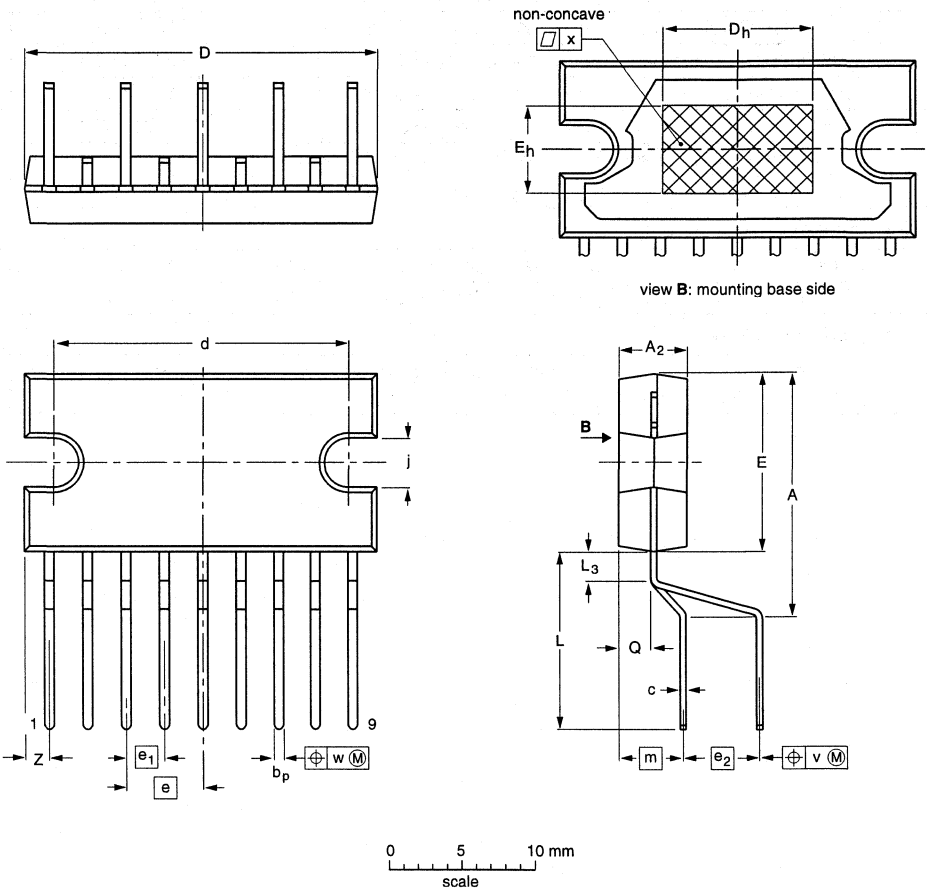
NAME	DESCRIPTION	VERSION	PAGE
DBS (DIL-bent-SIL)			
DBS9P	plastic DIL-bent-SIL power package; 9 leads (lead length 12 mm)	SOT157-2	
DBS13P	plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm)	SOT141-6	
DIP (dual in-line package)			
DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1	
DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1	
DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1	
DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1	
HDIP (heat-dissipating dual in-line package)			
HDIP18	plastic heat-dissipating dual in-line package; 18 leads	SOT398-1	
LQFP (low profile quad flat package)			
LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2	
LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2	
LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1	
LQFP128	plastic low profile quad flat package; 128 leads; body 14 × 20 × 1.4 mm	SOT425-1	
PLCC (plastic leaded chip carrier)			
PLCC44	plastic leaded chip carrier; 44 leads	SOT187-2	
PLCC68	plastic leaded chip carrier; 68 leads	SOT188-2	
PLCC84	plastic leaded chip carrier; 84 leads	SOT189-2	
QFP (quad flat package)			
QFP44	plastic quad flat package; 44 leads (lead length 2.35 mm); body 14 × 14 × 2.2 mm	SOT205-1	
QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2	
QFP64	plastic quad flat package; 64 leads (lead length 1.6 mm); body 14 × 14 × 2.7 mm	SOT393-1	
QFP80	plastic quad flat package; 80 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT318-2	
QFP80	plastic quad flat package; 80 leads (lead length 2.35 mm); body 14 × 20 × 2.8 mm	SOT318-3	
QFP100	plastic quad flat package; 100 leads (lead length 1.95 mm); body 14 × 20 × 2.7 mm; high stand-off height	SOT317-1	
SDIP (shrink dual in-line package)			
SDIP32	plastic shrink dual in-line package; 32 leads (400 mil)	SOT232-1	
SDIP42	plastic shrink dual in-line package; 42 leads (600 mil)	SOT270-1	
SDIP52	plastic shrink dual in-line package; 52 leads (600 mil)	SOT247-1	
SIL (single in-line)			
SIL9MPF	plastic single in-line medium power package with fin; 9 leads	SOT110-1	
SIL9P	plastic single in-line power package; 9 leads	SOT131-2	

Package information — Package outlines

NAME	DESCRIPTION	VERSION	PAGE
SO (small outline)			
SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1	
SO8	plastic small outline package; 8 leads (straight); body width 3.9 mm	SOT96-2	
SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1	
SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1	
SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1	
SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1	
SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1	
SO32	plastic small outline package; 32 leads; body width 7.5 mm	SOT287-1	
SSOP (shrink small outline package)			
SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1	
SSOP28	plastic shrink small outline package; 28 leads; body width 5.3 mm	SOT341-1	
SQFP (shrink quad flat package)			
SQFP208	plastic shrink quad flat package; 208 leads (lead length 1.95 mm); body 28 × 28 × 3.4 mm	SOT316-1	

DBS

DBS9P: plastic DIL-bent-SIL power package; 9 leads (lead length 12 mm) SOT157-2



DIMENSIONS (mm are the original dimensions)

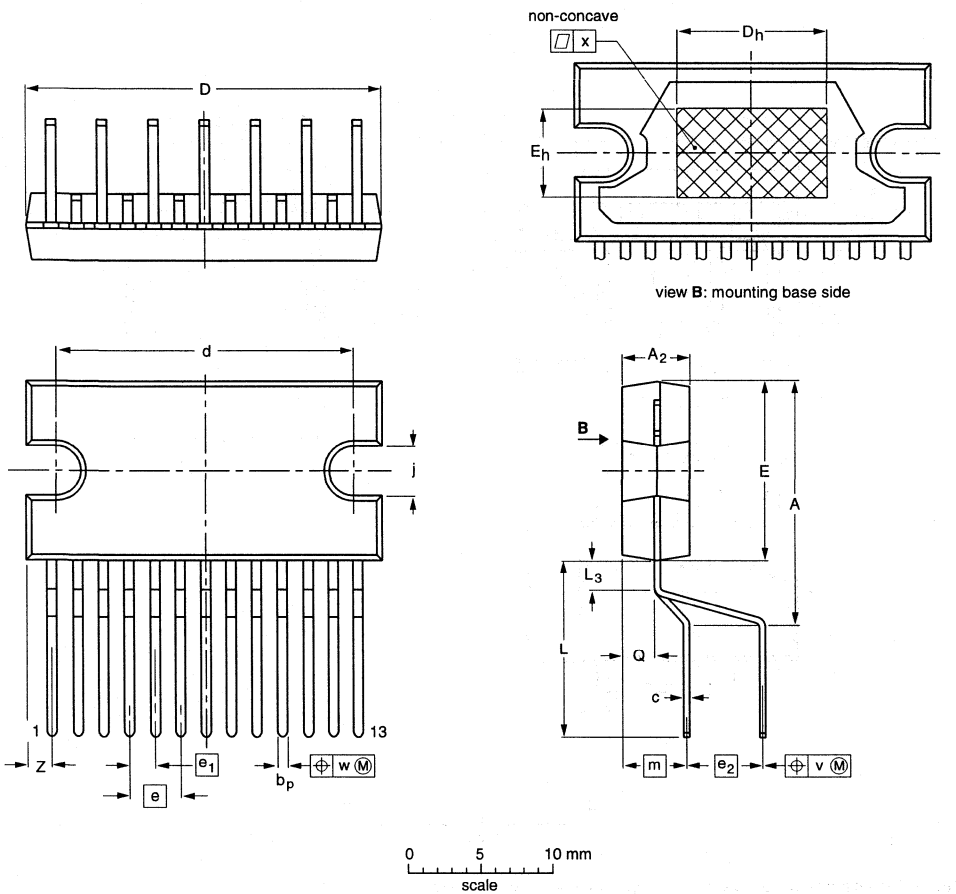
UNIT	A	A_2	b_p	c	$D^{(1)}$	d	D_h	$E^{(1)}$	e	e_1	e_2	E_h	j	L	L_3	m	Q	v	w	x	$Z^{(1)}$
mm	17.0 15.5	4.6 4.2	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	5.08	2.54	5.08	6	3.4 3.1	12.4 11.0	2.4 1.6	4.3	2.1 1.8	0.8	0.25	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT157-2						~~92-10-12~~ 95-03-11

DBS13P: plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm) SOT141-6



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_2	b_p	c	$D^{(1)}$	d	D_h	$E^{(1)}$	e	e_1	e_2	E_h	j	L	L_3	m	Q	v	w	x	$Z^{(1)}$
mm	17.0 15.5	4.6 4.2	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	3.4	1.7	5.08	6	3.4 3.1	12.4 11.0	2.4 1.6	4.3	2.1 1.8	0.8	0.25	0.03	2.00 1.45

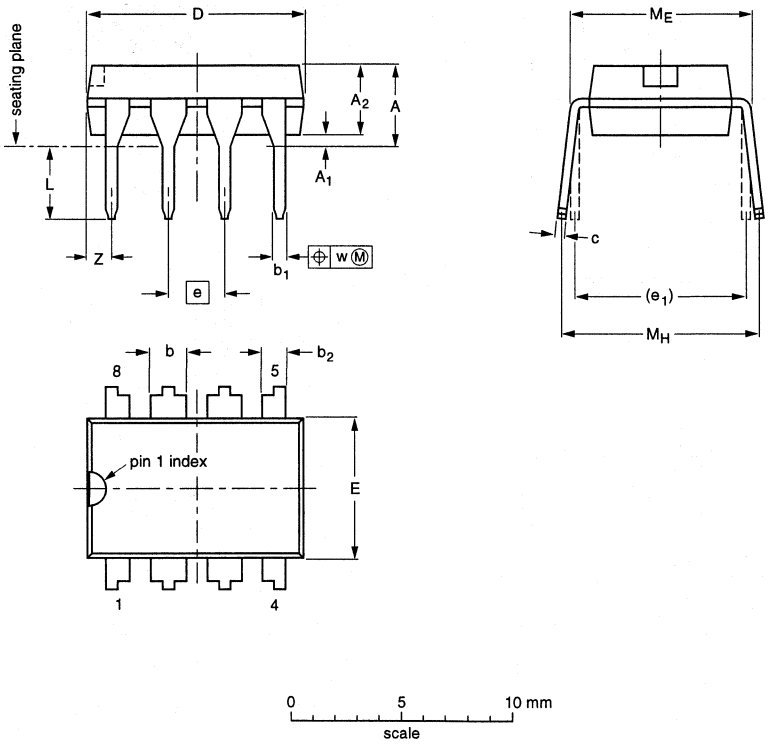
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT141-6						~~92-11-17~~ 95-03-11

DIP

DIP8: plastic dual in-line package; 8 leads (300 mil) SOT97-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

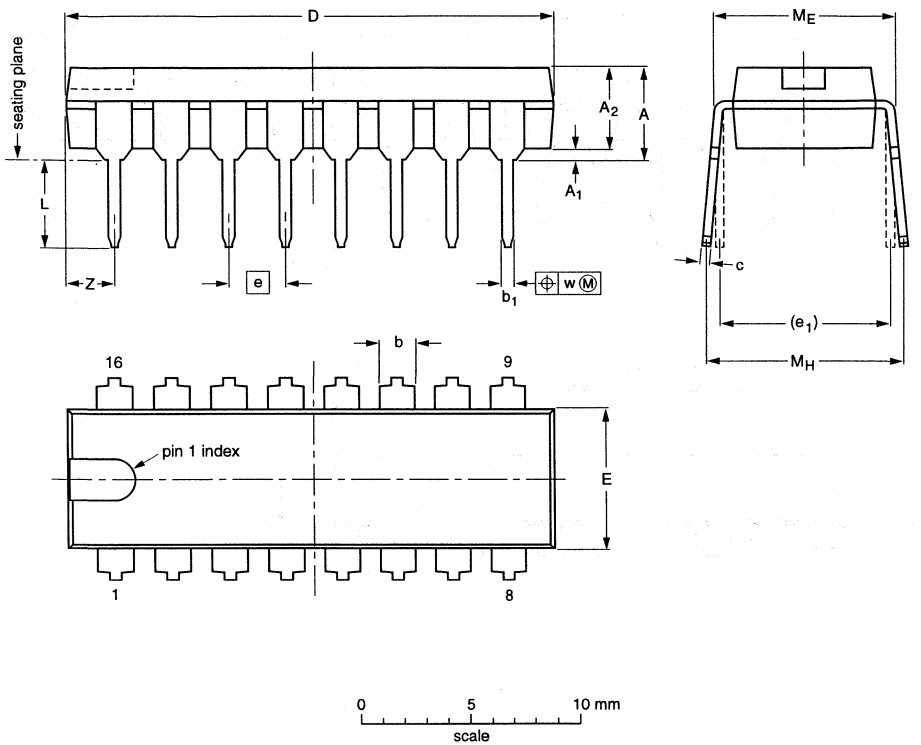
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.020	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT97-1	050G01	MO-001AN				~~92-11-17~~ 95-02-04

DIP16: plastic dual in-line package; 16 leads (300 mil); long body **SOT38-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

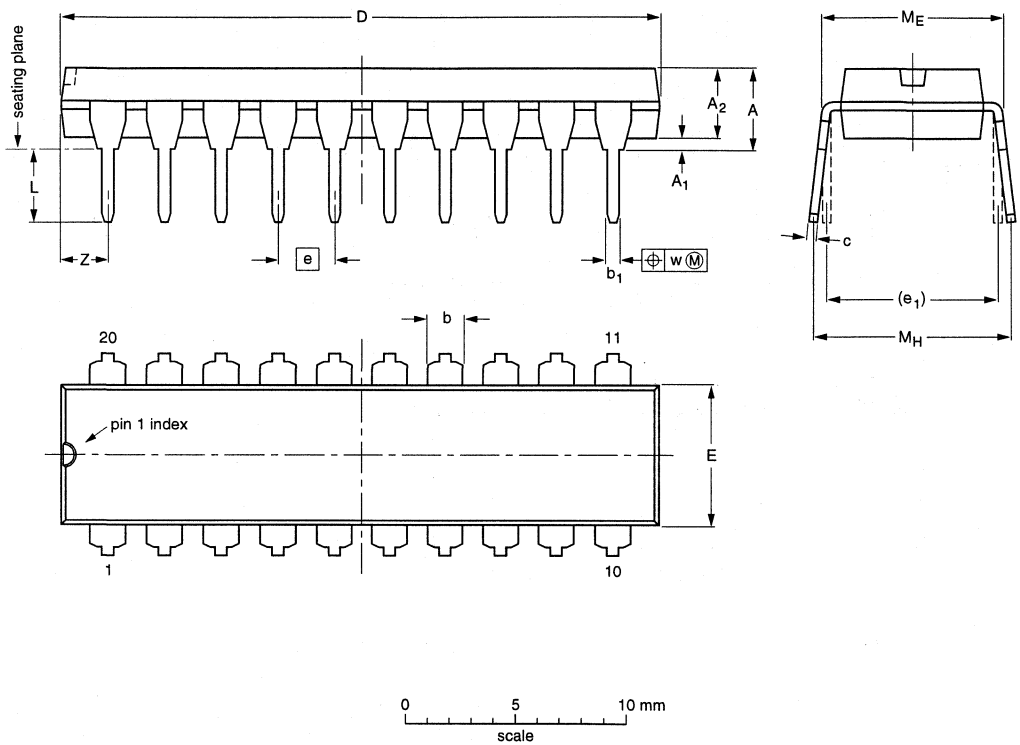
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
inches	0.19	0.020	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-1	050G09	MO-001AE				~~92-10-02~~ 95-01-19

DIP20: plastic dual in-line package; 20 leads (300 mil) SOT146-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

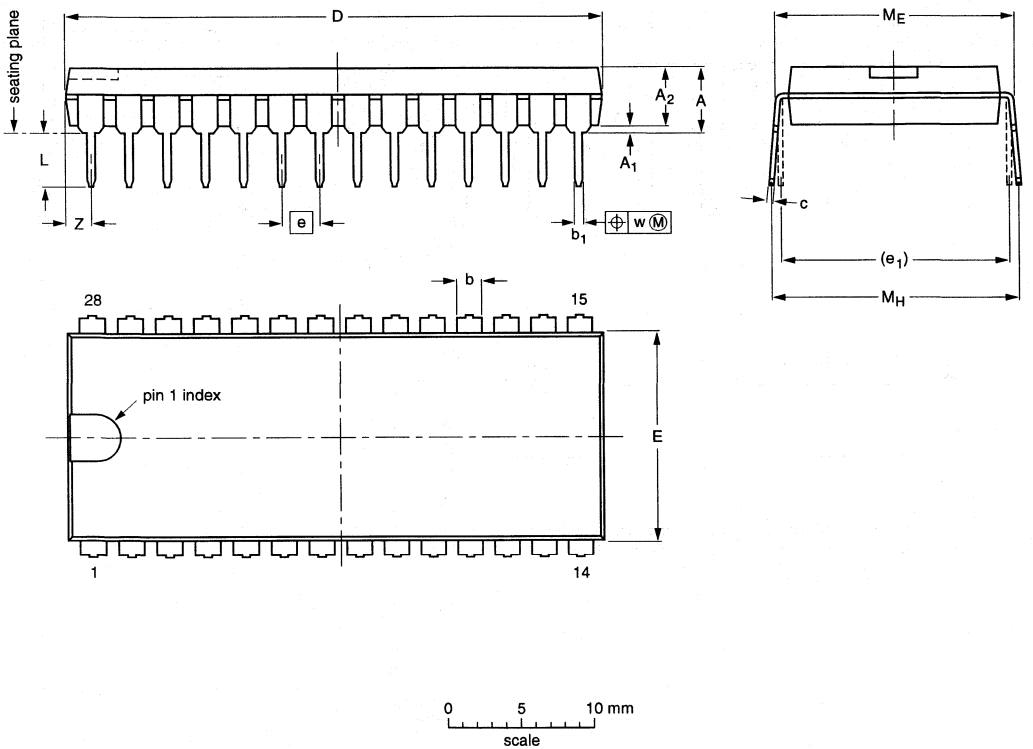
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			~~92-11-17~~ 95-05-24

DIP28: plastic dual in-line package; 28 leads (600 mil) **SOT117-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	36.0 35.0	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	1.7
inches	0.20	0.020	0.16	0.066 0.051	0.020 0.014	0.013 0.009	1.41 1.34	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.067

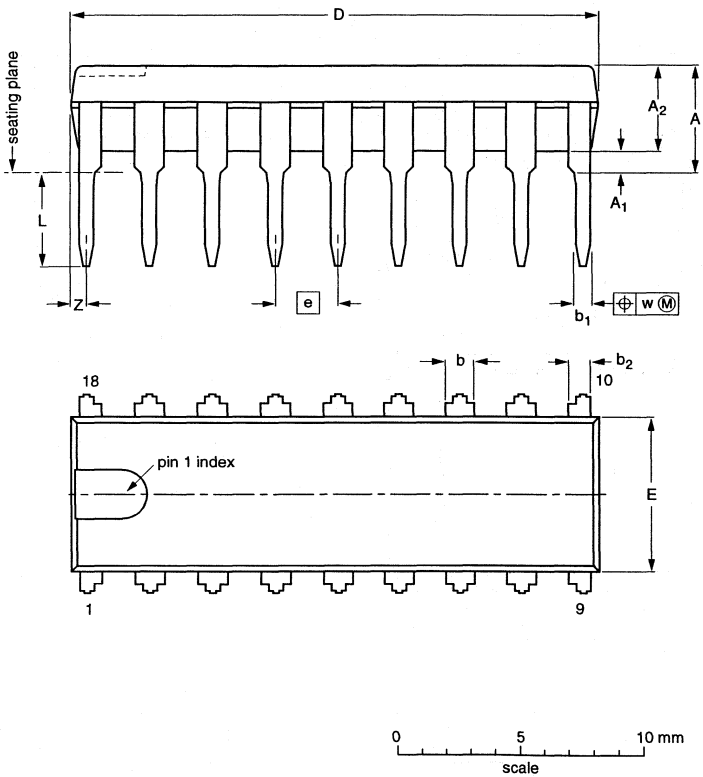
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT117-1	051G05	MO-015AH				~~92-11-17~~ 95-01-14

HDIP

HDIP18: plastic heat-dissipating dual in-line package; 18 leads SOT398-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D(1)	E(1)	e	e_1	L	M_E	M_H	w	Z(1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.67 0.50	1.05 0.75	0.47 0.38	21.85 21.35	6.5 6.2	2.54	7.62	3.9 3.1	8.32 8.02	8.7 7.7	0.25	1.0
inches	0.19	0.02	0.15	0.06 0.04	0.03 0.02	0.04 0.03	0.02 0.01	0.87 0.84	0.26 0.24	0.10	0.30	0.15 0.12	0.33 0.32	0.34 0.30	0.01	0.04

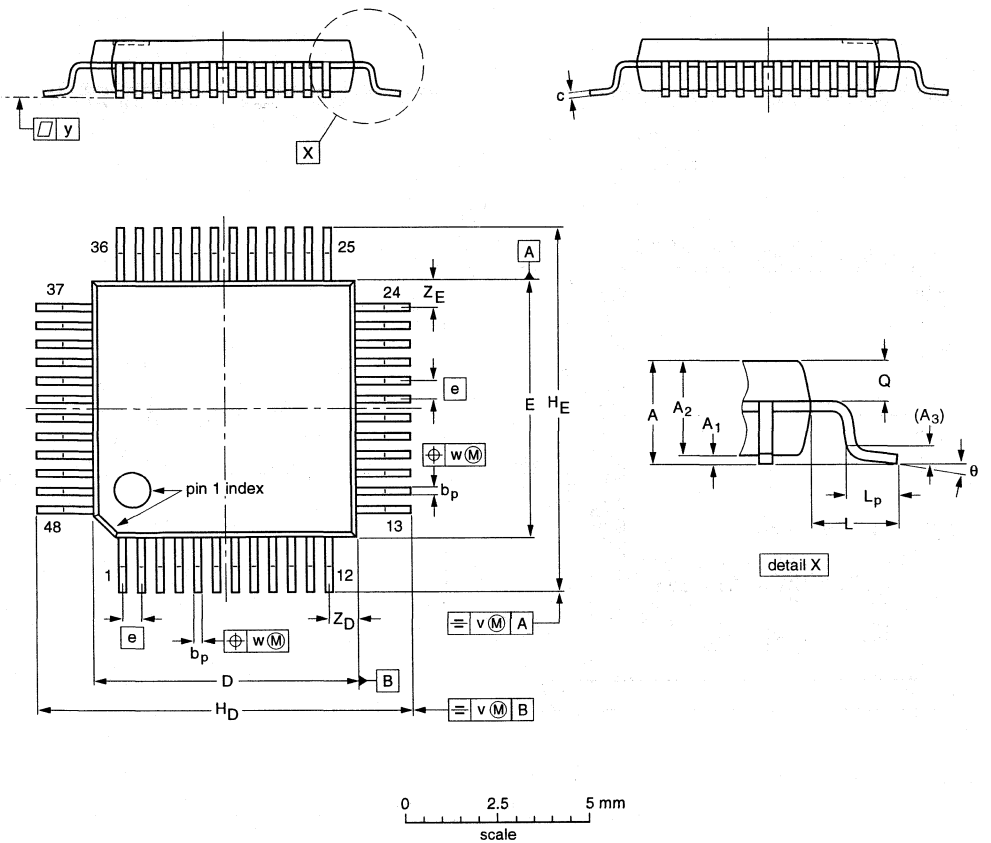
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT398-1						~~94-04-13~~ 95-01-25

LQFP

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm SOT313-2



DIMENSIONS (mm are the original dimensions)

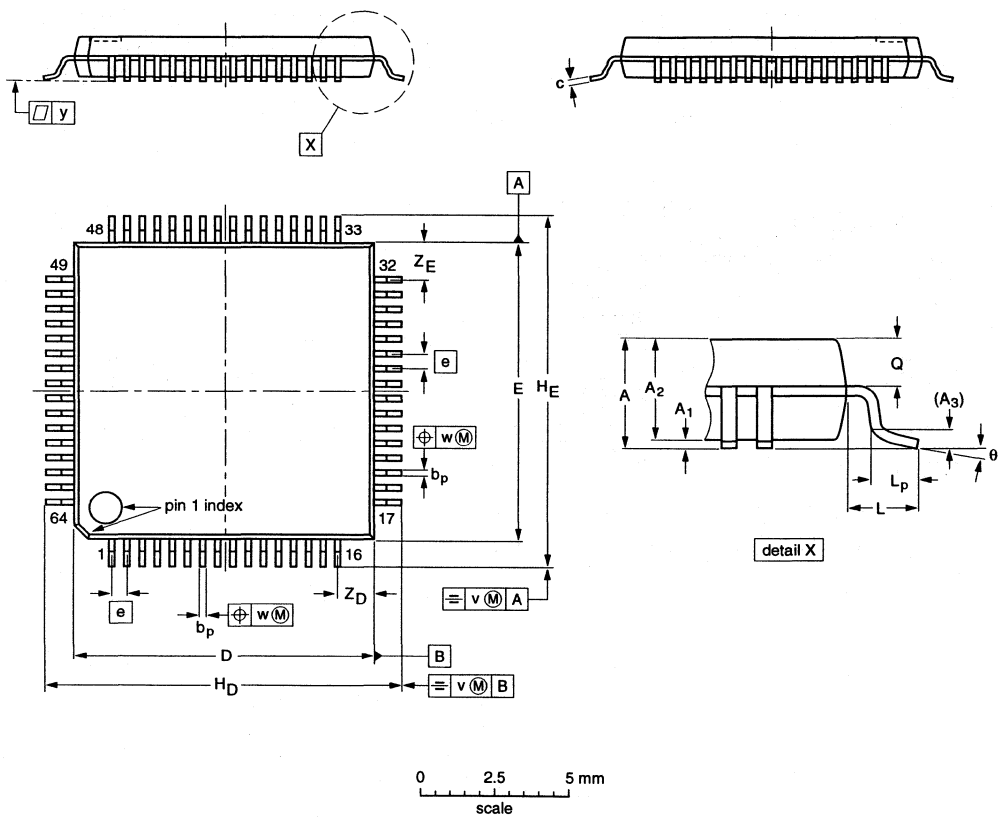
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.69 0.59	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT313-2						~~93-06-15~~ 94-12-19

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm **SOT314-2**



DIMENSIONS (mm are the original dimensions)

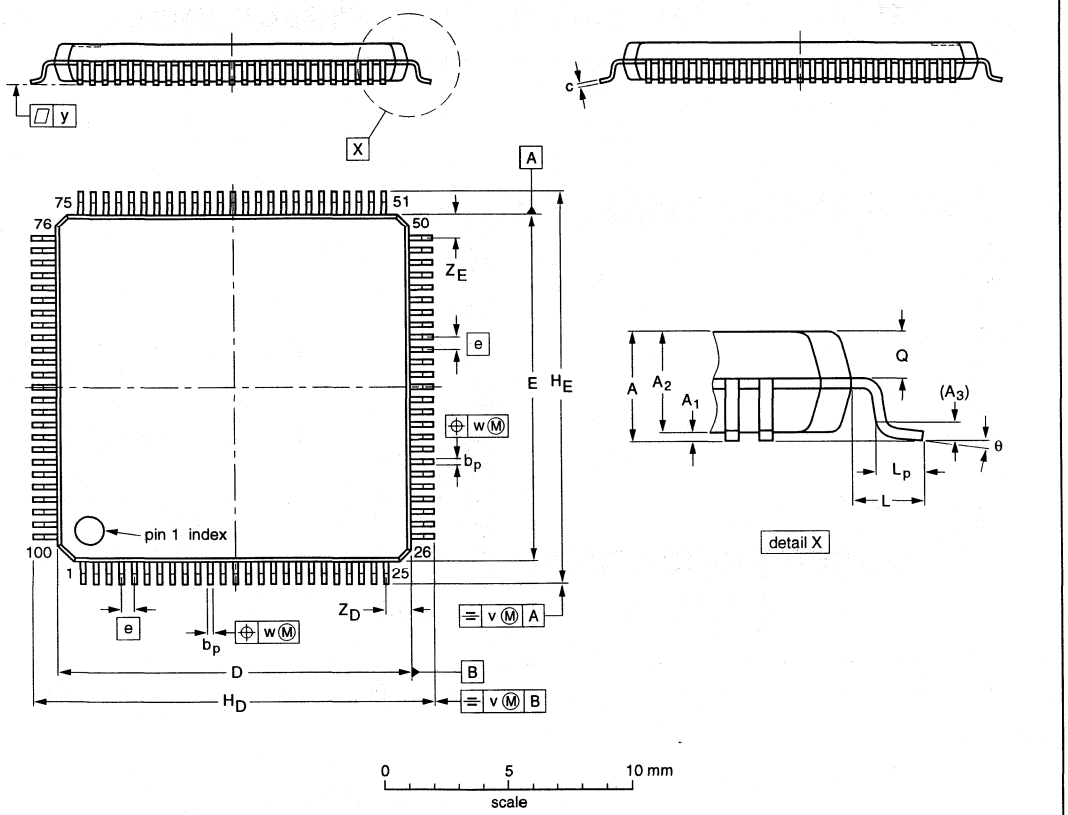
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1.0	0.75 0.45	0.69 0.59	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT314-2						~~94-01-07~~ 95-12-19

LQFP100: plastic low profile quad flat package; 100 leads; body 14 x 14 x 1.4 mm **SOT407-1**



DIMENSIONS (mm are the original dimensions)

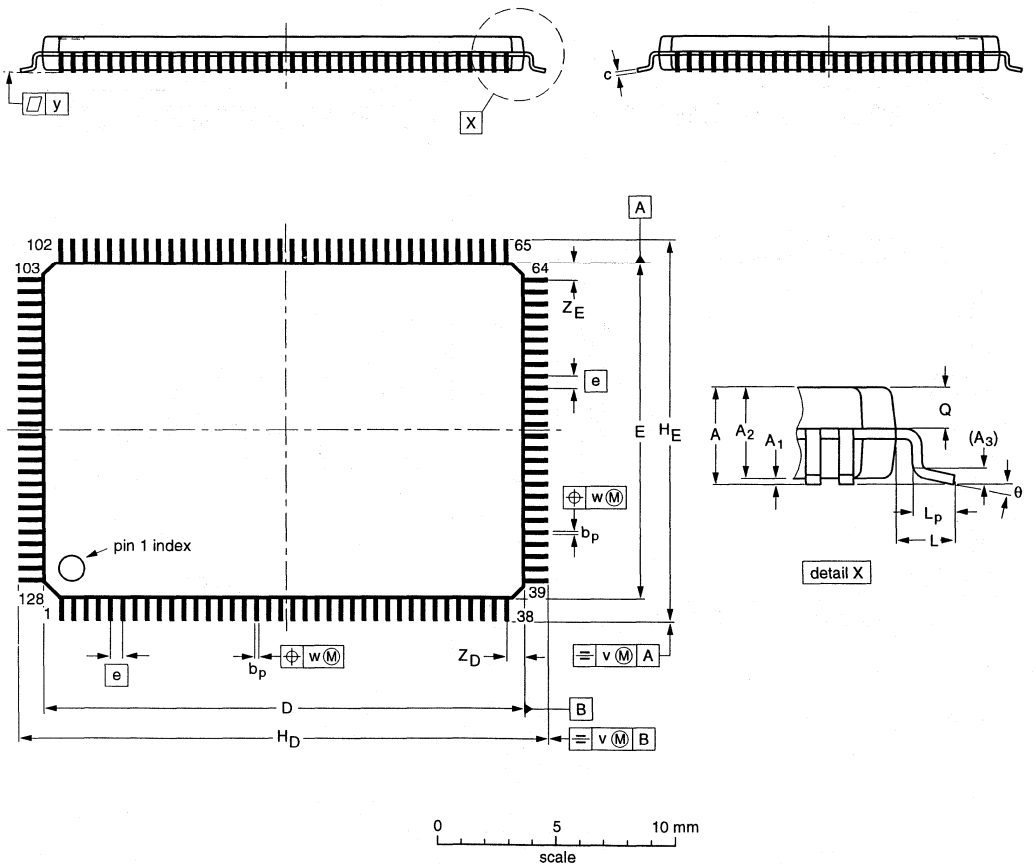
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.5 1.3	0.25	0.28 0.16	0.18 0.12	14.1 13.9	14.1 13.9	0.5	16.25 15.75	16.25 15.75	1.0	0.75 0.45	0.70 0.57	0.2	0.12	0.1	1.15 0.85	1.15 0.85	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT407-1						95-12-19

LQFP128: plastic low profile quad flat package; 128 leads; body 14 x 20 x 1.4 mm **SOT425-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	20.1 19.9	14.1 13.9	0.5	22.15 21.85	16.15 15.85	1.0	0.75 0.45	0.70 0.58	0.2	0.12	0.1	0.81 0.59	0.81 0.59	7° 0°

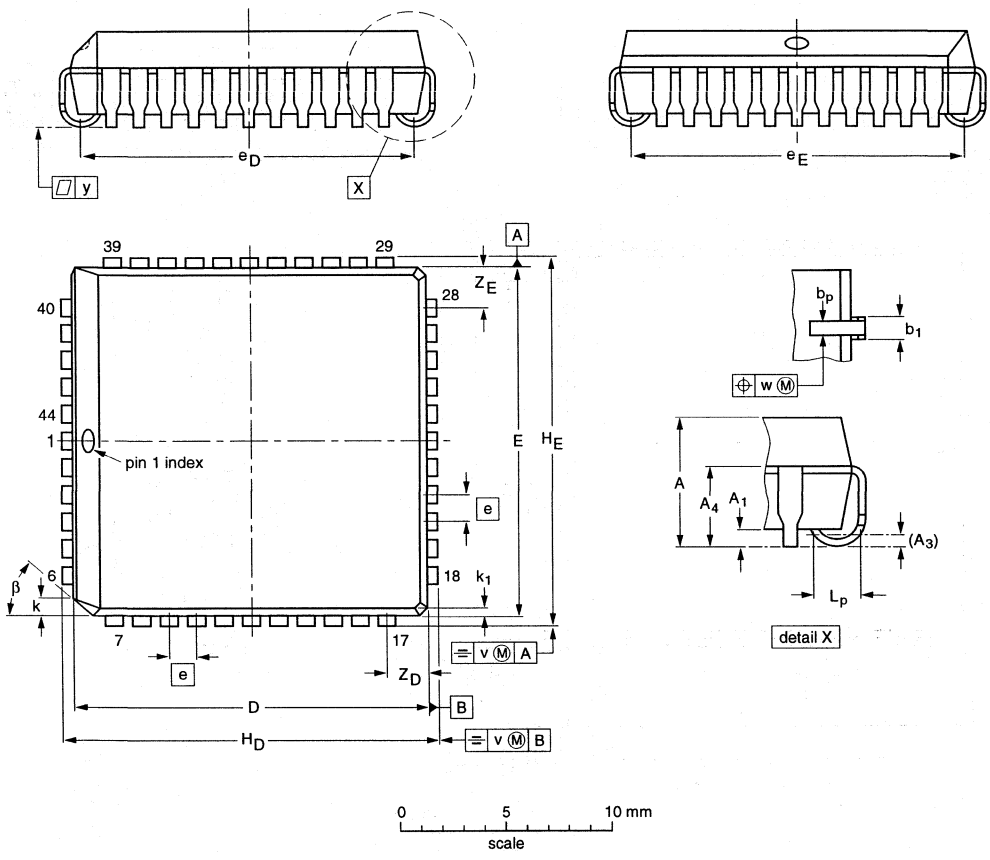
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT425-1						96-04-02

PLCC

PLCC44: plastic leaded chip carrier; 44 leads SOT187-2



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

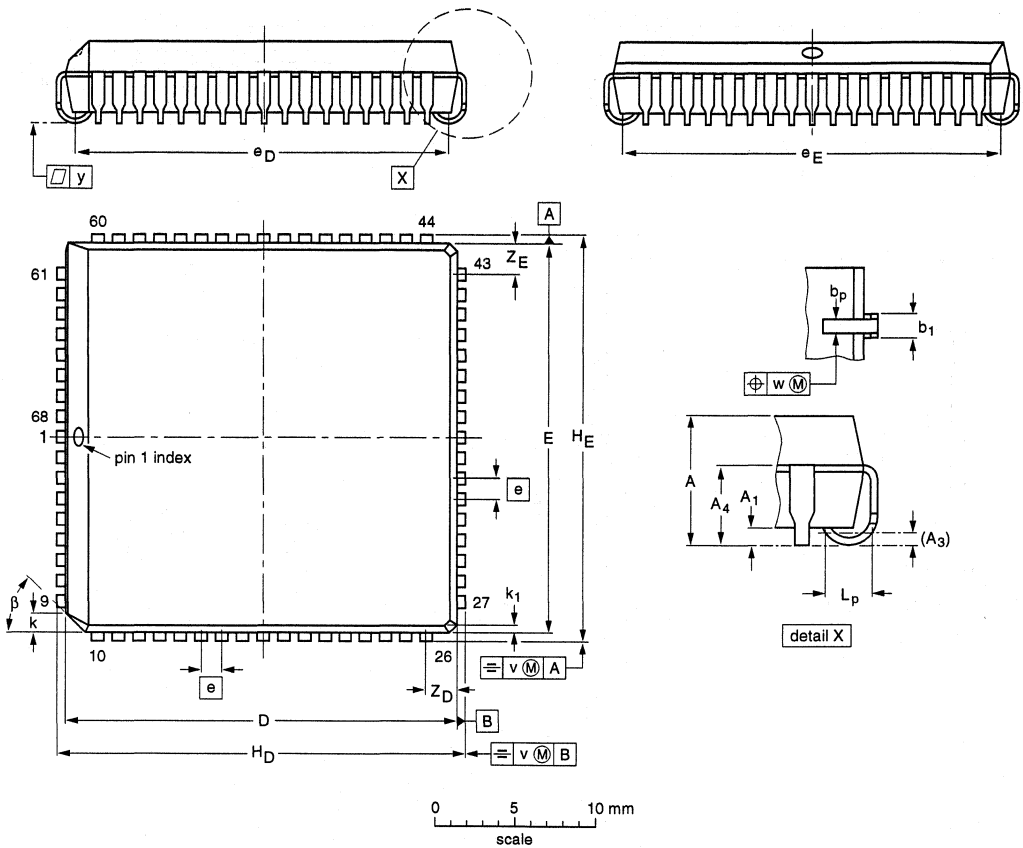
UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	k_1 max.	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	16.66 16.51	16.66 16.51	1.27	16.00 14.99	16.00 14.99	17.65 17.40	17.65 17.40	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.12	0.021 0.013	0.032 0.026	0.656 0.650	0.656 0.650	0.05	0.630 0.590	0.630 0.590	0.695 0.685	0.695 0.685	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT187-2	112E10	MO-047AC				~~92-11-17~~ 95-02-25

PLCC68: plastic leaded chip carrier; 68 leads SOT188-2



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

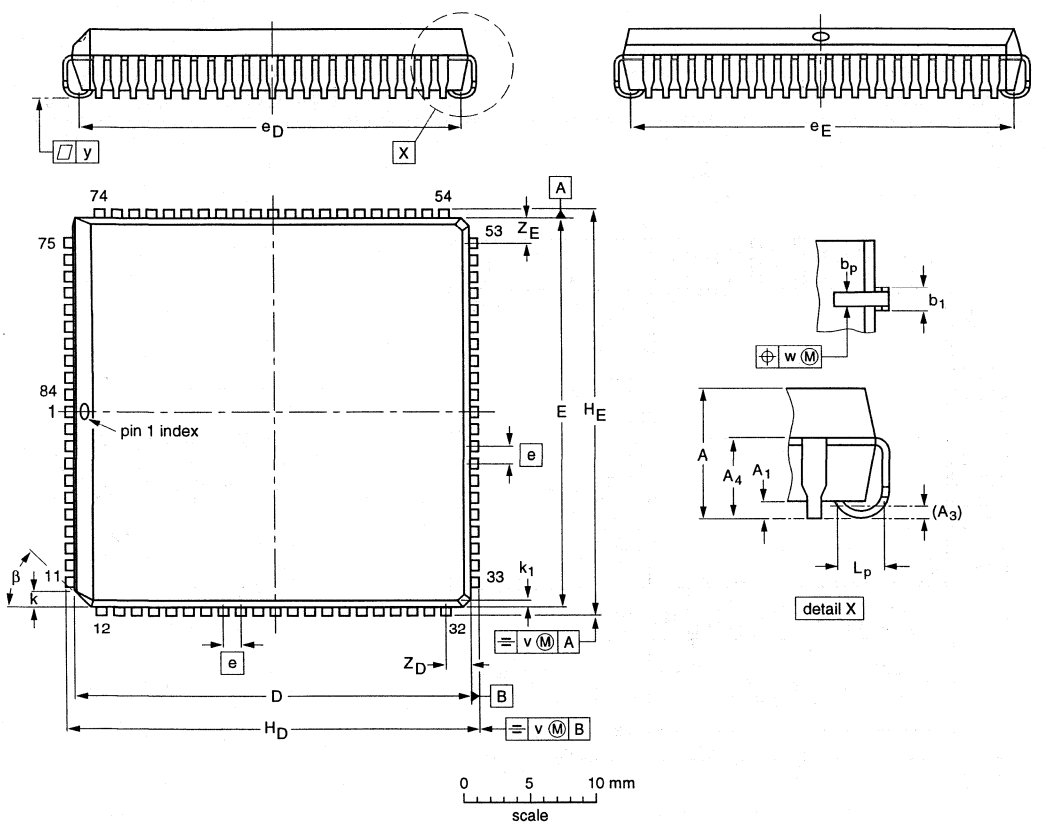
UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	k_1 max.	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.30	0.53 0.33	0.81 0.66	24.33 24.13	24.33 24.13	1.27	23.62 22.61	23.62 22.61	25.27 25.02	25.27 25.02	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.13	0.021 0.013	0.032 0.026	0.958 0.950	0.958 0.950	0.05	0.930 0.890	0.930 0.890	0.995 0.985	0.995 0.985	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT188-2	112E10	MO-047AC				~~92-11-17~~ 95-03-11

PLCC84: plastic leaded chip carrier; 84 leads **SOT189-2**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	k_1 max.	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.30	0.53 0.33	0.81 0.66	29.41 29.21	29.41 29.21	1.27	28.70 27.69	28.70 27.69	30.35 30.10	30.35 30.10	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.13	0.021 0.013	0.032 0.026	1.158 1.150	1.158 1.150	0.05	1.130 1.090	1.130 1.090	1.195 1.185	1.195 1.185	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

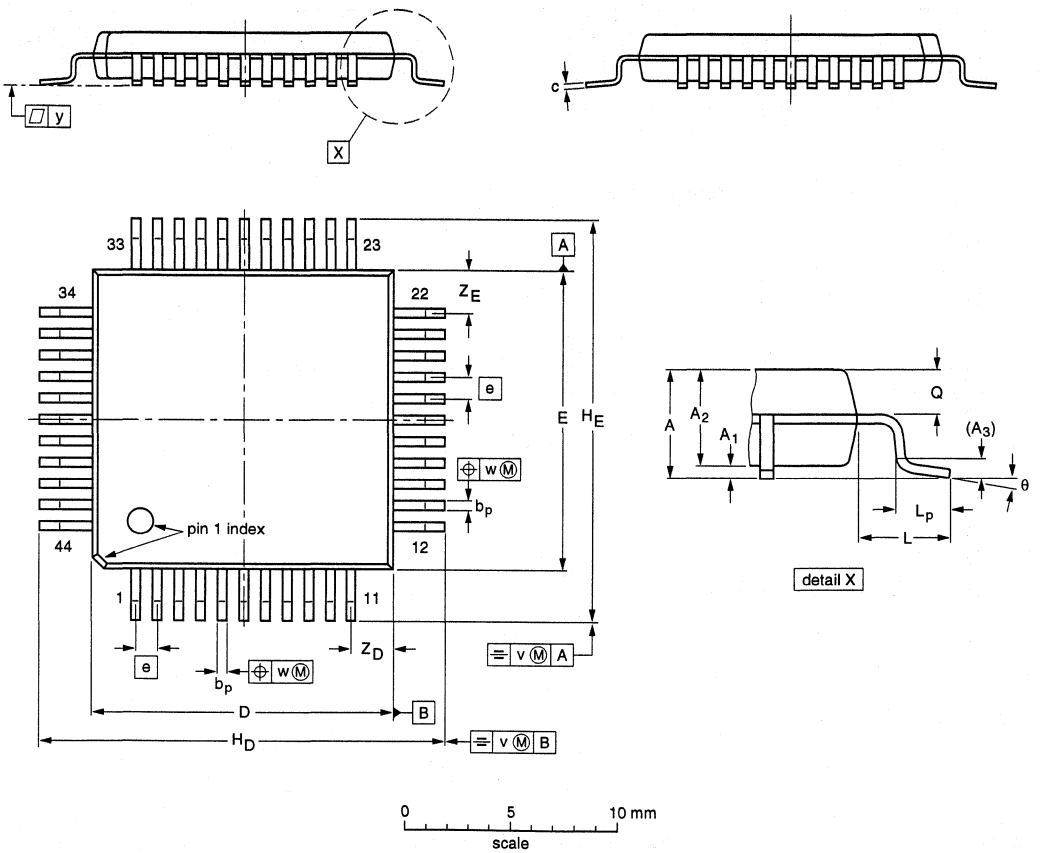
Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT189-2						~~92-11-17~~ 95-03-11

QFP

QFP44: plastic quad flat package; 44 leads (lead length 2.35 mm); body 14 x 14 x 2.2 mm SOT205-1



DIMENSIONS (mm are the original dimensions)

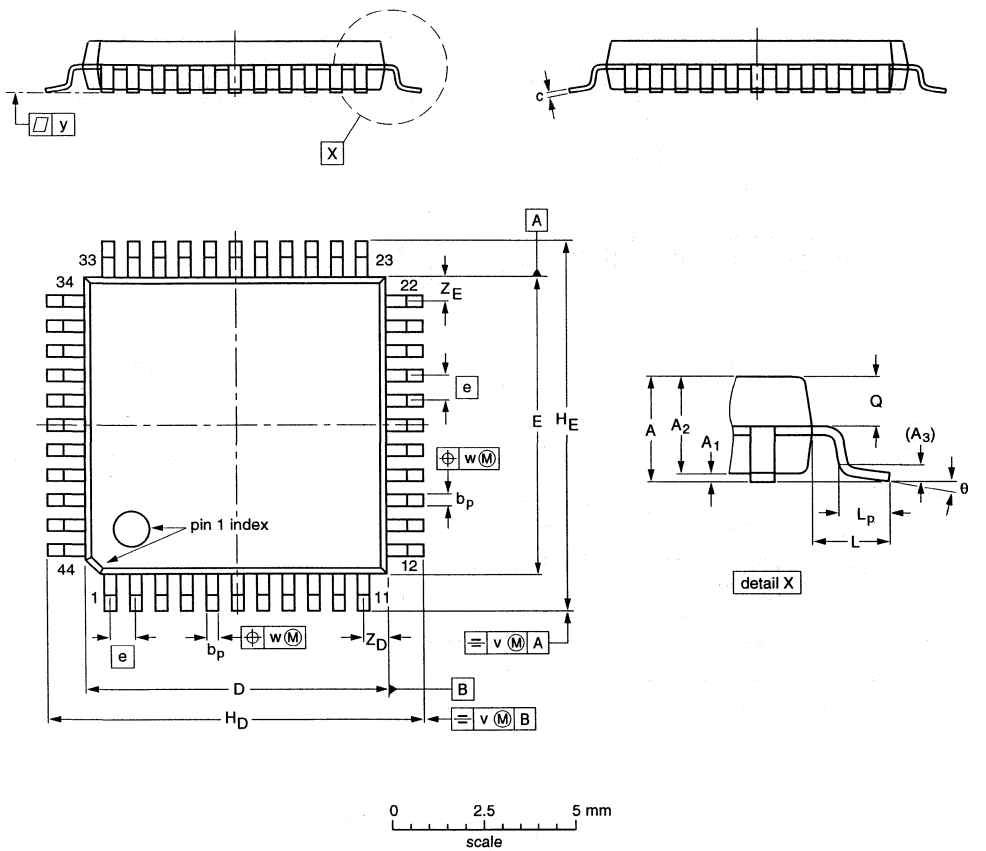
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.60	0.25 0.05	2.3 2.1	0.25	0.50 0.35	0.25 0.14	14.1 13.9	14.1 13.9	1	19.2 18.2	19.2 18.2	2.35	2.0 1.2	1.2 0.9	0.3	0.15	0.1	2.4 1.8	2.4 1.8	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT205-1	133E01A					~~92-11-17~~ 95-02-04

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm **SOT307-2**



DIMENSIONS (mm are the original dimensions)

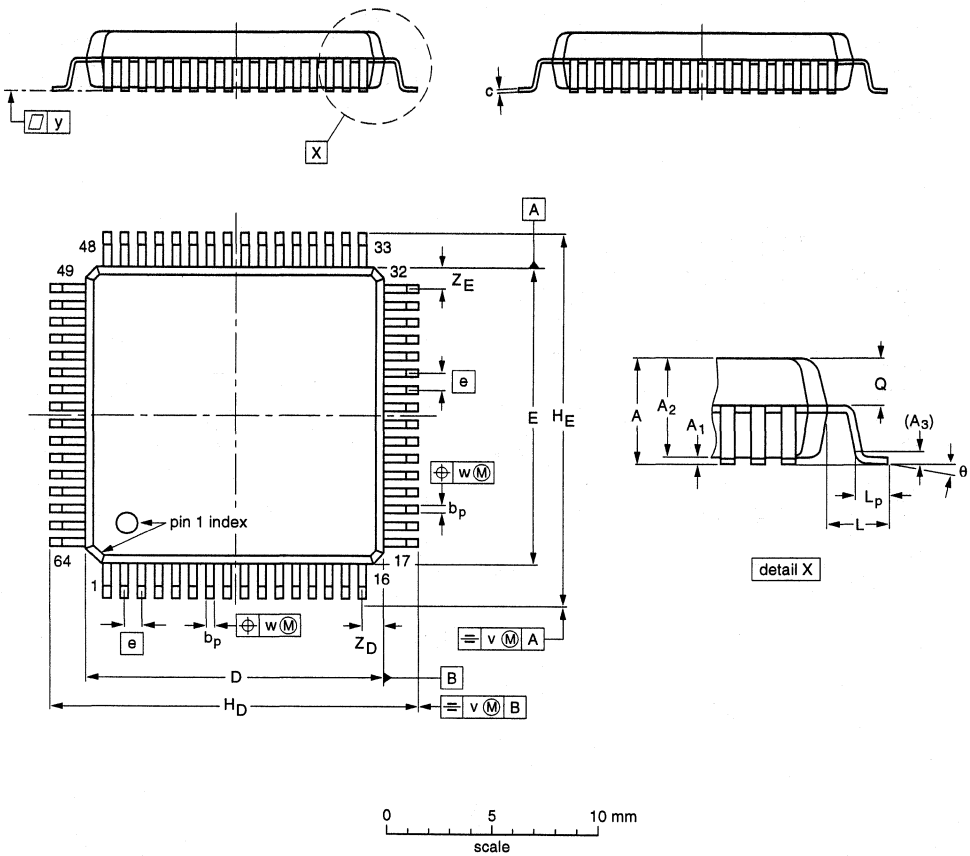
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.10	0.25 0.05	1.85 1.65	0.25	0.40 0.20	0.25 0.14	10.1 9.9	10.1 9.9	0.8	12.9 12.3	12.9 12.3	1.3	0.95 0.55	0.85 0.75	0.15	0.15	0.1	1.2 0.8	1.2 0.8	10° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT307-2						~~92-11-17~~ 95-02-04

QFP64: plastic quad flat package; 64 leads (lead length 1.6 mm); body 14 x 14 x 2.7 mm **SOT393-1**



DIMENSIONS (mm are the original dimensions)

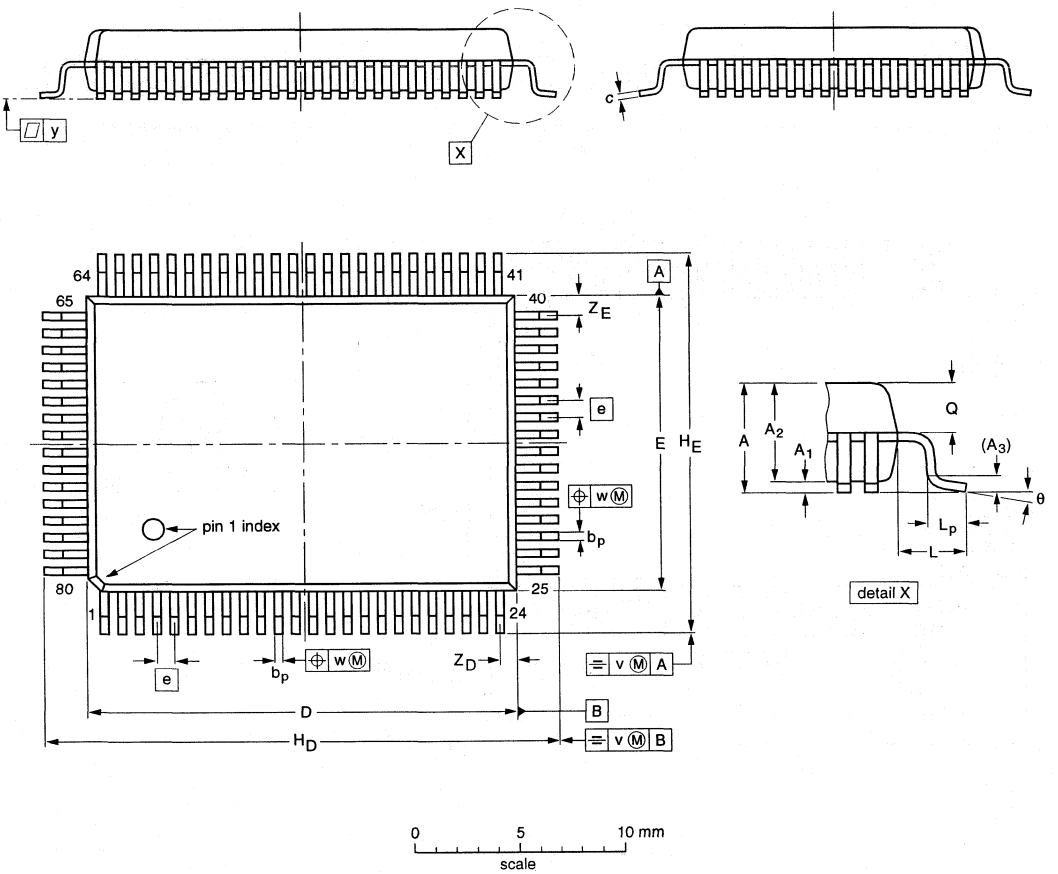
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.00	0.25 0.10	2.75 2.55	0.25	0.45 0.30	0.23 0.13	14.1 13.9	14.1 13.9	0.8	17.45 16.95	17.45 16.95	1.60	1.03 0.73	1.4 1.1	0.16	0.16	0.10	1.2 0.8	1.2 0.8	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT393-1		MS-022				~~94-06-22~~ 96-05-21

QFP80: plastic quad flat package; 80 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm **SOT318-2**



DIMENSIONS (mm are the original dimensions)

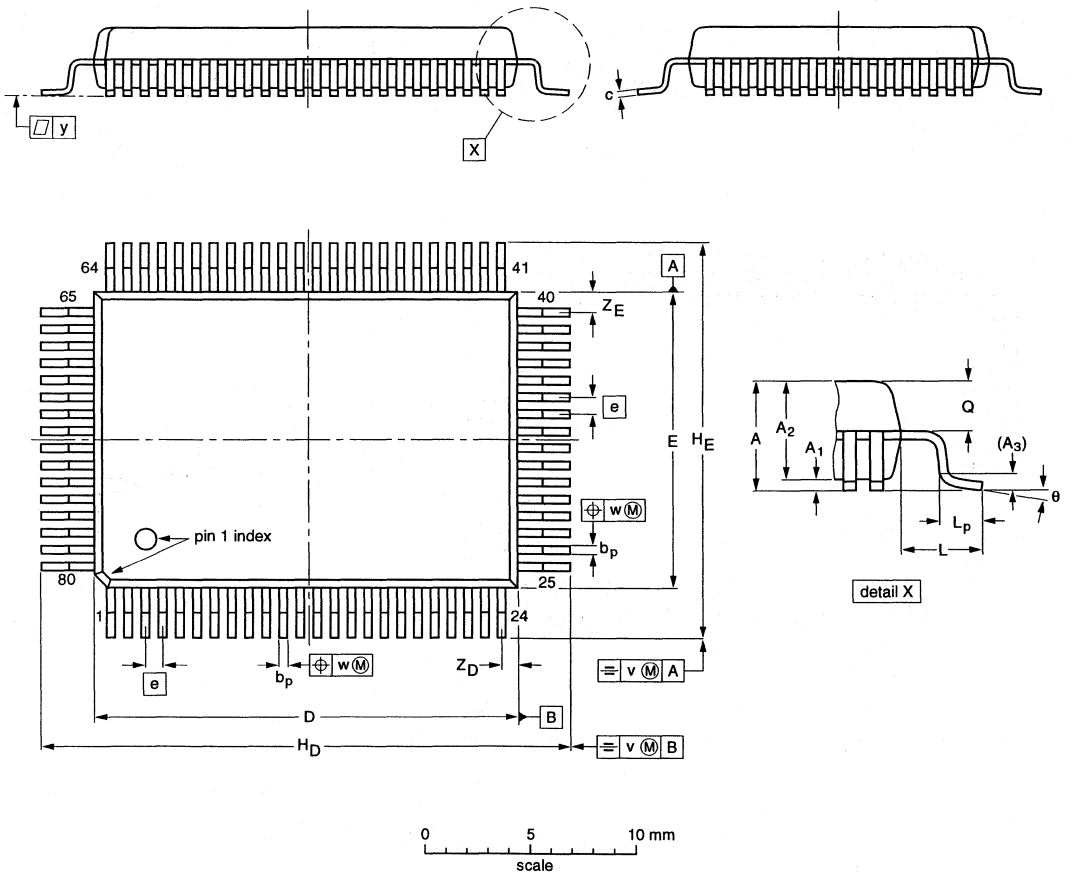
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.2	0.25 0.05	2.90 2.65	0.25	0.45 0.30	0.25 0.14	20.1 19.9	14.1 13.9	0.8	24.2 23.6	18.2 17.6	1.95	1.0 0.6	1.4 1.2	0.2	0.2	0.1	1.0 0.6	1.2 0.8	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT318-2						~~92-12-15~~ 95-02-04

QFP80: plastic quad flat package; 80 leads (lead length 2.35 mm); body 14 x 20 x 2.8 mm **SOT318-3**



DIMENSIONS (mm are the original dimensions)

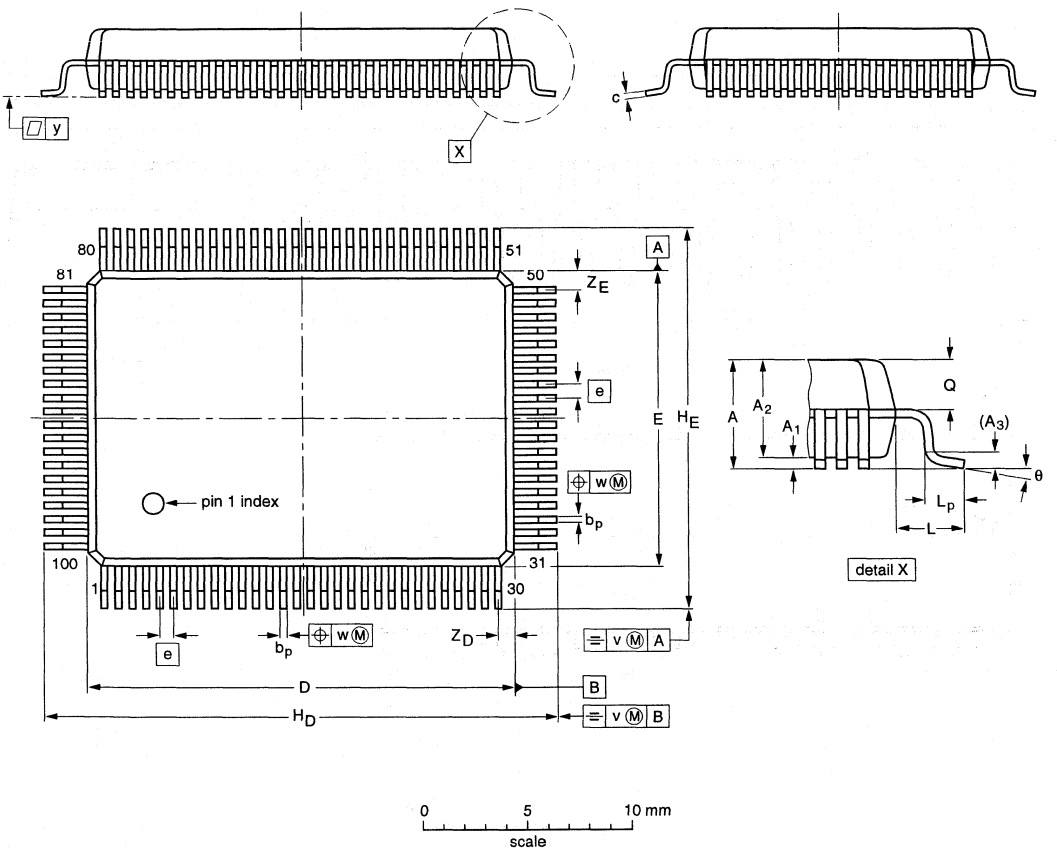
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.25	0.30 0.10	2.90 2.65	0.25	0.45 0.30	0.25 0.14	20.1 19.9	14.1 13.9	0.8	25.0 24.4	19.0 18.4	2.35	1.4 1.0	1.4 1.2	0.2	0.2	0.1	1.0 0.6	1.2 0.8	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT318-3						~~95-02-04~~ 95-04-25

QFP100: plastic quad flat package;
100 leads (lead length 1.95 mm); body 14 x 20 x 2.7 mm; high stand-off height **SOT317-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.3	0.36 0.10	2.87 2.57	0.25	0.40 0.25	0.25 0.13	20.1 19.9	14.1 13.9	0.65	24.2 23.6	18.2 17.6	1.95	1.0 0.6	1.43 1.23	0.2	0.15	0.1	0.8 0.4	1.0 0.6	7° 0°

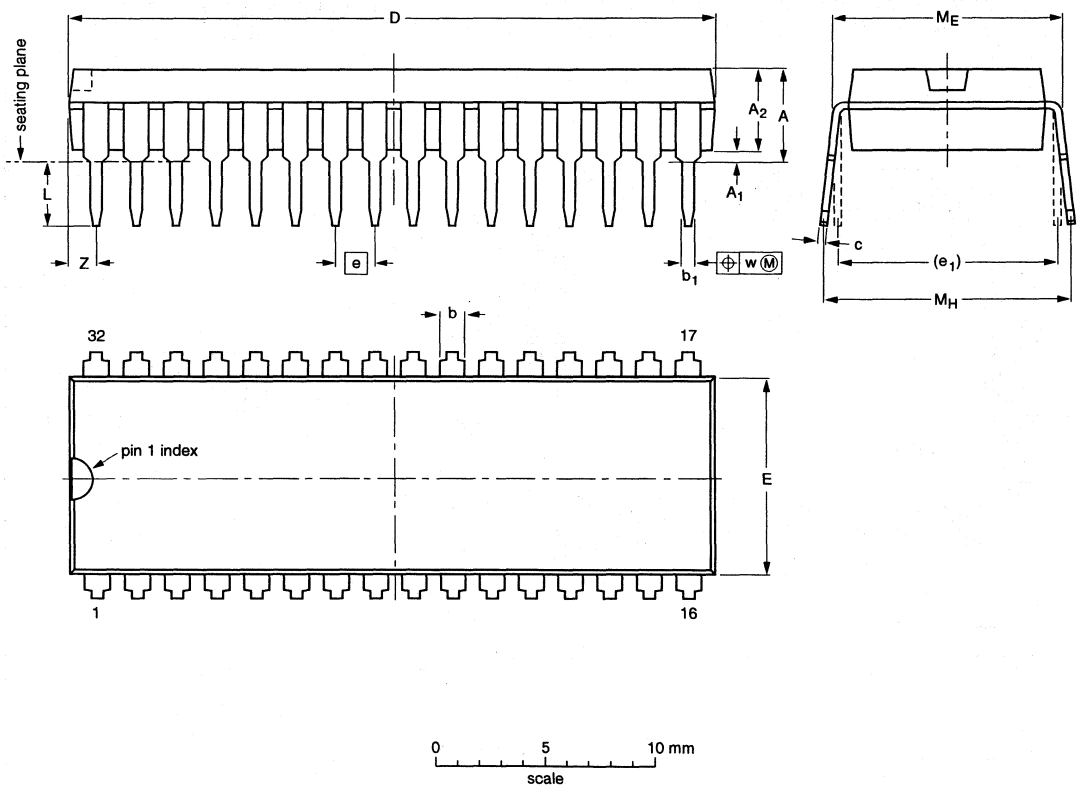
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT317-1						~~92-11-17~~ 95-02-04

SDIP

SDIP32: plastic shrink dual in-line package; 32 leads (400 mil) SOT232-1



DIMENSIONS (mm are the original dimensions)

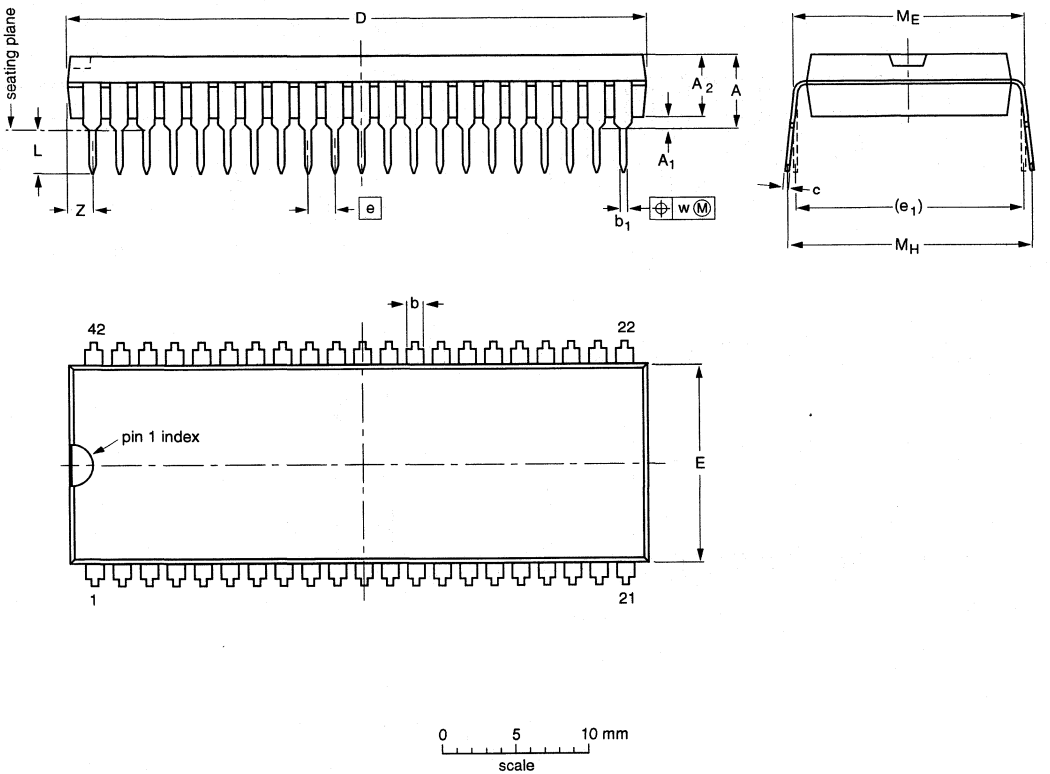
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.8	1.3 0.8	0.53 0.40	0.32 0.23	29.4 28.5	9.1 8.7	1.778	10.16	3.2 2.8	10.7 10.2	12.2 10.5	0.18	1.6

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT232-1						~~92-11-17~~ 95-02-04

SDIP42: plastic shrink dual in-line package; 42 leads (600 mil) **SOT270-1**



DIMENSIONS (mm are the original dimensions)

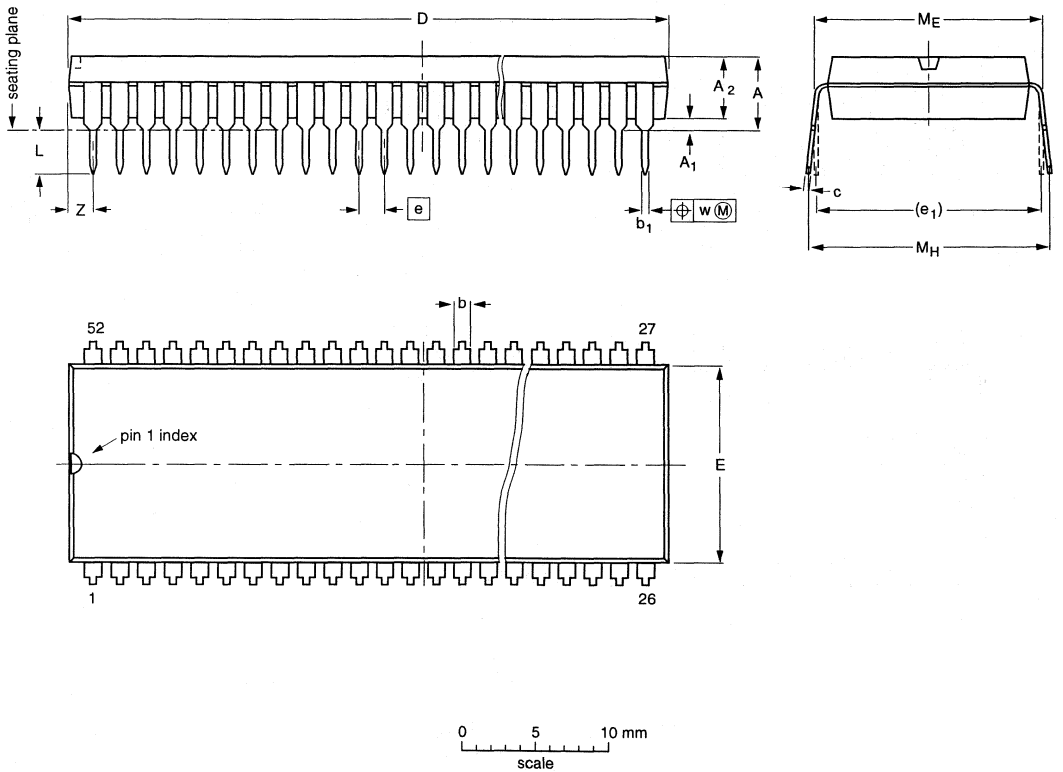
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.08	0.51	4.0	1.3 0.8	0.53 0.40	0.32 0.23	38.9 38.4	14.0 13.7	1.778	15.24	3.2 2.9	15.80 15.24	17.15 15.90	0.18	1.73

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT270-1						~~90-02-13~~ 95-02-04

SDIP52: plastic shrink dual in-line package; 52 leads (600 mil) **SOT247-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.08	0.51	4.0	1.3 0.8	0.53 0.40	0.32 0.23	47.9 47.1	14.0 13.7	1.778	15.24	3.2 2.8	15.80 15.24	17.15 15.90	0.18	1.73

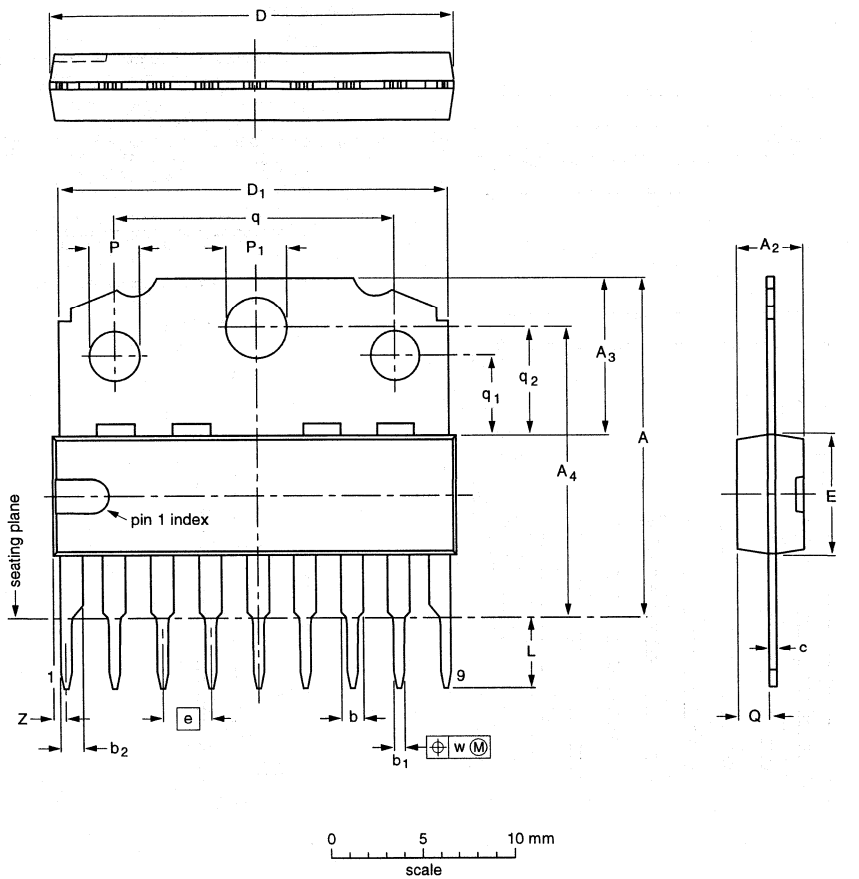
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT247-1						~~90-01-22~~ 95-03-11

SIL

SIL9MPF: plastic single in-line medium power package with fin; 9 leads SOT110-1



DIMENSIONS (mm are the original dimensions)

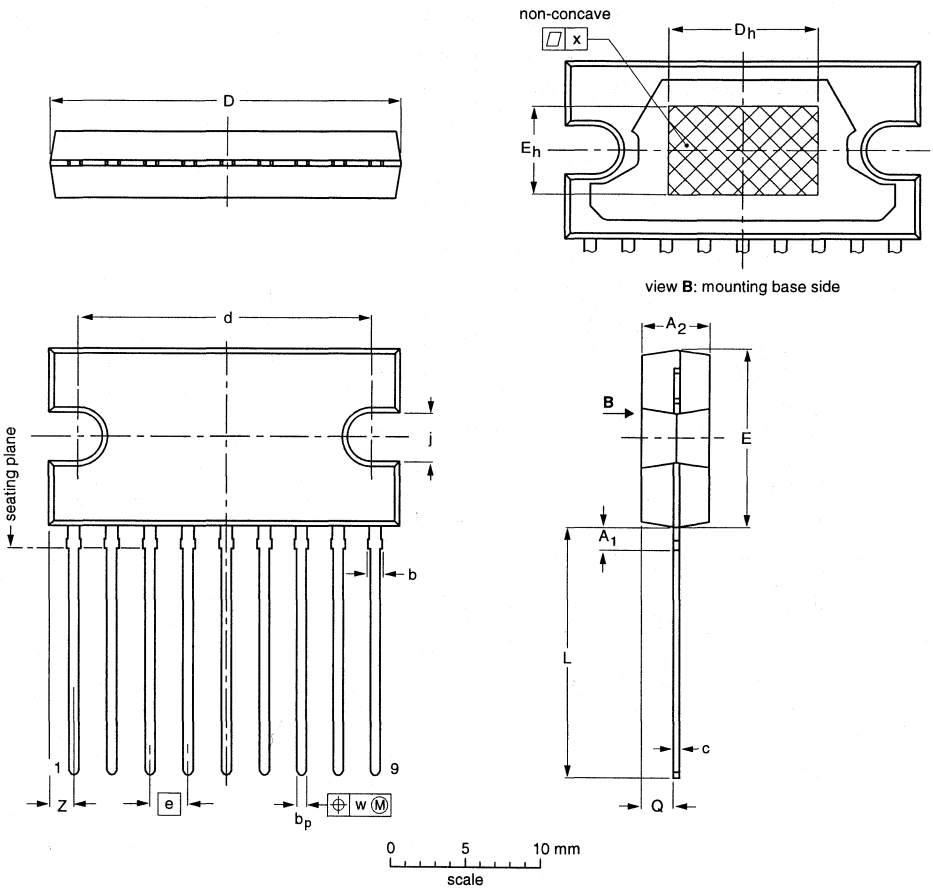
UNIT	A	A_2 max.	A_3	A_4	b	b_1	b_2	c	$D^{(1)}$	D_1	$E^{(1)}$	e	L	P	P_1	Q	q	q_1	q_2	w	$Z^{(1)}$ max.
mm	18.5 17.8	3.7	8.7 8.0	15.8 15.4	1.40 1.14	0.67 0.50	1.40 1.14	0.48 0.38	21.8 21.4	21.4 20.7	6.48 6.20	2.54	3.9 3.4	2.75 2.50	3.4 3.2	1.75 1.55	15.1 14.9	4.4 4.2	5.9 5.7	0.25	1.0

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT110-1						~~92-11-17~~ 95-02-25

SIL9P: plastic single in-line power package; 9 leads **SOT131-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A_1 max.	A_2	b max.	b_p	c	$D^{(1)}$	d	D_h	$E^{(1)}$	e	E_h	j	L	Q	w	x	$Z^{(1)}$
mm	2.0	4.6 4.2	1.1	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	2.54	6	3.4 3.1	17.2 16.5	2.1 1.8	0.25	0.03	2.00 1.45

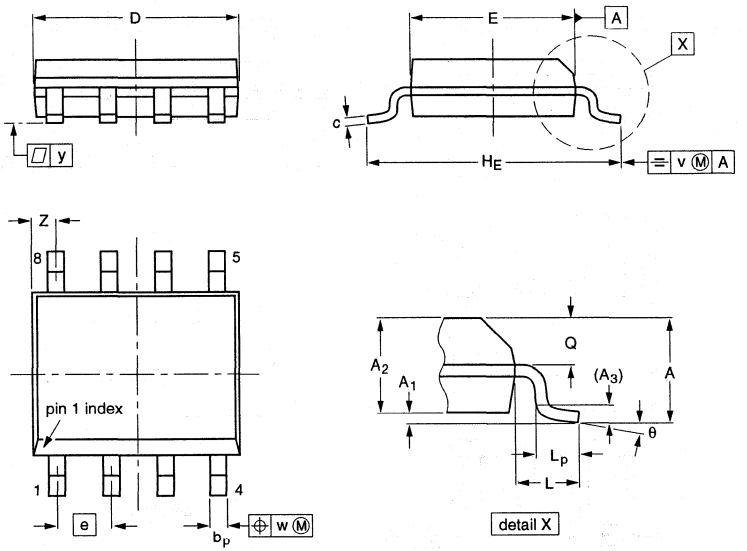
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT131-2						~~92-11-17~~ 95-03-11

SO

SO8: plastic small outline package; 8 leads; body width 3.9 mm SOT96-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

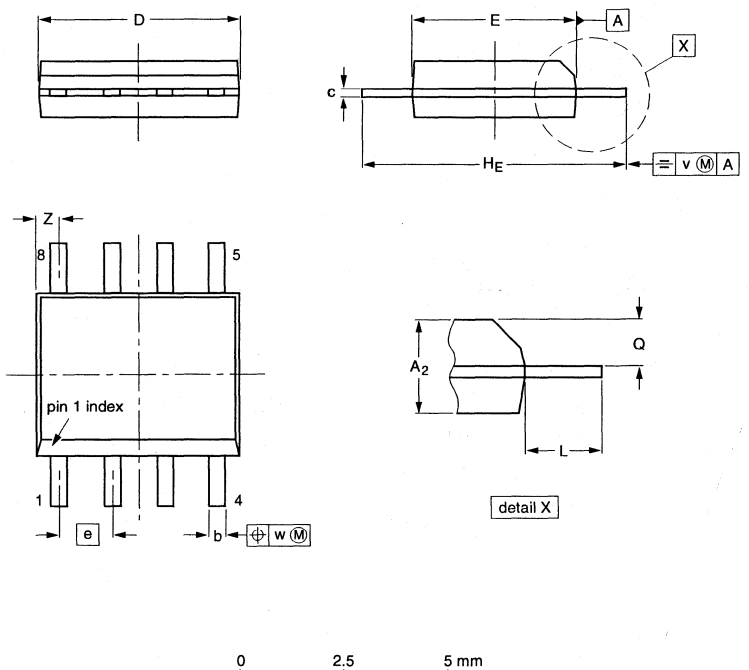
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.20 0.19	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03S	MS-012AA				~~92-11-17~~ 95-02-04

SO8: plastic small outline package; 8 leads (straight); body width 3.9 mm **SOT96-2**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

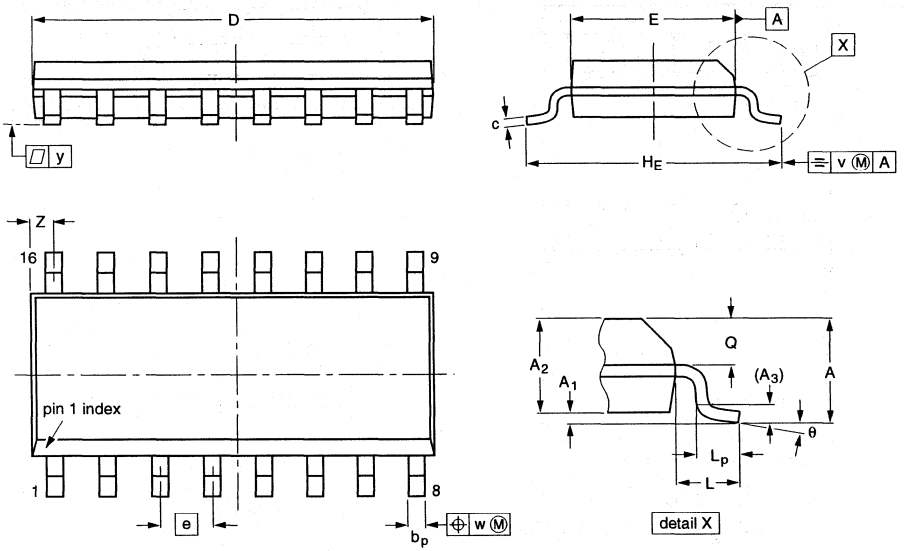
UNIT	A_2	b	c	D(1)	E(2)	e	H_E	L	Q	v	w	Z(1)
mm	1.45 1.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.4 6.2	1.2	0.7 0.6	0.25	0.25	0.7 0.3
inches	0.057 0.049	0.019 0.014	0.0098 0.0075	0.20 0.19	0.16 0.15	0.050	0.025 0.024	0.047	0.028 0.024	0.01	0.01	0.028 0.012

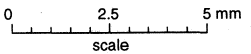
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-2						~~92-11-17~~ 95-02-04

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

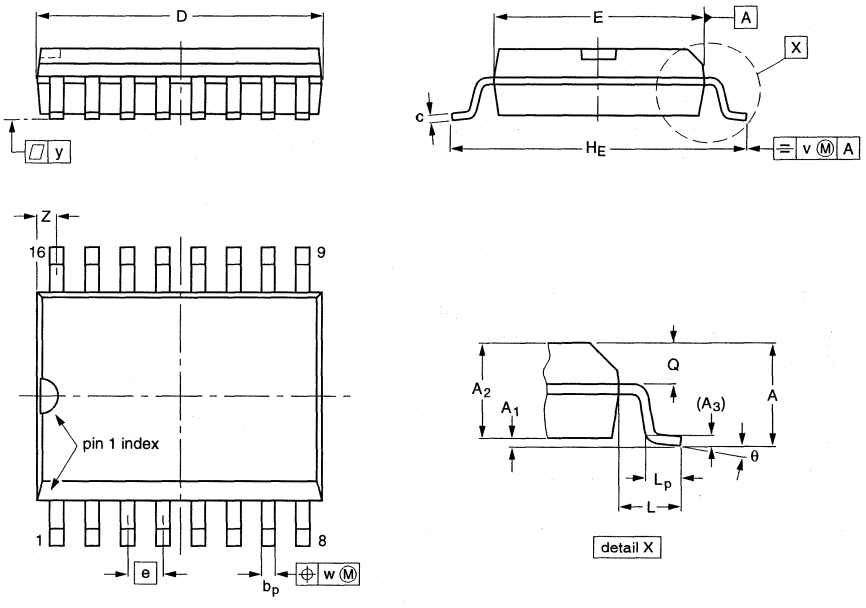
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.39 0.38	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				~~91-08-13~~ 95-01-23

SO16: plastic small outline package; 16 leads; body width 7.5 mm **SOT162-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

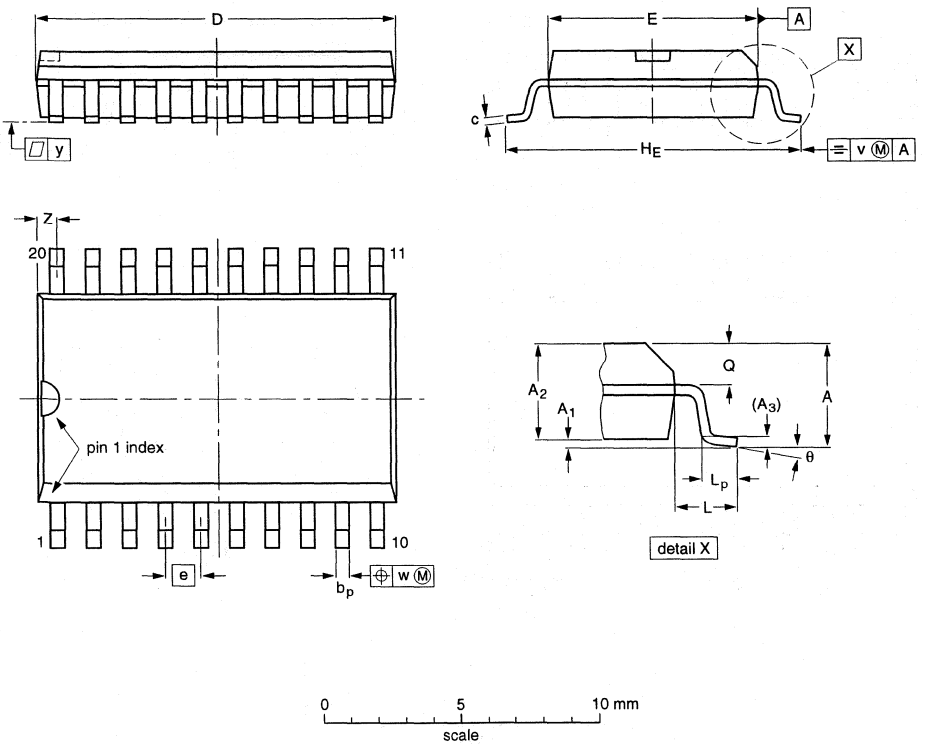
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT162-1	075E03	MS-013AA				~~92-11-17~~ 95-01-24

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

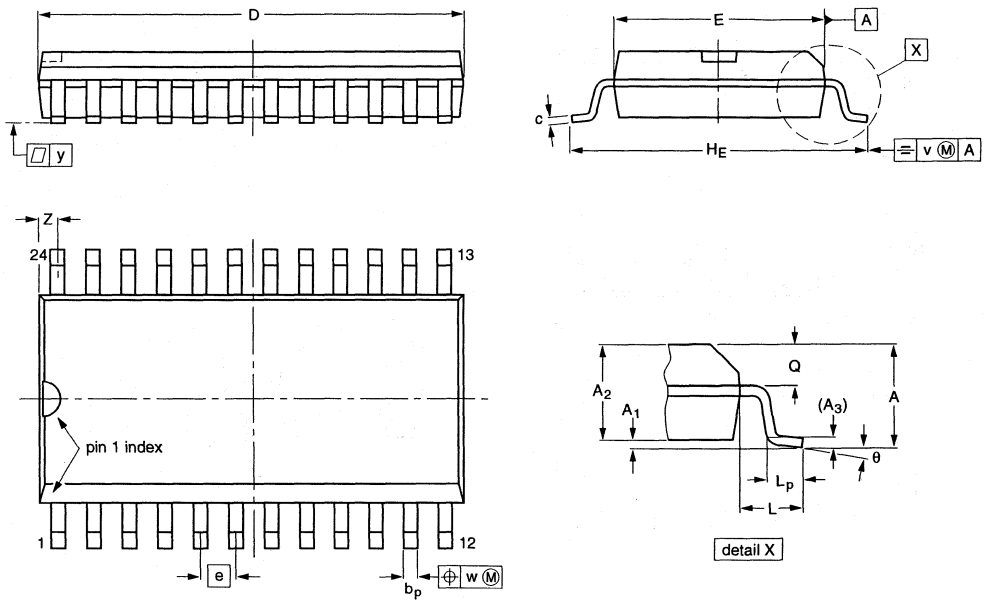
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~92-11-17~~ 95-01-24

SO24: plastic small outline package; 24 leads; body width 7.5 mm SOT137-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

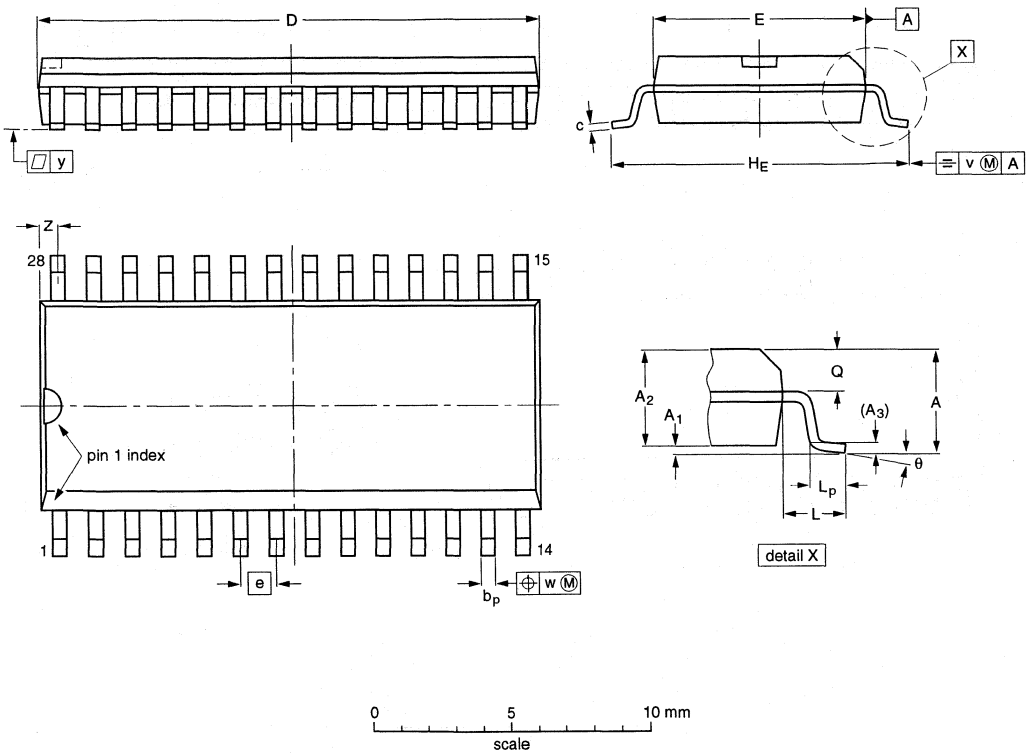
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~92-11-17~~ 95-01-24

SO28: plastic small outline package; 28 leads; body width 7.5 mm **SOT136-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

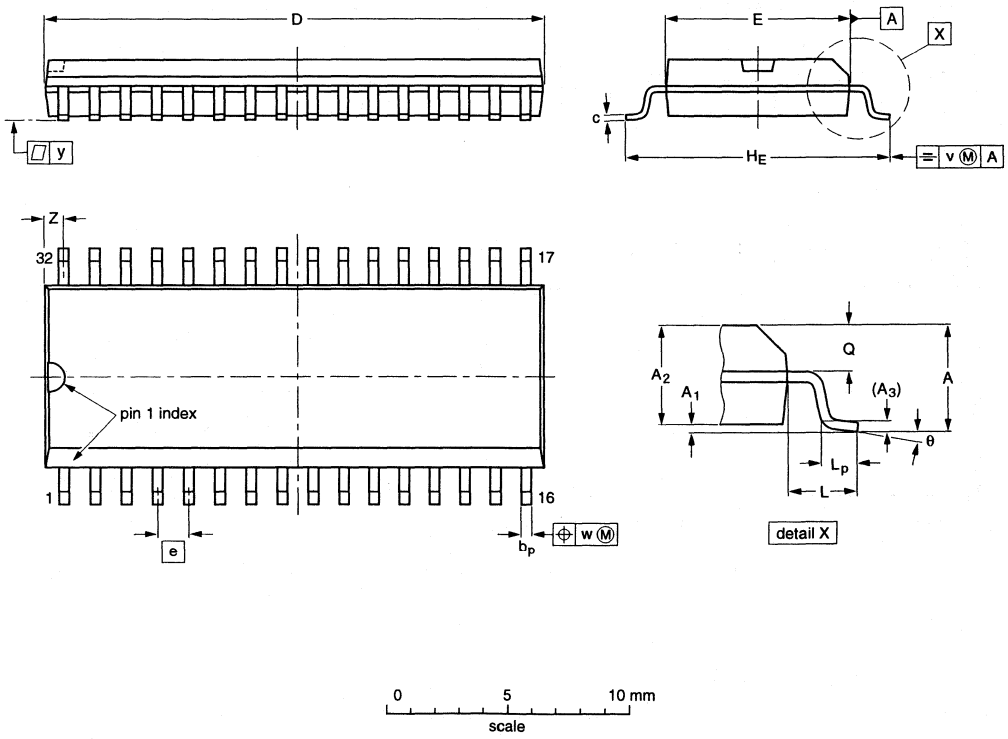
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	18.1 17.7	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.71 0.69	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT136-1	075E06	MS-013AE				~~91-08-13~~ 95-01-24

SO32: plastic small outline package; 32 leads; body width 7.5 mm SOT287-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.27 0.18	20.7 20.3	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.2 1.0	0.25	0.25	0.1	0.95 0.55	8° 0°
inches	0.10	0.012 0.004	0.096 0.086	0.01	0.02 0.01	0.011 0.007	0.81 0.80	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.047 0.039	0.01	0.01	0.004	0.037 0.022	

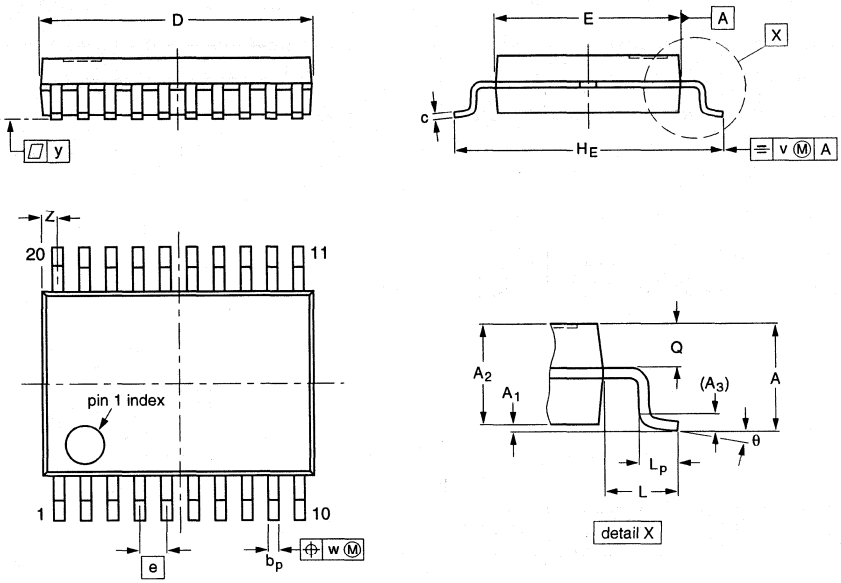
Note

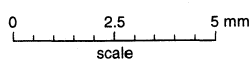
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT287-1						~~92-11-17~~ 95-01-25

SSOP

SSOP20: plastic shrink small outline package; 20 leads; body width 4.4 mm SOT266-1





DIMENSIONS (mm are the original dimensions)

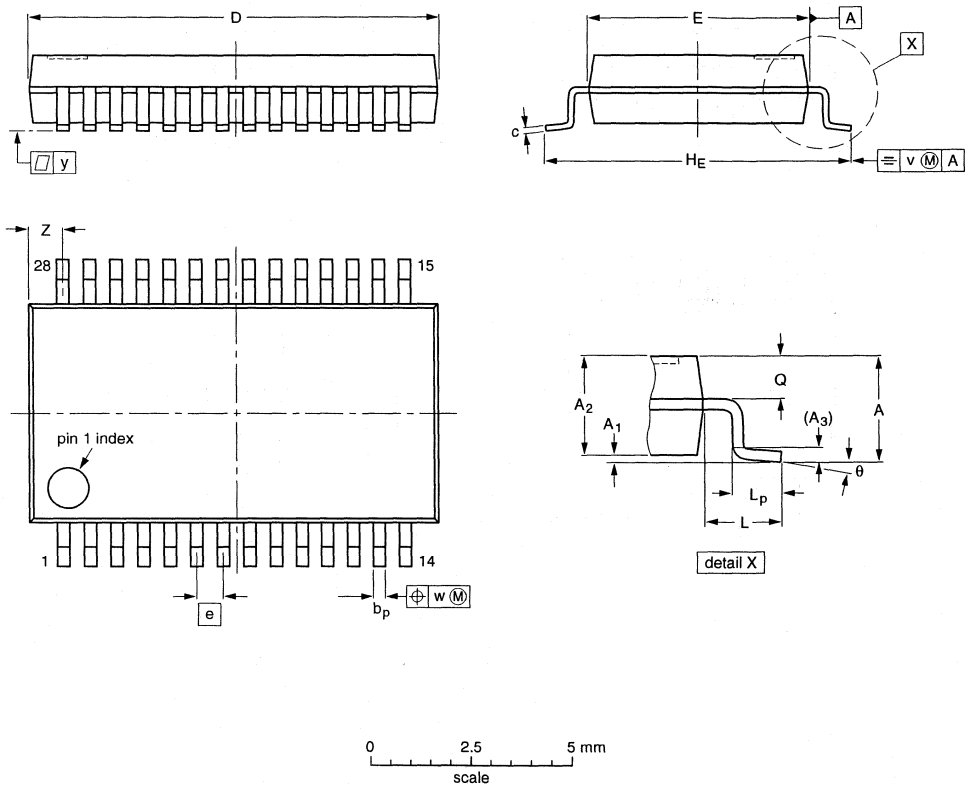
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.5	0.15 0	1.4 1.2	0.25	0.32 0.20	0.20 0.13	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT266-1							~~90-04-05~~ 95-02-25

SSOP28: plastic shrink small outline package; 28 leads; body width 5.3 mm **SOT341-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	10.4 10.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.1 0.7	8° 0°

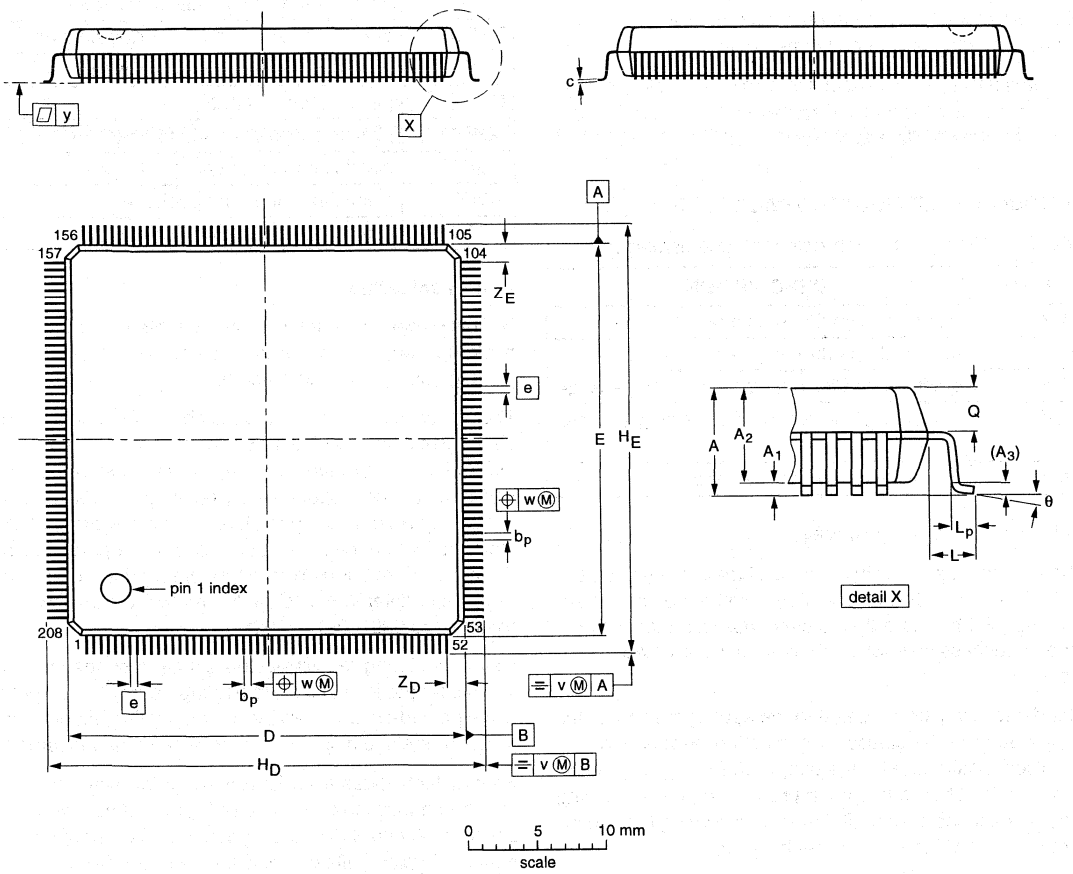
Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT341-1		MO-150AH				~~93-09-08~~ 95-02-04

SQFP

SQFP208: plastic shrink quad flat package;
208 leads (lead length 1.95 mm); body 28 x 28 x 3.4 mm **SOT316-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	4.10	0.40 0.25	3.70 3.15	0.25	0.25 0.13	0.23 0.13	28.1 27.9	28.1 27.9	0.5	30.9 30.3	30.9 30.3	1.3	0.70 0.45	1.70 1.55	0.1	0.1	0.075	1.45 1.05	1.45 1.05	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT316-1						~~93-08-23~~ 95-02-04

INTRODUCTION

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9397 750 0011).

THROUGH-HOLE MOUNTED PACKAGES

Table 1 Types of through-hole mounted packages

TYPE	DESCRIPTION
DIP	plastic dual in-line package
SDIP	plastic shrink dual in-line package
HDIP	plastic heat-dissipating dual in-line package
DBS	plastic dual in-line bent from a single in-line package
SIL	plastic single in-line package

Soldering by dipping or wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SURFACE MOUNTED PACKAGES

Table 2 Types of surface mounted packages

TYPE	DESCRIPTION
SO	plastic small outline package
SSOP	plastic shrink small outline package
TSSOP	plastic thin shrink small outline package
VSO	plastic very small outline package
QFP	plastic quad flat package
LQFP	plastic low profile quad flat package
SQFP	plastic shrink quad flat package
TQFP	plastic thin quad flat package
PLCC	plastic leaded chip carrier

Reflow soldering

Reflow soldering techniques are suitable for all SMD packages, ease of soldering varies with the type of package as indicated in Table 3.

The choice of heating method may be influenced by larger plastic packages (QFP or PLCC with 44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information on moisture prevention, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Table 3 Suitability of surface mounted packages for various soldering methods: rating from 'a' to 'd': **'a' indicates most suitable** (soldering is not difficult); **'d' indicates least suitable** (soldering is achievable with difficulty).

PACKAGE TYPE	REFLOW METHOD					DOUBLE WAVE METHOD
	INFRARED	HOT BELT	HOT GAS	VAPOUR PHASE	RESISTANCE	
SO	a	a	a	a	d	a
SSOP	a	a	a	c	d	c
TSSOP	b	b	b	c	d	d
VSO	b	b	a	b	a	b
QFP	b	b	a	c	a	c
LQFP	b	b	a	c	d	d
SQFP	b	b	a	c	d	d
TQFP	b	b	a	c	d	d
PLCC	c	b	b	d	d	b

Wave soldering

Wave soldering is **not** recommended for SSOP, TSSOP, QFP, LQFP, SQFP or TQFP packages, this is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- For SSOP, TSSOP and VSO packages, the longitudinal axis of the package footprint must be parallel to the solder flow **and** must incorporate solder thieves at the downstream end.
- For QFP, LQFP and TQFP packages, the footprint must be at an angle of 45° to the board direction **and** must incorporate solder thieves downstream and at the side corners.

Even with these conditions, consider wave soldering only for the following package types:

- SO
- VSO
- PLCC
- SSOP **only with body width 4.4 mm**, e.g. SSOP16 (SOT369-1) or SSOP20 (SOT266-1).
- QFP **except** QFP52 (SOT379-1), QFP100 (SOT317-1, SOT317-2, SOT382-1) and QFP160 (SOT322-1); these are **not** suitable for wave soldering.
- LQFP **except** LQFP32 (SOT401-1), LQFP48 (SOT313-1, SOT313-2), LQFP64 (SOT314-2), LQFP80 (SOT315-1); these are **not** suitable for wave soldering.
- TQFP **except** TQFP64 (SOT357-1), TQFP80 (SOT375-1) and TQFP100 (SOT386-1); these are **not** suitable for wave soldering.

SQFP are **not** suitable for wave soldering.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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Data handbook system

DATA HANDBOOK SYSTEM

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